**MIDDLE EAST TECHNICAL UNIVERSITY**

**ELECTRICAL AND ELECTRONICS ENGINEERING DEPARTMENT**



**EE463 STATIC POWER CONVERSION-II**

**PROJECT #1 REPORT**

**Due Date: 07.03.2019**

**Team Members**

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**Question 1-)**

**Part a-)**

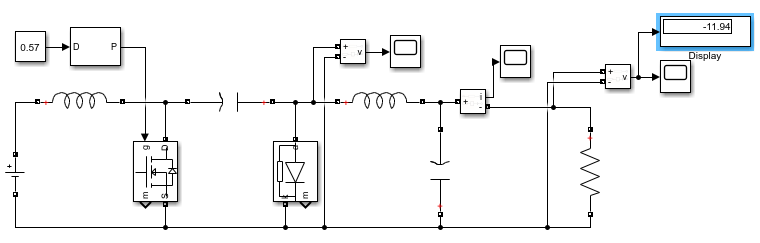


Figure 1: Cuk Converter Topology

In this part of the question, we are asked to design a Cuk converter but we are not given any values for any of the components. Hence we are going to utilize a number of specifications that are supplied beforehand. First relation to be used is output to input voltage ratio(equation-1) which is 4/3 from which D can be found as follows:

.....................................................equation-1.

* By using this relation, we can find the duty ratio(D) as %57.

Another unknown value is the resistor itself and we can find it by using the following (equation-2):

.........................................................equation-2.

* By using this relation, we can find the resistor value as 4 Ohms.

As a specification, maximum output voltage ripple is desired to be %2. For this purpose, we can utilize the ON state relations with a bunch of assumptions which are the following:

* VL2 is constant during ON state
* Output current is equal to IL2 so there is no current passing thru filter capacitor.
* Hence we can assume that ripple in the outputvoltage can be calculated by using the the change in VC1. So, the limiting element here is C1 itself.

In accordance with the above assumptions, following figure illustrates the computations to find C1 value:

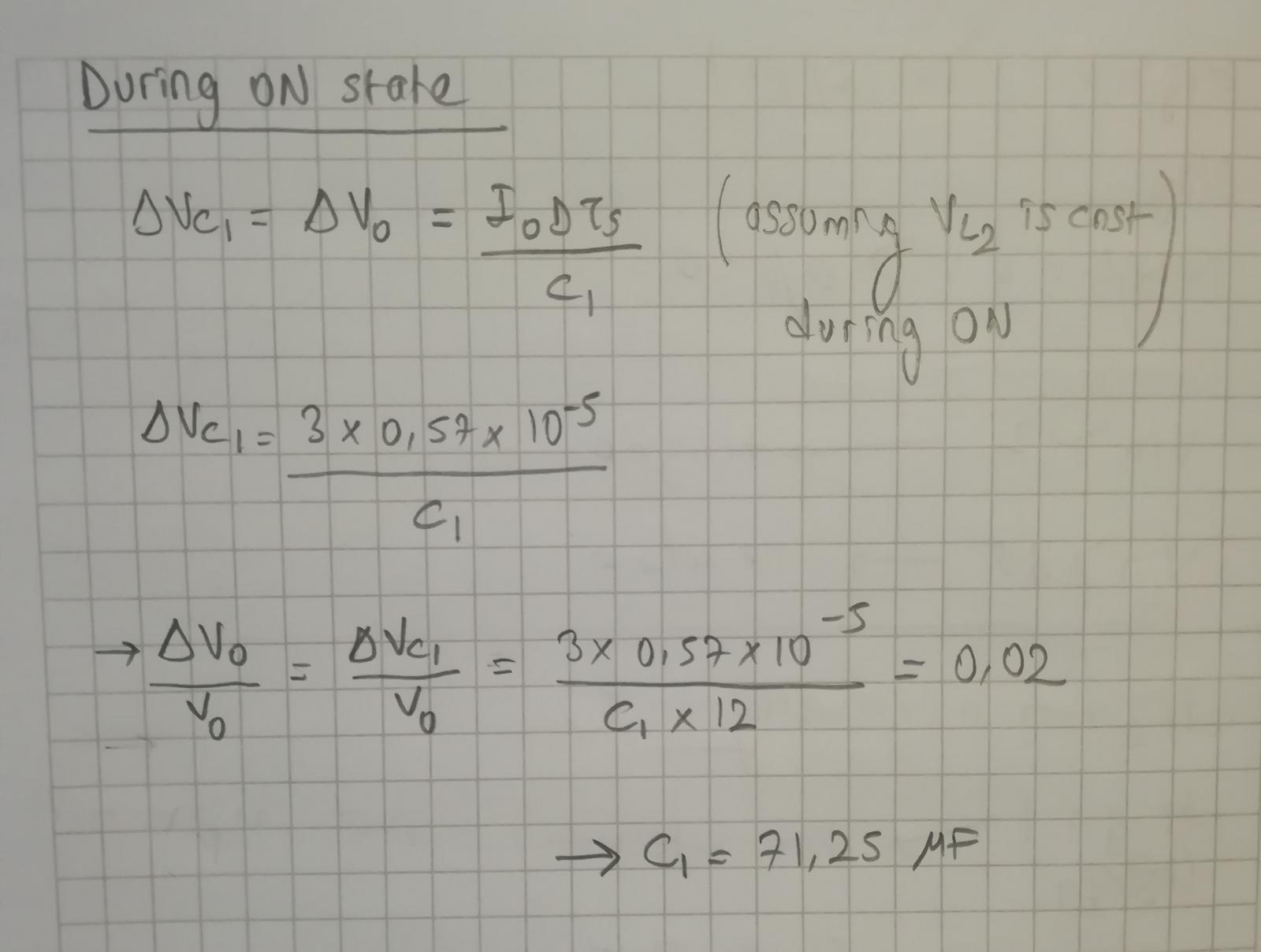


Figure 2- Computations to find the value of isolating capacitor (C1)

* The closest value available in the market for C1 is 68 uF so we are going to use it.
* Cout can be chosen smaller than C1 for example 900 nF in order not be bulky and expensive. Note that any arbitrary value for Cout will decrease output voltage ripples further since it is a filtering capacitor whose duty is exactly that.

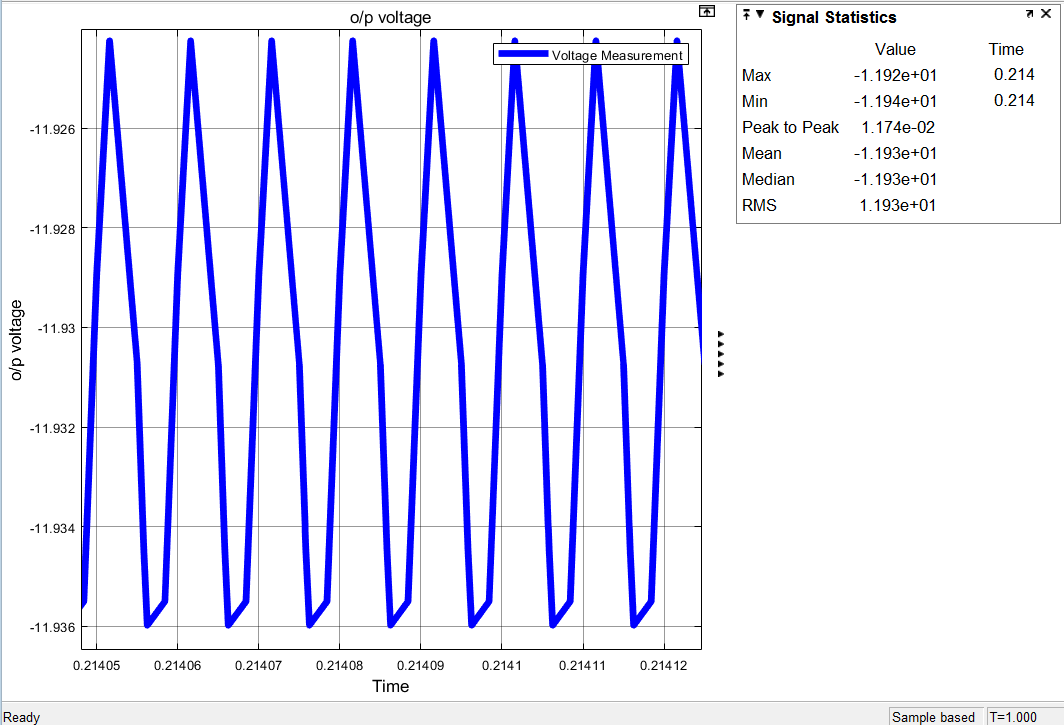


Figure 3- Output voltage characteristics

* If we look at figure-3, we can see that our voltage ripple is found to be 0.098% that is even smaller than 2% which is expected due to the existence of an additional capacitor which is filtering capacitor (Cout= 900nF)
* Also note that we have no idea about inductor current ripples and hence we cannot find the exact numerical value for inductors. However, we know that output current is expected to be constant for this converter to be performing well. Thus we can choose the inductor value as 510 uH in order to be big enough and at the same time not to be so expensive. However this choice is not completely arbitrary i.e. we must make sure that the converter is not going into DCM, for this purpose we are going to look at simulation result given in the following figure:

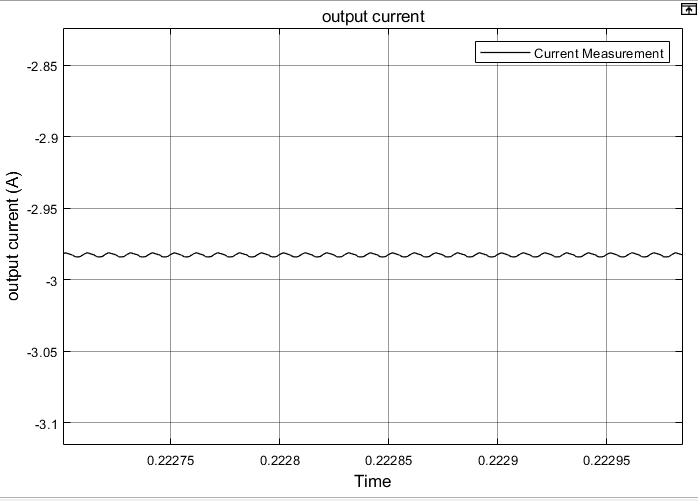


Figure 4- Inductor (L2) current characteristics

* If we look at figure 4, it is clear that the constructed converter topology is far from going into DCM, so there is no problem with the chosen inductance value

*Bonus:*

In order to find a commercial product for C1, we need the rated operation voltage induced between the terminals of it in addition to its capacitance value which is previously determined as 68uF.

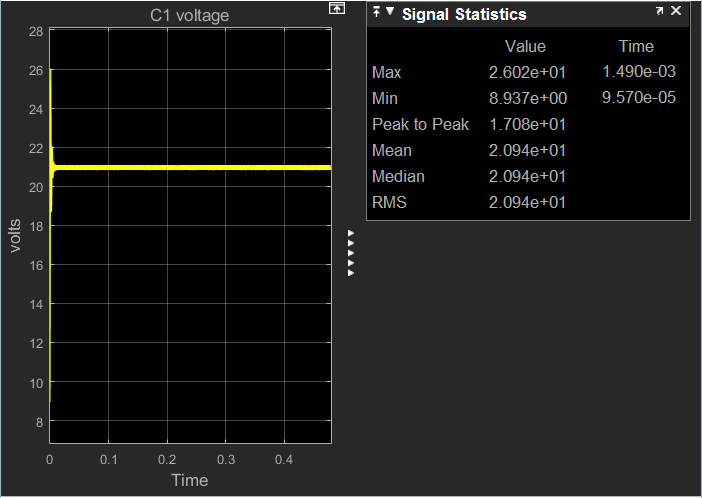


Figure - C1 voltage

* As can be seen in figure5, average voltage between the terminals of C1 equals to 21 V. However, we should take the maximum voltage induced on its terminals even if does not take so long. This maximum voltage is 26 V. To be on the safe side, we are going to choose the maximum rating above this value.
* **Chosen capacitor:** Panasonic’s 68 uF 35 V aluminium electrolytic capacitor.

For data sheet visit: *https://industrial.panasonic.com/cdbs/www-data/pdf/RDF0000/ABA0000C1022.pdf*

**Part b-)**

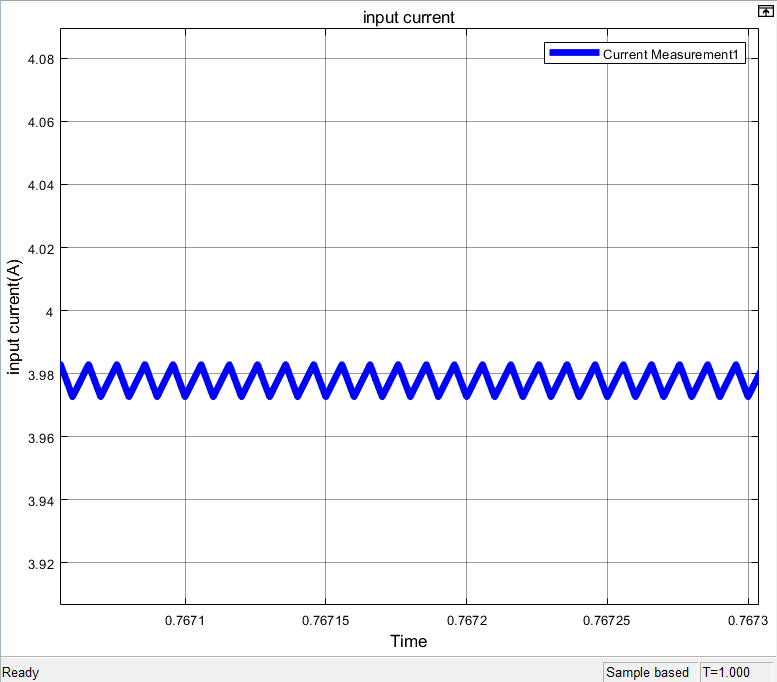


Figure 6- Input current of the Cuk converter

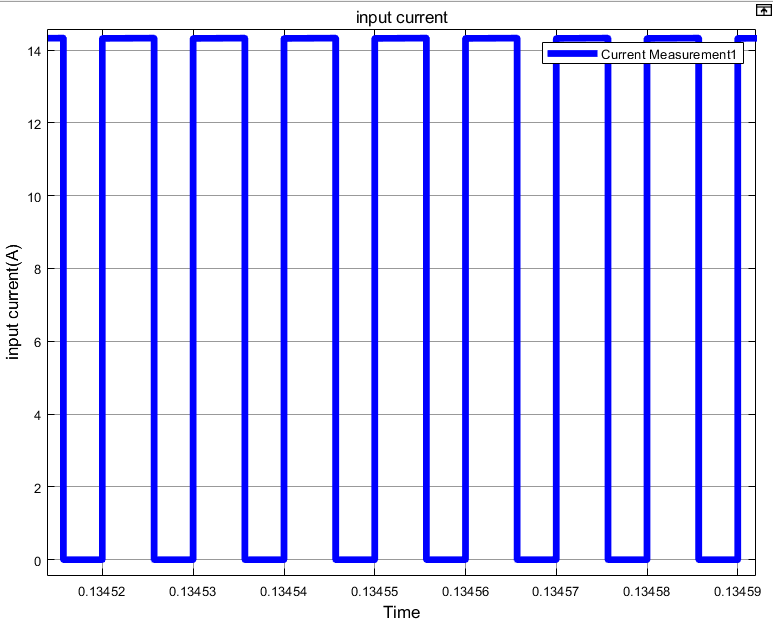


Figure 7- Input current of the Buck-boost converter

Although both topologies have the same sizes and give the same input current in average (4A), Cuk converter topology gives a much smoother waveform for the input current. This is because of Cuk converter having an inductor (L1) in the path for input current which does not exist in buck-boost topology. Hence, we observe a step waveform (discontinuous) for the input current in buck-boost topology.

**Part c-)**

In this part, we are asked to find capacitor(C1) voltage ripples and inductor (L2) ripples theoretically and also by using simulation.

* In order to find capacitor voltage ripples theoretically, we are going to utilize OFF state relations. The relevant calculations are shown in figure 7:

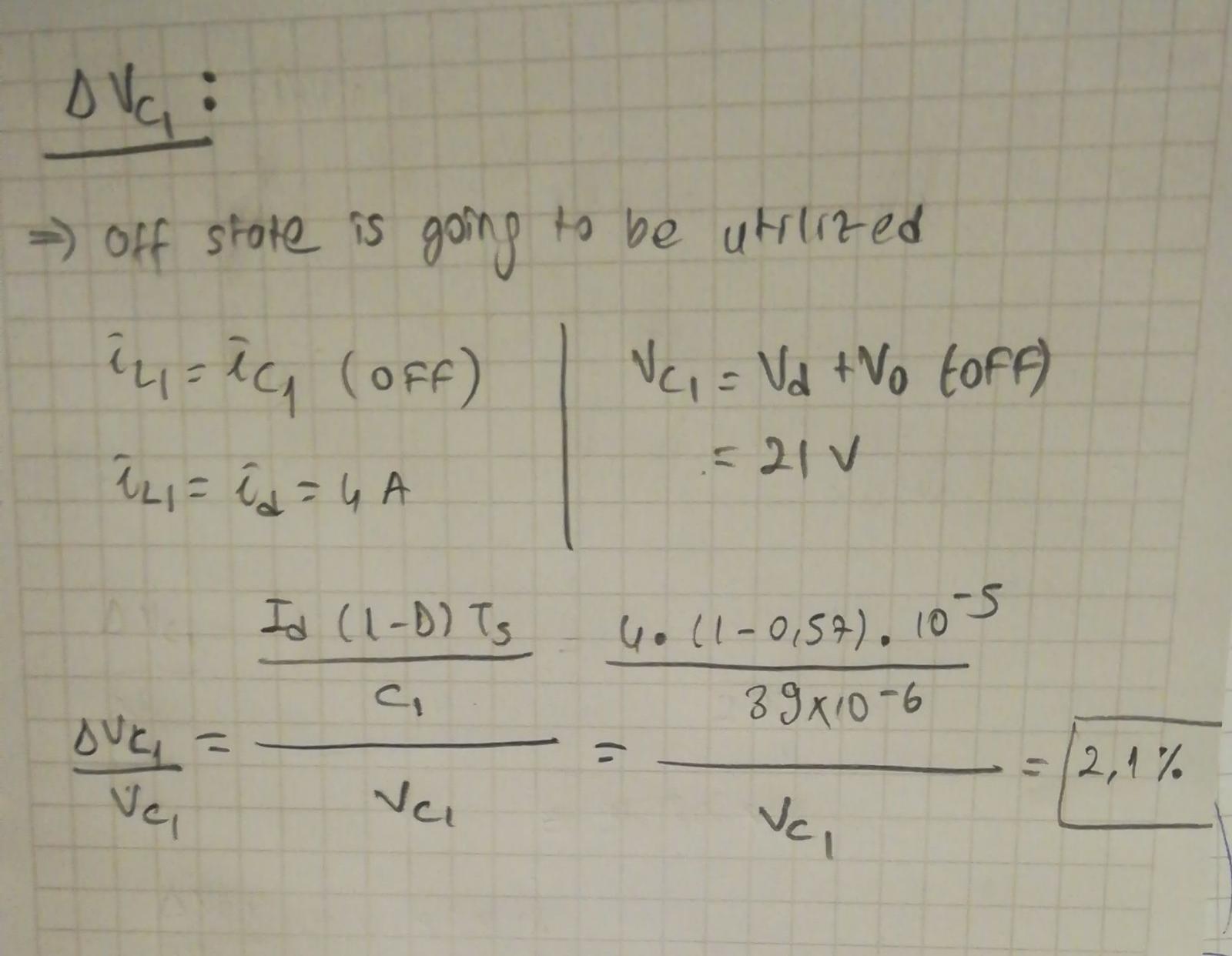


Figure 8- Computations to find Vc1 ripples

* As can be seen in figure 8, VC1 ripples are found to be 2.1%.
* Now we are going to give simulation results in figure 9 that shows VC1 ripples:

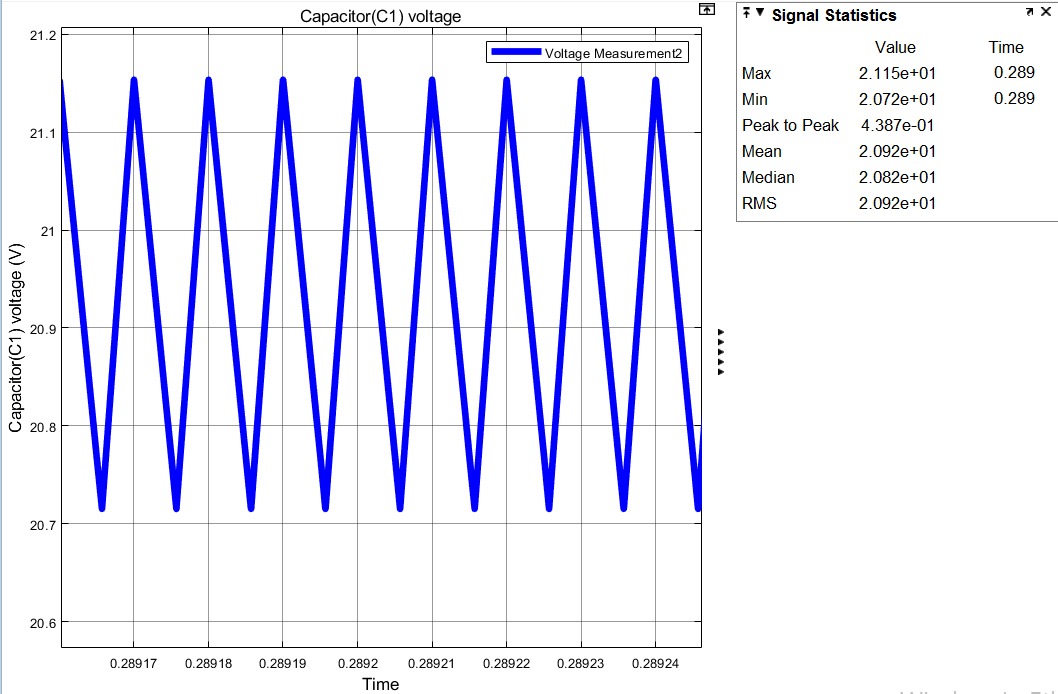


Figure 9- Simulation results of Vc1 voltage and its ripples

* As can be deduced from figure 9, VC1 ripples are found to be 2.3% which is really close to what we have found theoretically.
* In order to find inductor current ripples theoretically, we are going to utilize a number of relations. These relations and relevant calculations are shown in figure 10:

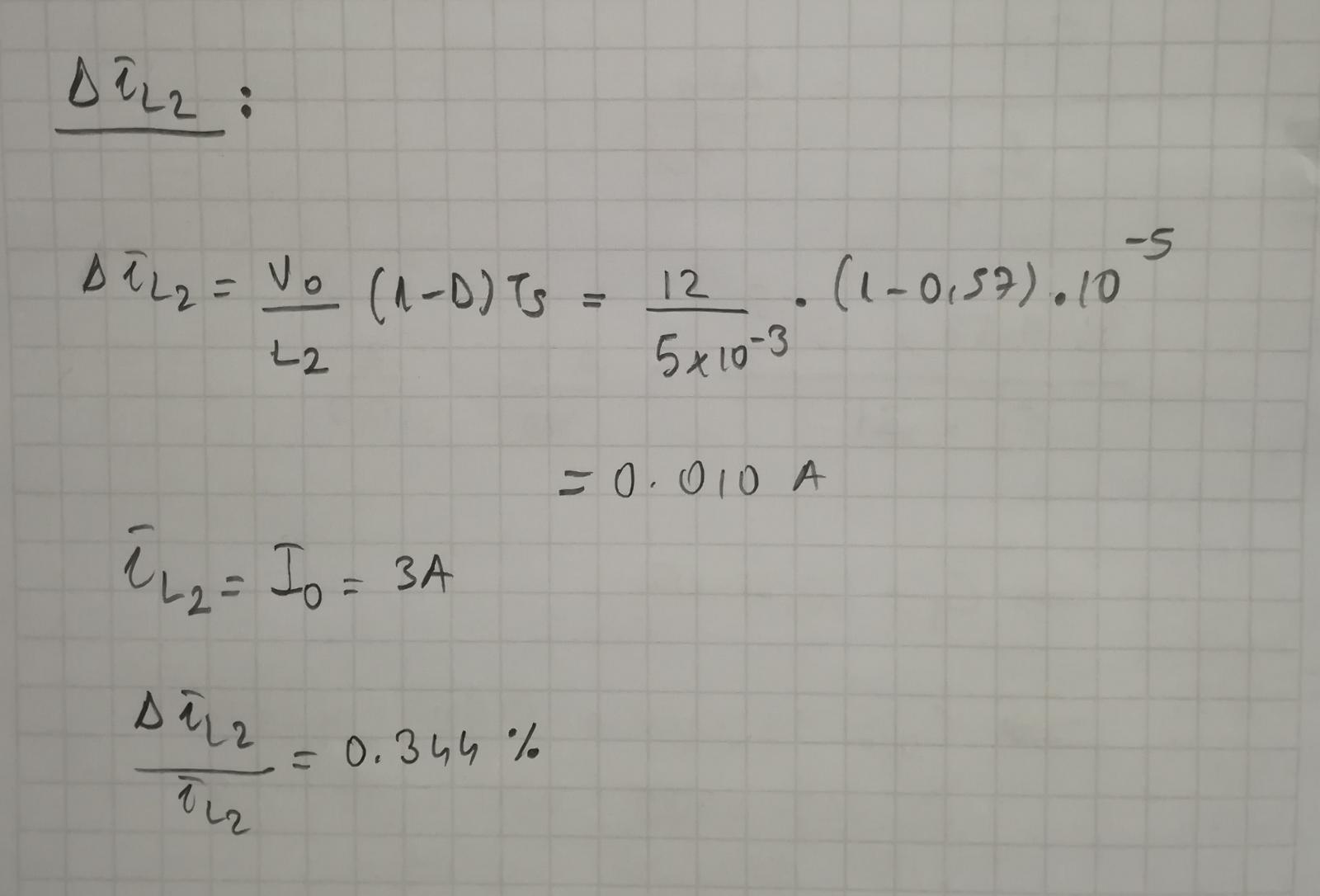


Figure 10- Computations to find IL2 ripples

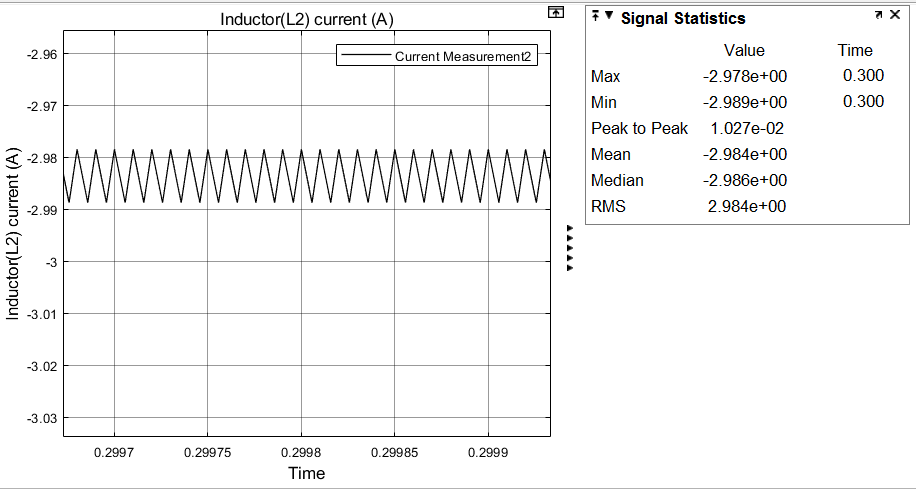


Figure 11- Simulation results of IL2 current and its ripples

* As can be deduced from figure 11, IL2 ripples are found to be 0.344% which is the exact theoretical value found above.

**Part d-)**

**Part e-)**

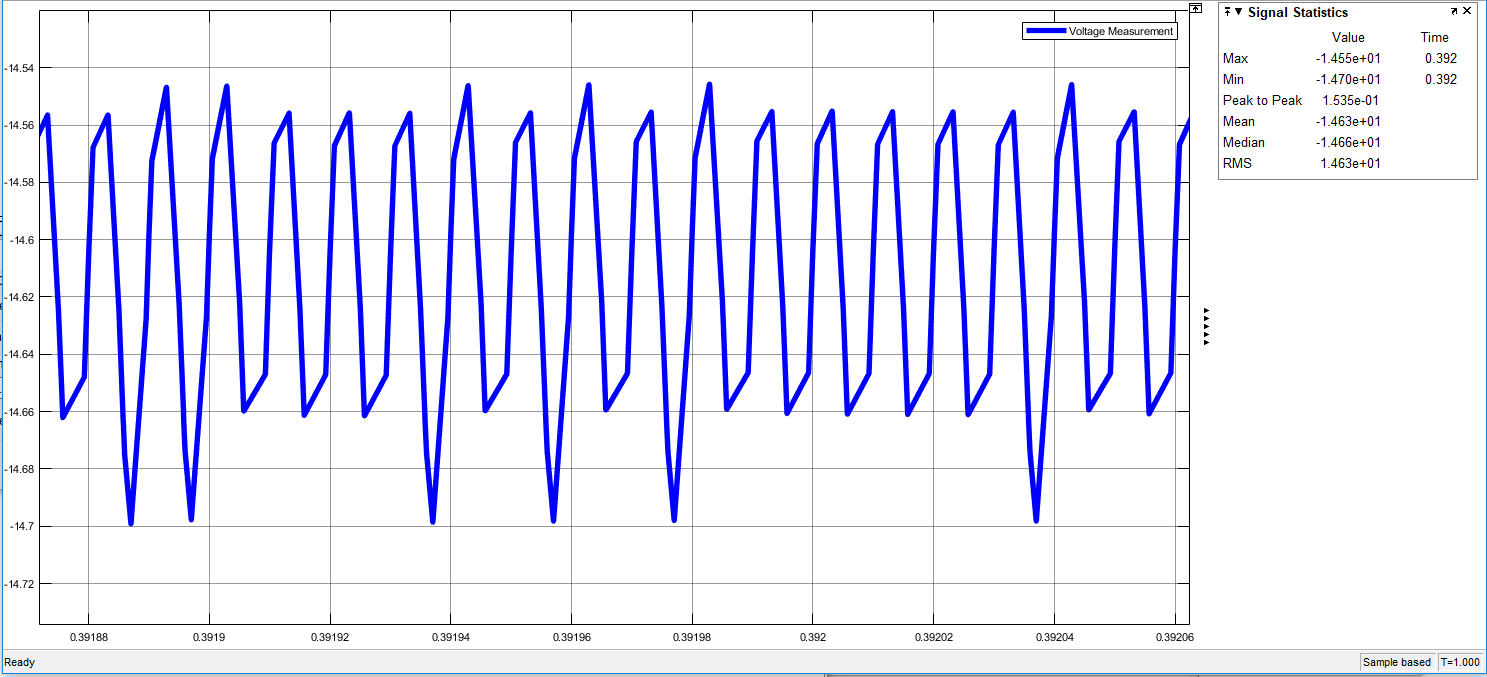


Figure : Output voltage ripple for 11V input voltage

When we looked at the figure 7, we can see output level increased to 14.6 V. Performance of controller is bad since increase of output voltage can be harmful for load. For a good controller, output voltage should not change a lot. However, voltage ripple is %1.