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PROPOSAL REPORT

INTRODUCTION

Our EE314 Laboratory project is AN FPGA BASED OSCILLOSCOPE. It is expected to design a digital oscilloscope by using FPGA board. The aim of the project work is to make us more familiar with some subject, especially Verilog coding. Also, this project makes us to be more creative. In this project, firstly, we should convert analog signal to digital signal in order to pass digital world. For this purpose, we do not need an external converter because the FPGA board has analog to digital converter chip. After converting, we need to store this data at RAM to protect the information. We do not need an external tool since FPGA board has 1GB RAM on it. Now, we should process data to create a VGA screen. At this point, we have selection module to enable user to control mode of the oscilloscope (AC-DC mode, time/div, volt/div and auto scale).

OVERALL PROJECT DIAGRAM

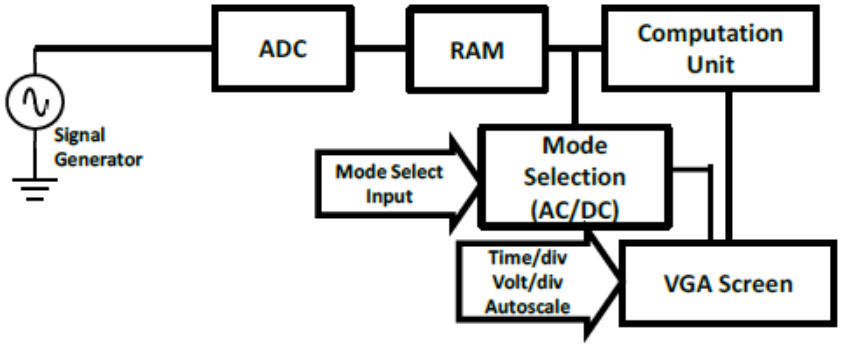

Figure 1: Overall Block Diagram

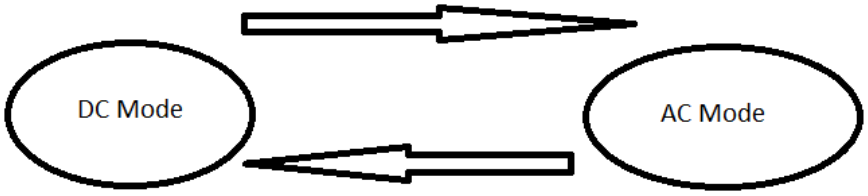

Figure 2: State diagram

PROJECT

ADC

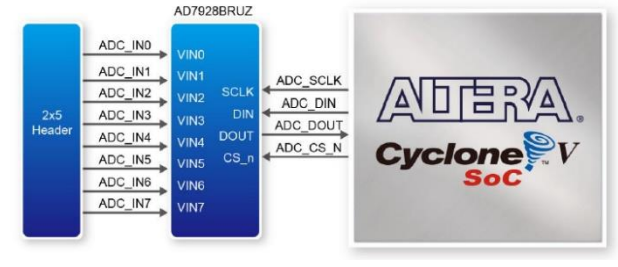

Figure 3: Connection between ADC and FPGA

In order to interpret an analog signal on digital system, we need to convert it to digital level. We reach this aim by using ADC chip on board. On ADC chip, there are eight channels to take data. It is required to one of them and ground pin on ADC header. ADC gives us serial output and we need to convert it to parallel data to store at RAM.

RAM

The aim of usage of RAM store data in order protect information. SDRAM chip consists of 16 bit data line and we send 16 bit parallel data. To hide data properly, we delete data continuously. For this purpose, we use the FIFO which is known as First in First out structure.

MODE SELECTION

This unit led us to select different modes which are AC-DC modes. At AC mode, the dc part ofvoltage is subtracted. At DC mode, this voltage is shown as taken.

COMPUTATION UNIT

At this unit, we need make some calculations to find some basic properties like frequency, RMS voltage of voltage waveform. Implementation of these calculations by using Verilog is challenge of this unit. This challenge is handled by creating easy algorithm for calculations.

VGA SCREEN

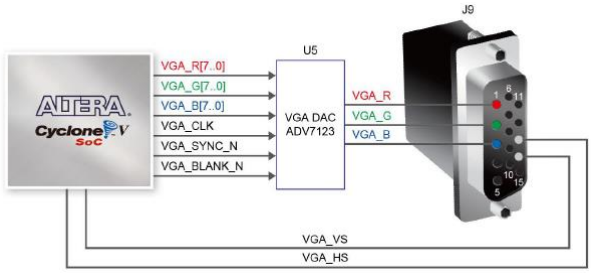

Figure 4: Connections between the FPGA and VGA

It is supposed to use VGA screen to show voltage waveform. At VGA screen, 640*480 image is called frame. For driving VGA, it is required generate 307200 bits store to show screen like video at 1 Hz. At VGA interface, we use five pins. Three of them are R, G, B pins which creates view. Two of them are synchronization pins.

AMPLITUDE MEASUREMENT

```
1   module amplitude(voltage,clk,out);
2   input [15:0] voltage;
3   input clk;
4   output reg [15:0] out;
5
6   reg [15:0] max;
7   reg [15:0] min;
8   initial
9   begin
10  out = 0;
11  max=0;
12  min=0;
13
14  end
15
16  always @(posedge clk)
17  begin
18     if(max<voltage) max<=voltage;
19     else max<=max;
20
21     if(min>voltage) min<=voltage;
22     else min<=min;
23
24
25     out<= max-min;
26
27  end
28  endmodule
29
```

Figure 5: Verilog code of amplitude measurement

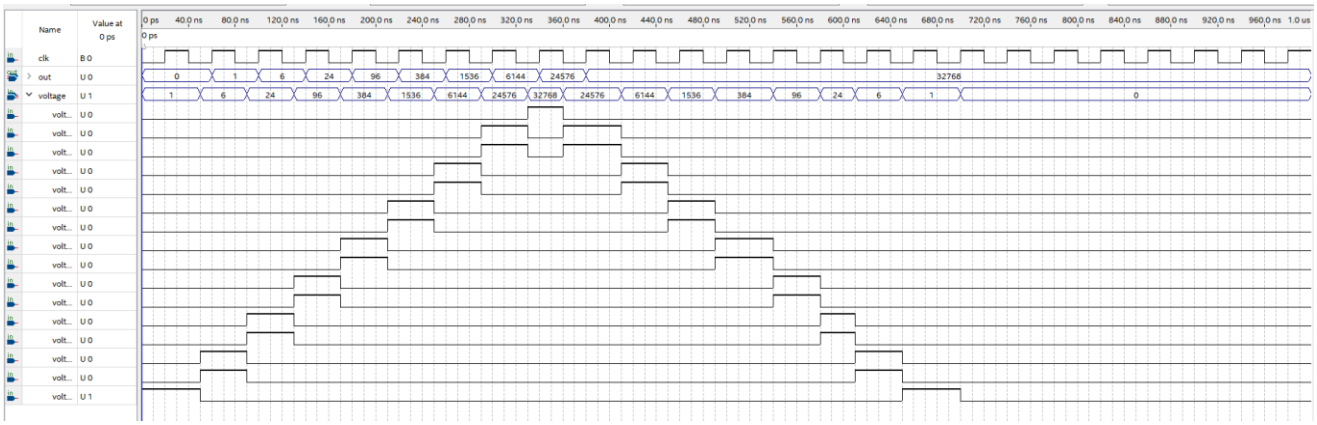

Figure 6: Simulation result of amplitude measurement