MIDDLE EAST TECHNICAL UNIVERSITY

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

EE 464 - Static Power Conversion II - Term Project

Social Isolation Inc.

Development of a DC-DC Converter for Battery Charging

Berkay UZUN - 2263812

Ali BELLİ - 2231421

Ahmet Halis SABIRLI – 2305225

TABLE OF CONTENTS

1. PROJECT DEFINITION

In electrical cars, inside the vehicle, there are two different electrical systems which are low voltage and high voltage. The use of low voltage is to run the low power and low voltage components of the vehicle such as monitor, audio player or fans of the cooling system. To be able to charge the low voltage battery, there is a need of DC/DC converter between high voltage and low voltage system. The main motivation of the project is to construct an isolated 100W DC/DC converter which steps down the 220-400 V input to the 12 V output.

2. TOPOLOGY SELECTION

For the topology selection, there is only one main consideration which is the output power level. The selected topology must satisfy the output power and should not be over designed on it. To do that, we have made some research and found the source to decide the topology. From the information given in Table 1, there are 5 options [1].

Table 1 Power ranges of some of isolated DC-DC converter topologies

TOPOLOGY	POWER RANGE HISTORICALLY USED
Flyback	<100 W
Forward	50W-200W
Active Clamp Forward	50W-300W
Push-Pull	100W-500W
Half-Bridge	100W-500W
Full-Bridge	>500W

When we look at the options, the Full-Bridge is not suitable. In addition, we can see that Push-Pull and Half-Bridge may be over design for our application because the lower limit of them is satisfying the maximum power requirement of our system. Therefore, they are not suitable for our application. After that point, there are staying 3 different topologies. Forward and Active Clamp Forward has more component

compared to the Flyback converter and the Flyback converters maximum power limitation is satisfying our power level. Because of these reasons, we decided to use the Flyback topology to design the DC-DC converter. In addition to them, Flyback is a widely used topology and there are a lot of sources and controllers for this topology in power electronics field. Therefore, easy implementation of the topology has also made us to choose this topology.

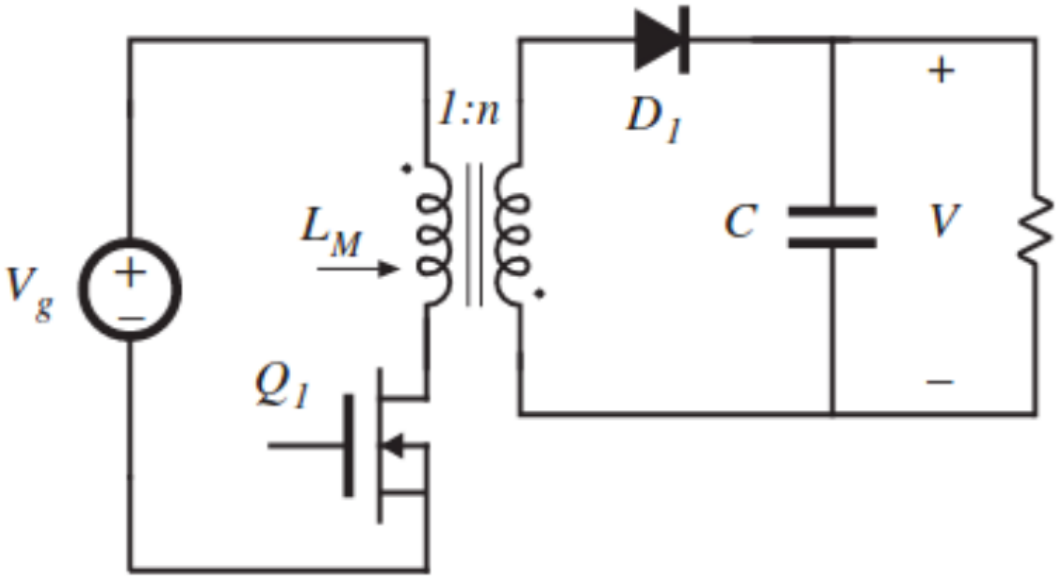

Figure 1 Flyback converter topology

3. CONTROLLER SELECTION

For the controller selection, we have only found two different controllers of the Analog Devices for our application. One of them is Forward and the other one is Flyback converter. The main limitation on the controllers is the maximum input voltage. Although, we have checked so many different producers' controllers, we did not find suitable controllers other than the LT8316 and LT3752-1. The main typical applications of the controllers are given in Fig.-1 and Fig.-2.

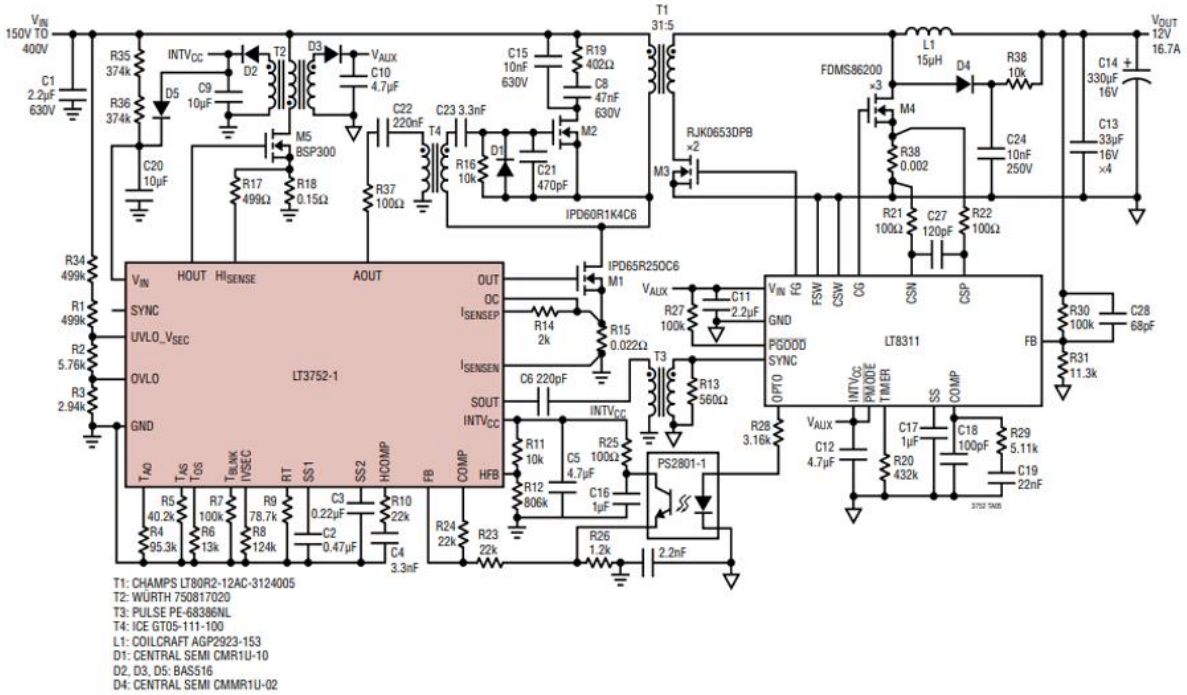

Figure 2 LT3752-1 Typical use

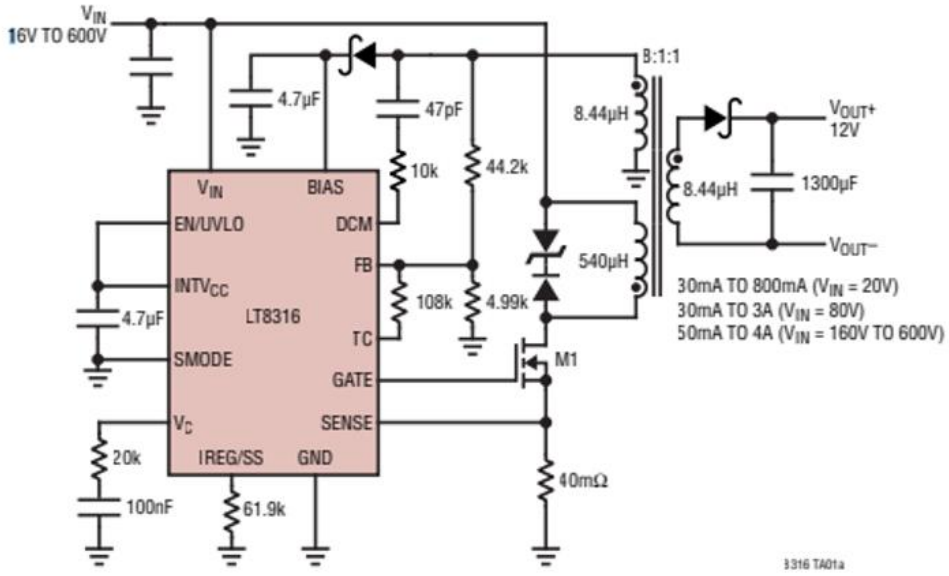

Figure 3 LT8316 Typical use

As the consideration given in the topology selection session, the Forward controller requires more component than the Flyback controller. Therefore, we have chosen the **LT8316 DC-DC Flyback controller** to develop the converter.

4. TRANSFORMER DESIGN

In this part of the project, the following steps were done, the Magnetic Core Design, Winding Selection and Finite Element analysis. To do that, at first, we examined the Flyback topology and developed and Excel program to find the proper interval of inductance and turning ratios. There are mainly to considerations to find the intervals, which are the properties of the controller and the requirements of the Flyback topology. Before going into the calculations of the controller, we calculated the topology requirements for these conditions. After that we obtained the controller needs and intervals. By considering the results, we decided on which core we will use. When we finished the core selection, we began to clarify the wiring properties which are depended on the effective window area of the core and current flowing through wirings. After completing the wire and core selection parts, we run a finite element on ANYSY to check whether our transformer going into the saturation or not. By proving the non-saturated behavior of the core during the maximum limits of the operation, we finished the Transformer Design part.

4.1. Magnetic Core Selection

Before going through the design, at first, we need to decide how we make design, in other words we need to fix some of the parameters to find the rest of the values. We decided to fix the desired duty cycle, desired current ripple, estimated efficiency, and the switching frequency. The switching frequency and the desired current ripple are fixed by considering the operation of the converter. After the fixing the values, the theoretical calculation of the Flyback topology going through like that,

$$\%\Delta I_L = 100\ (For\ boundary\ discontinous\ operation, nature\ of\ the\ controller)$$

$$D_{max} = 0.35\ , f = 140\ kHz, \eta = 0.8$$

We need to find some important variables of the circuit to continue the calculations.

$$I_{out} = \frac{W_{out}}{V_{out}} = \frac{100}{12} = 8.34\ A$$

$$I_{out,average} = \frac{I_{out}}{1-D} = \frac{8.34}{1-0.35} = 12.83\ A$$

$$N_{PS} = \frac{D}{1-D} * \frac{V_{in,min}}{V_{out} + V_{diode}} = \frac{0.35}{1-0.35} * \frac{220}{12+0.5} = 9.47$$

The ratio is hard to find a proper turn numbers of the primary and secondary, therefore,

$$N_{PS} \approx 9$$

After deciding the turn, we need calculate estimated duty cycle of the system to find the turn number of the primary and secondary windings.

$$D_{estimated\_max} = \frac{1}{1 + \frac{V_{in,min}}{V_{out}} * \frac{1}{N_{PS}}} = \frac{1}{1 + \frac{220}{12} * \frac{1}{9}} = 0.33$$

$$D_{estimated\_min} = \frac{1}{1 + \frac{V_{in,max}}{V_{out}} * \frac{1}{N_{PS}}} = \frac{1}{1 + \frac{400}{12} * \frac{1}{9}} = 0.21$$

Now, let's find the maximum turn number of the primary side,

$$N_{P,max} = V_{out,max} * \frac{D_{estimated\_min}}{f * A_c * B_{sat}}$$

As you can observe, we need the find a core to use the effective core area (A_c) and the saturation flux density (B_{sat}). Selecting the core is not straight forward issue. We selected it by checking the limitations again and again for different cores. The

limitations will be calculated later. We selected one of the cores of **TDK**, which is **ETD 29/16/10**. The selected core properties are given in the Table 2.

Table 2 Selected magnetic Mn-Zn ETD shape core

PROPERTIES	**VALUES**
Saturation Flux Density(T)	~0.39
Effective magnetic cross section(mm^2)	76
Window Area (Winding Cross Section) (mm^2)	97
Inductance Factor(nH/$turn^2$)	383
Average Length of Turn(mm)	52.8
Effective magnetic path length (mm)	70.4
Relative permeability of core material (Ungapped)	1470
Relative permeability of core material (Gapped)	281
Airgap(mm)	0.2

$$N_{P,min} = V_{out,max} * \frac{D_{estimated\_min}}{f * A_c * B_{sat}} = \frac{400 * 0.213}{140 * 76 * 0.39 * 10^{-3}} = 20.53$$

$$N_{s,min} = \frac{N_{p,min}}{N_{PS}} = \frac{21.92}{9} = 2.28$$

We decided to use the primary turn as 25 and secondary as 3. Now, we need to calculate the final, effective, duty cycle,

$$D_{effective\_max} = \frac{1}{1 + \frac{V_{in,min}}{V_{out}} * \frac{N_s}{N_p}} = \frac{1}{1 + \frac{220}{12} * \frac{3}{25}} = 0.31$$

Now, let's find the effective inductance values for %100 inductor current ripple,

$$L_{effect,sec} = \frac{V_{out} + V_{diode}}{1} * \frac{1 - D_{effective,max}}{f * I_{out,average}} * \frac{1}{\frac{\Delta I_L}{I_L}} = \frac{12.5 * 0.69}{140 * 12.83 * 10^3} * \frac{1}{1} = 4.8\ \mu H$$

$$L_{effect.prim} = L_{effect,sec} * N_{PS}^2 = 333\ \mu H$$

After finishing the theoretical calculations, now we need the find the limitations of the controller. There are 3 different minimum primary inductance limitation and one maximum primary inductance limitation. Before starting to the calculations, there are some parameters must be given which are used in the following calculations coming from the nature of the controller.

$$t_{off(min)} = 800\ ns$$

$$I_{SW(min)} = 20\frac{mV}{R_{SNS}}, R_{SNS} \approx 28\ m\Omega$$

$$t_{on(min)} = 300\ ns$$

$$I_{SW(max)} = 100\frac{mV}{R_{SNS}}$$

$$t_{BU} = 50\ \mu s$$

$$L_{min1} = t_{off(min)} * N_{PS} * \frac{V_{out} + V_{diode}}{I_{SW(min)}} = \frac{800 * 8.34 * 12.5 * 10^{-9}}{\frac{20}{28}} = 116\ \mu H$$

$$L_{min2} = t_{on(min)} * \frac{V_{in,max}}{I_{SW(min)}} = \frac{300 * 400 * 10^{-9}}{\frac{20}{28}} = 168\ \mu H$$

$$L_{min3} = 2 * (V_{out} + V_{diode}) * \frac{I_{out}}{\eta * I_{SW(max)}^2 * f} = \frac{2 * 12.5 * 8.34}{0.8 * \left(\frac{100}{28}\right)^2 * 140 * 10^3} = 146\ \mu H$$

$$L_{max} = \frac{0.8 * (V_{out} + V_{diode}) * (N_{PS} * t_{BU})}{I_{SW(max)}} = \frac{0.8 * 12.5 * 8.34 * 50 * 10^{-6}}{\frac{100}{28}} = 116.7\ \mu H$$

By using the core properties, we can calculate the primary and secondary inductances and check whether we stay in the controller specifications or not and whether we close to theoretical calculations.

$$L_{prim} = A_L * N_P^2 = 383 * 25^2 * 10^{-9} = 240 \ \mu H$$

$$L_{sec} = A_L * N_S^2 = 383 * 3^2 * 10^{-9} = 3.47 \ \mu H$$

The selection of the inductance factor (A_L) is not a straightforward issue and we selected it by considering the saturation limit of the selected core. Therefore, we have had to lose some inductance to satisfy the non-saturated operation and to leave the final duty cycle lower than the desired one. As a result, the inductance values are suitable for the controller and the controller will handle rest of the parameters by using the feedback loop inside it.

We checked how much airgap we need to stay in the non-saturated region during the operation,

$$Gap_{min} = \mu_o * N_p^2 * \frac{A_e}{L_{primary}} - \frac{l_e}{\mu_e} = 4 * \pi * 10^{-7} * 25^2 . \frac{76 * 10^{-6}}{240 * 10^{-6}} - \frac{70.4 * 10^{-3}}{1470}$$

$$Gap_{min} = 0.2 \ mm$$

We have used the equation given below to check whether the core is going through the saturation during the operation or not,

$$B_{max} = \mu_o * \mu_e * N_P * \frac{I_{in,max}}{I_e} = \frac{4 * \pi * 10^{-7} * 281 * 25 * \left(\frac{100}{220 * (0.31)} * 2\right)}{70.4 * 10^{-3}}$$

$$B_{max} = \mathbf{0.37\ T < 0.39\ T}$$

We are satisfying saturation condition, which is the most important one for the application. At that point, we are finishing the core selection part and moving to the winding selection part.

4.2. Winding Selection

Winding selection is another important topic while designing a transformer. Both the wire itself and the wiring type effects the performance of the transformer. Choosing thicker wire may seem to reduce the resistance and losses however due to skin and proximity effects, diameter of the wire does not affect losses after a point. Moreover, thicker wires result in bulkier windings which increases leakage inductances. However, choosing wires too thin may result in excessive heat generation and meltdown in critical points of the winding. Therefore, we tried to make a balanced selection.

First, we assumed that output current flows through the windings without alternating and find a wire so that current density of the wire is around 5 A/mm2

$$I_{out} = 8.34\ A$$

$$A_{wire} = \frac{I}{J} = \frac{8.34}{5} = 1.668\ mm^2$$

$$D_{wire} = 1.458\ mm$$

Even though, due to skin and proximity effects, current will flow nonhomogeneous and most of the copper will not carry any current, high heat capacitance of thicker wire will prevent burnouts in the winding.

We have total of 31 turns of winding which consists of 25 primary, 3 secondary and 3 feedback turns. The selected core can accommodate around 12-13 turns per layer. Since we only needed three layers of windings, we did not see necessary to make interleaved winding and make two layers of primary winding and one layer of combined secondary and feedback winding. In this case, we chose **AWG15 cable**.

4.3. Finite Element Analysis

After deciding the core material, shape, airgap and the windings, we started to draw the transformer in Maxwell 3D. For faster analysis, continuous surfaces were drawn with edges as shown in Fig 5. Main reason of Finite Element Analysis is to check our design parameters and calculate transformer parameters which cannot be calculated analytically. First, we draw only the primary winding to check our model's validity. After finding that analysis results were almost same with datasheet values of the core we continued with secondary and feedback windings. However, if we make 25 turn primary and 3 turn secondary, secondary inductance becomes larger than the calculations. This is most probably due to reduction of magnetic path (therefore reduction in reluctance) while increasing layer number (winding radius). This kind of secondary effects was the first reason why we did finite element analysis. To overcome this effect, we reduced the secondary turn number to 2.5 and the results were satisfactory.

	Current1	Current3	Current5
Current1	244.11	28.622	28.607
Current3	28.622	3.5545	3.3315
Current5	28.607	3.3315	3.5369

Figure 4. Self and mutual inductances of the windings (μH)

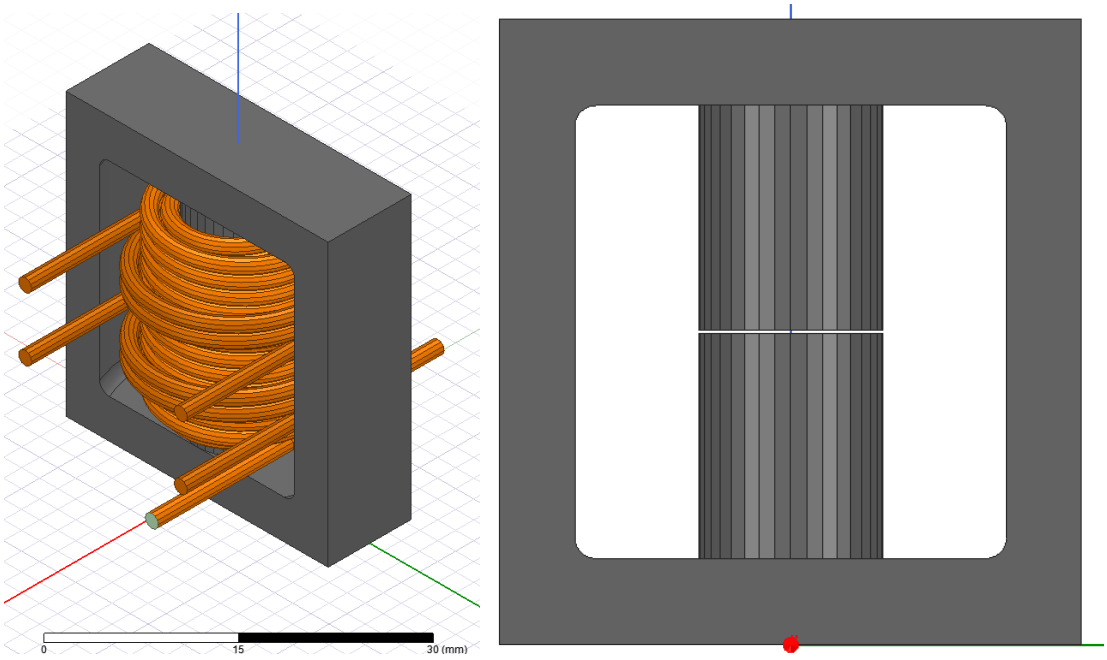

Figure 5 Maxwell 3D model

After satisfying inductance and turn ratio parameters we moved on to saturation control. To observe the magnetic flux density in most extreme case, we supplied primary winding with 3A current. This 3A comes from the calculations of the controller and it is also observed in LTspice. To ease the work of the computer, meshing was concentrated in the inner corner and near the airgap. Both magnetic flux density and vectors can be seen in Fig 6,7 and 8.

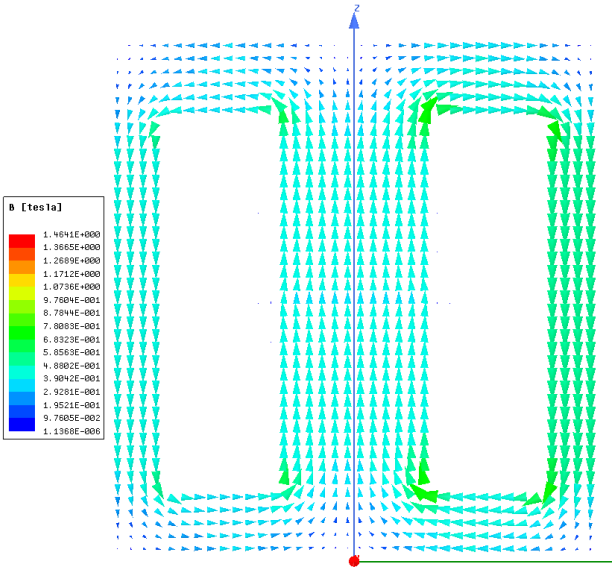

Figure 6 Magnetic flux vectors

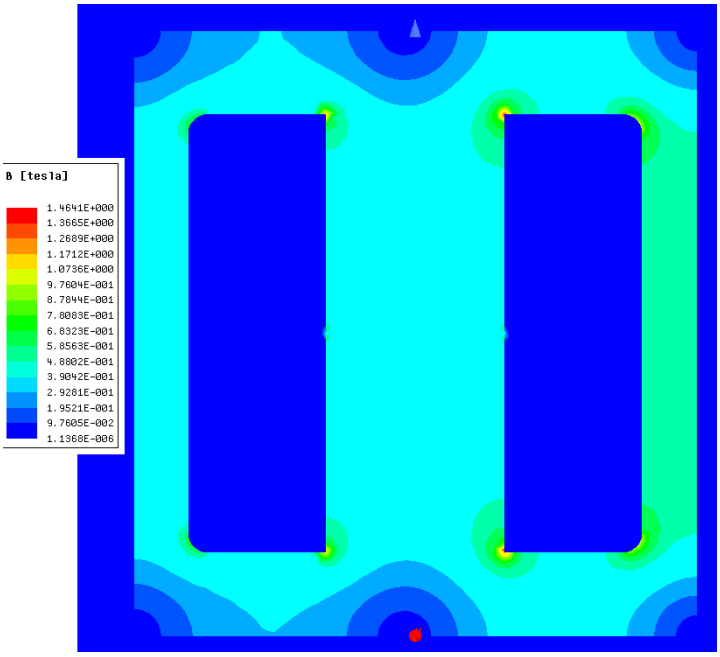

Figure 7 Magnetic flux density

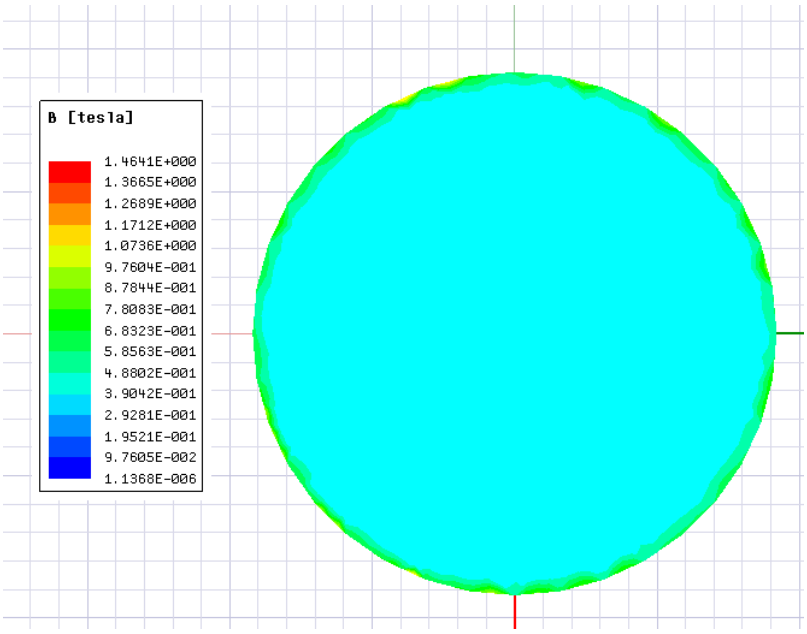

Figure 8 Magnetic flux density of the core center

At maximum magnetic flux density that the core can see, most of the core remans unsaturated. However, some corners of the core are saturated. This may be acceptable since transformer will work in this condition on extreme cases and for transient times. Transformer current will reduce after reaching steady state.

Final analysis that we made is eddy current analysis. We made this analysis to estimate the AC resistance of the windings and to observe the current density in those windings. Current density can be seen in Fig 9.

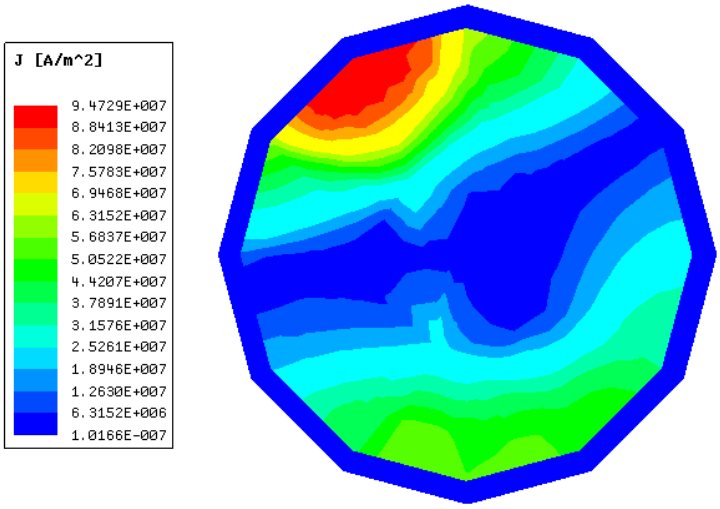

Figure 9 Current density of a single wire in primary winding

As expected, we see nonhomogeneous current distribution in the conductor due to skin and proximity effects. More important than to see the current distribution is to get the AC resistance to accurately calculate copper losses in the transformer.

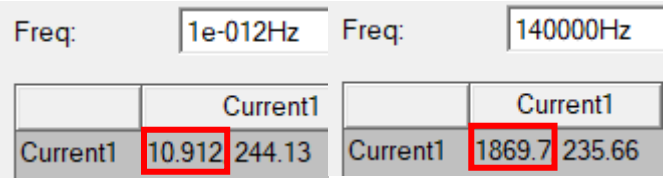

Figure 10 DC and AC resistances of primary winding (mΩ)

As we can see in Fig 10. Frequency has a significant effect on the resistance. Even though we expected such increase, numerical value of the resistance is found by FEA. Therefore, we used this result (1.869Ω) in LTspice simulations.

5. COMPONENT SELECTION

For the component selection part, there are 3 main subtitles, which are the output capacitor selection, controller passive elements selection and the power semiconductor selection for now to complete the simulations. When we begin to develop the PCB schematics and layouts, there will be also connector selection part and elements of protection circuits.

5.1 Output Capacitor Selection

The output capacitor should be selected to reduce output voltage ripple while also keeping in view the larger size and price of a larger capacitor. The minimum output capacitor can be calculated using the equation as below:

$$C_{out,min} = \frac{L_{prim} * I_{lim}^2}{2 * V_{ripple} * V_{out}} = \frac{244.11 * 10^{-6} * \left(\frac{100 * 10^{-3}}{27.62 * 10^{-3}}\right)^2}{2 * 0.48 * 12} = 277.77\ \mu F$$

where I_{lim} = Maximum primary current = 100mV/R_{sense}

In this equation, we found the minimum output capacitor value that is required. However, we chose around 438 μF capacitor for better filtering. Also, we aimed to minimize ESR. For this reason, we choose following capacitors:

Type	Value	Quantity
Aluminum	100 µF	3
Ceramic	47 µF	2
Ceramic	10 µF	4
Ceramic	1 µF	4

5.2 Controller Passive Elements Selection

5.2.1 Snubber Resistance and Capacitor Selection

The proposed design solution for the RC snubber is to power up at low voltage to prevent overvoltage stress, calculate the duration of the ringing on the MOSFET's drain when the power switch turns off without the snubber, and then apply capacitance $C_{Snubber}$ until the ringing period is 1.5 to 2 times longer. To find the snubber resistance, we first need to find leakage inductance. The leakage inductance depends on the coupling coefficient. Coupling coefficients of k=99 percent are typical, and they are determined by the transformer's structure and materials.

$$L_{leak} = \frac{2 * L_{pri}(1-k)}{k} = 2 * 244.11 * 10^{-6} * \frac{1-0.99}{0.99} = 4.93\ \mu H$$

Now, we can find the snubber resistance with equation below. The capacitor value here is taken from the datasheet of the mosfet we have chose.

$$R_{Snubber} = \sqrt{\frac{L_{leak}}{C_{in}}} = \sqrt{\frac{4.93 * 10^{-6}}{1150 * 10^{-12}}} = 65.47\ \Omega$$

Component	Type	Value
Snubber Resistance	Chip Resistor-Surface Mount	68Ω
Snubber Capacitor	Ceramic	470pF

5.2.2 Feedback Resistances Selection

The isolated output voltage is controlled by the LT8316 using a special sampling scheme. The scheme experiences repeatable delays and error sources due to its sampling design, which would influence the output voltage and cause a reevaluation of the resistor values. So, the controller needs feedback resistors to regulate this situation. According to the datasheet, in order to determine the values of these resistors, we need to assign a value to one of them and find the other with the equation below.

$$R_{fb1} = 10\ k\Omega\ (\ fixed\ value)$$

$$R_{fb2} = R_{fb1} * \left(\frac{V_{out} + V_{diode}}{1.22} * N_{TS} - 1\right) = 10 * 10^3 * \left(\frac{12 + 0.5}{1.22} * 1 - 1\right) = 92.45\ \text{k}\Omega$$

Resistance	Type	Value
R_{fb1}	Chip Resistor-Surface Mount	10kΩ
R_{fb2}	Chip Resistor-Surface Mount	90kΩ

5.2.3 $R_{IREG/SS}$ Selection

This resistor is used to regulate the output current. We can find the resistance value we need to use with the equation given below:

$$R_{IREG/SS} = \frac{2.5M\Omega * I_{out} * R_{sense}}{N_{PS}} = \frac{2.5 * 10^6 * \frac{100}{12} * 27.62 * 10^{-3}}{8.34} = 68.9\ k\Omega$$

According to the above equation, we found the required resistance value of 68.9kΩ.

Type	Value
Chip Resistor-Surface Mount	69.8kΩ

5.2.4 Sense Resistor Selection

We need a sense resistor to be able to set the maximum current. In the datasheet of the controller we chose, the formula for R_{sense} is shown as below:

$$R_{sense} = \frac{1 - D_{V_{in}(min)}}{I_{out(\max)}} * 50mV * N_{ps} * 0.8 = \frac{1 - 0.31}{\frac{100}{12} * 2} * 50 * 10^{-3} * 8.34 * 0.8$$

$$R_{sense} = 27.62\ m\Omega$$

Type	Value
Chip Resistor-Surface Mount	28mΩ

5.2.5 Boundary Mode Detection Capacitor

Application note of the controller suggest using 47pF capacitor and check if the operating point is in boundary condition. If not, it is suggested to increase this capacitor up to 100pF. 47pF was satisfactory for our application so we selected this value.

Type	Value
Ceramic	47pF

5.2.6 Additional Component

C_{DRV}, C_{BIAS} and V_c capacitor, V_c resistance, DCM resistance, thermal correction resistance and are not specified as application dependent capacitors in the datasheet. Therefore, we used same values capacitors as given in the typical application.

Bias diode is also not specified in the application note but it is denoted with fast diode symbol. We will choose this diode according to the simulation results.

Component	Type	Value
V_c Resistance	Chip Resistor-Surface Mount	20kΩ
Thermal Correction Resistance	Chip Resistor-Surface Mount	500kΩ
DCM Resistance	Chip Resistor-Surface Mount	10kΩ
Bias Capacitor	Ceramic	4.7µF
Drive Capacitor	Ceramic	4.7µF
V_c Capacitor	Ceramic	100nF

Type	Package	Maximum Voltage (V)	Maximum Current (A)
Schottky	DO-214AC	150	3A

5.3 Semiconductor Selection

5.3.1 Snubber Diodes Selection

Fast recovery: According to the application note, breakdown voltage of this diode must be greater than the drain pin voltage of the MOSFET.

Type	Package	Maximum Voltage (V)	Maximum Current (A)
Fast Recovery	DO-214AC	600	2A

Zener: Zener voltage must be largest possible value withing given limitations. And it is recommended to use around 500 mV Zener diode in the snubber. According to the controller's datasheet, we can calculate the maximum voltage capacity of the Zener diode with the following equation:

$$V_{zener} \leq V_{breakdown} - V_{in,max}$$

$$V_{zener} \leq 650V - 400V$$

$$V_{zener} \leq 250V$$

Type	Package	Maximum Voltage (V)	Maximum Power (W)
Zener	SMB	150	3

5.3.2 MOSFET Selection

As can be seen from the simulation result in Figures 11 and 12, the maximum voltage is around 630V and current value is around 3.6A on the MOSFET. While choosing the MOSFET, we made a choice considering these values. High current rated MOSFET is selected due to its low resistance.

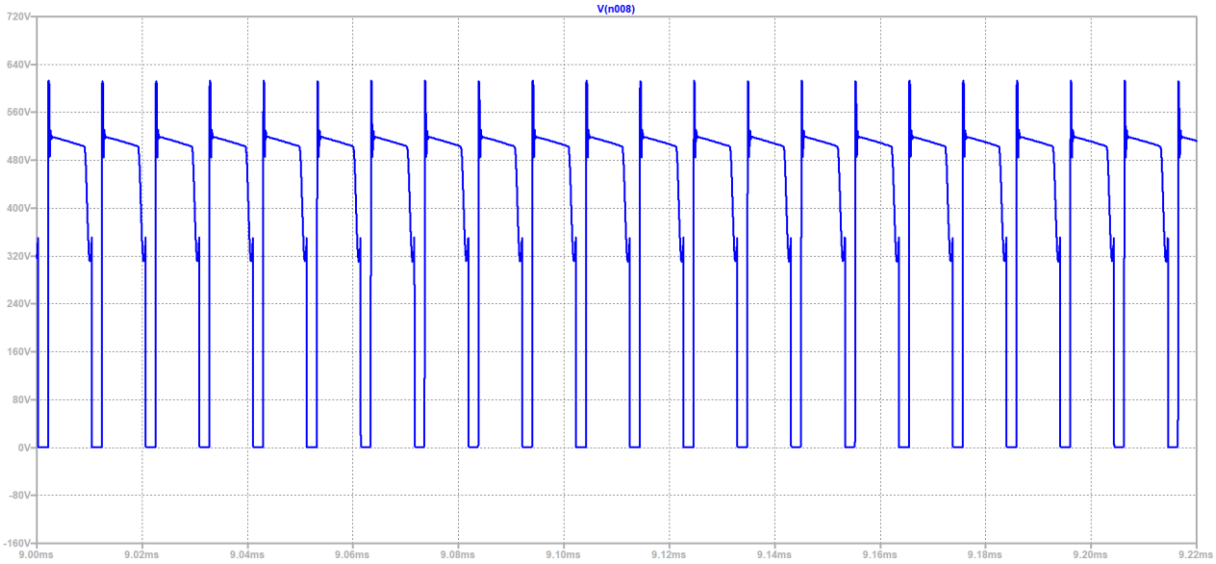

Figure 11 MOSFET voltage graph

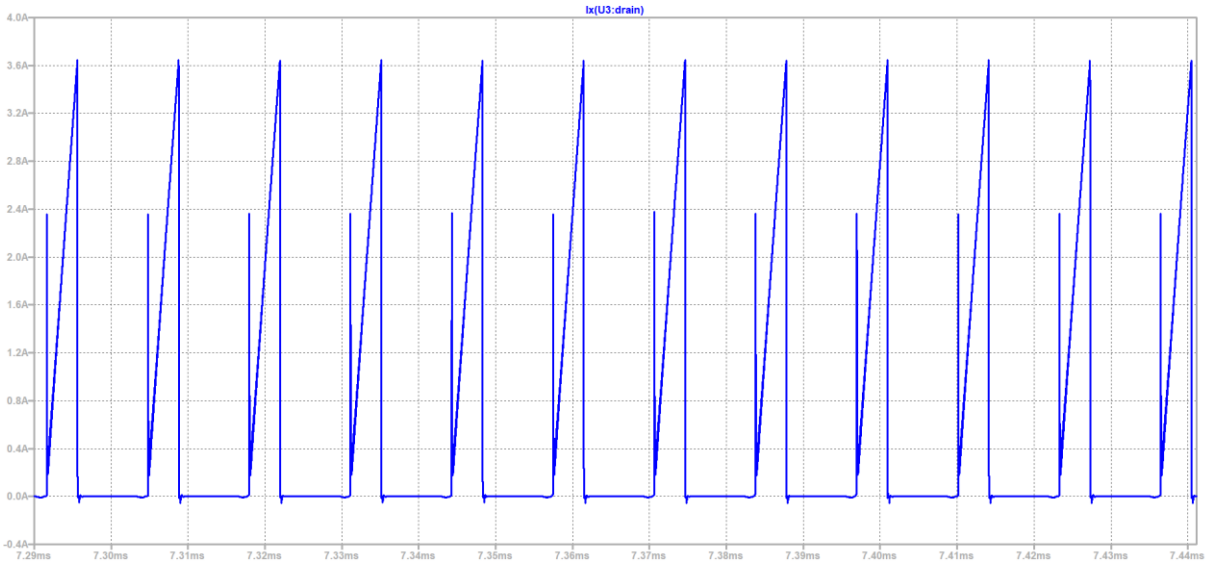

Figure 12 MOSFET current graph

Type	Package	Maximum Voltage (V)	Maximum Current (A)
CoolMOS™	PG-TO252-3	800	17A

5.3.3 Output Diode Selection

The Figures below, namely Figure 13 and Figure 14, show the reverse voltage of the diode and the peak forward current. According to these graphs, the reverse voltage on the diode is around 65V. The current flowing on it is approximately 35 A. We should choose the output diode by considering these criteria.

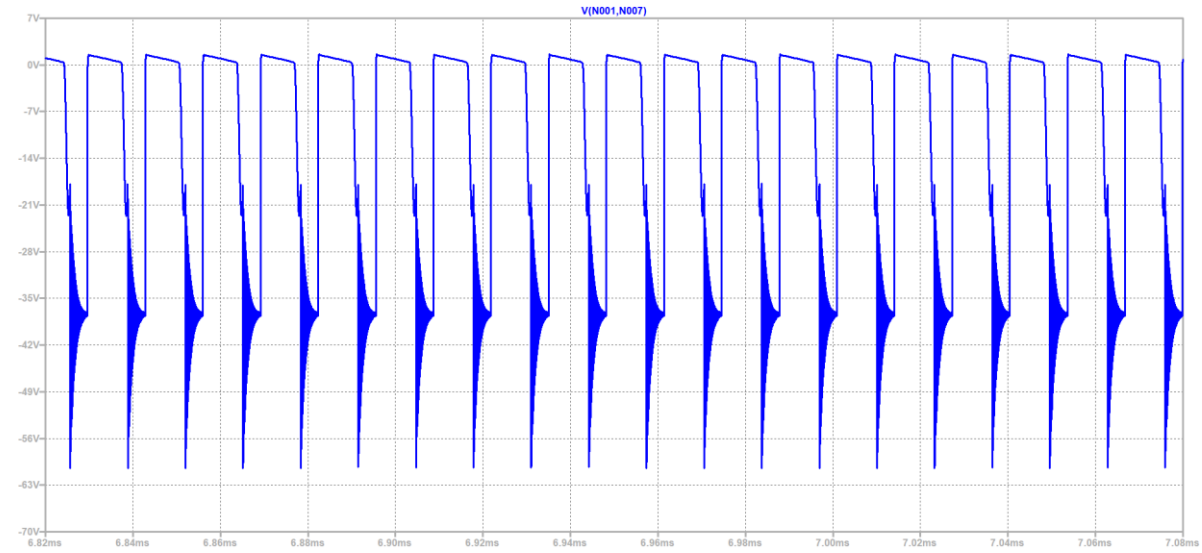

Figure 13 Output diode voltage graph

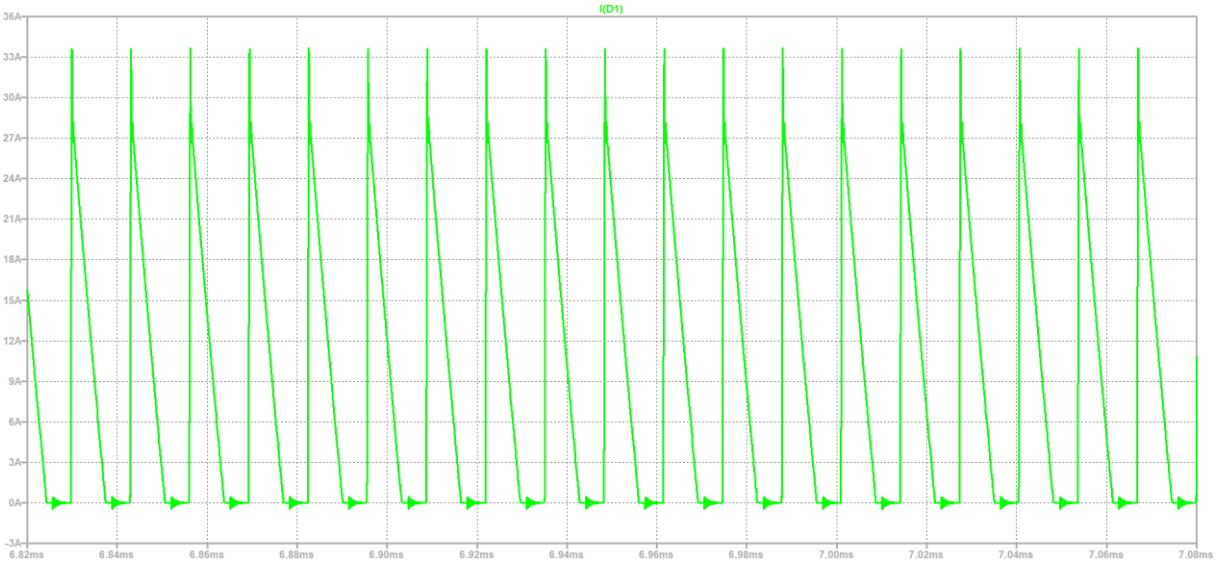

Figure 14 Output diode current graph

Type	Package	Maximum Voltage (V)	Maximum Current (A)
Schottky	TO-277	80	20

6. PROTECTION CIRCUITS

Protection circuits are required for all electrical equipment. They are used to safeguard the linked circuit from a reverse connected power supply. They're also utilized to defend connected circuits from a reverse-connected power source or a voltage that's higher than the circuit's design voltage.

6.1 Output Overcurrent Protection Circuit

Over current at the output can occur due to many reasons like inrush current or short circuit. To protect both the load and the converter we need to shut down the converter in such cases. Most common way to protect from over current is to use a slow burn fuse. However, fuses require replacement if they burn. Therefore, we designed a circuit so that no replacement is necessary.

First, we measure the load current with an IC and compared with the limit current (15A) that we specified using a Zener voltage reference. Then, we added an analog delay (2ms) circuit so that converter is not turned off during transients or small inrush current event. Resulting overcurrent signal drives MOSFETs that turns down the converter using it's "Enable" pin. Between the MOSFETs and the converter an optocoupler is used to maintain the isolation. Op-amp and reference voltage generator is supplied with a small 5V switching regulator. Figure 15 shows the schematic of the output overcurrent protection circuit.

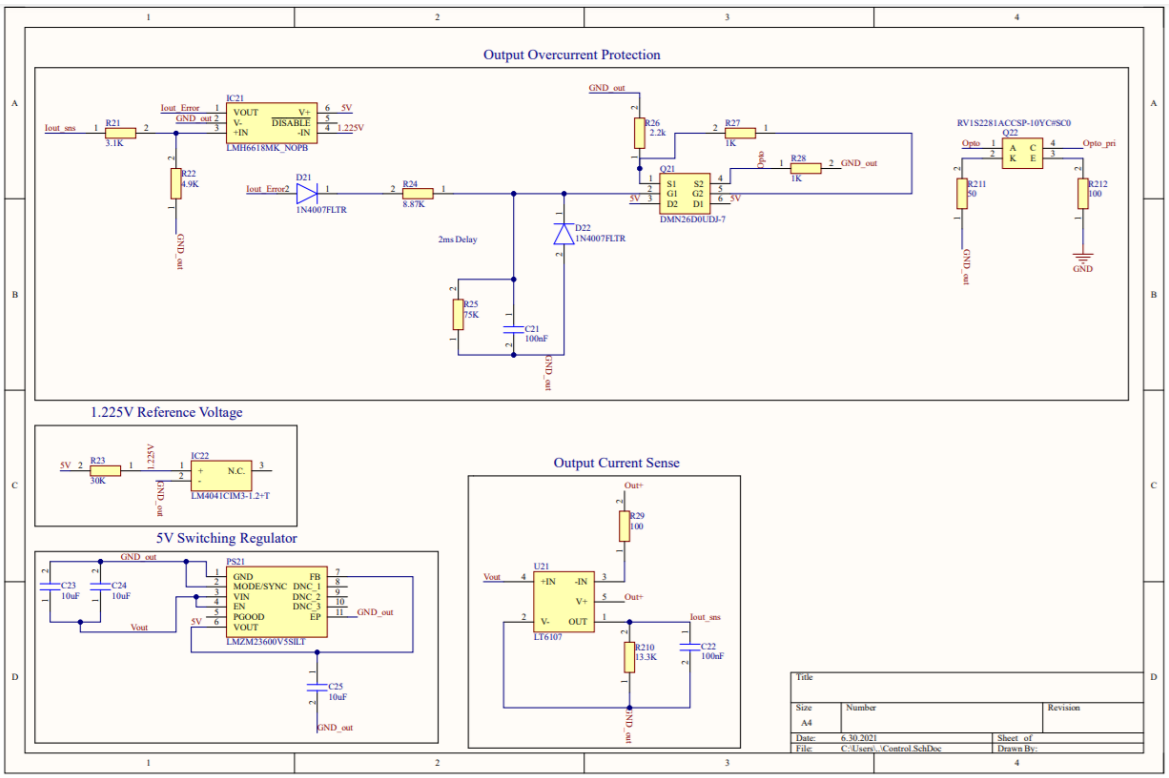

Figure 15 Schematic of the Output Overcurrent Protection Circuit

6.2 Input Reverse Polarity Protection Circuit

Reverse voltage is destructive to the circuit due to unipolar components. To avoid this, we implemented PMOS reverse polarity protection between the input and the converter. PMOS protection is selected due to its simplicity. Since our input current is quite low, loss of the PMOS is also very small (~0.8W). Zener diode is used so that V_{SG} voltage of the MOSFET stays in the limit. Simulation and the schematic are given below figures.

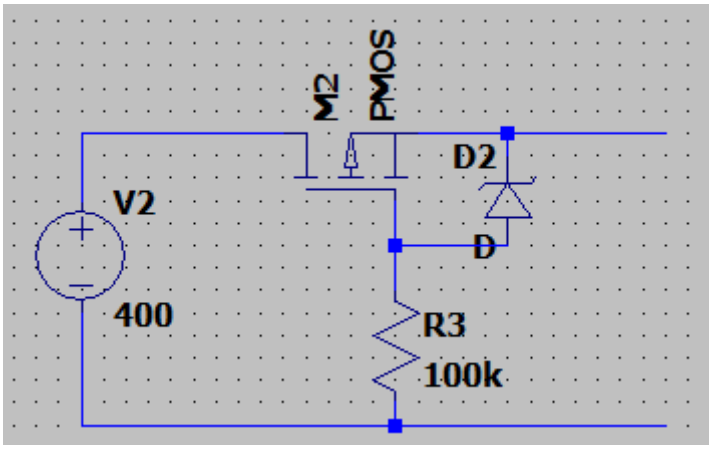

Figure 16 Schematic of the Input Reverse Polarity Protection Circuit

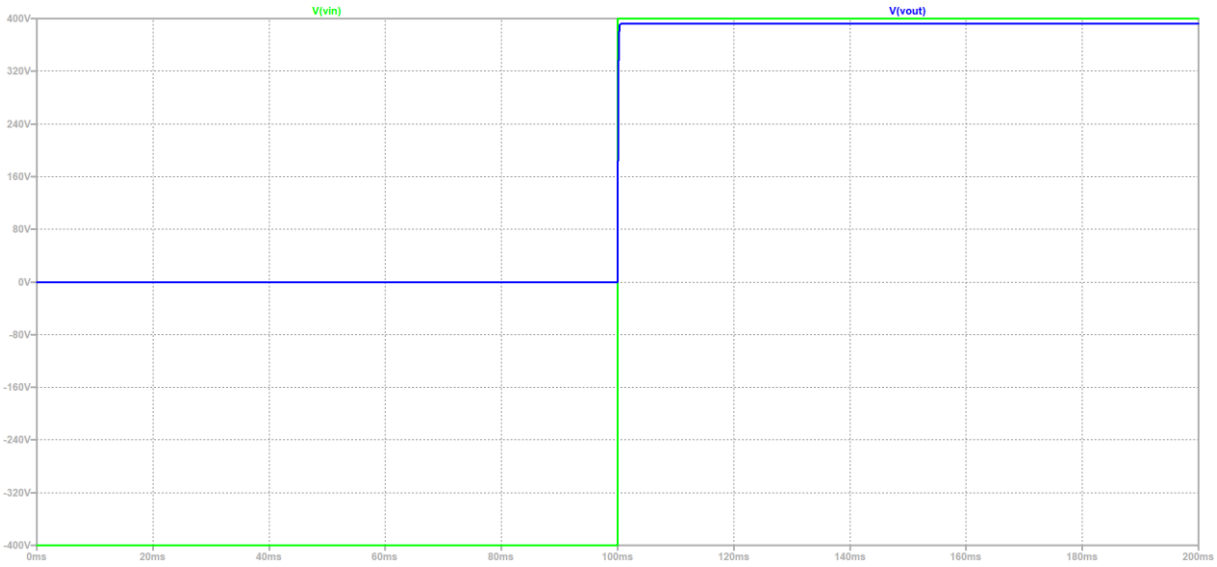

Figure 17 Simulation Result of the Input Reverse Polarity Protection Circuit

7. LTSPICE SIMULATION RESULTS

We divided LTspice simulation results into three subtitles, which are Steady-State Full-Load Responses, Load Regulation and Line Regulation. To do that, we constructed all the circuit on the LTspice by reducing the ideality of the circuit by adding some of the real-time application parameters such as Leakage inductances and series resistance of the primary and secondary side of the transformer. The overall simulation model is given in the Figure 18.

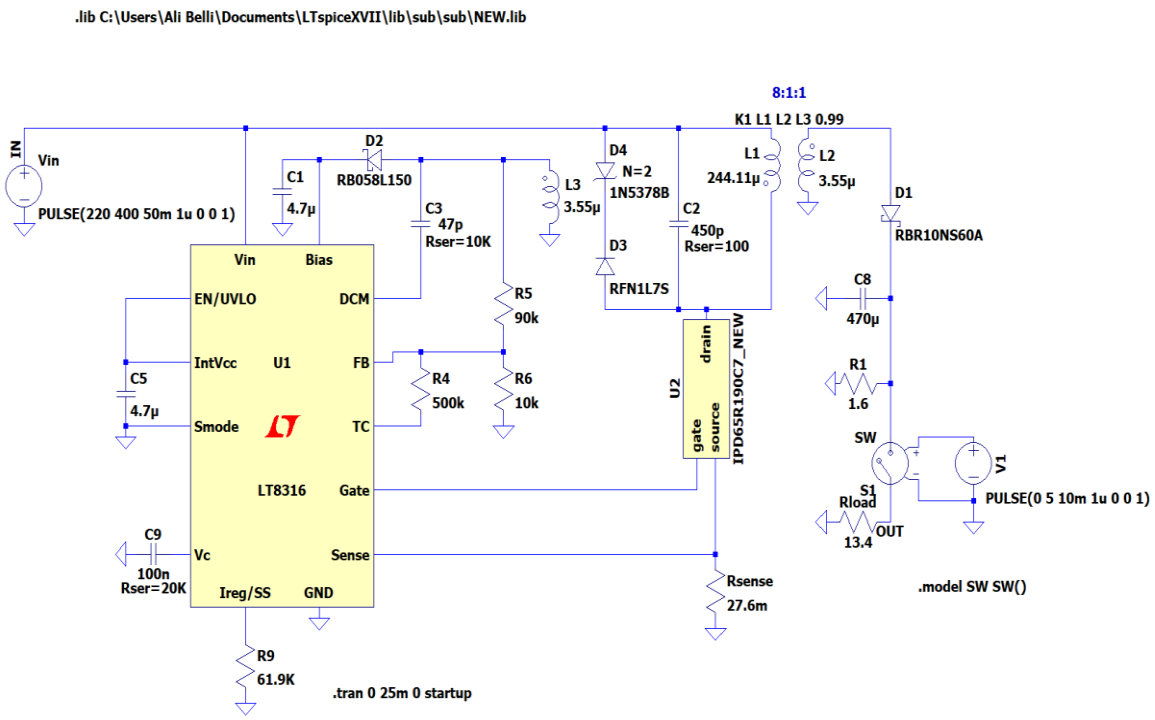

Figure 18 Project design schematic

7.1 Steady-State Full-Load Responses

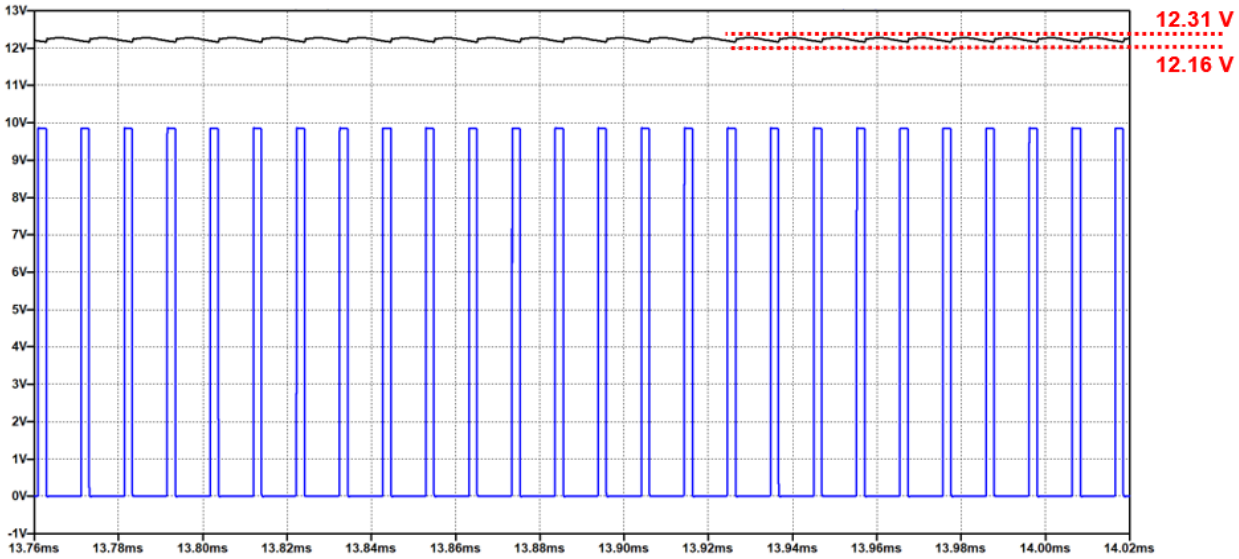

Figure 19 Output Voltage at 400 V input

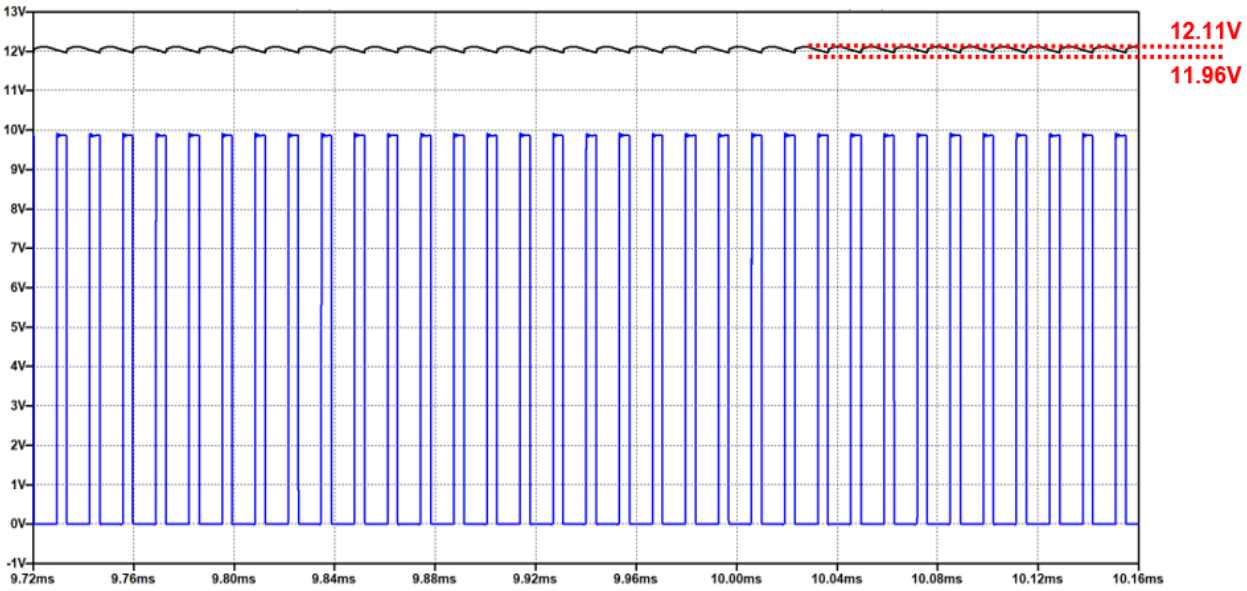

Figure 20 Output Voltage at 220 V input

From the steady-state full load analysis of the converter at 400 V maximum input and 220 V minimum input conditions, which are given in the Figure 19 and Figure 20 respectively, we can claim that the output voltage of the controller is including ripple less than %4. As a proof,

$$\%\Delta V_{out,220} = \frac{12.11 - 11.96}{12} * 100 = \%1.25 < \%4$$

$$\%\Delta V_{out,400} = \frac{12.31 - 12.16}{12} * 100 = \%1.25 < \%4$$

7.2 Load Regulation

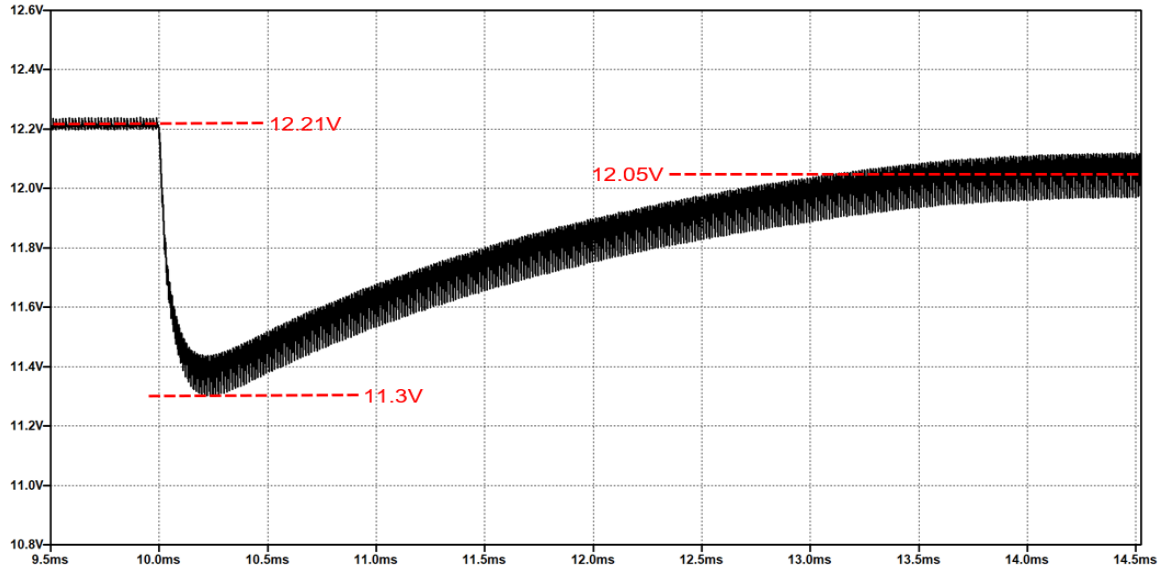

Figure 21 Light Load to Full Load Response

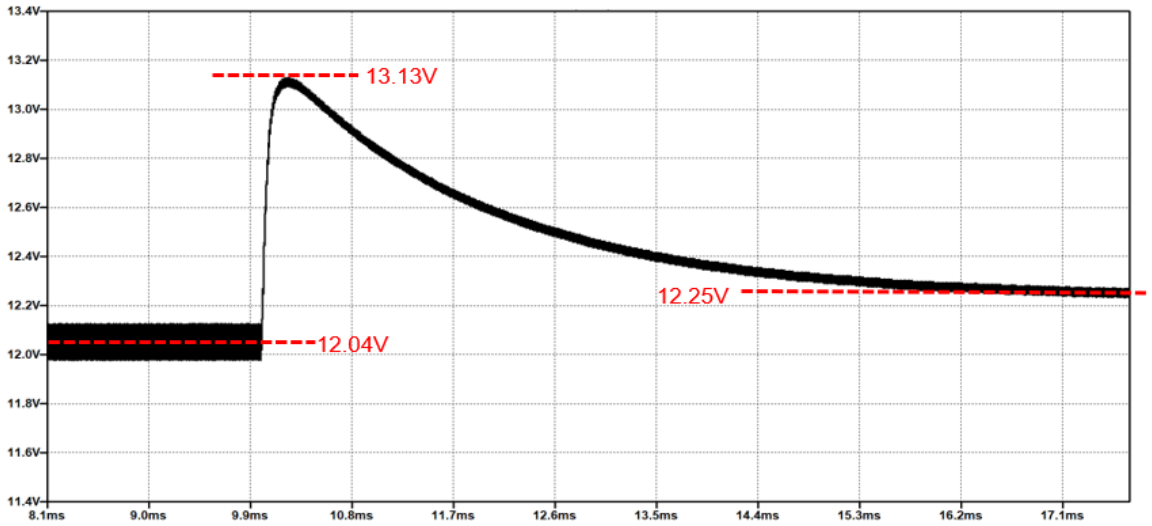

Figure 22 Full Load to Light Load Response

The load regulation simulations were conducted as two part, which are heavy load to light load and vice versa. The results are given in Figure 21 and Figure 22. From the figures, we can say that the results are satisfying the load regulation limitation. As a proof,

$$\%\Delta V_{out,load1} = \frac{12.21 - 12.05}{12} * 100 = \%1.33 < \%3$$

$$\%\Delta V_{out,load2} = \frac{12.25 - 12.04}{12} * 100 = \%1.75 < \%3$$

7.3 Line Regulation

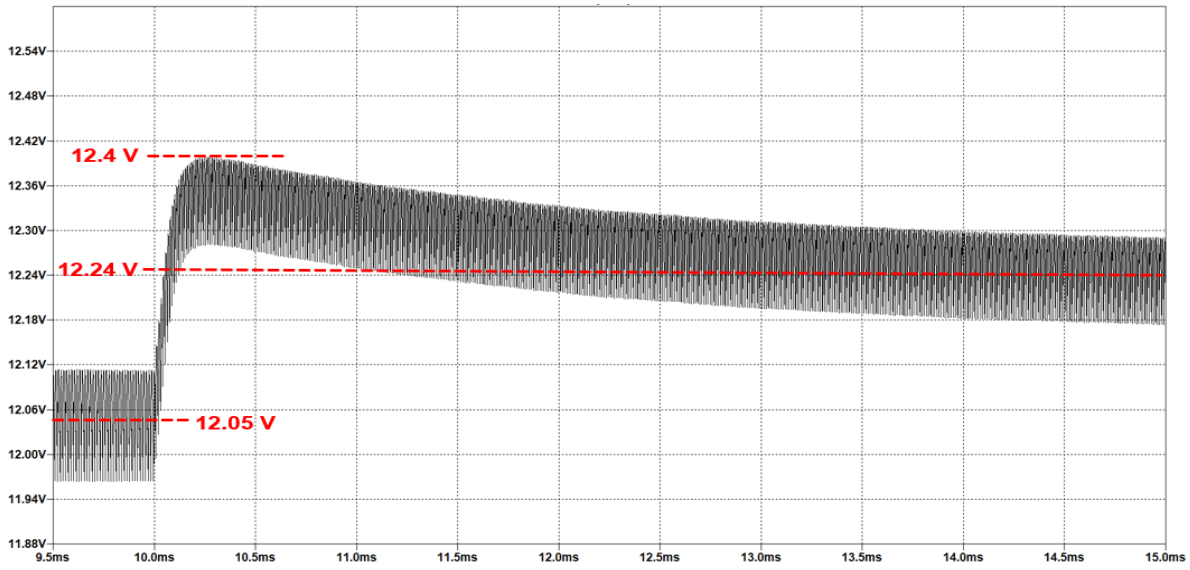

Figure 23 220V to 400V Response

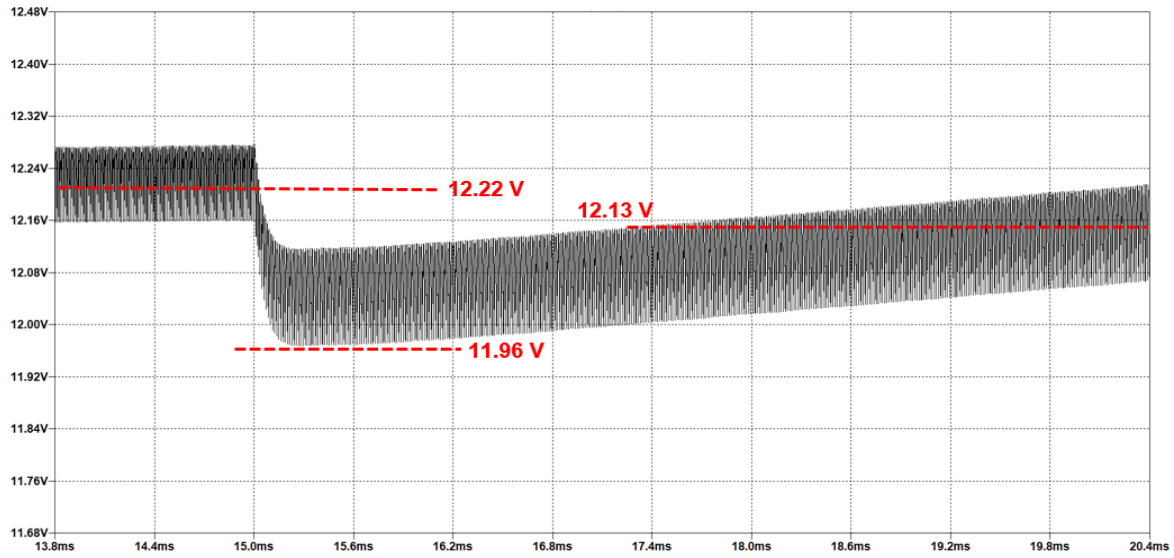

Figure 24 400V to 220V Response

The line regulation simulations were conducted as two part, which are 220 V input to 400V and vice versa. The results are given in Figure 23 and Figure 24. From the figures, we can say that the results are satisfying the line regulation limitation. As a proof,

$$\%\Delta V_{out,line1} = \frac{12.24 - 12.05}{12} * 100 = \%1.58 < \%3$$

$$\%\Delta V_{out,line2} = \frac{12.22 - 12.13}{12} * 100 = \%0.75 < \%3$$

8. LOSS CALCULATIONS

There are losses in some parts of the circuit we designed. One of the parts where these losses occur is the MOSFET. There are both switching and conduction losses on the MOSFET. These losses are calculated as shown below:

$$P_{sw} = E_{sw} * f$$

$$P_{sw} = 5.2 * 10^{-6} * 150 * 10^{3}$$

$$\boldsymbol{P_{sw} = 0.78\,W}$$

$$P_{conduction} = I_{D,RMS}^{2} * R_{DS}$$

$$P_{conduction} = 0.827^{2} * 0.280$$

$$\boldsymbol{P_{conduction} = 0.19\,W}$$

Another part is the diode. There is no switching loss on the diode. There is only conduction loss. This loss is calculated as follows:

$$P_{conduction} = I * V_{on}$$

$$P_{conduction} = 11.94 * 0.56$$

$$\boldsymbol{P_{conduction} = 6.69\,W}$$

Compared to the MOSFET and the diode, the part where the loss is higher is the transformer. Transformer has core loss and copper loss. Copper loss is calculated as shown below.

$$P_{cu} = P_{cu,pri} + P_{cu,sec} = I_{pri,RMS}^2 * R_{pri,AC} + I_{sec,RMS}^2 * R_{sec,AC}$$

$$P_{cu} = 0.833^2 * 1.87 + 12.04^2 * 0.042$$

$$\boldsymbol{P_{cu} = 7.39\,W}$$

Core loss is calculated from online calculator offered by TDK.

$$\boldsymbol{P_{core} = 11.89\,W}$$

Finally, there is a loss on the snubber. Although the loss here is not as much as the transformer, it is more than the MOSFET and diode. This loss is calculated as shown below:

$$P_{Snubber} = P_{diode} + P_{resistor}$$

$$P_{Snubber} = 2.16 + 6.35$$

$$\boldsymbol{P_{Snubber} = 8.51\,W}$$

The total loss in the isolated DC-DC converter we designed is as follows:

$$P_{TOTAL} = P_{MOSFET} + P_{DIODE} + P_{TRANSFORMER} + P_{SNUBBER}$$

$$P_{TOTAL} = 0.78\,W + 0.19\,W + 6.69\,W + 7.39\,W + 11.89\,W + 8.51\,W$$

$$\boldsymbol{P_{TOTAL} = 35.45\,W}$$

9. THERMAL ANALYSIS

As previously stated, a temperature increase can be caused by a variety of losses. The first one is the MOSFET's conductor and switching losses. These losses were calculated in the previous part. The junction temperature without a heatsink is computed as follows. Assume that the ambient temperature is 25°C.

$$T_{junction} = P_{loss} * R_{\Theta JA} + T_{ambient}$$

$$T_{junction} = (0.78 + 0.19) * 45 + 25°$$

$$\boldsymbol{T_{junction} = 68.65°}$$

The second one is the conductor loss on the diode. This loss was calculated in the previous part. The junction temperature without a heatsink is computed as follows. Assume that the ambient temperature is 25°C.

$$T_{junction} = P_{loss} * R_{\Theta JL} + T_{ambient}$$

$$T_{junction} = 6.69 * 10 + 25°$$

$$\boldsymbol{T_{junction} = 91.9°}$$

The third one is the loss on the snubber. This loss also was calculated in the previous part. The junction temperature without a heatsink is computed as follows. Assume that the ambient temperature is 25°C.

$$T_{junction} = P_{loss} * R_{\Theta JA} + T_{ambient}$$

$$T_{junction} = 2.16 * 24 + 25°$$

$$\boldsymbol{T_{junction} = 76.84°}$$

In the circuit we designed above, the junction temperature was calculated without the heatsink of the components that cause the system to heat up. Looking at the results, it is clearly seen that the most heated component is the output diode. However, the working range of these selected components can generally go up to 150 degrees. In addition, in a circuit designed for this area, the junction temperatures of the components are expected to rise up to 125 degrees. Considering the results of our calculations, the junction temperatures we calculated do not even exceed 100 degrees. For this reason, there is no need to use a heat sink. As a result, using this designed circuit in such an area will not be a problem.

Thermal analysis is also required for the core since its thermal resistance is not given in the datasheet. We used ANSYS Mechanical to make finite element analysis. After importing the model from Maxwell 3D and specifying the materials we defined internal heat generation in the core according to loss calculations. Heat generation is assumed to be homogeneous for simplicity. After meshing, convection is defined at the sides of the core. Convection coefficient is selected as 14 W/m²-K which is obtained from "Parametric Study of Heating in a Ferrite Core Using SolidWorks Simulation Tools" by Gregory K. Ovrebo. Analysis results is given below Figure 25. We can see that maximum temperature is around 82°C which is below the suggested temperature of the core (100°C)

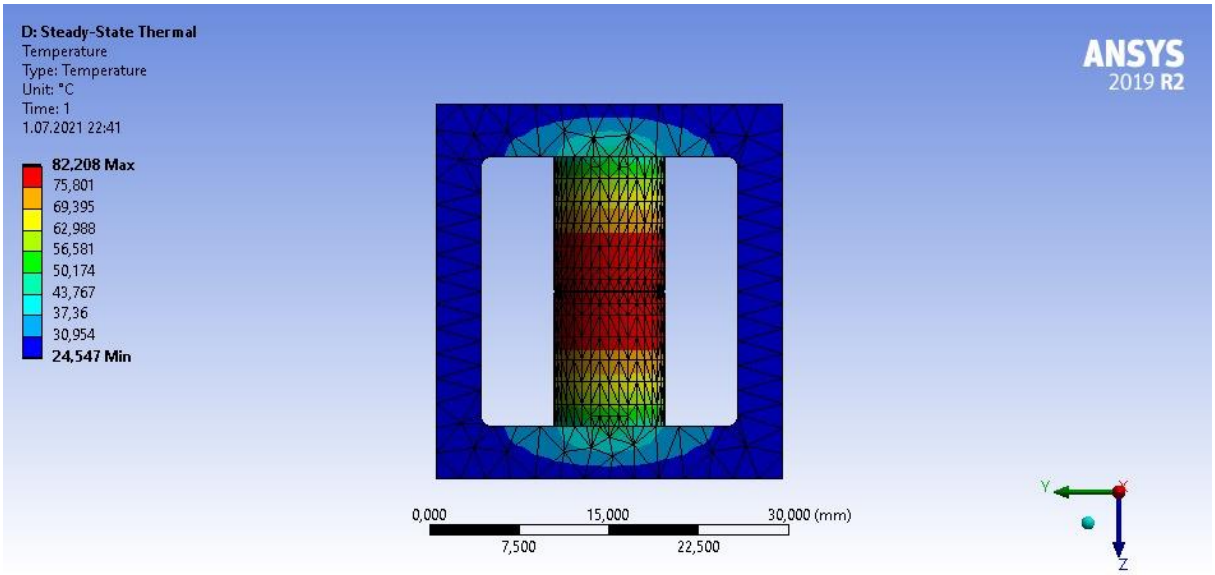

Figure 25 The Result of Thermal Analysis of the Core

10. PCB DESIGN

There are some points to be considered while designing a PCB. When these points are applied as specified, the product shows the expected performance. One of these issues is EMI. Some EMI (Electro-Magnetic Interfere) problems were taken into account when developing a PCB. In the next part, we'll go through the points we've taken into consideration.

Electro Magnetic Interfere (EMI)

Changes in the electric field also affect the magnetic field. Likewise, changes in the magnetic field also affect the electric field. This effect is known as EMI. The tricks to consider about EMI effect while designing PCB are listed below.

The use of sharp bends: The capacitive effect and change in characteristic impedance of the traces are increased when the traces are turned 90˚. As a result, abrupt bends are frequently used in the PCB design stage. Figure 26 shows various examples of potential bends, ranging from the worst to the best.

Figure 26 Corner Examples of Traces from the Worst Case to the Best Case

Grounding: The ground point is utilized as a reference bus in all circuit designs. Using more than one ground line while constructing a PCB may result in a voltage differential between the ground locations. As a result of this circumstance, various references are used in the same circuit design, affecting the circuit's performance.

Trace spacing layout: The conductive paths through which current flows are traces. There is some capacitive interaction between these traces if they are so near to each other. To eliminate or minimize this capacitive effect, the spacing between traces on a PCB is usually left at three times the trace width.

During the design of the board, we have focused on 3 three important points which are the compactness of the board, the isolation barrier between the primary and secondary, and the proper selected width of the planes and tracks between the connections of the power line. The outcome of the board is given in the APPENDIX. As a summary, the dimension of the board is 66.44mm (Length) x 41.15mm (width) x

43.95mm (height). The isolation barrier between the primary and secondary side is 3.048mm, which is much more than desired one (0.255mm). Finally, the PCB is 4 layers, and both inner layers are used to root the grounds and root one or two signals.

The PCB for this project has been developed using the abovementioned techniques and following Figure 27 shows the isometric view of PCB.

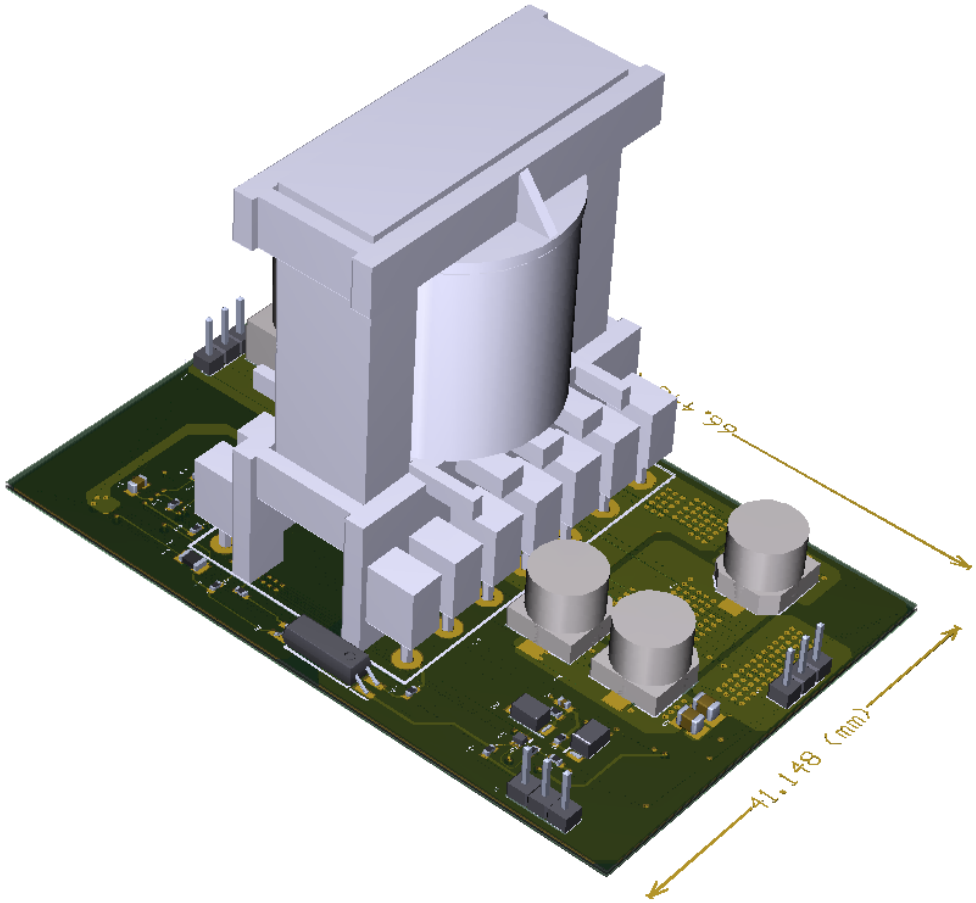

Figure 27 The Isometric view of PCB

11. COST ANALYSIS

The table below shows the cost analysis of the components we have selected. The price of the components is calculated over 1000 pieces.

Table 2 Cost Analysis of the Overall Project

Manufacturer Name	Quantity	Digi-Key Part Number	Unit Price($)	Price($)
Analog Devices Inc.	1000	LT8316IFE#PBF-ND	3.68	3679.50
EPCOS- TDK Electronics	2000	495-5450-ND	0.43	855.42
KEMET	3000	399-EDH107M016A9GAATR-ND	0.09	283.17
Venkel	2000	2679-C1206X5R160-476MNETR-ND	0.69	1374.98
Samsung Electro-Mechanics	7000	1276-1096-2-ND	0.02	133.84
Taiyo Yuden	4000	587-5514-1-ND	0.02	60.96
Venkel	1000	2679-LCR2512-R028FTTR-ND	0.19	189.27
Yageo	1000	311-69.8KCRCT-ND	0.01	7.59
Yageo	1000	311-20.0KHRCT-ND	0.00	4.36
Samsung Electro-Mechanics	2000	1276-3431-1-ND	0.01	19.40
Vishay Dale	1000	BC4966CT-ND	0.15	148.12
Vishay Dale Thin Film	1000	764-1550-2-ND	0.22	220.00
TE Connectivity Passive Product	1000	A121294CT-ND	0.21	211.73
Taiyo Yuden	1000	587-4896-1-ND	0.09	86.22
TDK Corporation	1000	445-7479-1-ND	0.07	72.45
Würth Elektronik	3000	732-7532-1-ND	0.02	46.44
AVX Corporation	1000	478-1282-1-ND	0.03	28.81
Yageo	1000	311-3383-1-ND	0.03	33.05
Rohm Semiconductor	1000	RB058L150TE25TR-ND	0.15	150.68
Diodes Incorporated	1000	1SMB5953B-13DI-ND	0.14	136.13
Taiwan Semiconductor Corporation	1000	TSPB20U80SS2G-ND	0.63	627.60
ON Semiconductor	1000	SURA8260T3GOSCT-ND	0.16	160.27
Delta Electronics/Cyntec	1000	2037-RL1632T4F-R001-FNHCT-ND	0.18	179.44
IXYS	1000	IXTA10P50P-TRLTR-ND	4.27	4273.39
Diodes Incorporated	1000	DDZ9697DICT-ND	0.06	56.10
Stackpole Electronics Inc	2000	RMCF0402FT100RCT-ND	0.00	5.48
KOA Speer Electronics, Inc.	1000	2019-RN73H1ETTP4931B25CT-ND	0.11	105.00
KOA Speer Electronics, Inc.	1000	2019-RN73H1ETTP3121D50CT-ND	0.08	78.40
SMC Diode Solutions	2000	1655-1N4007FLCT-ND	0.03	61.38
KOA Speer Electronics, Inc.	1000	2019-RN73H1ETTP8871F50CT-ND	0.08	78.40
Bourns Inc.	1000	CR0402-JW-753GLFCT-ND	0.00	3.50
Vishay Dale	1000	541-RCS040230K0FKEDCT-ND	0.02	17.71
Nichicon	1000	493-6711-2-ND	0.39	394.96
Samtec Inc.	4000	SAM10770-ND	0.42	1680.64
Vishay Dale	1000	541-3971-1-ND	0.01	6.10
Yageo	2000	13-AF0402JR-071KLCT-ND	0.01	13.10
Vishay Dale	1000	541-4715-1-ND	0.01	6.10
TE Connectivity Passive Product	1000	A116024CT-ND	0.17	169.96
Analog Devices Inc.	1000	LT6107HS5#TRMPBFTR-ND	1.96	1963.50
Texas Instruments	1000	LMH6618MK/NOPBTR-ND	2.38	2378.25
Maxim Integrated	1000	LM4041CIM3-1.2+TCT-ND	3.17	3165.00
Diodes Incorporated	1000	DMN26D0UDJ-7DICT-ND	0.12	118.80
Texas Instruments	1000	296-49459-2-ND	3.53	3533.25
Infineon Technologies	1000	IPD80R280P7ATMA1CT-ND	1.89	1888.20
PCBWay	1000	PCB	0.45	450.00
			TOTAL COST	**29156.65**

12. CONCLUSION

This report includes the topology selection, controller selection after topology selection, transformer design, component selection, implemented protection circuits, overall simulation results, loss calculations, thermal analysis, PCB design, and cost analysis of the project.

For the simulation part of the project, there are some important parts of the project must be completed before going on details of simulation. At first, a topology must had been selected and we selected the Flyback topology. After topology selection, we found a controller which satisfies the needs of the system. In addition, there is a need for a transformer as we use Flyback topology. An Excel program is developed to calculate the properties of the transformer recursively. When we finished the transformer design part, we run a finite element analysis on the ANSYS to prove the non-saturated behavior of the converter during the operation. After that, we continued with the passive element selection of the converter and selection of the semiconductor devices of the flyback topology and snubber circuit. When the component selections and the transformer design parts are completely done, we conducted the simulations and prove that the converter satisfies the features wanted at the project definition. Thermal calculations were made and observed that our design also satisfies thermal requirements. Finally, we implemented reverse polarity protection at the input and overcurrent protection at the output. These protection circuits increase the reliability of our converter design. Since all components and subcircuits were ready, we started to design the PCB. Final cost of the design is calculated using BOM manager tool of DigiKey.

The main purpose of the report is to prove that the designed converter is satisfying the requirements, and at the end of it, we can claim that we are satisfying all needs of the project.

13. REFERENCES

1. Topology Key to Power Density in Isolated DC-DC Converters. (n.d.). Retrieved April 27, 2021, from https://www.powerelectronics.com/technologies/dc-dc-converters/article/21854364/topology-key-to-power-density-in-isolated-dcdc-converters

14. APPENDIX

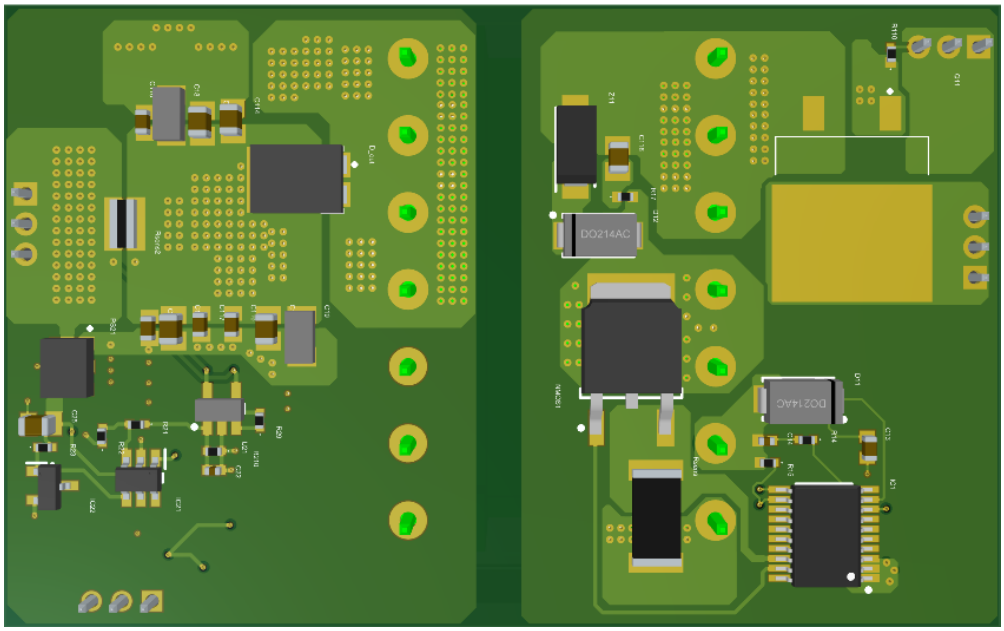

Figure 28 Bottom View of PCB

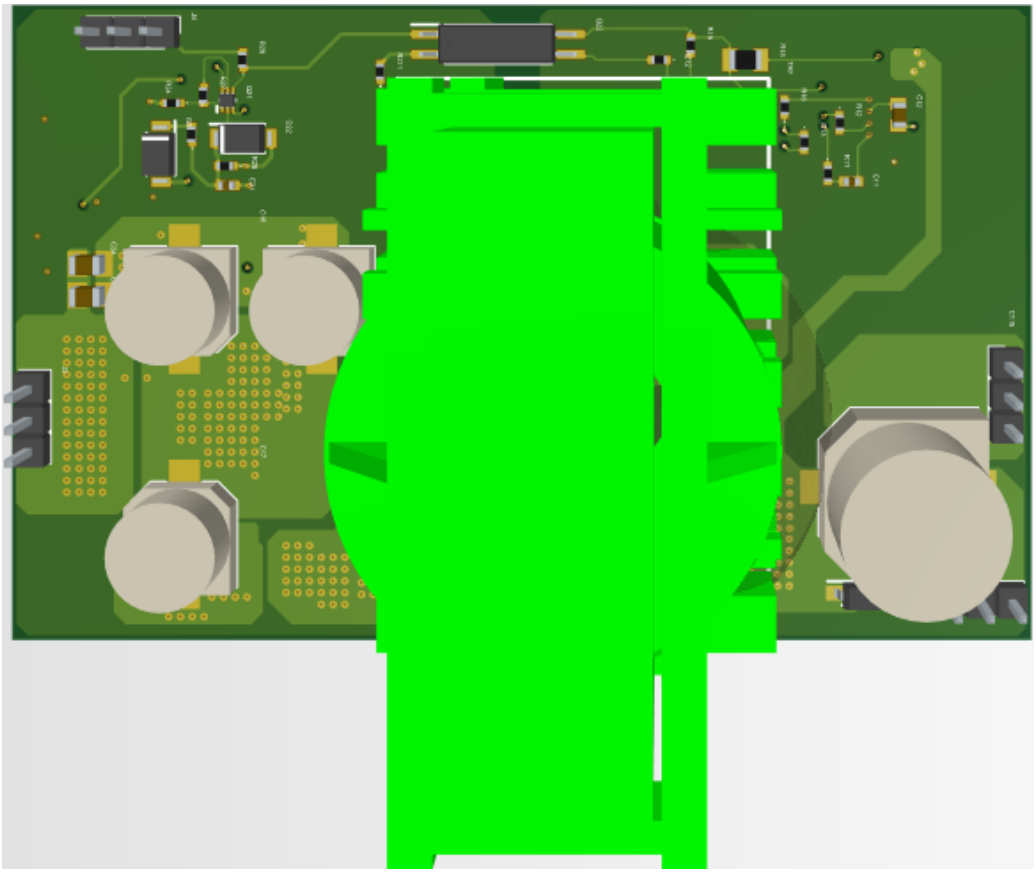

Figure 29 Top View of PCB

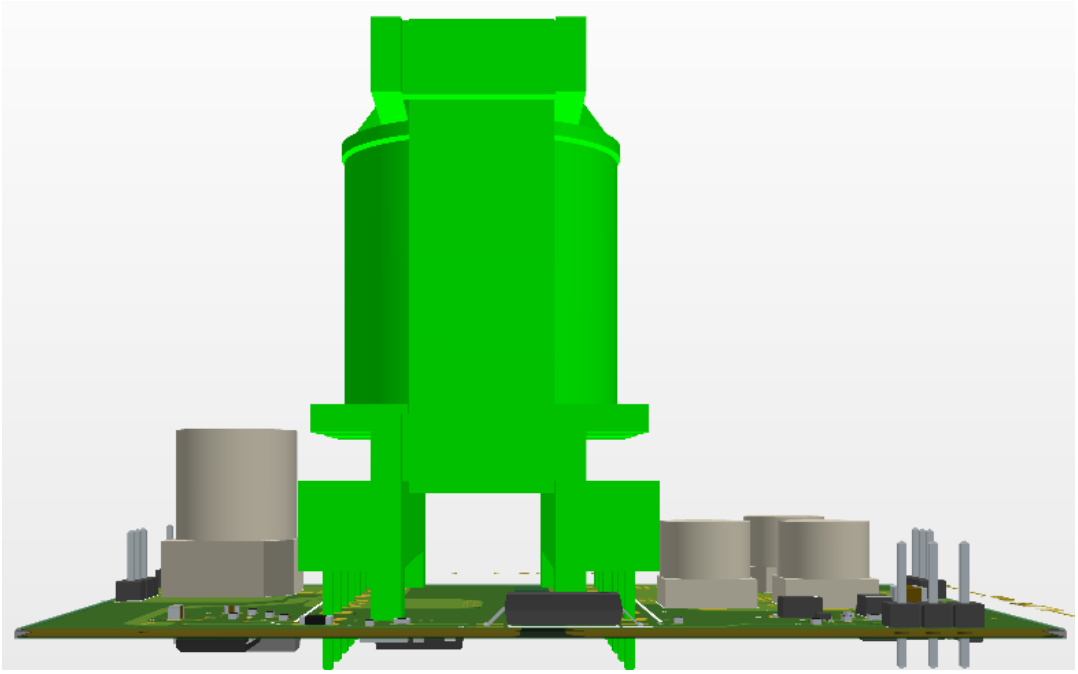

Figure 30 Front View of PCB

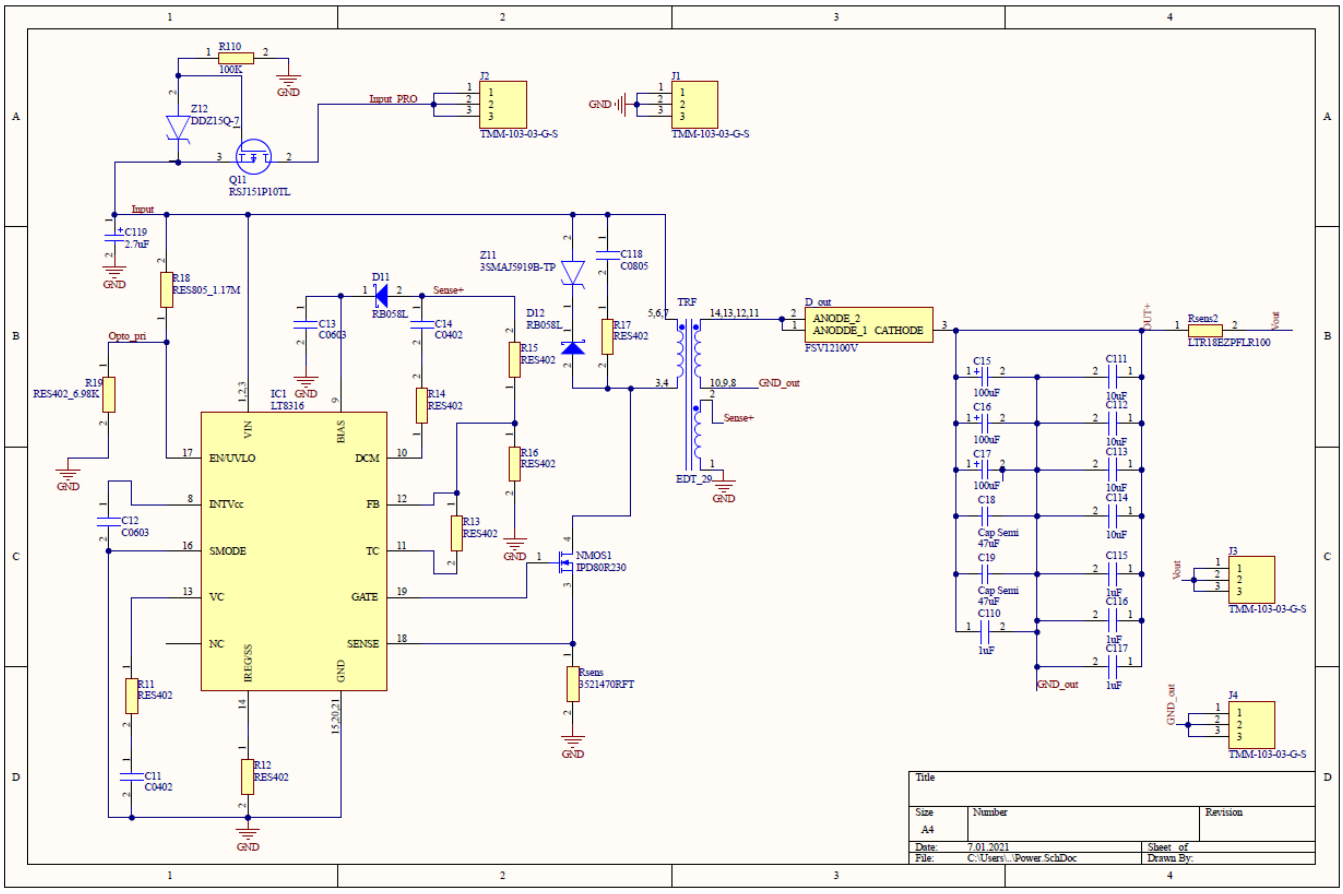

Figure 31 Schematic of the Design-1

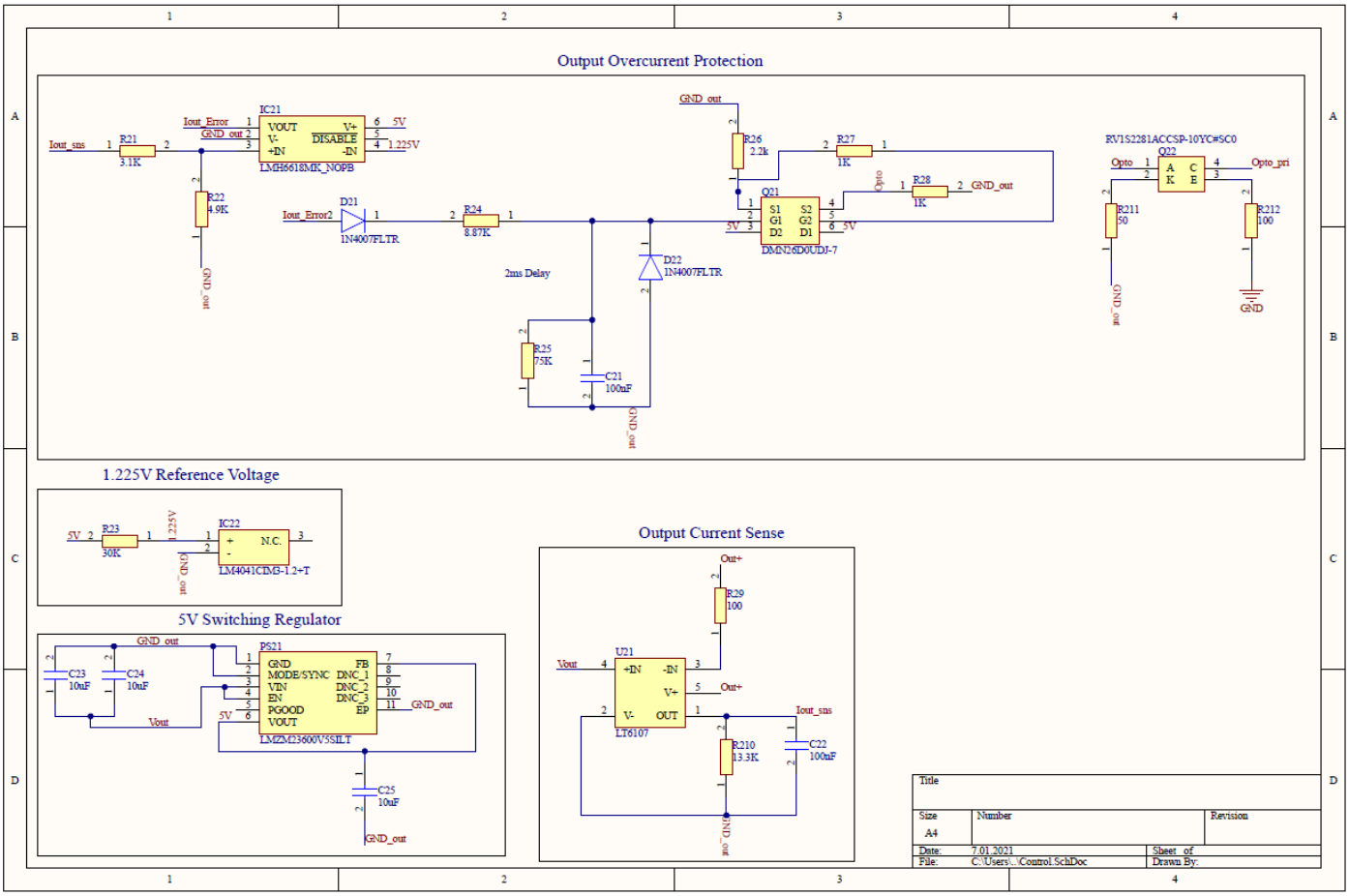

Figure 32 Schematic of the Design-2

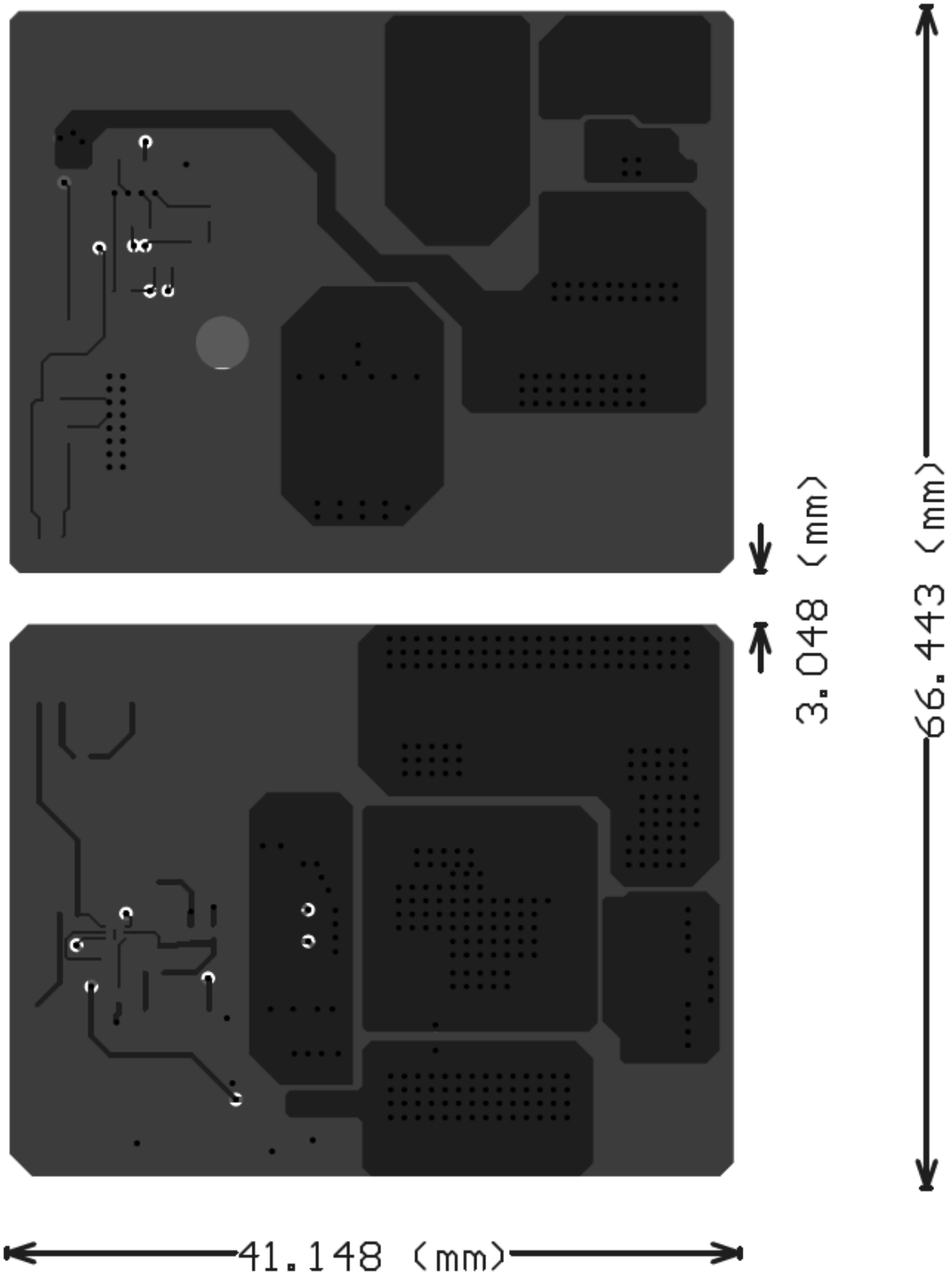

Figure 33 Dimensions of the PCB