CSE 331/503

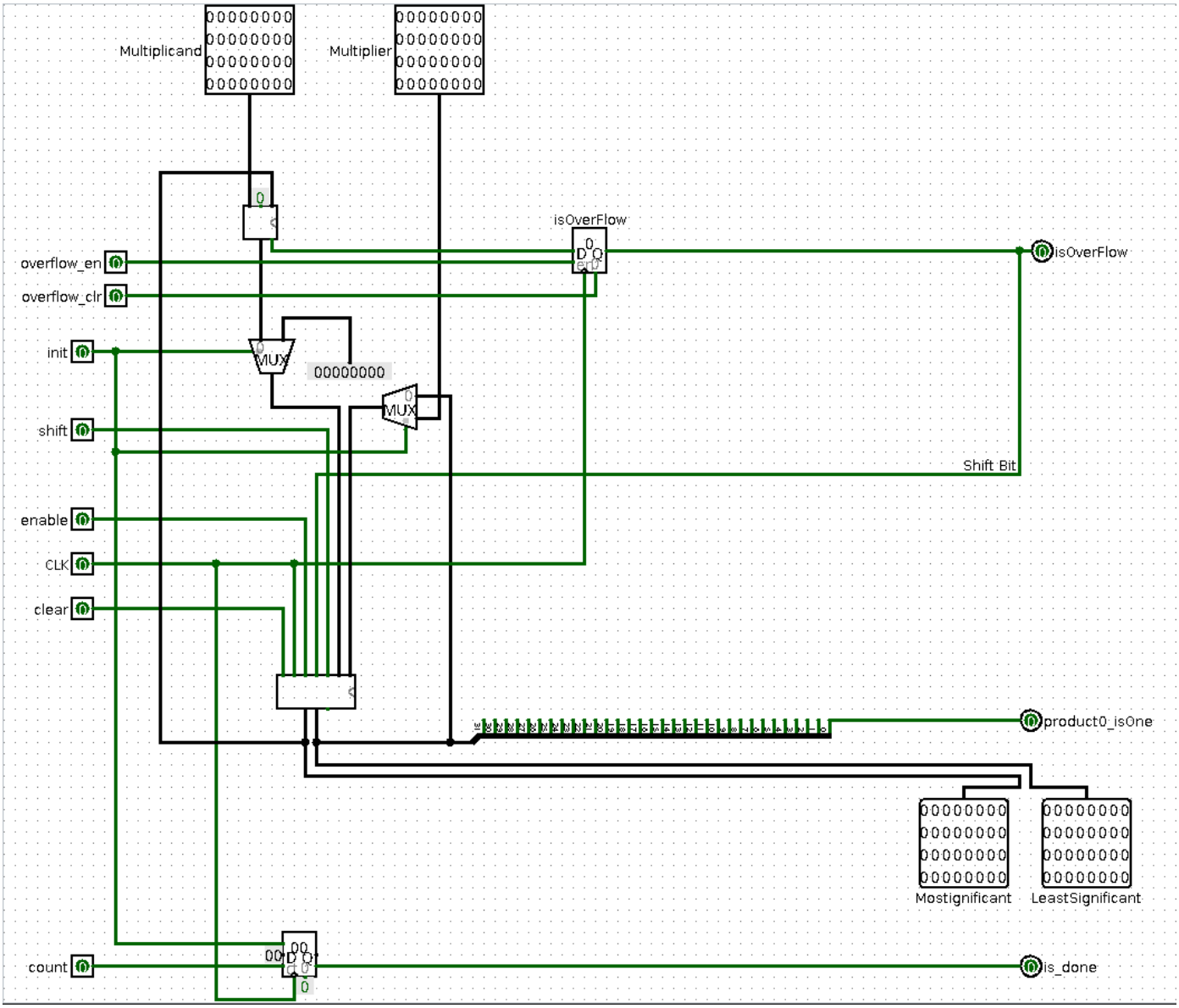
Computer Organization

Homework 3

Ali Bahar – 171044066

Datapath Design:

I have designed adder and shift register.



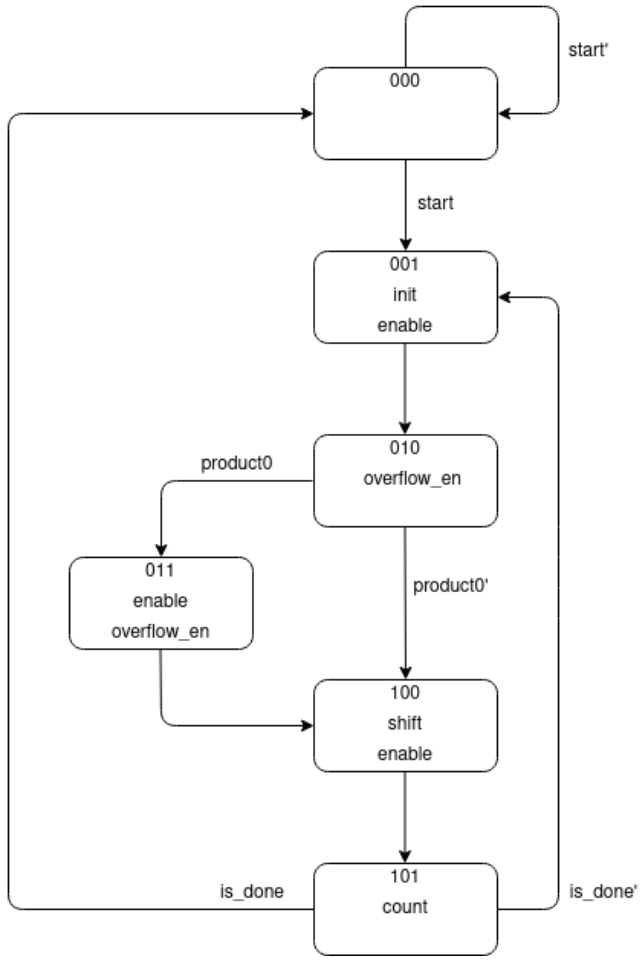
Truth Table:

s2	s1	s0	start	Product_0	Is_done	n2	n1	n0
0	0	0	0	x	x	0	0	0
0	0	0	1	x	x	0	0	1
0	0	1	x	x	x	0	1	0
0	1	0	x	0	x	1	0	0
0	1	0	x	1	x	0	1	1
0	1	1	x	x	x	1	0	0
1	0	0	x	x	x	1	0	1
1	0	1	x	x	0	0	1	0
1	0	1	x	x	1	0	0	0

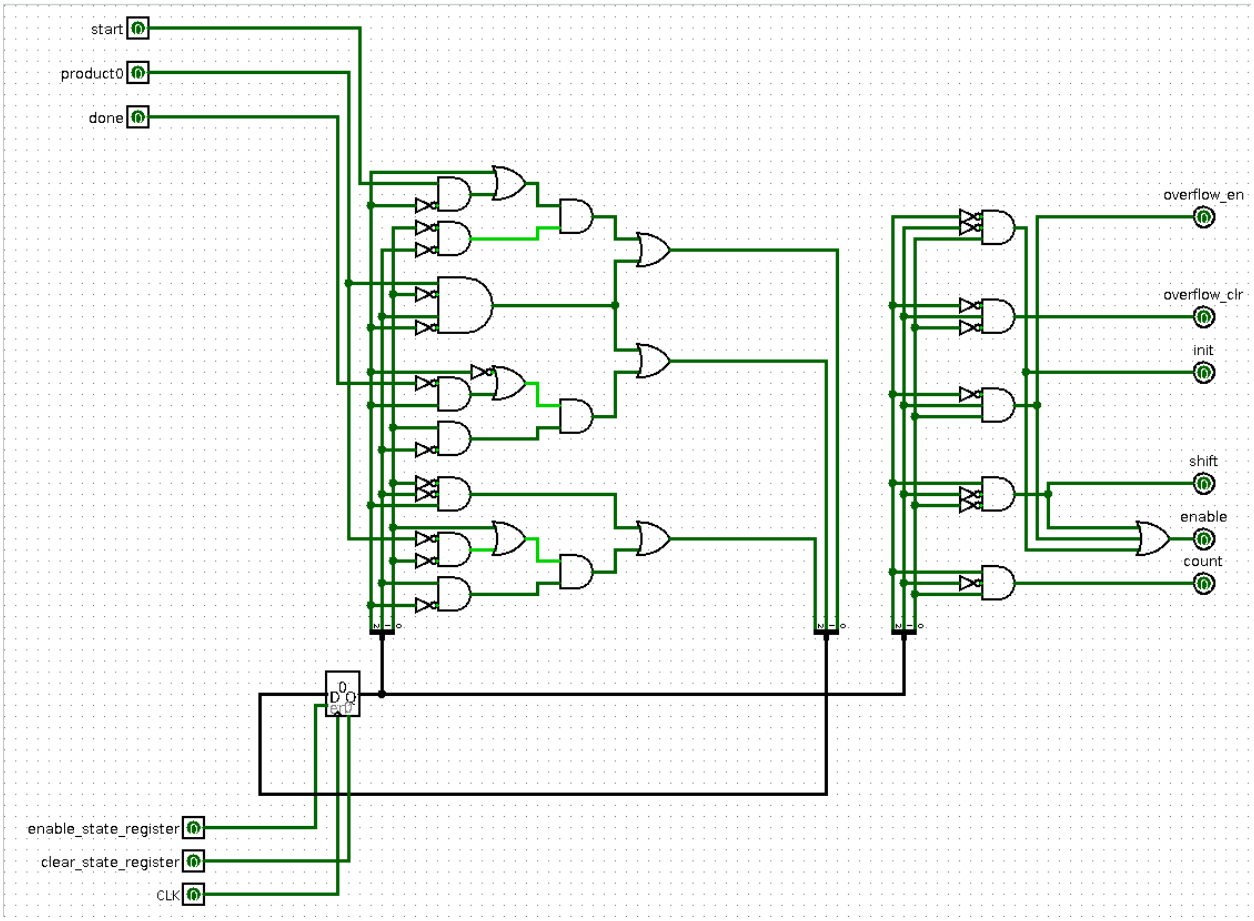
n2 = s2’.s1.(s0’p’+s0’) + s2.s1’.s0’

n1 = s1’.s0.(s2’ + s2.done’) + s2’.s1.s0

n0 = s1’.s0’(s2’.start + s2) + s2’s1s0’.p

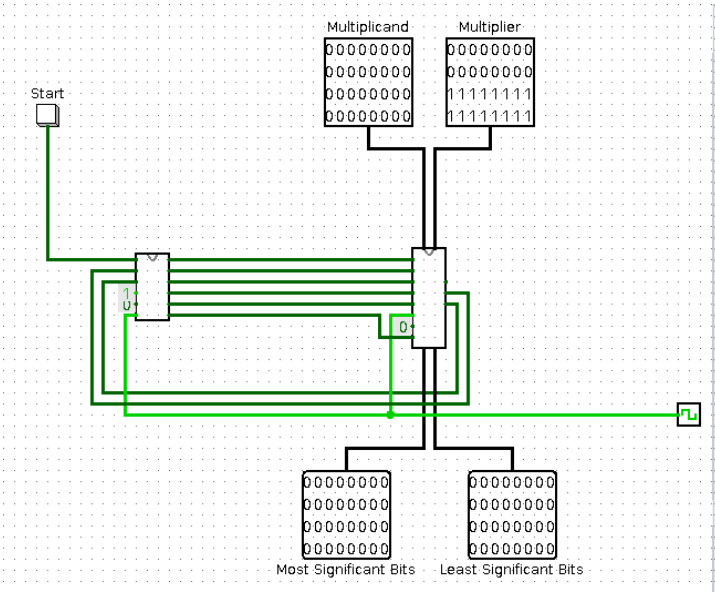


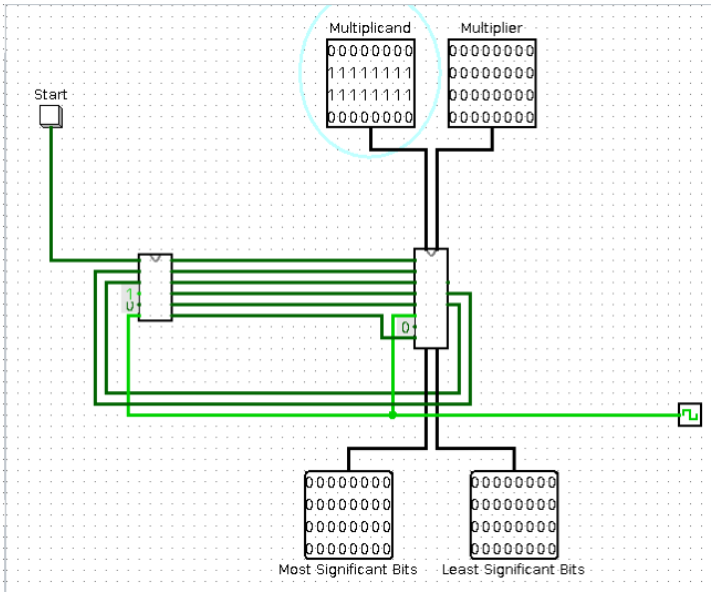
Control Unit Design:



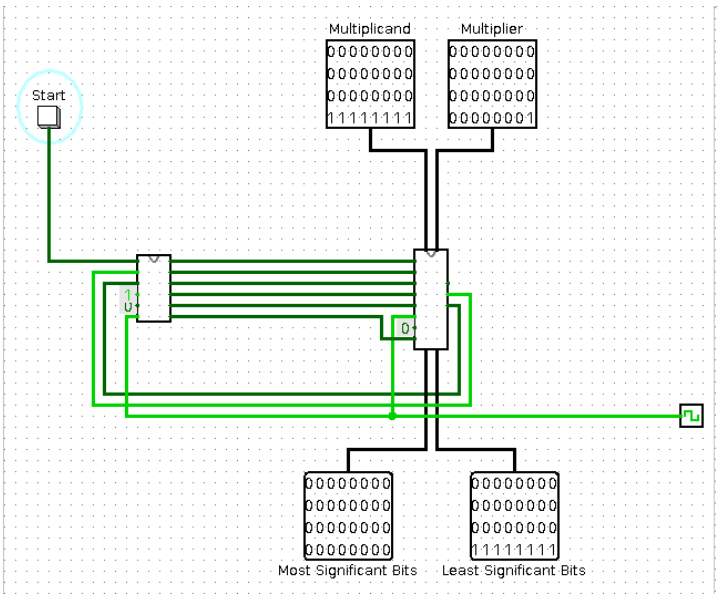
All Tests are added to ”mult32.circ”.

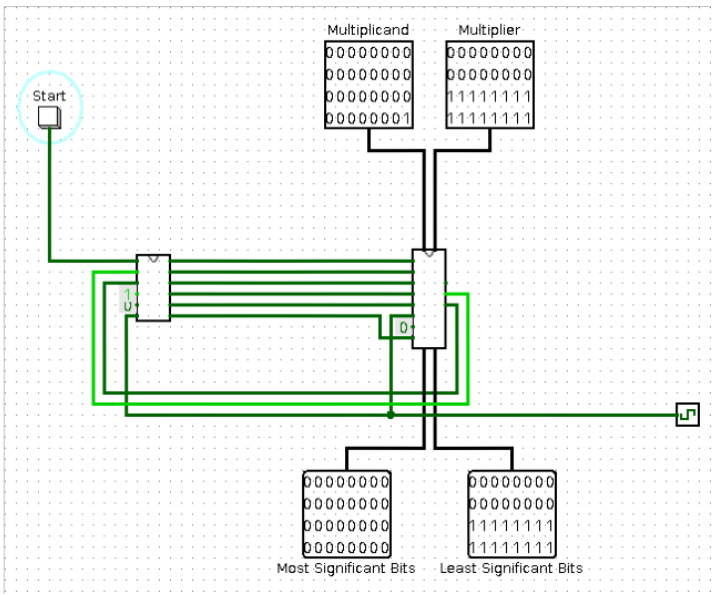
Test Case 1:



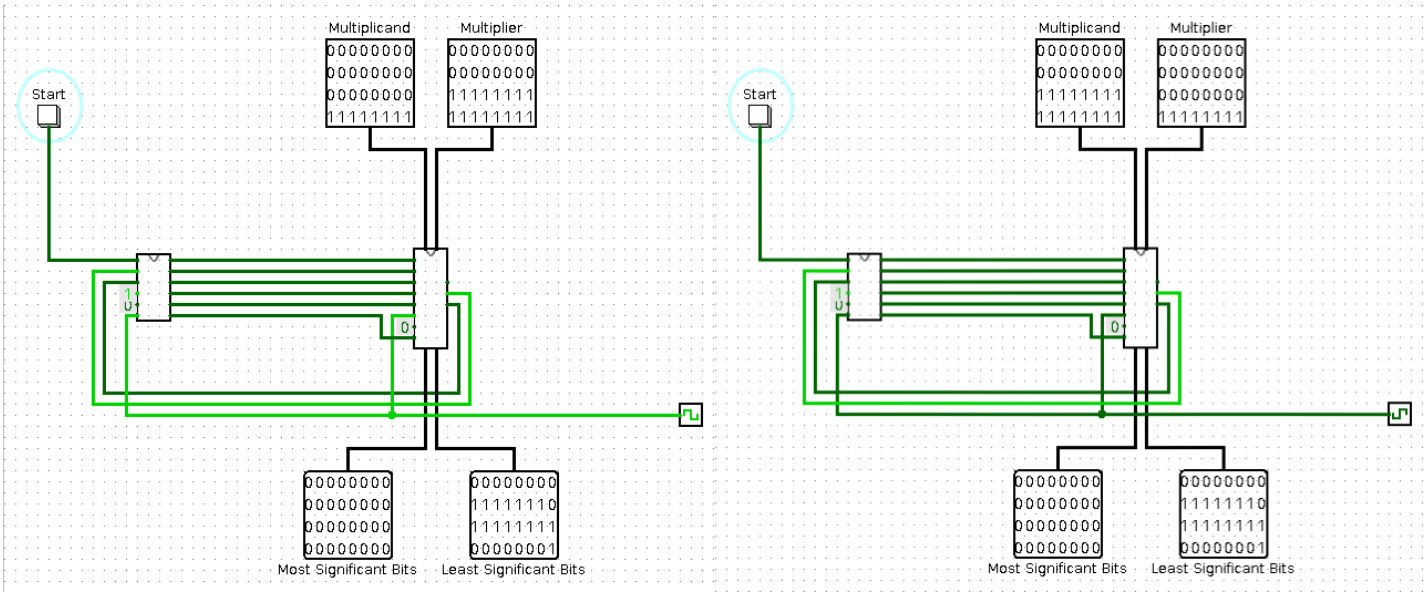


Test Case 2:

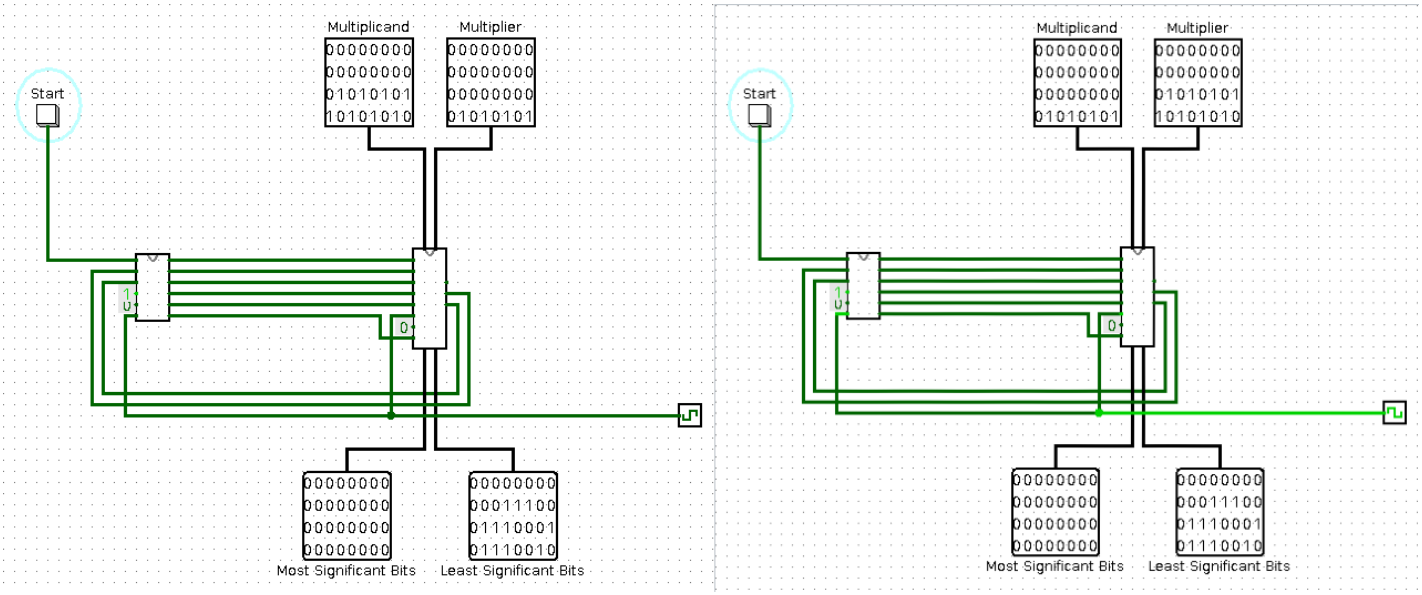




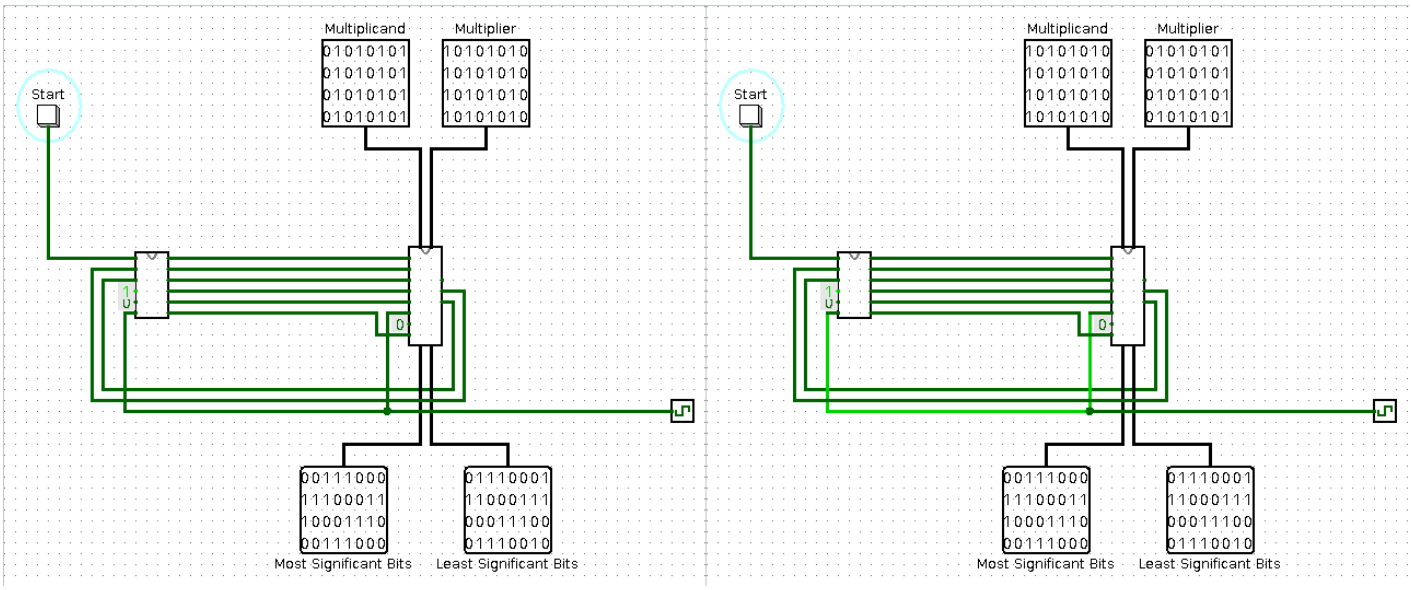
Test Case 3:



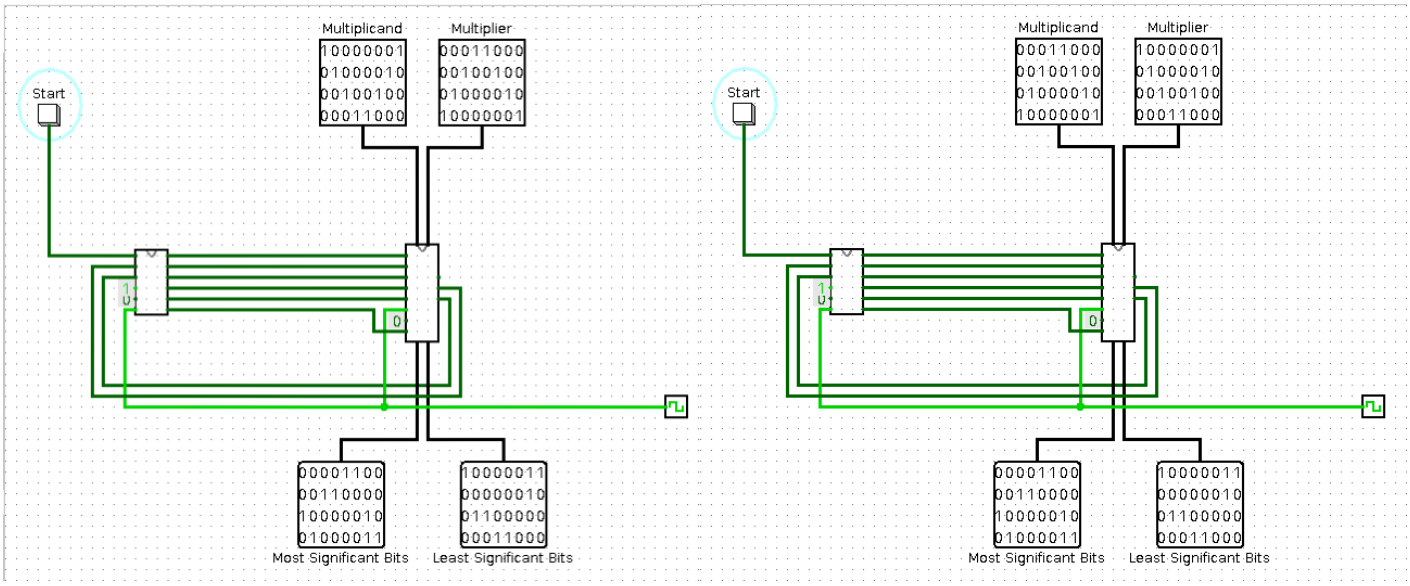
Test Case 4:



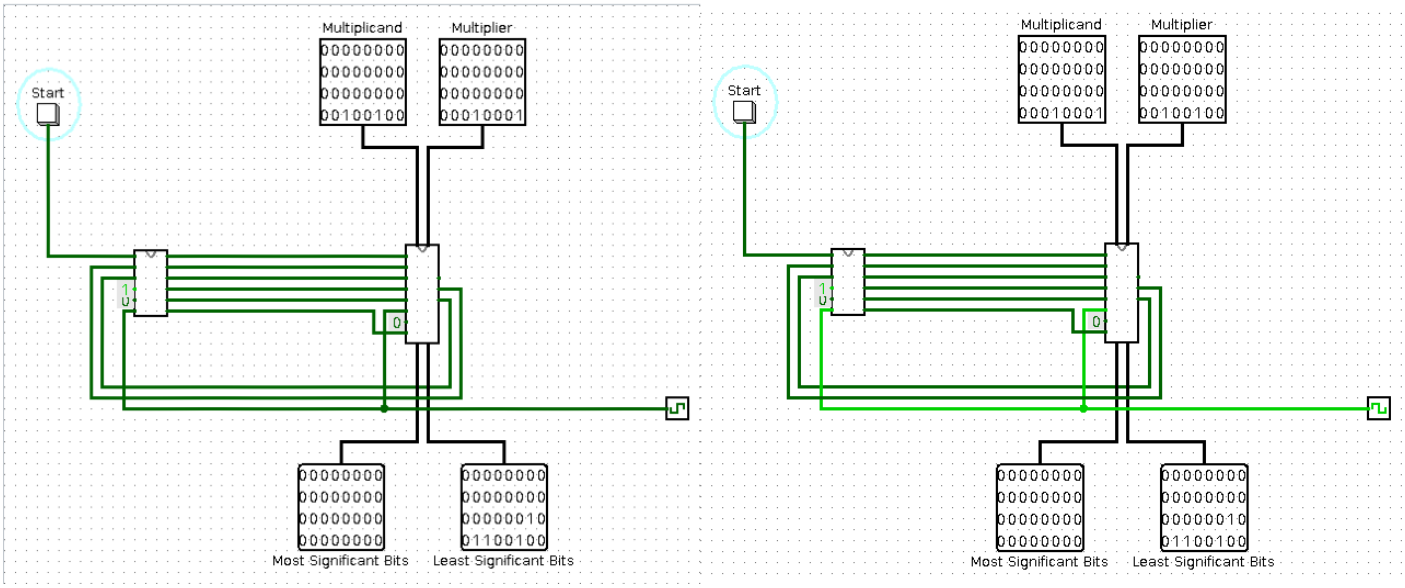
Test Case 5:



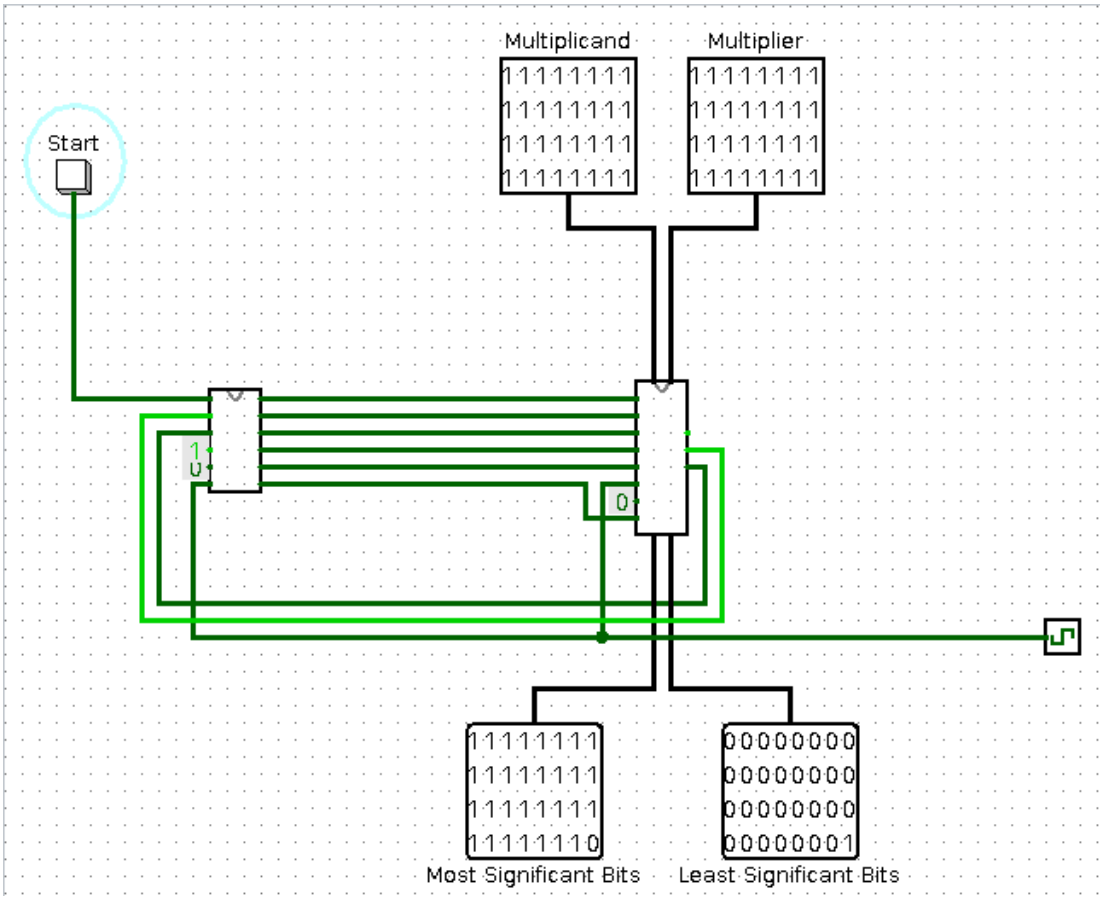
Test Case 6:

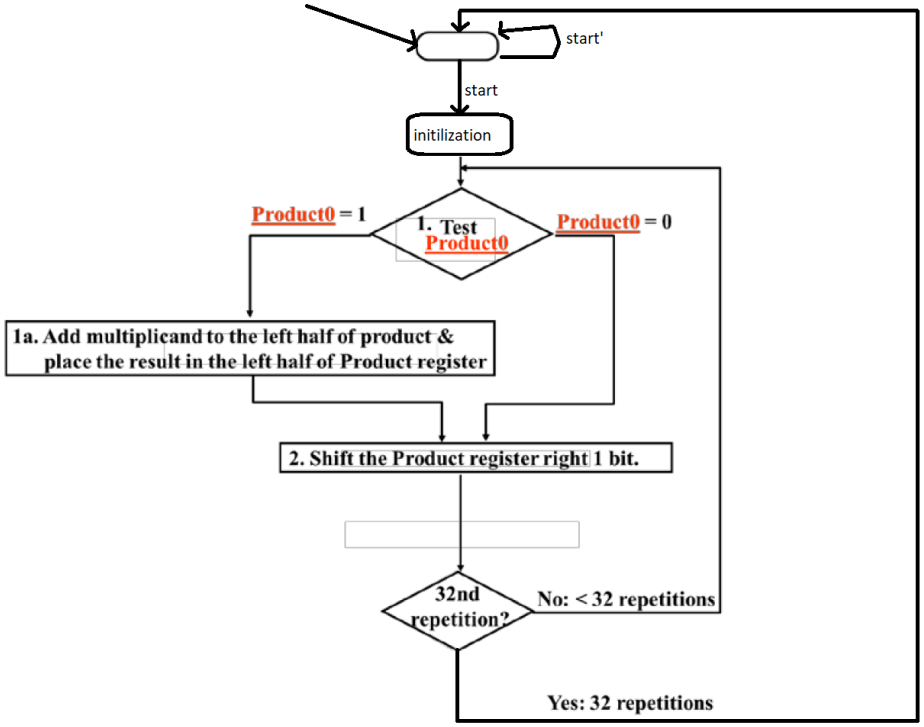


Test Case 7:



Test Case 8:




start'
start
initilization
Product0 = 1
1. Test Product0
Product0 = 0
1a. Add multiplicand to the left half of product & place the result in the left half of Product register
2. Shift the Product register right 1 bit.
32nd repetition?
No: < 32 repetitions
Yes: 32 repetitions