Digital Logic Design – Fall 2024

CA4 - Sequential Circuit Design

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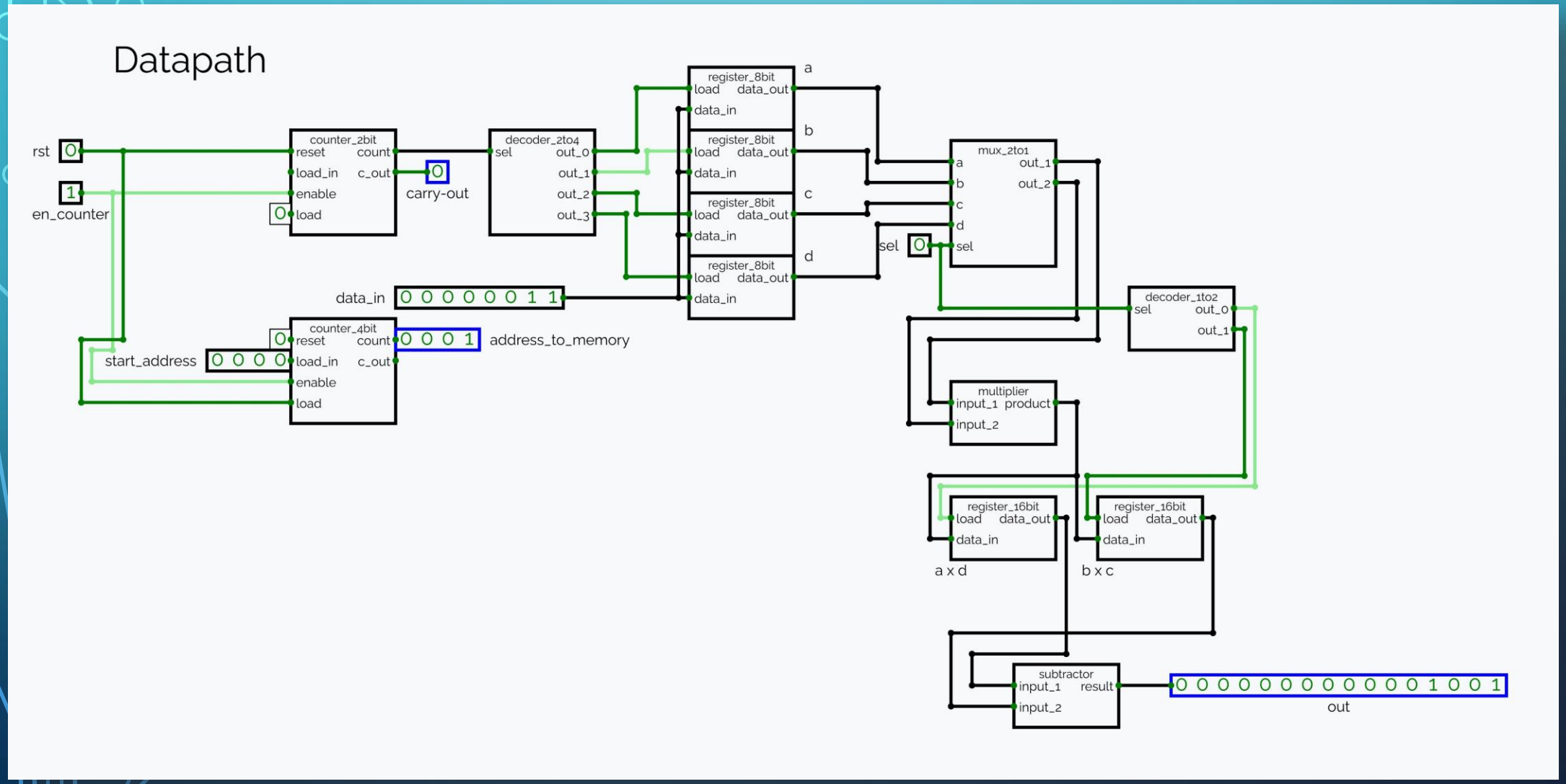
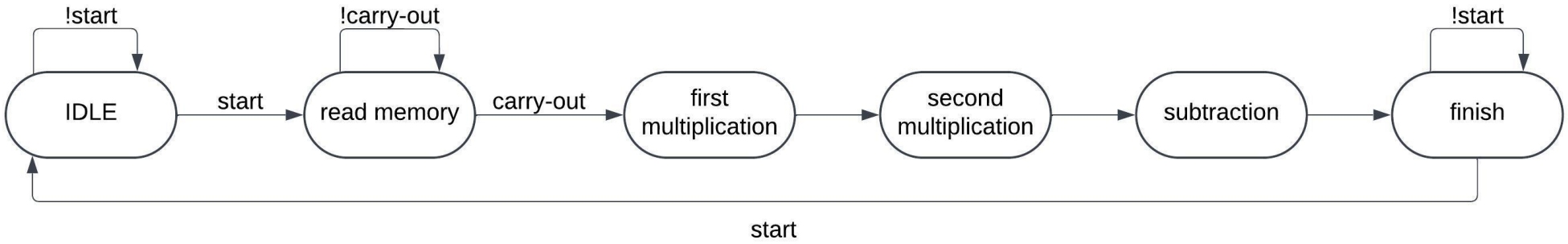
Datapath


Datapath
rst
0
1
en_counter
counter_2bit
reset
count
load_in
c_out
enable
load
carry-out
decoder_2to4
sel
out_0
out_1
out_2
out_3
register_8bit
load
data_out
data_in
a
b
c
d
mux_2to1
sel
data_in
0 0 0 0 0 0 1 1
counter_4bit
start_address
0 0 0 0
0 0 0 1
address_to_memory
decoder_1to2
multiplier
input_1
product
input_2
register_16bit
a x d
b x c
subtractor
result
0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1
out

Controller - FSM

Moore-type state diagram



IDLE: rst = 1, done = 0, sel = 0, en_counter = 0

read memory: rst = 0, en_counter = 1

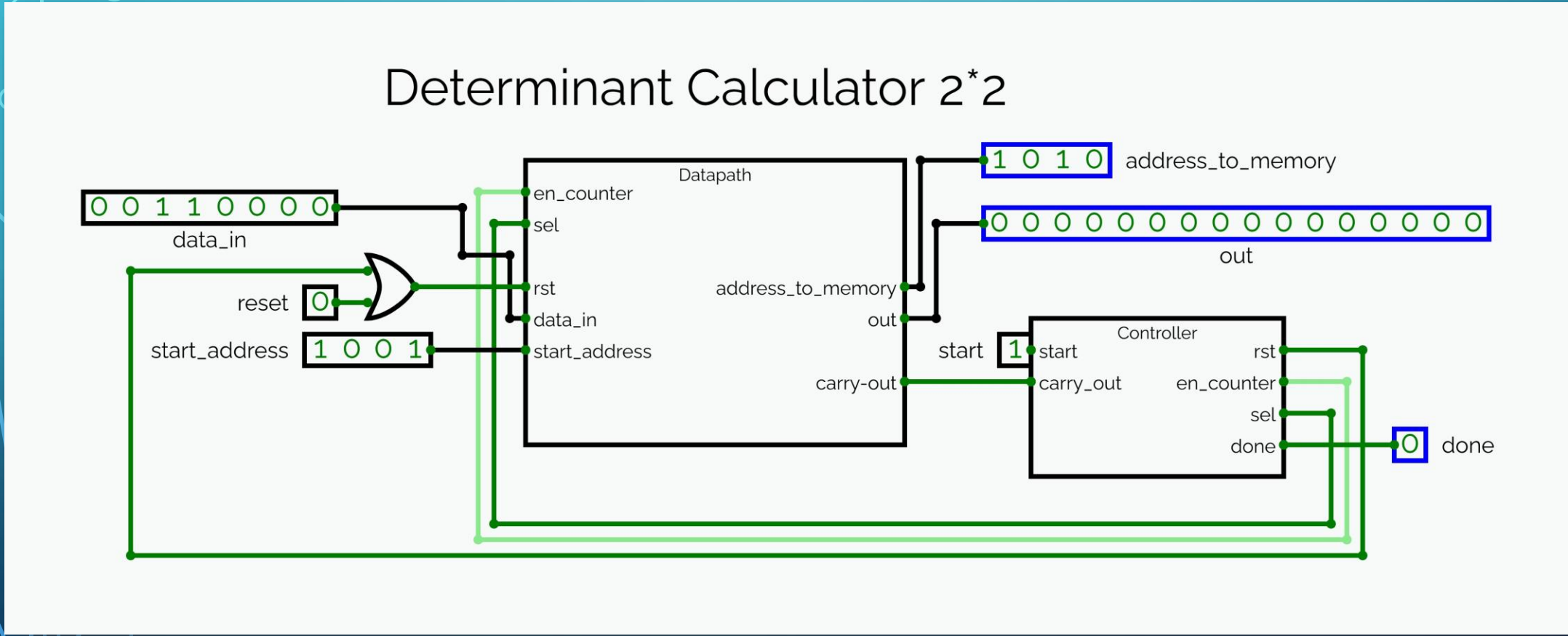
first multiplication: en_counter = 0

second multiplication: sel = 1

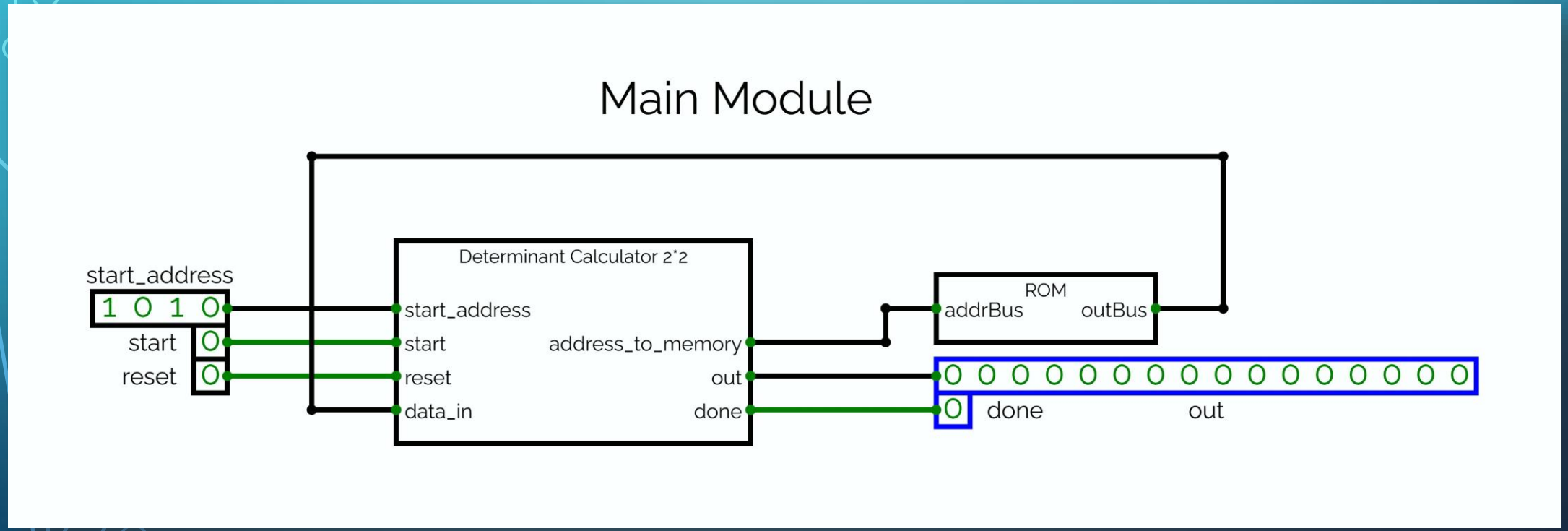
subtraction

finish: done = 1

Determinant Calculator 2*2



Main Module


Main Module
start_address
1 0 1 0
start
0
reset
0
Determinant Calculator 2*2
start_address
start
reset
data_in
address_to_memory
out
done
ROM
addrBus
outBus
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0
done
out

Main Module (Waveforms from TB)

In this testbench, radix is on decimal and after turning off the reset and turning on the start signal, the start address is 2. The calculation will be completed and the output is 3813 and done signal is high. Before that the start address was changed to 5. As we can see the output is -3072 and done signal is high and it's true. The calculations for start address = 4, have not been performed because the start signal is low and done signal remains high until start is low. Outputs like 5888 and 7552 are not valid because done signal is low.