Digital Logic Design – Fall 2024

CA2 – Design and implementation of an ALU

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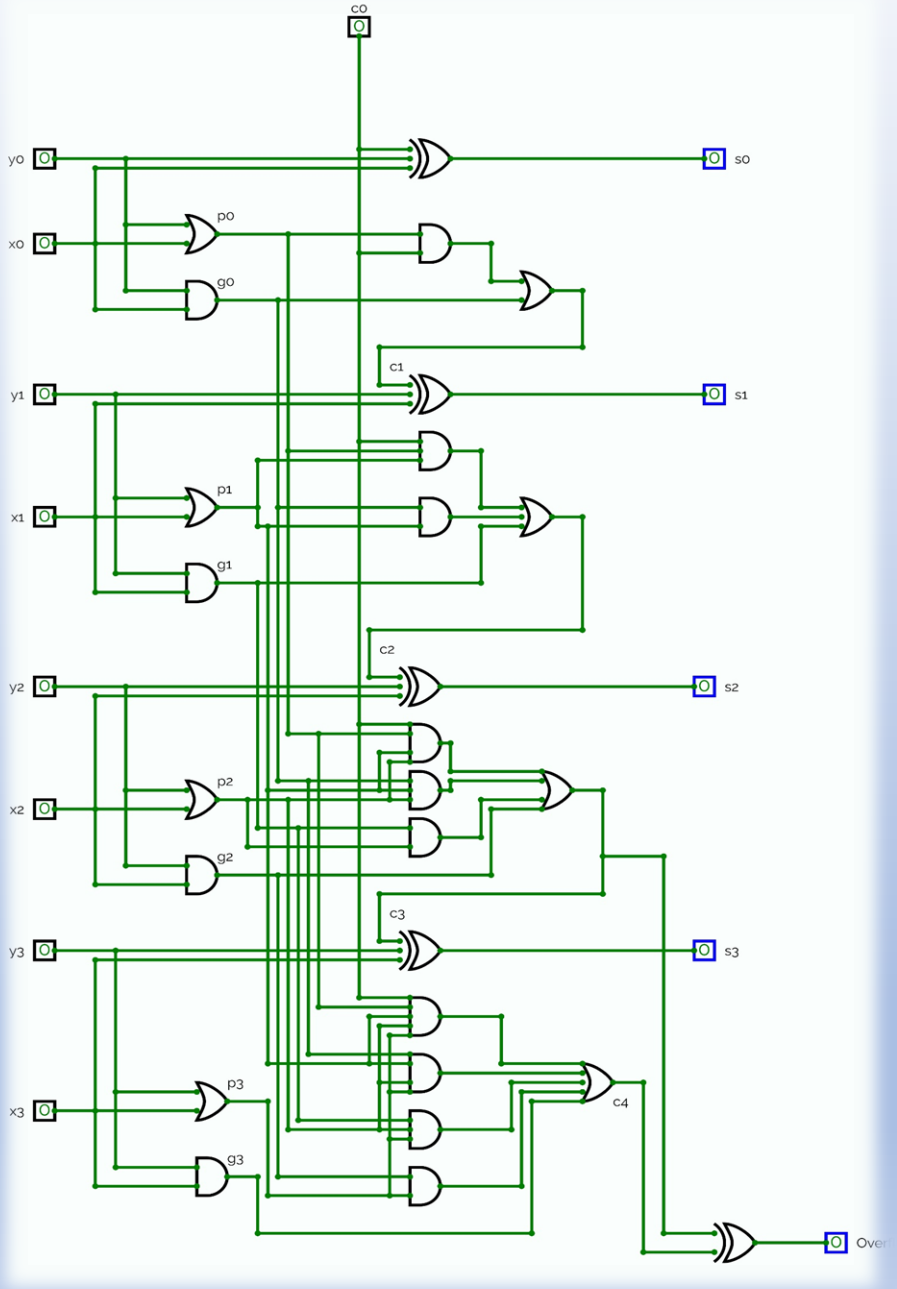
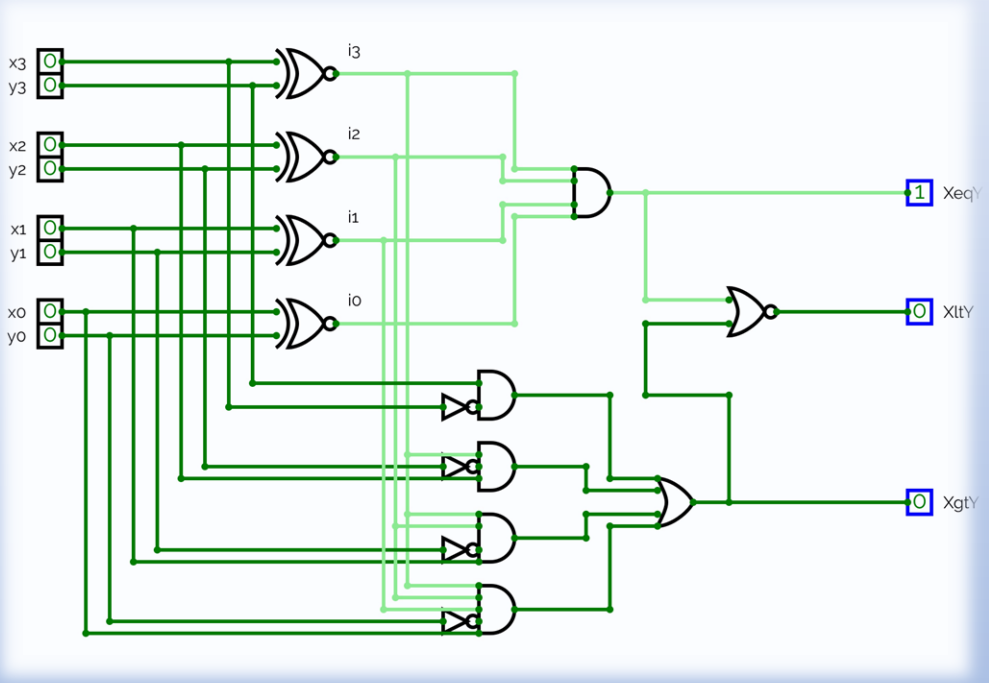


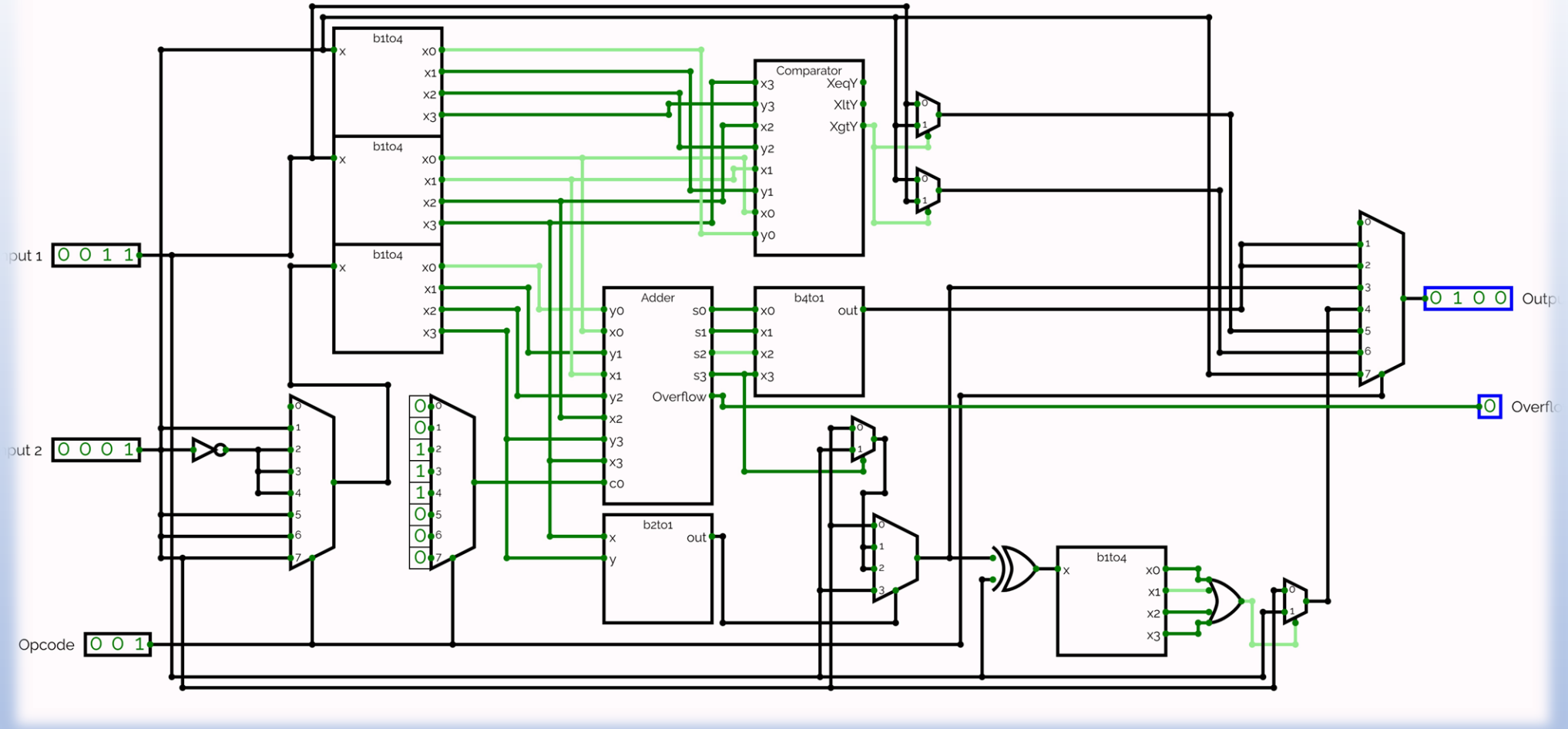
The view of a

4-bit Carry Lookahead Adder

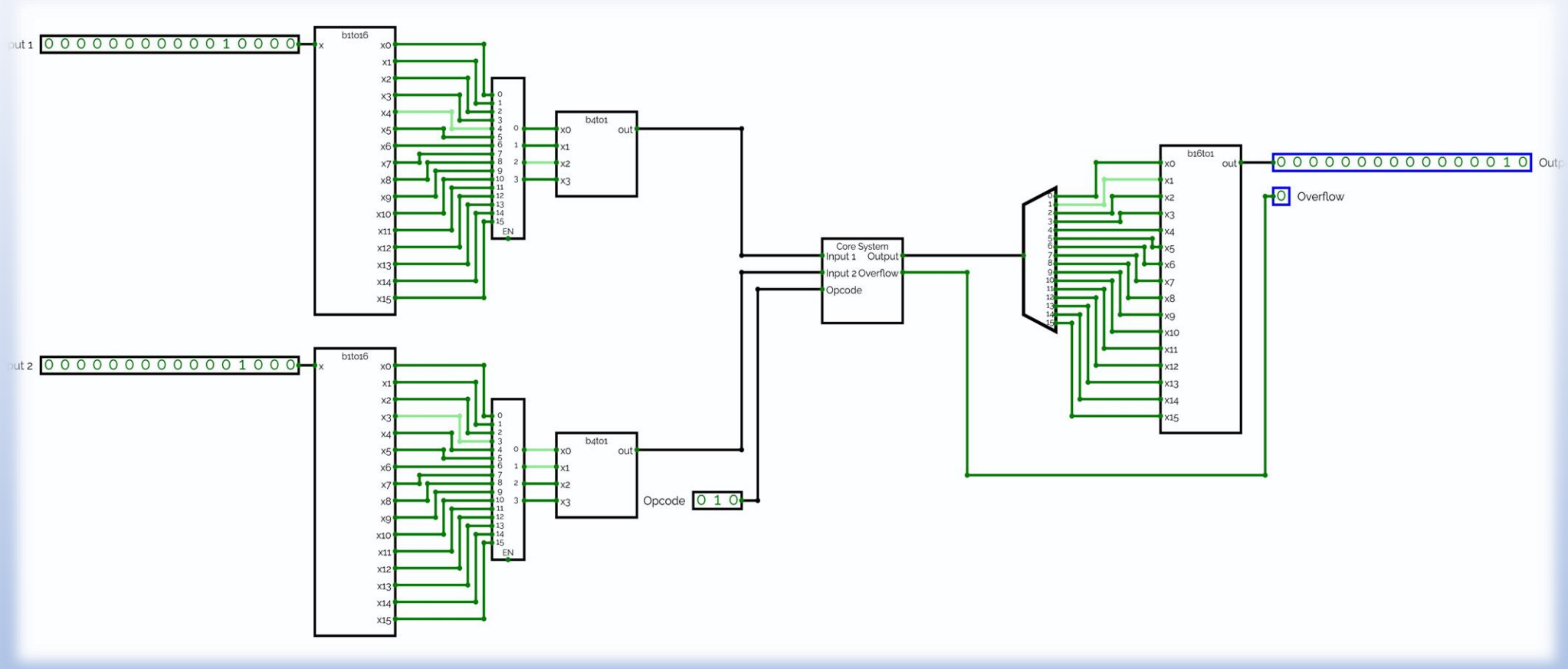


The view of a 4-bit Comparator

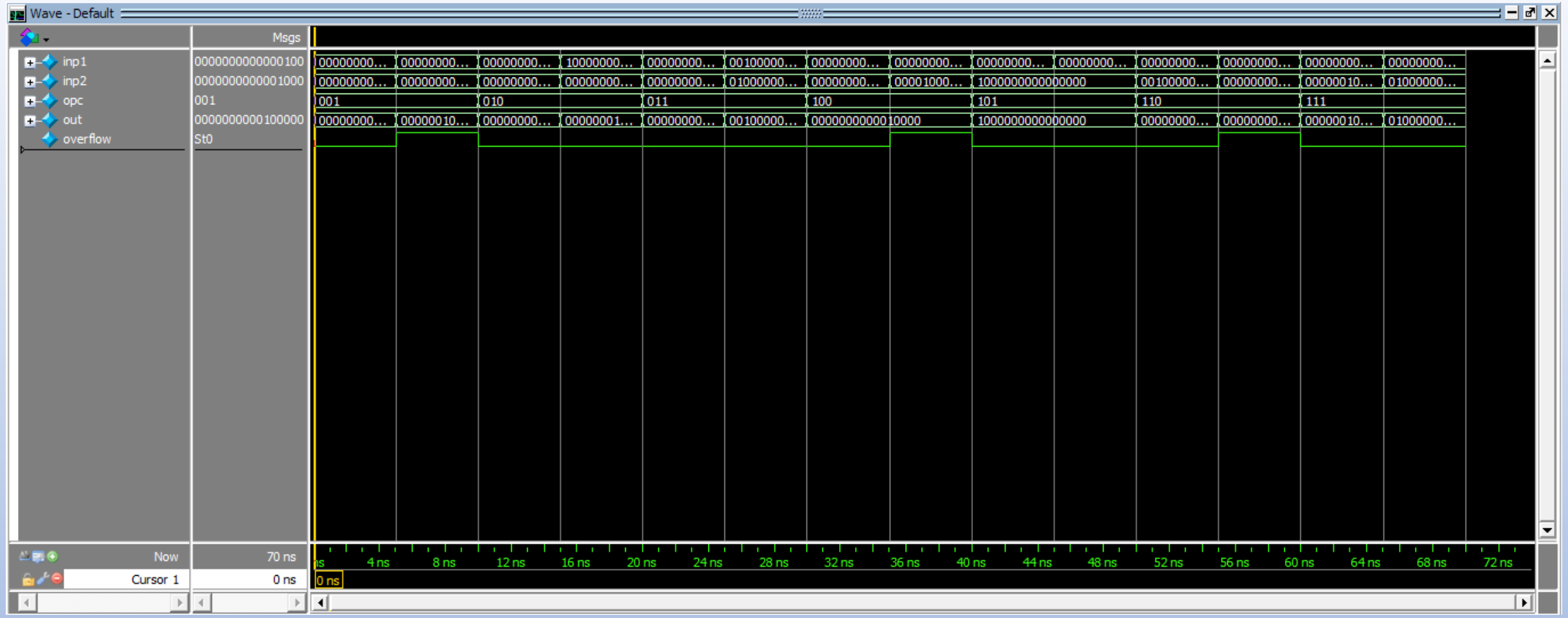
It will compare two numbers, by considering two's complement format.



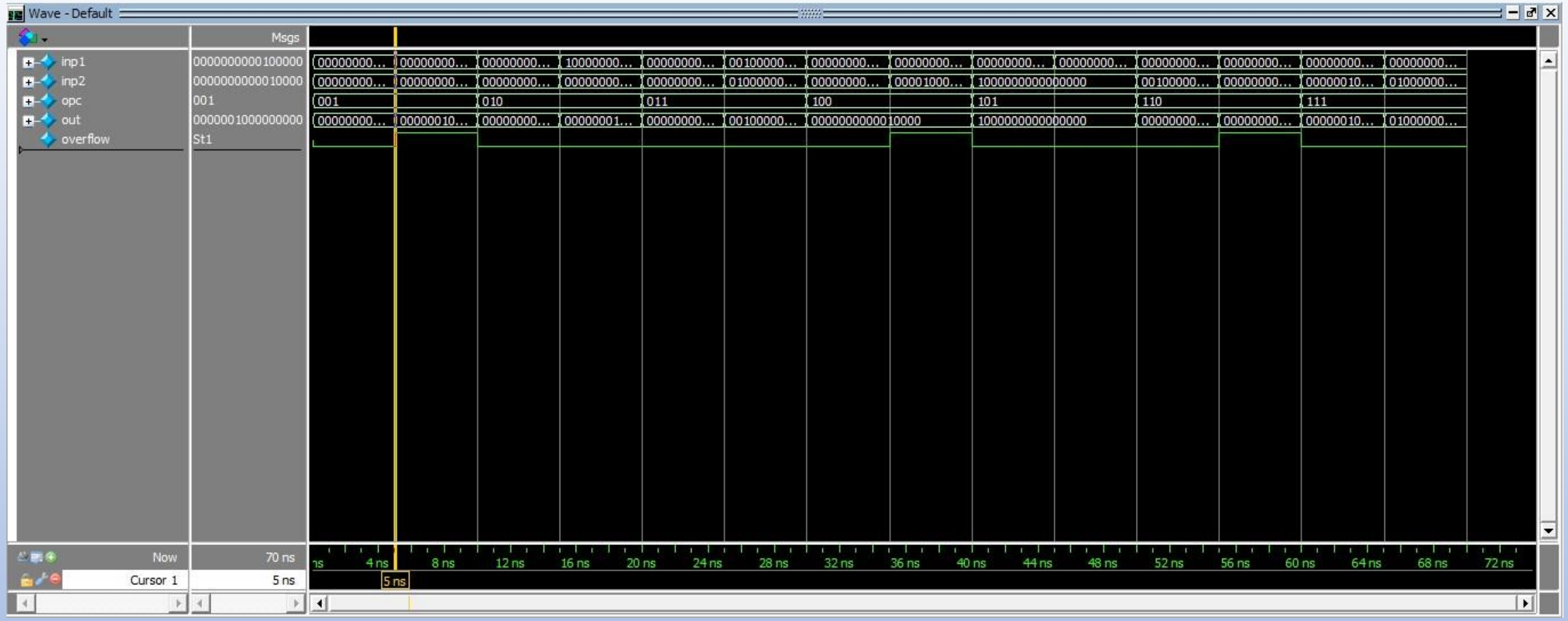
This is the view of the core system which takes two 4-bits inputs and the opcode and then will do the propriate arithmetic operation according to value of the opcode. The output is a 4-bits number. We also have overflow output using in addition and subtraction operations.



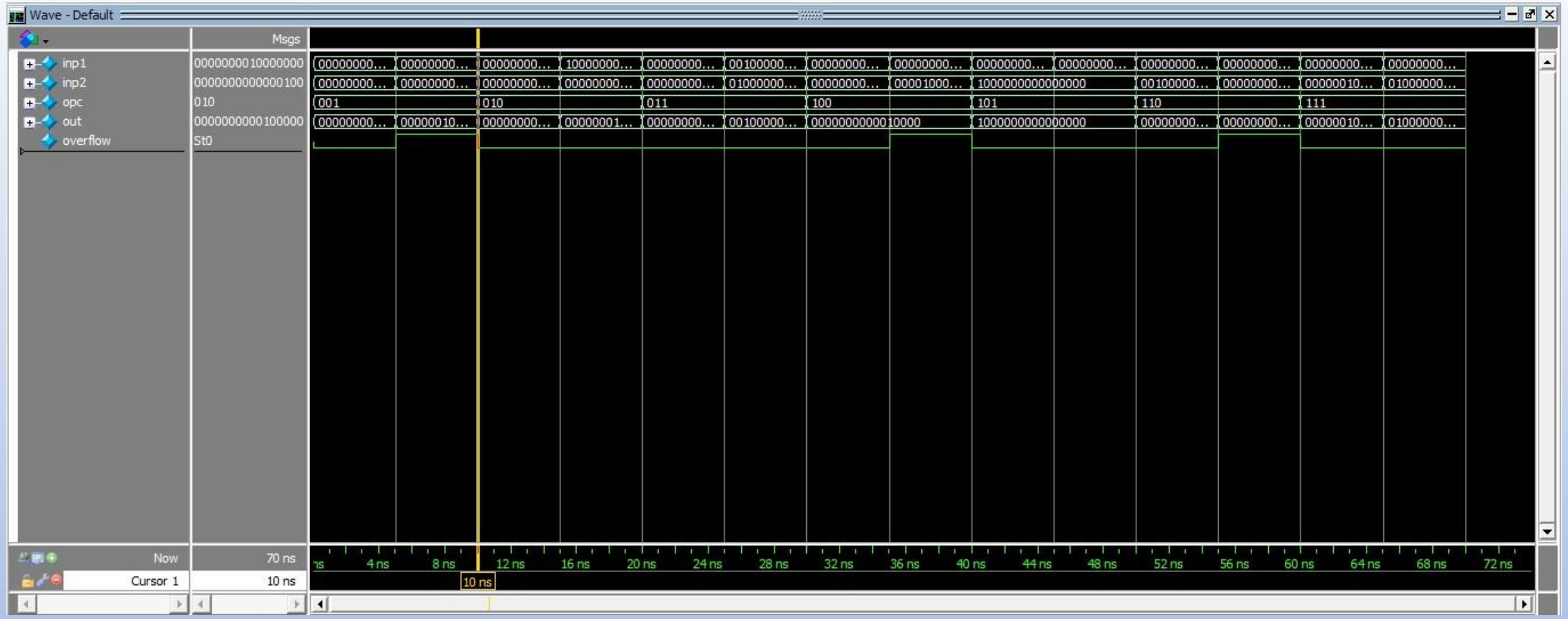
This is Top_Module component that takes the 16-bits inputs and the 3-bits opcode. It will takes the inputs to the core system and then will converts the 4-bits output of the core system to a 16-bits number using a decoder. Thus the output will be a 16-bits number and an overflow signal.



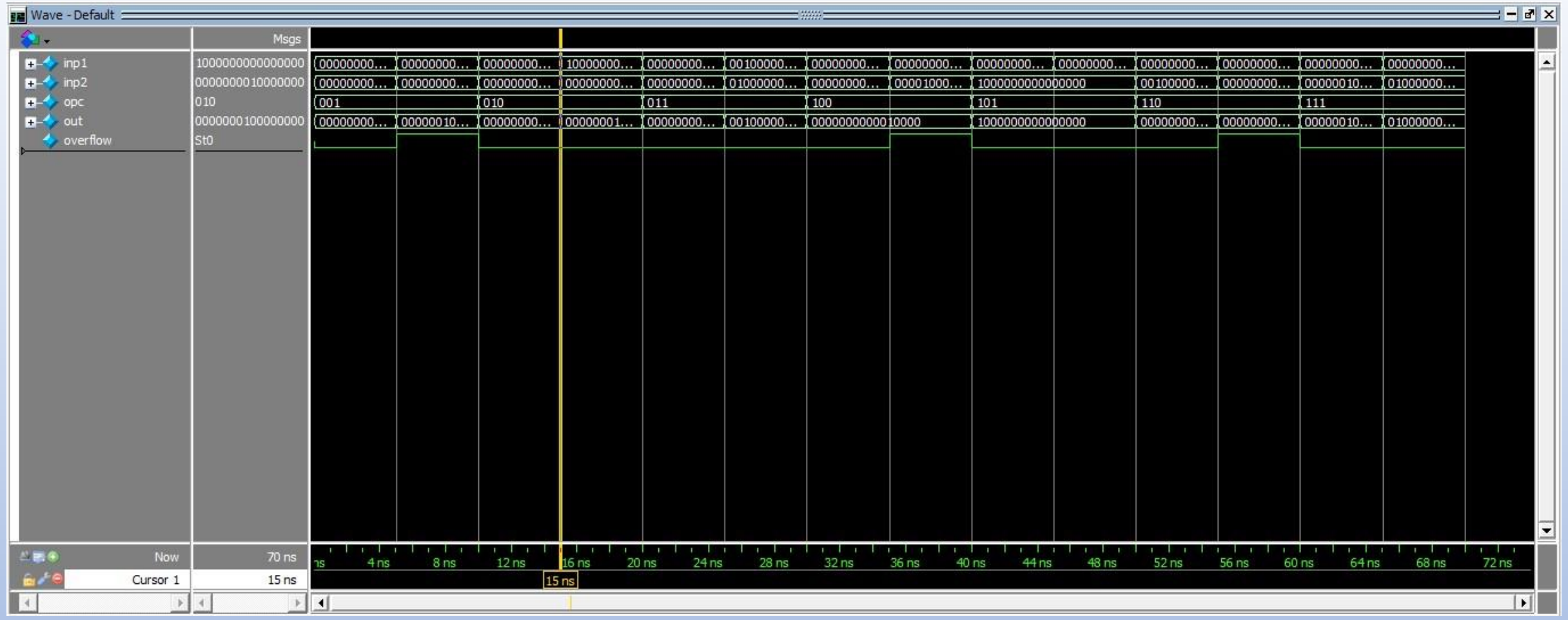
Test 1
Opcode 1 (ADD)
input 1: 2
input 2: 3
output: 5



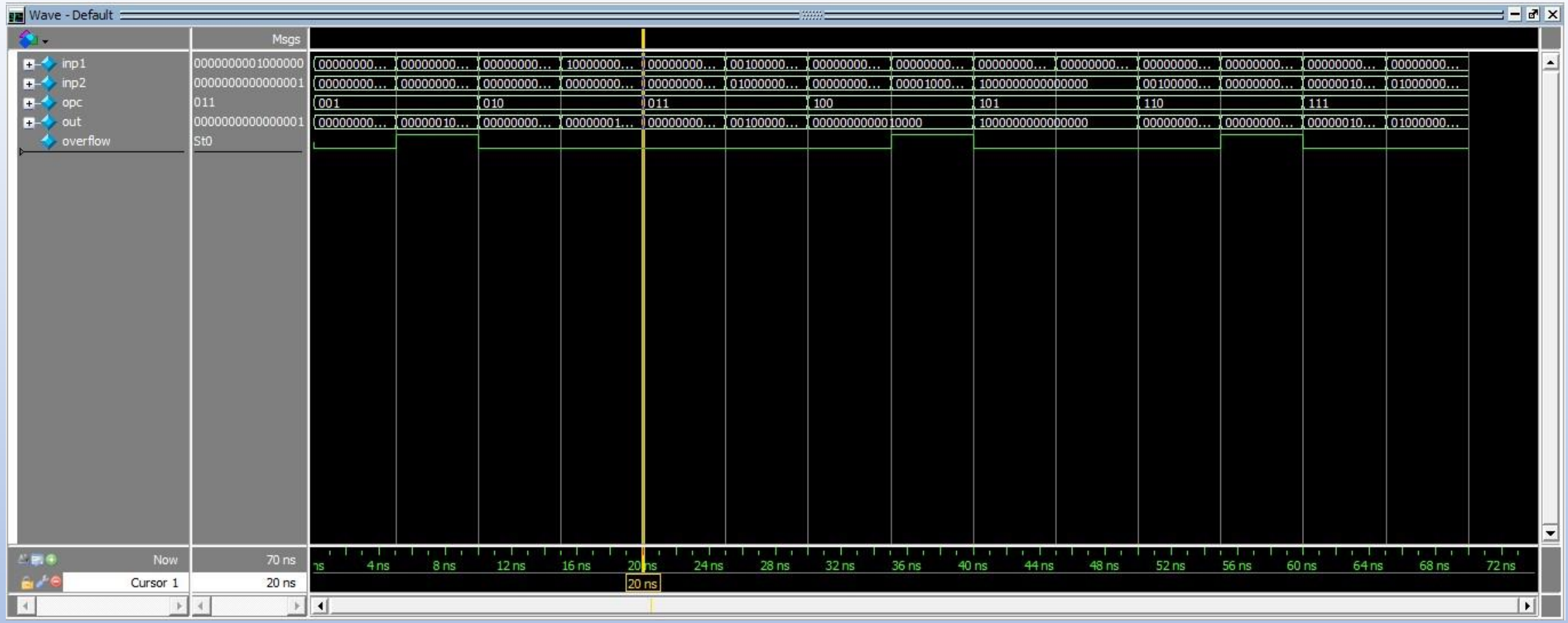
Test 2
Opcode 1 (ADD)
input 1: 5
input 2: 4
output: The output is not valid because the overflow signal is high.



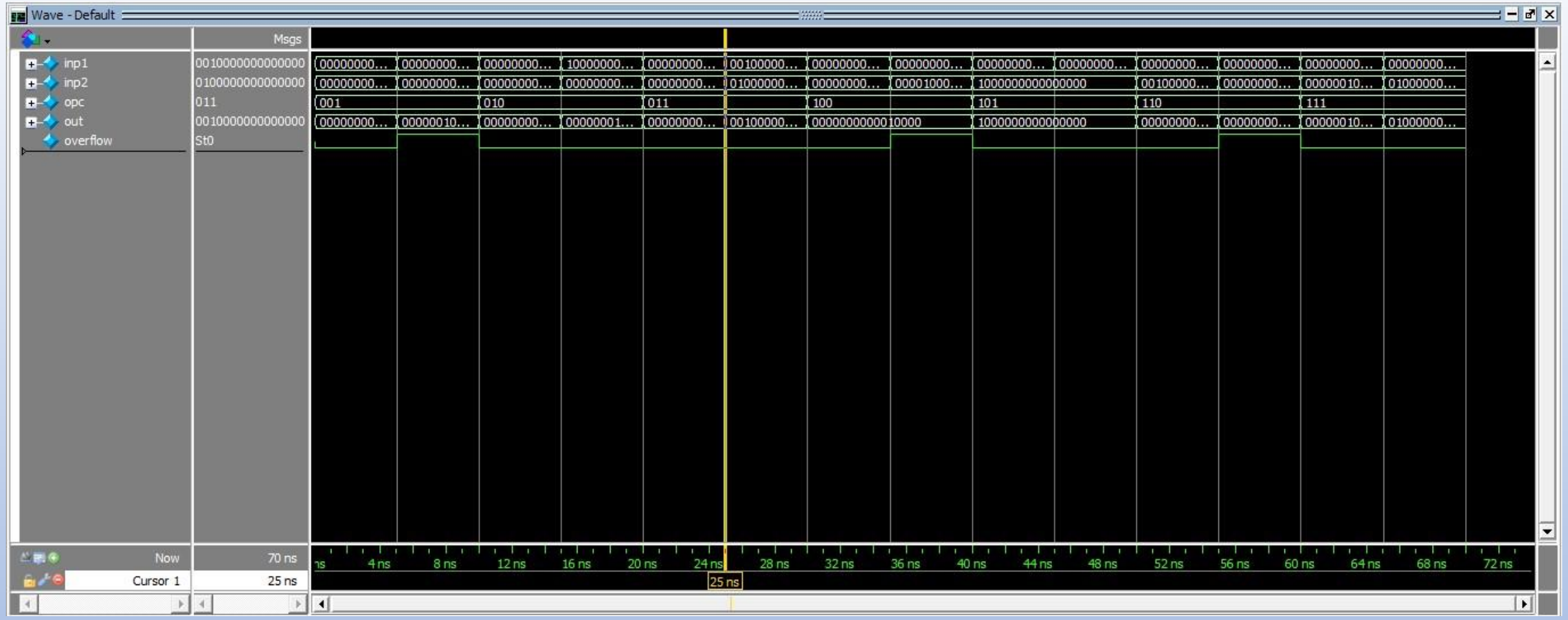
Test 3
Opcode 2 (SUB)
input 1: 7
input 2: 2
output: 5



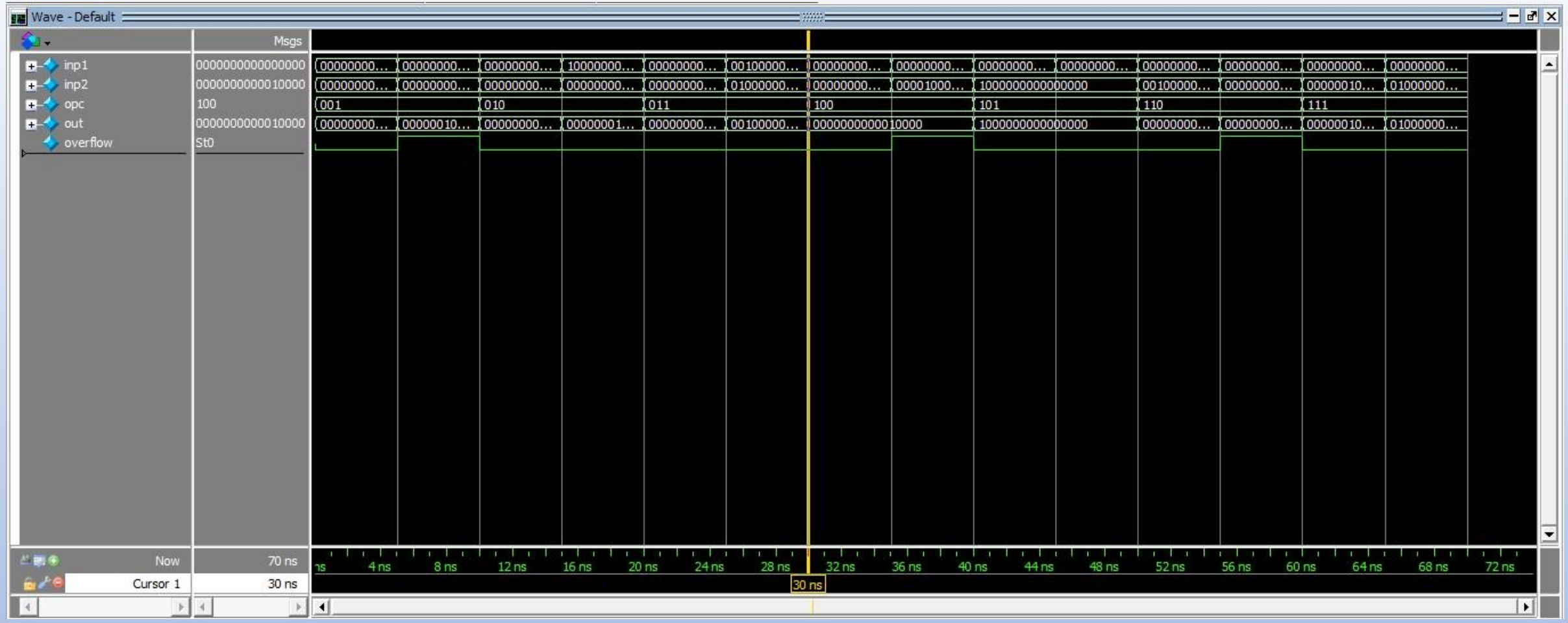
Test 4
Opcode 2 (SUB)
input 1: -1
input 2: 7
output: -8



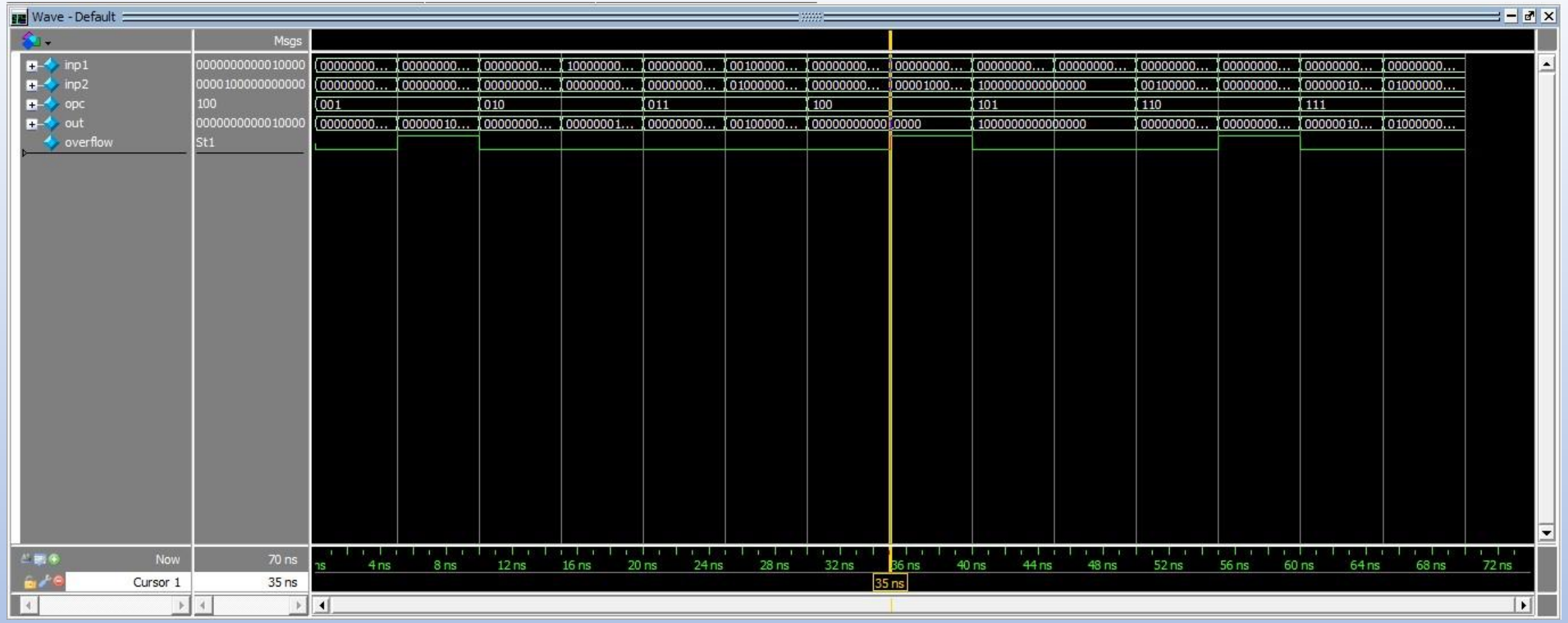
Test 5
Opcode 3 (Min (by adder))
input 1: 6
input 2: 1
output: 1



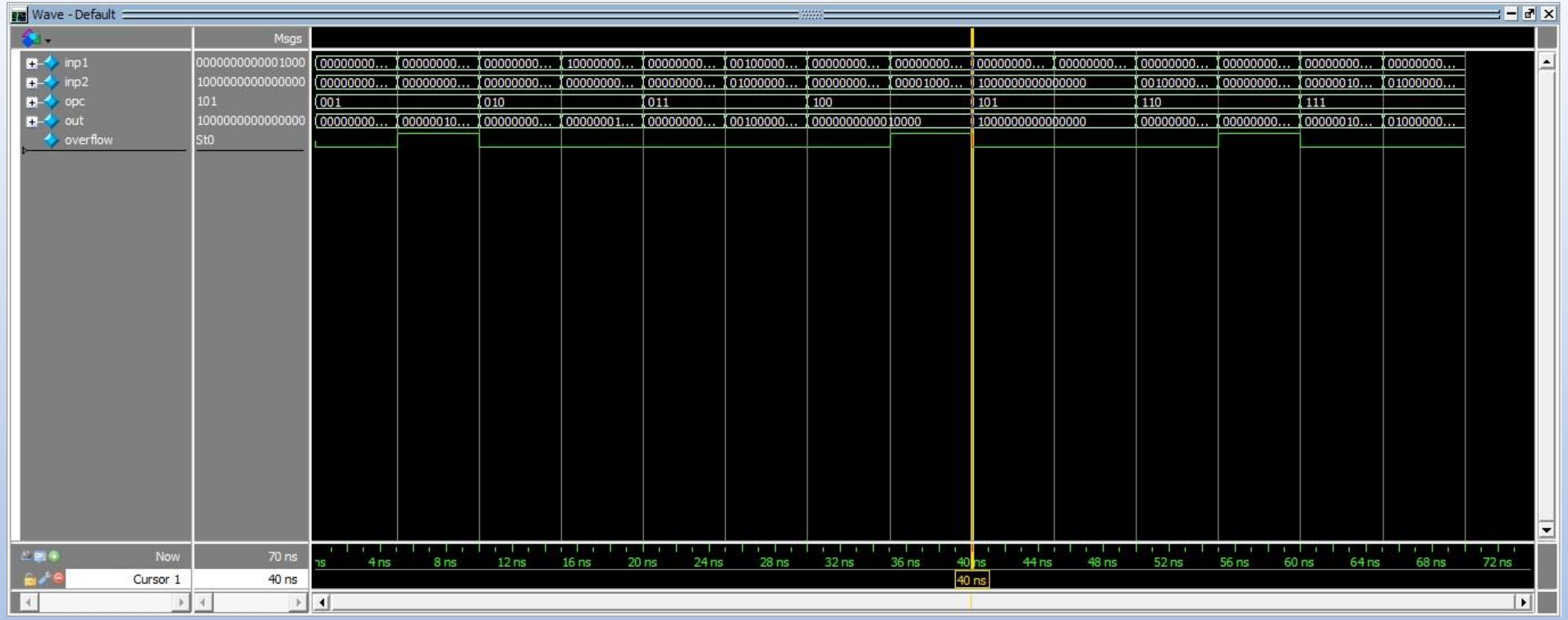
Test 6
Opcode 3 (Min (by adder))
input 1: -3
input 2: -2
output: -3



Test 7
Opcode 4 (Max (by adder))
input 1: 0
input 2: 4
output: 4

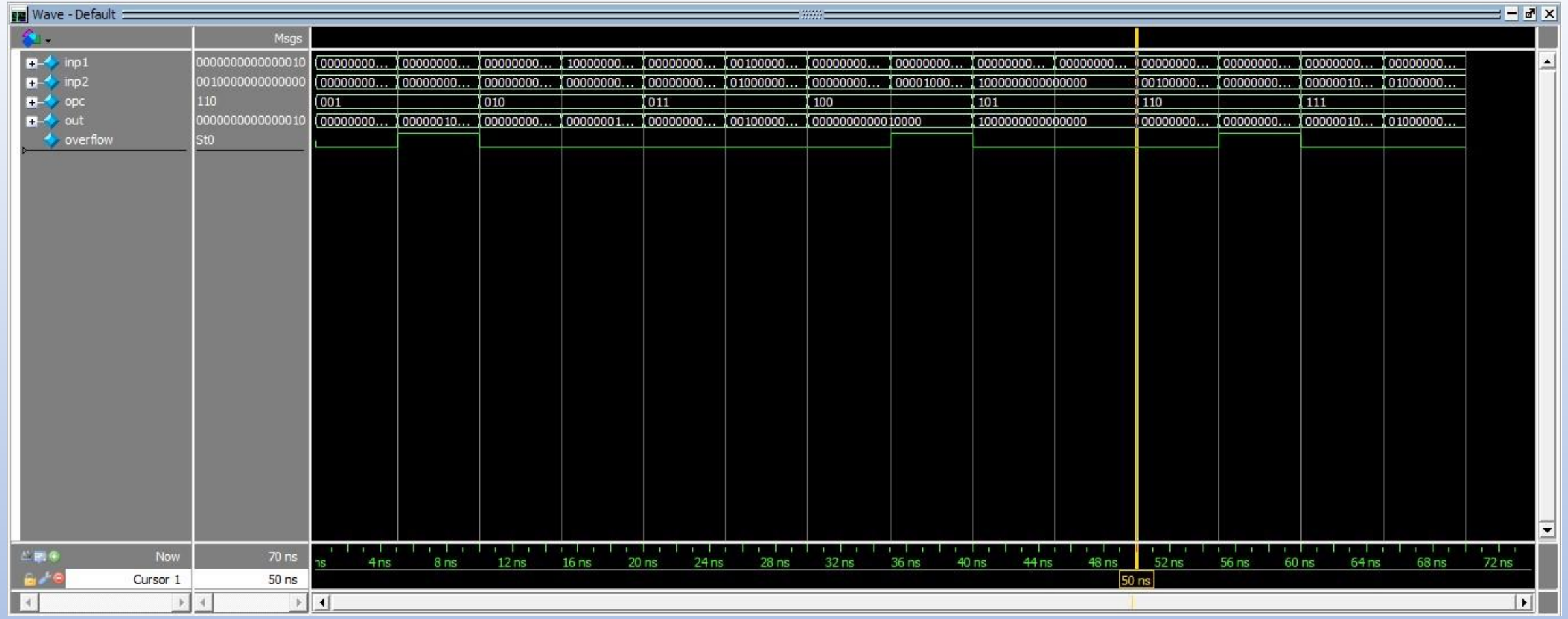


Test 8
Opcode 4 (Max (by adder))
input 1: 4
input 2: -5
output: 4

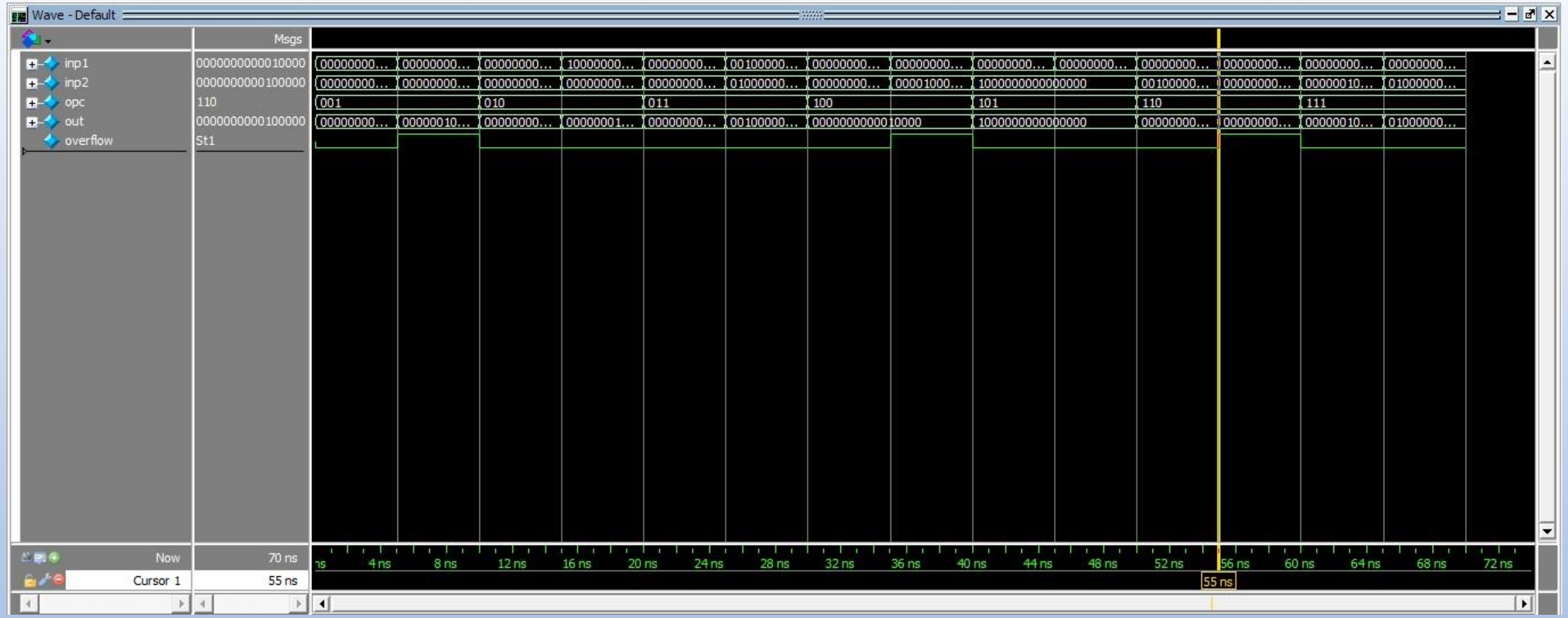


Test 9
Opcode 5 (Min (by comparator))
input 1: 3
input 2: -1
output: -1

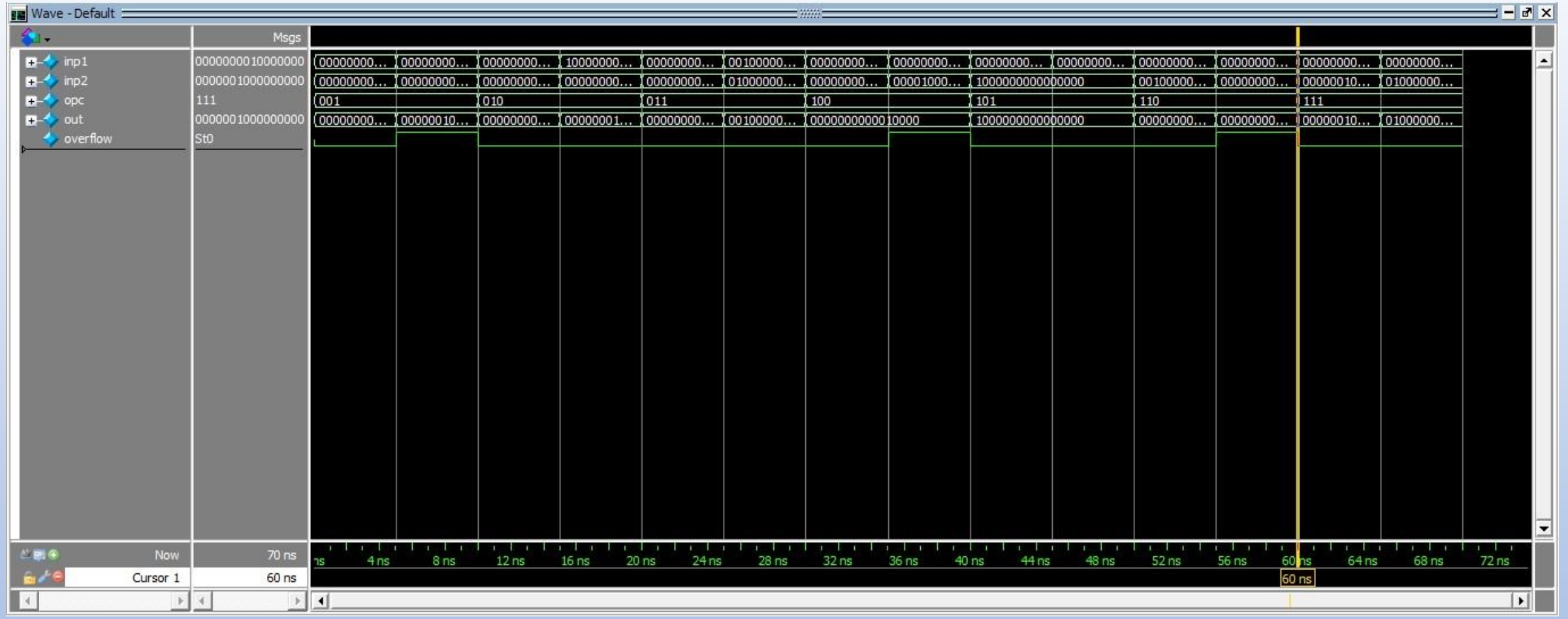
Test 10
Opcode 5 (Min (by comparator))
input 1: 6
input 2: -1
output: -1



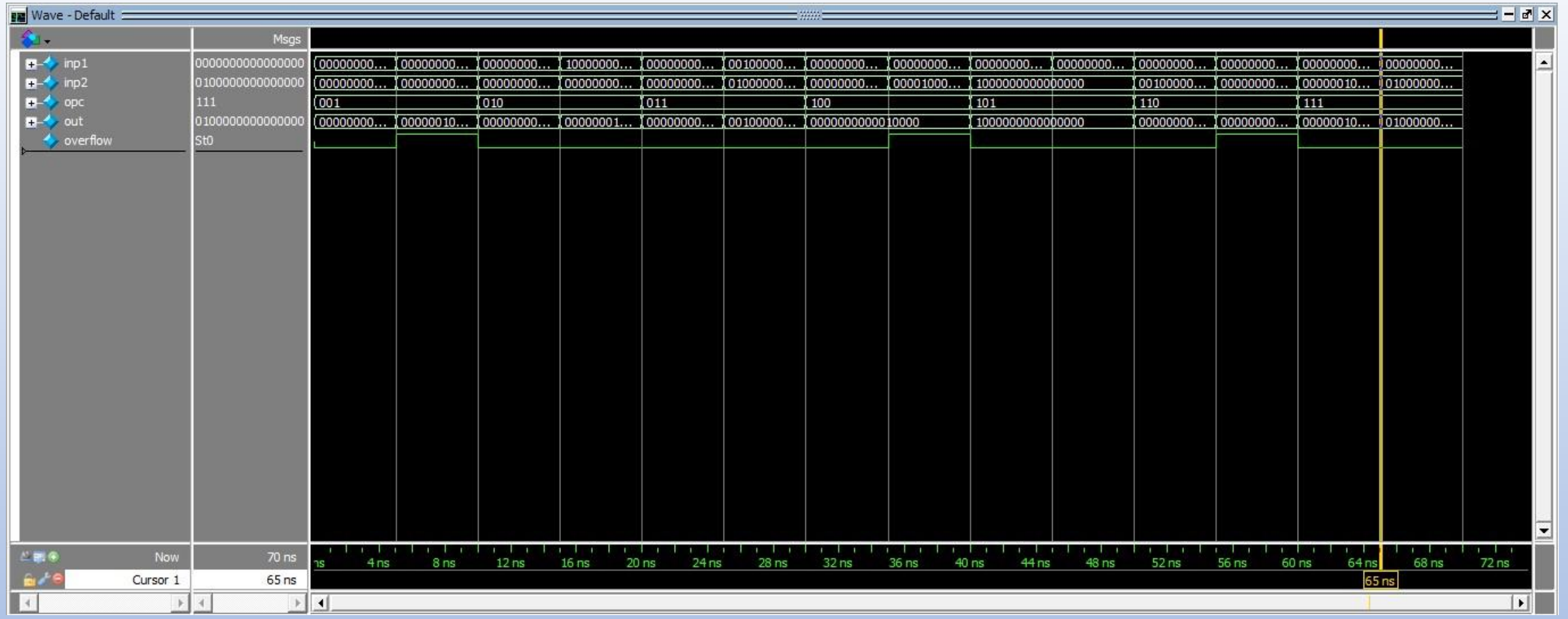
Test 11
Opcode 6 (Max (by comparator))
input 1: 1
input 2: -3
output: 1



Test 12
Opcode 6 (Max (by comparator))
input 1: 4
input 2: 5
output: 1



Test 13
Opcode 7 (Move)
input 1: 7
input 2: 9
output: 9



Test 14
Opcode 7 (Move)
input 1: 0
input 2: -2
output: -2