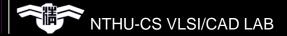
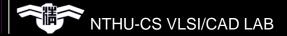
2016 Architecture

# Project 1 – Instruction simulator



# **Outline**

- Workstation setting : MobaXterm
- Project



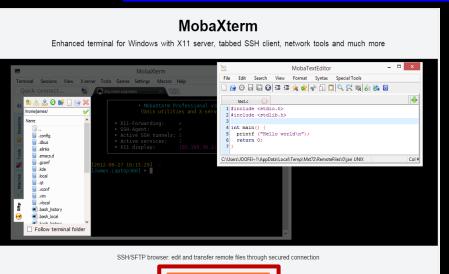
# **Outline**

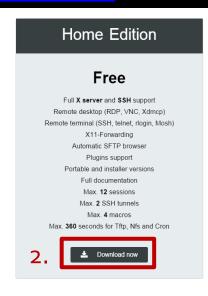
- Workstation setting : MobaXterm
- Project



### MobaXterm Download

- Download the free version of MobaXterm
  - http://mobaxterm.mobatek.net/









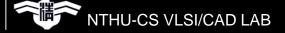
### MobaXterm Installation

- Installation
  - Next & Accept → Finish

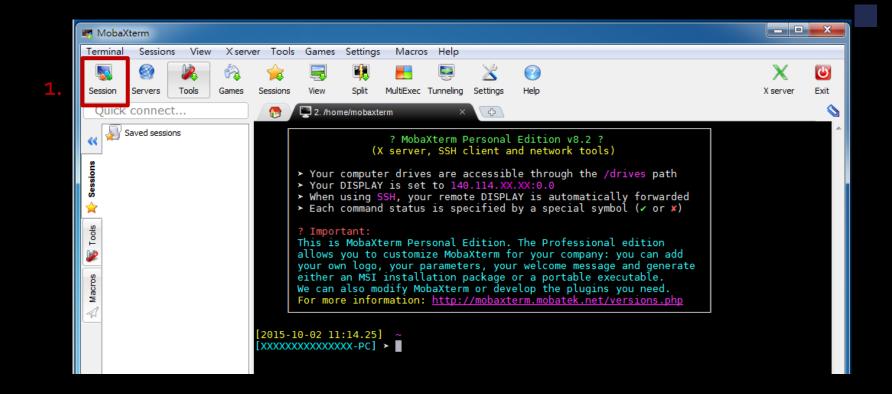


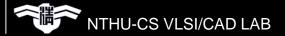
Click the icon on desktop





# **Workstation Setup**

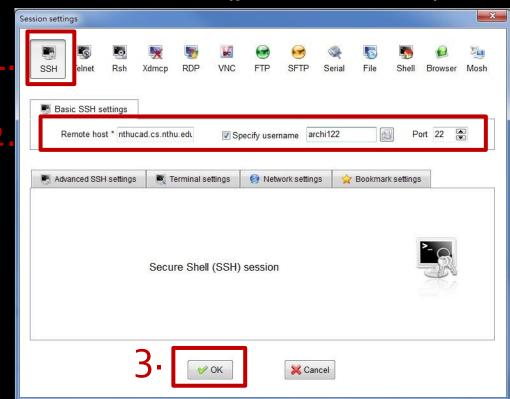




# Workstation Setup (Cont.)

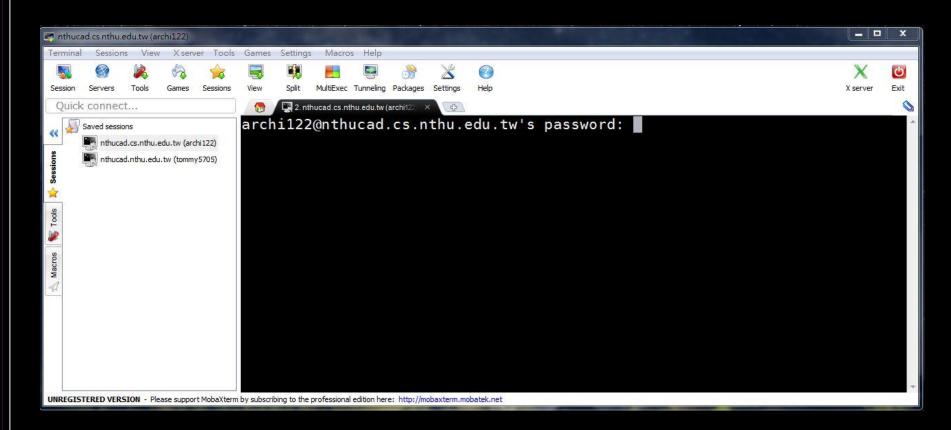
- Enter the following blank
  - Remote host: nthucad.cs.nthu.edu.tw
  - Specify username : archiXX (your account)
  - Port: 22

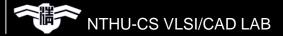
Click "OK"



# Login at the First Time

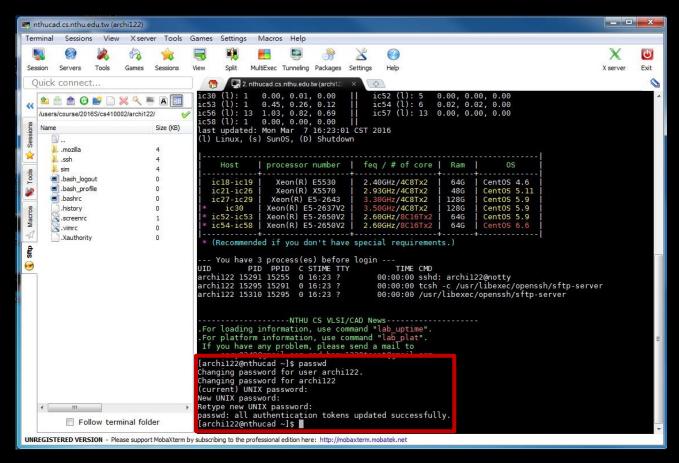
Key in your initial password from e-mail

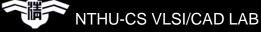




# Change Your Password

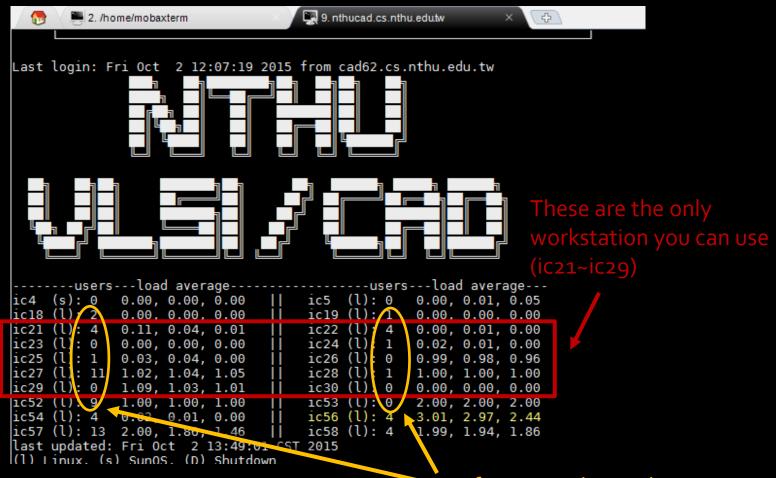
Type "passwd" to change your password





# **Connecting to Workstation**

- You can only choose on workstation from ic21 ~ ic29
- Find a workstation with less user



# Connecting to Workstation (Cont.)

- Connect to a workstation
  - ssh -X icXX

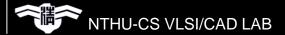
```
3. nthucad.cs.nthu.edu.tw (archi122 × \ \cdot)
        -----NTHU CS VLSI/CAD News-----
.For loading information, use command "lab uptime".
.For platform information, use command "lab plat".
 If you have any problem, please send a mail to
[archi122@nthucad ~]$ ssh -X ic21
The authenticity of host 'ic21 (192.168.75.51)' can't be established.
RSA key fingerprint is e0:06:4a:9a:6d:b2:a1:c7:c7:f6:49:b0:39:54:8c:7a.
Are you sure you want to continue connecting (yes/no)? yes
                                                                                      Type "yes"
Warning: Permanently added 'ic21,192.168.75.51' (RSA) to the list of known hosts.
archi122@ic21's password:
             0.00, 0.01, 0.05
                                                  0.00, 0.00, 0.00
             0.00, 0.00, 0.00
                                     ic21 (l): 3
                                                  0.02, 0.01, 0.00
             0.00, 0.00, 0.00
                                     ic23 (l): 17 2.03, 1.97, 1.57
             0.00. 0.00. 0.00
                                                  0.00. 0.00. 0.00
             0.00, 0.00, 0.00
                                                  0.08, 0.07, 0.02
             0.00, 0.00, 0.00
                                                  0.01, 0.02, 0.00
             0.00, 0.00, 0.00
                                                  0.00, 0.03, 0.05
             0.01, 0.09, 0.08
                                     ic54 (l): 6
                                                  0.63, 0.18, 0.05
ic56 (l): 13 1.02, 0.79, 0.74
                                     ic57 (l): 13 0.00, 0.00, 0.00
ic58 (l): 1 0.00, 0.00, 0.00
last updated: Mon Mar 7 16:07:01 CST 2016
(l) Linux, (s) SunOS, (D) Shutdown
       -----NTHU CS VLSI/CAD News-----
.For loading information, use command "lab uptime".
.For platform information, use command "lab plat".
 If you have any problem, please send a mail to
     cory8249@gmail.com and hsnu1220toast@gmail.com
Synopsys licenses have set!
                                2. Should be [XXX@icXX ~] s after connecting
[archi122@ic21 ~]$
```



NTHU-CS VLSI/CAD LAB

#### Run simulation

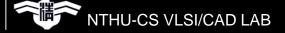
- Use "NC verilog" as standard simulation platform
  - Commercial software by Cadence
- You can use any IDE/Editor to program



### Run simulation

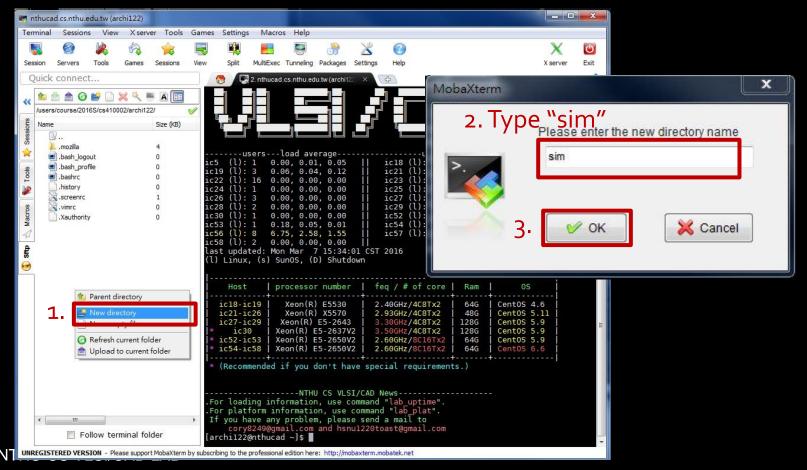
- \$ ncverilog all .v file you need
  - Ex: \$ncverilog Simulator.v Test\_Bench.v

```
🕞 🖳 2. nthucad.cs.nthu.edu.tv
                Initial blocks:
                Pseudo assignments:
                Simulation timescale: 1ps
        Writing initial simulation snapshot: worklib.Test Bench:v
Loading snapshot worklib.Test Bench:v ....................... Done
*Verdi3* Loading libsscore ius141.so
*Verdi3* : Enable Parallel Dumping.
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
$0: 0
$1: 0
$27: 0
Simulation complete via $finish(1) at time 2010 NS + 0
./Test Bench.v:45
                      #(`CYCLE_TIME*`END_CYCLE) $finish;
ncsim> exit
```



# **Create directory**

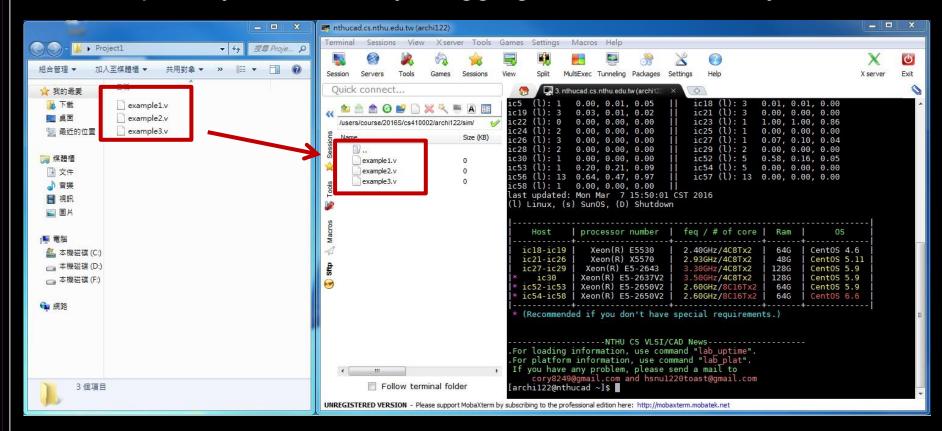
Right click to create new directory "sim" or by command line "mkdir sim"

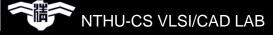




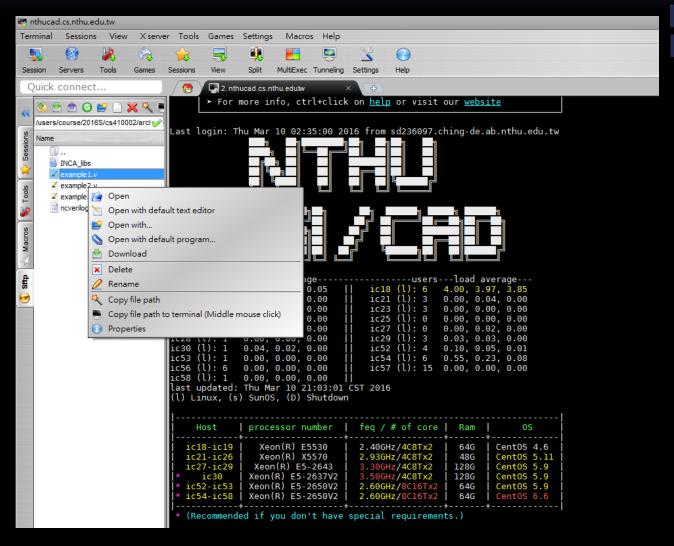
# Uploading .v Files

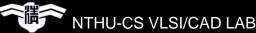
- Upload files
  - Upload your .v files by dragging them into directory





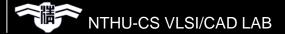
### **Edit with MobaXterm**





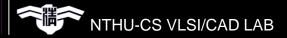
### Useful tool

- Makefile
  - No need to type "ncverilog ..." all the time
- Screen
  - Multiscreen in linux
- ■鳥哥的Linux 私房菜
  - Linux introduction and instruction



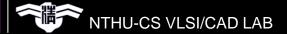
# **Outline**

- Workstation setting : MobaXterm
- Project



### Goal

- Implement chosen instructions
  - We've implemented ADD without error detection
    - Simulator.v
    - □ Test\_Bench.v



# R-type instruction

Instruction	Example	Meaning	Op field	Function field
ADD(Addition)	add r1, r2, r3	r1 = r2 + r3	0x00	32(0x20)
<b>SUB</b> (Subtraction)	sub r1, r2, r3	r1 = r2 - r3	0x00	34(0x22)
<b>AND</b> (Logic And)	and r1, r2, r3	r1 = r2 & r3	0x00	36(0x24)
<b>OR</b> (Logic Or)	or r1, r2, r3	r1 = r2   r3	0x00	37(0x25)
<b>SLT</b> (Set on Less Than) signed comparison	slt r1, r2, r3	if (r2 < r3) r1 = 1 else r1 = 0	0x00	42(0x2a)

# I-type instruction

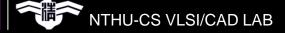
Instruction	Example	Meaning	Op field
ADDI(Add Immediate)	addi r1, r2, 100	r1 = r2 + 100	0x08
<b>LW</b> (Load word)	lw r1, o(s1)	R1 = 4 byte from Mem[s1+o]	0x23
<b>SW</b> (Store word)	sw r1, o(s1)	4 byte from Mem[s1+o] = r1	0x2B
<b>SLTI</b> (Set on Less Than Immediate)	slti r1, r2, 10	if( r2 < 10) r1 = 1 else r1 = 0	0x0A
<b>BEQ</b> (Branch On Equal)	beq r1, r2, 25	if (r1 == r2) go to PC+4+100	0x04

Immediate is signed for these instructions

#### Error instruction detection

- Write to register \$zero
- Access I/D memory out of address bound
  - I/D memory size: 1KB
- Data misaligned
  - Ex: LW \$5 2(\$0)

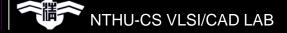
Instruction considered as No Operation if one of situations happen



#### **Initial status**

- Data memory and register should be set to 0 at the beginning
- PC start with 0

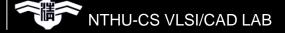
Be able to reset program by rst\_i



### **Notice**

- Please upload all your .v file without being compressed and without Test\_Bench.v to iLMS
  - No file I/O
  - No clk and rst setting
- There shouldn't be \$stop in your code

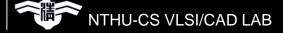
Violate: -40 points



### **Notice**

- Don't modify name, usage, size
  - Top module Simulator.v Name: Simulator
  - Register file: [32-1:0] Reg\_File [0:32-1]
    - Store value of register
    - □ Simulator.Reg\_File
  - Instruction memory: [32-1:0] Instr\_Mem [0:256-1]
    - Store value of instruction memory
    - Simulator.Instr\_Mem

Violate: -40 points



# Grade

- Three test case
  - Completely correct or wrong

Test case	Points	
ADD, SUB, AND, OR, SLT ADDI, SLTI	60%	
+BEQ	20%	
+LW,SW	20%	



# Test case example

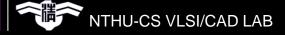
- Test case format
  - Each line occupied by one assembly code

#### 

#### testcase.txt

```
addi $1, $0, 10
addi $2, $0, 4
slt $3, $1, $2
add $4, $1, $2
sub $5, $1, $2
```

#### Result



# Test case example

#### testcase\_1.txt

addi \$1, \$0, 10 addi \$2, \$0, 4 slt \$3, \$1, \$2 beq \$3, \$0, 1 add \$4, \$1, \$2 sub \$5, \$1, \$2

#### Result

#### testcase\_2.txt

addi \$9, \$0, 10 addi \$10, \$0, 4 sw \$10,0(\$11) slt \$12, \$9, \$10 sub \$13, \$9, \$10 lw \$14, 0(\$11)

#### Result

\$9=10, \$10=4, \$12=0, \$13=6, \$14=4

### **Deadline**

- Deadline: 3/31, 23:59
- No late submission is allowed

