Lab 1: Modeling Styles for Full Adder

Due: March 5, 2013

Objective

- To be familiar with Verilog structural modeling, data flow modeling and behavioral modeling.

Action Items

1. Write a Verilog module that models a full adder using gate primitives and test your module using the testbench file Lab1_1_t.v.

   You have to use the following template for your design.

```
module Lab1_1(a , b , cin , sum , cout);
input a , b, cin ;
output sum , cout ;
   // add your design here
endmodule
```

2. Re-write the module using continuous assignments and re-test your module using the testbench file Lab1_2_t.v.

   You have to use the following template for your design.

```
module Lab1_2(a , b , cin , sum , cout);
input a , b, cin ;
output sum , cout ;
   // add your design here
endmodule
```

3. Re-write the module using behavioral modeling and re-test your module using the testbench file Lab1_3_t.v.

   You have to use the following template for your design.

```
module Lab1_3(a , b , cin , sum , cout);
input a , b, cin ;
output sum , cout ;
```

```
    // add your design here
endmodule
```