Lab 3: BCD Up/Down Counter

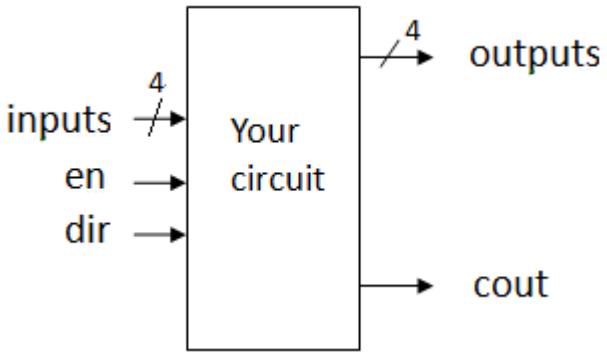
Due: March 19, 2015

Objective

- Be familiar with Verilog and BCD counter.

Action Items

1. Design a circuit that converts a 4-bit BCD number to its next or previous BCD number. The block diagram of the circuit is shown below.



- If en is 0, outputs = inputs and cout = 0.
- If en is 1 and dir is 1, the outputs and cout are as follows.

inputs[3]	inputs[2]	inputs[1]	inputs[0]	outputs[3]	outputs[2]	outputs[1]	outputs[0]	cout
0	0	0	0	0	0	0	1	0
0	0	0	1	0	0	1	0	0
0	0	1	0	0	0	1	1	0
0	0	1	1	0	1	0	0	0
0	1	0	0	0	1	0	1	0
0	1	0	1	0	1	1	0	0
0	1	1	0	0	1	1	1	0
0	1	1	1	1	0	0	0	0
1	0	0	0	1	0	0	1	0
1	0	0	1	0	0	0	0	1
1	0	1	0					
		⋮		0	0	0	0	0
1	1	1	1					

- If en is 1 and dir is 0, the outputs and cout are as follows.

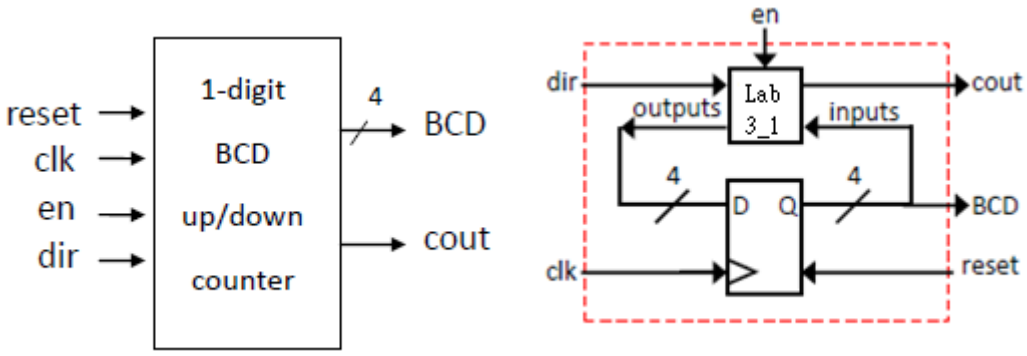
inputs[3]	inputs[2]	inputs[1]	inputs[0]	outputs[3]	outputs[2]	outputs[1]	outputs[0]	cout
0	0	0	0	1	0	0	1	1
0	0	0	1	0	0	0	0	0
0	0	1	0	0	0	0	1	0
0	0	1	1	0	0	1	0	0
0	1	0	0	0	0	1	1	0
0	1	0	1	0	1	0	0	0
0	1	1	0	0	1	0	1	0
0	1	1	1	0	1	1	0	0
1	0	0	0	0	1	1	1	0
1	0	0	1	1	0	0	0	0
1	0	1	0					
		⋮		0	0	0	0	0
1	1	1	1					

You have to use the following template for your design.

```
module Lab3_1(cout, outputs, inputs, en, dir );
input en;
input dir;
input [3:0] inputs;
output [3:0] outputs;
output cout;
   // add your design here
endmodule
```

You should use the given testbench (Lab3_1_t.v) to verify your design.

2. Design a positive-edge triggered 1-digit BCD up/down counter whose block diagrams are shown below.



The clk is the clock signal. The reset is an asynchronous control signal and when it is 0, the counter is reset to 0 (i.e., BCD=0000). If en is 0, the counter remains unchanged; otherwise (i.e., en=1), the counter is incremented or decremented by 1 according to the value of dir. If dir is 1, the counter is incremented; otherwise (i.e., dir=0), the counter is decremented. You must reuse your design of Lab3_1 to create the 1-digit BCD counter.

You have to use the following template for your design.

```
module Lab3_2(cout, BCD, dir, en, reset, clk );
input en, dir, reset, clk;
output [3:0] BCD;
output cout;
   // add your design here
endmodule
```

You should use the given testbench (Lab3_2_t.v) to verify your design.