Lab 8: LCD Controller

Due: April 23, 2015

Objective

- To be familiar with how to control the LCD.

Action Item

1. Modify the Verilog code introduced in today's class to design a LCD controller. The controller has the following input ports:

```
input   CLK;

input   RESET;
```

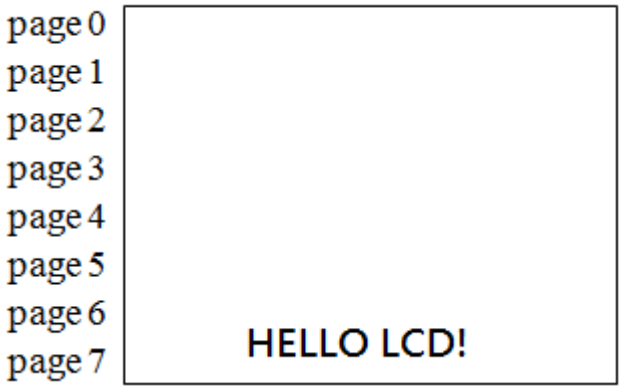
and the following output ports:

```
output LCD_ENABLE;
output LCD_RW;
output LCD_DI;
output LCD_CS1;
output LCD_CS2;
output LCD_RST;
output [7:0] LCD_DATA;
```

The behavior of the controller is explained below.

- After pressing the RESET button, the LCD will first show the string "HELLO LCD!" (which is stored in pages 6 and 7 of the display data RAM) at the bottom of the screen, and then start to repeatedly scroll up the string page by page under the frequency of CLK divided by 2^8 (i.e., CLK/2^8).

Here are some example operations of the controller:



press RESET

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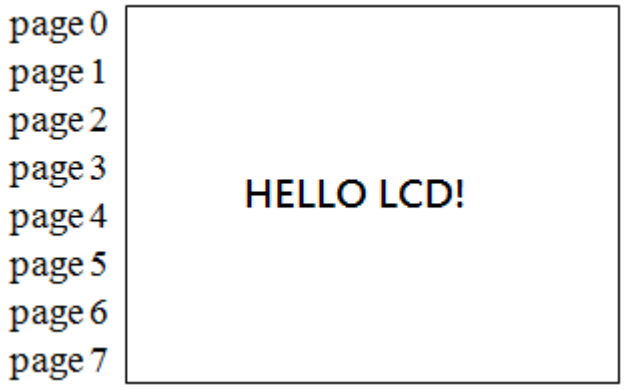

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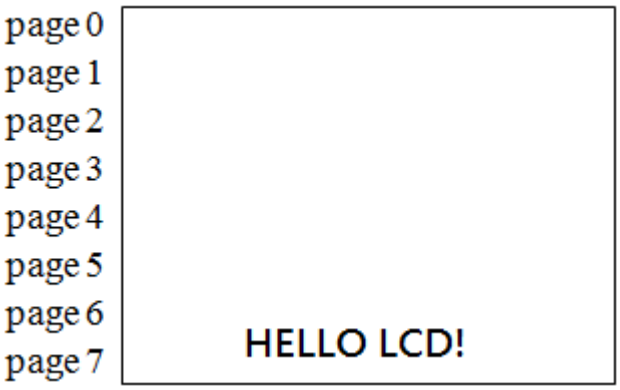

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More details about the I/O signals of the controller are given below.

- **CLK:** Clock signal which is connected to the FPGA pin **R10**.
- **RESET:** Asynchronous negative trigger reset which is connected to the pushbutton **S1** (i.e., the FPGA pin **N3**).
- **LCD_ENABLE:** signal to enable the LCD, which is connected to the E signal of the LCD (i.e., the FPGA pin **F5**).
- **LCD_RW:** signal to control read or write of the LCD, which is connected to the R/$\overline{W}$ signal of the LCD (i.e., the FPGA pin **C2**).
- **LCD_DI:** signal to indicate data or instruction for the LCD, which is connected to the D/$\overline{I}$ signal of the LCD (i.e., the FPGA pin **C1**).
- **LCD_CS1:** signal to select column 1 ~ 64 of the LCD, which is connected to the CS1 signal of the LCD (i.e., the FPGA pin **F4**).
- **LCD_CS2:** signal to select column 65 ~ 128 of the LCD, which is connected to the CS2 signal of the LCD (i.e., the FPGA pin **E1**).
- **LCD_RST:** signal to reset the LCD, which is connected to the $\overline{RST}$ signal of the LCD (i.e., the FPGA pin **E3**).
- **LCD_DATA:** data bits for the LCD, which are connected to the DB7~DB0 signals of the LCD (i.e., the FPGA pins **F3, D2, D1, H7, G6, E4, D3, F6**).