Lab 5: Pingpong Counter

Due: April 2, 2015

Objective

- To be familiar with the FPGA design flow and the demo board.

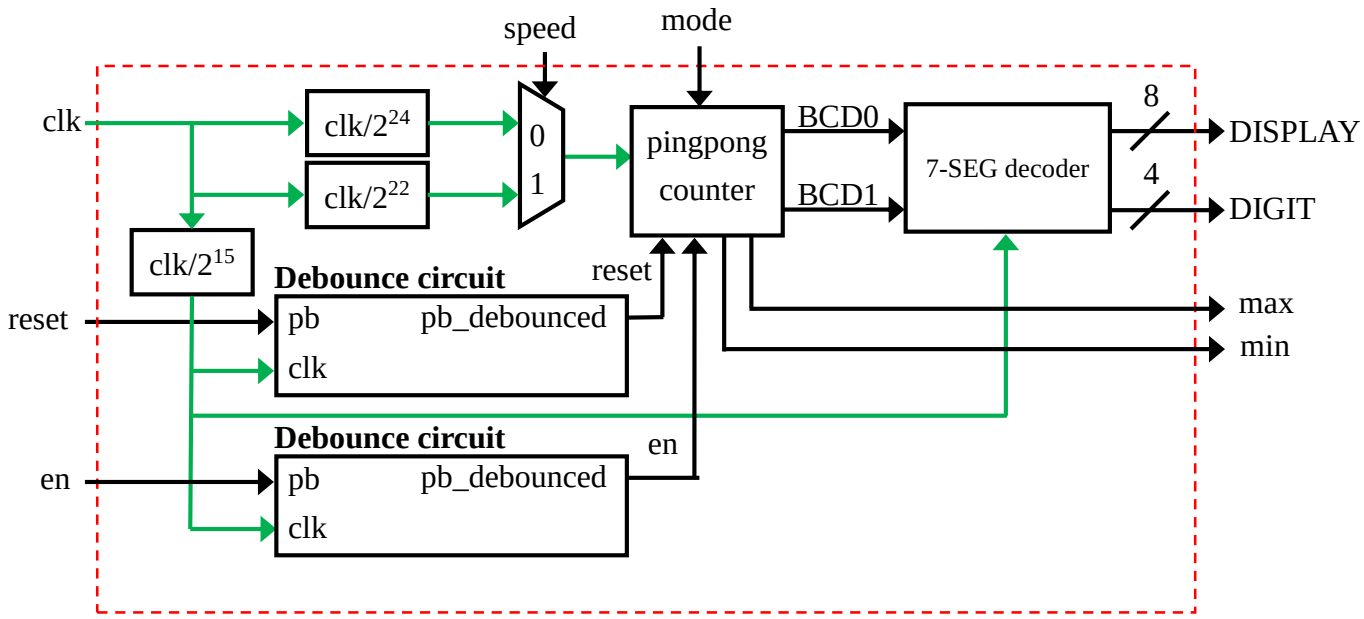
Action Items

1. Write and test your Verilog code that models a two-digit pingpong counter. The counter has two counting modes. One mode is to first count down from 99 to 00 and then count up from 00 to 99. The other mode is to first count down from 60 to 00 and then count up from 00 to 60. The counter will repeatedly count down and up in either mode until it is disabled. You need to design the counter such that it can run at two different speeds. The I/O signals and the block diagram of the counter are shown below.

   Signal specification：

   clk: clock signal (connected to FPGA pin **R10**)
   reset: asynchronous active-low reset (connected to FPGA pin **N3**)
   en: pushing the button even times to start counting, and odd times to stop counting (connected to FPGA pin **P4**)
   speed: 1 to perform the counting at a higher speed, clk/2^{22}, and 0 to perform the counting at a lower speed, clk/2^{24} (connected to FPGA pin **T1**)
   mode: 1 to perform the counting between 99 and 00, and 0 to perform the counting between 60 and 00 (connected to FPGA pin **L2**)
   DISPLAY: signal to show the two BCD digits of the counter on the two rightmost 7-segment displays
   DIGIT: signal to enable one 7-segment display
   max: 1 if the counter reaches the largest number 99 or 60, depending on the mode (connected to FPGA pin **K4** which triggers the associated LED to light up when max is set to 1)
   min: 1 if the counter reaches the smallest number 00 (connected to FPGA pin **K3** which triggers the associated LED to light up when

min is set to 1)



You have to use the following template for your design.

```
module Lab5(DIGIT, DISPLAY, max, min, clk, reset, en, speed, mode);
input clk;
input reset;
input en;
input speed;
input mode;
output [3:0] DIGIT;
output [7:0] DISPLAY;
output max;
output min;
    // add your design here
endmodule
```