Lab 4: FPGA and Demo Board

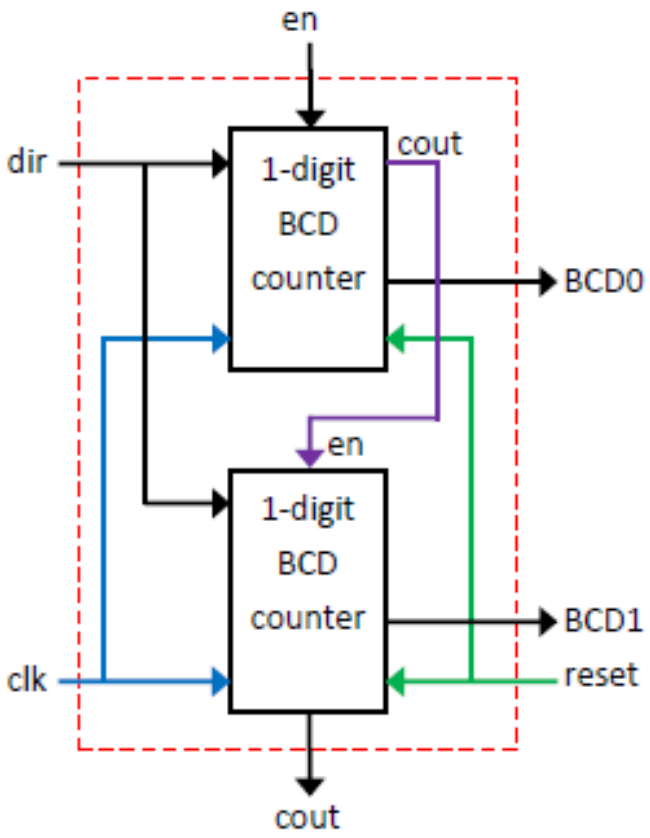
Due: March 26, 2015

Objective

- To be familiar with the FPGA design flow and the demo board.

Action Items

1. Write Verilog code to model a positive-edge triggered 2-digit BCD up/down counter. Its I/O signals are the same as the 1-digit BCD counter of Lab 3, except that the 1-digit BCD output is now changed to the 2-digit BCD output. You must implement the 2-digit BCD up/down counter based on the following block diagram which comprises two 1-digit BCD up/down counters. You may reuse the 1-digit BCD counter that you completed in Lab 3, and instantiate two instances in your 2-digit counter.



You have to use the following template for your design, and use the

given testbench (Lab4_1_t.v) to verify your design.

```
module lab4_1(BCD0, BCD1, cout, dir, en, reset, clk);
input clk;
input reset;
input en;
input dir;
output cout;
output [3:0] BCD0;
output [3:0] BCD1;
   // add your design here
endmodule
```

2. Program your 2-digit BCD up/down counter to the FPGA on the demo board. Before doing it, you must follow the block diagram shown below to write your Verilog code. The block diagram indicates that in addition to your 2-digit BCD counter, two clock generators with different frequencies and a 7-segment decoder are also required. The I/O signals are explained below:

   clk: clock signal (connected to FPGA pin **R10**)
   reset: asynchronous active-low reset (connected to FPGA pin **P1**)
   en: 1 to start counting, and 0 to stop counting (connected to FPGA pin **T1**)
   dir: 1 to count up, and 0 to count down (connected to FPGA pin **P2**)
   DISPLAY: signal to show the two BCD digits of the counter on the two rightmost 7-segment displays
   DIGIT: signal to enable one 7-segment display