Lab 6: Keyboard Controller

Due: April 9, 2015

Objective

- To be familiar with how to control the keyboard and 7-segment displays.

Action Items

1. Modify the Verilog code introduced in today's class to design a keyboard controller. The controller has the following input ports:

```
input    CLK;
input    RESET;
input    [3:0]    COLUMN;
```

and the following output ports:

```
output [3:0]    ROW;
output [3:0]    ENABLE;
output [7:0]    SEGMENT;
```

The behavior of the controller is explained below.

- When pressing the RESET button, the 7-segment displays will show " 0000 ".
- Whenever a key is pressed, it is shown on the rightmost 7-segment display, and meanwhile the previous letters/digits on the 7-segment diplays are left shiftted by one position (which means the letter or digit on the leftmost 7-segment display is shifted out and is not shown any more).

Here are some example operations of the controller:

0000	Press reset
0001	Press 1
0012	Press 2
0123	Press 3
123A	Press A
23Ab	Press B

More details about the I/O signals of the design are given below.

- **CLK:** Clock signal which is connected to the FPGA pin **R10**.
- **RESET:** Asynchronous negative trigger reset which is connected to the pushbutton **S1** (i.e., the FPGA pin **N3**).
- **COLUMN:** column signals which are connected to the FPGA pins **J3, J1, H2,H1**.
- **ROW:** row signals which are connected to the FPGA pins **K2, K1, L4,L3,**.
- **SEGMENT:** signals to show a pressed key.
- **ENABLE:** signals to enable one 7-segment display.