2017 Digital IC Design
Homework 5: Color Transform Engine

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Simulation Result

Testfixture 1 (YUV -> RGB)

Functional simulation	Pass	Gate-level simulation	Pass

Testfixture 2 (RGB -> YUV)

Pattern 1	Functional simulation	A	Gate-level simulation	A	Gate-level simulation time	23447.900 ns
Pattern 2	Functional simulation	A	Gate-level simulation	A	Gate-level simulation time	23447.900 ns
Pattern 3	Functional simulation	A	Gate-level simulation	A	Gate-level simulation time	23447.900 ns

Minimum CYCLE in Gate-level simulation	15.57 ns

your pre-sim result of Testfixture 1

```
# ---------------------------------------------------
#
# Congratulations! All data have been generated successfully!
#
# -------------Function 1 (YUV->RGB) PASS--------------------
#
# ** Note: $finish    : /home/yutongshen/HW5/testfixture1.v(126)
#    Time: 150301 ns  Iteration: 0  Instance: /test
# 1
# Break in Module test at /home/yutongshen/HW5/testfixture1.v line 126
```

your post-sim result of Testfixture 1

```
# ---------------------------------------------------
#
# Congratulations! All data have been generated successfully!
#
# -------------Function 1 (YUV->RGB) PASS--------------------
#
# ** Note: $finish    : /home/yutongshen/HW5/testfixture1.v(126)
#    Time: 150301 ns  Iteration: 0  Instance: /test
# 1
# Break in Module test at /home/yutongshen/HW5/testfixture1.v line 126
```

your pre-sim result of Testfixture 2, pattern 1

```
# ---------------------------------------------------
#
# Square Distance of All YUV = 419.000000
#
# Square of All YUV Signal   = 23195754.000000
#
# ---------------------------------------------------
#
# So Your Error Ratio:
#
# (Square Distance of YUV)/(Square of All YUV Signal) = 0.000018
#
# ---------------------------------------------------
#
# Your Score Level: A
#
# Congratulations! CTE's Function2 Successfully!
#
# -------------------------PASS-------------------------
#
# ** Note: $finish    : /home/yutongshen/HW5/testfixture2.v(208)
#    Time: 23447900 ps  Iteration: 0  Instance: /test
# 1
# Break in Module test at /home/yutongshen/HW5/testfixture2.v line 208
```

your post-sim result of Testfixture 2, pattern 1

```
# ---------------------------------------------------
#
# Square Distance of All YUV = 419.000000
#
# Square of All YUV Signal   = 23195754.000000
#
# ---------------------------------------------------
#
# So Your Error Ratio:
#
# (Square Distance of YUV)/(Square of All YUV Signal) = 0.000018
#
# ---------------------------------------------------
#
# Your Score Level: A
#
# Congratulations! CTE's Function2 Successfully!
#
# -------------------------PASS-------------------------
#
# ** Note: $finish    : /home/yutongshen/HW5/testfixture2.v(208)
#    Time: 23447900 ps  Iteration: 0  Instance: /test
# 1
# Break in Module test at /home/yutongshen/HW5/testfixture2.v line 208
```

your pre-sim result of Testfixture 2, pattern 2	your post-sim result of Testfixture 2, pattern 2
# ---------- # # Square Distance of All YUV = 410.000000 # # Square of All YUV Signal = 22233632.000000 # # ---------- # # So Your Error Ratio: # # (Square Distance of YUV)/(Square of All YUV Signal) = 0.000018 # # ---------- # # Your Score Level: A # # Congratulations! CTE's Function2 Successfully! # # ----------PASS---------- # # ** Note: $finish : /home/yutongshen/HW5/testfixture2.v(208) # Time: 23447900 ps Iteration: 0 Instance: /test # 1 # Break in Module test at /home/yutongshen/HW5/testfixture2.v line 208	# ---------- # # Square Distance of All YUV = 410.000000 # # Square of All YUV Signal = 22233632.000000 # # ---------- # # So Your Error Ratio: # # (Square Distance of YUV)/(Square of All YUV Signal) = 0.000018 # # ---------- # # Your Score Level: A # # Congratulations! CTE's Function2 Successfully! # # ----------PASS---------- # # ** Note: $finish : /home/yutongshen/HW5/testfixture2.v(208) # Time: 23447900 ps Iteration: 0 Instance: /test # 1 # Break in Module test at /home/yutongshen/HW5/testfixture2.v line 208
your pre-sim result of Testfixture 2, pattern 3	your post-sim result of Testfixture 2, pattern 3
# ---------- # # Square Distance of All YUV = 381.000000 # # Square of All YUV Signal = 21561234.000000 # # ---------- # # So Your Error Ratio: # # (Square Distance of YUV)/(Square of All YUV Signal) = 0.000018 # # ---------- # # Your Score Level: A # # Congratulations! CTE's Function2 Successfully! # # ----------PASS---------- # # ** Note: $finish : /home/yutongshen/HW5/testfixture2.v(208) # Time: 23447900 ps Iteration: 0 Instance: /test # 1 # Break in Module test at /home/yutongshen/HW5/testfixture2.v line 208	# ---------- # # Square Distance of All YUV = 381.000000 # # Square of All YUV Signal = 21561234.000000 # # ---------- # # So Your Error Ratio: # # (Square Distance of YUV)/(Square of All YUV Signal) = 0.000018 # # ---------- # # Your Score Level: A # # Congratulations! CTE's Function2 Successfully! # # ----------PASS---------- # # ** Note: $finish : /home/yutongshen/HW5/testfixture2.v(208) # Time: 23447900 ps Iteration: 0 Instance: /test # 1 # Break in Module test at /home/yutongshen/HW5/testfixture2.v line 208

Synthesis Result	
Total logic elements	286
Total memory bit	0
Embedded multiplier 9-bit element	0

(your flow summary)

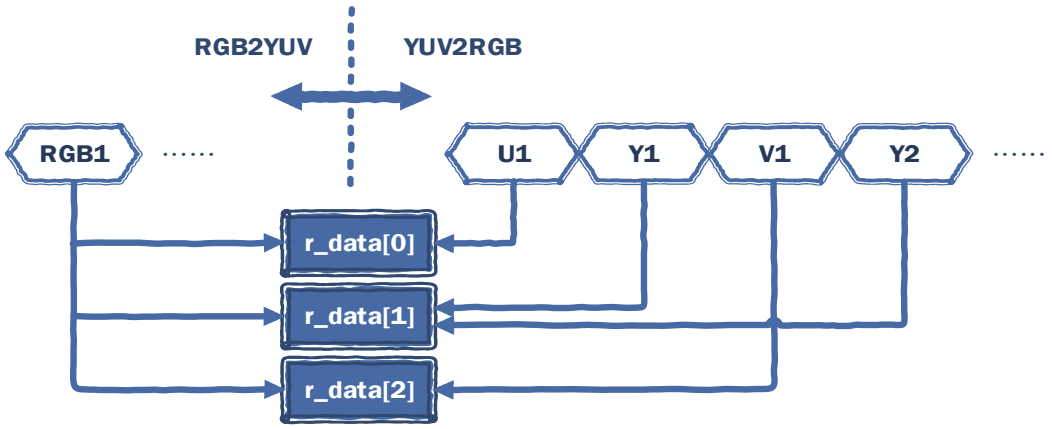
Flow Summary

Flow Status	Successful - Fri Dec 22 20:26:18 2017
Quartus II Version	10.0 Build 262 08/18/2010 SP 1 SJ Full Version
Revision Name	CTE
Top-level Entity Name	CTE
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Met timing requirements	Yes
Total logic elements	286 / 68,416 (< 1 %)
Total combinational functions	286 / 68,416 (< 1 %)
Dedicated logic registers	74 / 68,416 (< 1 %)
Total registers	74
Total pins	70 / 622 (11 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

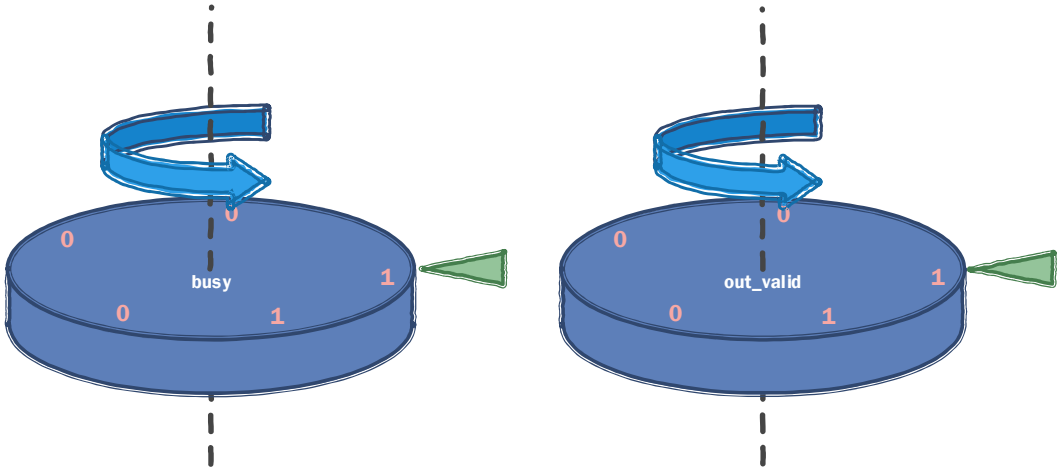
Description of your design

(1) Register file：

分別為 r_data[0]、r_data[1]、r_data[2]，在 op_mode = 0 時會依序存取 YUV；op_mode = 1 時會存取 RGB，如圖所示。



(2) Busy、Valid 及其他控制訊號之處理：



本電路採用類似轉盤的模型，經過設計，每完成一組計算（含 YUV2RGB 及 RGB2YUV）需要 6 個 cycle，故列舉 Busy、Valid 及其他控制訊號在這 6 個 cycle 所使用的訊號組成的 Array，而每組 Array 可以想像為每個不同的轉盤，上面刻有 6 個刻度（如上圖），被綠色指針指到的刻度即為本周期輸出的訊號，然而每經過 1 個 cycle 後轉盤轉向下一個刻度，如此一來即能完成所有的 Busy、Valid 及其他控制訊號。經過比較，使用 Counter 或狀態機來決定 Busy、Valid 及其他控制訊號的方法所需的 Delay 時間較長，而轉盤方式能達到直接讀出訊號（僅有 Register 的 Delay）是壓縮本電路計算時間的一大主因。

(3) YUV2RGB：

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1.625 \\ 1 & -0.25 & -0.75 \\ 1 & 2 & 0 \end{bmatrix} \begin{bmatrix} Y \\ U \\ V \end{bmatrix}$$

先將 YUV2RGB 矩陣轉換為 2 進制，得到 R 計算方式為 $Y + 1.101_2 * V$，G 計算方式為 $Y - 0.01_2 * U - 0.11_2 * V$，B 計算方式為 $Y + 10_2 * U$，再用位移加法來完成。

(4) RGB2YUV：

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = \begin{bmatrix} 0.29\overline{09} & 0.63\overline{03} & 0.0\overline{78} \\ -0.1\overline{45} & -0.31\overline{51} & 0.46\overline{06} \\ 0.4\overline{36} & -0.3\overline{87} & -0.0\overline{48} \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

由於如果想要使用暴力解此矩陣需要花費大量的加法器（乘法器皆由加法器取代），故在此改變策略，先將原矩陣進行高斯消去法：

$$\begin{bmatrix} Y \\ U + 0.5Y \\ V + \frac{8}{13}Y \end{bmatrix} = \begin{bmatrix} 0.29\overline{09} & 0.63\overline{03} & 0.0\overline{78} \\ 0 & 0 & 0.5 \\ \frac{8}{13} & 0 & 0 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

然而再轉換為二進制並取近似到小數點後 8 bits，得到 Y 計算方式為 $0.0100101_2 * R + 0.000101_2 * G + 0.10100001_2 * B$，U 計算方式為 $0.1_2 * (B - Y)$，V 計算方式為 $0.10011110_2 * (R - Y)$，再用位移加法來完成。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (longest gate-level simulation time in ns)*

*= (286 + 0 + 9 * 0) * 23,447.900 = 6,706,099*