2017 Digital IC Design

Homework 5: Color Transform Engine

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| **Simulation Result** | | | | | | | | | | | |
| **Testfixture 1 (YUV -> RGB)** | | | | | | | | | | | |
| Functional simulation | | | Pass | | | Gate-level simulation | | | | Pass | |
| **Testfixture 2 (RGB -> YUV)** | | | | | | | | | | | |
| **Pattern 1** | Functional simulation | | | A | Gate-level simulation | | | A | Gate-level simulation time | | 23447.900 ns |
| **Pattern 2** | Functional simulation | | | A | Gate-level simulation | | | A | Gate-level simulation time | | 23447.900 ns |
| **Pattern 3** | Functional simulation | | | A | Gate-level simulation | | | A | Gate-level simulation time | | 23447.900 ns |
| Minimum CYCLE in Gate-level simulation | | | | | | | | 15.57 ns | | | |
| your pre-sim result of Testfixture 1  pre1.jpg | | | | | | | your post-sim result of Testfixture 1  post1.jpg | | | | |
| your pre-sim result of Testfixture 2, pattern 1  pre2a.jpg | | | | | | | your post-sim result of Testfixture 2, pattern 1  post2a.jpg | | | | |

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| your pre-sim result of Testfixture 2, pattern 2  pre2b.jpg | | your post-sim result of Testfixture 2, pattern 2  post2b.jpg |
| your pre-sim result of Testfixture 2, pattern 3  pre2c.jpg | | your post-sim result of Testfixture 2, pattern 3  post2c.jpg |
| **Synthesis Result** | | |
| Total logic elements | 286 | |
| Total memory bit | 0 | |
| Embedded multiplier 9-bit element | 0 | |
| (your flow summary)  quartus.jpg | | |
| **Description of your design** | | |
| 1. **Register file：**   分別為r\_data[0]、r\_data[1]、r\_data[2]，在op\_mode = 0時會依序存取YUV；op\_mode = 1時會存取RGB，如圖所示。     1. **Busy、Valid及其他控制訊號之處理：**     本電路採用類似轉盤的模型，經過設計，每完成一組計算（含YUV2RGB及RGB2YUV）需要6個cycle，故列舉Busy、Valid及其他控制訊號在這6個cycle所使用的訊號組成的Array，而每組Array可以想像為每個不同的轉盤，上面刻有6個刻度（如上圖），被綠色指針指到的刻度即為本周期輸出的訊號，然而每經過1個cycle後轉盤轉向下一個刻度，如此一來即能完成所有的Busy、Valid及其他控制訊號。經過比較，使用Counter或狀態機來決定Busy、Valid及其他控制訊號的方法所需的Delay時間較長，而轉盤方式能達到直接讀出訊號（僅有Register的Delay）是壓縮本電路計算時間的一大主因。   1. **YUV2RGB：**   先將YUV2RGB矩陣轉換為2進制，得到R計算方式為Y + 1.1012 \* V，G計算方式為Y - 0.012 \* U – 0.112 \* V，B計算方式為Y + 102 \* U。   1. **RGB2YUV：**   由於如果想要使用暴力解此矩陣需要花費大量的加法器（乘法器皆由加法器取代），故在此改變策略，先將原矩陣進行高斯消去法：  然而再轉換為二進制並取近似到小數點後8 bits，得到Y計算方式為0.010010102 \* R + 0.000101002 \* G + 0.101000012 \* B，U計算方式為0.12 \* B - 0.12 \* Y，V計算方式為0.100111102 \* R - 0.100111102 \* Y。 | | |

*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) (longest gate-level simulation time in ns)*

*= (286 + 0 + 9 \* 0) \* 23,447.900 = 6,706,099*