

Homework 4: Edge-Based Line Average interpolation

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Simulation Result						
Test pattern 1	Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	2433.740 ns
Test pattern 2	Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	2433.740 ns

```

VSIM 7> run -all
# -----
# \0\ All data have been generated successfully! \0\
#
# ** Note: $finish      : /home/yutongshen/HW4/testfixture.v(69)
#    Time: 2433740 ps   Iteration: 0   Instance: /test
# 1
# Break in Module test at /home/yutongshen/HW4/testfixture.v line 69

VSIM 9> run -all
# -----
# \0\ All data have been generated successfully! \0\
#
# ** Note: $finish      : /home/yutongshen/HW4/testfixture.v(69)
#    Time: 2433740 ps   Iteration: 0   Instance: /test
# 1
# Break in Module test at /home/yutongshen/HW4/testfixture.v line 69

VSIM 5> run -all
# -----
# \0\ All data have been generated successfully! \0\
#
# ** Note: $finish      : /home/yutongshen/HW4/testfixture.v(69)
#    Time: 2433740 ps   Iteration: 0   Instance: /test
# 1
# Break in Module test at /home/yutongshen/HW4/testfixture.v line 69

VSIM 3> run -all
# -----
# \0\ All data have been generated successfully! \0\
#
# ** Note: $finish      : /home/yutongshen/HW4/testfixture.v(69)
#    Time: 2433740 ps   Iteration: 0   Instance: /test
# 1
# Break in Module test at /home/yutongshen/HW4/testfixture.v line 69

```

Synthesis Result

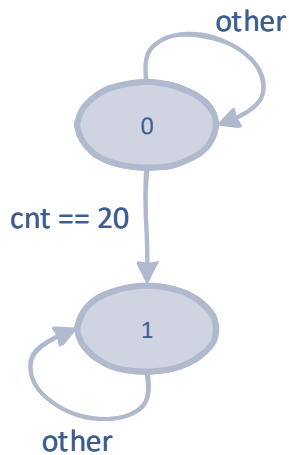
Total logic elements	341
Total memory bit	0
Embedded multiplier 9-bit element	0

Flow Summary	
Flow Status	Successful - Fri Dec 08 14:41:24 2017
Quartus II Version	10.0 Build 262 08/18/2010 SP 1 SJ Full Version
Revision Name	ELA
Top-level Entity Name	ELA
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Met timing requirements	N/A
Total logic elements	341 / 68,416 (< 1 %)
Total combinational functions	340 / 68,416 (< 1 %)
Dedicated logic registers	232 / 68,416 (< 1 %)
Total registers	232
Total pins	20 / 622 (3 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

FSM 設定：

本電路使用兩種狀態，初始化為狀態 0，故只需 1bit 儲存 current state。



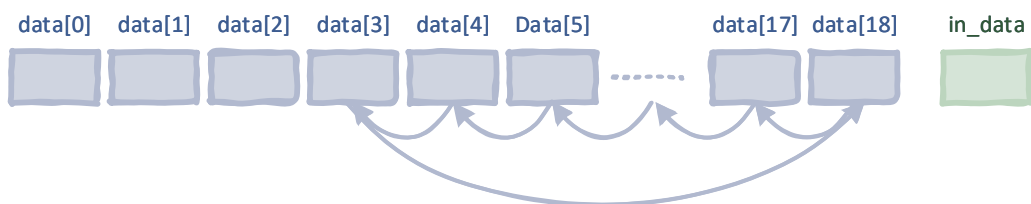
Register File 存取資料模式：

本電路使用的 Register File 共 19 個，儲存 in_data 分為兩種模式：

模式 1 為將 in_data 放置到 data[18]，然後把所有 data 往前位移。



模式 2 為將 data[3]放置到 data[18]，然後把 data[4]~data[18]往前位移。



FSM 運作：

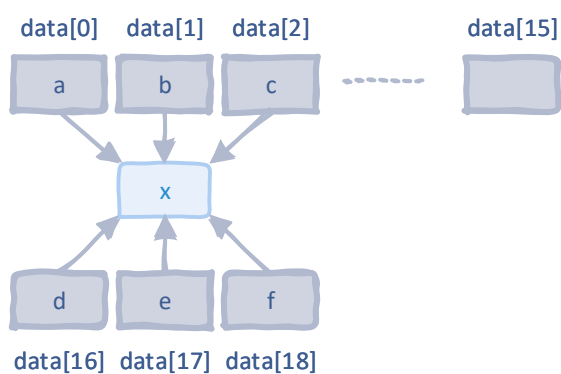
狀態 0 時，Register File 採用模式 1 推進資料，out_data 不斷的輸出

data[18]資料。

狀態 1 分為兩部分：

前 16 cycle，Register File 採用模式 1 推進資料，計算 out_data 方式為下

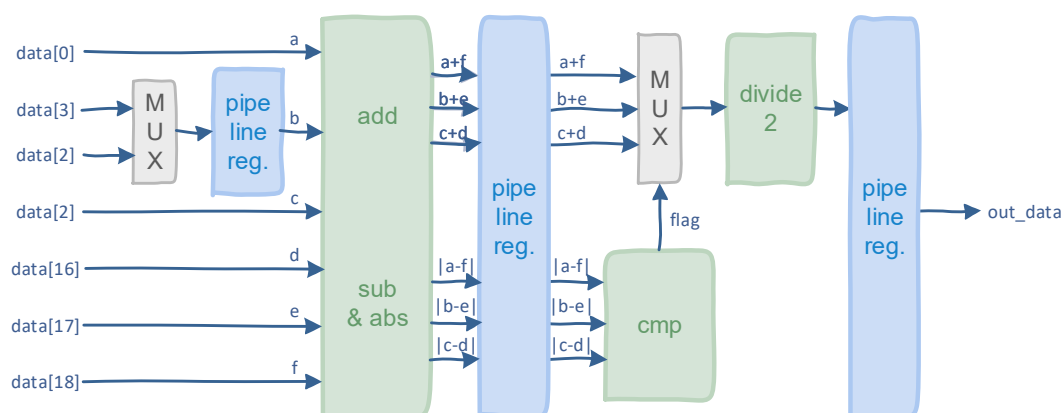
圖。



故本電路採用下圖電路切割 pipeline，其中 data[3]與 data[2]之間的 MUX

是為解決 Register File 推進資料模式改變後的第 1 個 cycle 造成資料位置差

異而設立。



後 16 cycle，Register File 採用模式 2 推進資料，out_data 不斷的輸出 data[16](因配合 pipeline 設計，in_data 與 out_data 存在 2 cycle delay，故需取 data[16])資料。

$$\begin{aligned} \text{Scoring} &= (\text{Total logic elements} + \text{total memory bit} + 9 * \text{embedded multiplier 9-bit element}) \times (\text{longest gate-level simulation time in } \underline{\text{ns}}) \\ &= (341 + 0 + 9 * 0) * 2,433.74 = 829,905 \end{aligned}$$