Device Usage Page (usage_statistics_webtalk.html)

This HTML page displays the device usage statistics that will be sent to Xilinx.

Software Version and Target Device			
Product Version:	ISE:14.7 (WebPack) - P.20131013	**Target Family:**	Spartan3
OS Platform:	NT64	**Target Device:**	xc3s50
Project ID (random number)	12515609d0dd49d58be7029b6b2c4f2d.0DB23DC06B794E8591294495CB57407B.48	**Target Package:**	pq208
Registration ID	__0_0_0	**Target Speed:**	-5
Date Generated	2018-01-24T14:48:26	**Tool Flow**	ISE

User Environment			
OS Name	Microsoft , 64-bit	**OS Release**	major release (build 9200)
CPU Name	Intel(R) Core(TM) i7-4702MQ CPU @ 2.20GHz	**CPU Speed**	2195 MHz

Device Usage Statistics

Macro Statistics	Miscellaneous Statistics	Net Statistics	Site Usage
Adders/Subtractors=21 • 6-bit adder=5 • 6-bit adder carry out=1 • 8-bit adder=14 • 8-bit adder carry out=1 FSMs=1 Registers=22 • Flip-Flops=22	MiscellaneousStatistics • AGG_BONDED_IO=26 • AGG_IO=26 • AGG_SLICE=26 • NUM_4_INPUT_LUT=27 • NUM_BONDED_IOB=26 • NUM_BUFGMUX=1 • NUM_SLICEL=26 • NUM_SLICE_FF=28	NetStatistics • NumNets_Active=84 • NumNets_Gnd=1 • NumNets_Vcc=1 • NumNodesOfType_Active_CLKPIN=20 • NumNodesOfType_Active_CNTRLPIN=30 • NumNodesOfType_Active_DOUBLE=127 • NumNodesOfType_Active_DUMMY=104 • NumNodesOfType_Active_DUMMYESC=10 • NumNodesOfType_Active_GLOBAL=10 • NumNodesOfType_Active_HFULLHEX=1 • NumNodesOfType_Active_HLONG=1 • NumNodesOfType_Active_HUNIHEX=5 • NumNodesOfType_Active_INPUT=149 • NumNodesOfType_Active_IOBOUTPUT=10 • NumNodesOfType_Active_OMUX=81 • NumNodesOfType_Active_OUTPUT=48 • NumNodesOfType_Active_PREBXBY=29 • NumNodesOfType_Active_VFULLHEX=2 • NumNodesOfType_Active_VLONG=1 • NumNodesOfType_Gnd_INPUT=1 • NumNodesOfType_Gnd_OMUX=1 • NumNodesOfType_Gnd_OUTPUT=1 • NumNodesOfType_Gnd_PREBXBY=1 • NumNodesOfType_Vcc_CNTRLPIN=1 • NumNodesOfType_Vcc_VCCOUT=1 SiteStatistics • IOB-DIFFM=11 • IOB-DIFFS=10 • SLICEL-SLICEM=12	SiteSummary • BUFGMUX=1 • BUFGMUX_GCLKMUX=1 • BUFGMUX_GCLK_BUFFER=1 • IOB=26 • IOB_INBUF=10 • IOB_OUTBUF=16 • IOB_PAD=26 • SLICEL=26 • SLICEL_F=13 • SLICEL_F5MUX=8 • SLICEL_FFX=18 • SLICEL_FFY=10 • SLICEL_G=14

Configuration Data

BUFGMUX • S=[S_INV:1] [S:0] BUFGMUX_GCLKMUX • DISABLE_ATTR=[LOW:1] • S=[S_INV:1] [S:0] IOB • O1=[O1_INV:0] [O1:16] • T1=[T1_INV:0] [T1:14] IOB_OUTBUF • IN=[IN_INV:0] [IN:16] • TRI=[TRI_INV:0] [TRI:14] IOB_PAD	SLICEL • BX=[BX_INV:0] [BX:18] • BY=[BY:12] [BY_INV:0] • CE=[CE:8] [CE_INV:0] • CLK=[CLK:20] [CLK_INV:0] • SR=[SR:8] [SR_INV:0] SLICEL_F5MUX • S0=[S0:8] [S0_INV:0] SLICEL_FFX • CE=[CE:8] [CE_INV:0] • CK=[CK:18] [CK_INV:0] • D=[D:18] [D_INV:0] • FFX_INIT_ATTR=[INIT0:18] • FFX_SR_ATTR=[SRLOW:18]	SLICEL_FFY • CK=[CK:10] [CK_INV:0] • D=[D:10] [D_INV:0] • FFY_INIT_ATTR=[INIT0:9] [INIT1:1] • FFY_SR_ATTR=[SRLOW:9] [SRHIGH:1] • LATCH_OR_FF=[FF:10] • SR=[SR:6] [SR_INV:0] • SYNC_ATTR=[ASYNC:4] [SYNC:6]

• DRIVEATTRBOX=[12:16] • IOATTRBOX=[LVCMOS25:26] • SLEW=[SLOW:16]	• LATCH_OR_FF=[FF:18] • REV=[REV_INV:0] [REV:2] • SR=[SR:6] [SR_INV:0] • SYNC_ATTR=[ASYNC:12] [SYNC:6]	

Pin Data

BUFGMUX • I0=1 • O=1 • S=1 BUFGMUX_GCLKMUX • I0=1 • OUT=1 • S=1 BUFGMUX_GCLK_BUFFER • IN=1 • OUT=1 IOB • I=10 • O1=16 • PAD=26 • T1=14 IOB_INBUF • IN=10 • OUT=10	IOB_OUTBUF • IN=16 • OUT=16 • TRI=14 IOB_PAD • PAD=26 SLICEL • BX=18 • BY=12 • CE=8 • CLK=20 • F1=13 • F2=13 • F3=13 • F4=12 • G1=14 • G2=14 • G3=13 • G4=11 • SR=8 • X=13 • XQ=18 • Y=6 • YQ=10	SLICEL_F • A1=13 • A2=13 • A3=13 • A4=12 • D=13 SLICEL_F5MUX • F=8 • G=8 • OUT=8 • S0=8 SLICEL_FFX • CE=8 • CK=18 • D=18 • Q=18 • REV=2 • SR=6	SLICEL_FFY • CK=10 • D=10 • Q=10 • SR=6 SLICEL_G • A1=14 • A2=14 • A3=13 • A4=11 • D=14

Tool Usage

Command Line History

- xst -intstyle ise -ifn <ise_file>
- xst -intstyle ise -ifn <ise_file>
- ngdbuild -intstyle ise -dd _ngo -nt timestamp -i -p xc3s50-pq208-4 <ise_file> <fname>.ngd
- map -intstyle ise -p xc3s50-pq208-4 -cm area -ir off -pr off -c 100 -o <fname>.ncd <fname>.ngd <fname>.pcf
- par -w -intstyle ise -ol high -t 1 <fname>.ncd <fname>.ncd <fname>.pcf
- trce -intstyle ise -v 3 -s 4 -n 3 -fastpaths -xml <fname>.twx <fname>.ncd -o <fname>.twr <fname>.pcf
- xst -intstyle ise -ifn <ise_file>
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- trce -intstyle ise -v 3 -s 4 -n 3 -fastpaths -xml <fname>.twx <fname>.ncd -o <fname>.twr <fname>.pcf
- netgen -intstyle ise -ar Structure -tm <design> -w -dir netgen/synthesis -ofmt vhdl -sim <fname>.ngc <fname>.vhd
- xst -intstyle ise -ifn <ise_file>
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- ngdbuild -intstyle ise -dd _ngo -nt timestamp -i -p xc3s50-pq208-4 <ise_file> <fname>.ngd
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- bitgen -intstyle ise -f <fname>.ut <fname>.ncd
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- xst -intstyle ise -ifn <ise_file>
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- par -w -intstyle ise -ol high -t 1 <fname>.ncd <fname>.ncd <fname>.pcf
- trce -intstyle ise -v 3 -s 4 -n 3 -fastpaths -xml <fname>.twx <fname>.ncd -o <fname>.twr <fname>.pcf
- xst -intstyle ise -ifn <ise_file>
- ngdbuild -intstyle ise -dd _ngo -nt timestamp -i -p xc3s50-pq208-5 <ise_file> <fname>.ngd
- map -intstyle ise -p xc3s50-pq208-5 -cm area -ir off -pr off -c 100 -o <fname>.ncd <fname>.ngd <fname>.pcf
- par -w -intstyle ise -ol high -t 1 <fname>.ncd <fname>.ncd <fname>.pcf
- trce -intstyle ise -v 3 -s 5 -n 3 -fastpaths -xml <fname>.twx <fname>.ncd -o <fname>.twr <fname>.pcf
- bitgen -intstyle ise -f <fname>.ut <fname>.ncd
- fuse

Software Quality							
Run Statistics							
Program Name	**Runs Started**	**Runs Finished**	**Errors**	**Fatal Errors**	**Internal Errors**	**Exceptions**	**Core Dumps**
bitgen	3	3	0	0	0	0	0
map	174	146	0	0	0	0	0
netgen	2	2	0	0	0	0	0
ngdbuild	179	179	0	0	0	0	0
par	146	146	0	0	0	0	0
trce	146	146	0	0	0	0	0
xst	579	578	0	0	0	0	0

Help Statistics
Help files
/doc/usenglish/isehelp/pn_db_design_properties.htm (1)

Project Statistics	
PROPEXT_xilxSynthMaxFanout_virtex2=100000	PROP_Enable_Message_Filtering=false
PROP_FitterReportFormat=HTML	PROP_LastAppliedGoal=Balanced
PROP_LastAppliedStrategy=Xilinx Default (unlocked)	PROP_ManualCompileOrderImp=false
PROP_PropSpecInProjFile=Store all values	PROP_SelectedInstanceHierarchicalPath=/veNeumannComputer
PROP_Simulator=ISim (VHDL/Verilog)	PROP_SynthTopFile=changed
PROP_Top_Level_Module_Type=HDL	PROP_UseSmartGuide=false
PROP_UserConstraintEditorPreference=Text Editor	PROP_intProjectCreationTimestamp=2018-01-03T15:12:27
PROP_intWbtProjectID=0DB23DC06B794E8591294495CB57407B	PROP_intWbtProjectIteration=48
PROP_intWorkingDirLocWRTProjDir=Same	PROP_intWorkingDirUsed=No
PROP_selectedSimRootSourceNode_behav=work.veNeumannComputer	PROP_xilxBitgStart_IntDone=true
PROP_AutoTop=false	PROP_DevFamily=Spartan3
PROP_DevDevice=xc3s50	PROP_DevFamilyPMName=spartan3
PROP_DevPackage=pq208	PROP_Synthesis_Tool=XST (VHDL/Verilog)
PROP_DevSpeed=-5	PROP_PreferredLanguage=VHDL
FILE_VHDL=11	

Unisim Statistics			
NGDBUILD_PRE_UNISIM_SUMMARY			
NGDBUILD_NUM_BUFGP=1	NGDBUILD_NUM_FDE=16	NGDBUILD_NUM_FDR=3	NGDBUILD_NUM_FDRE=6
NGDBUILD_NUM_FDRS=2	NGDBUILD_NUM_FDS=1	NGDBUILD_NUM_GND=1	NGDBUILD_NUM_IBUF=9
NGDBUILD_NUM_LUT2=1	NGDBUILD_NUM_LUT3=3	NGDBUILD_NUM_LUT4=23	NGDBUILD_NUM_MUXF5=8
NGDBUILD_NUM_OBUF=2	NGDBUILD_NUM_OBUFT=14	NGDBUILD_NUM_VCC=1	
NGDBUILD_POST_UNISIM_SUMMARY			
NGDBUILD_NUM_BUFG=1	NGDBUILD_NUM_FDE=16	NGDBUILD_NUM_FDR=3	NGDBUILD_NUM_FDRE=6
NGDBUILD_NUM_FDRS=2	NGDBUILD_NUM_FDS=1	NGDBUILD_NUM_GND=1	NGDBUILD_NUM_IBUF=9
NGDBUILD_NUM_IBUFG=1	NGDBUILD_NUM_LUT2=1	NGDBUILD_NUM_LUT3=3	NGDBUILD_NUM_LUT4=23
NGDBUILD_NUM_MUXF5=8	NGDBUILD_NUM_OBUF=2	NGDBUILD_NUM_OBUFT=14	NGDBUILD_NUM_VCC=1

XST Command Line Options
XST_OPTION_SUMMARY

-ifn=<fname>.prj	-ifmt=mixed	-ofn=<design_top>	-ofmt=NGC
-p=xc3s50-5-pq208	-top=<design_top>	-opt_mode=Speed	-opt_level=1
-iuc=NO	-keep_hierarchy=No	-netlist_hierarchy=As_Optimized	-rtlview=Yes
-glob_opt=AllClockNets	-read_cores=YES	-write_timing_constraints=NO	-cross_clock_analysis=NO
-bus_delimiter=<>	-slice_utilization_ratio=100	-bram_utilization_ratio=100	-verilog2001=YES
-fsm_extract=YES	-fsm_encoding=Auto	-safe_implementation=No	-fsm_style=LUT
-ram_extract=Yes	-ram_style=Auto	-rom_extract=Yes	-shreg_extract=YES
-rom_style=Auto	-auto_bram_packing=NO	-resource_sharing=YES	-async_to_sync=NO
-mult_style=Auto	-iobuf=YES	-max_fanout=100000	-bufg=8
-register_duplication=YES	-register_balancing=No	-optimize_primitives=NO	-use_clock_enable=Yes
-use_sync_set=Yes	-use_sync_reset=Yes	-iob=Auto	-equivalent_register_removal=YES
-slice_utilization_ratio_maxmargin=5			

ISim Statistics
Xilinx HDL Libraries Used=std, ieee
Fuse Resource Usage=593 ms, 30932 KB
Total Signals=91
Total Nets=111
Total Blocks=12
Total Processes=19
Total Simulation Time=1 us
Simulation Resource Usage=0.34375 sec, 812068 KB
Simulation Mode=gui
Hardware CoSim=0