FINAL SPRING 2024

Graded

Student

Total Points

101 / 101 pts

Question 1

(no title) **21** / 21 pts

1.1 **(no title)** **6** / 6 pts

✔ **+ 6 pts** Correct

x	y	z	E	F	G
0	0	0	0	0	1
0	0	1	d	d	d
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	1	1	0
1	0	1	1	1	0
1	1	0	d	d	d
1	1	1	d	d	d

1.2 **(no title)** **8** / 8 pts

✔ **+ 8 pts** Correct

$$E = x + y$$
$$F = x$$
$$G = x'y' + x'z$$
$$G = x'y' + yz$$

1.3 **(no title)** **7** / 7 pts

✔ **+ 7 pts** Correct

Question 2

(no title) **20** / 20 pts

2.1 (no title) **12** / 12 pts

✔ **− 0 pts** Correct (x'z' + xz)

2.2 (no title) **8** / 8 pts

✔ **− 0 pts** Correct K-Map and results (x'z + xz)

Question 3

(no title) **1** / 1 pt

✔ **+ 1 pt** Correct

Question 4

(no title) **31** / 31 pts

4.1 (no title) **10** / 10 pts

✔ **+ 10 pts** Correct

4.2 (no title) **7** / 7 pts

✔ **− 0 pts** Correct

4.3 (no title) **7** / 7 pts

✔ **− 0 pts** Correct

4.4 (no title) **7** / 7 pts

✔ **+ 7 pts** Correct

Question 5

(no title) **28** / 28 pts

5.1 **(no title)** **7** / 7 pts

✔ **+ 7 pts** Correct

5.2 **(no title)** **Resolved** **7** / 7 pts

✔ **+ 7 pts** Correct

Regrade Request **Submitted on: May 23**

I mistakenly wrote Da and Db instead of An+1 and Bn+1. However, above Da and Db says Next State so I don't see the confusion. And the grade says I didn't compute the next states but I clearly did... if i didn't how else could I have done the state diagram

Okay, I'll give you the benefit of the doubt. Many other students only computed D*A and D_B and not A*{n+1} and B_{n+1}.

Reviewed on: May 24

5.3 **(no title)** **7** / 7 pts

✔ **+ 7 pts** Correct

5.4 **(no title)** **7** / 7 pts

✔ **+ 7 pts** Correct

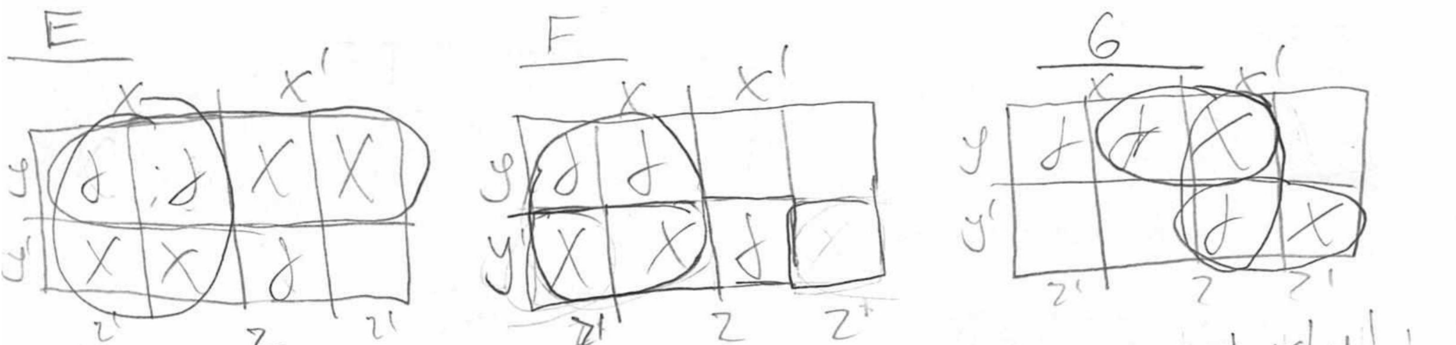
1. Design a combinational circuit with three inputs: x, y, z and three outputs: E, F, G, such that,

- When the binary input xyz represents the decimal digits $2, 3,$ or 4, the binary output EFG should represent the decimal digit that is 2 greater than the input: that is $4, 5, or\ 6$ respectively.
- Similarly, when the binary input represents the digits 0 or 5, the binary output should represent the digit that is 1 greater than the input.
  1 6
- The remaining three, binary representations of the decimal digits $1, 6,$ and 7 never occur.

a) Start by drawing the truth table for the functions $E, F,$ and G.

X	y	z	E	F	G
0	0	0	0	0	1
0	0	1	d	d	d
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	1	1	0
1	0	1	1	1	0
1	1	0	d	d	d
1	1	1	d	d	d

b) Next, using K-Maps find all minimal forms of the three functions.

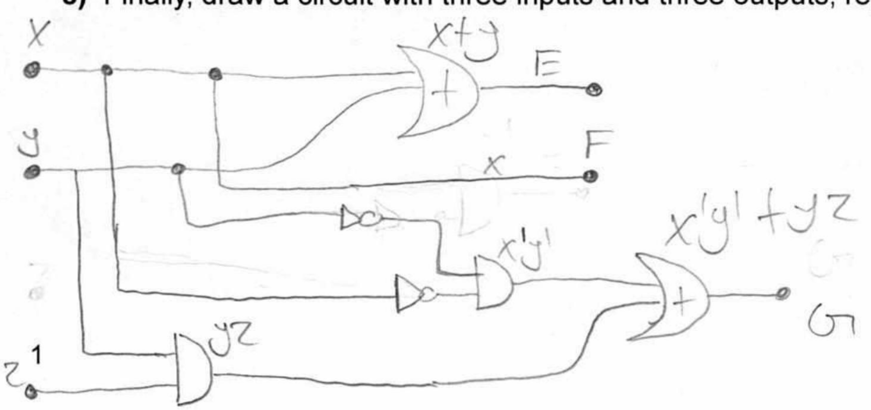


$E = X + y$

$F = X$

$G = yz + x'y'$
or $x'z + xy'$

c) Finally, draw a circuit with three inputs and three outputs, representing a minimal form of the functions.



2. a) Find all minimal forms of the function below using the Tabulation Method and the Prime Implicant Table.

$f = \Sigma(0, 2, 5, 7) + d\Sigma(3, 6)$

Index	Binary	Decimal
0	000	0
1	010	2
2	011	3
	101	5
	110	6
3	111	7

Index	Binary	Decimal
0	0-0	0,2
1	01-	2,3
	-10	2,6
2	-11	3,7
	1-1	5,7
	11-	6,7

Index	Binary	Decimal
0	0-0	0,2
1	-1-	2,3,6,7
2	1-1	5,7

	x'z'	y	xz
0	X		
2	X	X	
5			X
7		X	X

Essential

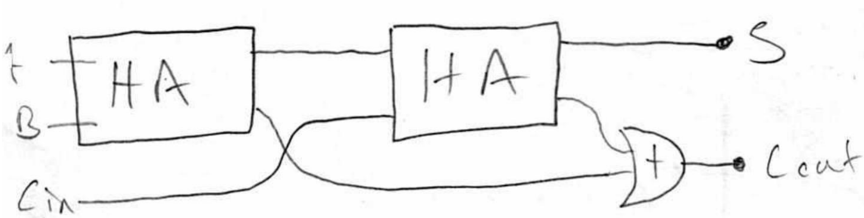
$xz + x'z'$

b) Now use a K-Map to confirm your results in 2.a).

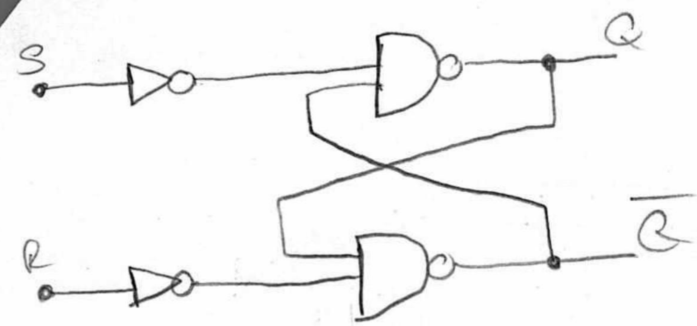
	x	x	x'	x'
y	d	X	d	X
y'		X		X
	z'	z		z'

→ $xz + x'z'$

3. Draw a full-adder using two half-adders, and one more simple gate only.



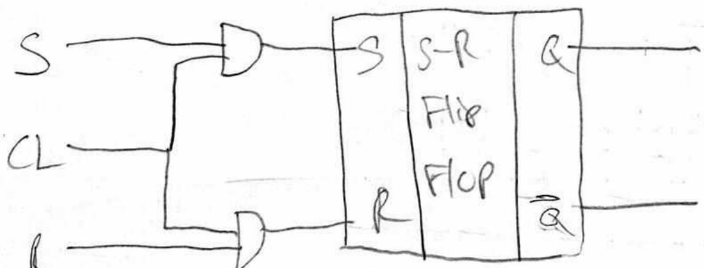
a) Draw a simple S-R-Flip-Flop using two gates and inverters, and show the truth table for this flip-flop.



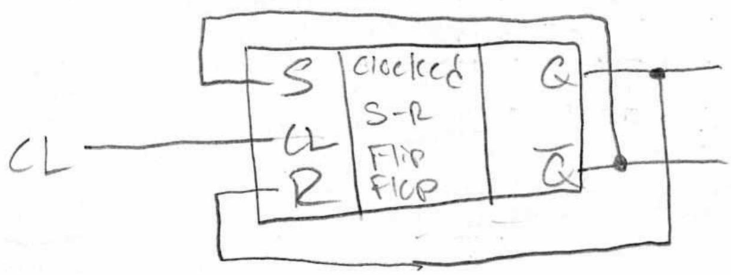
S	R	Q	$\overline{Q}$
0	0	PS	PS
0	1	0	1
1	0	1	0

1,1 doesn't count

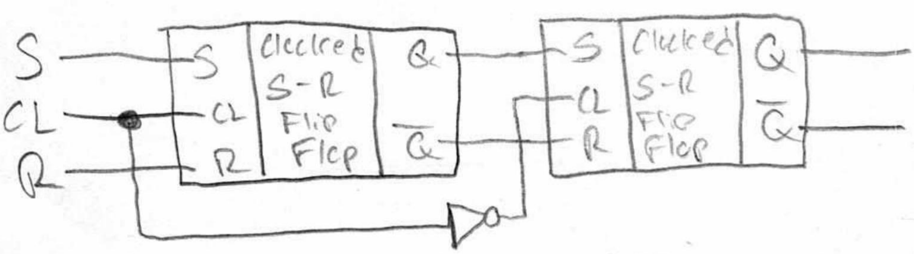
b) Draw a Clocked (controlled) S-R-Flip-Flop using an existing simple S-R-Flip-Flop and additional gates.



c) Draw a T-Flip-Flop using an existing Clocked S-R-Flip-Flop and wires only.



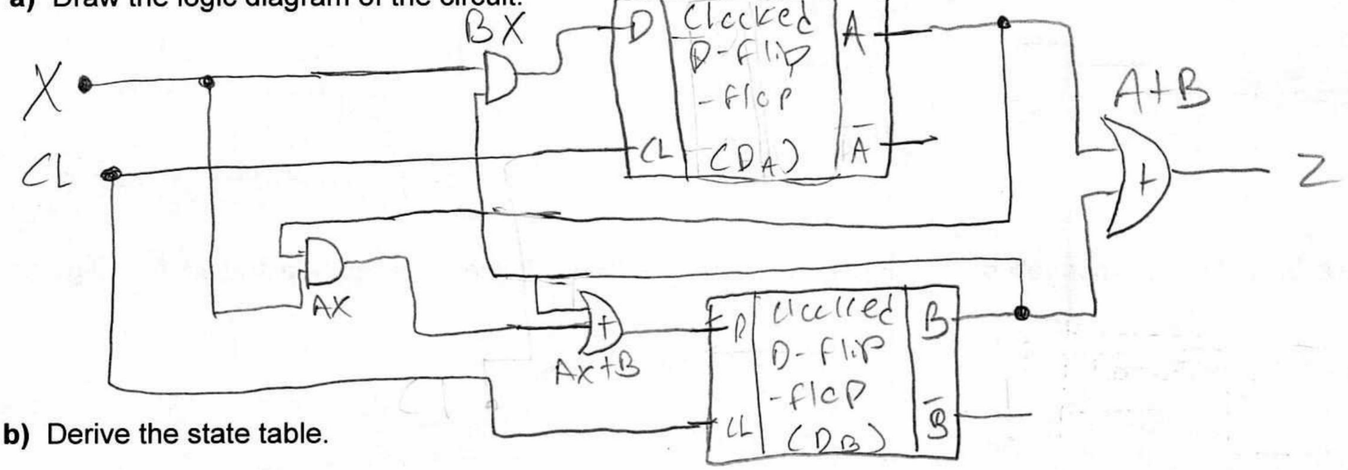
d) Draw the Racing Problem solution for a Clocked S-R-Flip-Flop using two existing Clocked S-R-Flip-Flops.



5. A sequential circuit with two clocked *D-flip-flops* A and B, one input x, and one output z is specified by the following input equations:

$$D_A = B*x\,,\quad D_B = A*x + B\,,\quad z = A+B$$

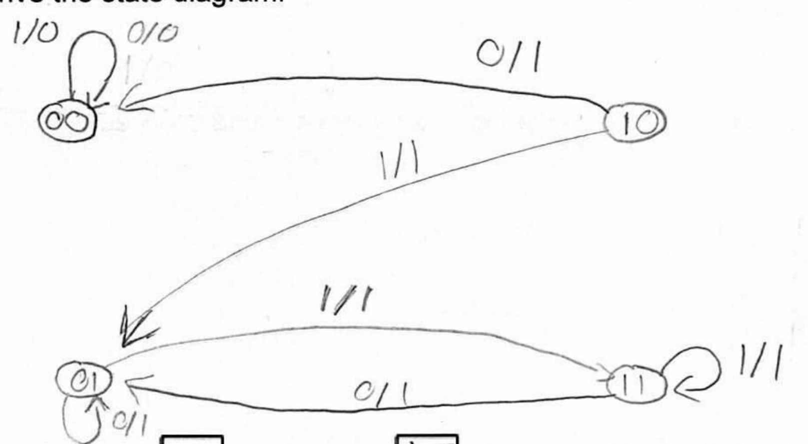
a) Draw the logic diagram of the circuit.



b) Derive the state table.

Previous State		Input	Next State		Output
A	B	x	D_A	D_B	z
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	1	1
0	1	1	1	1	1
1	0	0	0	0	1
1	0	1	0	1	1
1	1	0	0	1	1
1	1	1	1	1	1

c) Derive the state diagram.



d) Is this a Mealy ☐ or a Moore ☒ finite state machine? Check the appropriate box.