# Multi-core Programming

## Assignment 5

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#### Abstract

In this report, we'll analyze the *prefix-sum* (*scan*) problem. There are many uses for scan, including, but not limited to, sorting, lexical analysis, string comparison, polynomial evaluation, stream compaction, and building histograms and data structures (graphs, trees, and so on) in parallel. There are also multiple solutions and algorithms to compute the prefix sum of an array. Sources for this report are provided in the *src* folder.

Keywords.

# 1 Hillis & Steele Algorithm

#### 1.1 How it works?

Recall that in each step, we had to add up the elements of the array until now and replace the current element with the addition result. The sequential implementation takes exactly n operations (n is the size of the array) to complete. The Hillis & Steele algorithm, provides a simple and intuitive parallelization trick using addition as a binary operator which takes only two arguments. The idea is parallel in theory but it has some problems in practice. Figure 1.1 demonstrates this algorithm better.

## 1.2 Assumptions

This algorithm assumes that there are as many as processors as data elements. The programmer must divide the computation among a number of thread blocks that each scans a portion of the array on a single multiprocessor of the GPU. Even still, the number of processors in a multiprocessor is typically much smaller than the number of threads per block, so the hardware automatically partitions the *for all* statement into small parallel batches (called warps) that are executed sequentially on the multiprocessor. Because not all threads run simultaneously for arrays larger than the warp size, this algorithm will not work, because it performs the scan in place on the array. The results of one warp will be overwritten by threads in another warp.

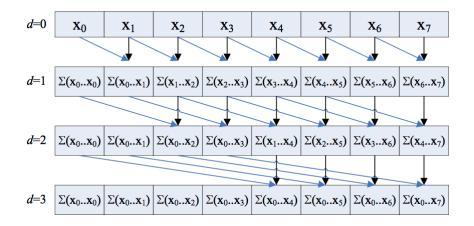


Figure 1.1: Demonstration of *Hillis & Steele* Algorithm.

## 1.3 Work Efficiency

Even if this algorithm works in some cases, it is not *work efficient*. The minimum number of addition operations needed in the sequential algorithm was n. In this algorithm, this number increases to  $n \log n$ . That's the main reason we call the *Hillis & Steele* algorithm a *work inefficient* algorithm.

## 1.4 Pseudocode

```
1: for d = 1 to log2 n do
2: for all k in parallel do
3: if k >= power(2, d) then
4: x[k] = x[k - power(2, d-1)] + x[k]
```

## 1.5 CUDA Kernel

This implementation can handle arrays not bigger than a *warp* size.

# 1.6 Grid & Block Size Analysis

For the first implementation, I've chose the grid size to be 1 in a one dimensional manner. I've also selected the block size as 32 (same as warp size) in the first dimension. Grid size is dedicated to our estimation of number of blocks needed to process the data. The block size should be selected so that computation mean squared error is 0. In this case, the proper size for the blocks is 32 (same as

warp size). The reason is there are multiple add operations needed to be written back to the array a whenever each thread does its job. The problem does not appear until the number of threads is greater than the warp size(32). Each warp overwrites the values previous warp was written. That yields incorrect results.

## 1.7 Mean Squared Error Analysis

All of the results are evaluated using *Mean Squared Error* metric. The code is given below:

```
float compute_mse(int *a, int *b, int n) {
    float err;

    for (int i = 0; i < n; i++) {
        err += pow(a[i] - b[i], 2);
    }

    return err;
}</pre>
```

The mean squared error for arrays not bigger than the warp size (which is 32 in my case), is 0. For warp sizes greater than 32 the error increases. The result is absolutely stunning! As you can see in the figure 1.2, the mean square error for the input of sizes less than 32 is computed without errors. That's mainly because of the issue with the maximum number of threads running together. Figure 1.3 illustrates this issue as the size of the input array goes higher than 32.

Figure 1.2: Computed MSE for Arrays with Size Less than 32.

```
[-] Please enter N: 33
[-] array: 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 31, 32, 33
Processing data on GPU...
Computation error is 278784.000000
[-] array: 1, 3, 6, 10, 15, 21, 28, 36, 45, 55, 66, 78, 91, 105, 120, 136, 351, 378, 406, 435, 465, 496, 528, 33
Press any key to continue . . .
```

Figure 1.3: Computed MSE for Arrays with Size Greater than 32.

# 1.8 Performance Analysis

Now, let's look at how this implementation performs against the sequential implementation. Table 1.1 illustrates this phenomenon.

Size	5 MB	50 MB	80 MB
Error	Very High	Very High	Very High
(grid, block)	(n/1024, 1024)	(n/1024, 1024)	(n/1024, 1024)
Time(ms)	1.285472	1.431008	1.461440

Table 1.1: Results of Prefix Sum Sequential Implementation of *integer* type.

As can be seen from this table, there is a lot of computation error with the raw algorithm of Hillis & Steele. The improvement of the algorithm in next section will solve this problem.

# 1.9 A Deeper Look at Blocks and Grids

Here we'll suppose the array size to be 5 MB only. In this case, there are 1250000 integer elements in the array. Since each multiprocessor can accept up to 1024 threads, we can set the number of blocks to 1221 (Ceil of 1220.70) and the number of threads to 1024 in each block. This solution will not work since the warp size is 32 and there is dependency in different steps of the algorithm. The array will be overwritten and the result is incorrect.