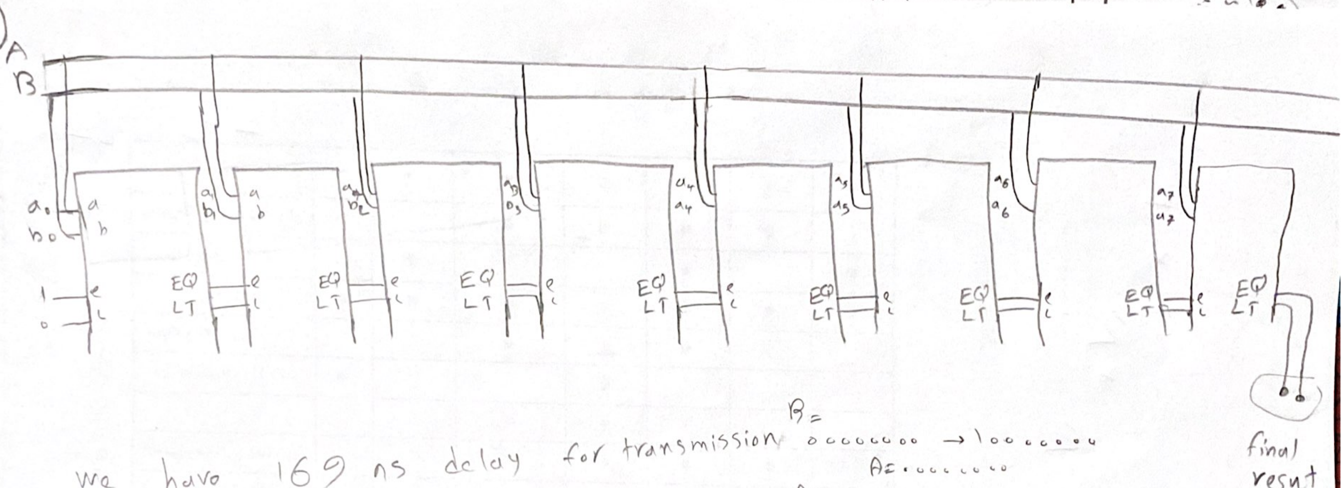
810198519

Worksheet

②



we have 169 ns delay for transmission B= 00000000 → 10000000 A=00000000

we have 158 ns delay for transmission A= 00000000 → 10000000 B=10000000

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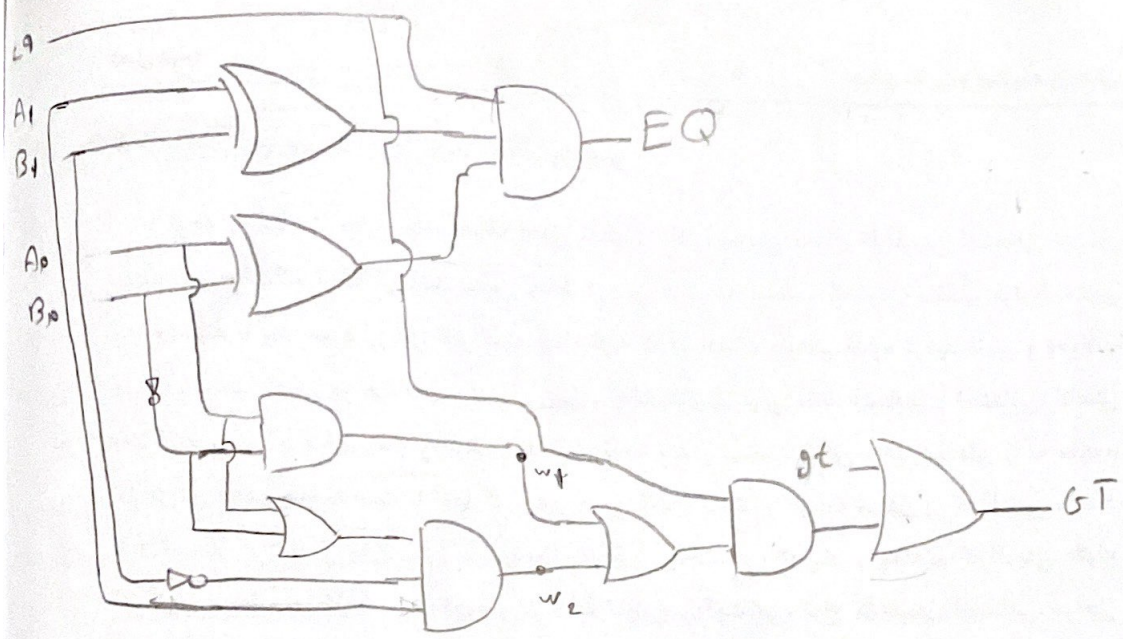
(3)



EQ:

worst case delay To1: 3_input_AND To1 (17) + XNOR To1 (12) = 29

worst case delay To0: 3_input_AND To0 (22) + XNOR To0 (12) = 34

GT:

To1: OR (19) + AND (13) + OR (19)
- $w_1=0$ → AND (17) ⇒ $A_1=0$
- $w_1=1$ → 3_input AND (17) + OR ($B_1=0$) → inverter To1 (19 + 5) = 92

To0: OR (17) + AND (17) + OR (17)
- $w_1=0$ → AND (17) ⇒ $A_1=0$
- $w_1=0$ → 3_input AND (22) + OR ($B_1=1$) → inverter To0 (17 + 7) = 97

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we have 368 ns delay when this transmition occurs: (4)

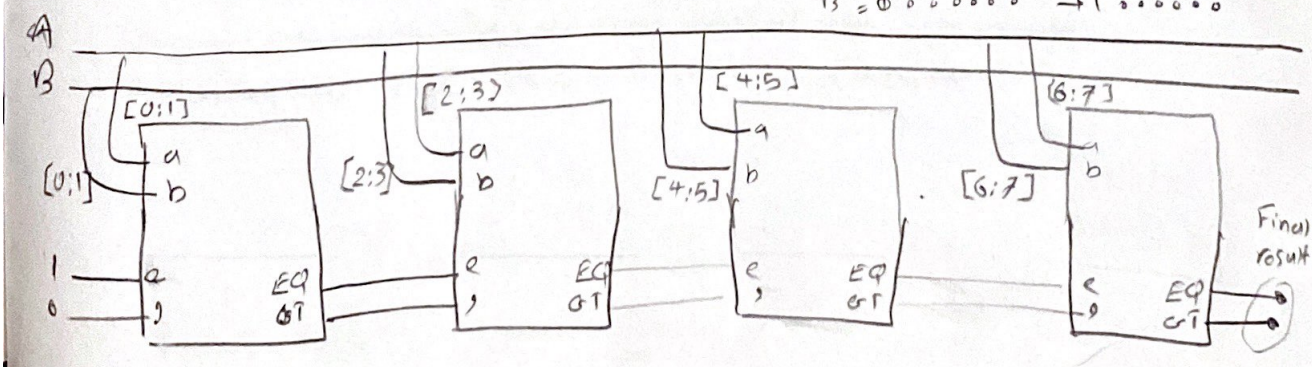
A= 00000000 → 10000000

B= 00000000

we have 388 ns delay when this transmition occurs

A = 10000000

B = 00000000 → 10000000



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(5)

disadvantages of TCS: we needed to implement it again like other gates such as 3-input NAND and bigger delay value for small numbers

advantages of TCS: in bigger nums and more significant bits, TCS is better than BCS less gates overall for delay