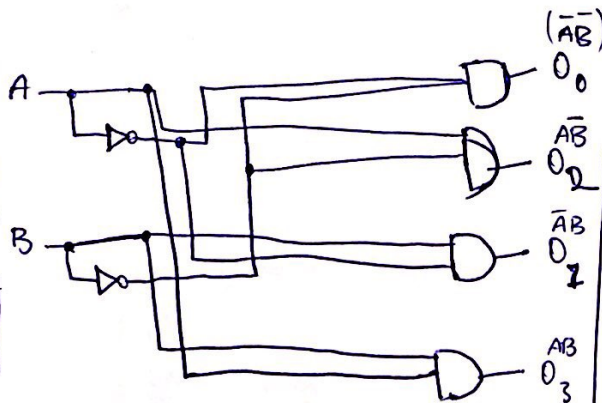


Decoder  
4x2

in	out
00	0000
01	0001
11	0100
10	1000



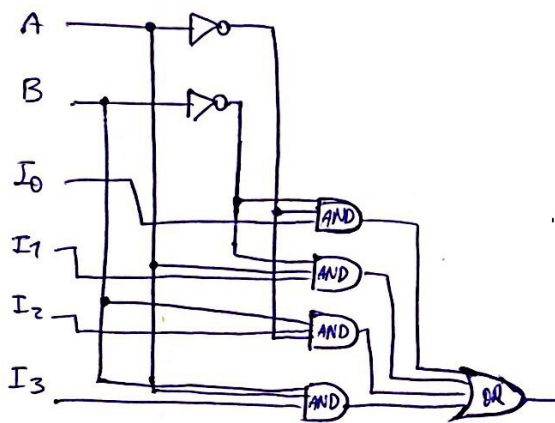
```

module decoder (in, out, enb);
    input [1:0] in;
    input enb;
    output [3:0] out;
    wire [5:0] out;
    assign out = (enb) ?
        (1 << in) : 16'b0;
endmodule

```

MUX  
4x1

AB	out
00	I <sub>0</sub>
01	I <sub>1</sub>
10	I <sub>2</sub>
11	I <sub>3</sub>



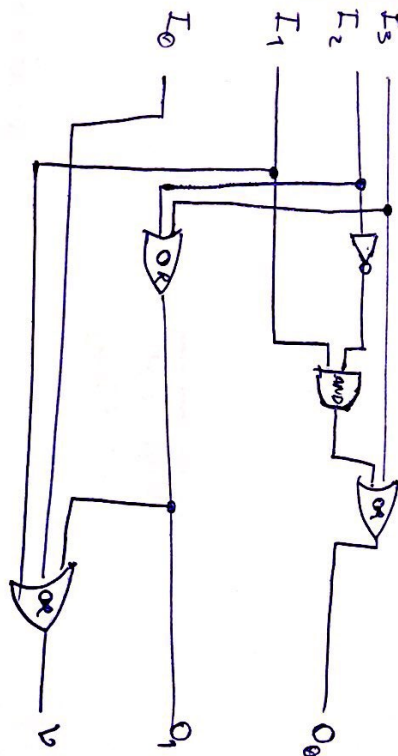
```

module mux (in, sel, out);
    input [3:0] in; sel;
    output out;
    wire out;
    assign out = (sel) ? in[3] :
        in[2] : in[1] : in[0];
endmodule

```

Priority  
Encoder  
4x2

I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	O <sub>1</sub>	O <sub>0</sub>	V
0	0	0	0	x	x	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	x	1	0	1
1	x	x	x	1	1	1



```

module pEncoder (in, out);
    input in [3:0]; V;
    output out [2:0];
    assign O0 = in[3] | (~in[2] & in[1]);
    assign O1 = in[3] | in[2];
    assign V = O1 | in[0] | in[1];
endmodule

```