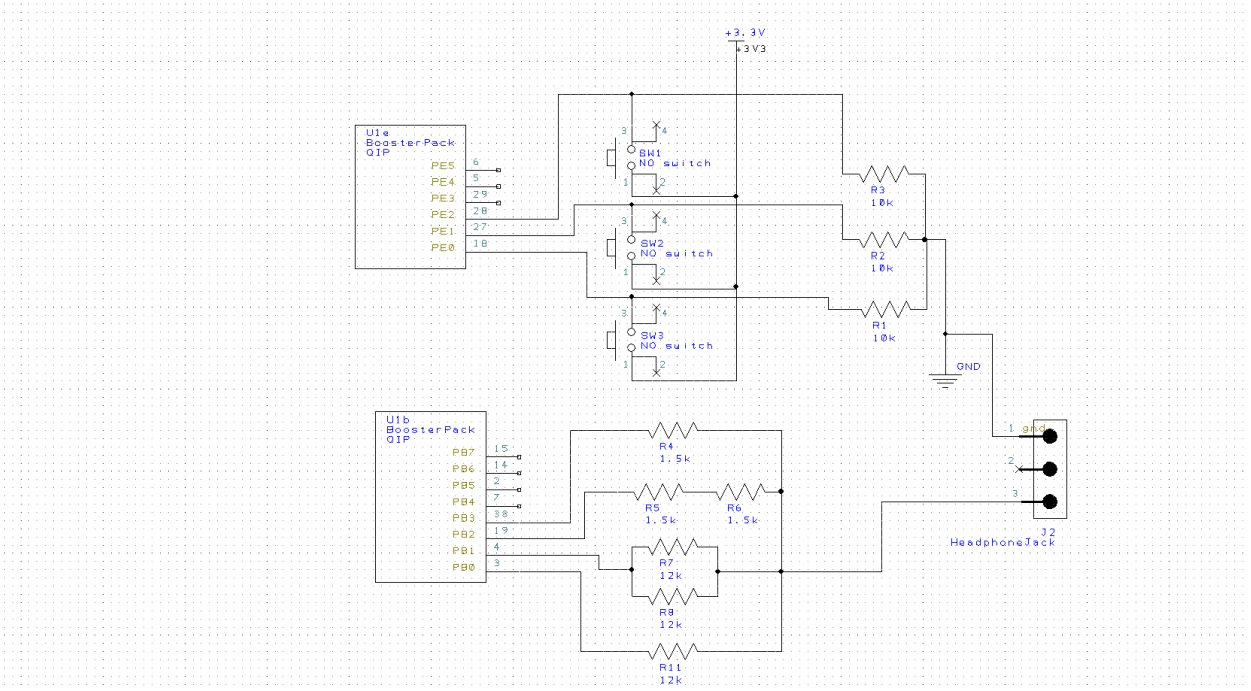
Circuit Schematic



All resistors are 1/4 watt 5% carbon composition
C1 is ceramic Z5U
Switches are www.BGMicro.com SWT1043
Red LEDs. T1 3/4. 20mA Digikey 160-1087-ND
Yellow LEDs. T1 3/4. 20mA Digikey 160-1088-ND
Green LEDs. T1 3/4. 20mA Digikey 160-1089-ND
Slide pot. Bourns SSHA20B20300 www.AllElectronics.comSP-20K

University Of Texas At Austin	
Schematic Name: EK-TM4C123GXL	
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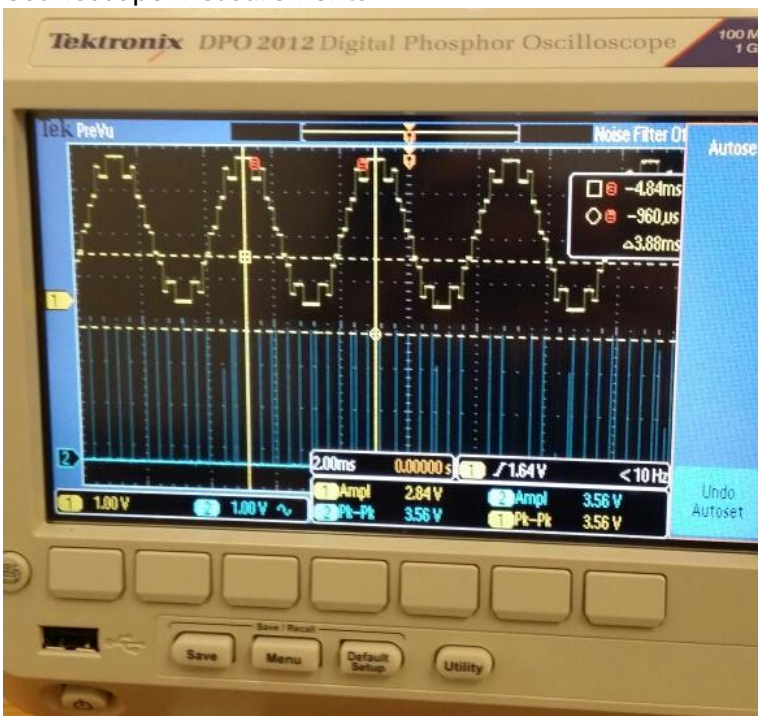
Oscilloscope Measurements



Sine Table Array for Piano wave:

SinTab[0] 8
SinTab[1] 9
SinTab[2] 11
SinTab[3] 13
SinTab[4] 14
SinTab[5] 14
SinTab[6] 15
SinTab[7] 15
SinTab[8] 15
SinTab[9] 15
SinTab[10] 14
SinTab[11] 14
SinTab[12] 13
SinTab[13] 11
SinTab[14] 9
SinTab[15] 8
SinTab[16] 7
SinTab[17] 6
SinTab[18] 4
SinTab[19] 2
SinTab[20] 1
SinTab[21] 1
SinTab[22] 0
SinTab[23] 0
SinTab[24] 0
SinTab[25] 0
SinTab[26] 1
SinTab[27] 1
SinTab[28] 2
SinTab[29] 4
SinTab[30] 6
SinTab[31] 7

Bit3 bit2 bit1 bit0	Theoretical DAC voltage	Measured DAC voltage
0	0V	0V
1	0.22V	0.219V
2	0.44V	0.438V
3	0.66V	0.657V
4	0.88V	0.878V
5	1.1V	1.089V
6	1.32V	1.320V
7	1.54V	1.538V
8	1.76V	1.757V
9	1.98V	1.979V
10	2.2V	2.187V
11	2.42V	2.417V
12	2.64V	2.638V
13	2.86V	2.859V
14	3.08V	3.067V
15	3.3V	3.258V

Range(volts) = Precision * Resolution(volts)
Range = 3.3-0 = 3.3V
Resolution = 16V
Precision = 0.206
Accuracy = 0.4545%

Brief, one sentence answers to the following questions

a. When does the interrupt trigger occur?
It occurs when the value of the current register in the SysTick hits 0.

b. In which file is the interrupt vector?
Startup.s

c. List the steps that occur after the trigger occurs and before the processor executes the handler.
The PC and the PSR get saved onto the stack.

d. It looks like **`BX LR`** instruction simply moves LR into PC, how does this return from interrupt?
Before the Handler is executed, the PC saved to LR is the incremented PC therefore when PC is restored back, it points to the next instruction in the program (this is for returning from a subroutine). An arbitrary value will be put into the link register to indicate that it is indeed returning from an interrupt rather than a subroutine.