# UART Transmitter implementation

Ali Morgan

Mohamed Maged

Khalid Montaser

Ahmed Elshrif

## 1 Architecture

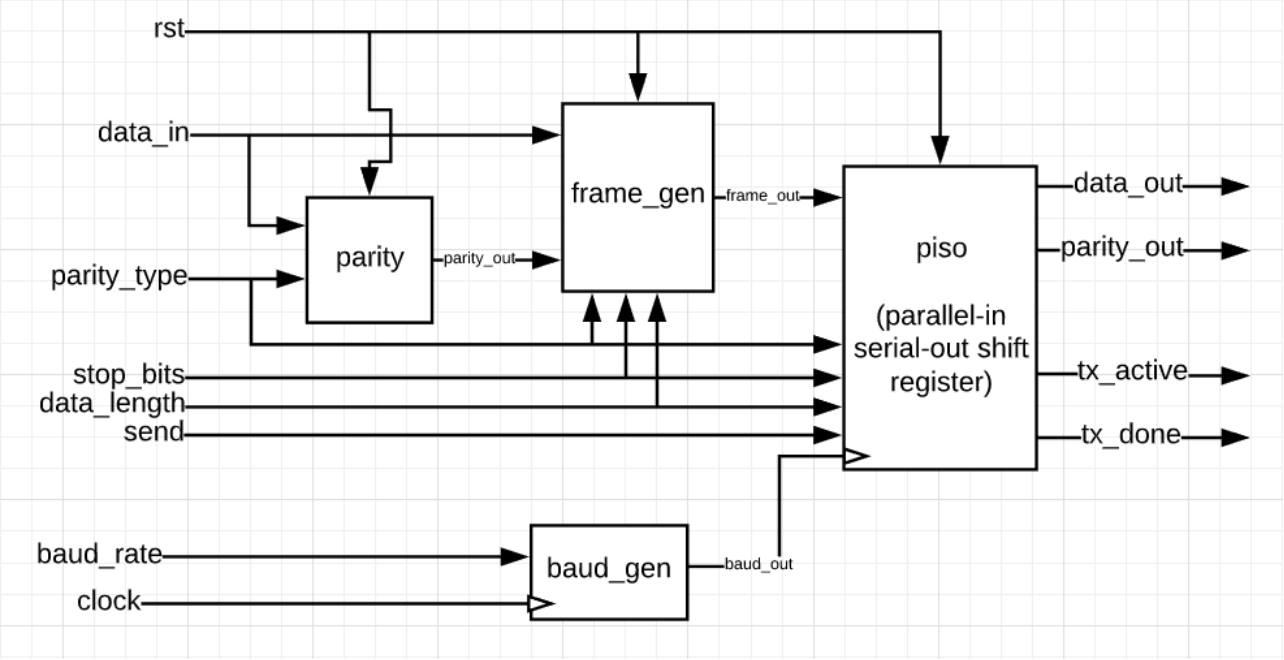


Figure 1: architecture for UART transmitter

every module has two files one for the design itself and one for testbench.

# 2 Top Module

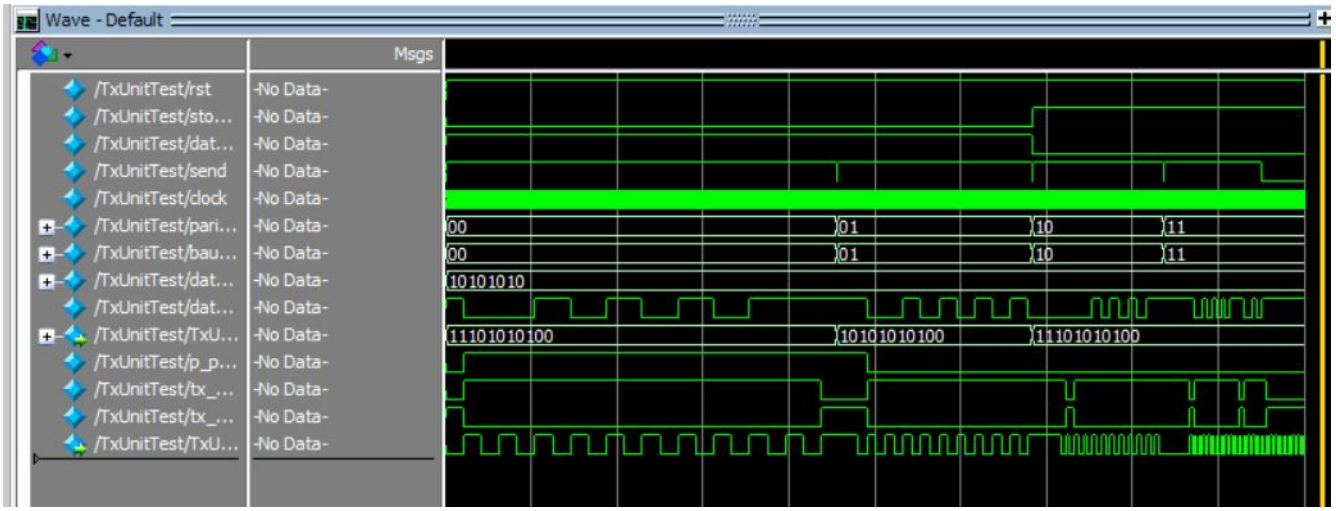


Figure 2: top module testing

# 3 PISO

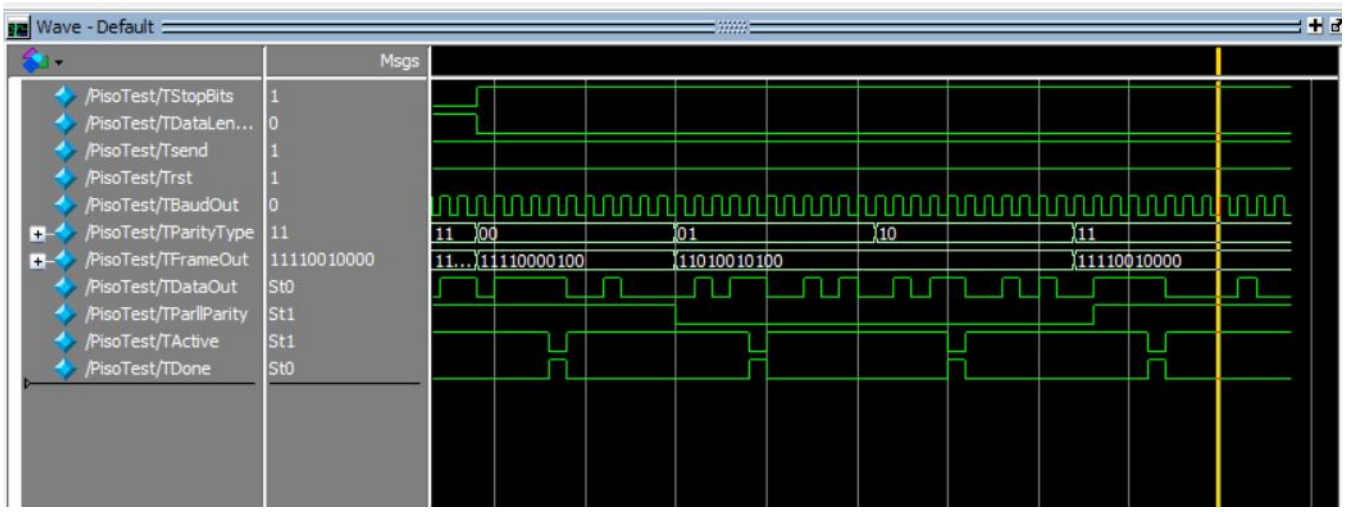


Figure 3: PISO testing

# 4 Baud Generator

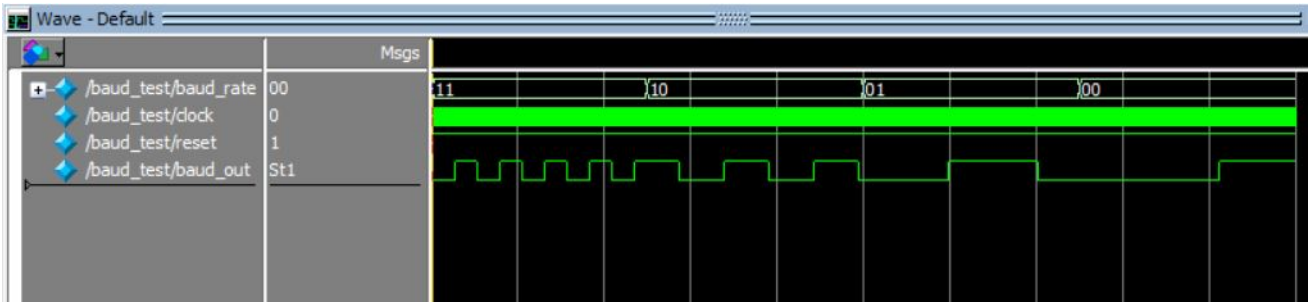


Figure 4: baud generator testing

# 5 Frame Generator

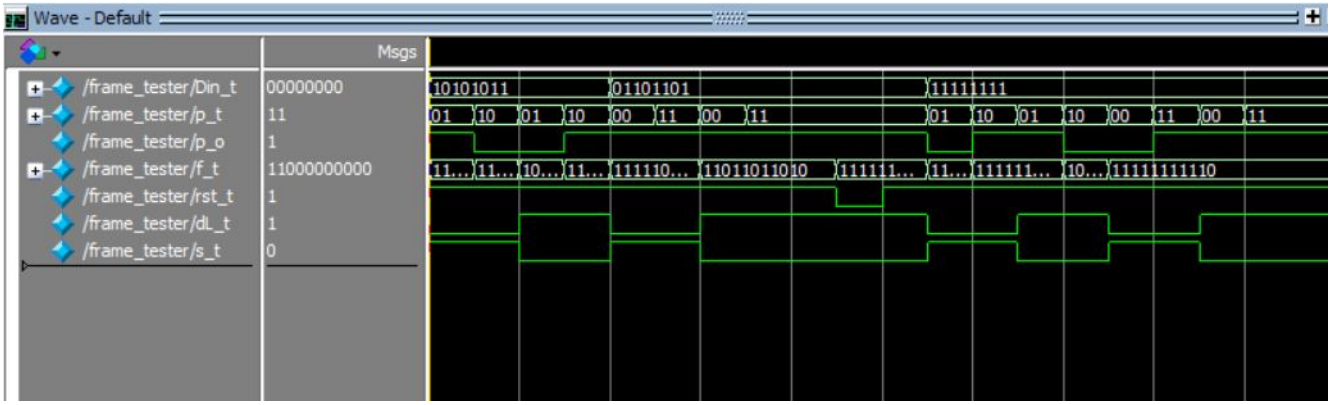


Figure 5: frame generator testing

# 6 Parity Generator

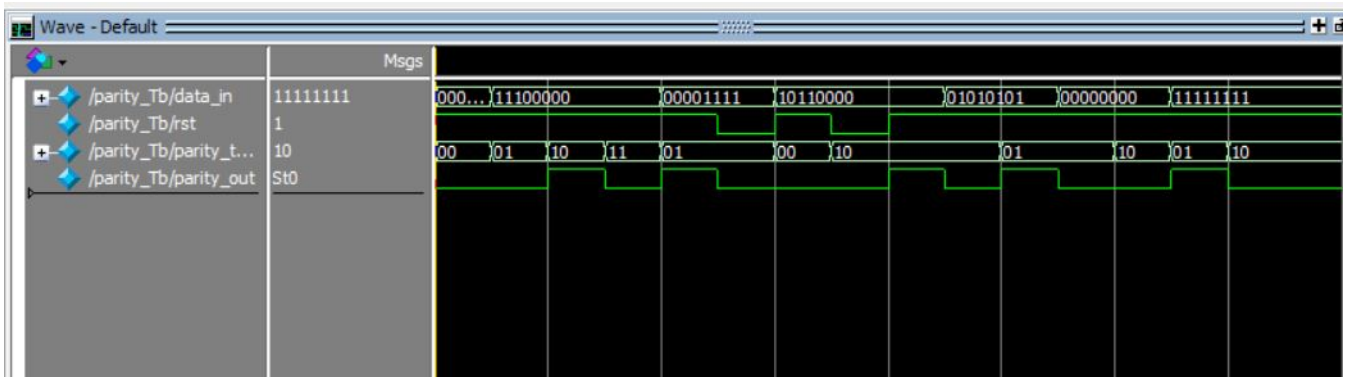


Figure 6: Parity Generator testing