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A Step-Up Switched-Capacitor Multilevel Inverter With Self-Voltage Balancing

Yuanmao Ye, K. W. E. Cheng, *Senior Member, IEEE*, Junfeng Liu, and Kai Ding

***Abstract*—The objective of this paper is to propose a new inverter topology for a multilevel voltage output. This topology is designed based on a switched capacitor (SC) technique, and the number of output levels is determined by the number of SC cells. Only one dc voltage source is needed, and the problem of capacitor voltage balancing is avoided as well. This structure is not only very simple and easy to be extended to a higher level, but also its gate driver circuits are simplified because the number of active switches is reduced. The operational principle of this inverter and the targeted modulation strategies are presented, and power losses are investigated. Finally, the performance of the proposed multilevel inverter is evaluated with the experimental results of an 11-level prototype inverter.**

***Index Terms*—H-bridge, multilevel inverter, selective harmonic elimination (SHE), sinusoidal pulsewidth modulation (SPWM), switched capacitor (SC).**

I. Introduction

With THE increasing higher power quality requirements for numerous industrial applications and renewable energy sources such as photovoltaic, wind, and fuel cells, classical three-level inverters have difficulty in meeting these requirements of clean nonpolluted sinusoidal waveforms and a minimal distortion factor. As a result, multilevel inverters have been introduced as an alternative in high power quality situations. For several attractive features, such as near-sinusoidal staircase output voltage waveforms, reduced dv/dt stress, operating with a lower switching frequency stress, etc. [1], multilevel inverters, as an alternative solution, have been receiving much attention. As a result, many different topologies and a wide variety of control strategies have been proposed [2].

Conventionally, multilevel inverter topologies can be divided into three categories, i.e., neutral-point-clamped inverters [3], flying capacitors [4], and the H-bridge cascade [5]–[9]. In many industrial applications, these inverters have been playing very important roles in terms of high-quality ac supplies and motor drivers because of their good performance [10], [11]. However, their drawbacks are also apparent. For instance, multiple separated voltage sources are required for the H-bridge cascade topology [2], [6]–[9]. In addition, the problem of voltage balancing among dc-link series capacitors exists in both neutral-point-clamped and capacitor-clamped inverters [12]–[14].

In recent years, numerous new multilevel inverter topologies that cannot be attributed to the traditional three classifications aforementioned have been reported in [2] and [15]–[21]. Specifically, multiple submultilevel converter units and full-bridge converters are employed in the new multilevel inverter topology [15]. In [16], a simple topology is proposed, but multiple separated dc voltage sources are still required. The coupled-inductor technique used in multilevel inverters was introduced in [2] and [17]. The structures are simplified, but it is difficult to expand this technique to higher level applications. In [18], [20], and [21], novel topologies based on switched capacitor (SC) [22] and boost techniques were presented, but their numbers of output voltage levels are limited at 13, 7, and 5, respectively. In contrast, the multilevel topology introduced in [19] can be extended to higher levels. However, the use of a large number of active switches increases the cost and component counts in terms of gate driver circuits and the overall system.

Based on the SC technique that has been applied in many applications [23], a novel multilevel inverter topology connecting a multilevel dc–dc converter and a full bridge is presented in this paper. With the proposed topology, only one dc voltage source is required, and many other problems, such as voltage balancing, numerous active switches, and complex gate driver circuits, are avoided. The dc–dc conversion section is the key point of the whole topology, which is designed by connecting multiple SC cells. Each SC cell consists of a capacitor, an active switch, and two diodes. Consequently, the output voltage levels of the proposed inverter could be flexibly varied by employing different numbers of SC cells.

II. Circuit Description and State Analysis

The proposed multilevel inverter is cascaded by a dc–dc multilevel converter and a full bridge, as shown in Fig. 1. For its dc–dc converter section that consists of the number of n SC cells, it is capable of providing the number of $n+1$ voltage levels according to different switching states. With the operation of the H-bridge, a total of $2n+3$ voltage levels can be produced, i.e., $0, \pm V_{\rm in}, \pm 2V_{\rm in}, \ldots, \pm(n+1)V_{\rm in}$. Without

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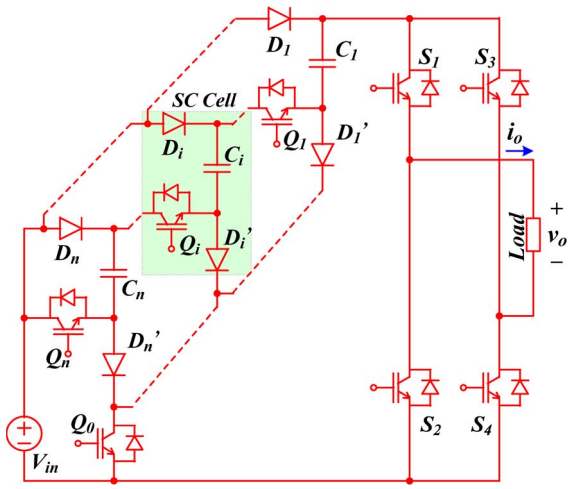


Fig. 1. Topology of the proposed multilevel inverter.

loss of generality, the following assumptions have been made for analysis.

1) The values of all SCs C_i are large enough, and the voltage ripples across them are negligible.
2) All the switching devices are ideal, i.e., no ON-state voltage drop and on-resistance.
3) Input power source $V_{\rm in}$ is ideal, i.e., it is constant and there is no series impedance.

A. Zero-Level Output

When switch Q_0 is turned ON while $Q_i (i = 1, 2, \ldots, n)$ is OFF, all SCs C_i are charged by input power source $V_{\rm in}$ through diodes D_i and D_i', as shown in Fig. 2(a). For the H-bridge, only switch S_1 is turned ON, whereas the others are OFF. There is no voltage developed for the load. The output voltage is therefore equal to zero. Output current i_O can be freewheeling through S_1 and the bypass diode of S_3 when the load is not pure resistance. There is also another zero level that can be produced by turning ON S_2 while the other switches are OFF.

B. Level of $\pm V_{\rm in}$ Output

For the dc–dc conversion section, its operating state is the same as that for the zero-level state aforementioned, i.e., Q_0 maintains the ON-state while the other switches are OFF. The voltages across capacitors C_i are eventually equal to input voltage $V_{\rm in}$, i.e., $V_{C_i} = V_{\rm in}$ $(i = 1, 2, \ldots, n)$. For the H-bridge, switches S_1 and S_4 are turned ON simultaneously, whereas S_2 and S_3 maintain the OFF-state. Voltage $V_{\rm in}$ is developed by the input power directly to the load, as shown in Fig. 2(b). Similarly, the level of $-V_{\rm in}$ can be developed by turning ON switches S_2 and S_3, whereas S_1 and S_4 are OFF.

C. Level of $\pm i \times V_{\rm in}$ Output

When switch Q_0 is turned OFF, voltage level $i \times V_{\rm in}$ can be developed in the dc–dc conversion section by turning ON switches Q_1–Q_{i-1} $(i = 2, 3, \ldots, n)$, whereas Q_i–Q_n are OFF. In this case, capacitors C_1–C_{i-1} are connected in series with input source $V_{\rm in}$, and the total voltage level, i.e., $V_{\rm in} + V_{C_1} + \cdots + V_{C_i-1}$, is produced. Based on the aforementioned assumption, the voltages across all capacitors are the same as input voltage $V_{\rm in}$. This total voltage level is therefore equal to $i \times V_{\rm in}$. With the operation of the full bridge, this voltage level can be developed to the load by turning ON S_1 and S_4, whereas S_2 and S_3 are OFF, as shown in Fig. 2(c). The level of $-i \times V_{\rm in}$ can be also provided to the load by controlling the full bridge in a reverse manner. In particular, when $i = n$, the output level is equal to $\pm nV_{\rm in}$, as shown in Fig. 2(d).

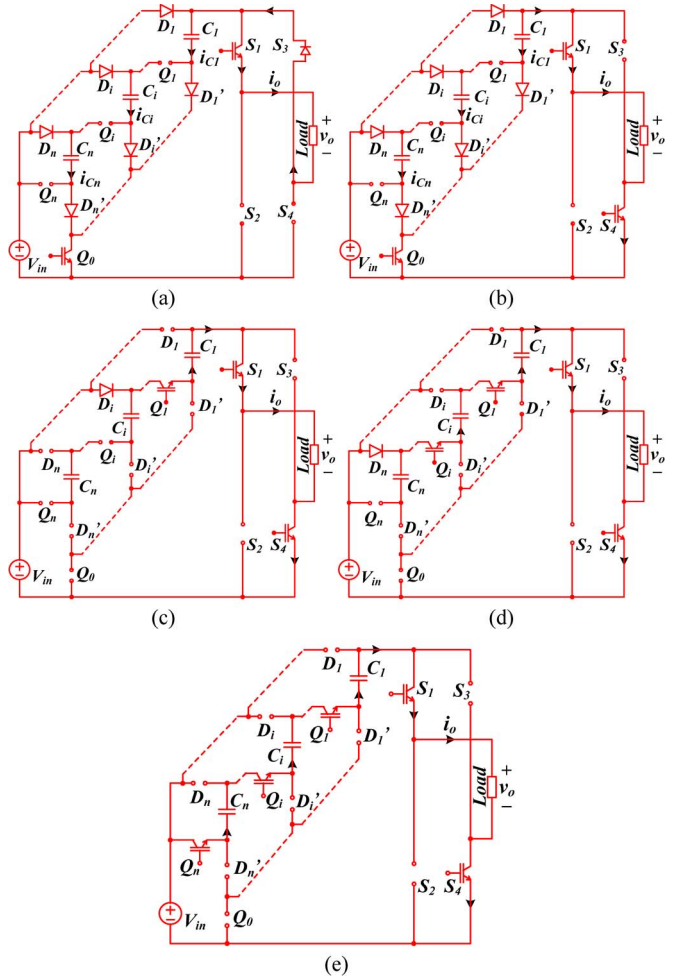


Fig. 2. Working states for the proposed inverter. (a) Zero-level output. (b) Level of the $V_{\rm in}$ output. (c) Level of the $i \times V_{\rm in}$ output. (d) Level of the $nV_{\rm in}$ output. (e) Level of the $(n+1)V_{\rm in}$ output.

D. Level of $\pm(n+1)V_{\rm in}$ Output

For the dc–dc section, the highest voltage level $(n+1)V_{\rm in}$ can be obtained by connecting all capacitors C_i in series with input $V_{\rm in}$ when switches Q_1–Q_n are all turned ON, whereas Q_0 maintains the OFF-state, as shown in Fig. 2(e). Based on the aforementioned analysis, the positive and negative levels, i.e., $\pm(n+1)V_{\rm in}$, can be generated by turning ON S_1 and S_4 or S_2 and S_3.

Based on the aforementioned analysis, the combinations of the working states of the proposed multilevel inverter can be concluded, as shown in Table I. It is shown that there are $2n + 4$

TABLE I
COMBINATION OF THE WORKING STATES FOR THE PROPOSED INVERTER

No. of states	Switching states										Output levels
	Q_0~Q_n						S_1~S_4				
1	0	1	1	1	1	1	1	0	0	1	$+(n+1)V_{in}$
2	0	1	1	1	1	0	1	0	0	1	$+n\times V_{in}$
⋮	0	1	1	1	…	0	1	0	0	1	⋮
n-i+1	0	1	1	1	0	0	1	0	0	1	$+(i+1)V_{in}$
n-i+2	0	1	1	0	0	0	1	0	0	1	$+i\times V_{in}$
⋮	0	1	…	0	0	0	1	0	0	1	⋮
n	0	1	0	0	0	0	1	0	0	1	$+2V_{in}$
n+1	1	0	0	0	0	0	1	0	0	1	$+V_{in}$
n+2	1	0	0	0	0	0	1	0	0	0	0
n+3	1	0	0	0	0	0	0	1	0	0	
n+4	1	0	0	0	0	0	0	1	1	0	$-V_{in}$
n+5	0	1	0	0	0	0	0	1	1	0	$-2V_{in}$
⋮	0	1	…	0	0	0	0	1	1	0	⋮
n+i+3	0	1	1	0	0	0	0	1	1	0	$-i\times V_{in}$
n+i+4	0	1	1	1	0	0	0	1	1	0	$-(i+1)V_{in}$
⋮	0	1	1	1	…	0	0	1	1	0	⋮
$2n$+3	0	1	1	1	1	0	0	1	1	0	$-n\times V_{in}$
$2n$+4	0	1	1	1	1	1	0	1	1	0	$-(n+1)V_{in}$

working states corresponding to $2n+3$ different output voltage levels, including two zero-level states. Consequently, controlled by appropriate modulation strategies, the proposed topology could operate as a $(2n+3)$-level inverter. When the inverter alternatively operates in two adjacent states, there are only one or two switch states that need to be changed. In addition, the numbers of capacitors and active switches required in the inverter are n and $n+5$, respectively.

III. MODULATION STRATEGIES

A variety of modulation strategies have been used in multilevel inverters to synthesize the output voltage as close as possible to the sinusoidal waveform. These modulation methods can be classified into two main categories according to the switching frequency [1], i.e., the high-frequency modulation (HFM) and the fundamental frequency modulation (FFM).

A. HFM for the Proposed Inverter

For the HFM methods, there are many commutations for the power switches in one period of the fundamental output voltage. The HFM can be further divided into several specific modulation methods, of which a very popular method is the multilevel carrier-based sinusoidal pulsewidth modulation (SPWM) [24], [25]. Therefore, this method will be introduced to control the proposed inverter and is discussed as follows.

For the proposed $(2n+3)$-level inverter, $2n+2$ triangular carriers are needed. The carriers have the same peak-to-peak amplitude A_C and the same frequency f_C. The modulating signal is a sinusoidal waveform with frequency f_S and amplitude A_S. During each period of the fundamental cycle, each carrier is compared with the modulating signal, and the results of the comparison are used to control the corresponding active switches, as shown in Fig. 3, in which

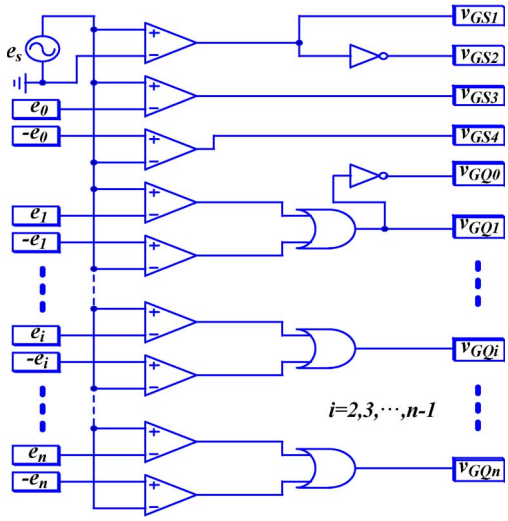


Fig. 3. Multicarrier logic modulating circuit for the proposed inverter.

$\pm e_0, \pm e_1, \ldots, \pm e_i, \ldots, \pm e_n$ are carriers, and e_s is the modulating signal. All of them can be mathematically described as

$$e_S = A_S \sin(2\pi f_S t) \tag{1}$$

$$e_0 = \begin{cases} 2A_C f_C \left(t - \frac{k-1}{f_C}\right), & \frac{k-1}{f_C} < t \le \frac{2k-1}{2f_C} \\ A_C \left[1 - 2f_C \left(t - \frac{2k-1}{2f_C}\right)\right], & \frac{2k-1}{2f_C} < t \le \frac{k}{f_C} \end{cases} \tag{2}$$

$$\begin{cases} e_i = i * A_C + e_0 \\ i = 1, 2, \ldots, n \end{cases} \tag{3}$$

where k is the number of triangle waves. It is a natural number and ranged from 1 to infinity.

Amplitude modulation index M_a and frequency ratio M_f are therefore defined, respectively, as

$$M_a = \frac{A_S}{(n+1)A_C} \tag{4}$$

$$M_f = \frac{f_C}{f_S}. \tag{5}$$

B. FFM for the Proposed Inverter

For the FFM methods, a staircase voltage waveform is generated by connecting different numbers of capacitor sources to the output terminal and with only one or two commutations of active switches during one cycle of the fundamental output voltage. A representative of this family is the selective harmonic elimination (SHE) method [26]. It was also introduced to modulate the proposed inverter to output a staircase voltage.

For a staircase waveform with z steps, its Fourier transform can be expressed as

$$v(\omega t) = \frac{4V_{\text{in}}}{\pi} \sum_k \left[\cos(k\theta_1) + \cos(k\theta_2) + \cdots + \cos(k\theta_Z)\right] \times \frac{\sin(k\omega t)}{k} \tag{6}$$

where $k = 1, 3, 5, 7, \ldots$ are odd numbers. θ_1, θ_2 to θ_Z are the conducting angles for each step of the staircase waveform.

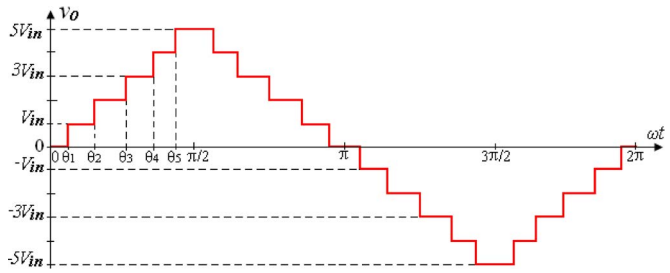


Fig. 4. Eleven-level staircase waveform.

The fundamental content and its maximum attainable amplitude can be therefore derived as

$$v_1(\omega t) = \frac{4V_{\text{in}}}{\pi}\left[\cos(\theta_1) + \cos(\theta_2) + \cdots + \cos(\theta_Z)\right]\sin(\omega t) \tag{7}$$

$$V_{1\_\max} = \frac{4z}{\pi}V_{\text{in}}. \tag{8}$$

The main idea of the SHE method is to choose the appropriate conduction angles θ_1–θ_Z to make the Fourier coefficients of the selected harmonics equal to zero, i.e.,

$$\cos(m\theta_1) + \cos(m\theta_2) + \cdots + \cos(m\theta_Z) = 0 \tag{9}$$

where m is the number of the selected harmonics.

Taking into account amplitude modulation index M_a', which is defined as $V_1^*/V_{1\_\max}$, where V_1^* is the desired amplitude of the output voltage and is determined by the values of conducting angles θ_1, θ_2 to θ_Z, there are $z-1$ high harmonics that could be chosen to be eliminated, i.e., m has $z-1$ different values. Taking the 11-level staircase waveform as an example, as shown in Fig. 4, there are five steps. The 5th, 7th, 11th, and 13th harmonics can be chosen to be eliminated, and the values of the conducting angles can be decided by

$$\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)+\cos(\theta_4)+\cos(\theta_5)=5M_a' \tag{10}$$

$$\begin{cases} \cos(5\theta_1)+\cos(5\theta_2)+\cos(5\theta_3)+\cos(5\theta_4)+\cos(5\theta_5)=0 \\ \cos(7\theta_1)+\cos(7\theta_2)+\cos(7\theta_3)+\cos(7\theta_4)+\cos(7\theta_5)=0 \\ \cos(11\theta_1)+\cos(11\theta_2)+\cos(11\theta_3)+\cos(11\theta_4)+\cos(11\theta_5)=0 \\ \cos(13\theta_1)+\cos(13\theta_2)+\cos(13\theta_3)+\cos(13\theta_4)+\cos(13\theta_5)=0. \end{cases} \tag{11}$$

For different values of amplitude modulation index M_a', there are different combinations of values for conducting angles θ_1, θ_2 to θ_Z.

The SHE method can be also implemented by using multiple carriers $\pm e_0$, $\pm e_1, \ldots, \pm e_{z-1}$ and a sinusoidal modulating signal e_S. In particular, the carriers are no longer triangular signals but multiple constant dc signals with different levels. Their levels can be calculated by the sinusoidal modulating signal and conducting angles θ_1, θ_2 to θ_Z. The specific relationships are given as

$$\begin{cases} e_{i-1} = A_S \sin\theta_i \\ i = 1, 2, \ldots, z \end{cases} \tag{12}$$

where A_S is the amplitude of the modulating signal.

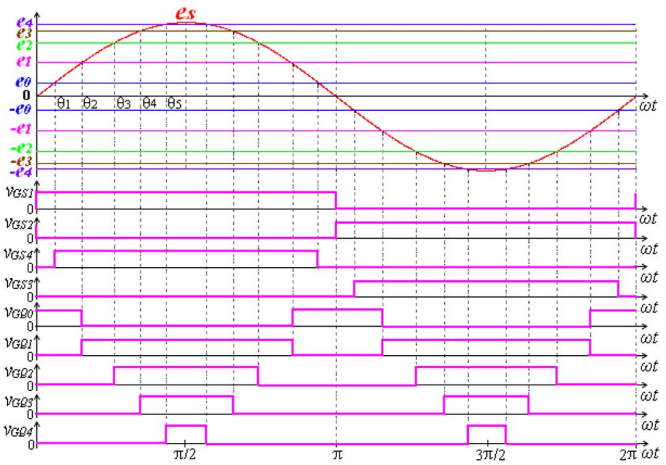


Fig. 5. Idealized modulation waveforms of the SHE modulation logic circuit.

In this case, the SHE modulation circuit of the proposed inverter is the same as that used for the SPWM method, as shown in Fig. 3. In addition, the idealized modulation waveforms are shown in Fig. 5.

With the same modulation logic circuit, it means that the proposed inverter can operate at both the high switching frequency mode with the PWM output voltage waveform and the fundamental switching frequency mode with the staircase output voltage waveform. The only difference is that the carriers are high-frequency triangular signals or constant dc signals.

IV. Voltage Ripples and Power Loss Analysis

A. Voltage Ripples of Capacitors

For the SCs in the proposed inverter, they provide voltage and current to the load simultaneously. Their voltage levels are mainly determined by input voltage V_{in} and is basically equal to V_{in}. However, they are also influenced by output current i_O, and the voltage ripples across the capacitors are unavoidable. For different capacitors, the voltage ripples are different because the discharging periods are not the same and the output current varies along with time.

In detail, the discharging period of capacitor C_i $(i = 1, 2, \ldots, n)$ starts when switch Q_i is turned ON and ends when Q_i is turned OFF. The voltage ripple ΔV_i across the capacitor can be therefore expressed as

$$\Delta V_i = \frac{1}{C_i}\int_{t_{i\_1}}^{t_{i\_2}} i_O dt \tag{13}$$

where t_{i_1} and t_{i_2} are the start and end times of the discharging duration, respectively. Their values are not the same for the different modulation strategies.

For the SHE method, in each half-period of the fundamental frequency, the discharging period of capacitors C_i is from θ_{i+1} to $\pi - \theta_{i+1}$, where θ_{i+1} is the conducting angle of switch Q_i. The voltage ripple can be therefore further expressed as

$$\Delta V_i' = \frac{1}{2\pi f_S C_i}\int_{\theta_{i+1}}^{\pi-\theta_{i+1}} i_O d(\omega t) \tag{14}$$

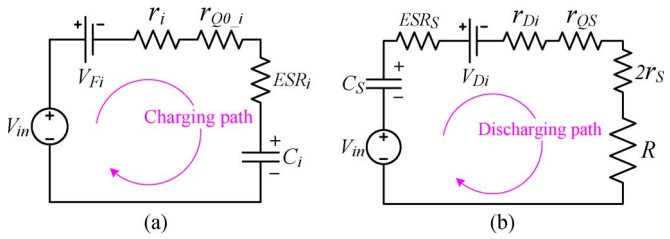


Fig. 6. (a) Equivalent charging circuit and (b) discharging circuit for the proposed inverter.

where f_S is the fundamental frequency, and ω is the corresponding angular frequency. For the pure resistance load, the output current is also a staircase waveform, and charge amount ΔQ_i flowing out capacitors C_i during the discharging period can be therefore approximately calculated by

$$\Delta Q_i \approx \frac{V_{\text{in}}}{2\pi f_S R}\sum_{a=i}^{n}(\pi - 2\theta_{a+1})(a+1) \tag{15}$$

where R is the value of the pure resistance load. The voltage ripple can be therefore further derived as

$$\Delta V_i'' \approx \frac{V_{\text{in}}}{2\pi f_S R C_i}\sum_{a=i}^{n}(\pi - 2\theta_{a+1})(a+1). \tag{16}$$

It is shown in both (13) and (14) that the voltage ripple is inversely proportional to the capacitance and proportional to the output current. It means that the larger the switched capacitance, the stronger the load capacity is. Practically, the values of the capacitors should be determined by the design requirements of the maximum output current and the minimum voltage ripples.

B. Conduction Loss Analysis

When switch Q_0 is turned ON, capacitor C_i is charged by V_{in} through D_i and D_i', as shown in Fig. 6(a), where V_{Fi} and r_i are the forward voltage drop and internal resistance of pair diodes D_i and D_i', i.e., $V_{Fi} = V_{D_i} + V_{D_i'}$, and $r_i = r_{D_i} + r_{D_i'}$; $r_{Q_{0\_i}}$ is the equivalent resistance of the ON-resistance of Q_0 for this charging path; and ESR_i is the equivalent series resistance of C_i. There are n similar charging paths operated in a parallel manner, and they share the common switch Q_0 and power source V_{in}. Equivalent resistance $r_{Q_{0\_i}}$, therefore, can be approximately equal to $n \times r_{Q_0}$. The maximum current flowing through the diodes and the charging switch Q_0 can be therefore expressed as

$$\begin{cases} I_{D_{i\_\max}} = I_{D_{i\_\max}'} = \dfrac{\Delta V_{C_i}}{r_i + nr_{Q_0} + \text{ESR}_i} \\ I_{Q_{0\_\max}} = \displaystyle\sum_{i=1}^{n} \dfrac{\Delta V_{C_i}}{r_i + nr_{Q_0} + \text{ESR}_i}. \end{cases} \tag{17}$$

The energy profile for each SC cell over one charging cycle can be expressed as

$$\begin{cases} E_{\text{in(C_i)}} = C_i V_{\text{in}} \Delta V_i \\ E_{C_i} = C_i(V_{\text{in}} - V_{Fi})\Delta V_i - \frac{1}{2}C_i \Delta V_i^2 \\ \Delta E_{C_i} = E_{\text{in}(C_i)} - E_{C_i}. \end{cases} \tag{18}$$

The total conduction losses of all SC cells caused in the charging processes can be therefore derived as

$$P_{\text{loss\_chr}} = \frac{f_{Q_0}}{2}\sum_{i=1}^{n} C_i(2V_{Fi} + \Delta V_i)\Delta V_i \tag{19}$$

where f_{Q_0} is the switching frequency of switch Q_0. It is double fundamental frequency f_S for the SHE modulation method, i.e., $f_{Q_0} = 2f_S$. It could be seen that the larger voltage ripple will cause more power losses in the charging duration. According to (13), however, the lower voltage ripple can be produced by employing larger SCs and, then, results in less power losses.

During the discharging process, in different states, varied numbers of capacitors are connected in series with V_{in} to provide the different voltage levels to load R, as shown in Fig. 6(b), where C_S is the equivalent capacitance of the discharging path, and ESR_S is its equivalent series resistance. Only one diode D_i with voltage drop V_{D_i} and internal resistance r_{D_i} appears in the discharging loop. r_{QS} is the ON-resistance of all switches Q_i connected in the path, which is varied from 0 to $r_{Q_1} + r_{Q_2} + \cdots + r_{Q_n}$ corresponding to the output voltage varied from $\pm V_{\text{in}}$ to $\pm(n+1)V_{\text{in}}$. r_S is the ON-resistance of each switch for the H-bridge. The instantaneous conduction loss of the discharging loop is expressed as

$$P_{\text{loss\_disr}} = (\text{ESR}_S + r_{D_i} + 2r_S + r_{QS}) \times \left(\frac{V_{\text{in}} + V_{Cs} - V_{D_i}}{R + \text{ESR}_S + r_{D_i} + 2r_S + r_{QS}}\right)^2. \tag{20}$$

For the SHE modulation method, the average conduction loss of the discharging path can be approximately calculated by

$$P_{\text{loss\_disr}}' \approx \frac{2f_S}{\pi}\sum_{i=1}^{n+1}(\theta_{i+1} - \theta_i)(2r_S + r_{D_i} + \text{ESR}_{S_i} + r_{QS_i}) \times \left(\frac{i * V_{\text{in}} - V_{D_i}}{R + 2r_S + r_{D_i} + \text{ESR}_{S_i} + r_{QS_i}}\right)^2 \tag{21}$$

where $\text{ESR}_{S_1} = 0$, and $\text{ESR}_{S_i} = \sum_{k=1}^{i-1}\text{ESR}_k$; $r_{QS_1} = 0$, and $r_{QS_i} = \sum_{k=1}^{i-1} r_{Q_k}$; and $r_{D(n+1)} = 0$, $V_{D(n+1)} = 0$, and $\theta_{n+2} = \pi/2$.

It could be seen from the aforementioned analysis that, in order to reduce the power loss caused in the discharging process, the power switches with smaller ON-resistance, the diodes with a lower voltage drop, and the capacitors with smaller ESR are our priority to be worked on.

C. Switching Losses and Switch Stress Analysis

The switching losses can be calculated by considering the charging and discharging processes of the output capacitance of switches [27]. When the transistor is turned OFF, parasitic capacitor C_T is charged, and its voltage increases from nearly zero to V_T, which is subject to the maximum voltage stress of the transistor. Then, the transistor is turned ON, and the output capacitor is shorted out. Its voltage falls back to nearly zero. Considering the whole switching cycle, if the voltage stress does not oscillate but may be varied during the OFF-state, the

TABLE II
COMPARISON OF THE PROPOSED TOPOLOGY WITH THE INVERTERS SUGGESTED IN [15] AND [19] FOR THE $(2n+3)$-LEVEL OUTPUT

Comparing items	Fig. 1 in [19]	Fig. 4 in [15]	Proposed
Capacitors	***n***	***n+1***	***n***
Balancing circuits	***No need***	***Need***	***No need***
Active switches	***3n+4***	***2(n+1)+4***	***n+5***
Diodes	***0***	***0***	***2n***
H-bridge's stress	***(n+1)V_C***	***(n+1)V_C***	***(n+1)V_C***

switching power loss of the transistor during one switching cycle can be expressed as

$$E_{T\_\text{loss}} = C_T V_T^2 \tag{22}$$

which results in the switching power loss in the transistor, i.e.,

$$P_{T\_\text{loss}} = f_T C_T V_T^2 \tag{23}$$

where f_T is the switching frequency of the transistor.

For the proposed inverter with the SHE modulation, the switching frequency is the same as fundamental frequency f_S for each transistor S_i in the H-bridge and $2f_S$ for other switches Q_0–Q_n. Ignoring the voltage ripple across SC C_i, the maximum voltage stresses are $(n+1)V_{\text{in}}$ for the OFF-transistors S_1–S_4, nV_{in} for Q_0, and V_{in} for Q_i $(i = 1, 2, \ldots, n)$. The total switching losses of the proposed inverter can be therefore calculated by

$$P_{\text{loss\_sw}} = f_S V_{\text{in}}^2 \left[2n^2 C_{Q_0} + 2\sum_{i=1}^{n} C_{Q_i} + (n+1)^2 \sum_{j=1}^{4} C_{S_j} \right] \tag{24}$$

where C_{Q_0}, C_{Q_i}, and C_{S_j} are the output capacitance values of transistors Q_0, Q_i, and S_j, respectively.

Additionally, all OFF-diodes D_i and D_i' suffer from the maximum voltage stress when all transistors Q_i are turned ON. Similarly, ignoring the voltage ripple across SC C_i, the values of the $(n-i+1)V_{\text{in}}$ and $(i-1)V_{\text{in}}$ voltage stresses are developed across diodes D_i and D_i', respectively.

V. COMPARISON OF THE PROPOSED TOPOLOGY WITH TOPOLOGIES SUGGESTED IN [15] AND [18]–[21]

To compare the proposed topology with the topologies suggested in [15] and [19], the main circuit characteristics of the three topologies with the same number of output levels $2n+3$ are concluded in Table II. It shows that the number of capacitors required in the inverter in [15, Fig. 4] is more than that of the two other topologies. In addition, the auxiliary circuits need to be added to solve the problem of voltage unbalance. In contrast, the capacitor voltages in the inverter in [19, Fig. 1] and the proposed inverter are both automatically balanced during the charging process. For the number of switches, no diode is employed in the two existing topologies in [15] and [19], but the number of $2n$ diodes is required in the proposed inverter. However, the least active switches and gate driver circuits are needed in the proposed inverter. Additionally, the three compared inverters are all simply developed by a cascade of a multilevel dc–dc converter and an H-bridge. The switch stresses for the four transistors of the bridge in the three topologies are all the same as the maximum voltage level provided by their dc conversion sections.

TABLE III
SPECIFICATION AND COMPONENTS OF THE 11-LEVEL INVERTER

Input Voltage (V_{in})	36VDC
Output Voltage Frequency	400 Hz
C_1, C_2, C_3, C_4 (Electrolytic Capacitor)	4700μF
Q_1,Q_2, Q_3, Q_4 (N-channel MOSFET)	IRFI540N
S_1,S_2, S_3, S_4 (N-channel MOSFET)	FDPF33N25T
Q_0 (N-channel MOSFET)	IRFB4227PBF
D_1, D_2, D_3, D_4 (Schottky Diode)	MBR20150CT
D_1', D_2', D_3', D_4' (Schottky Diode)	MBR20150CT
Rated Power	300 W

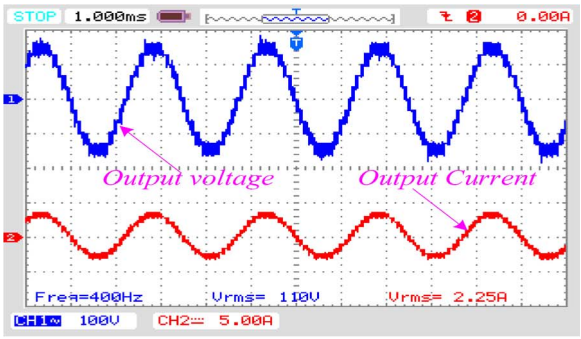
Similar to the topologies presented in [18], [20], and [21], the capacity of the proposed inverter with an inductive load is limited. Specifically, in [18], [20], and [21], the phase difference Φ between output voltage v_O and output current i_O cannot be larger than θ_1, i.e., $\Phi < \theta_1$, where the definition of θ_1 is the same as that in Fig. 4. This is because voltage levels $\pm V_C$ is provided to the output terminal through the diodes and there is no freewheeling circuit. In the proposed inverter, output voltage levels $\pm V_{\text{in}}$ is also provided through diode D_1. However, there is a freewheeling circuit $C_1 - D_1' - Q_0$ existing. The phase difference Φ for the proposed inverter can be therefore larger than θ_1 but must be smaller than θ_2 because switch Q_0 is turned OFF when $\pm 2V_{\text{in}}$ output levels need to be provided. Hence, the proposed inverter is capable of operating with the inductive load, but the impedance angle Φ of the load cannot be larger than θ_2.

VI. EXPERIMENTAL RESULTS

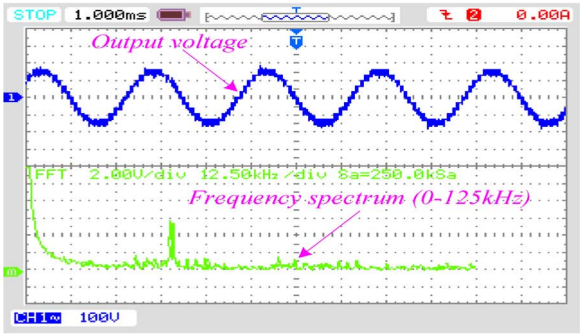
In order to verify the feasibility of the proposed multilevel inverter topology and evaluate its performance with the corresponding modulation methods, the proposed 11-level multilevel inverter prototype is built. In addition, the design parameters are listed in Table III. Verification tests, including the HFM test, the FFM test, and the test for different output frequencies, are implemented on the prototype. The results are analyzed as follows.

A. Results for HFM

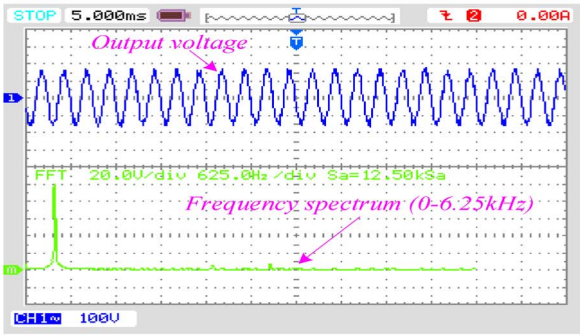
There are eight triangular carriers with a frequency of 40 kHz and one sinusoidal modulating signal with a frequency of 400 Hz used to control the prototype circuit. The modulation logic is shown in Fig. 4. When the load is a pure resistor with a value of 48 Ω and amplitude modulation index M_a is set to 0.95 according to (4), the output voltage and current are shown in Fig. 7(a). The frequency is 400 Hz, which is the same as the frequency of the modulating signal. The RMS of the output voltage is 110 V, which is lower than the mathematical value of 121 V. This is mainly caused by the voltage drop of the switching devices and the power losses caused in the charging and discharging processes. The measured efficiency is 89.2%. In addition, the fast-Fourier-transform-analyzed results are given in Fig. 7(b) and (c). It is shown in Fig. 7(b) that the higher harmonics are mainly concentrated in a switching



(a)

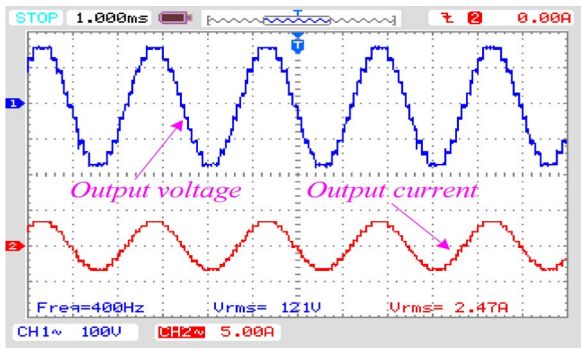


(b)

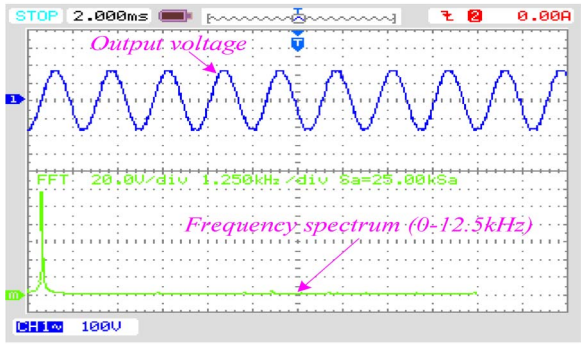


(c)

Fig. 7. Experimental results of HFM for the 11-level inverter. (a) Waveforms of the output voltage and current. (b) and (c) Frequency spectrum of the output voltage.



(a)



(b)

Fig. 8. Experimental results of HFM for the 11-level inverter. (a) Waveforms of the output voltage and current. (b) Frequency spectrum of the output voltage.

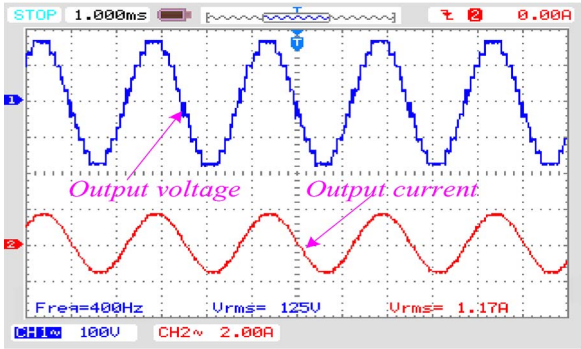


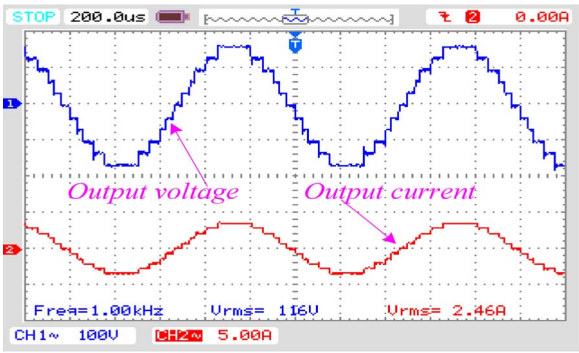
Fig. 9. Experimental results of HFM with an inductive load.

frequency of 40 kHz. The lower frequency spectrum is shown in Fig. 7(c). It depicts that there is a little amount of the seventh and ninth harmonics.

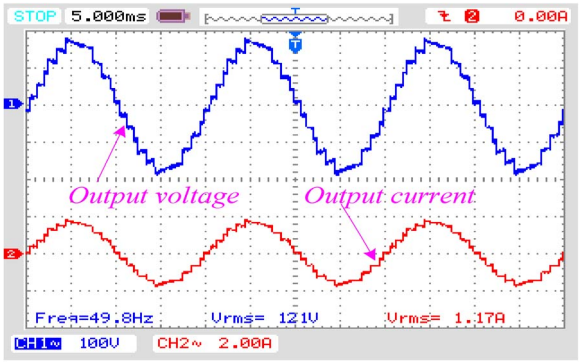
B. Results for FFM

With the same modulation logic and drive circuit that were used for the aforementioned HFM and the modulating signal still being a sinusoidal signal with a frequency of 400 Hz and amplitude A_S, the eight triangular carriers have been replaced by eight constant dc signals whose level is set according to (12), and the 11-level inverter prototype operates in the fundamental frequency switching mode and outputs a staircase voltage waveform. When the load is still a 48-Ω pure resistor and amplitude modulation index M_a' is set to 0.8, the output voltage and current waveforms are obtained, as shown in Fig. 8(a). The frequency is 400 Hz, which is also the same as desired. The RMS of the output voltage is 121 V, which is slightly lower than the mathematical value of 129.7 V, and the cause is the same as that in the aforementioned HFM. The measured efficiency is 91.6%. Although the waveforms are staircase rather than fully sinusoidal, the frequency spectrum for the output voltage waveform is very well, as shown in Fig. 8(b). It shows that only very small amounts of the 9th, 15th, and 17th harmonics appeared.

With the same test conditions but with the pure load replaced by a series-connected RL load ($R = 103\ \Omega$; $L = 10$ mH), the output voltage and current waveforms are shown in Fig. 9. The RMS of the output voltage is 125 V, and the measured efficiency is 92.9%. It is shown that the voltage waveform is basically the same as that for the pure resistance load, but the current is closer to the sinusoidal waveform but with a slight time delay. It indicates that the inverter prototype has good performance for the inductive load with a small impedance angle Φ.



(a)



(b)

Fig. 10. Experimental results of the 11-level inverter with fundamental frequencies of (a) 1 kHz and (b) 50 Hz.

C. Results for Different Output Frequencies

The output frequency varies with the modulating signal's frequency f_S. Fig. 10(a) and (b) shows the waveforms of the output voltage and current when the fundamental frequencies are set to be 1 kHz and 50 Hz, respectively. The load is a pure resistor with a value of 48 Ω for Fig. 10(a), whereas it is 103 Ω for Fig. 10(b). It is shown in Fig. 10 that the load capacity of the inverter declines along with the output frequency decreasing. Therefore, to meet the low-frequency and large output current applications with a reduced voltage ripple, the value of SCs should be larger. In other words, the proposed multilevel inverter topology is more suitable for high-frequency output voltage applications. The same conclusion can be also derived from (14).

Overall, although the satisfactory near-sinusoidal step-up output voltage waveforms with an extremely low distortion could be produced by the proposed inverter in both the HFM and FFM modes, the performance of the FFM mode, in terms of the frequency spectrum and the deviation of the measured output voltage and the mathematical value, is better than the HFM mode. In addition, the load capacity is related to its output voltage frequency. The higher the frequency, the better the load capacity is.

VII. Conclusion

In this paper, a step-up SC multilevel inverter, which is a combination of a multilevel dc–dc converter and a full bridge, has been proposed. The dc–dc conversion section consists of multiple SC cells. By connecting different numbers of SC cells, the output voltage level could be varied flexibly. It has been analyzed that the proposed inverter provides $2n + 3$ levels on the output voltage, using only n capacitors and $n + 5$ active switches. It enables the simple structure and low cost of the gate driver circuits. Meanwhile, the high switching frequency modulation and fundamental switching frequency modulation methods for the proposed inverter are discussed. Both of them could be implemented by using the multicarrier logic modulating circuit that is specifically designed for the proposed inverter. In addition, the voltage ripples across capacitors and power losses are analyzed in detail. Finally, the operation and performance of the proposed inverter are verified with experiments on an 11-level inverter prototype. Although good performance could be obtained in both the high switching frequency and fundamental switching frequency modes, it can be seen that the presented inverter is more suitable for the latter modulation method by comparing the experimental results. Experimental waveforms also indicate that the load capacity of the inverter declines with the decrease in the output frequency. Therefore, the proposed inverter is more suitable for high-frequency applications.

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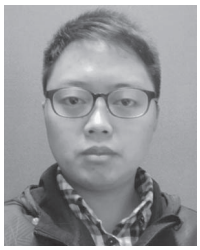

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