

NINE-LEVEL INVERTER BASED ON SWITCHED-CAPACITANCE STRUCTURE

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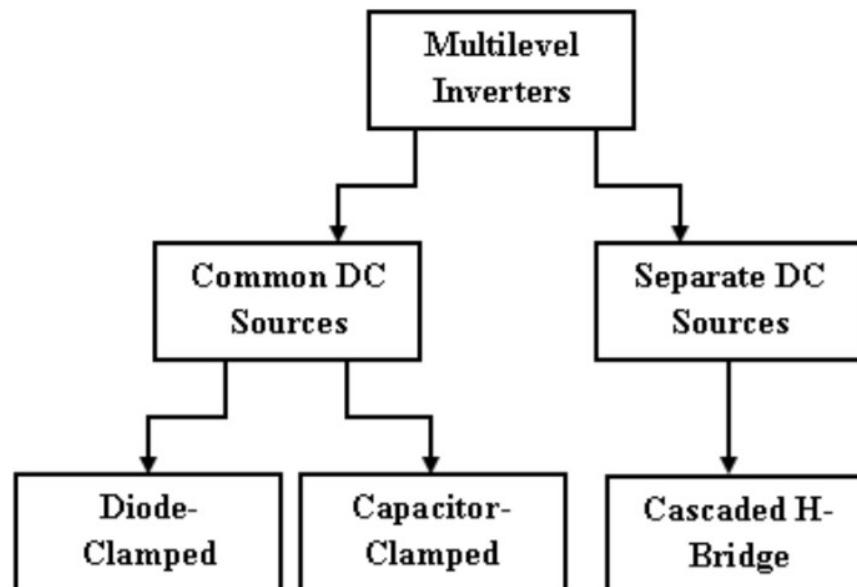
Introduction

- Recently, multilevel inverters (MIs) are getting more attention from researchers because of advantages like better waveform quality, lower EM noise, and lower device stress.
- MIs are used to couple a DC source to an AC bus for applications like electric motor drivers, uninterruptible power supplies, and distributed generation systems.

Literature Survey

The following topologies are now used in practice:-

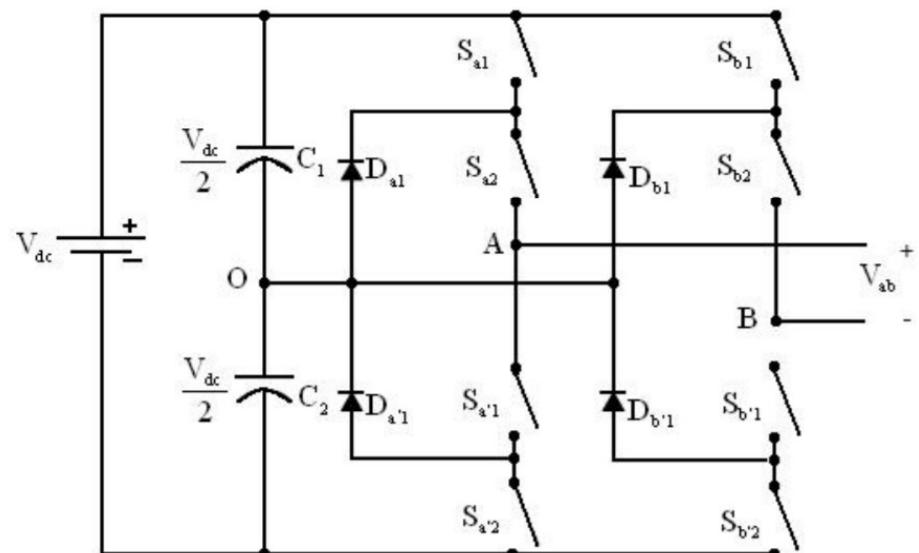
- Neutral-point clamped (Diode clamped)
- Flying capacitor
- Cascaded H-bridge (CHB)



Neutral-point clamped (Diode clamped)

DISADVANTAGES

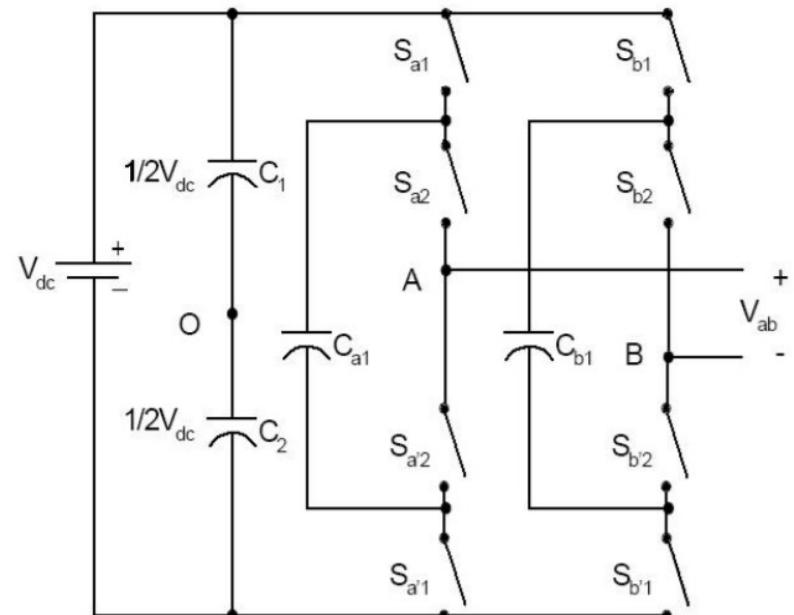
- Using extra diodes in series becomes impractical when the number of levels n increases
- The switch duty cycle is different for some of the switches requiring different current ratings
- Capacitors do not share the same discharge or charge current resulting in a voltage imbalance of the series capacitors.



Flying Capacitor MI

DISADVANTAGES

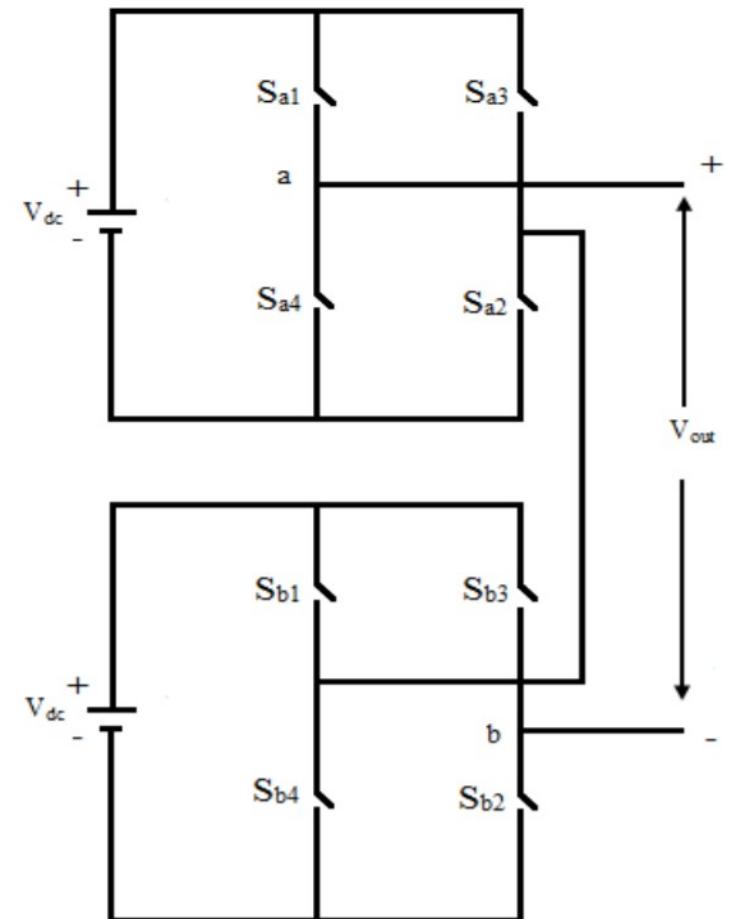
- Large numbers of capacitors are bulky and more expensive than the clamping diodes
- Complex control is required to maintain the capacitor's voltage balance.
- Switching utilization and Efficiency are poor for real power transmission.



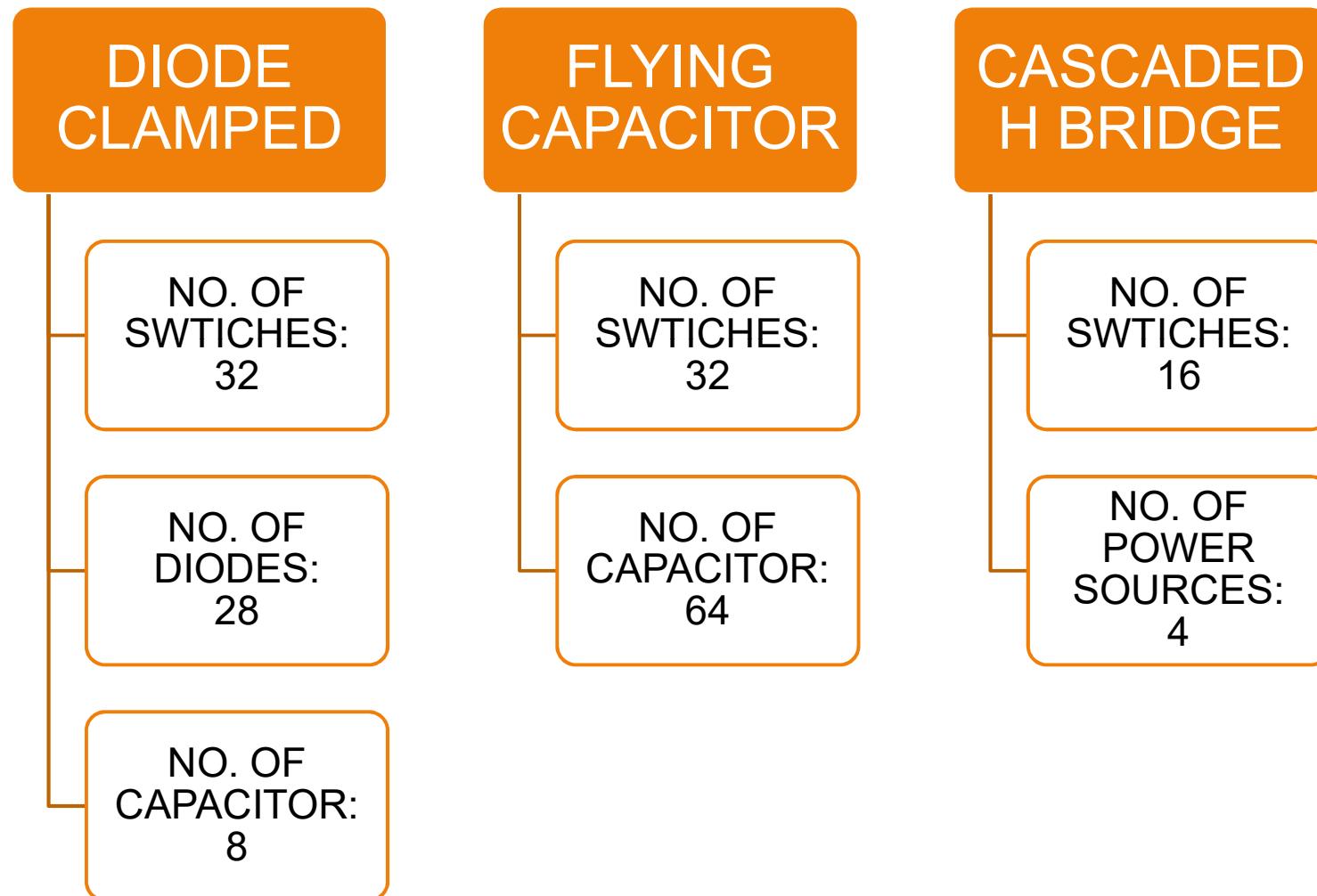
Cascaded H-Bridge MI

DISADVANTAGE

- Needs separate DC sources.



Components count for a nine level inverter



Summary of existing topologies

- Large number of components(switches, power supplies, capacitors, and diodes)
- Large size and high cost
- Complex control.

For low-power applications, the system size and cost are the main concerns

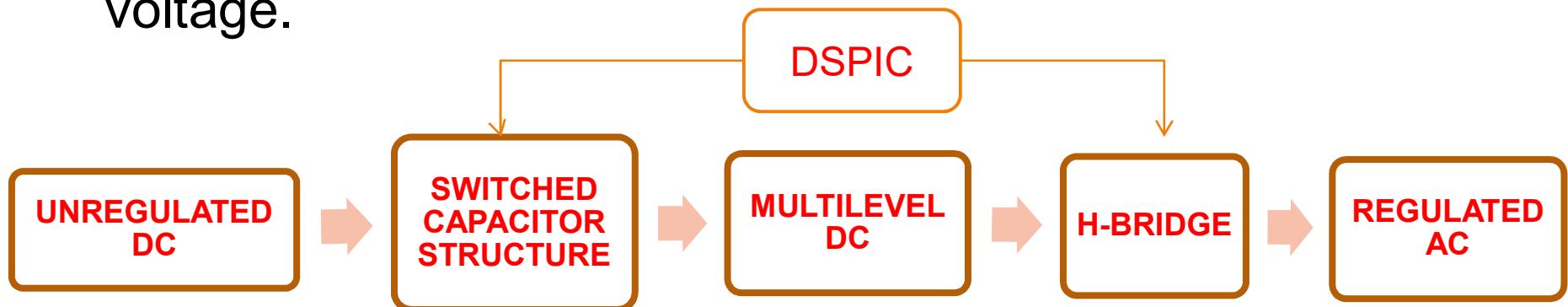
System Objective

The objective of the system is to achieve the following characteristics for a SC-MI:

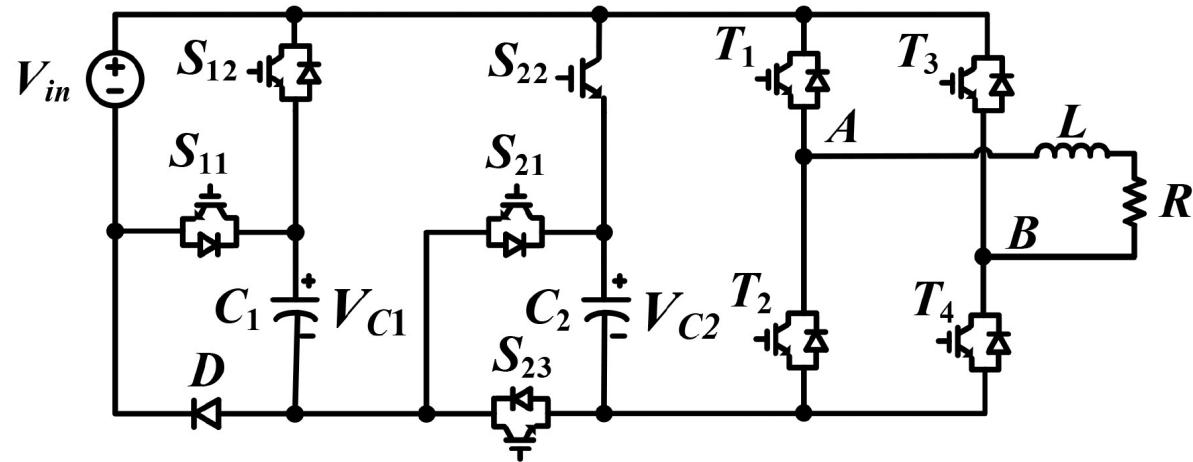
- Fewer components(switches, sources & capacitors)
- Smaller & less expensive.
- Less complex control.
- Requires only one power DC source.
- Boost operation without magnetic elements.

Topology

- Switched-capacitor (SC) structure is added to the H-bridge inverter.
- The SC structures use capacitors, switches, and diodes to create a multilevel DC voltage at the DC bus of the H-bridge circuit.
- H-bridge circuit inverts the multilevel DC voltage to AC voltage.



Schematic

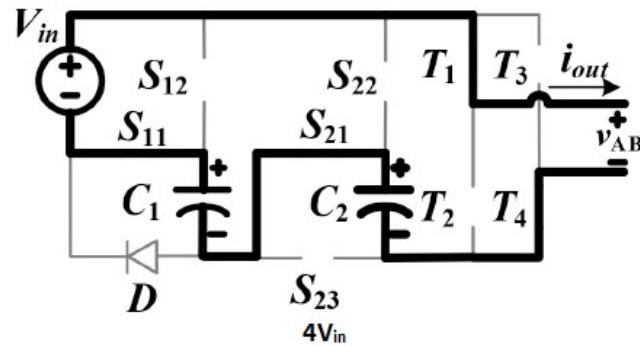
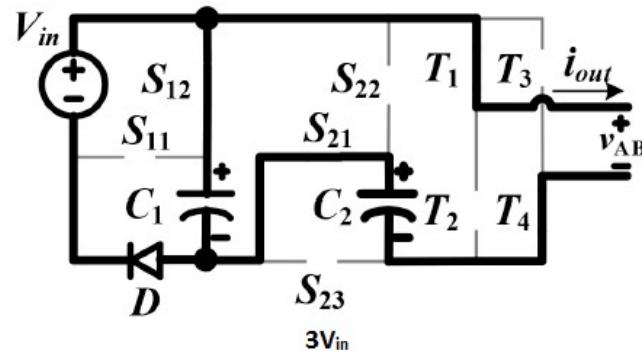
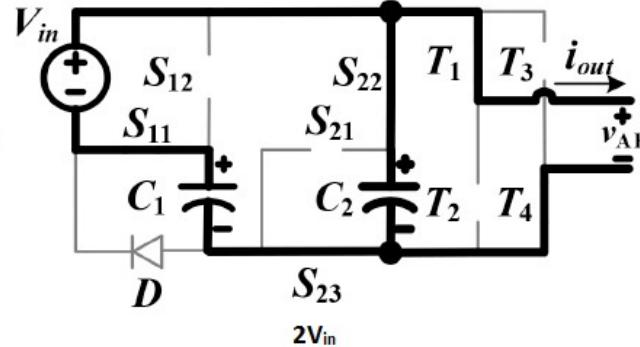
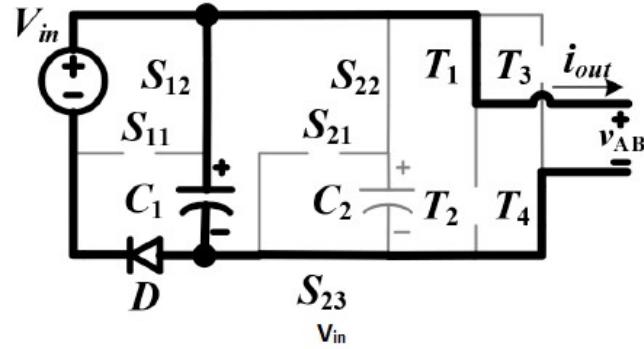


SC nine-level inverter topology

The first SC cell : $(C_1-D-S_{11}-S_{12})$,

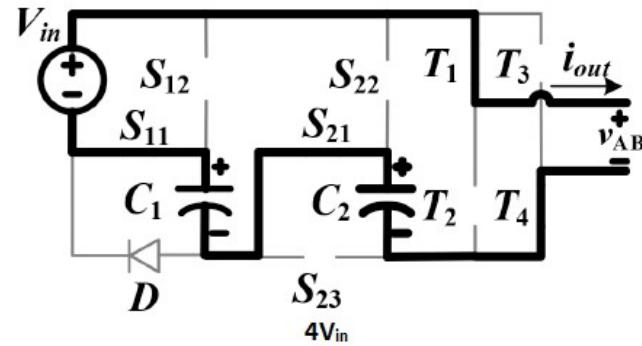
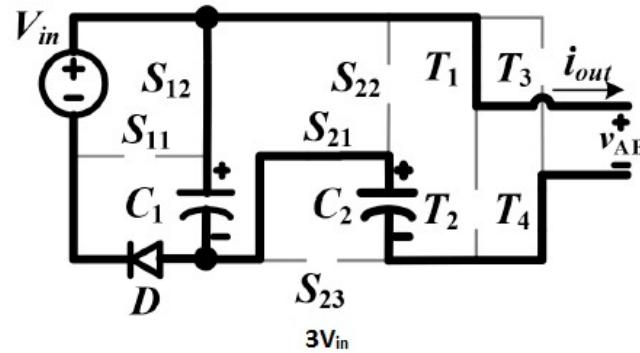
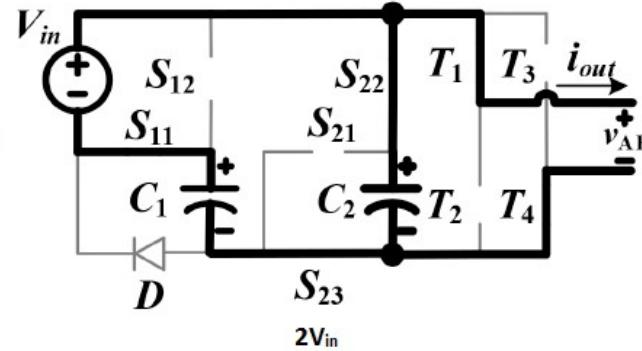
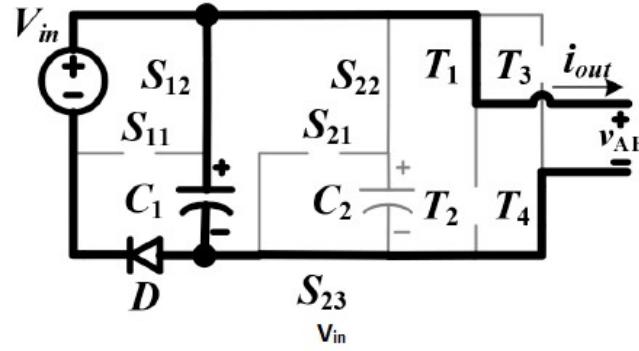
The second SC cell : $(C_2-S_{21}-S_{22}-S_{23})$.

Modes of operation



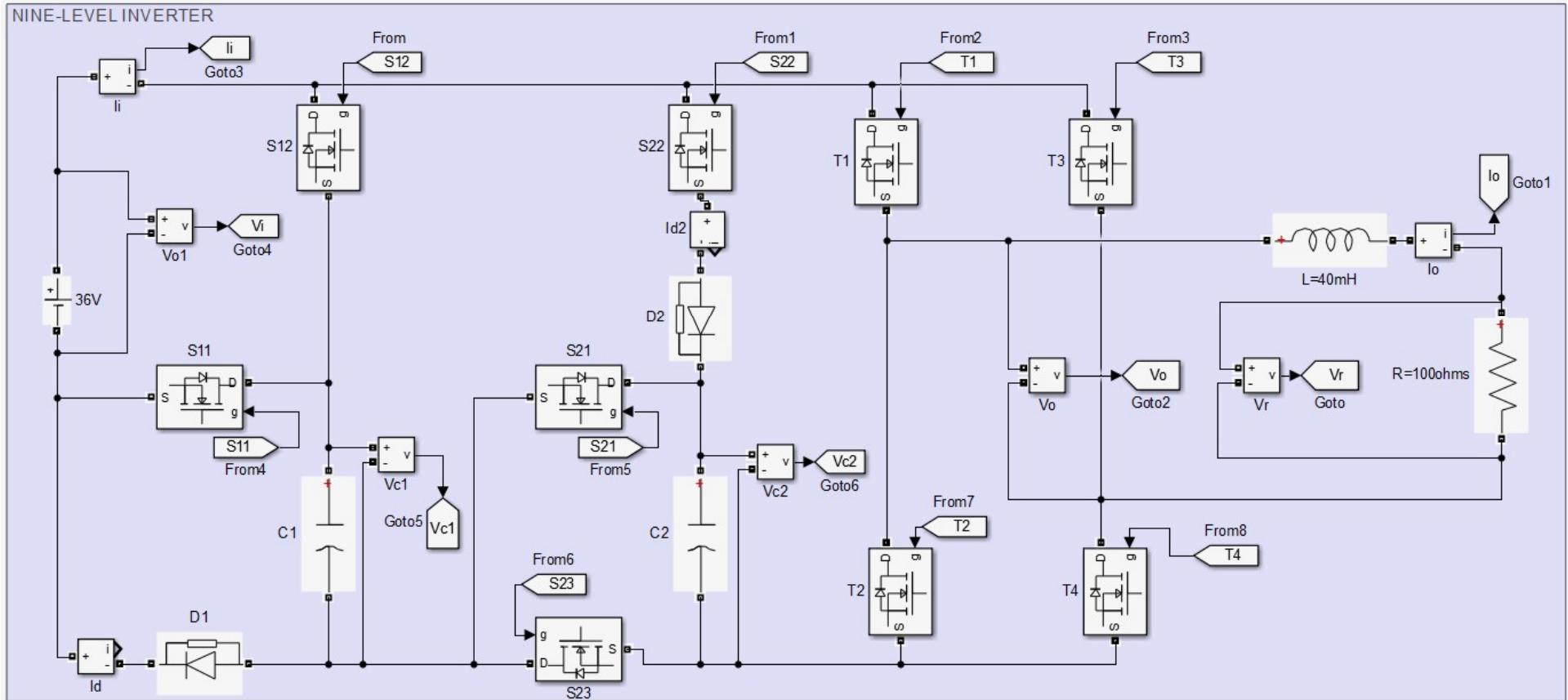
- $1V_{in}$ – Source and C_1 in parallel.
- $2V_{in}$ – Source and C_1 in series which is then parallel with C_2 .
- $3V_{in}$ – Source and C_1 in parallel which is then series with C_2 .
- $4V_{in}$ – Source, C_1 and C_2 all in series.

Switching States



MODE	OUTPUT VOLTAGE	D	S_{11}	S_{12}	S_{23}	S_{22}	S_{21}
1	V_{in}	ON	OFF	ON	ON	ON	OFF
2	$2V_{in}$	OFF	ON	OFF	ON	ON	OFF
3	$3V_{in}$	ON	OFF	ON	OFF	OFF	ON
4	$4V_{in}$	OFF	ON	OFF	OFF	OFF	ON

Simulation

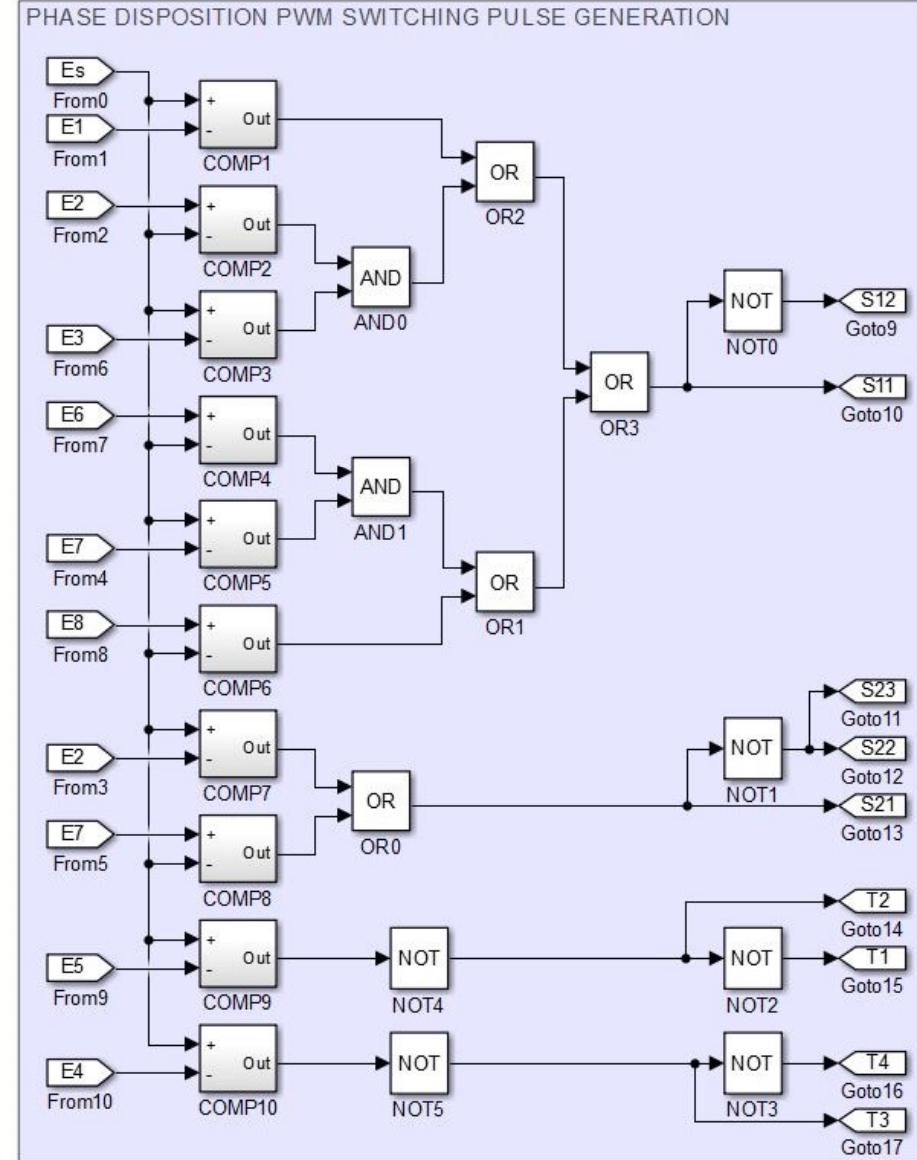
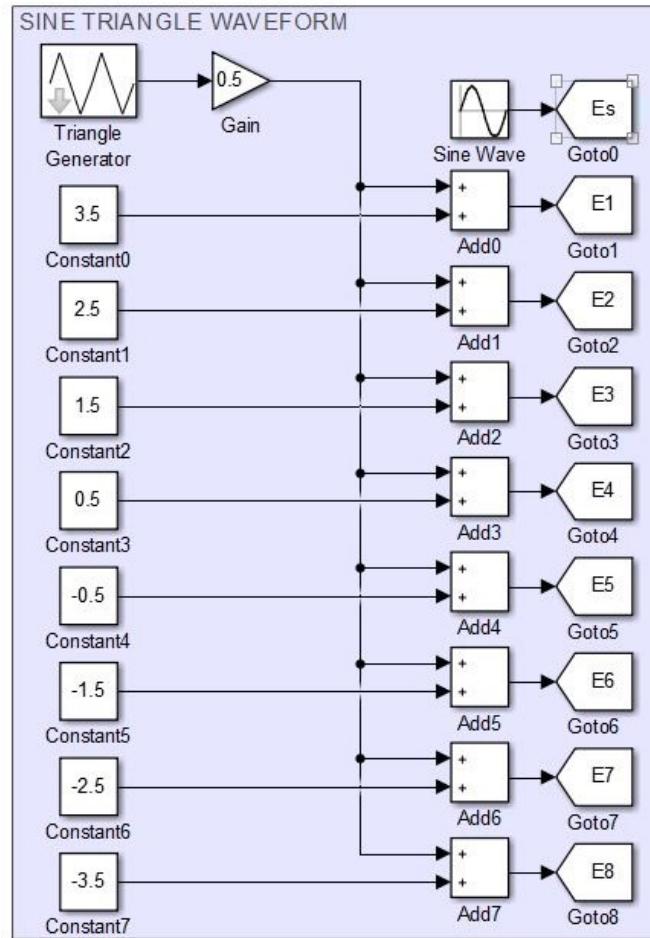


9 Level inverter using 9 Switches 2 diodes.
Simulink model

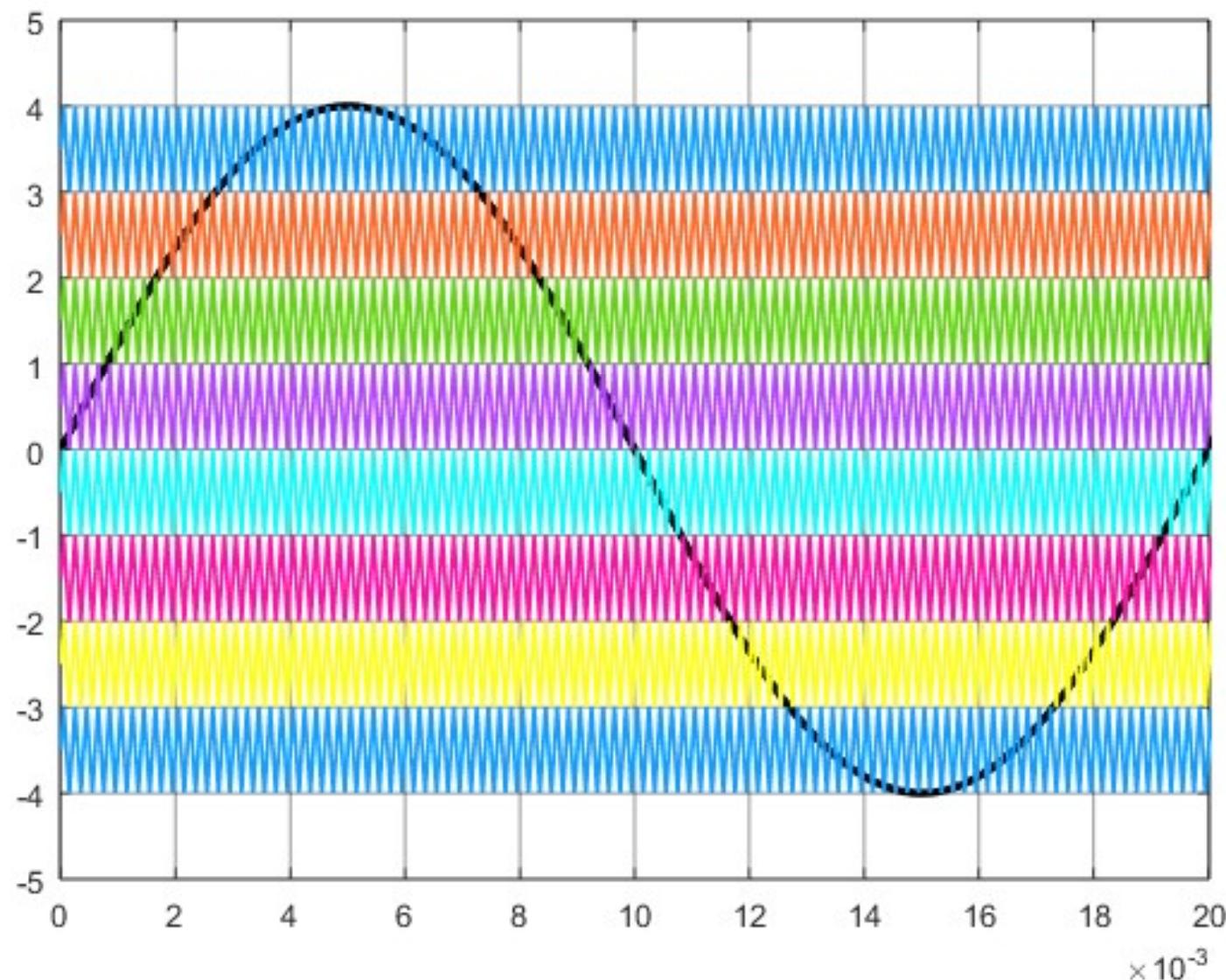
Model Parameters

- Input Voltage: 36V
- Output Voltage : 100V(RMS)
- Output Power: 100Watts
- RL load: $100 + j12.5$ ohms
- Switching frequency: 5KHz
- $C_1 : 2400\mu F$
- $C_2 : 3600\mu F$

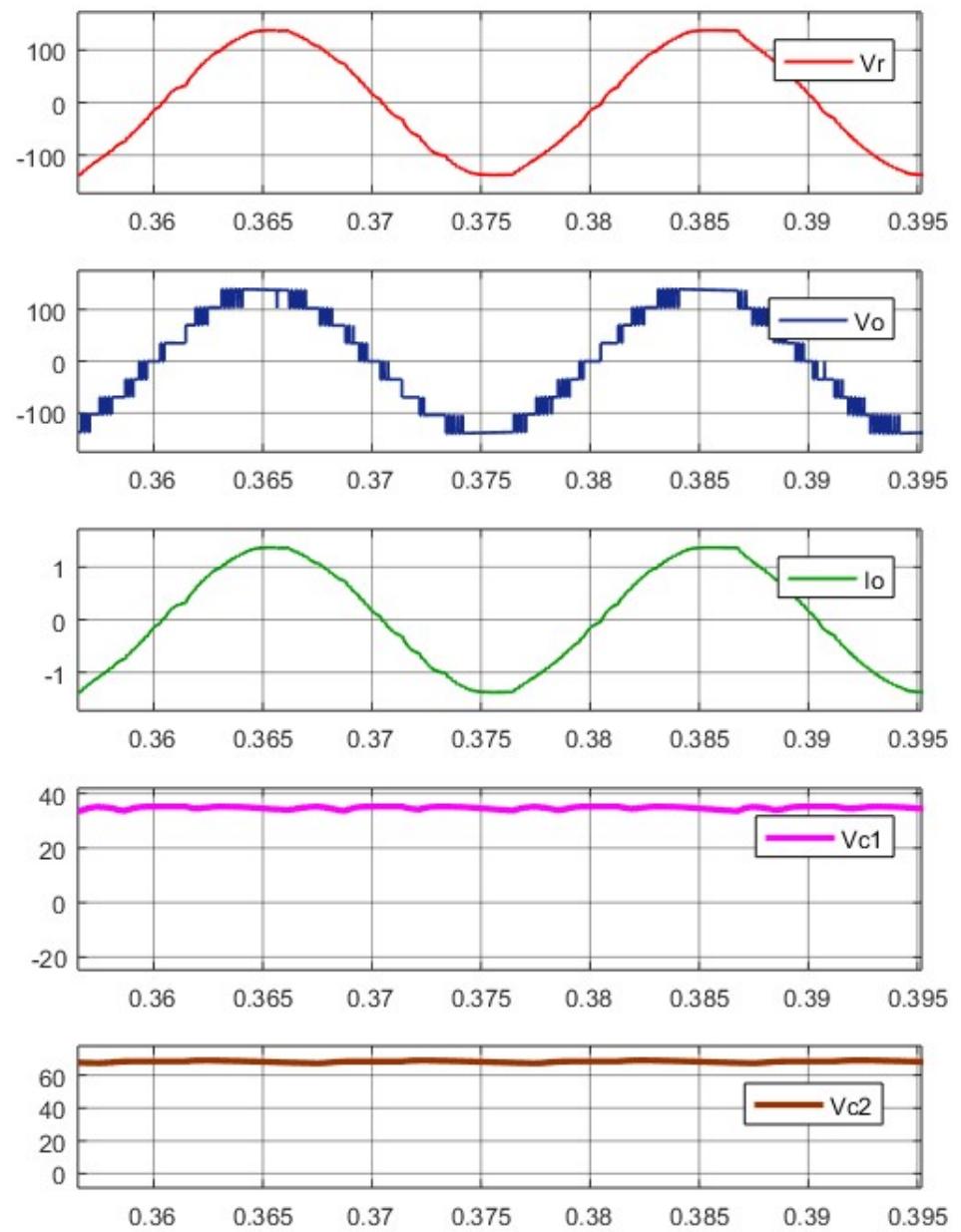
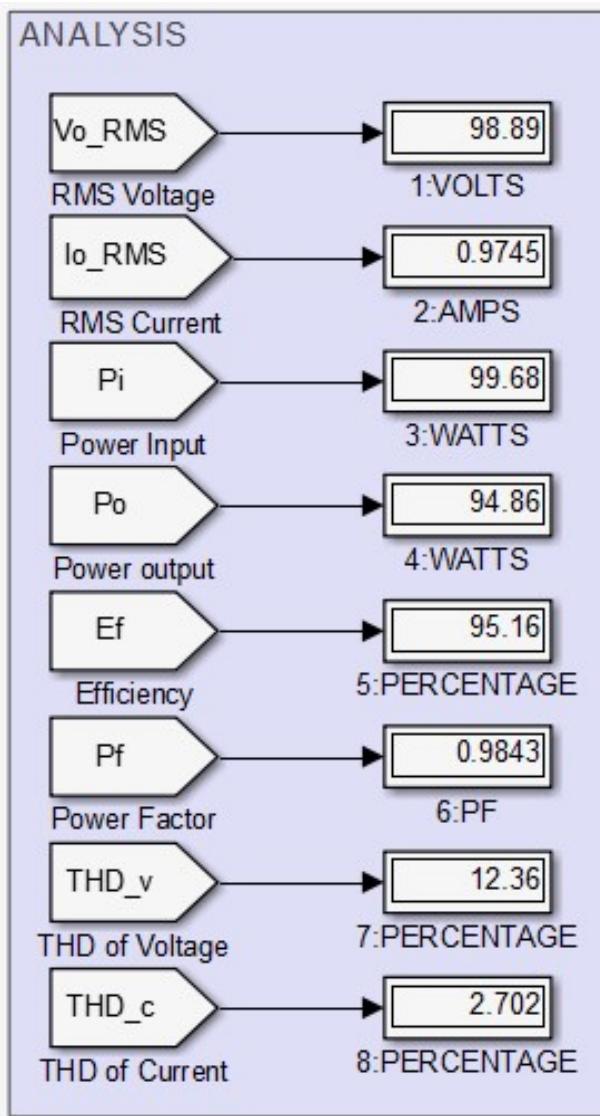
Switching Scheme: PDPWM



Switching Scheme:PDPWM



Simulation Result



Hardware Implementation

➤ Switching Device: MOSFET IRFP460

- Drain to source breakdown Voltage (V_{DS}) : 500V
- Continuous Drain Current(I_D) : 20A
- Turn On delay time(T_{ON}) : 18nS
- Turn Off delay time(T_{OFF}) : 110nS
- Gate Source Threshold(V_{GST}) : 4V



➤ Diode : MUR460

- DC blocking Voltage (V_R) : 600V
- Continuous Forward Current(I_F) : 4A
- Reverse Recovery time(T_{rr}) : 75nS
- Forward Recovery time(T_{fr}) : 50nS



➤ C_1

: 2400 μ F

➤ C_2

: 3600 μ F

Hardware Implementation

- Logic Controller : DSpic30F2020
 - Three 16-bit timers/counters
 - Up to 30 MIPS operation
 - Four PWM generators with 8 outputs
 - Individual dead time for each PWM generator

PWM modes supported:

- Complementary
- Push-Pull
- Multi-Phase
- Variable Phase
- Current Reset
- Current-Limit

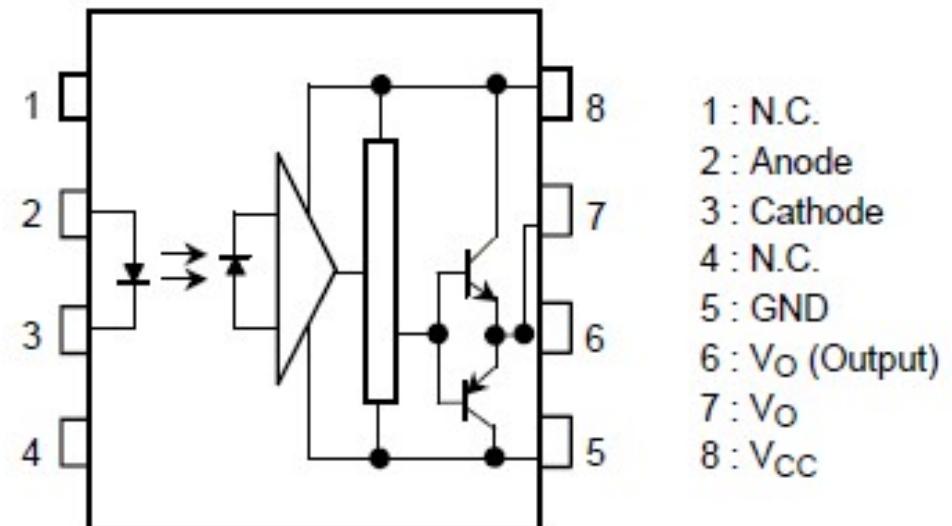


Gate Driver Opto Coupler

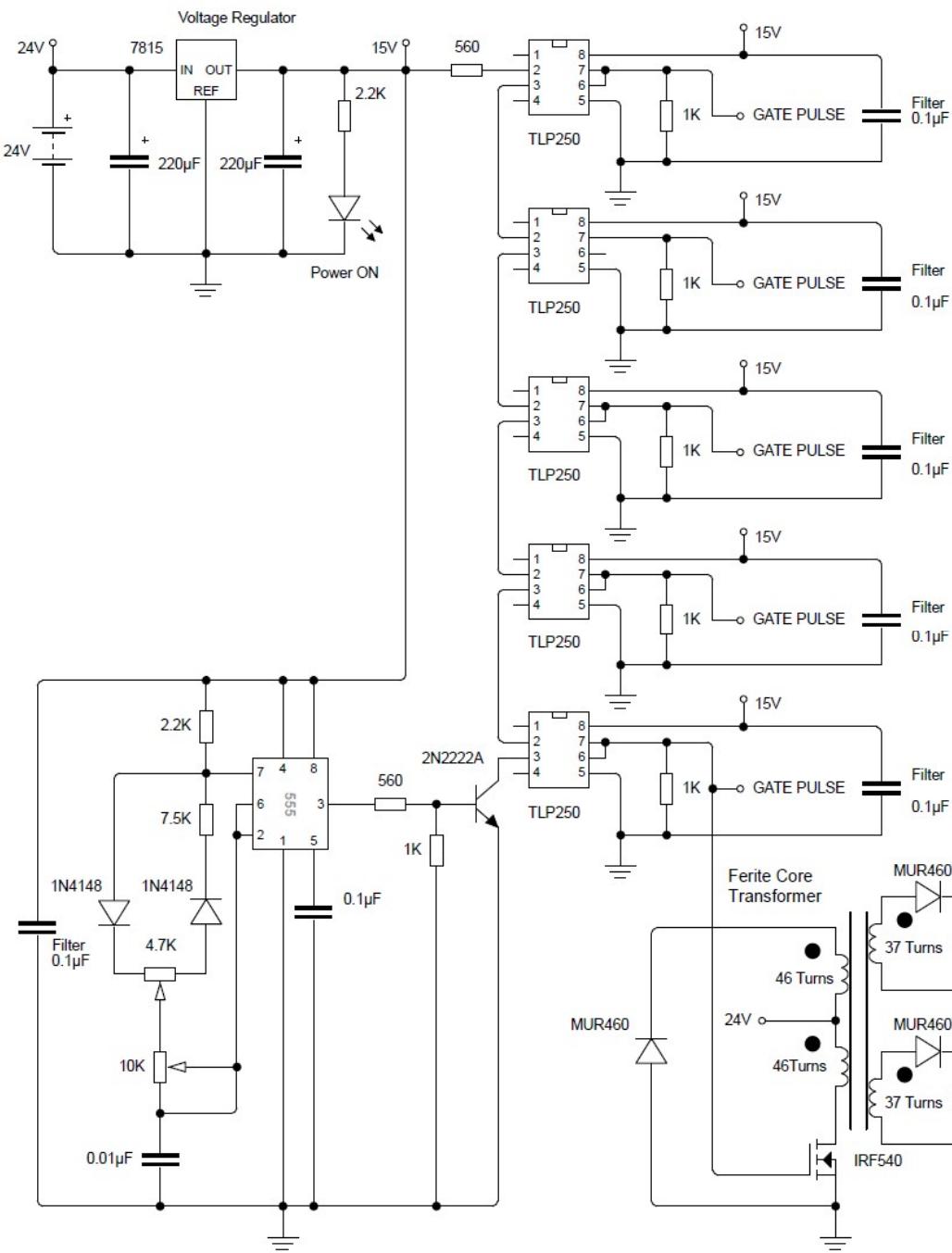
- Provides Isolation
- Converts 5v pulses from Dspic to 15v Gate pulse for Mosfet
- Input threshold current:
 $I_F=5\text{mA}(\text{max})$
- Supply voltage (V_{CC}): 10–35V
- Isolation voltage: $2500\text{V}_{\text{rms}}(\text{min})$

TLP250

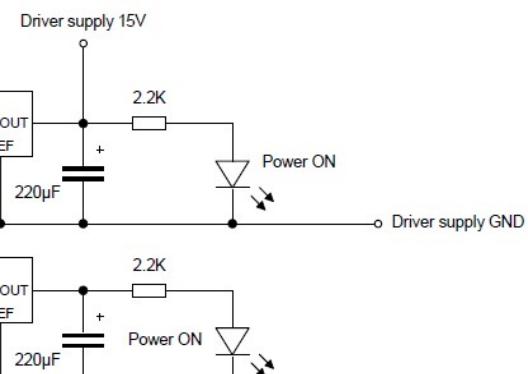
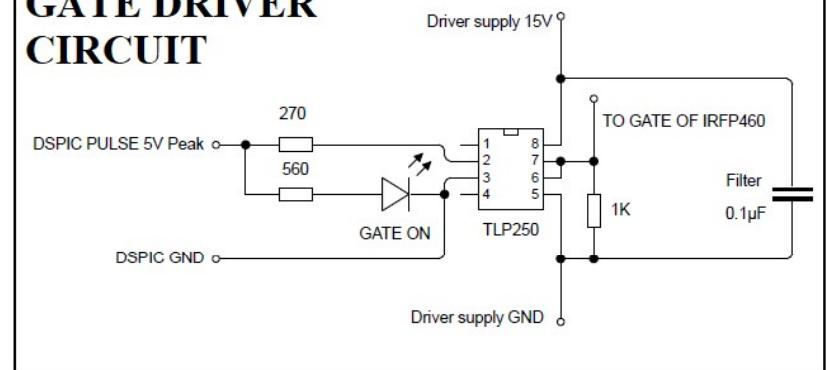
Pin Configuration (top view)



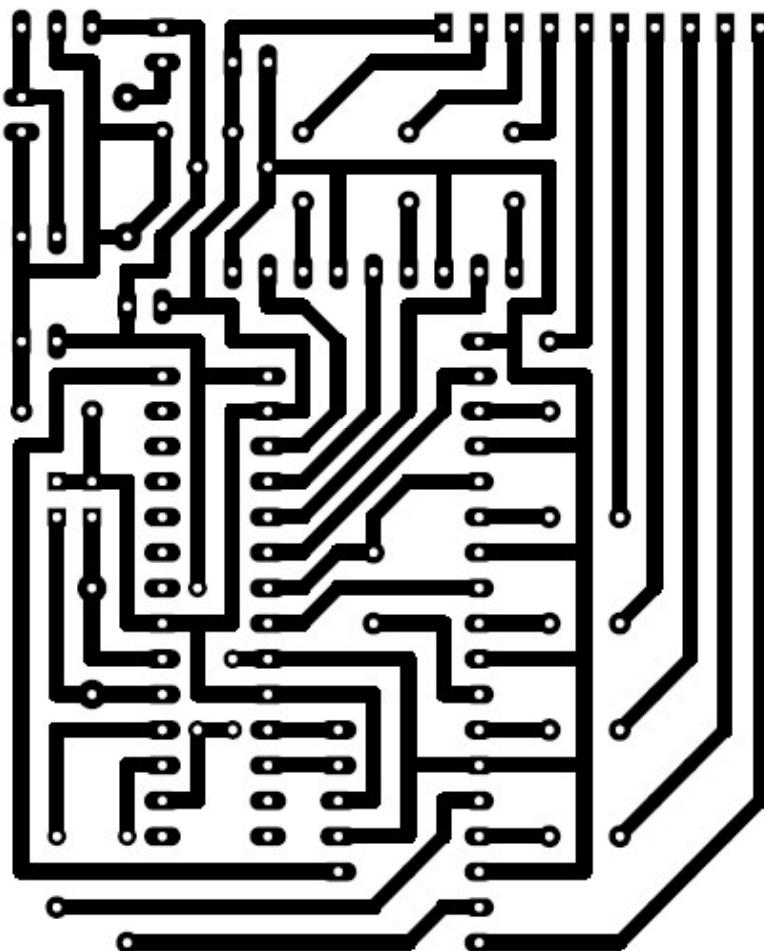
GATE DRIVER POWER SUPPLY CIRCUIT



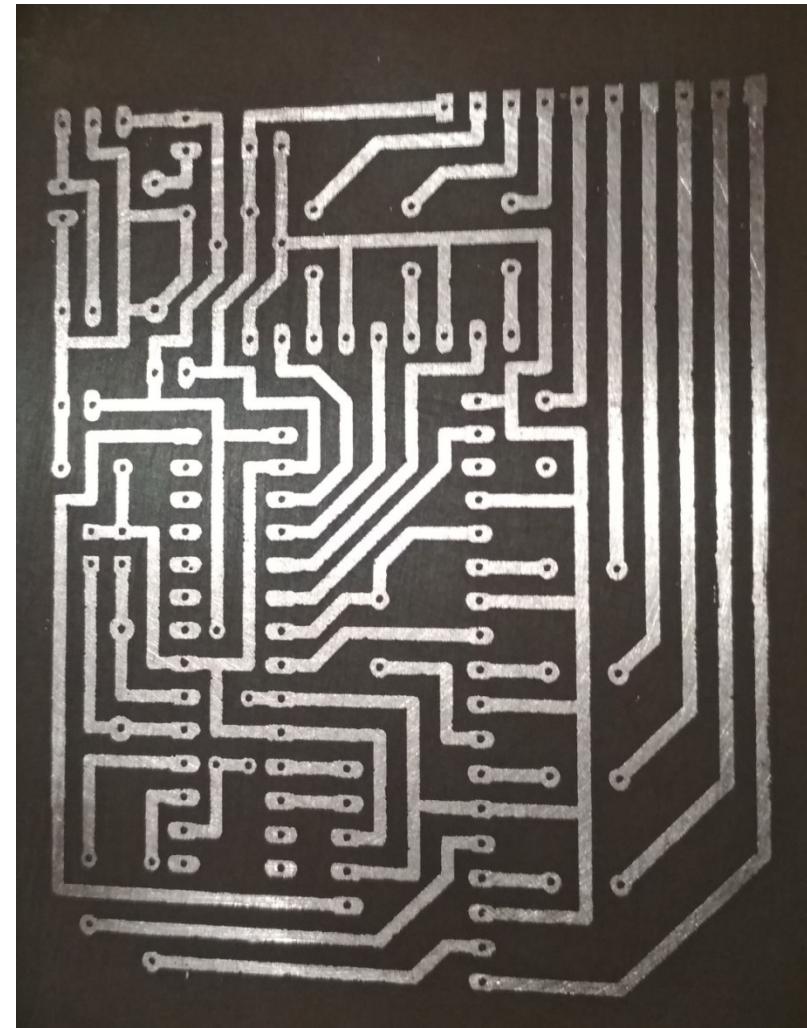
GATE DRIVER CIRCUIT



PCB Realization



Dspic Board Design

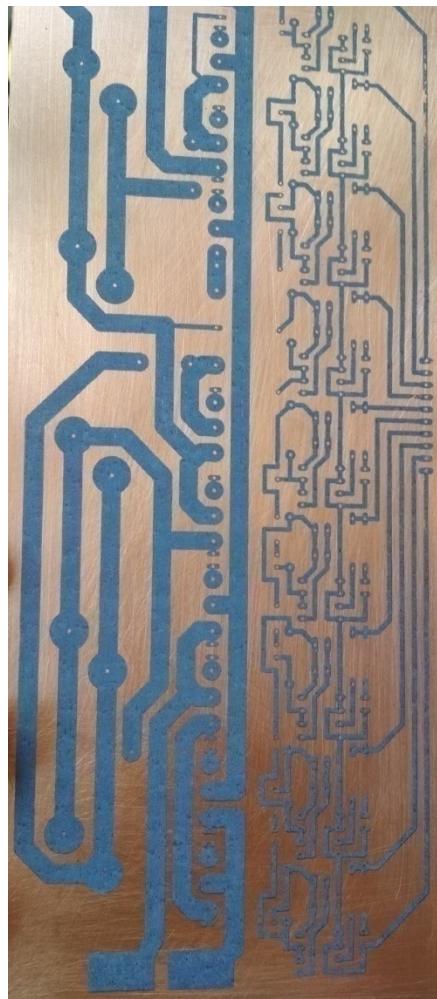


Dspic Board PCB Realization

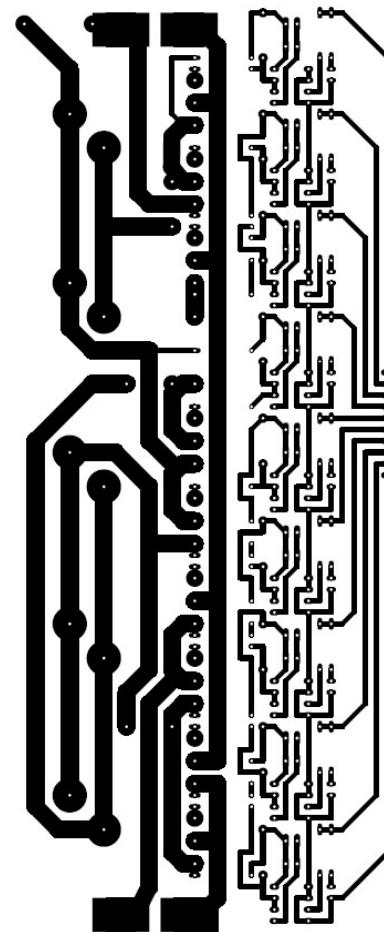
PCB Realization



INVERTER REALIZATION



PCB TONER TRANSFER



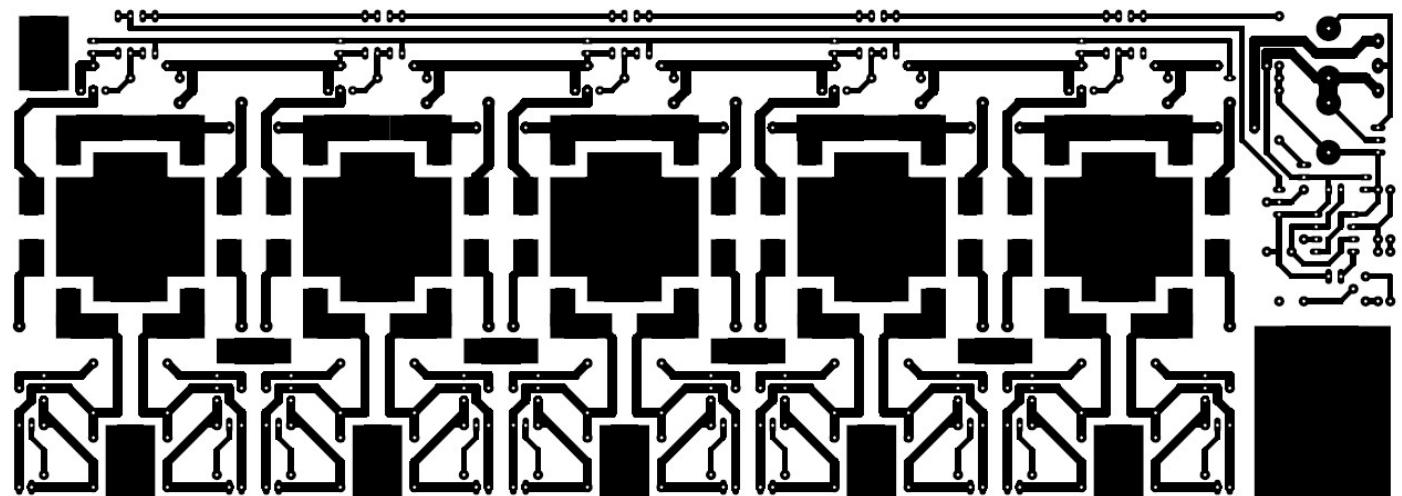
INVERTER PCB DESIGN

PCB Realization

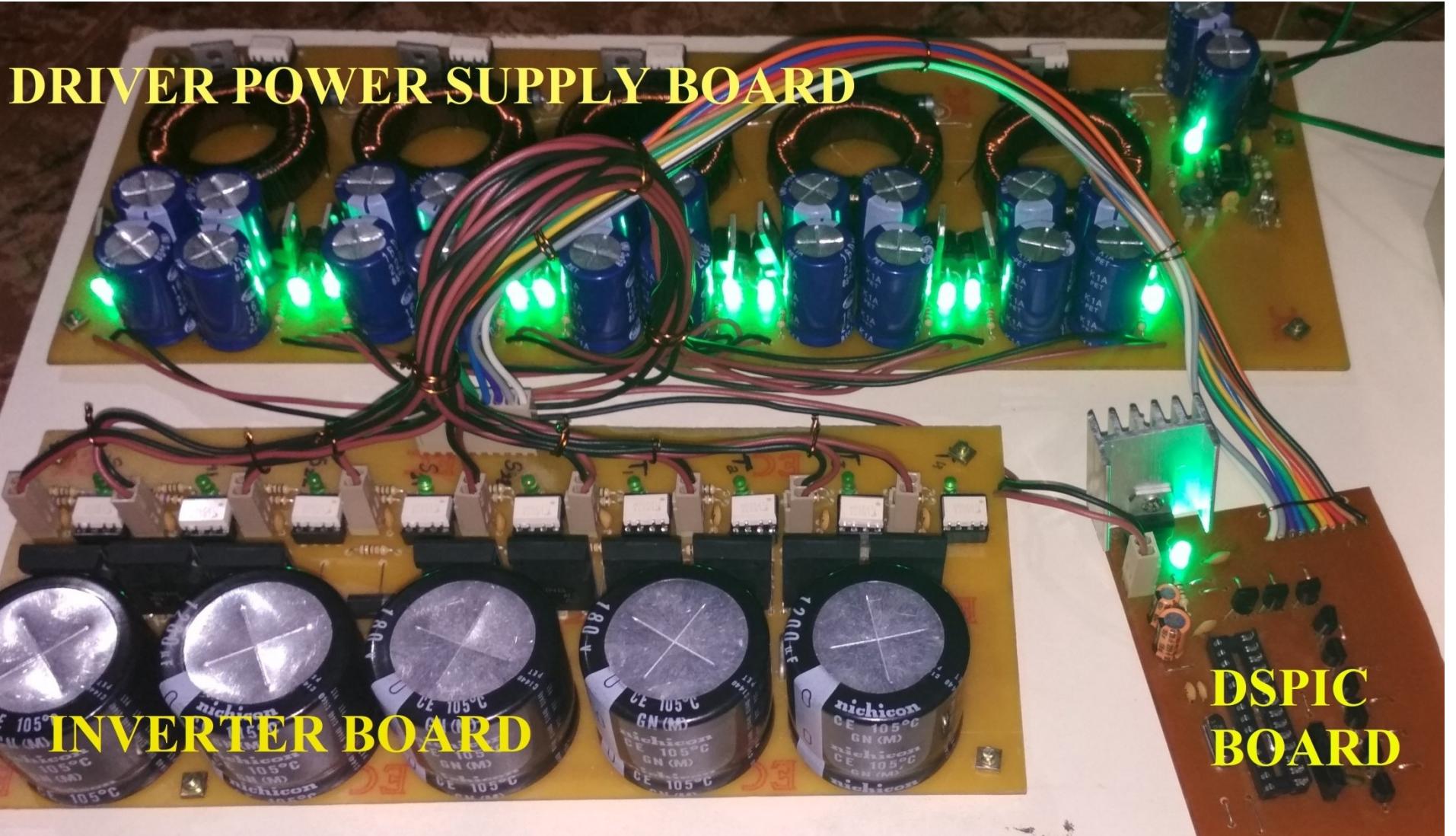
DRIVER SUPPLY
REALIZATION

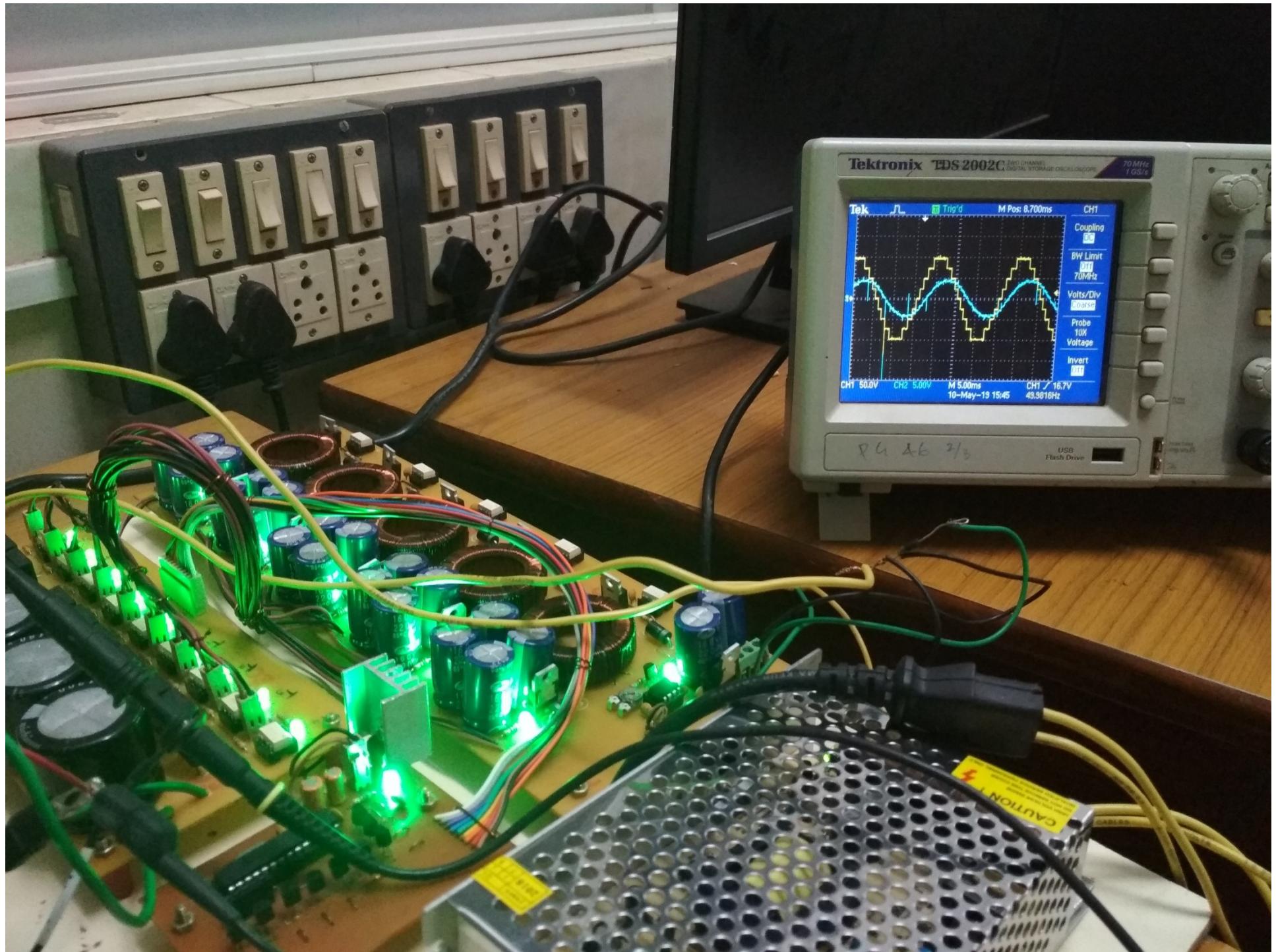


DRIVER SUPPLY
PCB DESIGN

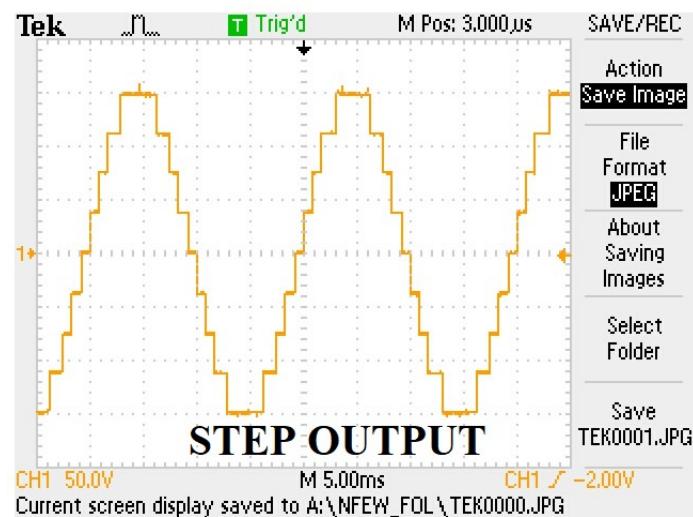
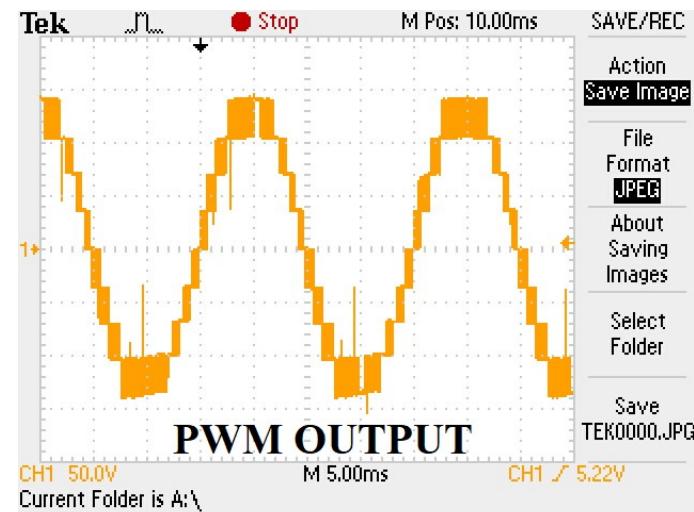


Hardware Realization



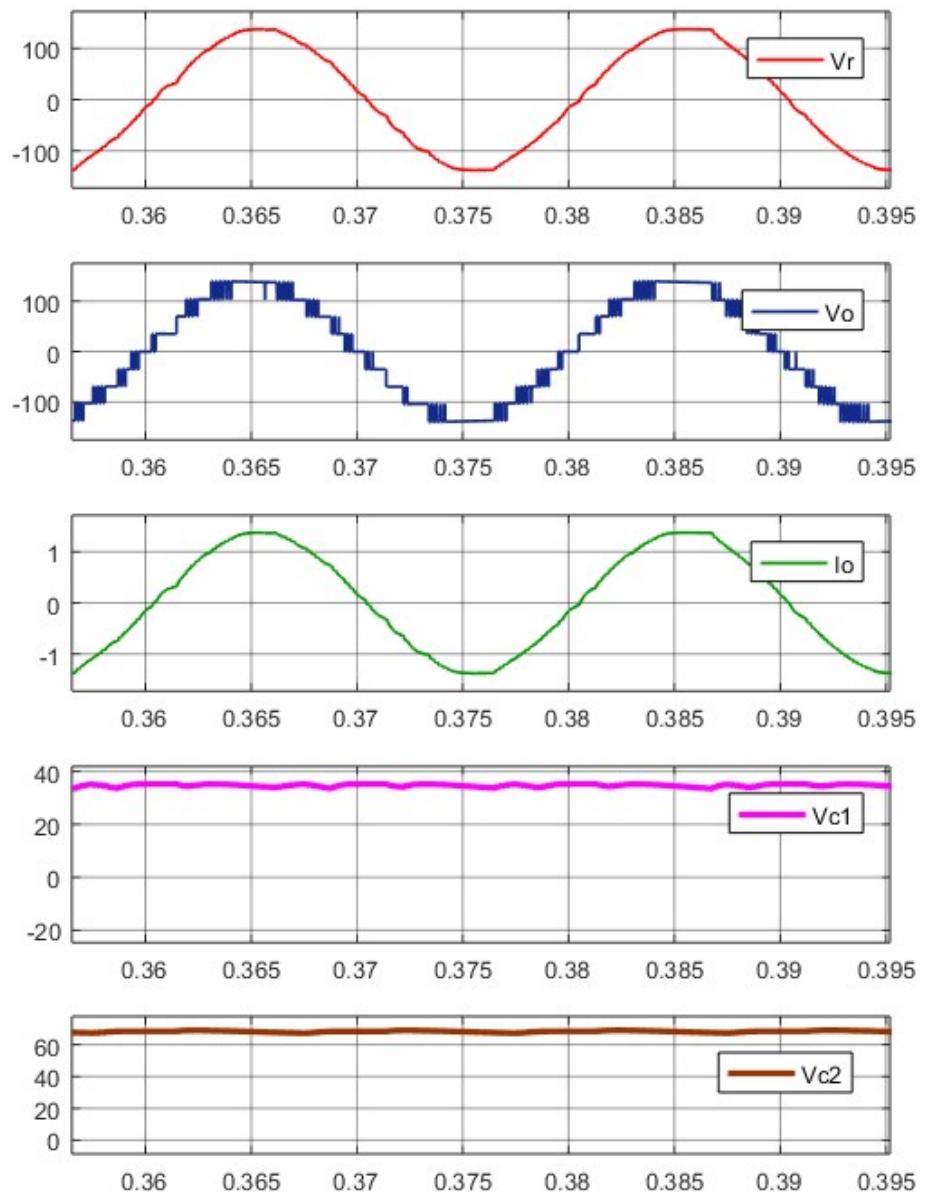


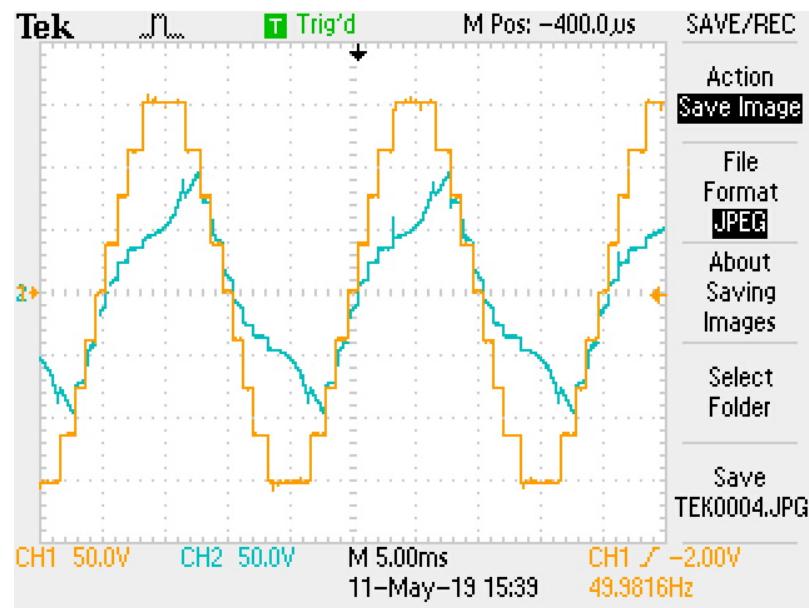
Results



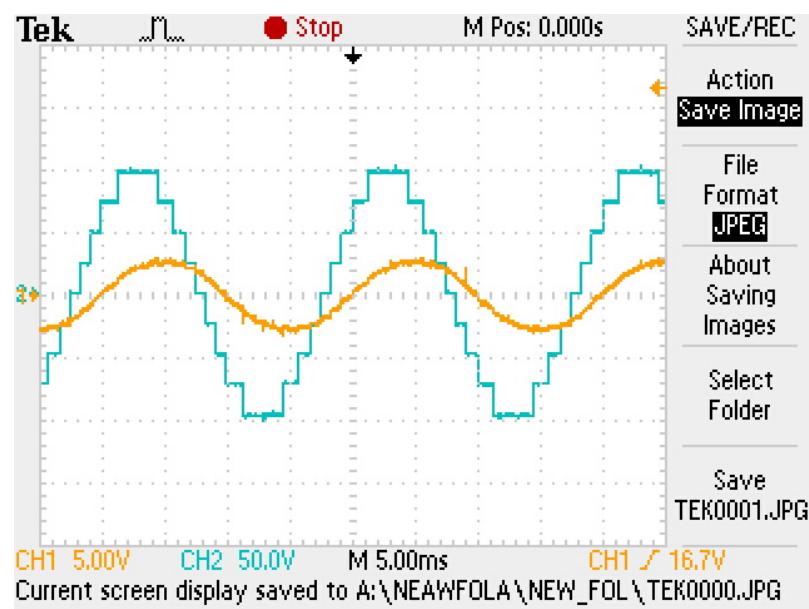
Pk-Pk Voltage: 300 Volts

Simulation Pk-Pk: 300Volts





RL Load @ High Power Factor High THD



The reactance acts as a filter to remove the high frequency components of current.

RL Load @ Low Power Factor Low THD

Conclusion

- Literature survey of the existing multilevel inverter topology was carried out.
- Some shortcomings were discovered and a new topology based on switched capacitor structure was found to be a solution.
- The simulation and modelling of the inverter based on switched capacitor was done.
- Hardware implementation was done to verify the same and was found to be in agreement with the simulation findings.
- Documentation of the findings and results were prepared.

REFERENCE

- [1] Bac-Bien Ngo, Minh-Khai Nguyen , Jae-Hong Kim2 and Firuz Zare, “Single-phase multilevel inverter based on switched-capacitor structure”, *IET Power Electron*, June 2018, ISSN 1755-4535
- [2] Barry W Williams, “Principles and Elements of Power Electronics Devices, Drivers, Applications, and Passive Components”, 2006, ISBN 978-0-9553384-0-3
- [3] Yuanmao Ye, K. W. E. Cheng, Junfeng Liu and Kai Ding, “A Step-Up Switched-Capacitor Multilevel Inverter With Self-Voltage Balancing”, *IEEE Trans. Ind. Electron*, Vol. 61, No. 12, December 2014
- [4] Bhagyalakshmi P S, Beena M Varghese and Dr. Bos Mathew Jos, “Switched Capacitor Multilevel Inverter With Different Modulation Techniques”, *International Conference on Innovations in information Embedded and Communication Systems*, 2017



Thank you