# Multilevel Inverter Based on Switched-Capacitance Structure

INTERIM PROJECT REPORT
Submitted by

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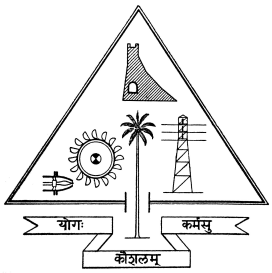


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**Abstract**

Multilevel inverter is a power electronic device capable of providing desired output using multiple lower level DC voltages as an input. Multilevel inverters are gaining popularity over conventional two level inverters because it can produce a smoother stepped output waveform. Moreover, the output obtained from multilevel inverters has lower $d_v/d_t$ and lower harmonic distortions. Multilevel inverters usually make use of diode clamped, flying capacitor or cascaded H-bridge topologies. These topologies suffer from disadvantages such as multitude of components, large size and cost as well as complex control. This project aims to use a switched-capacitance (SC) structure to overcome the disadvantages of the existing topologies. It involves adding an SC structure to the H-bridge inverter using capacitors, switches and diodes to create a multilevel DC voltage at the DC bus of the H-bridge circuit. The proposed technology will improve upon the existing technology by having boost operation without magnetic elements, fewer components, less complex control and using only one power DC source. This project work involves the simulation and hardware implementation of Switched Capacitance Multilevel Inverter

# Introduction

Recently, multilevel inverters (MIs) are getting more attention from researchers because of advantages like better waveform quality, lower EM noise, and lower device stress. MIs are used to couple a DC source to an AC bus for applications like electric motor drivers, uninterruptible power supplies, and distributed generation systems. The following topologies are now used in practice:-

1)Neutral-point clamped (Diode clamped).
2)Flying capacitor.
3)Cascaded H-bridge (CHB).

For low-power applications, the system size and cost are the main concerns. Problems in multilevel inverters (MIs) employing current topologies are the following:-

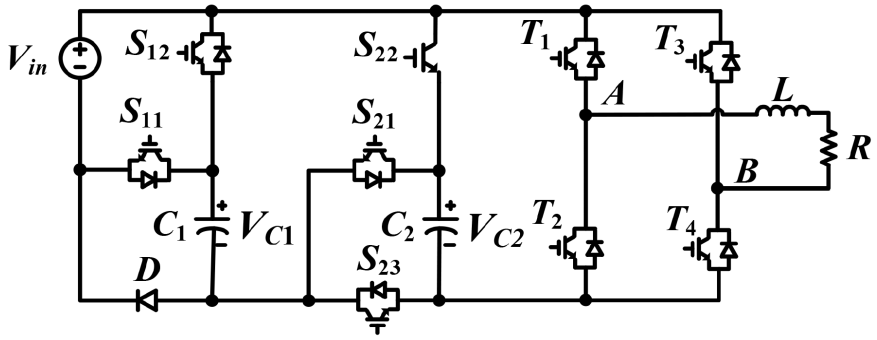
1)Large number of components( switches, power supplies, capacitors, and diodes).
2)Large size and high cost.
3)Complex control.

Solution to the problem is a new MI topology that uses a Switched Capacitor(SC) structure in cascade with an H-bridge. The objective of this new system is to achieve the following characteristics for a SC-MI:-

1)Fewer components(switches, sources and capacitors).
2)Smaller and less expensive.
3)Less complex control.
4)Requires only one power DC source.
5)Boost operation without magnetic elements.

| **Hardware Requirements** | **Software Requirements** |
|---|---|
| DSO (Analysis) | Matlab (Simulation) |
| DSP (controller) | Proteus (Design) |
| Function generator (Analysis and reference) | Latex (Documentation) |

# Methodology




The proposed inverter consists of a single DC source, two SC cells connected in parallel with the H-bridge circuit and a load. The first SC cell is a combination of one capacitor, one diode, and two switches ($C_1 - D - S_{11} - S_{12}$), and the second SC cell includes one capacitor, and three switches ($C_2 - S_{21} - S_{22} - S_{23}$).

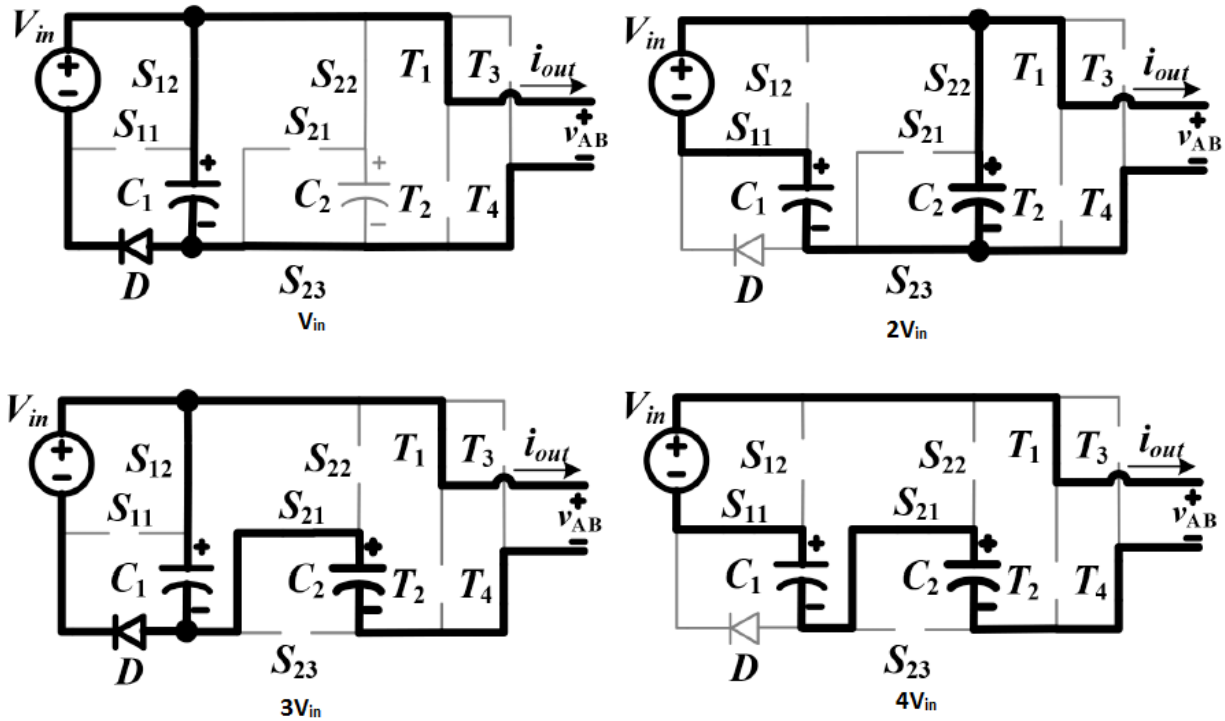
## Working

Capacitor $C_1$ is charged while connected in parallel with the input source through $S_{12}$. It is discharged in series with the input source through $S_{11}$. Capacitor $C_2$ is charged in parallel from the input source and capacitor $C_1$ through $S_{22}$ and $S_{23}$. It is discharged in series with capacitor $C_1$ and the input source through $S_{21}$. $C_1$ is thus charged to $V_{in}$ and $C_2$ is charged to $2V_{in}$. Four Levels of voltage (in addition to a zero level) are therefore obtained by the following combinations:-

| MODE | OUTPUT VOLTAGE | STATE |
|---|---|---|
| 1 | $V_{in}$ | Source and $C_1$ in parallel. |
| 2 | $2V_{in}$ | Source and $C_1$ in series which is then parallel with $C_2$. |
| 3 | $3V_{in}$ | Source and $C_1$ in parallel which is then series with $C_2$. |
| 4 | $4V_{in}$ | Source, $C_1$ and $C_2$ all in series. |

These four levels of voltage can be reversed in polarity at the output by the H-Bridge. Therefore there are 9 different voltage levels ($4 * 2 + 1$) available at the output of the inverter. The switching states are controlled by Phase disposition PWM (PD-PWM).

## Modes of Operation




| MODE | OUTPUT VOLTAGE | $D$ | $S_{11}$ | $S_{12}$ | $S_{23}$ | $S_{22}$ | $S_{21}$ |
|---|---|---|---|---|---|---|---|
| 1 | $V_{in}$ | ON | OFF | ON | ON | ON | OFF |
| 2 | $2V_{in}$ | OFF | ON | OFF | ON | ON | OFF |
| 3 | $3V_{in}$ | ON | OFF | ON | OFF | OFF | ON |
| 4 | $4V_{in}$ | OFF | ON | OFF | OFF | OFF | ON |

| MODE | OUTPUT VOLTAGE | STATE |
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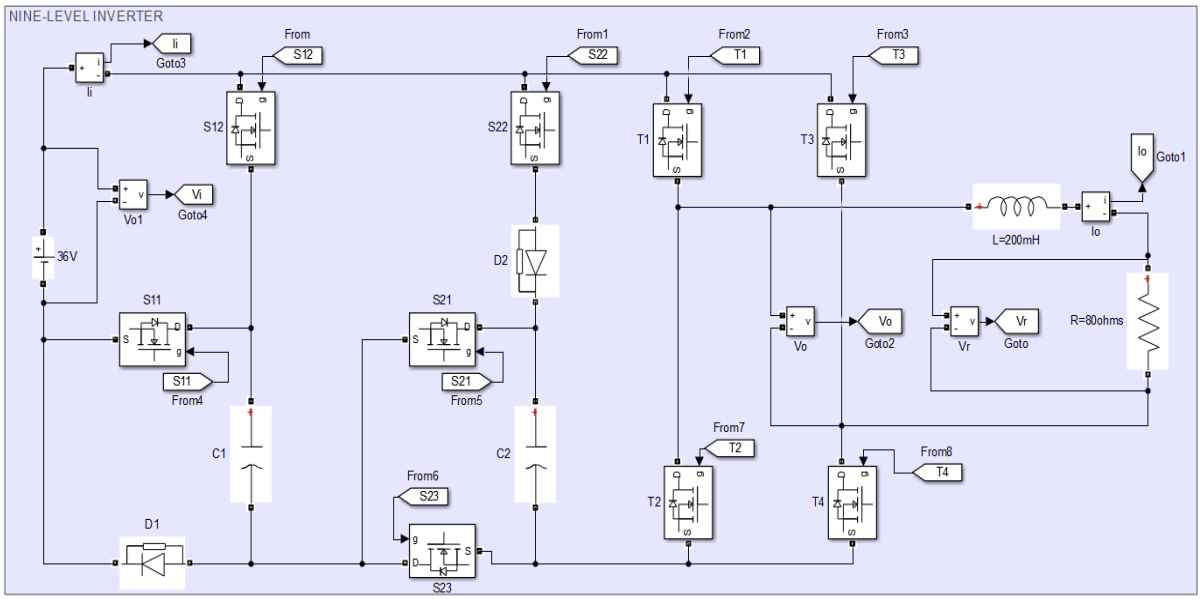
| 4 | $4V_{in}$ | Source, $C_1$ and $C_2$ all in series. |

In the positive half cycle $T_1$ and $T_4$ are fully turned on whereas $T_2$ and $T_3$ are fully turned OFF. Similarly, in the negative period, $T_2$ and $T_3$ are fully turned on whereas $T_1$ and $T_4$ are fully turned OFF and the components of the SC cells are similar to those in the positive period. To acheive zero voltage output $T_1$ and $T_3$ are turned on simultaneously.

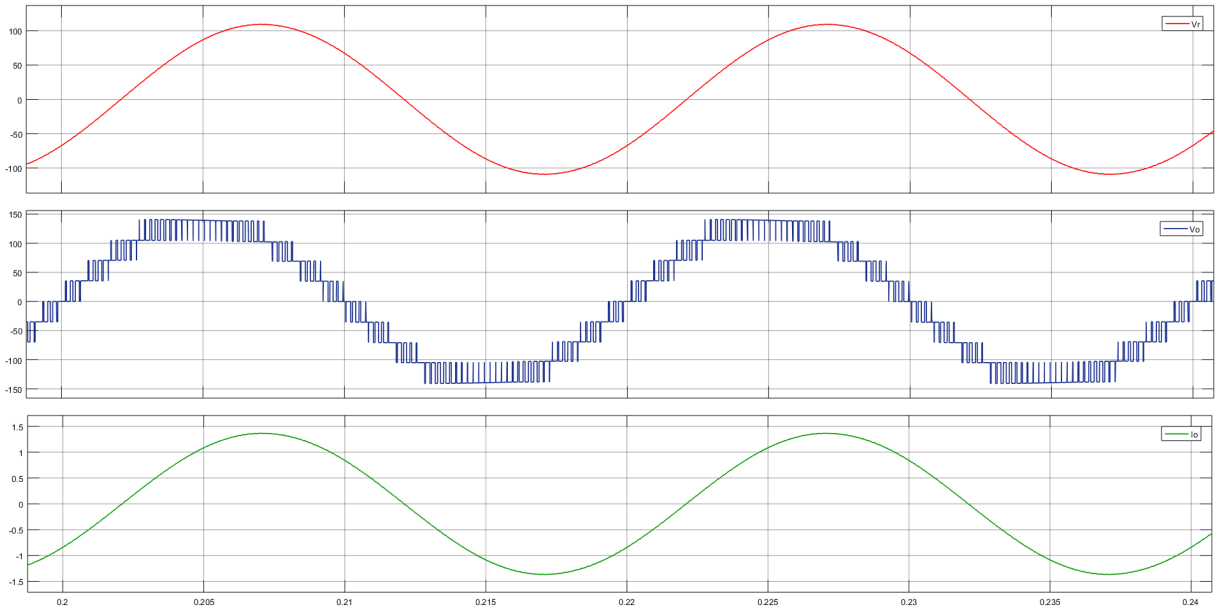
# Simulation



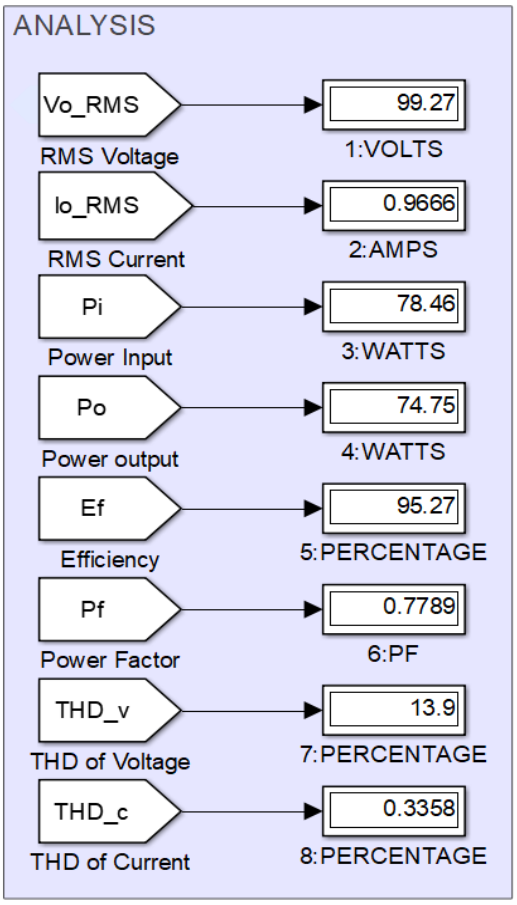

The simulation of the NINE-LEVEL INVERTER was done using the simulink tool in matlab. Operation of the inverter was verified with R and R-L load. Gating pulses are derived using PD-PWM technique. The switching delay and gate delay are neglected. The design consideration are given in the table below.

| **PARAMETER** | **VALUE** |
|---|---|
| $V_{in}$ | $36V$ |
| $C_1$ , $C_2$ | $2000\mu F$ |
| $R + jX_l$ | $80\ \Omega + j60\Omega$ |
| Diode Forward Drop | $0.7V$ |
| Mosfet On Resistance | $0.1\Omega$ |
| Modulating Frequency | $50H_z$ |
| Carrier Frequency | $5000H_z$ |
| Modulating index | $100\%$ |

# Result




The Total Harmonic Distortion in Current was found to be 0.3358%. Efficiency of the inverter is 95.27%.



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