

NINE LEVEL INVERTER BASED ON SWITCHED CAPACITOR STRUCTURE

PROJECT REPORT

Submitted by

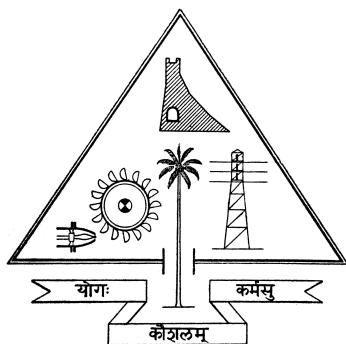
ABHILASH M M (TCR15EE002)
ALIN ANTO (TCR15EE016)
DEVIKA SAJEEV (TCR15EE042)
DON DEV (TCR15EE046)

to

The APJ Abdul Kalam Technological University
in partial fulfillment of the requirements for the award of the degree

of

Bachelor of Technology
in
Electrical and Electronics Engineering



Department of Electrical Engineering
Government Engineering College, Thrissur
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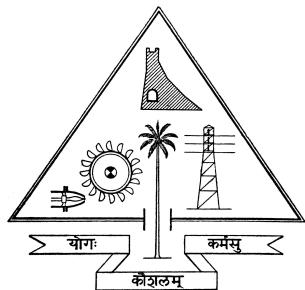
DECLARATION

We undersigned hereby declare that the project report (Nine Level Inverter based on Switched Capacitor Structure), submitted for partial fulfillment of the requirements for the award of degree of Bachelor of Technology of the APJ Abdul Kalam Technological University, Kerala is a bonafide work done by us under supervision of T.G. SANISH KUMAR, Associate Professor, Government Engineering College, Thrissur. This submission represents our ideas in our own words and where ideas or words of others have been included; we have adequately and accurately cited and referenced the original sources. We also declare that we have adhered to ethics of academic honesty and integrity and have not misrepresented or fabricated any data or idea or fact or source in our submission. We understand that any violation of the above will be a cause for disciplinary action by the institute and/or the University and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been obtained. This report has not been previously formed the basis for the award of any degree, diploma or similar title of any other University.

Thrissur
15/05/2019

ABHILASH MM
ALIN ANTO
DEVIKA SAJEEV
DON DEV

Department of Electrical Engineering Government Engineering College, Thrissur



CERTIFICATE

This is to certify that the Project Report titled "**NINE LEVEL INVERTER BASED ON SWITCHED CAPACITOR STRUCTURE**" is a bonafide record of the work carried out by **ABHILASH M M (TCR15EE002)**, **ALIN ANTO (TCR15EE016)**, **DEVIKA SAJEEV (TCR15EE042)**, **DON DEV (TCR15EE046)** to the APJ Abdul Kalam Technological University in partial fulfillment of the requirements for the award of the Degree of Bachelor of Technology (Electrical and Electronics Engineering) is a bonafide record of the project work carried out by them under my guidance and supervision. This report in any form has not been submitted to any other University or Institute for any purpose.

Internal Supervisor

T.G SANISH KUMAR

Associate Professor

Dept. of Electrical Engineering

Govt. Engineering College, Thrissur

Dr. REJI P

Head of Department

Dept. of Electrical Engineering

Govt. Engineering College, Thrissur

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ABSTRACT

Multilevel inverter is a power electronic device capable of providing desired output using multiple lower level DC voltages as an input. Multilevel inverters are gaining popularity over conventional two level inverters because it can produce a smoother stepped output waveform. Moreover, the output obtained from multilevel inverters has lower dv/dt and lower harmonic distortions. Multilevel inverters usually make use of diode clamped, flying capacitor or cascaded H-bridge topologies. These topologies suffer from disadvantages such as multitude of components, large size and cost as well as complex control. This project aims to use a switched-capacitance (SC) structure to overcome the disadvantages of the existing topologies. It involves adding an SC structure to the H-bridge inverter using capacitors, switches and diodes to create a multilevel DC voltage at the DC bus of the H-bridge circuit. The proposed technology will improve upon the existing technology by having boost operation without magnetic elements, fewer components, less complex control and using only one power DC source. This project work involves the simulation and hardware implementation of Nine level Inverter based on Switched Capacitance Structure.

Contents

ACKNOWLEDGEMENT	3
ABSTRACT	4
LIST OF FIGURES	7
LIST OF TABLES	9
1 INTRODUCTION	10
1.1 GENERAL BACKGROUND	10
1.2 OBJECTIVE	10
1.3 SCOPE	11
1.4 REQUIREMENTS	11
2 LITERATURE SURVEY	12
2.1 Diode Clamped Structure	13
2.2 Capacitor-Clamped Inverter	14
2.3 Cascaded H-Bridge Inverter	15
3 SWITCHED CAPACITOR NINE LEVEL INVERTER	17
3.1 Switched Capacitor Structure	18
3.2 Modes of Operation	19
3.3 Switching States	21
3.4 Phase Disposition PWM	21
4 SIMULATION RESULTS	24
4.1 Result	26
4.1.1 Peak Inverse Voltage(PIV)	26

4.1.2	Total Harmonic Distortion(THD)	27
4.1.3	Efficiency	27
5	HARDWARE IMPLEMENTATION AND RESULTS	30
5.1	MOSFET IRFP460	31
5.2	MUR460	31
5.3	DSPIC30F2020	32
5.4	Gate Driver Opto Coupler	34
5.5	Gate Power Supply	35
5.6	PCB Realization	36
5.7	Hardware Realization	39
5.8	Results	41
6	CONCLUSION	44
References		44

List of Figures

2.1	Two phase diode clamped multilevel inverter	13
2.2	Capacitor-Clamped Multilevel Inverter	15
2.3	Single H-Bridge Topology	16
3.1	Switched Capacitor 9-level inverter circuit	17
3.2	Modes of operation	20
3.3	Phase Disposition PWM Scheme	22
3.4	Switching diagram	23
4.1	Simulink circuit	24
4.2	Simulink Pulse Derivation	25
4.3	Measurement Block	26
4.4	Simulink analysis	27
4.5	Simulink Output	28
4.6	Simulink FFT analysis with R load	29
4.7	Simulink FFT analysis with RL load	29
5.1	IRFP460	31
5.2	MUR460	31
5.3	DSPICIC30F2020 Pin diagram.	32
5.4	TLP250 Pin Configuration	34
5.5	Gate Driver Power Supply Circuit	35
5.6	DSPIC Board Design	36
5.7	DSPIC Board PCB Realisation	36
5.8	Inverter Realisation	37
5.9	PCB Toner Transfer	37
5.10	Inverter PCB Design	37

5.11	Driver Supply Realization	38
5.12	Driver Supply PCB Design	38
5.13	Nine level inverter hardware	39
5.14	Hardware	40
5.15	Output voltage waveform for R load ($R=100\Omega$)	41
5.16	Output voltage and current waveforms for RL load ($R=300\Omega$, $L=20mH$)	42
5.17	Output voltage and current waveforms for RL load ($R=100\Omega$, $L=40mH$)	42

List of Tables

1.1	System Requirements	11
3.1	Comparison of the number of components in a 9 level inverter	18
3.2	Output voltage states	19
3.3	Output voltage states	21
3.4	Switching states	21
4.1	Simulation specification	25
5.1	Hardware specification	30
5.2	IRFP460 Specs	31
5.3	MUR460 Specs	31
5.4	TLP250 Specs	34

Chapter 1

INTRODUCTION

1.1 GENERAL BACKGROUND

Recently, multilevel inverters (MIs) are getting more attention from researchers because of advantages like better waveform quality, lower EM noise, and lower device stress. MIs are used to couple a DC source to an AC bus for applications like electric motor drivers, uninterruptible power supplies, and distributed generation systems. The following topologies are now used in practice:-

- 1)Neutral-point clamped (Diode clamped).
- 2)Flying capacitor.
- 3)Cascaded H-bridge (CHB).

1.2 OBJECTIVE

For low-power applications, the system size and cost are the main concerns. Problems in multilevel inverters (MIs) employing current topologies are the following:-

- 1)Large number of components(switches, power supplies, capacitors, and diodes).
- 2)Large size and high cost.
- 3)Complex control.

Solution to the problem is a new MI topology that uses a Switched Capacitor(SC) structure in cascade with an H-bridge. The objective of this new system is to achieve the following characteristics for a SC-MI:-

- 1)Fewer components(switches, sources and capacitors).
- 2)Smaller and less expensive.
- 3)Less complex control.
- 4)Requires only one power DC source.
- 5)Boost operation without magnetic elements.

1.3 SCOPE

Future holds immense scope for multi-level inverters. The electronic devices in the future which may comprise entirely of ICs and other microprocessors would require very high standards of power quality which may not be realistically conceived by means of the existing inverter topologies. Also, the existing MI topologies are bulky, complex to control and expensive. The switched capacitance topology is however, easy to control and cheap while using lesser number of switches. With further research and development, mutli-level inverters may take over the market for inverters in the growing electronic industry.

1.4 REQUIREMENTS

Hardware Requirements	Software Requirements
DSO (Analysis)	Matlab (Simulation)
DSP (controller)	Proteus (Design)
Function generator (Analysis and reference)	Latex (Documentation)

Table 1.1: System Requirements

Chapter 2

LITERATURE SURVEY

The Multilevel inverter is a novel concept emerging as a promising advancement in the field of inverters since they provide features like fewer components, smaller and less expensive system, less complex control, etc. The existing researches have implemented multilevel inverters using techniques like cascaded H-bridge, diode clamped, flying capacitor structure, etc. Multilevel inverters have an arrangement of power switching devices and capacitor voltage sources. Multilevel inverters are suitable for high-voltage applications because of their ability to synthesize output voltage waveforms with a better harmonic spectrum and attain higher voltages with a limited maximum device rating.

Balancing among dc link and clamping capacitors exists in both neutral point clamped and flying capacitor inverters. Diode clamped or neutral clamped has the difficulty of increase in the number of clamping diodes as the level increases. Similarly, in flying capacitor the number of capacitors increases and system becomes bulkier. Among these inverter topologies cascaded inverter achieves greater reliability and simplicity.

A multilevel inverter has several advantages over a conventional two-level inverter that uses high switching frequency pulse width modulation (PWM). The most attractive features of a multilevel inverter are as follows:

- 1) They can generate output voltages with extremely low distortion and lower dv/dt .
- 2) They draw input current with very low distortion.
- 3) They generate smaller common-mode (CM) voltage.
- 4) They can operate with a lower switching frequency.

Multilevel inverters have an arrangement of power switching devices and capacitor voltage sources. Multilevel inverters are suitable for high-voltage applications because of their ability to synthesize output voltage waveforms with a better harmonic spectrum and attain higher voltages with a limited maximum device rating.

There are three main types of multilevel inverters: diode-clamped (neutral-clamped), capacitor-clamped (flying capacitors), and cascaded H-bridge inverter.

2.1 Diode Clamped Structure

The diode-clamped inverter is also known as the neutral-point clamped inverter (NPC) which was introduced by Nabae et al (1981). The diode-clamped inverter consists of two pairs of series switches (upper and lower) in parallel with two series capacitors where the anode of the upper diode is connected to the midpoint (neutral) of the capacitors and its cathode to the midpoint of the upper pair of switches; the cathode of the lower diode is connected to the midpoint of the capacitors and divides the main DC voltage into smaller voltage.

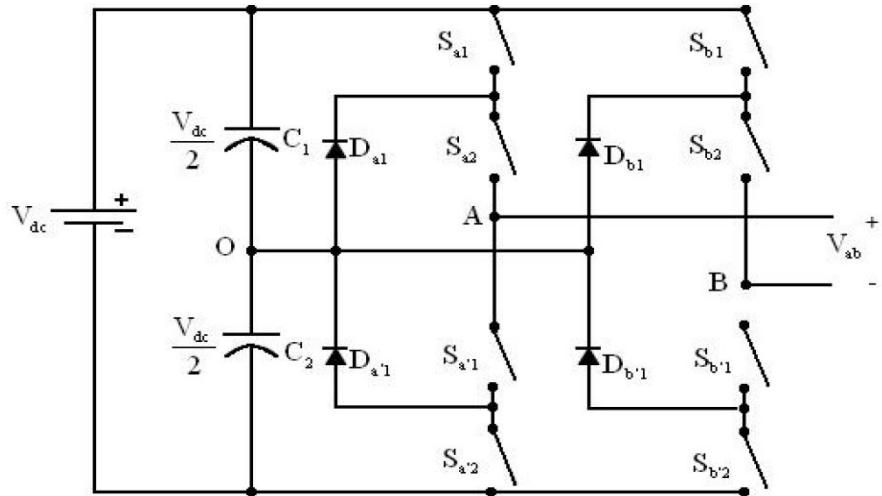


Figure 2.1: Two phase diode clamped multilevel inverter

The middle point of the two capacitors can be defined as the neutral point. The NPC uses a single dc bus that is subdivided into a number of voltage levels by a series string of capacitors. For a three-level diode-clamped inverter if the point O is taken as the ground

reference, the output voltage has three states 0, $+1/2V_{dc}$ and $-1/2V_{dc}$. The line-line voltages of two legs with the capacitors are: 0, $+1/2V_{dc}$, $-1/2V_{dc}$, $+V_{dc}$, $-V_{dc}$. Three phases are necessary to generate a three-phase voltage.

The disadvantages of this system are,

- (1) Different voltage ratings for clamping diodes are required.
- (2) Real power flow is difficult because of the capacitors imbalance.
- (3) Need high voltage rating diodes to block the reverse voltages.
- (4) The number of switches, capacitors, and diodes required in the circuit increases with the increase in the number of output voltage levels. Extra clamping diodes required are n 1 n 2 per phase.

2.2 Capacitor-Clamped Inverter

Capacitor-clamped multilevel inverter topologies are relatively new compared to the diode-clamped or the cascaded H-bridge cell inverter topologies. Redundancy in the switching states is available by using flying capacitors instead of clamping diodes. This redundancy can be used to regulate the capacitor voltages and obtain the same desired level of voltage at the output. Figure 2.2 shows a single-phase five-level capacitor-clamped multilevel inverter topology. The voltage across the capacitors is considered to be half of DC source voltage V_{dc} . The output voltage consists of five different voltage levels, 0, $+1/2V_{dc}$, $-1/2V_{dc}$, $+V_{dc}$, $-V_{dc}$. Similar to the other multilevel inverter topologies, capacitor clamped multilevel inverter also has complementary pairs of switches. The number of switching states for the capacitor-clamped multilevel inverter topology is higher than that of the diode-clamped inverter. The number of voltage levels at the output can be increased by adding a pair of complementary switches and a capacitor. An output voltage can be produced by using different combinations of switches. The topology allows increased flexibility in how the majority of the voltage levels may be chosen. In addition, the switches may be chosen to charge or discharge the clamped capacitors, which balance the capacitor voltage.

The disadvantages are,

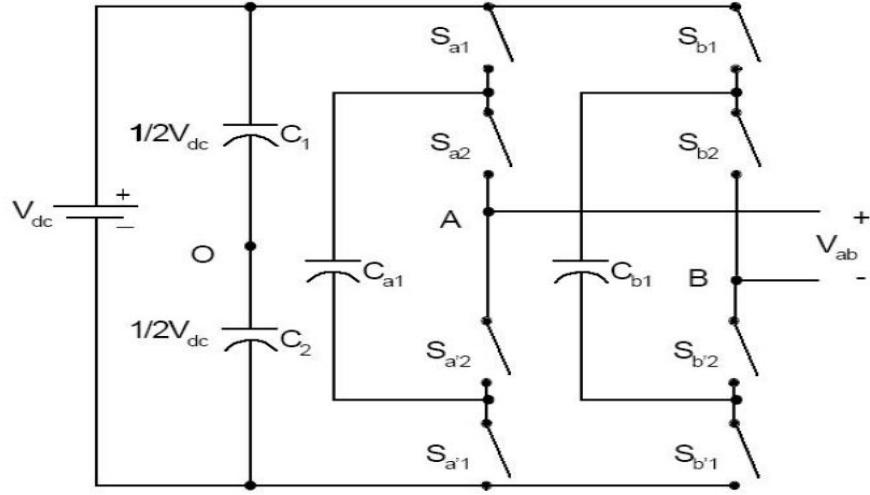


Figure 2.2: Capacitor-Clamped Multilevel Inverter

- (1) Large numbers of capacitors are bulky and more expensive than the clamping diodes used in the diode-clamped multilevel inverter.
- (2) Complex control is required to maintain the capacitors voltage balance.
- (3) Switching utilization and efficiency are poor for real power transmission.

2.3 Cascaded H-Bridge Inverter

The cascaded H-bridge inverter has drawn tremendous interest due to the greater demand of medium-voltage high-power inverters. The cascaded inverter uses series strings of single-phase full-bridge inverters to construct multilevel phase legs with separate dc sources. The output of each H-bridge can have three discrete levels, results in a staircase waveform that is nearly sinusoidal even without filtering. A single H-bridge is a three-level inverter. Each single-phase full-bridge inverter generates three voltages at the output: $+V_{dc}$, 0 and $-V_{dc}$. The four switches S_1 , S_2 , S_3 and S_4 are controlled to generate three discrete outputs out V with levels $+V_{dc}$, 0 and $-V_{dc}$. When S_1 and S_2 are on, the output is V_{dc} ; when S_3 and S_4 are on, the output is $-V_{dc}$.

- The disadvantage for cascaded multilevel H-bridge inverter is the following:
- (1) Needs separate DC sources.
 - (2) Needs large number of switches.

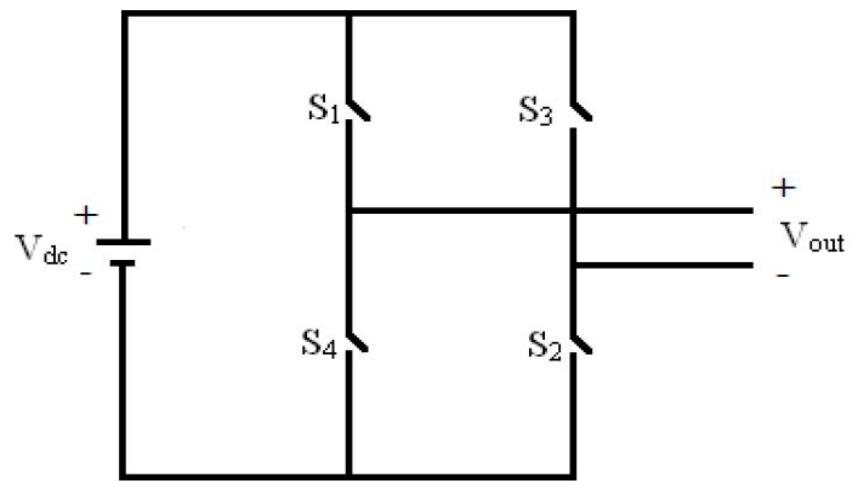


Figure 2.3: Single H-Bridge Topology

This project presents a multilevel inverter based on switched capacitance structure which can generate a greater number of voltage levels with optimum number of components.

Chapter 3

SWITCHED CAPACITOR NINE LEVEL INVERTER

This chapter discusses the working of a switched capacitor based nine level inverter with reduced switch count and a single DC source. It also explains the phase disposition PWM technique used to generate the switching signals for the inverter.

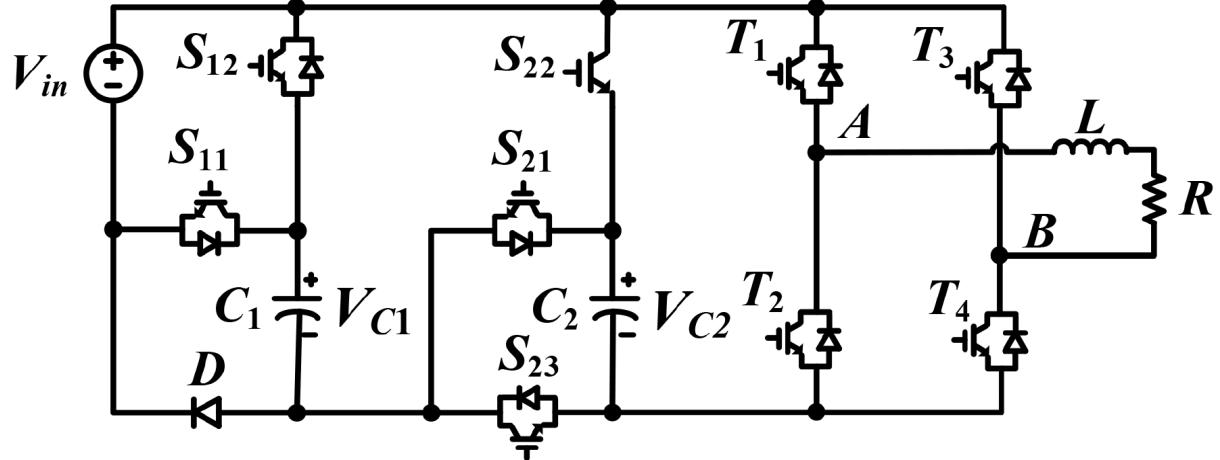


Figure 3.1: Switched Capacitor 9-level inverter circuit

The proposed inverter consists of a single DC source, two SC cells connected in parallel with the H-bridge circuit and a load. The first SC cell is a combination of one capacitor, one diode, and two switches ($C_1 - D - S_{11} - S_{12}$), and the second SC cell includes one capacitor, and three switches ($C_2 - S_{21} - S_{22} - S_{23}$). Switched capacitor

is the most famous voltage boosting technique. This technique uses capacitor in conjunction with power semiconductor switches. A voltage doubler is an electronic circuit which charges capacitors from the input voltage and switches these charges in such a way that, in the ideal case, exactly twice the voltage is produced at the output as at its input. The simplest of these circuits are a form of rectifier which take an AC voltage as input and outputs a doubled DC voltage. The switching elements are simple diodes and they are driven to switch state merely by the alternating voltage of the input. DC-to-DC voltage doublers cannot switch in this way and require a driving circuit to control the switching. They frequently also require a switching element that can be controlled directly, such as a transistor, rather than relying on the voltage across the switch as in the simple AC-to-DC case. Cascading identical stages together achieves a greater voltage multiplication. A comparison of the number of components used in realising a 9 level inverter using switched capacitor structure and other conventional topologies are summarised in the table below.

Topology	Capacitor	Diode	Switch	DC Source
Switched Capacitor MLI	2	2	9	1
Diode clamped MLI	8	28	32	1
Flying Capacitor MLI	64	0	32	1
Cascaded H-Bridge MLI	0	0	16	4

Table 3.1: Comparison of the number of components in a 9 level inverter

3.1 Switched Capacitor Structure

Capacitor C_1 is charged while connected in parallel with the input source through S_{12} . It is discharged in series with the input source through S_{11} . Capacitor C_2 is charged in parallel from the input source and capacitor C_1 through S_{22} and S_{23} . It is discharged in series with capacitor C_1 and the input source through S_{21} . C_1 is thus charged to V_{in} and C_2 is charged to $2V_{in}$. Four Levels of voltage (in addition to a zero level) are therefore obtained by the following combinations:-

In mode 1, the voltage across C_1 and that of voltage source V_{in} are equal and parallel.
In mode 2, the voltage source V_{in} and the voltage across C_1 (which is V_{in}) are connected in

MODE	OUTPUT VOLTAGE	STATE
1	V_{in}	Source and C_1 in parallel.
2	$2V_{in}$	Source and C_1 in series, then parallel with C_2 .
3	$3V_{in}$	Source and C_1 in parallel, then series with C_2 .
4	$4V_{in}$	Source, C_1 and C_2 all in series.

Table 3.2: Output voltage states

series due to the configuration and switching ON of the corresponding switches. Thus, the second output voltage stage, i.e. $2V_{in}$ is obtained. In mode 3, the voltage source V_{in} and the capacitor C_1 are in parallel which makes the effective voltage across the parallel block to be V_{in} . The capacitor was charged to a voltage of $2V_{in}$ in the previous cycle. Hence, a series connection between the parallel block and the capacitor C_2 produces the additive sum of the parallel block and the capacitor C_2 to produce a voltage $3V_{in}$. In mode 4, the voltage source V_{in} and the capacitor C_1 are in series which produces a voltage equal to $2V_{in}$ in the series network. This network is connected in series with capacitor (charged to voltage $2V_{in}$). The cumulative voltage across the series connected networks is $4V_{in}$, which appears as the fourth voltage stage.

3.2 Modes of Operation

In mode 1, the voltage across C_1 and that of voltage source V_{in} are equal and parallel. Hence, the total voltage that is produced across the load is same as V_{in} . This is the first output voltage stage.

In mode 2, the voltage source V_{in} and the voltage across C_1 (which is V_{in}) are connected in series due to the configuration and switching ON of the corresponding switches. This results in additive sum of the voltage source and the capacitor C_1 , i.e. $2V_{in}$ to appear across the load. Thus, the second output voltage stage, i.e. $2V_{in}$ is obtained.

In mode 3, the voltage source V_{in} and the capacitor C_1 are in parallel which makes the effective voltage across the parallel block to be V_{in} . The capacitor was charged to a voltage of $2V_{in}$ in the previous cycle. Hence, a series connection between the parallel block

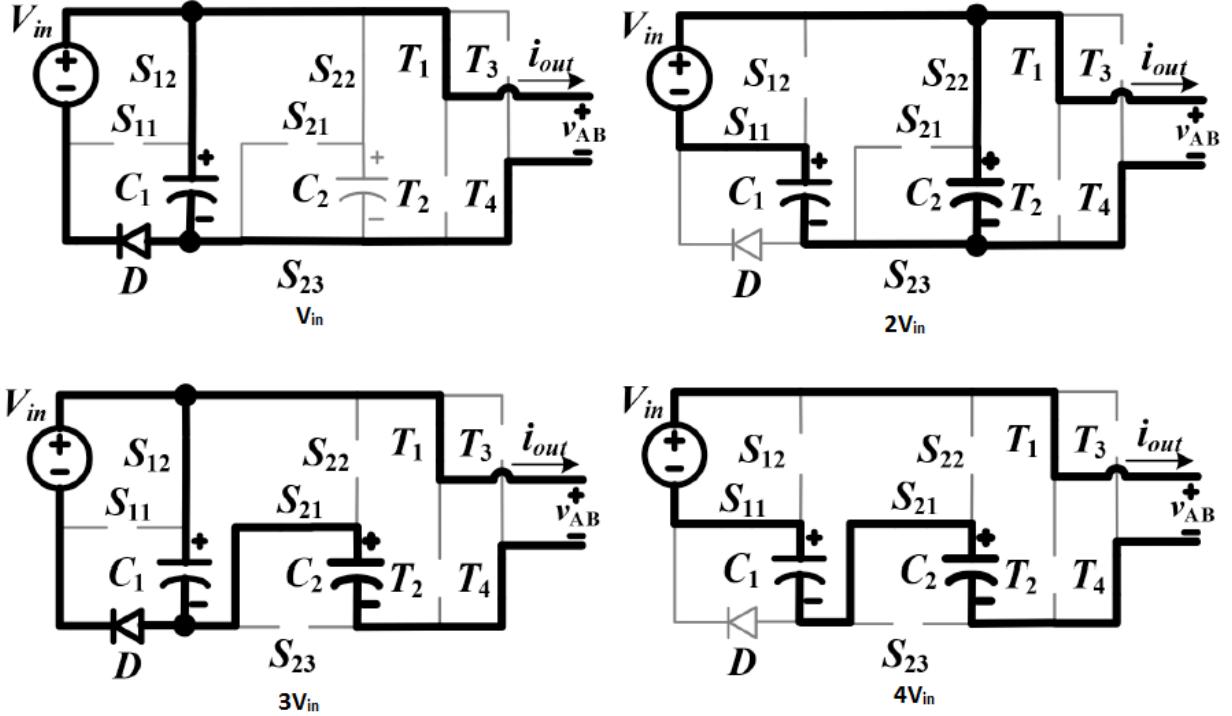


Figure 3.2: Modes of operation

and the capacitor C_2 produces the additive sum of the parallel block and the capacitor C_2 to produce a voltage across the load. This voltage $3V_{in}$ is the third voltage stage in the inverter output.

In mode 4, the voltage source V_{in} and the capacitor C_1 are in series which produces a voltage equal to $2V_{in}$ in the series network. This network is connected in series with capacitor (charged to voltage $2V_{in}$). The cumulative voltage across the series connected networks is $4V_{in}$, which appears as the fourth voltage stage.

These four levels of voltage can be reversed in polarity at the output by the H-Bridge. Therefore there are 9 different voltage levels ($4 * 2 + 1$) available at the output of the inverter. The switching states are controlled by Phase disposition PWM (PD-PWM).

3.3 Switching States

MODE	OUTPUT VOLTAGE	STATE
1	V_{in}	Source and C_1 in parallel.
2	$2V_{in}$	Source and C_1 in series, then parallel with C_2 .
3	$3V_{in}$	Source and C_1 in parallel, then series with C_2 .
4	$4V_{in}$	Source, C_1 and C_2 all in series.

Table 3.3: Output voltage states

In the positive half cycle T_1 and T_4 are fully turned on whereas T_2 and T_3 are fully turned OFF. Similarly, in the negative period, T_2 and T_3 are fully turned on whereas T_1 and T_4 are fully turned OFF and the components of the SC cells are similar to those in the positive period. To achieve zero voltage output T_1 and T_3 are turned on simultaneously.

MODE	OUTPUT VOLTAGE	D	S_{11}	S_{12}	S_{23}	S_{22}	S_{21}
1	V_{in}	ON	OFF	ON	ON	ON	OFF
2	$2V_{in}$	OFF	ON	OFF	ON	ON	OFF
3	$3V_{in}$	ON	OFF	ON	OFF	OFF	ON
4	$4V_{in}$	OFF	ON	OFF	OFF	OFF	ON

Table 3.4: Switching states

3.4 Phase Disposition PWM

Carrier based disposition PWM methods were first proposed by Carrara et al. These techniques can be efficiently applied for Diode Clamped and Cascaded Multilevel Inverters. The main classification of carrier based PWM techniques are Phase shifted carrier PWM and Carrier disposition PWM. Most of the carrier based PWM techniques have been derived from the classical carrier disposition strategies. The phases of carrier signals are rearranged to produce three main disposition techniques known as PD, POD and APOD. Carrier Disposition method arranges N-1 carrier waveforms of same amplitude and frequency in continuous bands to fully occupy the linear modulation range of

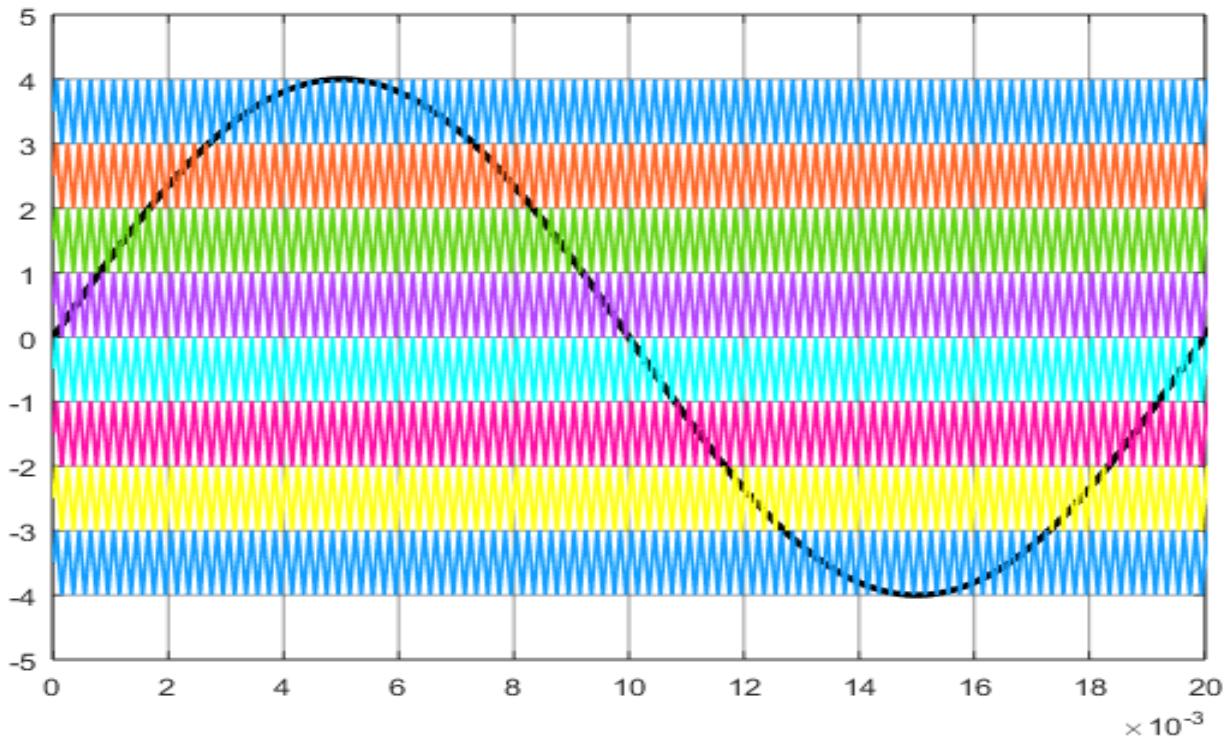


Figure 3.3: Phase Disposition PWM Scheme

the inverter. The reference or modulating wave is positioned at the centre of the carrier set, and continuously compared with the carriers. Whenever the magnitude of reference wave is greater than a carrier wave, positive going switching pulse is obtained. When the reference goes above all the carriers maximum output is obtained. As the reference falls below each carrier the corresponding levels in the inverter output gets reduced.

Switching scheme used in this inverter is phase disposition pulse width modulation. Eight level-shifted triangular carrier signals are modulated using a single sine wave. All triangular waves are in phase. The amplitude of the sine wave is 4 units. Each triangular wave is level-shifted by 1 unit corresponding to each output level.

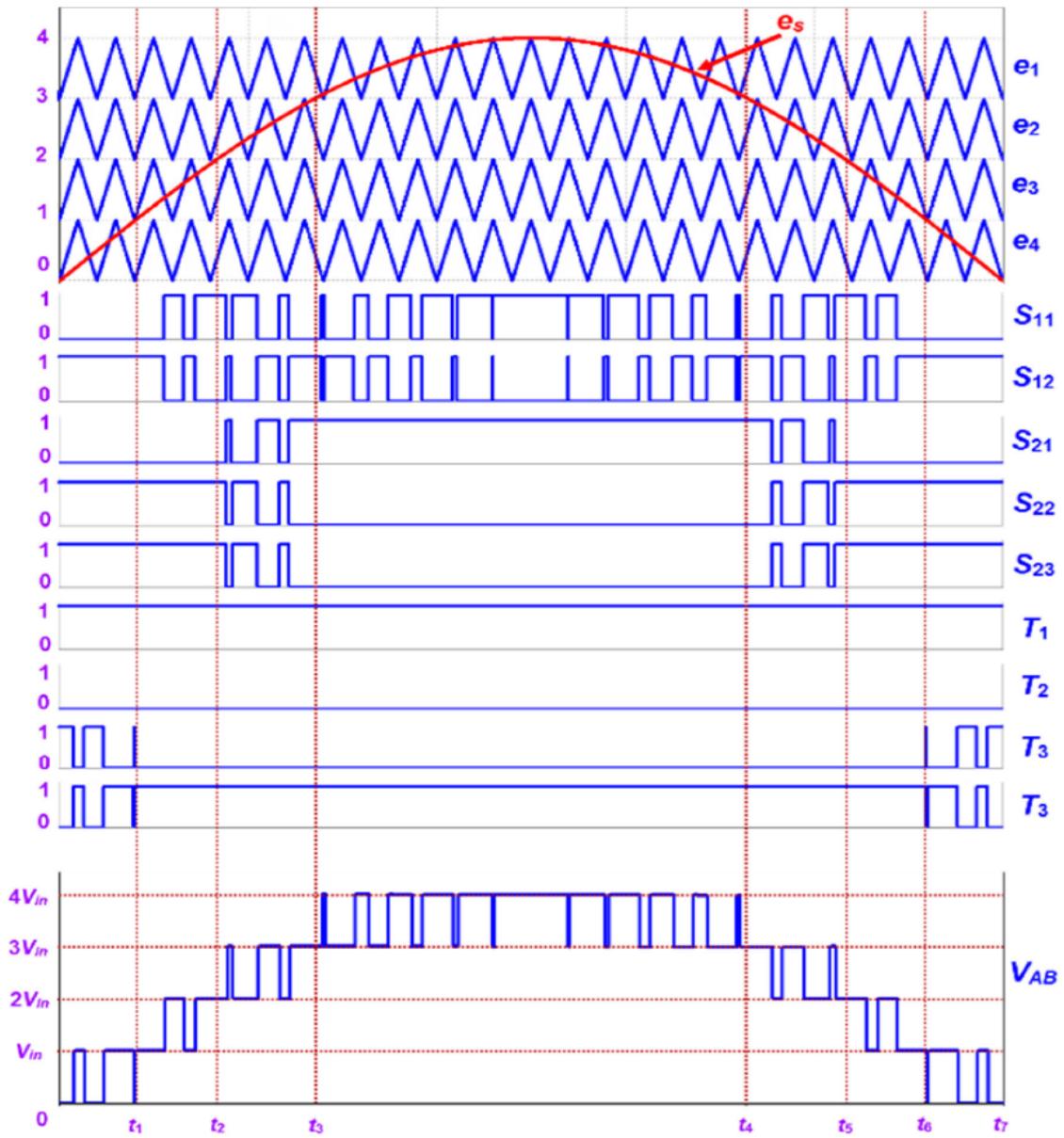


Figure 3.4: Switching diagram

Chapter 4

SIMULATION RESULTS

This chapter discusses about the simulation model of the nine level inverter based on switched capacitor structure. Further the analysis of the simulink model is also given.

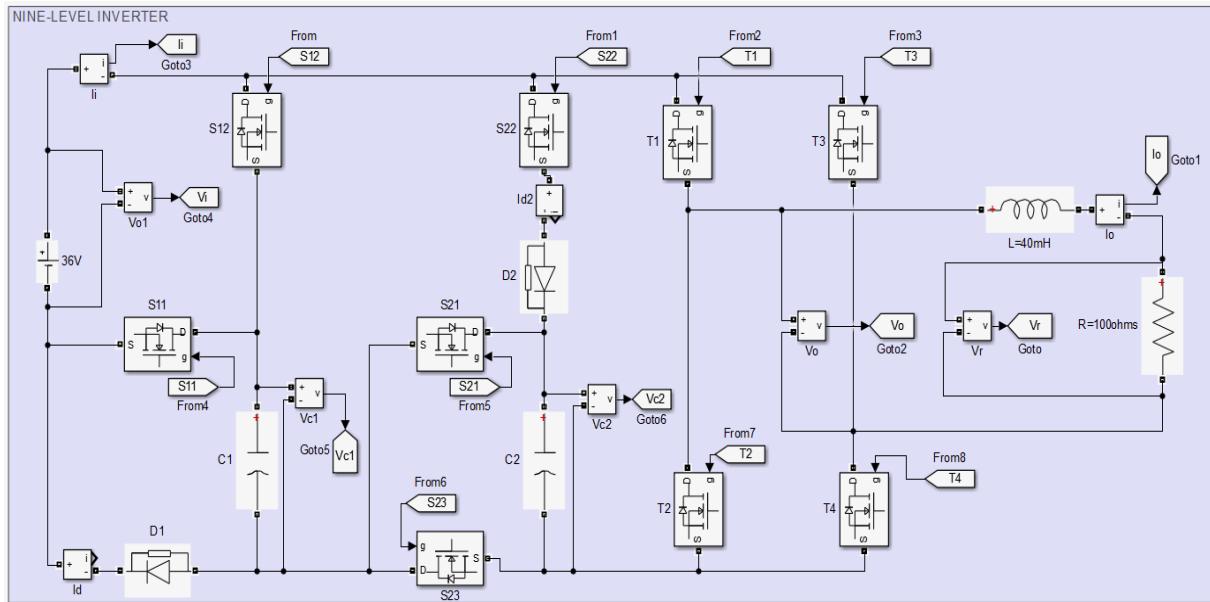


Figure 4.1: Simulink circuit

The simulation of the NINE-LEVEL INVERTER was done using the simulink tool in matlab. Operation of the inverter was verified with R and R-L load. Gating pulses are derived using PD-PWM technique. The switching delay and gate delay are neglected. The design consideration are given in the table below.

PARAMETER	VALUE
V_{in}	36V
V_{out}	100V
Power Rating	100W
C_2	$2400\mu F$, 180V
C_2	$3600\mu F$, 180V
Load($R + jX$)	$100 + j12$
Carrier frequency	5000KHz
Modulation	50Hz
Switching scheme	PDPWM

Table 4.1: Simulation specification

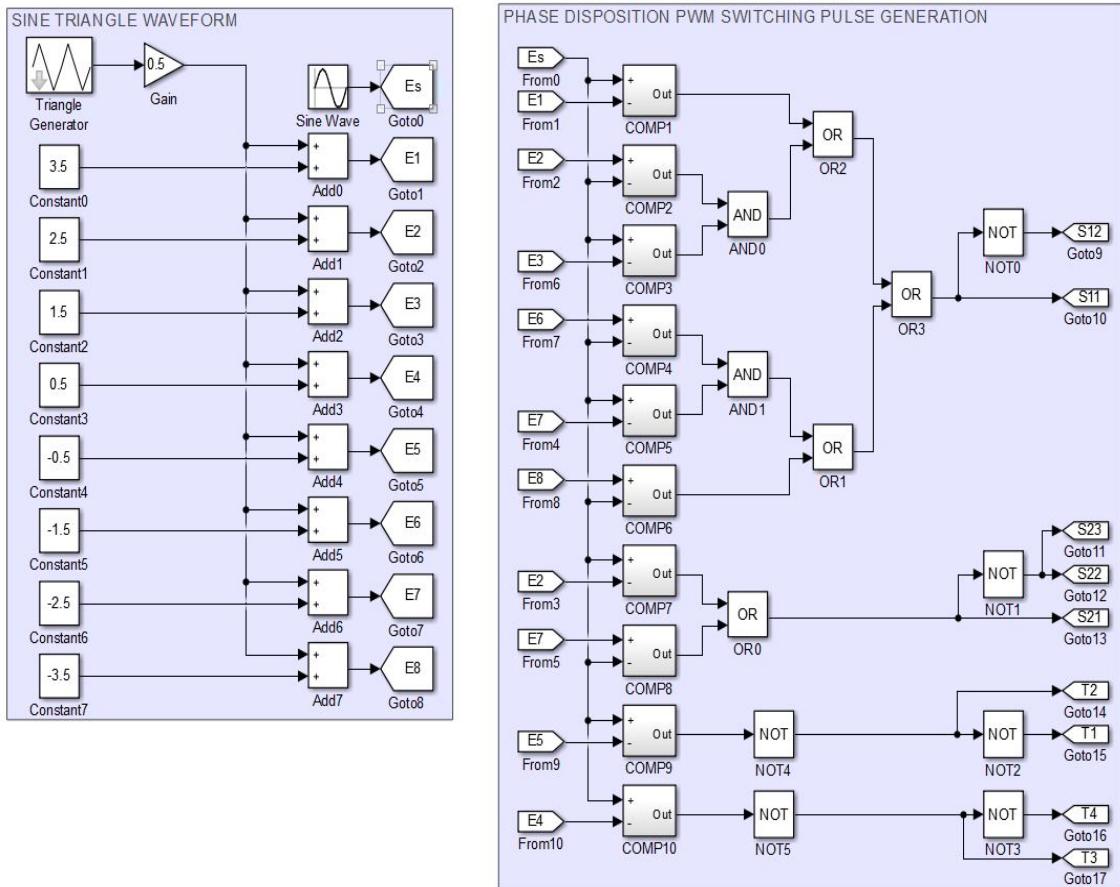


Figure 4.2: Simulink Pulse Derivation

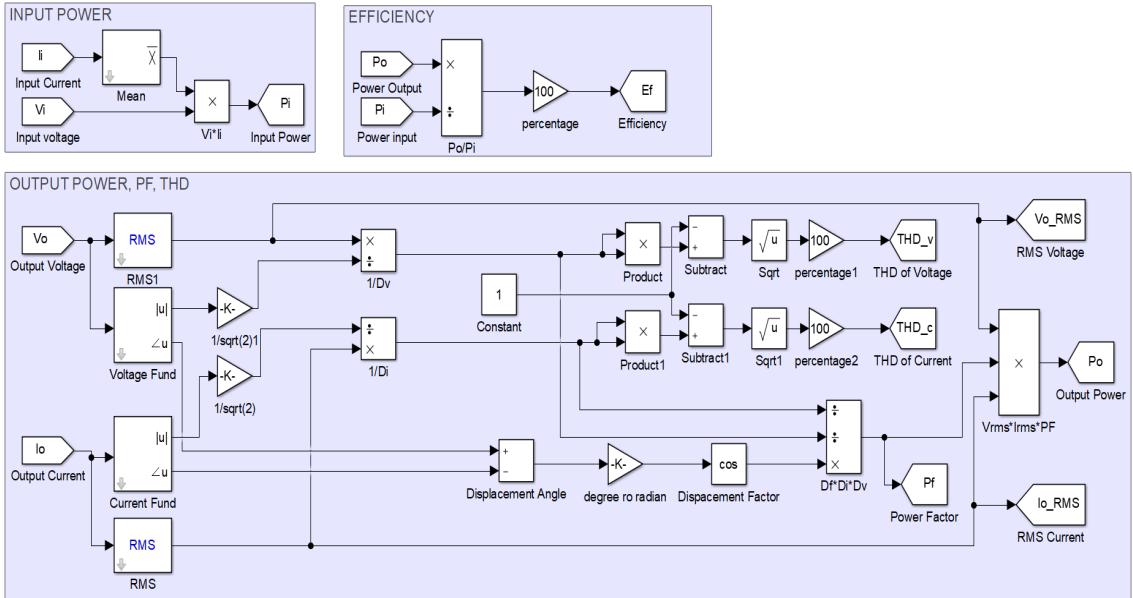


Figure 4.3: Measurement Block

4.1 Result

The output of the simulink simulation is shown in the following figures. Figure 4.5 shows the output voltage, capacitor voltage and current. Figure 4.4 shows the analysis after measurement of various inverter parameters. The peak voltage output of the inverter is 144V. The RMS value of output voltage is 100V. The RMS value of output current is 1A. The capacitor voltage is nearly constant with neglegible ripple. The model is found to meet the expected design power outout of 100Watts.

4.1.1 Peak Inverse Voltage(PIV)

The voltag stress across the switches S_{11} and S_{12} are V_{in} where V_{in} is the input dc voltage. The voltage stress across the switches S_{21} , S_{22} and S_{23} are $2V_{in}$. The voltage stress across the switches of H-bridge T_1 , T_2 , T_3 and T_4 are $4V_{in}$. The peak load voltage is $4V_{in}$.

4.1.2 Total Harmonic Distortion(THD)

The output voltage waveform for a load resistance of $Z_L = 100\Omega$ and its FFT analysis is shown in figure 4.6. It's THD is found to be 13.92%. The output voltage waveform for a load resistance of $Z_L = 100\Omega + j12\Omega$ and its FFT analysis is shown in figure 4.7. It's THD is found to be 1.013%.

4.1.3 Efficiency

Efficiency of the switched capacitor nine-level inverter for a load of $Z_L = 100\Omega + j12\Omega$ is found to be 95.37% for a power output of 100W.

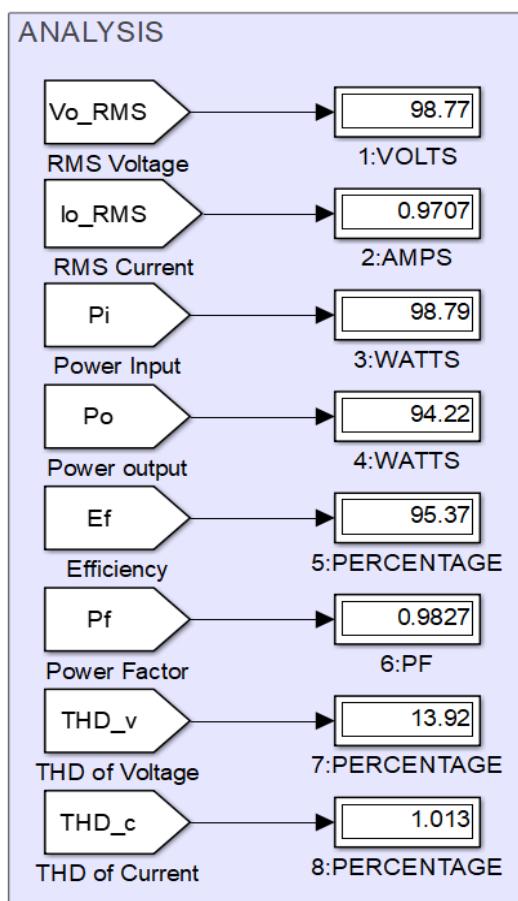


Figure 4.4: Simulink analysis

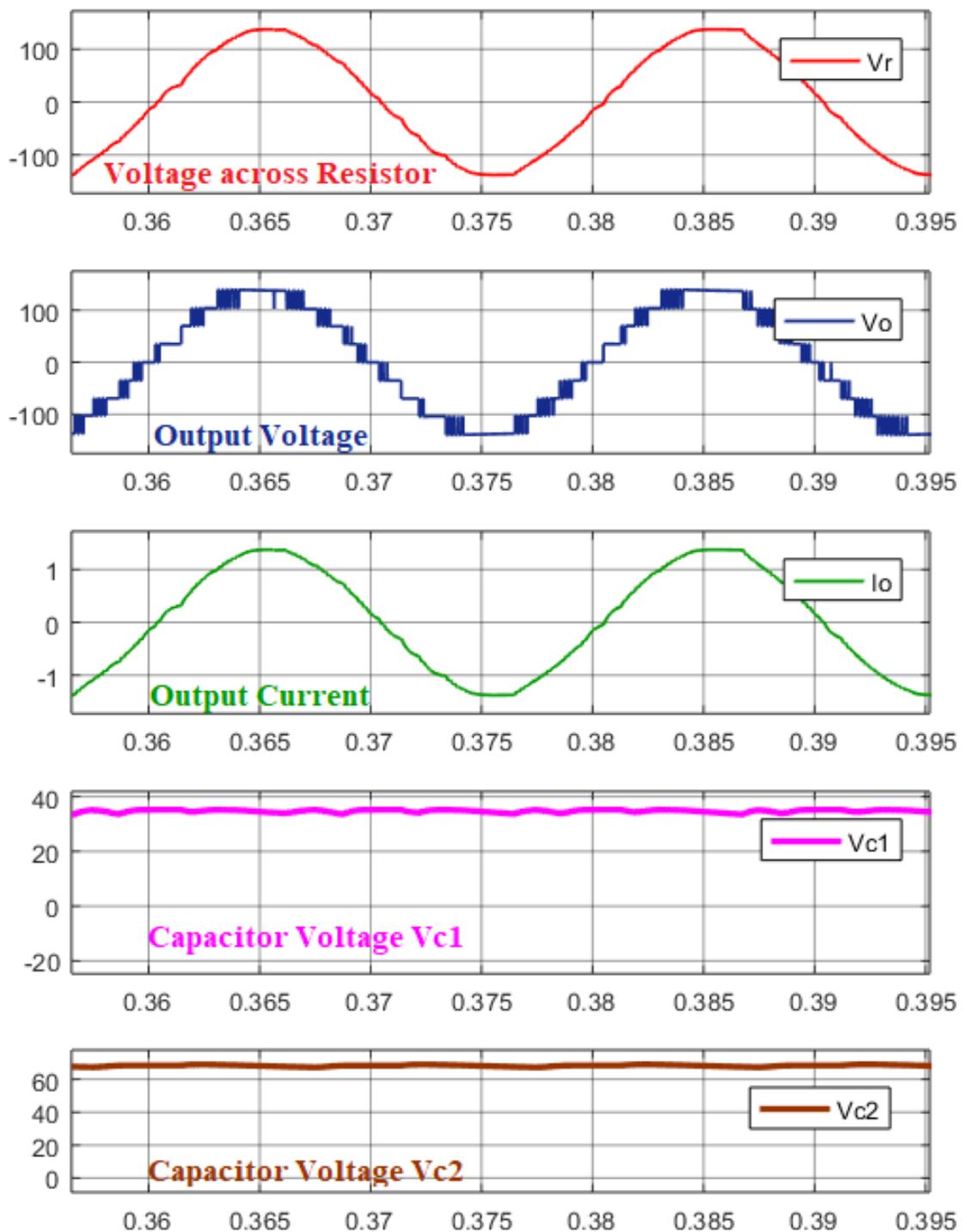


Figure 4.5: Simulink Output

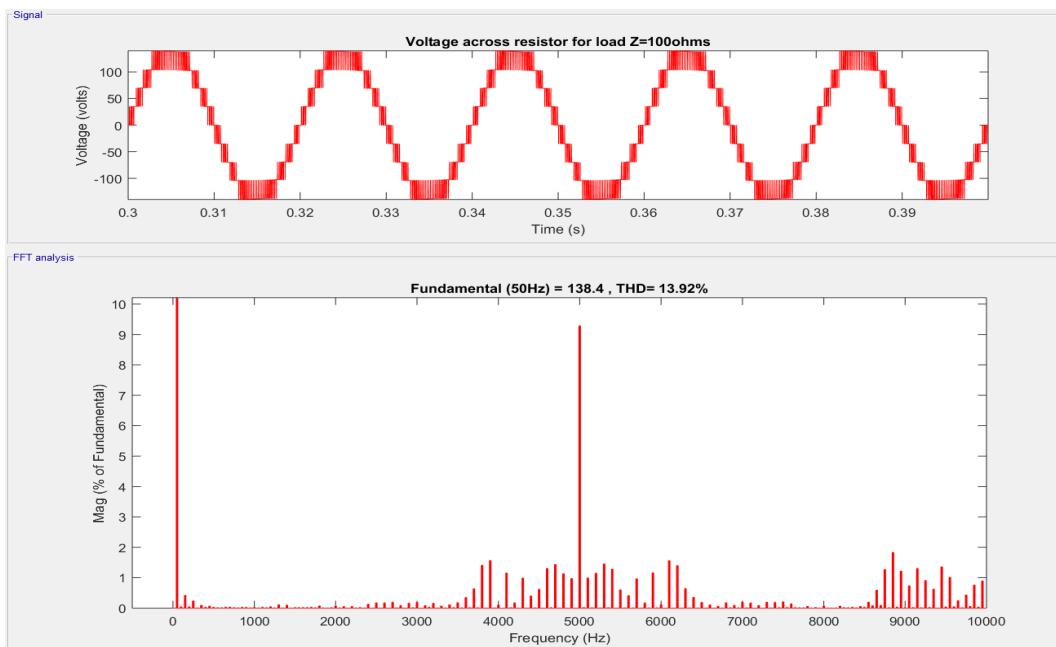


Figure 4.6: Simulink FFT analysis with R load

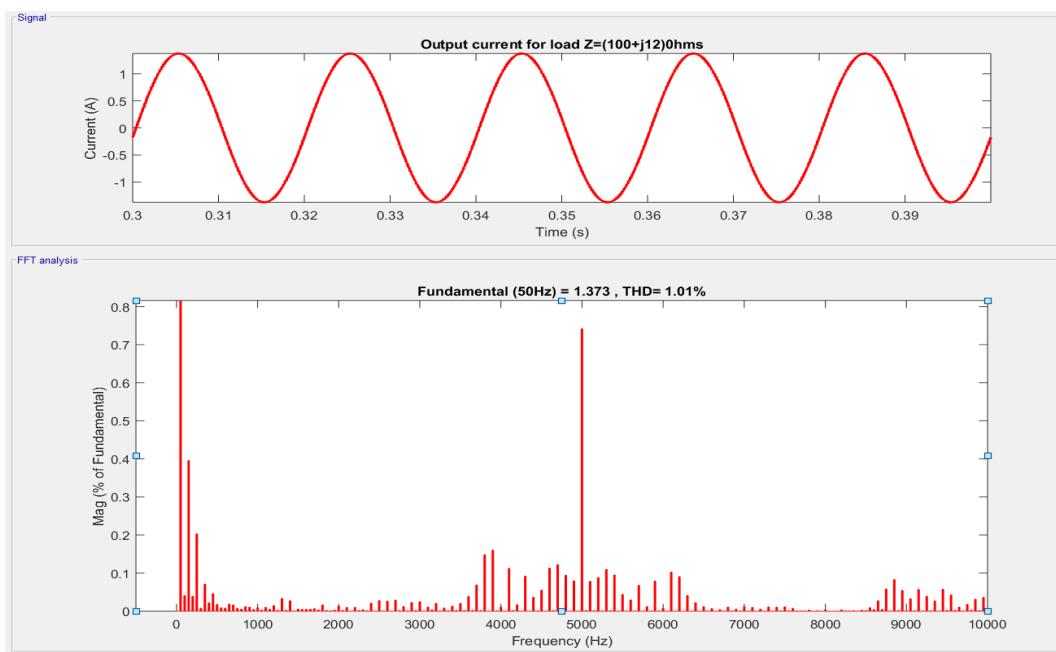


Figure 4.7: Simulink FFT analysis with RL load

Chapter 5

HARDWARE IMPLEMENTATION AND RESULTS

This chapter discusses in detail about the hardware implementation of the nine level inverter based on switched capacitor structure. The components used in realization are explained in detail. Various stages of the work like PCB realization etc are also included. The following table summarises the hardware specifications of the project.

PARAMETER	VALUE
V_{in}	36V
V_{out}	100V
Power Rating	100W
Switch Used	MOSFET IRFP460
Diode	MUR460
MOSFET Drives	TLP250
C_2	$2400\mu F$, 180V
C_2	$3600\mu F$, 180V
Carrier frequency	5000KHz
Modulation	50Hz
Switching scheme	PDPWM
Switching pulse realisation	DSPIC30F2020

Table 5.1: Hardware specification

5.1 MOSFET IRFP460

Third Generation HEXFETs from international Rectifier provide the designer with the best combination of fast switching ruggedized device design, low on-resistance and cost-effectiveness. The TO-247 package is preferred for commercial industrial applications where high power levels preclude the use of TO-220 devices. It also provides greater creepage between pins to meet the requirements of most safety specifications.

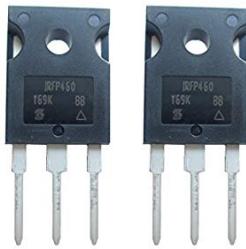


Figure 5.1: IRFP460

V_{DSS}	500V
V_{GS}	2 – 4V
$R_{DS(on)}$	0.27ohm
$t_{d(on)}$	18ns
$t_{d(off)}$	110ns
I_s	20A

Table 5.2: IRFP460 Specs

5.2 MUR460

MUR460 is designed for use in switching power supplies, inverters and as free-wheeling diodes. These devices have the following features:

Peak Reverse Voltage	600V
Average Forward Current	4A
Reverse Recovery Time	75nS
Forward Recovery Time	50nS

Table 5.3: MUR460 Specs



Figure 5.2: MUR460

1. 175 ° C operating junction temperature
3. Low forward voltage
4. Low leakage current
5. High temperature glass passivated junction

5.3 DSPIC30F2020

28-Pin SDIP and SOIC

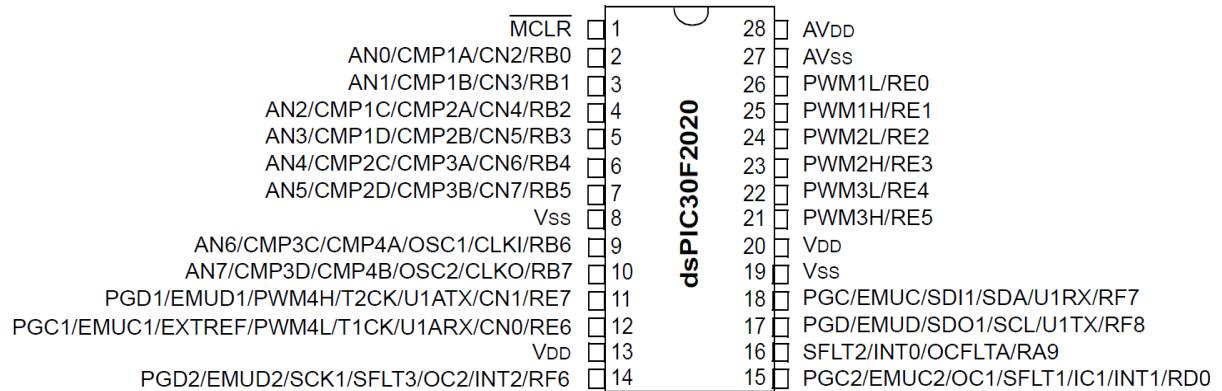


Figure 5.3: DSPIC30F2020 Pin diagram.

High-Performance Modified RISC CPU:

- Modified Harvard architecture
- C compiler optimized instruction set architecture
- 83 base instructions with flexible addressing modes.
- 24-bit wide instructions, 16-bit wide data path
- 12 Kbytes on-chip Flash program space
- 512 bytes on-chip data RAM
- 16 x 16-bit working register array.
- Up to 30 MIPS operation:
 - Dual Internal RC
 - 9.7 and 14.55 MHz
 - 6.4 and 9.7 MHz

- 32X PLL with 480 MHz VCO
- PLL inputs
- External EC clock 6.0 to 14.55 MHz
- HS Crystal mode 6.0 to 14.55 MHz

- 32 interrupt sources
- Three external interrupt source
- 8 user-selectable priority levels for each interrupt.
- 4 processor exceptions and software traps.

Power Supply PWM Module Features:

- Four PWM generators with 8 outputs
- Each PWM generator has independent time base and duty cycle
- Duty cycle resolution of 1.1 ns at 30 MIPS
- Individual dead time for each PWM generator:
 - Dead-time resolution 4.2 ns at 30 MIPS
 - Dead time for rising and falling edges
- Phase-shift resolution of 4.2 ns @ 30 MIPS
- Frequency resolution of 8.4 ns @ 30 MIPS
- PWM modes supported: - Complementary
 - Push-Pull
 - Multi-Phase
 - Variable Phase
 - Current Reset
 - Current-Limit
- Independent Current-Limit and Fault Inputs
- Output Override Control

- Special Event Trigger
- PWM generated ADC Trigger

DSPIC30F2020 is programmed so as to produce driving signals to the switches in the inverter circuit. The DSPIC30F2020 also has PWM capabilities which can be operated by giving basic values like the duty cycle.

5.4 Gate Driver Opto Coupler

The TLP250 consists of a GaAlAs light emitting diode and an integrated photo detector. The unit is an 8-lead DIP package. TLP250 is suitable for gate-driving circuit of IGBT or power MOSFET.

Input Threshold current	$5mA$
Input Reverse Voltage	$5V$
Operating frequency	$25KHz$
Junction Temperature	$125^{\circ}C$
Isolation Voltage	$2500V$
Supply Current	$11mA$
Supply Voltage	$10V - 35V$
Output Current	$1.5A$
Switching time	$1.5\mu S$

Table 5.4: TLP250 Specs

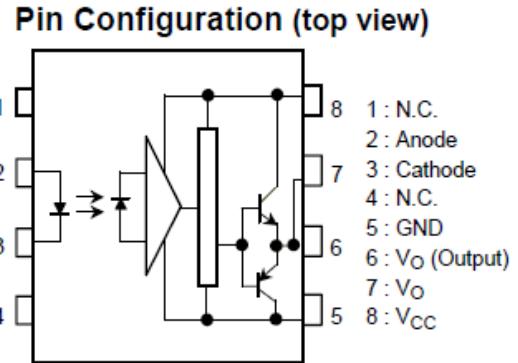


Figure 5.4: TLP250 Pin Configuration

The TLP250 plays an important role in the inverter circuit. It is used to produce high-voltage pulses as supplied to it such that the input pulse is electrically isolated from the output. The input section consists of an LED. The gate pulse of $5V$ is dropped to the LED driving voltage using a resistor. The output stage consists of a photo detector and transistors in totem-pole structure. When a gate pulse is supplied to the input stage, the LED is illuminated in the ON stage and otherwise in the OFF stage. This produces corresponding pulse signal in the output using the photo detector of amplitude equal to the gate drive power supply which in this case is $15V$.

5.5 Gate Power Supply

The 15 V pulse is necessary to drive IRFP460 since the output voltage from the DSPIC is insufficient to drive the high power switch. The 15 V pulse is obtained using the Gate driver optocoupler which requires a voltage input of 15V called Gate Driver Power Supply. The Gate driver power supply circuit consists of 10 output configurations consisting of a transformer, regulator configuration. The driving circuit is fired using the gate pulse. The transformer is wound with 46 turns in the primary and 37 in the secondary so that an input signal of 24 Volt can be transformed into 20 V.

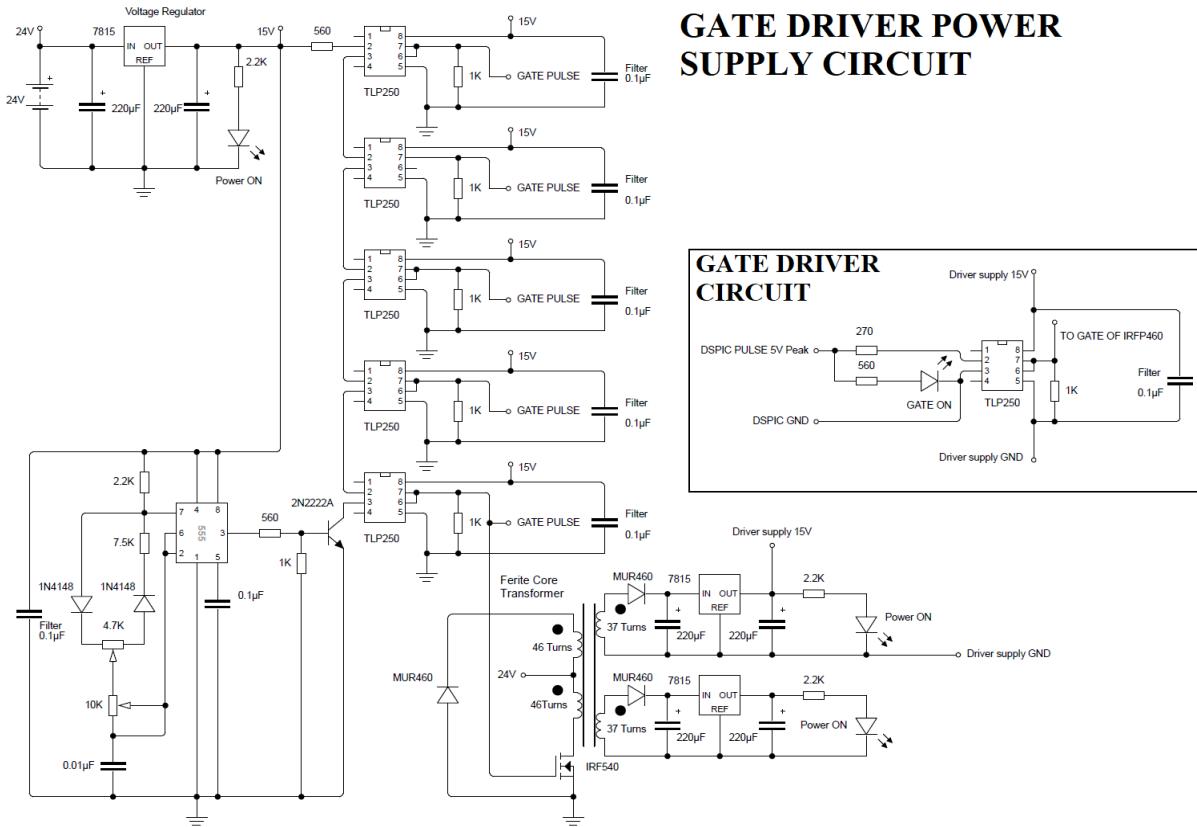


Figure 5.5: Gate Driver Power Supply Circuit

When the pulse is high, the IRF540 is ON. Hence, the voltage of 24 Volt is induced on both the primaries of the transformer. A voltage almost equal to 20V is then induced on the secondary windings according to dot convention. This signal is then filtered, regulated to 15 V and filtered once again to produce the supply. In the OFF state of the

IRF540, the presence of the MUR460 diode allows the flow of the remaining energy stored back to the supply, thus completing the circuit. Ten similar configurations produce 10 sources of 15 V each which are isolated from each other. Out of these, 9 sources are used to drive the TLP250 in the inverter circuit whereas one of them is used to drive the DSPIC. The gate pulse to drive the IRF540 switch is obtained by using a 555 IC timer network. The IC network is so designed that adjusting the 10k pot helps to vary the duty cycle and the 4.7k pot can be used to vary the time period and thereby frequency.

5.6 PCB Realization

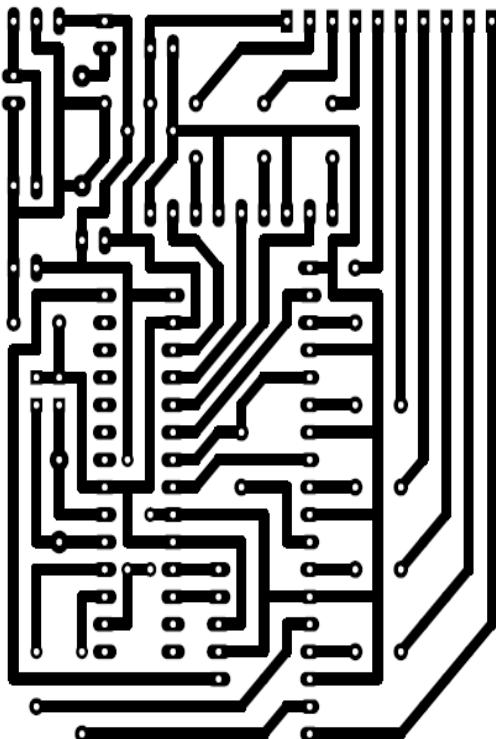


Figure 5.6: DSPIC Board Design

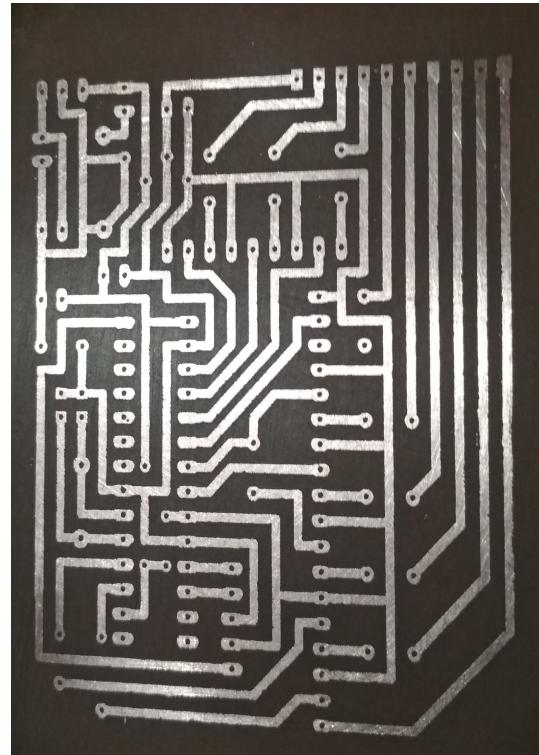


Figure 5.7: DSPIC Board PCB Realisation



Figure 5.8: Inverter Realisa-
tion

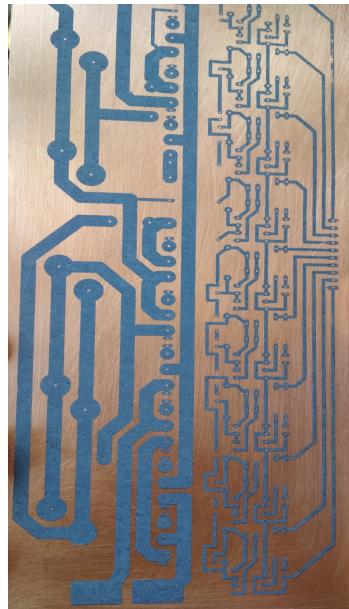


Figure 5.9:
PCB Toner
Transfer

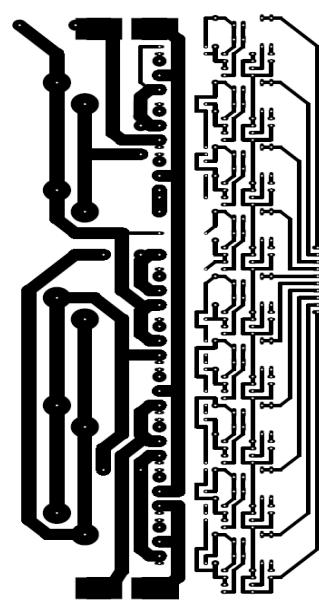


Figure 5.10:
Inverter PCB
Design

All the required circuits are etched on a copper plate by displacement method using $FeCl_3$ solution. This involves marking the tracks on the copper plate using either toner transfer method which involves the transfer of printed ink on glossy paper into the copper plate. This plate is then placed in a $FeCl_3$ bath and agitated till the Cu from the non-painted region is eroded. This produces proper Cu tracks on the board. Necessary holes are pierced on the board so that necessary elements can be fixed on the same.

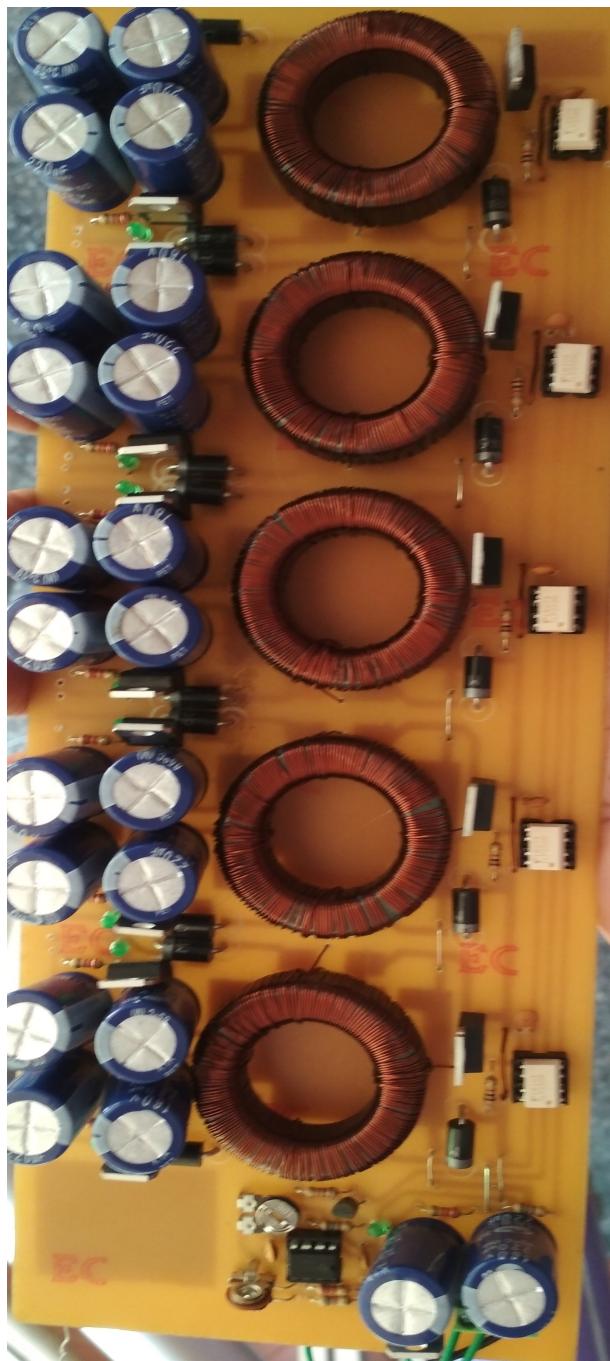


Figure 5.11: Driver Supply Realization

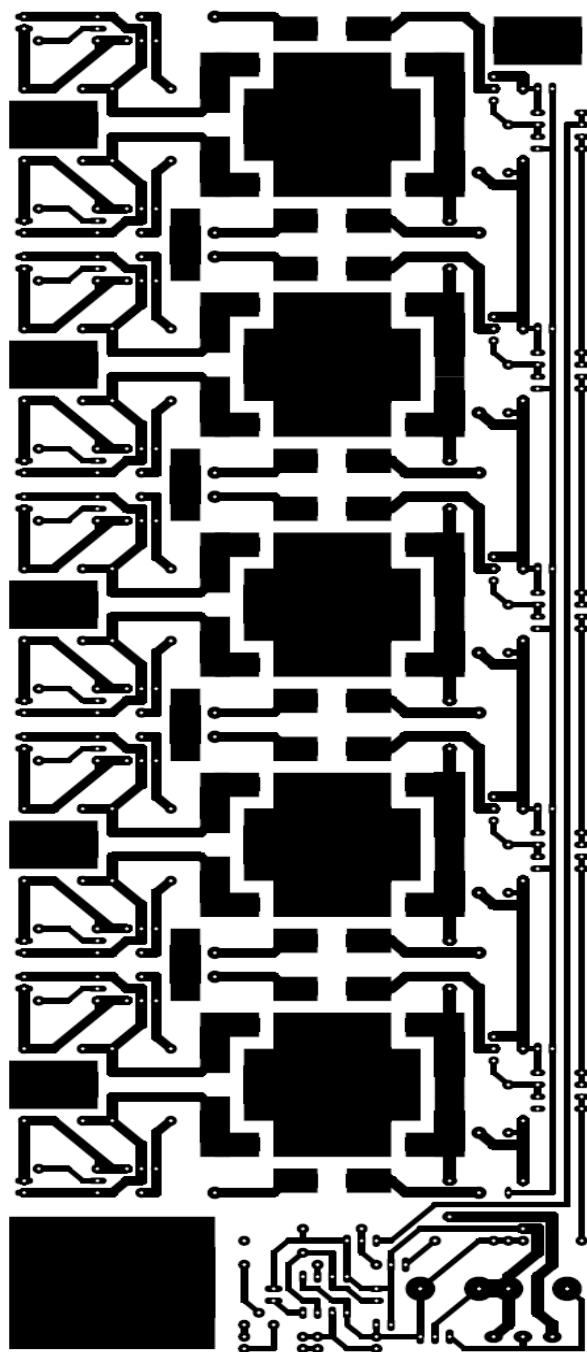


Figure 5.12: Driver Supply PCB Design

5.7 Hardware Realization

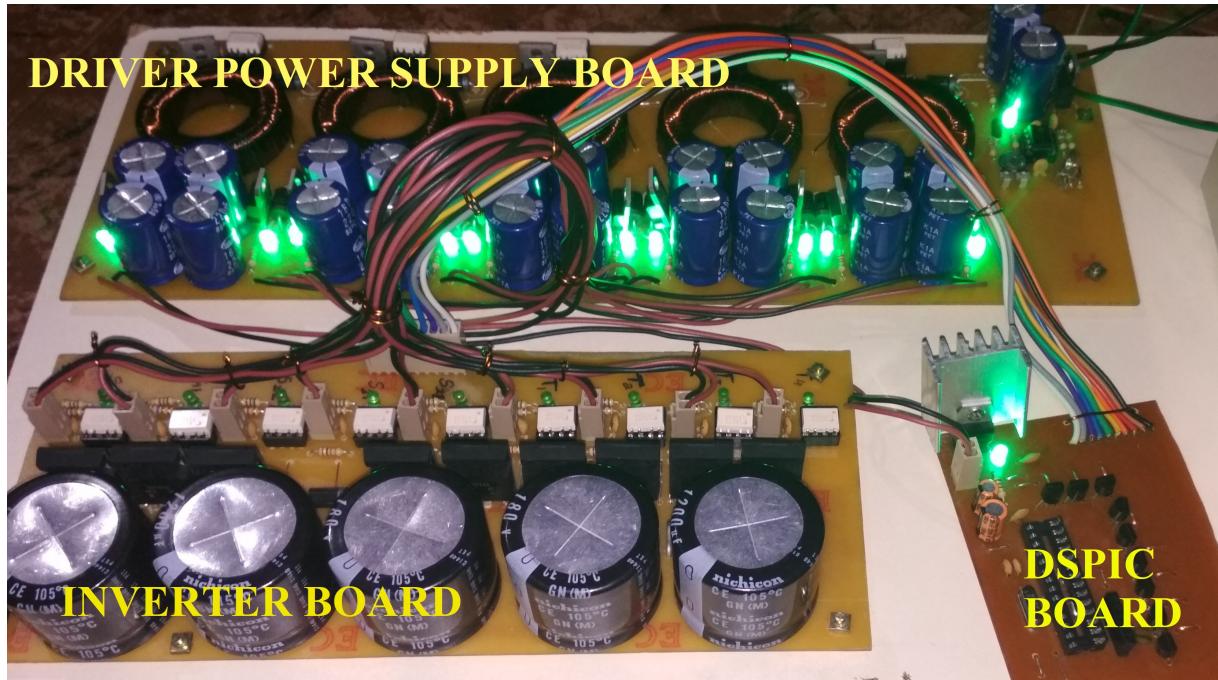


Figure 5.13: Nine level inverter hardware

The hardware realisation consists of the integration of 3 circuits, namely:

1. Driver power supply board.
2. Inverter board.
3. DSPIC Board.

The driver power supply board takes the 24 V supply from the source and then converts it into 20V and is then further regulated to obtain 15V output. The 15V output of the driver power supply board acts as the source of power for the 9 TLP250 optocoupler circuits and a DSPIC. 9 separate sources are required because using a common source for multiple switches may produce internal short circuit through the source and the connected switches. The inverter board takes 36 Voltage input and converts it into 9 level PWM signal. The TLP250 are used since the IRFP460 requires high power to switch ON which cannot be provided by the output of the DSPIC.

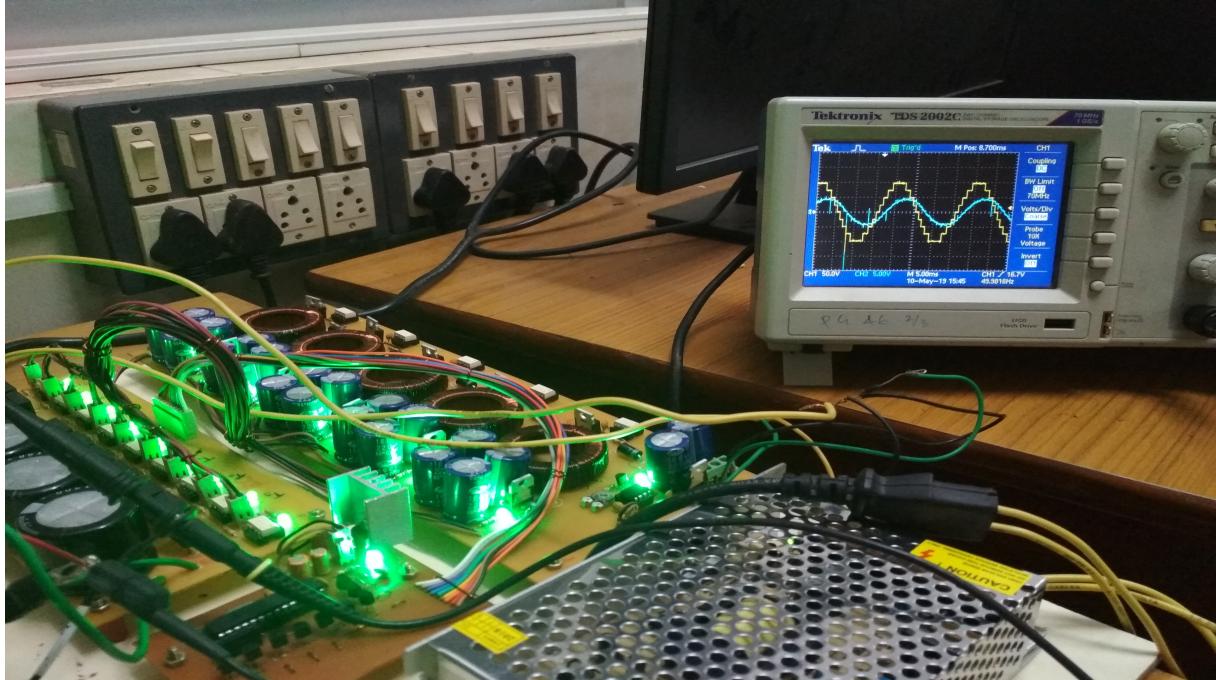


Figure 5.14: Hardware

The DSPIC30F2020 is programmed to excite the switches in the inverter depending upon the way in which it is programmed. The DSPIC30F2020 produces voltage in the output pins in the range of 5V which is given to TLP250 where the 5V pulse is converted into 15V pulses by the 15V input given to the TLP250 from the driver power circuits.

5.8 Results

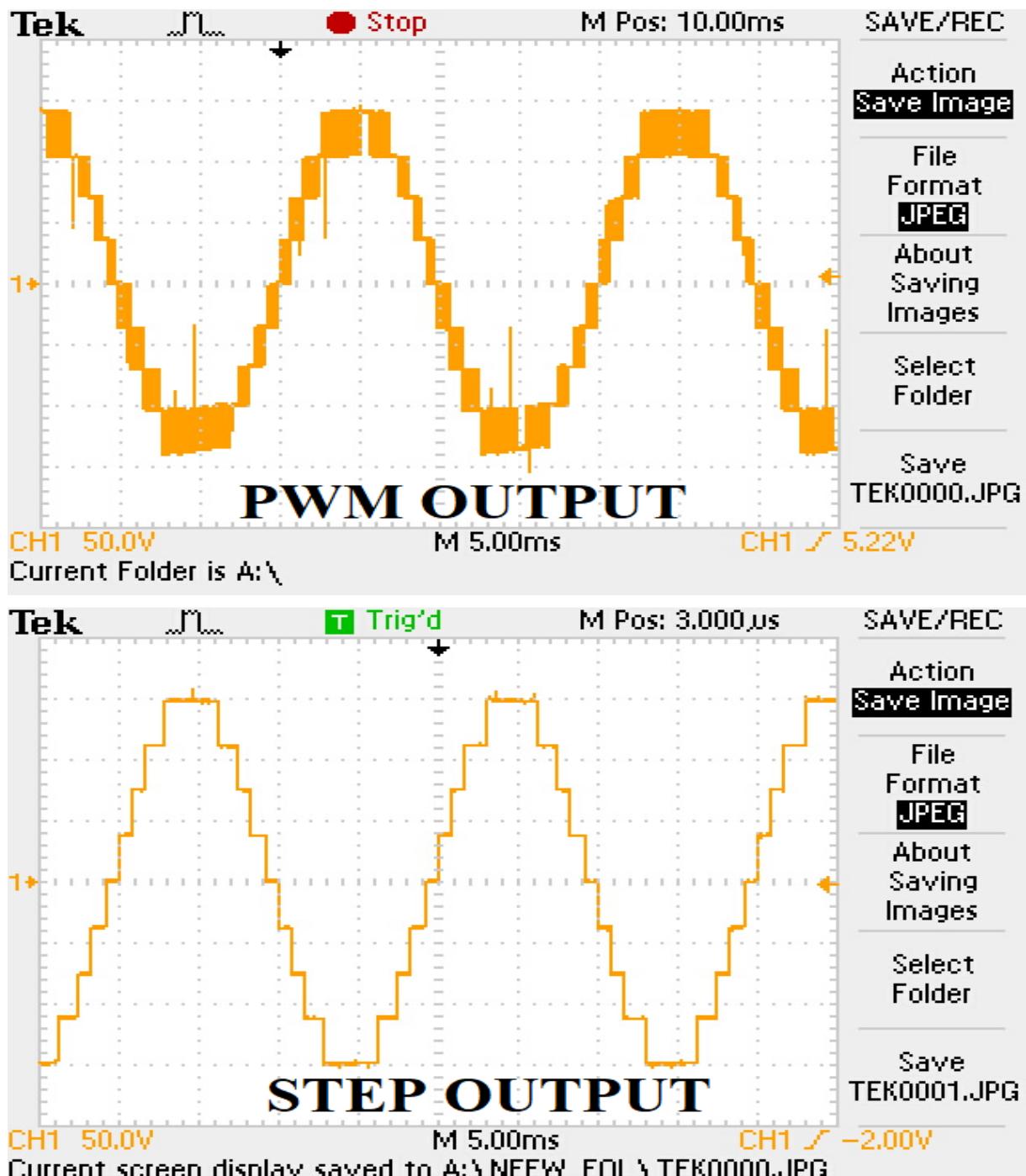


Figure 5.15: Output voltage waveform for R load ($R=100\Omega$)

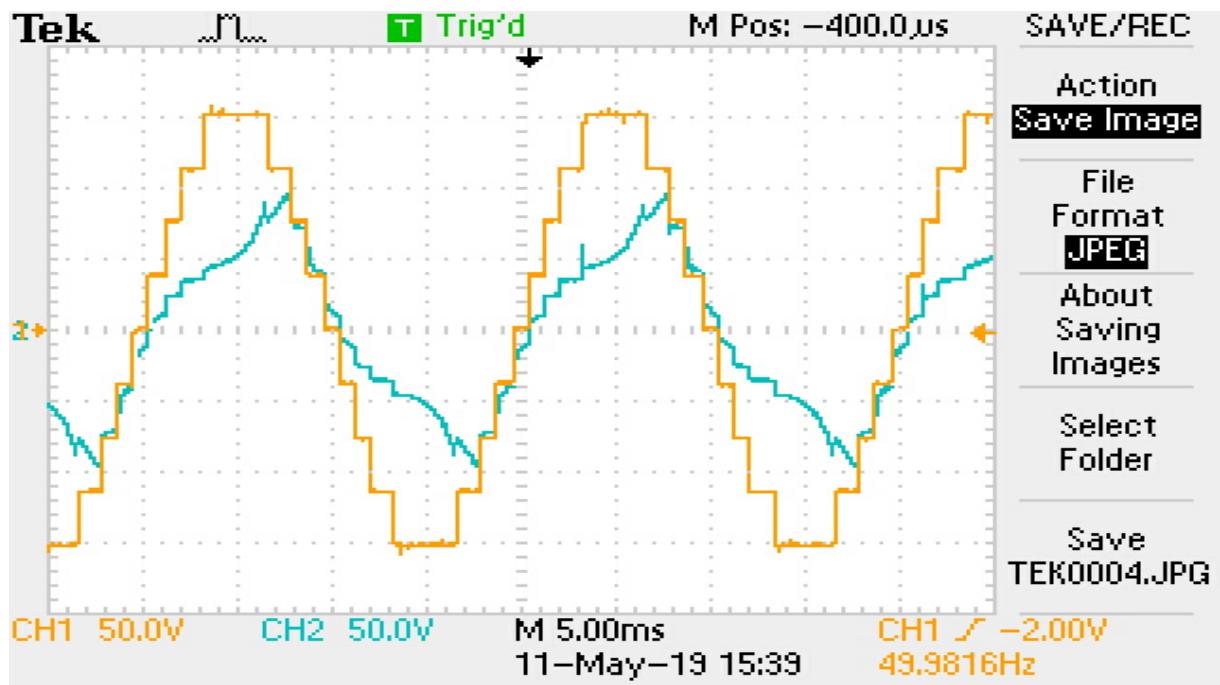


Figure 5.16: Output voltage and current waveforms for RL load ($R=300\Omega$, $L=20\text{mH}$)

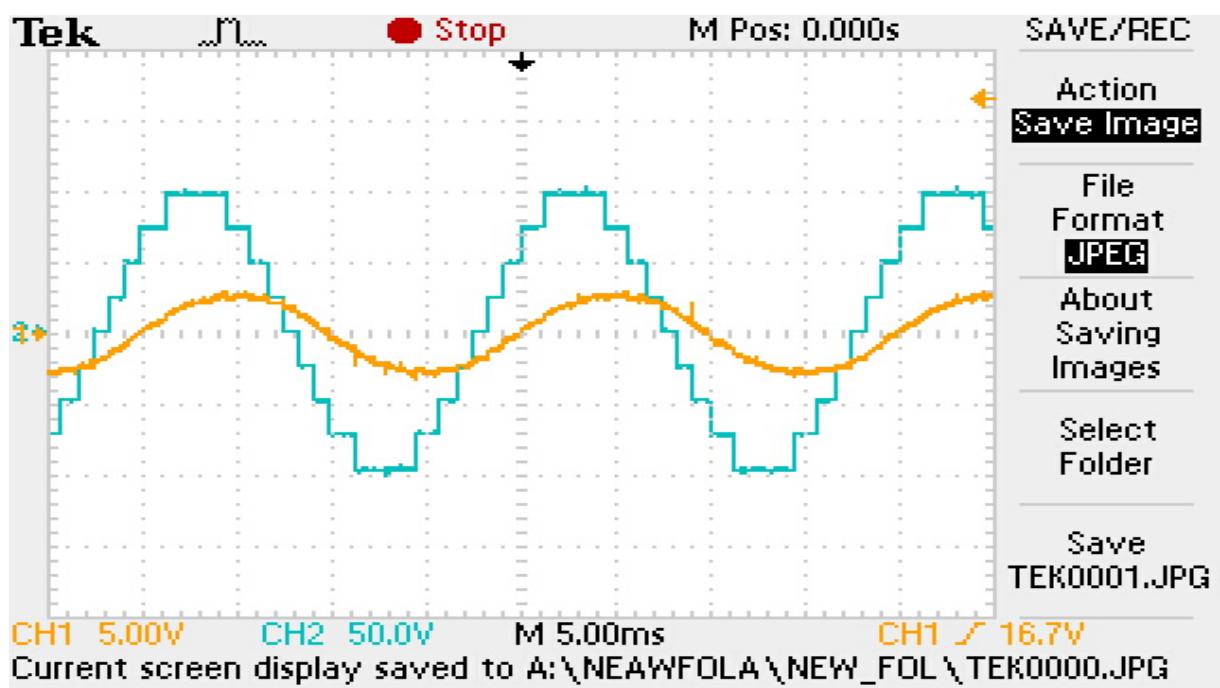


Figure 5.17: Output voltage and current waveforms for RL load ($R=100\Omega$, $L=40\text{mH}$)

The peak to peak value of the inverter output wave was found to be 300 volts. When no PWM was done, the output current could only be filtered by very low power factor loads. But when PWM was given the current distortion was easily reduced at high power factor loads itself. This is due to the high frequency switching which shifts the harmonics into higher order which can easily be filtered out by very low inductance. Therefore almost the entire voltage could be applied across the R load rather than dropping a main portion of it in the inductance. Moreover the nine level switching levels further reduce the harmonic content in the output voltage due to which satisfactoy filtering is obtained at low switching frequencies like 5khz . The RMS voltage of $100V$ and power rating of $100W$ was found to be in agreement with the simulation model.

Chapter 6

CONCLUSION

In this project, simulation and hardware implementation of a single-phase nine-level inverter based on switched capacitor structure has been done. This converter has a single DC source and less number of power semiconductor switches compared to nine-level diode clamped/flying capacitor/cascaded H-bridge configurations. Hence the size and cost of the converter is reduced. The peak load voltage is $4V_{in}$. Efficiency of the converter is found to be 95%. While using PDPWM method for generation of switching signals with a switching frequency of 5kHz, the total harmonic distortion in load voltage and current are obtained 13.92% and 1.013% respectively. The voltage stress across the switches S_{11} , S_{12} are V_{in} , S_{21} , S_{22} , S_{23} are $2V_{in}$ and T_1 , T_2 , T_3 , T_4 are $4V_{in}$. The THD in the load current can be further reduced by providing a first order filter. The main disadvantage of this converter is that the voltage stress of the H-bridge switches is equal to the peak output voltage. This converter is very suitable for low power applications with single phase system. By extending the number of levels to 17, the output current can be made nearly sinusoidal.

References

- [1] B.-B. Ngo, M.-K. Nguyen, J.-H. Kim, and F. Zare, “Single-phase multilevel inverter based on switched-capacitor structure,” *IET Power Electronics*, vol. 11, no. 11, pp. 1858–1865, 2018.
- [2] B. W. Williams, “Principles and elements of power electronics,” *Devices, Drivers, Applications and Passive Components*, p. 1432, 2006.
- [3] Y. Ye, K. W. E. Cheng, J. Liu, and K. Ding, “A step-up switched-capacitor multilevel inverter with self-voltage balancing,” *IEEE Transactions on industrial electronics*, vol. 61, no. 12, pp. 6672–6680, 2014.
- [4] P. Bhagyalakshmi, B. M. Varghese, and B. M. Jos, “Switched capacitor multilevel inverter with different modulation techniques,” in *2017 International Conference on Innovations in Information, Embedded and Communication Systems (ICIIECS)*, pp. 1–6, IEEE, 2017.
- [5] J. Rodriguez, J.-S. Lai, and F. Z. Peng, “Multilevel inverters: a survey of topologies, controls, and applications,” *IEEE Transactions on industrial electronics*, vol. 49, no. 4, pp. 724–738, 2002.
- [6] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon, “Recent advances and industrial applications of multilevel converters,” *IEEE Transactions on industrial electronics*, vol. 57, no. 8, pp. 2553–2580, 2010.
- [7] Y. Hinago and H. Koizumi, “A switched-capacitor inverter using series/parallel conversion with inductive load,” *IEEE Transactions on industrial electronics*, vol. 59, no. 2, pp. 878–887, 2011.