

# Single-phase multilevel inverter based on switched-capacitor structure

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**Abstract:** This study proposes a new topology for multilevel inverters based on switched-capacitor structure. The proposed topology uses capacitor charged/discharged characteristic to boost the output voltage without employing magnetic elements. The proposed circuit configuration has fewer components, including switches, voltage sources, and capacitors comparing with the conventional similar topologies. A phase disposition pulse-width modulation method is used to enhance the output waveform quality of the proposed inverter. Nine-level and 17-level configurations are simulated. To verify the operating principle, the experimental results for a nine-level inverter topology are presented.

## 1 Introduction

Recently, multilevel inverters (MIs) have become more attractive to researchers owing to their advantages such as improved output waveform quality, lower electromagnetic interface, and lower device stress [1, 2]. MIs are used to switch a DC power source to an AC power source for applications such as electric motor drivers, uninterruptible power supplies, and distributed generation systems. Commonly used traditional MI configurations are the neutral-point clamped [3], flying capacitor [4], and cascaded H-bridge (CHB) configurations [5–7]. However, these configurations use a large number of components, including semiconductor switches, power supplies, capacitors, and diodes. As a result, the overall system has a large size and high cost, and complex control. For low-power applications, the system size and cost are the main concerns, a switched-capacitor (SC) structure is usually added to the H-bridge inverter [8–22]. The SC structures use capacitors, switches, and diodes to create a multilevel DC voltage at the DC bus of the H-bridge circuit. Then, the H-bridge circuit inverts the multilevel DC voltage to AC voltage. One of the advantages of SC-based MIs over traditional MIs is that they use fewer switches [8].

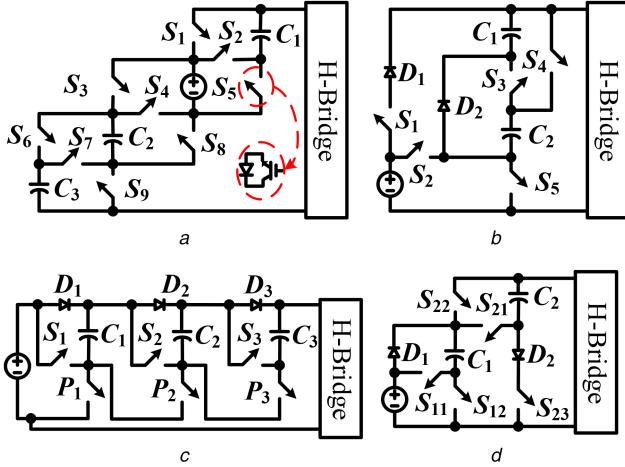
The SC multilevel inverter (SCMI) topologies in [9–18] use four input DC voltages, as required for a CHB topology to generate a multilevel voltage at the output. They include the cascaded half-bridge-based MI [9], T-type MI [10], cascaded bipolar switched-cell-based MI [11], series/parallel connection-based MI [12, 13], packed U-cell MI [14], reversing-voltage MI [15], two-switch enabled level-generation-based MI [16], series-connected-capacitor-based MI [17], and sub-MI [18]. However, the SC-based MIs in [9–18] use a large number of input DC voltages. SCMI based on a single-source voltage was recently proposed in [19–22]. The single-source-voltage-based SCMI uses the charging and discharging characteristics of the capacitor to decrease the number of sources in the power circuit. In the SCMI, the capacitors can be self-balanced by switching in parallel and in series through the switches. In parallel mode, the capacitors are directly charged by a power supply and release their stored energy in series mode. Since it uses SC structures, the system does not need additional power supplies to increase the output voltage level or transformers to boost the output voltage. As a result, the SCMI is smaller, is less expensive, and requires less complex control in comparison with the conventional similar topologies.

Fig. 1 shows SC-based nine-level inverters, where the SC structure is located at the frontend H-bridge circuit. In Fig. 1a, the capacitors of the MI [12] are switched in series and parallel connections. This topology uses a large number of components, including one input source, three capacitors, and 13 active switches. Fig. 1b shows a combination of SC and H-bridge configurations [22]. The SC contains two diodes, two capacitors, and five switches. Fig. 1c shows a topology consisting of a series combination of SC cells [19]. Each SC cell includes one diode, one capacitor, and two switches. An improved series-parallel conversion setup including two diodes, two capacitors, and five switches is used in [20, 21], as shown in Fig. 1d. These nine-level inverter topologies use only one source to produce a high output voltage without using any inductors. These topologies have fewer components in the circuit than traditional MIs.

This paper proposes a new SCMI configuration with fewer switches. The proposed inverter uses only one power DC source to raise the number of output voltage levels or boost the output voltage without using any inductors. The proposed inverter can also be extended to  $n_{\text{level}}$  by adding SC cells. This paper describes the theoretical operating principle, analysis, capacitance voltage ripple, and power loss calculation for the proposed inverter. The PSIM 9.0 software is used to prove the operating principle of the proposed inverter with nine-level and 17-level configurations. The experimental results for a nine-level inverter are also shown.

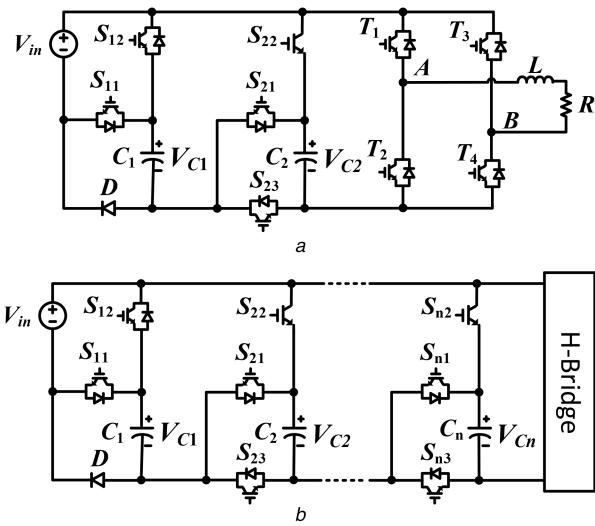
## 2 Proposed SC nine-level inverter

Fig. 2a shows the proposed SC nine-level inverter topology. The proposed inverter consists of a single DC source, two SC cells connected in parallel with the H-bridge circuit and a load. The first SC cell is a combination of one capacitor, one diode, and two switches ( $C_1-D-S_{11}-S_{12}$ ), and the second SC cell includes one capacitor, and three switches ( $C_2-S_{21}-S_{22}-S_{23}$ ). In the operation circuit, capacitor  $C_1$  is charged while connected in parallel with the input source through  $S_{12}$ , whereas it is discharged in series with the input source through  $S_{11}$ . Further, capacitor  $C_2$  is charged in parallel from the input source and capacitor  $C_1$  through  $S_{22}$  and  $S_{23}$ , whereas it is discharged in series with capacitor  $C_1$  and the input source through  $S_{21}$ .



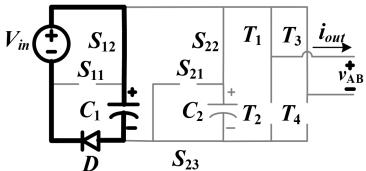
**Fig. 1** Nine-level inverters using

(a) Topology with series/parallel conversion [12], (b) Developed SC circuit [22], (c) Topology using SC units [19], (d) Improved SC circuit [20, 21]

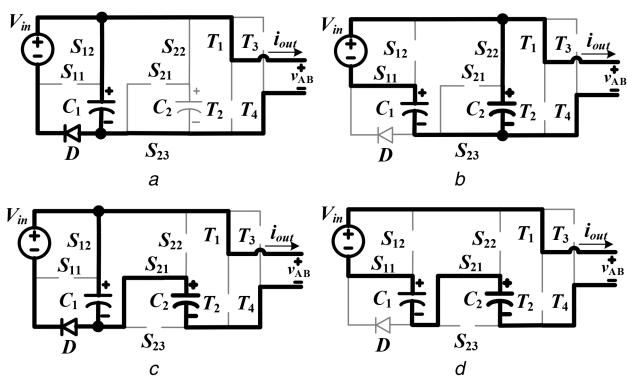


**Fig. 2** Proposed SCMI topologies

(a) Nine-level topology, (b) Extended topology



**Fig. 3** Operation state 1 and current flow of proposed inverter



**Fig. 4** Operation states and current flow of proposed inverter

(a) State 2, (b) State 3, (c) State 4, (d) State 5

## 2.1 Operating principle

Figs. 3–5 show the nine operating states of the proposed inverter. Fig. 6 illustrates the pulse-width modulation (PWM) scheme for the proposed inverter. In the positive period of the output voltage, the circuit operation includes seven stages and four states (states 2–5, Fig. 4). In this period, the switches of the H-bridge are not changed, T<sub>1</sub> and T<sub>4</sub> are fully turned ON, T<sub>2</sub> and T<sub>3</sub> are fully turned OFF, and the components of the SC cells are changed in each stage. The time intervals t<sub>0</sub>–t<sub>7</sub> are indicated in Fig. 6.

**Stage 1** [t<sub>0</sub>–t<sub>1</sub>, Figs. 3 and 4a]: S<sub>12</sub>, S<sub>22</sub>, S<sub>23</sub> and T<sub>1</sub> are fully turned ON, whereas S<sub>11</sub>, S<sub>21</sub>, and T<sub>2</sub> are fully turned OFF. Diode D is forward biased. Capacitor C<sub>1</sub> is charged from the input voltage, and V<sub>C1</sub> = V<sub>in</sub>. If T<sub>3</sub> is turned ON and T<sub>4</sub> is turned OFF, the output voltage is zero (V<sub>AB</sub> = 0), as shown in Fig. 3 for state 1. If T<sub>3</sub> is turned OFF and T<sub>4</sub> is turned ON, the output voltage equals the input voltage (V<sub>AB</sub> = V<sub>in</sub>), as shown in Fig. 4a for state 2.

**Stage 2** [t<sub>1</sub>–t<sub>2</sub>, Figs. 4a and b]: S<sub>22</sub> and S<sub>23</sub> are fully turned ON, whereas S<sub>21</sub> is fully turned OFF. If S<sub>11</sub> is turned OFF and S<sub>12</sub> is turned ON, diode D is forward-biased, and capacitor C<sub>1</sub> is charged from the input voltage. The output voltage is V<sub>AB</sub> = V<sub>C1</sub> = V<sub>in</sub>, as shown in Fig. 4a for state 2. If S<sub>11</sub> is turned ON and S<sub>12</sub> is turned OFF, diode D is reverse biased; capacitor C<sub>1</sub> is discharged, whereas capacitor C<sub>2</sub> is charged from the input voltage and the voltage of capacitor C<sub>1</sub>, and V<sub>C2</sub> = V<sub>in</sub> + V<sub>C1</sub> = 2V<sub>in</sub>. The output voltage is twice the input voltage (V<sub>AB</sub> = V<sub>C2</sub> = 2V<sub>in</sub>), as shown in Fig. 4b for state 3.

**Stage 3** [t<sub>2</sub>–t<sub>3</sub>, Figs. 4b and c]: If S<sub>11</sub> and S<sub>22</sub>, S<sub>23</sub> are turned ON and S<sub>12</sub> and S<sub>21</sub> are turned OFF, diode D is reverse biased; capacitor C<sub>1</sub> is discharged, whereas capacitor C<sub>2</sub> is charged from the input voltage and the voltage of capacitor C<sub>1</sub>. The output voltage is V<sub>AB</sub> = V<sub>in</sub> + V<sub>C1</sub> = 2V<sub>in</sub>, as shown in Fig. 4b for state 3. If S<sub>11</sub> and S<sub>22</sub>, S<sub>23</sub> is turned OFF and S<sub>12</sub> and S<sub>21</sub> are turned ON, diode D is forward biased; capacitor C<sub>1</sub> is charged from the input voltage, whereas capacitor C<sub>2</sub> is discharged, and the output voltage equals three times the input voltage (V<sub>AB</sub> = V<sub>in</sub> + V<sub>C2</sub> = 3V<sub>in</sub>), as shown in Fig. 4c for state 4.

**Stage 4** [t<sub>3</sub>–t<sub>4</sub>, Figs. 4c and d]: S<sub>21</sub> is fully turned ON, and S<sub>22</sub>, S<sub>23</sub> is fully turned OFF. Capacitor C<sub>2</sub> is discharged. If S<sub>12</sub> is turned ON and S<sub>11</sub> is turned OFF, diode D is forward biased, and capacitor C<sub>1</sub> is charged from the input voltage. The output voltage is V<sub>AB</sub> = V<sub>in</sub> + V<sub>C2</sub> = 3V<sub>in</sub>, as shown in Fig. 4c for state 4. If S<sub>12</sub> is turned OFF and S<sub>11</sub> is turned ON, diode D is reverse biased, and capacitor C<sub>1</sub> is discharged; the output voltage equals four times the input voltage (V<sub>AB</sub> = V<sub>in</sub> + V<sub>C1</sub> + V<sub>C2</sub> = 4V<sub>in</sub>), as shown in Fig. 4d for state 5.

**Stage 5** [t<sub>4</sub>–t<sub>5</sub>, Figs. 4b and c]: Similar to stage 3.

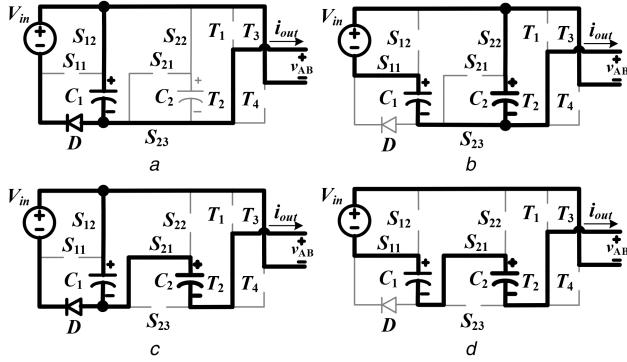
**Stage 6** [t<sub>5</sub>–t<sub>6</sub>, Figs. 4a and b]: Similar to stage 2.

**Stage 7** [t<sub>6</sub>–t<sub>7</sub>, Figs. 3 and 4a]: Similar to stage 1.

Similarly, in the negative period, the circuit operation includes seven stages with four states (states 6–9, as shown in Fig. 5, respectively). In this period, the switches of the H-bridge circuit are opposite to those in the positive period; T<sub>2</sub> and T<sub>3</sub> are fully turned ON, whereas T<sub>1</sub> and T<sub>4</sub> are fully turned OFF, and the components of the SC cells are similar to those in the positive period in each stage. Table 1 summarises the operating states of the proposed inverter.

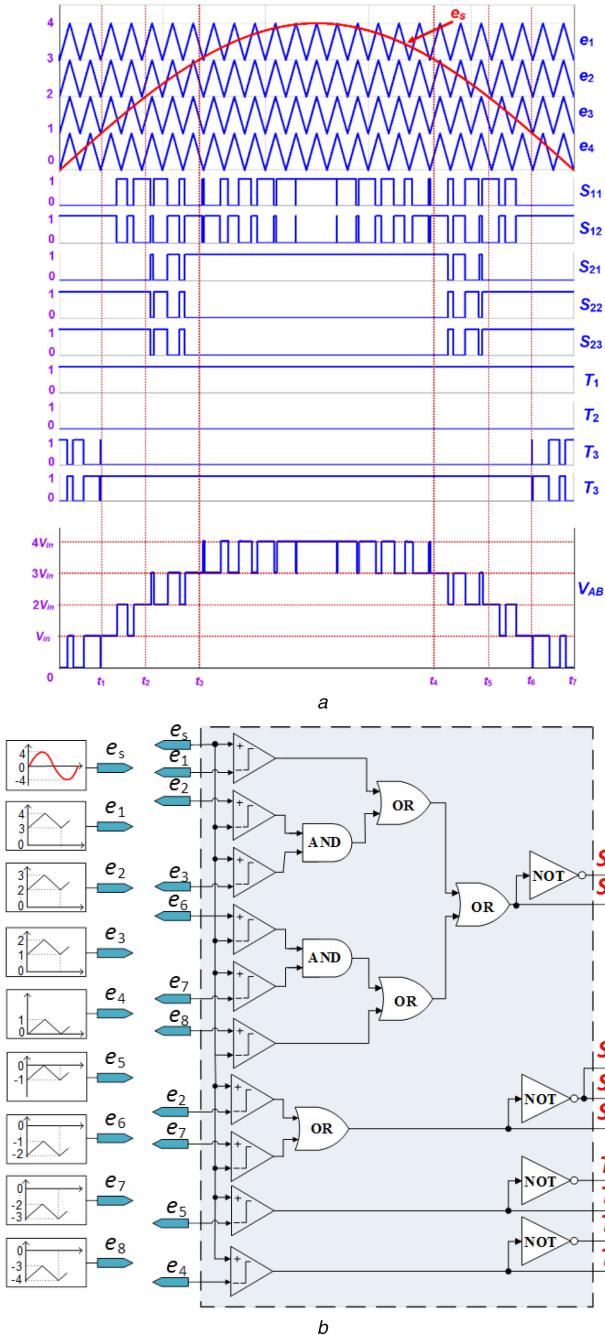
## 2.2 PWM control strategy

PWM control strategies such as space vector modulation [2], phase disposition (PD) PWM [23], phase opposite disposition PWM [24], alternative phase opposite disposition PWM [25], selective harmonic elimination [2], and hybrid modulation [26, 27] can be used to control the SCMI. As an example, PD-PWM is used to control the proposed inverter in this paper. Other control strategies can be applied to the proposed topology as long as the circuit operation states as shown in Table 1 are guaranteed. Fig. 6a shows



**Fig. 5** Operation states and current flow of proposed inverter

(a) State 6, (b) State 7, (c) State 8, (d) State 9



**Fig. 6** PD-PWM control method for the proposed inverter

(a) Waveforms in a half-period of the output voltage, where  $e_s$  is the reference waveform and  $e_1$ – $e_4$  are carrier waveforms, (b) Logic scheme

the PD-PWM control method for the proposed inverter in a half-period of the output voltage. Fig. 6b shows a logic scheme of the PD-PWM control method for the proposed inverter. For the nine-level inverter, eight carrier waveforms are synchronised to the same phase and the same amplitude that is used to control the switches. The reference waveform is  $e_s = U_s \times \sin(2\pi f_{ref} t)$ , where  $f_{ref}$  and  $U_s$  are the frequency and amplitude of the reference waveform, respectively. In PD-PWM, the modulation index is determined by the ratio of the amplitudes of the reference and carrier waveforms. In the proposed inverter, the amplitude modulation index is

$$M = \frac{U_s}{4U_c}, \quad (1)$$

where  $U_c$  is the peak-to-peak of the carrier waveform,  $e_4$ .

Based on the modulation index, the root-mean-squared (RMS) output voltage is approximated as follows:

$$V_{AB,\text{rms}} \approx M \frac{4V_{in}}{\sqrt{2}}, \quad (2)$$

The state of each switch at any time depends on the relationship between the reference and carrier waveform values. To generate the control signal to the switches,  $e_s$  is compared with  $e_1$ ,  $e_2$ ,  $e_3$ , and  $e_4$ . All the results of the control strategy analysis are synthesised in Table 1.

### 3 Extension of the proposed inverter

The nine-level SC inverter can be extended to a 17-level SC inverter by adding an SC cell including a capacitor and three semiconductor switches ( $C_3$ – $S_{31}$ – $S_{32}$ – $S_{33}$ ) or to a 33-level SC inverter by adding two SC cells. Generally, the proposed inverter can be extended to the  $(2^{n+1} + 1)$  SC level by adding  $n$  SC cells, as shown in Fig. 2b. The operation states of the extended circuit topology are shown in Table 2.

For an  $n_{\text{level}}$  extension of the proposed inverter, the number of required semiconducting switches ( $n_{\text{sw}}$ ), capacitors ( $n_C$ ), and power diodes ( $n_D$ ) are calculated as follows:

$$\begin{cases} n_{\text{level}} = 2^{n_C + 1} + 1 \\ n_{\text{sw}} = 3n_C + 3 \\ n_C = \log_2(n_{\text{level}} - 1) - 1 \\ n_D = 1. \end{cases} \quad (3)$$

Table 3 compares the extended topology of the proposed inverter to that of the extended inverter configurations in [12, 19–21]. Based on Table 3, when the topologies have same output voltage level, the proposed inverter reduces the number of components in comparison with other configurations. The proposed topology has the same features as that in [20, 21], but reduces a large number of diodes when the SC cell is increased.

### 4 Capacitance determination for the proposed nine-level SC inverter

The capacitance of capacitors  $C_1$  and  $C_2$  can be determined on the basis of their voltage ripples. For a smaller voltage ripple, the capacitor is more efficient. Determining the capacitance ensures that the maximum voltage ripple of the capacitor is  $X\%$  of the charged capacitor voltage.

Assuming that the modulation index  $M = 1$ , the times  $t_1$ ,  $t_2$ ,  $t_3$ , and  $t_4$  in Fig. 6 are determined as follows:

$$\begin{cases} t_1 = \frac{\sin^{-1}(1/4)}{2\pi f_{\text{ref}}}, \\ t_2 = \frac{\sin^{-1}(1/2)}{2\pi f_{\text{ref}}}, \\ t_3 = \frac{\sin^{-1}(3/4)}{2\pi f_{\text{ref}}}, \\ t_4 = \frac{\pi - \sin^{-1}(3/4)}{2\pi f_{\text{ref}}}. \end{cases} \quad (4)$$

Charging/discharging capacitors' voltages should be based on load current and adjacent voltage vector to reduce switching losses. In the proposed inverter, the switching transient number for charging/discharging to reduce switching losses cannot be minimised. This is one of the main issues of the proposed inverter. Although minimum switching transient cannot be achieved with respect to charging and discharging modes of capacitor voltages however, an optimum control algorithm can be developed with respect to (i) possible switching states, (ii) charging/discharging modes and load current and (iii) acceptable level of voltage fluctuation across each capacitor. For example, if the level of voltage fluctuation across each capacitor is change with respect to the reference voltage, more chose of freedom is provided for selecting different switching states. The level of the voltage fluctuation should be correlated with respect to the quality and harmonic emissions of the output voltage.

Given that the output power factor ( $\cos \phi$ ) is 1, capacitor  $C_1$  is discharged in the time intervals  $[t_1, t_2]$  and  $[t_3, t_4]$ , as shown in Fig.

**Table 1** Operation states of the proposed inverter

No.	Case	State	On-state switches and diodes	$V_{AB}$
1	$e_s > e_1$	state 5 (Fig. 4d)	$S_{11}, S_{21}, T_1, T_4$	$4V_{\text{in}}$
2	$e_1 \geq e_s > e_2$	state 4 (Fig. 4c)	$S_{12}, S_{21}, T_1, T_4, D$	$3V_{\text{in}}$
3	$e_2 \geq e_s > e_3$	state 3 (Fig. 4b)	$S_{11}, S_{22}, S_{23}, T_1, T_4$	$2V_{\text{in}}$
4	$e_3 \geq e_s > e_4$	state 2 (Fig. 4a)	$S_{12}, S_{22}, S_{23}, T_1, T_4, D$	$V_{\text{in}}$
5	$e_4 \geq e_s > e_5$	state 1 (Fig. 3)	$S_{12}, S_{22}, S_{23}, T_1, T_3, D$	0
6	$e_5 \geq e_s > e_6$	state 6 (Fig. 5a)	$S_{12}, S_{22}, S_{23}, T_2, T_3, D$	$-V_{\text{in}}$
7	$e_6 \geq e_s > e_7$	state 7 (Fig. 5b)	$S_{11}, S_{22}, S_{23}, T_2, T_3$	$-2V_{\text{in}}$
8	$e_7 \geq e_s > e_8$	state 8 (Fig. 5c)	$S_{12}, S_{21}, T_2, T_3, D$	$-3V_{\text{in}}$
9	$e_8 \geq e_s$	state 9 (Fig. 5d)	$S_{11}, S_{21}, T_2, T_3$	$-4V_{\text{in}}$

**Table 2** Operation states of the extend proposed inverter with  $n$ -SC cells

No	On-state switches	$V_{AB}$
1	$S_{11}, S_{21}, \dots, S_{n1}$ $T_1, T_4$	$(n+1)V_{\text{in}}$
2	$S_{12}, S_{21}, S_{31}, \dots, S_{n1}$ $T_1, T_4, D$	$nV_{\text{in}}$
3	$S_{11}, S_{22}, S_{23}, S_{31}, S_{41}, \dots, S_{n1}$ $T_1, T_4$	$(n-1)V_{\text{in}}$
4	$S_{12}, S_{22}, S_{23}, S_{31}, S_{41}, \dots, S_{n1}$ $T_1, T_4, D$	$(n-2)V_{\text{in}}$
...	...	...
$2^{n_C+1}-2$	$S_{12}, S_{22}, S_{23}, S_{31}, S_{41}, \dots, S_{n1}$ $T_2, T_3, D$	$-(n-2)V_{\text{in}}$
$2^{n_C+1}-1$	$S_{11}, S_{22}, S_{23}, S_{31}, S_{41}, \dots, S_{n1}$ $T_2, T_3$	$-(n-1)V_{\text{in}}$
$2^{n_C+1}$	$S_{12}, S_{21}, S_{31}, \dots, S_{n1}$ $T_2, T_3, D$	$-nV_{\text{in}}$
$2^{n_C+1}+1$	$S_{11}, S_{21}, \dots, S_{n1}$ $T_2, T_3$	$-(n+1)V_{\text{in}}$

6. Thus, the longest discharged time interval of capacitor  $C_1$  is from  $t_3$  to  $t_4$ . The discharged time of capacitor  $C_2$  is from  $t_2$  to  $t_5$ , as shown in Fig. 6. During the time interval from  $t_2$  to  $t_5$ , the output voltage changes from  $2V_{\text{in}}$  to  $3V_{\text{in}}$  and from  $3V_{\text{in}}$  to  $4V_{\text{in}}$  sequentially. Therefore, the switching interval is not enough to charge/discharge the capacitors safely. This is another limitation of the proposed inverter. In order to overcome this limitation, a high capacitance can be selected for  $C_2$  to reduce the capacitor voltage ripple. Note that these discharged time intervals of the capacitors are maximised because capacitors  $C_1$  and  $C_2$  can be charged during these time intervals. Consequently, the variation of the capacitor voltage ripples is approximated as follows:

$$\begin{cases} \Delta V_{C_{11}} \simeq \frac{1}{C_1} \int_{t_1}^{t_2} i_{C_1}(t) dt, \\ \Delta V_{C_{12}} \simeq \frac{1}{C_1} \int_{t_3}^{t_4} i_{C_1}(t) dt, \\ \Delta V_{C_2} \simeq \frac{1}{C_2} \int_{t_2}^{t_5} i_{C_2}(t) dt, \end{cases} \quad (5)$$

where  $\Delta V_{C_{11}}$ ,  $\Delta V_{C_{12}}$ , and  $\Delta V_{C_2}$  are the voltage ripple of capacitor  $C_1$  from  $t_1$  to  $t_2$ , the voltage ripple of capacitor  $C_1$  from  $t_3$  to  $t_4$ , and the voltage ripple of capacitor  $C_2$  from  $t_2$  to  $t_5$ , respectively. Since the maximum voltage ripple is  $X\%$  of the voltage of the charged capacitor, the capacitance values are

$$\begin{cases} C_1 \geq \max \left\{ \frac{1}{V_{\text{in}} X \%} \int_{t_1}^{t_2} i_{C_1}(t) dt, \frac{1}{V_{\text{in}} X \%} \int_{t_3}^{t_4} i_{C_1}(t) dt \right\}, \\ C_2 \geq \frac{1}{2V_{\text{in}} X \%} \int_{t_2}^{t_5} i_{C_2}(t) dt \end{cases} \quad (6)$$

Table 4 shows the voltage stress comparison between the topology in [20, 21] (see Fig. 1d) and the proposed topology for the same input and output voltage characteristics. As presented in Table 4, the voltage stress on capacitors, switches, and diode  $D_1$  of both topologies are the same. However, the topology in [20, 21] uses one more diode with the voltage stress of  $2V_{\text{in}}$ .

In general, the capacitance values are calculated as in (6). Under the same PD-PWM control strategy condition as shown in Fig. 6, the switching states of the topology in [20, 21] are similar to those of the proposed inverter in Figs. 3–5. Consequently, both inverters have the same charged and discharged values. Therefore, the inverter in [20, 21] and the proposed inverter have the same capacitor size under the same input/output voltage condition.

## 5 Power loss calculation for the proposed nine-level SC inverter

### 5.1 Switching losses

In the proposed topology, switching losses occur on the power switches, antiparallel diodes, and power diodes. The switching loss depends on the switching frequency. The switching losses of the power switches are

**Table 3** Comparison with the other inverter configurations

	Proposed inverter	Inverter in [12]	Inverter in [19]	Inverter in [20, 21]
$n_{\text{level}}$	$2^{n_C+1} + 1$	$2n_C + 3$	$2n_C + 3$	$2^{n_C+1} + 1$
$n_{\text{sw}}$	$3n_C + 3$	$3n_C + 4$	$2n_C + 4$	$3n_C + 3$
$n_D$	1	0	$n_C$	$n_C$
$n_C$	$n_C$	$n_C$	$n_C$	$n_C$
$n_V$	1	1	1	1

Where  $n_{\text{level}}$ ,  $n_{\text{sw}}$ ,  $n_D$ ,  $n_C$  and  $n_V$  are the number of level, the number of switches, the number of diodes, the number of capacitors and the number of input sources, respectively.

$$P_{sw,T} = (E_{on,T} + E_{off,T})f_{sw}, \quad (7)$$

where  $E_{on,T}$  is the switch turn-on energy loss,  $E_{off,T}$  is the switch turn-off energy loss, and  $f_{sw}$  is the switching frequency.

The switching losses of the diodes are calculated as

$$P_{sw,D} = (E_{on,D} + E_{off,D})f_{sw}, \quad (8)$$

where  $E_{on,D}$  is the diode turn-on energy loss, and  $E_{off,D}$  is the diode turn-off energy loss. The frequencies of the antiparallel diodes and switches are the same.

From Fig. 6, switches  $S_{11}$  and  $S_{12}$  are turned ON/OFF when the time is in the range  $[t_1, t_6]$  in the half-period. Thus, the average number of switching transitions  $\overline{N}_{S_{11}}$  and  $\overline{N}_{S_{12}}$  in one period of the reference waveform is calculated as

$$\overline{N}_{S_{11}} = \overline{N}_{S_{12}} = \frac{2(t_6 - t_1)}{T} \frac{f_c}{f_{ref}}, \quad (9)$$

where  $f_c$  is the carrier waveform frequency, and  $T$  is the reference waveform period.

From (7) and (9), the switching losses of switches  $S_{11}$  and  $S_{12}$  are calculated as

$$P_{sw,T_1} = (E_{on,T} + E_{off,T}) \frac{2(t_6 - t_1)}{T} \frac{f_c}{f_{ref}}, \quad (10)$$

The switching losses of the diodes connected antiparallel to switches  $S_{11}$  and  $S_{12}$  are

$$P_{sw,anti-D_1} = (E_{on,anti-D} + E_{off,anti-D}) \frac{2(t_6 - t_1)}{T} \frac{f_c}{f_{ref}}, \quad (11)$$

where  $E_{on,anti-D}$  is the antiparallel diode turn-on energy loss, and  $E_{off,anti-D}$  is the antiparallel diode turn-off energy loss.

Switches  $S_{21}$ ,  $S_{22}$  and  $S_{23}$  are switched ON/OFF during the time intervals  $[t_2, t_3]$  and  $[t_4, t_5]$  in the half-period. Thus, the average number of switching transitions  $\overline{N}_{S_{21}}$ ,  $\overline{N}_{S_{22}}$ , and  $\overline{N}_{S_{23}}$  in one period of the reference waveform is calculated as

$$\overline{N}_{S_{21}} = \overline{N}_{S_{22}} = \overline{N}_{S_{23}} = \frac{4(t_3 - t_2)}{T} \frac{f_c}{f_{ref}}, \quad (12)$$

$$P_{sw,T_2} = (E_{on,T} + E_{off,T}) \frac{4(t_3 - t_2)}{T} \frac{f_c}{f_{ref}}, \quad (13)$$

The switching losses of the diode connected antiparallel to switches  $S_{21}$  and  $S_{23}$  are

**Table 4** Voltage stress comparison between two inverters

	Topology in [20, 21]	Proposed topology
number of levels	9	9
input voltage	$V_{in}$	$V_{in}$
peak output voltage ( $V_{AB}$ )	$4V_{in}$	$4V_{in}$
Capacitors		
$C_1$	$V_{in}$	$V_{in}$
$C_2$	$2V_{in}$	$2V_{in}$
Diodes		
$D_1$	$V_{in}$	$V_{in}$
$D_2$	$2V_{in}$	0
Switches		
$S_{11}, S_{12}$	$V_{in}$	$V_{in}$
$S_{21}, S_{22}, S_{23}$	$2V_{in}$	$2V_{in}$
H-bridge ( $T_1-T_4$ )	$4V_{in}$	$4V_{in}$

$$P_{sw,anti-D_2} = (E_{on,anti-D} + E_{off,anti-D}) \frac{4(t_3 - t_2)}{T} \frac{f_c}{f_{ref}}, \quad (14)$$

Similarly, the switching losses of  $T_1$ ,  $T_2$ ,  $T_3$ ,  $T_4$  and the antiparallel diodes are calculated as

$$P_{sw,T_3} = (E_{on,T} + E_{off,T}) \frac{2t_1}{T} \frac{f_c}{f_{ref}}, \quad (15)$$

$$P_{sw,anti-D_3} = (E_{on,anti-D} + E_{off,anti-D}) \frac{2t_1}{T} \frac{f_c}{f_{ref}}, \quad (16)$$

In the proposed topology, the switching loss of the power diodes  $D$  is calculated as follows:

$$P_{sw,power-D} = (E_{on,power-D} + E_{off,power-D}) \overline{N}_D, \quad (17)$$

where  $E_{on,power-D}$ ,  $E_{off,power-D}$  and  $\overline{N}_D$  are the power diode turn-on energy loss, power diode turn-off energy loss, and average switching transition numbers of  $D$  ( $\overline{N}_D = \overline{N}_{S_{11}}$ ), respectively.

## 5.2 Conduction losses

Conduction loss occurs in the switches, antiparallel diodes, and power diodes. The conduction loss of the switches is calculated when the switches are in the ON state:

$$P_{cond,T} = \frac{1}{T} \int_0^T v_{CE}(t) i_{out}(t) dt, \quad (18)$$

where  $i_{out}(t)$  is the output current, and  $v_{CE}(t)$  is the ON-state collector-emitter voltage

$$v_{CE}(t) = V_{CE0} + R_0 i_{out}(t),$$

(19) where  $R_0$  is the collector-emitter ON-state resistance of the switches, and  $V_{CE0}$  is the ON-state zero-current collector-emitter voltage.

The conduction losses of the diodes are calculated when the diodes are forward biased:

$$P_{cond,D} = \frac{1}{T} \int_0^T V_{DF} i_{out}(t) dt, \quad (20)$$

where  $V_{DF}$  is the diode forward voltage.

## 5.3 Capacitor losses

The losses of the capacitor are caused by the voltage ripple and internal resistance of the capacitor

$$P_C = P_{rip} + P_{SC}, \quad (21)$$

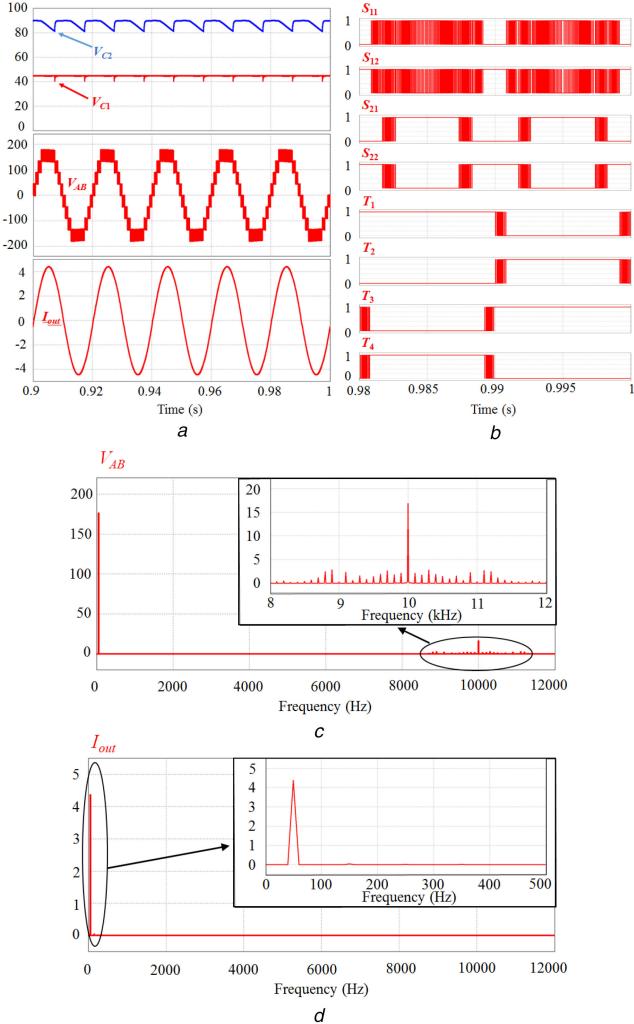
From (5), the losses caused by voltage ripple ( $P_{rip}$ ) are calculated as

$$P_{rip} = (\Sigma C_1 \Delta V_{C11}^2 + \Sigma C_1 \Delta V_{C12}^2 + \Sigma C_2 \Delta V_{C2}^2) f_{ref}, \quad (22)$$

When the capacitors are connected in series, the capacitor loss due to the internal resistance of the capacitor ( $r_{SC}$ ) is

$$P_{SC} = \frac{1}{T} \left( 4 \int_{t_1}^{t_2} r_{SC1} i_{C1}^2(t) dt + 2 \int_{t_3}^{t_4} r_{SC1} i_{C1}^2(t) dt + 2 \int_{t_2}^{t_5} r_{SC2} i_{C2}^2(t) dt \right), \quad (23)$$

where  $r_{SC1}$  and  $r_{SC2}$  are the internal resistances of capacitors  $C_1$  and  $C_2$ , respectively.



**Fig. 7** Simulation results for the proposed nine-level SC inverter

(a) Voltages of capacitors  $C_1$  and  $C_2$ , output voltage waveform ( $V_{AB}$ ), and output current waveform, (b) Control signals of  $S_{11}$ ,  $S_{12}$ ,  $S_{21}$ ,  $S_{22}$ ,  $T_1$ ,  $T_2$ ,  $T_3$ , and  $T_4$ , (c) Harmonic spectrum of output voltage, (d) Harmonic spectrum of output current

In comparison with the inverter in [20, 21], the proposed inverter has the same capacitor loss. However, the switching loss of diodes of the inverter in [20, 21] is larger than that of the proposed inverter because one additional  $D_2$  diode is used in [20, 21]. Moreover, the conduction loss of switches is the same while, the conduction loss of diodes of the inverter in [20, 21] is larger than that of the proposed inverter. Therefore, the proposed inverter has a better efficiency than the inverter in [20, 21] because the proposed inverter saves one diode that has a high voltage rating of  $2V_{in}$ .

## 6 Simulation and experimental results

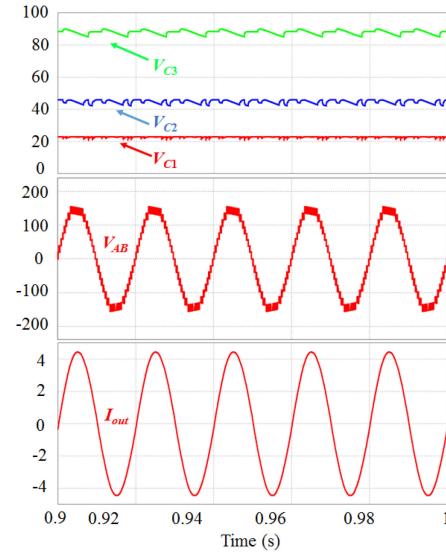
To confirm the operation of the proposed SC inverter, a simulation and an experiment were performed in this section. The parameters of the proposed topology are listed in Table 5. The simulation and experiment were performed for load of  $R = 40 \Omega$  and  $L = 14 \text{ mH}$ .

### 6.1 Simulation results

First, the proposed nine-level SC inverter was simulated using the parameters listed in Table 5. Fig. 7 shows the simulation results for an input voltage of 45 V. Fig. 7a shows the capacitors' voltages and the output voltage and output current waveforms. The average voltages of capacitors  $C_1$  and  $C_2$  are 44.2 and 87.4 V, respectively. The control signals of the switches in the proposed inverter are shown in Fig. 7b. Figs. 7c and d show the harmonic spectra of the output voltage and load current, respectively. The total harmonic distortion (THD) values of the output voltage and load current are 13.8 and 1.1%, respectively. Note that the THD value of the output

**Table 5** Parameters of the proposed SC inverter

	Nine-level	17-level
power rating	350 W	23 V
input voltage ( $V_{in}$ )	45 V	23 V
capacitors	$C_1 = C_2 = 2200 \mu\text{F}$	$C_1 = C_2 = C_3 = 2200 \mu\text{F}$
carrier frequency ( $f_c$ )	5 kHz	5 kHz
modulation index ( $M$ )	1	1
output voltage ( $V_{AB}$ )	127 V <sub>rms</sub>	127 V <sub>rms</sub>
output frequency ( $f_{ref}$ )	50 Hz	50 Hz
resistor ( $R$ )	40 Ω	40 Ω
inductor ( $L$ )	14 mH	14 mH



**Fig. 8** Simulation results for the proposed 17-level SC inverter: capacitor voltage waveform, output voltage ( $V_{AB}$ ), and output current waveform

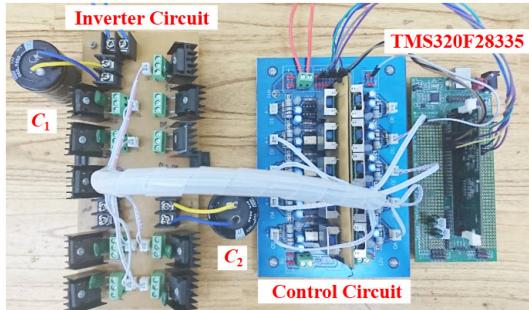
voltage is high because the measured THD value is based on one of the PWM methods while the THD value of the load current can be reduced for inductive and resistive load, providing a first-order filter.

Next, one more SC cell was added to obtain 17-level of the output voltage. The input voltage is reduced to 23 V to obtain the same 127 V<sub>rms</sub> output voltage. Table 5 also shows the operating parameters of the proposed 17-level SC inverter in the simulation. Fig. 8 shows the simulation results for the proposed 17-level SC inverter for an input voltage of 23 V. The output voltage waveform ( $V_{AB}$ ) has 17-level and a maximum voltage of 184 V. The output current waveform is sinusoidal and has a maximum value of 1.91 A.

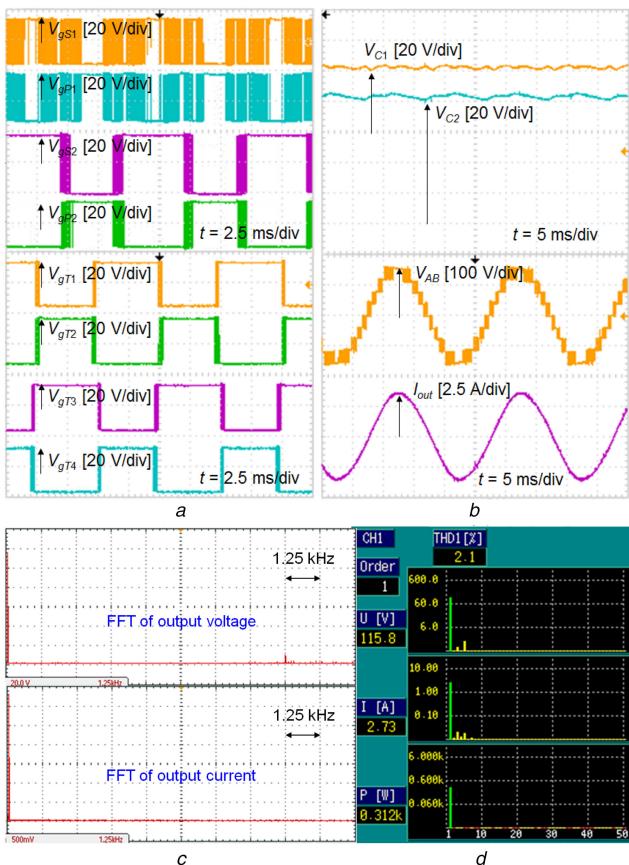
### 6.2 Laboratory results

Then, laboratory prototype was constructed to verify the operating theory of the proposed nine-level SC inverter, as shown in Fig. 9. The experimental parameters of the proposed nine-level SC inverter are also shown in Table 5. Switches  $S_{11}$ ,  $S_{21}$ ,  $S_{23}$ ,  $T_1$ ,  $T_2$ ,  $T_3$ , and  $T_4$  are G30N60 insulated-gate bipolar transistors (IGBTs) with body diodes, and switches  $S_{12}$  and  $S_{22}$  are G30T60 IGBTs. The power diodes are DSE130-60A. Capacitors  $C_1$  and  $C_2$  are 2200  $\mu\text{F}$ /250 V. To generate the control signals under the PD-PWM scheme, a microcontroller (DSP TMS320F28335, Texas Instruments) was used. The experimental results were measured using Tektronix electronic oscilloscopes (TPS 204B, MSO 2024B) and a power quality analyser (Hioki 3197). The output current waveform is measured using a current transducer (LEM LA 25-P). The input DC voltage is created by a three-phase diode rectifier.

Fig. 10 shows the experimental results for the proposed nine-level SC inverter. Fig. 10a shows the control signals of all the



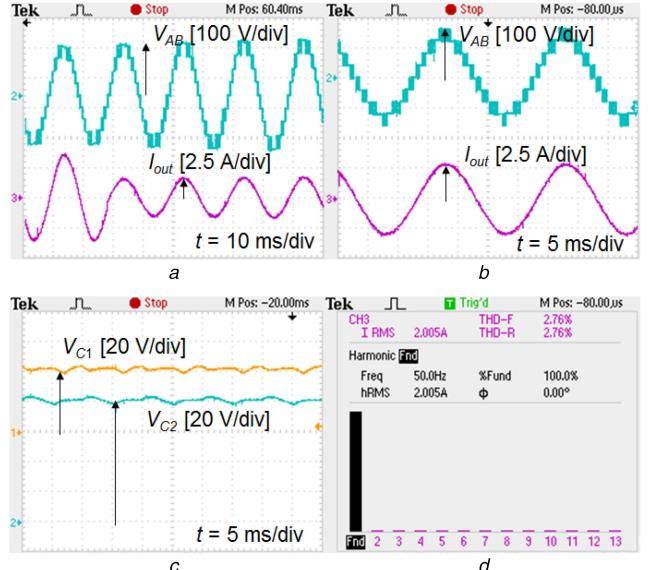
**Fig. 9** Experimental model of the proposed nine-level SC inverter



**Fig. 10** Experimental results for the proposed nine-level SC inverter  
(a) Control signals of  $S_1, P_1, S_2, P_2, T_1, T_2, T_3$  and  $T_4$ , (b) capacitor voltages, output voltage ( $V_{AB}$ ) and output current, (c) FFT of output voltage and output current, (d) harmonics values

switches, and Fig. 10b shows the voltage waveforms of the capacitors. The average voltages of capacitors  $C_1$  and  $C_2$  are 42.8 and 84.3 V, respectively. The voltage of capacitor  $C_1$  in the experiment is lower than the input voltage because the voltage drops on the diode and switches. Fig. 10b also shows the nine-level output voltage, where the current waveform is a sine waveform. Fig. 10c shows the fast Fourier transform (FFT) of the output nine-level voltage waveform ( $V_{AB}$ ), and the output current waveform. Fig. 10d shows the harmonic spectrum at the output measured by the power quality analyser. The measured output voltage is 115.8 V<sub>RMS</sub>; the THD value of the output voltage up to the 50th harmonic is 2.2%, and the output current is 2.73 A<sub>RMS</sub> at a frequency of 50 Hz.

Fig. 11 shows the experimental results of the proposed nine-level SC inverter for various operating conditions. As shown in Fig. 11a when the resistor load changes from 40 to 100  $\Omega$ , the output voltage is slightly increased because of the input voltage fluctuation. A close-loop feedback controller can be used to maintain a constant voltage at the output when either the input voltage or the load changes. Figs. 11b–d show the experimental



**Fig. 11** Experimental results of the proposed nine-level inverter for various operating conditions

(a) Resistor load changes from 40 to 100  $\Omega$  when  $M = 1$ , (b)–(d) Waveforms when  $M = 0.8$  and  $R = 40 \Omega$

**Table 6** Summarised results for peak-to-peak capacitor voltages when  $M = 1$

	Calculation, V	Simulation, V	Experiment, V
$V_{C1P-P}$	8.1	4.4	4.7
$V_{C2P-P}$	10.6	7.8	8.2

results of the proposed inverter when the modulation index is 0.8 and  $R = 40 \Omega$ . The output voltage and current are reduced when the modulation index is decreased from 1 to 0.8.

Table 6 compares the theoretical, simulated, and observed peak-to-peak capacitor voltages. The simulated and observed peak-to-peak capacitor voltages are lower than the values calculated from (5). The reason is that the discharged time intervals of the capacitors in (5) are longer than those in practice.

## 7 Conclusions

A new SCMI topology was proposed to reduce the number of switches. The proposed inverter has fewer components than previous SCMIs. As a result, the size and cost of the power circuit are reduced. An extension of the proposed inverter to 17-level was introduced. By switching the capacitors in series and in parallel, an output voltage larger than the input voltage is obtained. The operating principle and PWM method of the proposed nine-level SC inverter were presented. Moreover, the capacitor voltage ripple and power loss were calculated. Simulation and experimental results were shown to verify the validity of the proposed inverter.

Besides the merit of the component count reduction, the proposed inverter has three limitations: (i) the switching transient number for charging/discharging to reduce switching losses cannot be minimised, (ii) the switching interval is not enough to charge/discharge the capacitors safely, and (iii) the voltage stress of H-bridge switches is equal to the peak output voltage. These limitations are also found in the topology in [20, 21]. The comparison results of the proposed inverter with the inverter in [20, 21] prove the advantages of the proposed inverter in reducing the power loss because a high-voltage rating diode is not used in the proposed inverter. The proposed inverter is suitable for low-power applications with single-phase system. Since the proposed inverter uses the H-bridge circuit in front of load side, it can be used as the cascaded inverter for high-power applications with high number of levels and reduced component count.

## 8 References

- [1] Kouro, S., Malinowski, M., Gopakumar, K., et al.: ‘Recent advances and industrial applications of multilevel converters’, *IEEE Trans. Ind. Electron.*, 2010, **57**, (8), pp. 2553–2580
- [2] Rodriguez, J., Lai, J.S., Peng, F.Z.: ‘Multilevel inverters: a survey of topologies, controls, and applications’, *IEEE Trans. Ind. Electron.*, 2002, **49**, (4), pp. 724–738
- [3] Nabae, A., Takahashi, I., Akagi, H.: ‘A new neutral-point-clamped PWM inverter’, *IEEE Trans. Ind. Appl.*, 1981, **IA-17**, (5), pp. 518–523
- [4] Khazraei, M., Sepahvand, H., Corzine, K.A., et al.: ‘Active capacitor voltage balancing in single-phase flying-capacitor multilevel power converters’, *IEEE Trans. Ind. Electron.*, 2012, **59**, (2), pp. 769–778
- [5] Malinowski, M., Gopakumar, K., Rodriguez, J., et al.: ‘A survey on cascaded multilevel inverters’, *IEEE Trans. Ind. Electron.*, 2010, **57**, (7), pp. 2197–2206
- [6] Barzegarkhoo, R., Zamiri, E., Vosoughi, N., et al.: ‘Cascaded multilevel inverter using series connection of novel capacitor-based units with minimum switch count’, *IET Power Electron.*, 2016, **9**, (10), pp. 2060–2075
- [7] Hajizadeh, M., Fathi, S.H.: ‘Selective harmonic elimination strategy for cascaded H-bridge five-level inverter with arbitrary power sharing among the cells’, *IET Power Electron.*, 2016, **9**, (1), pp. 95–101
- [8] Gupta, K.K., Ranjan, A., Bhatnagar, P., et al.: ‘Multilevel inverter topologies with reduced device count: a review’, *IEEE Trans. Power Electron.*, 2016, **31**, (1), pp. 135–151
- [9] Su, G.J.: ‘Multilevel DC-link inverter’, *IEEE Trans. Ind. Appl.*, 2005, **41**, (3), pp. 848–854
- [10] Ceglia, G., Guzman, V., Sanchez, C., et al.: ‘A new simplified multilevel inverter topology for DC–AC conversion’, *IEEE Trans. Power Electron.*, 2006, **21**, (5), pp. 1311–1319
- [11] Babaei, E.: ‘A cascade multilevel converter topology with reduced number of switches’, *IEEE Trans. Power Electron.*, 2008, **23**, (6), pp. 2657–2664
- [12] Hinago, Y., Koizumi, H.: ‘A switched-capacitor inverter using series/parallel conversion with inductive load’, *IEEE Trans. Ind. Electron.*, 2012, **59**, (2), pp. 878–887
- [13] Tsunoda, A., Hinago, Y., Koizumi, H.: ‘Level- and phase-shifted PWM for seven-level switched-capacitor inverter using series/parallel conversion’, *IEEE Trans. Ind. Electron.*, 2014, **61**, (8), pp. 4011–4021
- [14] Ounejjar, Y., Al-Haddad, K., Gregoire, L.A.: ‘Packed U cells multilevel converter topology: theoretical study and experimental validation’, *IEEE Trans. Ind. Electron.*, 2011, **58**, (4), pp. 1294–1306
- [15] Najafi, E., Yatim, A.H.M.: ‘Design and implementation of a new multilevel inverter topology’, *IEEE Trans. Ind. Electron.*, 2012, **59**, (11), pp. 4148–4154
- [16] Kangarlu, M.F., Babaei, E.: ‘A generalized cascaded multilevel inverter using series connection of submultilevel inverters’, *IEEE Trans. Power Electron.*, 2013, **28**, (2), pp. 625–636
- [17] Ebrahimi, J., Babaei, E., Gharehpetian, G.B.: ‘A new multilevel converter topology with reduced number of power electronic components’, *IEEE Trans. Ind. Electron.*, 2012, **59**, (2), pp. 655–667
- [18] Choi, J.S., Kang, F.S.: ‘Seven-level PWM inverter employing series-connected capacitors paralleled to a single dc voltage source’, *IEEE Trans. Ind. Electron.*, 2015, **62**, (6), pp. 3448–3459
- [19] Babaei, E., Gowgani, S.S.: ‘Hybrid multilevel inverter using switched capacitor units’, *IEEE Trans. Ind. Electron.*, 2014, **61**, (9), pp. 4614–4621
- [20] Barzegarkhoo, R., Kojabadi, H.M., Zamiri, E., et al.: ‘Generalized structure for a single phase switched-capacitor multilevel inverter using a new multiple dc link producer with reduced number of switches’, *IEEE Trans. Power Electron.*, 2016, **31**, (8), pp. 5604–5617
- [21] Zamiri, E., Vosoughi, N., Hosseini, S.H., et al.: ‘A new cascaded switched-capacitor multilevel inverter based on improved series–parallel conversion with less number of components’, *IEEE Trans. Ind. Electron.*, 2016, **63**, (6), pp. 3582–3594
- [22] Liu, J., Wu, J., Zeng, J., et al.: ‘A novel nine-level inverter employing one voltage source and reduced components as high-frequency ac power source’, *IEEE Trans. Power Electron.*, 2017, **32**, (4), pp. 2939–2947
- [23] Ma, M., He, X., Cao, W., et al.: ‘Optimised phase disposition pulse-width modulation strategy for hybrid-clamped multilevel inverters using switching state sequences’, *IET Power Electron.*, 2015, **8**, (7), pp. 1095–1103
- [24] Shi, X., Wang, Z., Tolbert, L., et al.: ‘A comparison of phase disposition and phase shift PWM strategies for modular multilevel converters’. Proc. IEEE Energy Conversion Congress and Exposition (ECCE’2013), Denver, Colorado, USA, 2013, pp. 4089–4096
- [25] McGrath, B.P., Grahame, D.: ‘Multicarrier PWM strategies for multilevel inverter’, *IEEE Trans. Ind. Electron.*, 2002, **49**, (4), pp. 858–867
- [26] Mazumder, S. K.: ‘Hybrid modulation scheme for a high frequency ac link inverter’, *IEEE Trans. Power Electron.*, 2016, **31**, (1), pp. 861–870
- [27] Ren, L., Gong, C., He, K., et al.: ‘Modified hybrid modulation scheme with even switch thermal distribution for H-bridge hybrid cascaded inverters’, *IET Power Electron.*, 2017, **10**, (2), pp. 261–268