```
1  //*************************************************************//
2  //  Class: CECS 361                                            //
3  //  Project: Project1-Cecs361                                  //
4  //                                                             //
5  //  File name: <toplevel_ucf.ucf>                              //
6  //  Abstract: UCF FILE                                         //
7  //  Created by       <Alina Suon> on <09-18-18>.               //
8  //  Copyright © 2018 <Alina Suon>. All rights reserved.        //
9  //
   //                                                                    //
10 //  In submitting this file for class work at CSULB            //
11 //  I am confirming that this is my work and the work          //
12 //  of no one else. In submitting this code I acknowledge that //
13 //  plagiarism in student project work is subject to dismissal.//
14 //  from the class                                             //
15 //*************************************************************//
16
17 ## This file is a general .ucf for the Nexys4 DDR Rev C board
18 ## To use it in a project:
19 ## - uncomment the lines corresponding to used pins
20 ## - rename the used signals according to the project
21
22 ## Clock signal
23 NET "clk"   LOC = "E3"  | IOSTANDARD = "LVCMOS33";             #Bank = 35, Pin name =
   #IO_L12P_T1_MRCC_35,              Sch name = clk100mhz
24 #NET "clk100mhz" TNM_NET = sys_clk_pin;
25 #TIMESPEC TS_sys_clk_pin = PERIOD sys_clk_pin 100 MHz HIGH 50%;
26
27
28 ## Switches
29 NET "uphdnl"          LOC=J15 | IOSTANDARD=LVCMOS33; #IO_L24N_T3_RS0_15
30 #NET "sw<1>"          LOC=L16 | IOSTANDARD=LVCMOS33; #IO_L3N_T0_DQS_EMCCLK_14
31 #NET "sw<2>"          LOC=M13 | IOSTANDARD=LVCMOS33; #IO_L6N_T0_D08_VREF_14
32 #NET "sw<3>"          LOC=R15 | IOSTANDARD=LVCMOS33; #IO_L13N_T2_MRCC_14
33 #NET "sw<4>"          LOC=R17 | IOSTANDARD=LVCMOS33; #IO_L12N_T1_MRCC_14
34 #NET "sw<5>"          LOC=T18 | IOSTANDARD=LVCMOS33; #IO_L7N_T1_D10_14
35 #NET "sw<6>"          LOC=U18 | IOSTANDARD=LVCMOS33; #IO_L17N_T2_A13_D29_14
36 #NET "sw<7>"          LOC=R13 | IOSTANDARD=LVCMOS33; #IO_L5N_T0_D07_14
37 #NET "sw<8>"          LOC=T8 | IOSTANDARD=LVCMOS18; #IO_L24N_T3_34
38 #NET "sw<9>"          LOC=U8 | IOSTANDARD=LVCMOS18; #IO_25_34
39 #NET "sw<10>"         LOC=R16 | IOSTANDARD=LVCMOS33; #IO_L15P_T2_DQS_RDWR_B_14
40 #NET "sw<11>"         LOC=T13 | IOSTANDARD=LVCMOS33; #IO_L23P_T3_A03_D19_14
41 #NET "sw<12>"         LOC=H6 | IOSTANDARD=LVCMOS33; #IO_L24P_T3_35
42 #NET "sw<13>"         LOC=U12 | IOSTANDARD=LVCMOS33; #IO_L20P_T3_A08_D24_14
43 #NET "sw<14>"         LOC=U11 | IOSTANDARD=LVCMOS33; #IO_L19N_T3_A09_D25_VREF_14
44 #NET "sw<15>"         LOC=V10 | IOSTANDARD=LVCMOS33; #IO_L21P_T3_DQS_14
45
46
47 ## Buttons
48 #NET "cpu_resetn"     LOC=C12 | IOSTANDARD=LVCMOS33; #IO_L3P_T0_DQS_AD1P_15
49
50 NET "rst"           LOC=N17 | IOSTANDARD=LVCMOS33; #IO_L9P_T1_DQS_14
51 NET "inc"           LOC=P18 | IOSTANDARD=LVCMOS33; #IO_L9N_T1_DQS_D13_14
52 #NET "btnl"           LOC=P17 | IOSTANDARD=LVCMOS33; #IO_L12P_T1_MRCC_14
53 #NET "btnr"           LOC=M17 | IOSTANDARD=LVCMOS33; #IO_L10N_T1_D15_14
54 #NET "btnu"           LOC=M18 | IOSTANDARD=LVCMOS33; #IO_L4N_T0_D05_14
55
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56
57  ## LEDs
58  #NET "led<0>"          LOC=H17 | IOSTANDARD=LVCMOS33; #IO_L18P_T2_A24_15
59  #NET "led<1>"          LOC=K15 | IOSTANDARD=LVCMOS33; #IO_L24P_T3_RS1_15
60  #NET "led<2>"          LOC=J13 | IOSTANDARD=LVCMOS33; #IO_L17N_T2_A25_15
61  #NET "led<3>"          LOC=N14 | IOSTANDARD=LVCMOS33; #IO_L8P_T1_D11_14
62  #NET "led<4>"          LOC=R18 | IOSTANDARD=LVCMOS33; #IO_L7P_T1_D09_14
63  #NET "led<5>"          LOC=V17 | IOSTANDARD=LVCMOS33; #IO_L18N_T2_A11_D27_14
64  #NET "led<6>"          LOC=U17 | IOSTANDARD=LVCMOS33; #IO_L17P_T2_A14_D30_14
65  #NET "led<7>"          LOC=U16 | IOSTANDARD=LVCMOS33; #IO_L18P_T2_A12_D28_14
66  #NET "led<8>"          LOC=V16 | IOSTANDARD=LVCMOS33; #IO_L16N_T2_A15_D31_14
67  #NET "led<9>"          LOC=T15 | IOSTANDARD=LVCMOS33; #IO_L14N_T2_SRCC_14
68  #NET "led<10>"         LOC=U14 | IOSTANDARD=LVCMOS33; #IO_L22P_T3_A05_D21_14
69  #NET "led<11>"         LOC=T16 | IOSTANDARD=LVCMOS33; #IO_L15N_T2_DQS_DOUT_CSO_B_14
70  #NET "led<12>"         LOC=V15 | IOSTANDARD=LVCMOS33; #IO_L16P_T2_CSI_B_14
71  #NET "led<13>"         LOC=V14 | IOSTANDARD=LVCMOS33; #IO_L22N_T3_A04_D20_14
72  #NET "led<14>"         LOC=V12 | IOSTANDARD=LVCMOS33; #IO_L20N_T3_A07_D23_14
73  #NET "led<15>"         LOC=V11 | IOSTANDARD=LVCMOS33; #IO_L21N_T3_DQS_A06_D22_14
74
75
76  ##LEDs_RGB
77  #NET "led16_b"         LOC=R12 | IOSTANDARD=LVCMOS33; #IO_L5P_T0_D06_14
78  #NET "led16_g"         LOC=M16 | IOSTANDARD=LVCMOS33; #IO_L10P_T1_D14_14
79  #NET "led16_r"         LOC=N15 | IOSTANDARD=LVCMOS33; #IO_L11P_T1_SRCC_14
80  #NET "led17_b"         LOC=G14 | IOSTANDARD=LVCMOS33; #IO_L15N_T2_DQS_ADV_B_15
81  #NET "led17_g"         LOC=R11 | IOSTANDARD=LVCMOS33; #IO_0_14
82  #NET "led17_r"         LOC=N16 | IOSTANDARD=LVCMOS33; #IO_L11N_T1_SRCC_14
83
84
85  ## 7 segment display
86  NET "a"              LOC=T10 | IOSTANDARD=LVCMOS33; #IO_L24N_T3_A00_D16_14
87  NET "b"              LOC=R10 | IOSTANDARD=LVCMOS33; #IO_25_14
88  NET "c"              LOC=K16 | IOSTANDARD=LVCMOS33; #IO_25_15
89  NET "d"              LOC=K13 | IOSTANDARD=LVCMOS33; #IO_L17P_T2_A26_15
90  NET "e"              LOC=P15 | IOSTANDARD=LVCMOS33; #IO_L13P_T2_MRCC_14
91  NET "f"              LOC=T11 | IOSTANDARD=LVCMOS33; #IO_L19P_T3_A10_D26_14
92  NET "g"              LOC=L18 | IOSTANDARD=LVCMOS33; #IO_L4P_T0_D04_14
93  #NET "dp"              LOC=H15 | IOSTANDARD=LVCMOS33; #IO_L19N_T3_A21_VREF_15
94
95  NET "anode<0>"           LOC=J17 | IOSTANDARD=LVCMOS33; #IO_L23P_T3_FOE_B_15
96  NET "anode<1>"           LOC=J18 | IOSTANDARD=LVCMOS33; #IO_L23N_T3_FWE_B_15
97  NET "anode<2>"           LOC=T9 | IOSTANDARD=LVCMOS33; #IO_L24P_T3_A01_D17_14
98  NET "anode<3>"           LOC=J14 | IOSTANDARD=LVCMOS33; #IO_L19P_T3_A22_15
99  NET "anode<4>"           LOC=P14 | IOSTANDARD=LVCMOS33; #IO_L8N_T1_D12_14
100 NET "anode<5>"           LOC=T14 | IOSTANDARD=LVCMOS33; #IO_L14P_T2_SRCC_14
101 NET "anode<6>"           LOC=K2 | IOSTANDARD=LVCMOS33; #IO_L23P_T3_35
102 NET "anode<7>"           LOC=U13 | IOSTANDARD=LVCMOS33; #IO_L23N_T3_A02_D18_14
103
104
105 ## Pmod Header JA
106 #NET "ja<1>"           LOC=C17 | IOSTANDARD=LVCMOS33; #IO_L20N_T3_A19_15
107 #NET "ja<2>"           LOC=D18 | IOSTANDARD=LVCMOS33; #IO_L21N_T3_DQS_A18_15
108 #NET "ja<3>"           LOC=E18 | IOSTANDARD=LVCMOS33; #IO_L21P_T3_DQS_15
109 #NET "ja<4>"           LOC=G17 | IOSTANDARD=LVCMOS33; #IO_L18N_T2_A23_15
110 #NET "ja<7>"           LOC=D17 | IOSTANDARD=LVCMOS33; #IO_L16N_T2_A27_15
111 #NET "ja<8>"           LOC=E17 | IOSTANDARD=LVCMOS33; #IO_L16P_T2_A28_15
112 #NET "ja<9>"           LOC=F18 | IOSTANDARD=LVCMOS33; #IO_L22N_T3_A16_15
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113   #NET "ja<10>"          LOC=G18 | IOSTANDARD=LVCMOS33; #IO_L22P_T3_A17_15
114
115   ## Pmod Header JB
116   #NET "jb<1>"           LOC=D14 | IOSTANDARD=LVCMOS33; #IO_L1P_T0_AD0P_15
117   #NET "jb<2>"           LOC=F16 | IOSTANDARD=LVCMOS33; #IO_L14N_T2_SRCC_15
118   #NET "jb<3>"           LOC=G16 | IOSTANDARD=LVCMOS33; #IO_L13N_T2_MRCC_15
119   #NET "jb<4>"           LOC=H14 | IOSTANDARD=LVCMOS33; #IO_L15P_T2_DQS_15
120   #NET "jb<7>"           LOC=E16 | IOSTANDARD=LVCMOS33; #IO_L11N_T1_SRCC_15
121   #NET "jb<8>"           LOC=F13 | IOSTANDARD=LVCMOS33; #IO_L5P_T0_AD9P_15
122   #NET "jb<9>"           LOC=G13 | IOSTANDARD=LVCMOS33; #IO_0_15
123   #NET "jb<10>"          LOC=H16 | IOSTANDARD=LVCMOS33; #IO_L13P_T2_MRCC_15
124
125   ## Pmod Header JC
126   #NET "jc<1>"           LOC=K1 | IOSTANDARD=LVCMOS33; #IO_L23N_T3_35
127   #NET "jc<2>"           LOC=F6 | IOSTANDARD=LVCMOS33; #IO_L19N_T3_VREF_35
128   #NET "jc<3>"           LOC=J2 | IOSTANDARD=LVCMOS33; #IO_L22N_T3_35
129   #NET "jc<4>"           LOC=G6 | IOSTANDARD=LVCMOS33; #IO_L19P_T3_35
130   #NET "jc<7>"           LOC=E7 | IOSTANDARD=LVCMOS33; #IO_L6P_T0_35
131   #NET "jc<8>"           LOC=J3 | IOSTANDARD=LVCMOS33; #IO_L22P_T3_35
132   #NET "jc<9>"           LOC=J4 | IOSTANDARD=LVCMOS33; #IO_L21P_T3_DQS_35
133   #NET "jc<10>"          LOC=E6 | IOSTANDARD=LVCMOS33; #IO_L5P_T0_AD13P_35
134
135   ## Pmod Header JD
136   #NET "jd<1>"           LOC=H4 | IOSTANDARD=LVCMOS33; #IO_L21N_T3_DQS_35
137   #NET "jd<2>"           LOC=H1 | IOSTANDARD=LVCMOS33; #IO_L17P_T2_35
138   #NET "jd<3>"           LOC=G1 | IOSTANDARD=LVCMOS33; #IO_L17N_T2_35
139   #NET "jd<4>"           LOC=G3 | IOSTANDARD=LVCMOS33; #IO_L20N_T3_35
140   #NET "jd<7>"           LOC=H2 | IOSTANDARD=LVCMOS33; #IO_L15P_T2_DQS_35
141   #NET "jd<8>"           LOC=G4 | IOSTANDARD=LVCMOS33; #IO_L20P_T3_35
142   #NET "jd<9>"           LOC=G2 | IOSTANDARD=LVCMOS33; #IO_L15N_T2_DQS_35
143   #NET "jd<10>"          LOC=F3 | IOSTANDARD=LVCMOS33; #IO_L13N_T2_MRCC_35
144
145   ##Pmod Header JXADC
146   #NET "xa_n<1>"         LOC=A14 | IOSTANDARD=LVDS; #IO_L9N_T1_DQS_AD3N_15
147   #NET "xa_p<1>"         LOC=A13 | IOSTANDARD=LVDS; #IO_L9P_T1_DQS_AD3P_15
148   #NET "xa_n<2>"         LOC=A16 | IOSTANDARD=LVDS; #IO_L8N_T1_AD10N_15
149   #NET "xa_p<2>"         LOC=A15 | IOSTANDARD=LVDS; #IO_L8P_T1_AD10P_15
150   #NET "xa_n<3>"         LOC=B17 | IOSTANDARD=LVDS; #IO_L7N_T1_AD2N_15
151   #NET "xa_p<3>"         LOC=B16 | IOSTANDARD=LVDS; #IO_L7P_T1_AD2P_15
152   #NET "xa_n<4>"         LOC=A18 | IOSTANDARD=LVDS; #IO_L10N_T1_AD11N_15
153   #NET "xa_p<4>"         LOC=B18 | IOSTANDARD=LVDS; #IO_L10P_T1_AD11P_15
154
155
156   ##VGA Connector
157   #NET "vga_r<0>"        LOC=A3 | IOSTANDARD=LVCMOS33; #IO_L8N_T1_AD14N_35
158   #NET "vga_r<1>"        LOC=B4 | IOSTANDARD=LVCMOS33; #IO_L7N_T1_AD6N_35
159   #NET "vga_r<2>"        LOC=C5 | IOSTANDARD=LVCMOS33; #IO_L1N_T0_AD4N_35
160   #NET "vga_r<3>"        LOC=A4 | IOSTANDARD=LVCMOS33; #IO_L8P_T1_AD14P_35
161
162   #NET "vga_g<0>"        LOC=C6 | IOSTANDARD=LVCMOS33; #IO_L1P_T0_AD4P_35
163   #NET "vga_g<1>"        LOC=A5 | IOSTANDARD=LVCMOS33; #IO_L3N_T0_DQS_AD5N_35
164   #NET "vga_g<2>"        LOC=B6 | IOSTANDARD=LVCMOS33; #IO_L2N_T0_AD12N_35
165   #NET "vga_g<3>"        LOC=A6 | IOSTANDARD=LVCMOS33; #IO_L3P_T0_DQS_AD5P_35
166
167   #NET "vga_b<0>"        LOC=B7 | IOSTANDARD=LVCMOS33; #IO_L2P_T0_AD12P_35
168   #NET "vga_b<1>"        LOC=C7 | IOSTANDARD=LVCMOS33; #IO_L4N_T0_35
169   #NET "vga_b<2>"        LOC=D7 | IOSTANDARD=LVCMOS33; #IO_L6N_T0_VREF_35
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170   #NET "vga_b<3>"       LOC=D8 | IOSTANDARD=LVCMOS33; #IO_L4P_T0_35
171
172   #NET "vga_hs"         LOC=B11 | IOSTANDARD=LVCMOS33; #IO_L4P_T0_15
173   #NET "vga_vs"         LOC=B12 | IOSTANDARD=LVCMOS33; #IO_L3N_T0_DQS_AD1N_15
174
175
176   ##Micro SD Connector
177   #NET "sd_sck"         LOC=B1 | IOSTANDARD=LVCMOS33; #IO_L9P_T1_DQS_AD7P_35
178   #NET "sd_reset"       LOC=E2 | IOSTANDARD=LVCMOS33; #IO_L14P_T2_SRCC_35
179   #NET "sd_cd"          LOC=A1 | IOSTANDARD=LVCMOS33; #IO_L9N_T1_DQS_AD7N_35
180   #NET "sd_cmd"         LOC=C1 | IOSTANDARD=LVCMOS33; #IO_L16N_T2_35
181   #NET "sd_dat<0>"      LOC=C2 | IOSTANDARD=LVCMOS33; #IO_L16P_T2_35
182   #NET "sd_dat<1>"      LOC=E1 | IOSTANDARD=LVCMOS33; #IO_L18N_T2_35
183   #NET "sd_dat<2>"      LOC=F1 | IOSTANDARD=LVCMOS33; #IO_L18P_T2_35
184   #NET "sd_dat<3>"      LOC=D2 | IOSTANDARD=LVCMOS33; #IO_L14N_T2_SRCC_35
185
186
187   ##PWM Audio Amplifier
188   #NET "aud_pwm"        LOC=A11 | IOSTANDARD=LVCMOS33; #IO_L4N_T0_15
189   #NET "aud_sd"         LOC=D12 | IOSTANDARD=LVCMOS33; #IO_L6P_T0_15
190
191
192   ##Accelerometer
193   #NET "acl_miso"       LOC=E15 | IOSTANDARD=LVCMOS33; #IO_L11P_T1_SRCC_15
194   #NET "acl_mosi"       LOC=F14 | IOSTANDARD=LVCMOS33; #IO_L5N_T0_AD9N_15
195   #NET "acl_sclk"       LOC=F15 | IOSTANDARD=LVCMOS33; #IO_L14P_T2_SRCC_15
196   #NET "acl_csn"        LOC=D15 | IOSTANDARD=LVCMOS33; #IO_L12P_T1_MRCC_15
197   #NET "acl_int<1>"     LOC=B13 | IOSTANDARD=LVCMOS33; #IO_L2P_T0_AD8P_15
198   #NET "acl_int<2>"     LOC=C16 | IOSTANDARD=LVCMOS33; #IO_L20P_T3_A20_15
199
200
201   ##Temperature Sensor
202   #NET "tmp_ct"         LOC=B14 | IOSTANDARD=LVCMOS33; #IO_L2N_T0_AD8N_15
203   #NET "tmp_int"        LOC=D13 | IOSTANDARD=LVCMOS33; #IO_L6N_T0_VREF_15
204   #NET "tmp_scl"        LOC=C14 | IOSTANDARD=LVCMOS33; #IO_L1N_T0_AD0N_15
205   #NET "tmp_sda"        LOC=C15 | IOSTANDARD=LVCMOS33; #IO_L12N_T1_MRCC_15
206
207
208   ##USB-RS232 Interface
209   #NET "uart_cts"       LOC=D3 | IOSTANDARD=LVCMOS33; #IO_L12N_T1_MRCC_35
210   #NET "uart_rts"       LOC=E5 | IOSTANDARD=LVCMOS33; #IO_L5N_T0_AD13N_35
211   #NET "uart_rxd_out"   LOC=D4 | IOSTANDARD=LVCMOS33; #IO_L11N_T1_SRCC_35
212   #NET "uart_txd_in"    LOC=C4 | IOSTANDARD=LVCMOS33; #IO_L7P_T1_AD6P_35
213
214
215   ##Omnidirectional Microphone
216   #NET "m_clk"          LOC=J5 | IOSTANDARD=LVCMOS33; #IO_25_35
217   #NET "m_data"         LOC=H5 | IOSTANDARD=LVCMOS33; #IO_L24N_T3_35
218   #NET "m_lrsel"        LOC=F5 | IOSTANDARD=LVCMOS33; #IO_0_35
219
220
221   ##USB HID (PS/2)
222   #NET "ps2_clk"        LOC=F4 | IOSTANDARD=LVCMOS33; #IO_L13P_T2_MRCC_35
223   #NET "ps2_data"       LOC=B2 | IOSTANDARD=LVCMOS33; #IO_L10N_T1_AD15N_35
224
225
226   ##Quad SPI Flash
```

```
227   #NET "qspi_csn"       LOC=L13 | IOSTANDARD=LVCMOS33; #IO_L6P_T0_FCS_B_14
228   #NET "qspi_dq<0>"     LOC=K17 | IOSTANDARD=LVCMOS33; #IO_L1P_T0_D00_MOSI_14
229   #NET "qspi_dq<1>"     LOC=K18 | IOSTANDARD=LVCMOS33; #IO_L1N_T0_D01_DIN_14
230   #NET "qspi_dq<2>"     LOC=L14 | IOSTANDARD=LVCMOS33; #IO_L2P_T0_D02_14
231   #NET "qspi_dq<3>"     LOC=M14 | IOSTANDARD=LVCMOS33; #IO_L2N_T0_D03_14
232
233
234   ##SMSC Ethernet PHY
235   #NET "eth_rxd<0>"     LOC=C11 | IOSTANDARD=LVCMOS33; #IO_L13P_T2_MRCC_16
236   #NET "eth_rxd<1>"     LOC=D10 | IOSTANDARD=LVCMOS33; #IO_L19N_T3_VREF_16
237   #NET "eth_txd<0>"     LOC=A10 | IOSTANDARD=LVCMOS33; #IO_L14P_T2_SRCC_16
238   #NET "eth_txd<1>"     LOC=A8 | IOSTANDARD=LVCMOS33; #IO_L12N_T1_MRCC_16
239   #NET "eth_crsdv"      LOC=D9 | IOSTANDARD=LVCMOS33; #IO_L6N_T0_VREF_16
240   #NET "eth_intn"       LOC=B8 | IOSTANDARD=LVCMOS33; #IO_L12P_T1_MRCC_16
241   #NET "eth_mdc"        LOC=C9 | IOSTANDARD=LVCMOS33; #IO_L11P_T1_SRCC_16
242   #NET "eth_mdio"       LOC=A9 | IOSTANDARD=LVCMOS33; #IO_L14N_T2_SRCC_16
243   #NET "eth_refclk"     LOC=D5 | IOSTANDARD=LVCMOS33; #IO_L11P_T1_SRCC_35
244   #NET "eth_rstn"       LOC=B3 | IOSTANDARD=LVCMOS33; #IO_L10P_T1_AD15P_35
245   #NET "eth_txen"       LOC=B9 | IOSTANDARD=LVCMOS33; #IO_L11N_T1_SRCC_16
246   #NET "eth_rxerr"      LOC=C10 | IOSTANDARD=LVCMOS33; #IO_L13N_T2_MRCC_16
```