```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   //  Class: CECS 361                                                             //
4   //  Project: Project1-Cecs361                                                   //
5   //                                                                              //
6   //  File name: <testbench.v>                                                    //
7   //  Abstract: Test fixture                                                      //
8   //  Created by       <Alina Suon> on <09-18-18>.                                //
9   //  Copyright © 2018 <Alina Suon>. All rights reserved.                         //
10  //                                                                              //
    //                                                                                  //
11  //  In submitting this file for class work at CSULB                             //
12  //  I am confirming that this is my work and the work                           //
13  //  of no one else. In submitting this code I acknowledge that                  //
14  //  plagiarism in student project work is subject to dismissal.                 //
15  //  from the class                                                              //
16  //////////////////////////////////////////////////////////////////////////////////
17
18  module testbench;
19     // Inputs
20     reg clk;
21     reg reset;
22     reg inc;
23     reg uphdnl;
24     // Outputs
25     wire [7:0] anode;
26     wire a;
27     wire b;
28     wire c;
29     wire d;
30     wire e;
31     wire f;
32     wire g;
33  // Instantiate the Unit Under Test (UUT)
34     Top_Level uut (.clk(clk), .reset(reset), .inc(inc),
35                    .uphdnl(uphdnl), .anode(anode), .a(a),
36                    .b(b), .c(c), .d(d), .e(e), .f(f), .g(g));
37     always #5 clk= ~clk;
38     initial
39     begin
40  // Initialize Inputs
41        clk = 0;
42        reset = 1;
43        inc = 0;
44        uphdnl = 0;
45  // Wait 100 ns for global reset to finish
46        #100 reset = 0;
47  // Add stimulus here
48        #100 inc = 1;
49     end
50  endmodule
51
52
```