```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   //                                                                              //
4   //  Class: CECS 360                                                             //
5   //  Project name: Project1_CECS360                                              //
6   //  File name: AISO.v                                                           //
7   //                                                                              //
8   //  Created by Umar Khan on 09/16/2017                                          //
9   //                                                                              //
10  //  Abstract: Helps with the violation of timing constraints.                   //
11  //                                                                              //
12  //////////////////////////////////////////////////////////////////////////////////
13
14  module AISO(clk,reset, R_Sync);
15
16     input clk, reset;
17     output R_Sync;
18     wire R_sync;
19     reg F1, F2;
20
21     always @ (posedge clk, posedge reset) begin
22
23        if (reset)
24           {F1,F2} <= 2'B00;
25        else
26           {F1,F2} <= {1'b1,F1};
27        end
28
29        assign R_Sync = !F2;
30
31  endmodule
32
```