Project 1

Synchronous Design

Counter with Display

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CECS 360

09/21/2017

Introduction:

This project shows the synchronous design with the counter on the display. The switches are used for incrementing and decrementing the counter. The incrementing and decrementing depends on the switch on being up or down, however they are set in the counter. The up-switch increments and down-switch decrements. The project contains multiple modules in it i.e. AISO, Debounce, Pulse Maker, Counter, and Display Controller where all of them were instantiated in the top level.

Major Block Description:

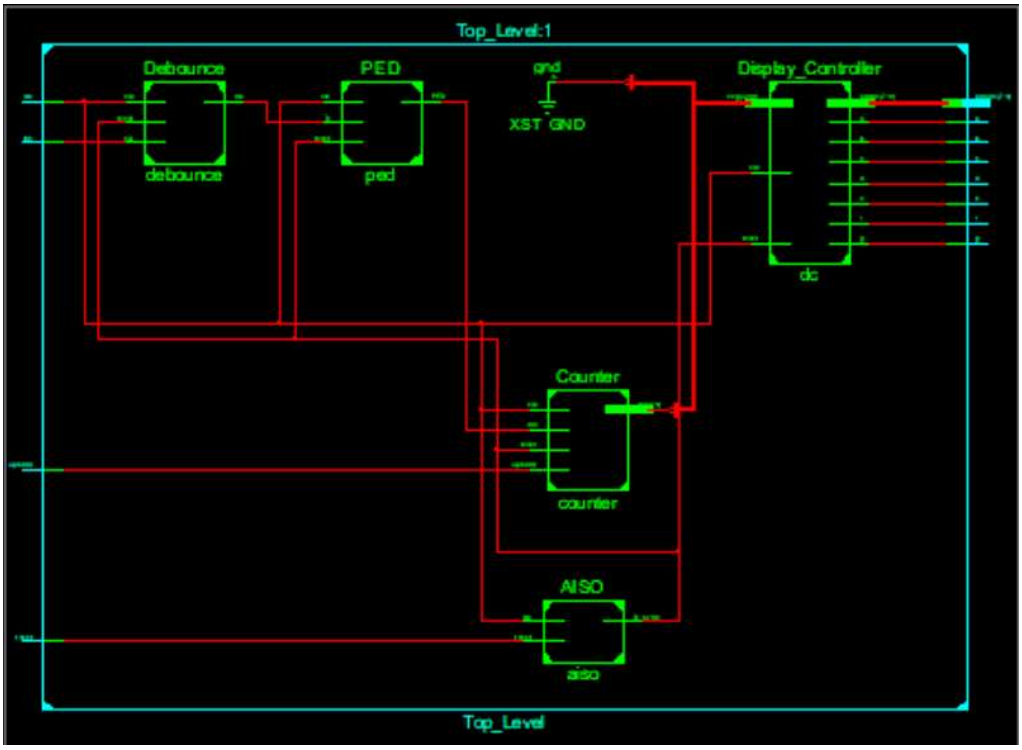
- Debounce: This block of the project stabilizes the output instead of showing too many transitions. Pulse maker is instantiated within the debounce.
    - Pulse Maker: This module generates a tick every 10ms.
- AISO: This module helps with the violation of timing constraints. This module defines the Asynchronous In and Synchronous out idea.
- PED: This module detects the positive edge of the clock. This is done since the output only changes on the positive edge of the clock.
- Counter: This is the module where incrementing and decrementing is done based on the condition of the switch. The switch is set as “Up High Down Low”.
- Display Controller: This is the module where the 7-segment module is instantiated and controlled using led clock, led controller, ad mux, and hex to 7 segment.
    - Led Clock: This is the module where frequency of clk_out is determined by integer count, count = (Incoming Freq/(Outgoing Freq))/2. Clk_out will alternate once every time clk_in alternates 'count' number of times. To achieve a refresh rate of 60Hz with 8 pixels, the output frequency must be 480hz. [Outgoing Freq = (Refresh Rate * Number of Pixels)] To produce an output clock of 480hz, we divide the clock every 104167 cycles. We assume that clk_in from the Nexys 4 FPGA is 100mhz.
    - Led Controller: This is the module that clock as an input. At every posedge clock, Moore state machines will increment the states regardless of the clock value (which always remains 1). Every state will output corresponding to the bit value of the a.

    - Ad Mux: This is the module where the 8 to 1 bit mux with 3 bit select is created and the output is determined by the 3 bit select.
    - Hex to 7 Segment: This module uses input hex and decodes the value to its equivalent representation for the NEXYS 4 seven segment display.
- TopLevel_UCF: This is the module where all the blocks are linked to the NEXYS 4 board.

Hierarchy:

- Top_Level
    - Debounce
        - Pulse_Maker
    - AISO
    - PED
    - Counter
    - Display Controller
        - Led_Clk
        - Led_Controller
        - Ad_Mux
        - Hex_to_7seg
    - Toplevel_ucf

RTL Schematic:



Conclusion:

In conclusion, using AISO module allowed us not to violate timing constraints and successfully make the Counter which decrements when the switch is set to low and vice versa. Also, Debounce stabilizes the output of the clock. The debounce was built referred to Pong Chu’s style. The counter is displayed on the board using the display controller. The counter can display 8-bit values or 16 bit values on the board.