```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   //                                                                              //
4   //  Class: CECS 360                                                             //
5   //  Project name: Project1_CECS360                                              //
6   //  File name: PED.v                                                            //
7   //                                                                              //
8   //  Created by Umar Khan 09/19/2017                                             //
9   //                                                                              //
10  //  Abstract: Detects the positive edge of the clock  .                         //
11  //            It detects the PED as the output will only                        //
12  //            change on the PED                                                 //
13  //                                                                              //
14  //////////////////////////////////////////////////////////////////////////////////
15  module PED(clk, reset, D, PED);
16
17     input clk, reset, D;
18
19     output PED;
20     wire PED;
21
22     reg F1;
23
24     always @ (posedge clk, posedge reset) begin
25        if (reset)
26           F1 <= 1'b00;
27        else
28           F1 <= D;
29        end
30
31     assign PED = {~F1 & D};
32
33  endmodule
34
35
```