```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   //  Class: CECS 361                                                             //
4   //  Project: Project1-Cecs361                                                   //
5   //                                                                              //
6   //  File name: <makePulse.v>                                                    //
7   //  Abstract: Make a pulse every 10ms.                                          //
8   //  Created by       <Alina Suon> on <09-18-18>.                                //
9   //  Copyright © 2018 <Alina Suon>. All rights reserved.                         //
10  //                                                                              //
    //                                                                                  //
11  //  In submitting this file for class work at CSULB                             //
12  //  I am confirming that this is my work and the work                           //
13  //  of no one else. In submitting this code I acknowledge that                  //
14  //  plagiarism in student project work is subject to dismissal.                 //
15  //  from the class                                                              //
16  //////////////////////////////////////////////////////////////////////////////////
17
18  module makePulse(clk, rst, pulse);
19     input        clk, rst;
20     output       pulse;
21     reg   [19:0] count;     //20 bit count
22
23     assign pulse = (count == 999999);
24
25     always @ (posedge clk, posedge rst)
26        if(rst)  count <= 20'b0;
27     else
28        if(pulse) count <= 20'b0;
29     else
30        count<= count + 20'b1;
31  endmodule
32
```