```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////
3   //  Class: CECS 361                                             //
4   //  Project: Project1-Cecs361                                   //
5   //                                                              //
6   //  File name: <PED.v>                                          //
7   //  Abstract: This module will detect the positive edge of the  //
8   //            clock specifically as an output. The output       //
9   //            can only change on the positive edge dectect.     //
10  //  Created by       <Alina Suon> on <09-18-18>.                //
11  //  Copyright © 2018 <Alina Suon>. All rights reserved.         //
12  //
    //                                                                    //
13  //  In submitting this file for class work at CSULB             //
14  //  I am confirming that this is my work and the work           //
15  //  of no one else. In submitting this code I acknowledge that  //
16  //  plagiarism in student project work is subject to dismissal.  //
17  //  from the class                                              //
18  //////////////////////////////////////////////////////////////////
19  module PED(clk, rst, d, PED);
20     input    clk, rst, d;
21     output   PED;
22     wire     PED;
23     reg      f1;
24
25     always @ (posedge clk, posedge rst)
26     begin
27        if (rst)
28           f1 <= 1'b00;
29        else
30           f1 <= d;
31     end
32     assign PED = {~f1 & d};
33  endmodule
34
35
```