```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   //  Class: CECS 361                                                             //
4   //  Project: Project1-Cecs361                                                   //
5   //                                                                              //
6   //  File name: <adMux.v>                                                        //
7   //  Abstract: An 8 to 1 mux that has a select of 3 bits.                        //
8   //  Created by       <Alina Suon> on <09-18-18>.                                //
9   //  Copyright © 2018 <Alina Suon>. All rights reserved.                         //
10  //                                                                              //
    //                                                                                  //
11  //  In submitting this file for class work at CSULB                             //
12  //  I am confirming that this is my work and the work                           //
13  //  of no one else. In submitting this code I acknowledge that                  //
14  //  plagiarism in student project work is subject to dismissal.                 //
15  //  from the class                                                              //
16  //////////////////////////////////////////////////////////////////////////////////
17  module adMux(seqSel, d0, d1, d2, d3, d4, d5, d6, d7, y);
18     input [2:0]   seqSel;
19     input [15:12] d0;
20     input [11:8]  d1;
21     input [7:4]   d2;
22     input [3:0]   d3;
23     input [15:12] d4;
24     input [11:8]  d5;
25     input [7:4]   d6;
26     input [3:0]   d7;
27     output[3:0]   y;     //y = output to the hex7seg
28     reg   [3:0]   y;
29
30     always @(*) begin
31        case(seqSel)
32           3'b000: y = d0;
33           3'b001: y = d1;
34           3'b010: y = d2;
35           3'b011: y = d3;
36           3'b100: y = d4;
37           3'b101: y = d5;
38           3'b110: y = d6;
39           3'b111: y = d7;
40        endcase
41     end
42  endmodule
43
```