```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////
3   //                                                              //
4   //  Class: CECS 360                                             //
5   //  Project name: Project1_CECS360                              //
6   //  File name: hex_to_7seg.v                                    //
7   //                                                              //
8   //  Created by Umar Khan 09/19/2017       .                     //
9   //                                                              //
10  //  Abstract: 8-to-1 4bit mux with 3 bit select(Sel). Output (y)
11  //            is always set to only one specific 4 bit input    //
12  //            (d7,d6,d5,d4,d3,d2,d1,d0)                         //
13  //            that is determined by the 3 bit select(seq_sel).  //
14  //////////////////////////////////////////////////////////////////
15  ////////////////////////////////////////////////////////////////////
16  module ad_mux(seq_sel, d0, d1, d2, d3, d4, d5, d6, d7, y);
17
18     input    [2:0]    seq_sel;
19     input    [15:12]  d0;
20     input    [11:8]   d1;
21     input    [7:4]    d2;
22     input    [3:0]    d3;
23     input    [15:12]  d4;
24     input    [11:8]   d5;
25     input    [7:4]    d6;
26     input    [3:0]    d7;
27
28     output   [3:0]    y;     //output to the hex_to_7seg
29
30     reg      [3:0]    y;
31
32     always @(*) begin
33        case(seq_sel)
34           3'b000:     y = d0;
35           3'b001:     y = d1;
36           3'b010:     y = d2;
37           3'b011:     y = d3;
38           3'b100:     y = d4;
39           3'b101:     y = d5;
40           3'b110:     y = d6;
41           3'b111:     y = d7;
42        endcase
43     end
44
45  endmodule
46
```