```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   //                                                                              //
4   //  Class: CECS 360                                                             //
5   //  Project name: Project1_CECS360                                              //
6   //  File name: Top_Level.v                                                      //
7   //                                                                              //
8   //  Created by Umar Khan 09/19/2017                                             //
9   //                                                                              //
10  //  Abstract: Instantiation of all the modules.                                 //
11  //                                                                              //
12  //////////////////////////////////////////////////////////////////////////////////
13  module Top_Level (clk, reset, inc, uphdnl, anode, a, b, c, d, e, f, g);
14
15      input  clk, reset, inc, uphdnl;
16
17      output [7:0] anode;
18      output a, b, c, d, e, f, g;
19
20      wire   [31:0] q;
21      wire   PED;
22      wire   reset_out;
23      wire   deb;
24
25
26      Debounce
27        debounce(clk, reset_out, inc, deb);
28
29      AISO
30        aiso(clk, reset, reset_out);
31
32      PED
33        ped(clk, reset_out, deb, PED);
34
35      Counter
36        counter(clk, reset_out, PED, uphdnl, q);
37
38      Display_Controller
39        dc(clk, reset_out, anode, q, a, b ,c ,d ,e, f,g);
40
41  endmodule
42
```