```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////
3   //  Class: CECS 361                                             //
4   //  Project: Project1-Cecs361                                   //
5   //                                                              //
6   //  File name: <aiso.v>                                         //
7   //  Abstract: Support timing constraints that are violated.     //
8   //  Created by       <Alina Suon> on <09-18-18>.                //
9   //  Copyright © 2018 <Alina Suon>. All rights reserved.         //
10  //                                                              //
    //                                                                  //
11  //  In submitting this file for class work at CSULB             //
12  //  I am confirming that this is my work and the work           //
13  //  of no one else. In submitting this code I acknowledge that  //
14  //  plagiarism in student project work is subject to dismissal.  //
15  //  from the class                                              //
16  //////////////////////////////////////////////////////////////////
17
18  module aiso(clk,rst, rst_sync);
19     input clk, rst;
20     output rst_sync;
21     wire rst_sync;
22     reg f1, f2;
23
24     always @ (posedge clk, posedge rst)
25        begin
26        if (rst)
27           {f1,f2} <= 2'B00;
28        else
29           {f1,f2} <= {1'b1,f1};
30        end
31     assign rst_sync = !f2;
32  endmodule
33
```