```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   //  Class: CECS 361                                                             //
4   //  Project: Project1-Cecs361                                                   //
5   //                                                                              //
6   //  File name: <displayController.v>                                            //
7   //  Abstract: This module instantiates the modules required for                 //
8   //             the 7 segment display.                                           //
9   //  Created by       <Alina Suon> on <09-18-18>.                                //
10  //  Copyright © 2018 <Alina Suon>. All rights reserved.                         //
11  //
    //                                                                                      //
12  //  In submitting this file for class work at CSULB                             //
13  //  I am confirming that this is my work and the work                           //
14  //  of no one else. In submitting this code I acknowledge that                  //
15  //  plagiarism in student project work is subject to dismissal.                 //
16  //  from the class                                                              //
17  //////////////////////////////////////////////////////////////////////////////////
18  module displayController(clk, rst, anode, seg, a, b, c, d, e, f, g);
19     input clk, rst;
20     input [31:0] seg;
21     output [7:0] anode;
22     output a, b, c, d, e, f, g;
23     wire led_cout;
24     wire [2:0] sel;
25     wire [3:0] y;
26    //Instantiate modules for 7 seg display
27     ledClk         a1 (clk, rst, led_cout);
28     ledController  a2 (led_cout, rst, anode, sel);
29     adMux          a3 (sel, seg[31:28], seg[27:24], seg[23:20],
30                        seg[19:16], seg[15:12], seg[11:8],
31                        seg[7:4], seg[3:0], y);
32     hex7seg        a4 (y, a, b, c, d, e, f, g);
33  endmodule
34
35
```