```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////
3   //  Class: CECS 361                                             //
4   //  Project: Project1-Cecs361                                   //
5   //                                                              //
6   //  File name: <counter.v>                                      //
7   //  Abstract: Will increment / decrement based on the switch    //
8   //            uphdnl.                                           //
9   //  Created by       <Alina Suon> on <09-18-18>.                //
10  //  Copyright © 2018 <Alina Suon>. All rights reserved.         //
11  //                                                              //
    //                                                                  //
12  //  In submitting this file for class work at CSULB             //
13  //  I am confirming that this is my work and the work           //
14  //  of no one else. In submitting this code I acknowledge that  //
15  //  plagiarism in student project work is subject to dismissal.  //
16  //  from the class                                              //
17  //////////////////////////////////////////////////////////////////
18  module counter(clk, rst, incr, uphdnl, q);
19     input         clk, rst;
20     input         uphdnl, incr;
21     output [15:0] q;
22     reg    [15:0] q;
23
24     always @(posedge clk, posedge rst)
25        if (rst) q <= 8'b0;
26        else if (incr) q <= (uphdnl)? q + 16'b1 : q - 16'b1;
27  endmodule
28
```