```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////
3   //  Class: CECS 361                                             //
4   //  Project: Project1-Cecs361                                   //
5   //                                                              //
6   //  File name: <topLevel.v>                                     //
7   //  Abstract: The top level module purpose is to instantiate all  //
8   //            the modules.                                      //
9   //  Created by       <Alina Suon> on <09-18-18>.                //
10  //  Copyright © 2018 <Alina Suon>. All rights reserved.         //
11  //
    //                                                                    //
12  //  In submitting this file for class work at CSULB             //
13  //  I am confirming that this is my work and the work           //
14  //  of no one else. In submitting this code I acknowledge that    //
15  //  plagiarism in student project work is subject to dismissal.   //
16  //  from the class                                              //
17  //////////////////////////////////////////////////////////////////
18  module topLevel(clk, rst, inc, uphdnl, anode, a, b, c, d, e, f, g);
19      input         clk, rst, inc, uphdnl;
20      output [7:0]  anode;               //8 bit anode
21      output        a, b, c, d, e, f, g;
22      wire   [31:0] q;                   //32 bit q
23      wire          PED;
24      wire          rst_o;
25      wire          deb;
26
27  //Instantiate modules
28      debounce
29        debounce (clk, rst_o, inc, deb);
30      aiso
31        aiso     (clk, rst, rst_o);
32      PED
33        ped      (clk, rst_o, deb, PED);
34      counter
35        counter  (clk, rst_o, PED, uphdnl, q);
36      displayController
37        dc       (clk, rst_o, anode, q, a, b ,c ,d ,e, f,g);
38  endmodule
39
```