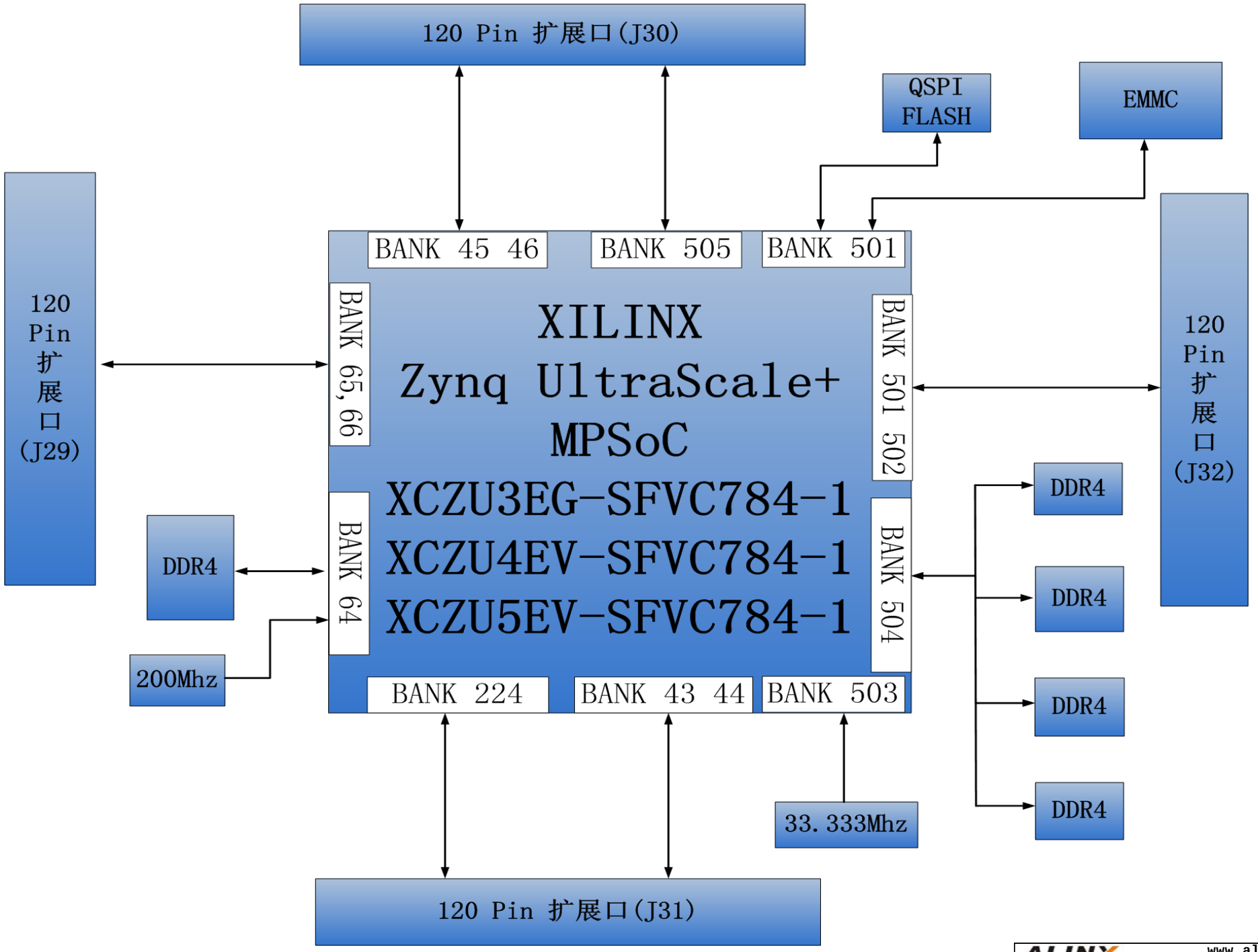

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Title: PAGE01 Block diagram		
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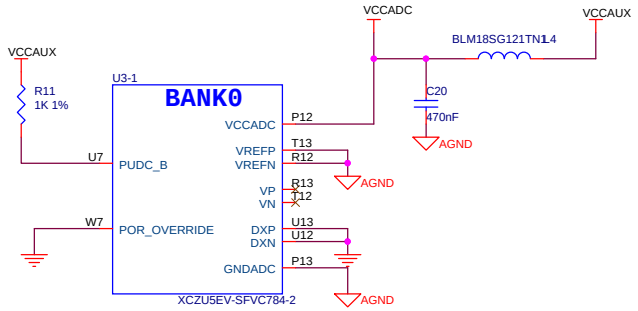
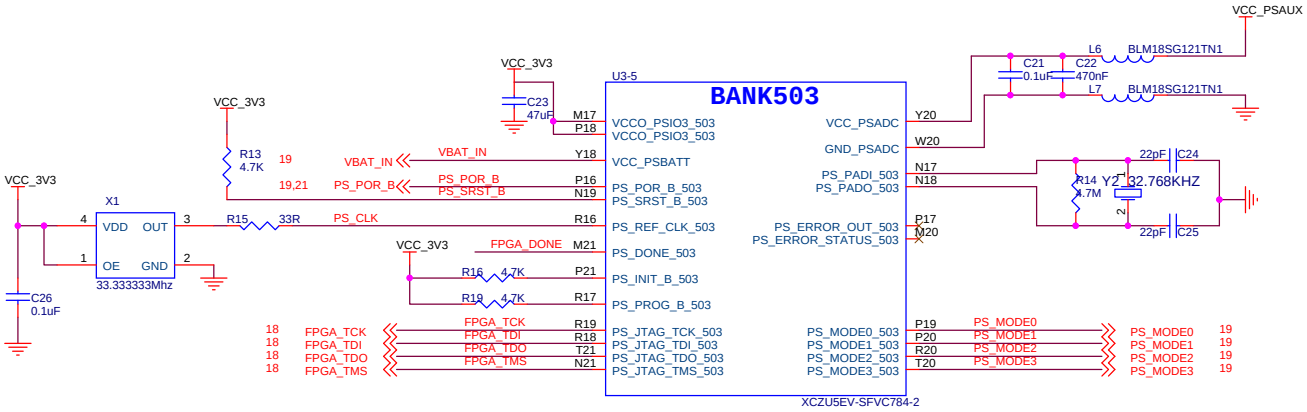
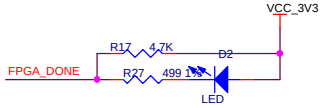
MODE[3:0]	BOOT MODE	Descritpion
0000	PS JTAG	PS JTAG Interface
0001	Quad_SPI(24b)	24-Bit addresssing(QSPI24)
0010	Quad_SPI(32b)	32-Bit addresssing(QSPI32)
0011	SD0(2.0)	SD2.0
0100	NAND	Requires 8-bit data bus width
0101	SD1(2.0)	SD2.0
0110	eMMC(1.8V)	eMMC version 4.5 at 1.8V
0111	USB0(2.0)	USB 2.0 only
1000	PJTAG(MIO #0)	PJTAG connection 0 option
1001	PJTAG(MIO #1)	PJTAG connection 1 option
1110	SD1 LS(3.0)	SD 3.0





FPGA DONE LED



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Title: Page02 Z7 Bank0 & BANK503

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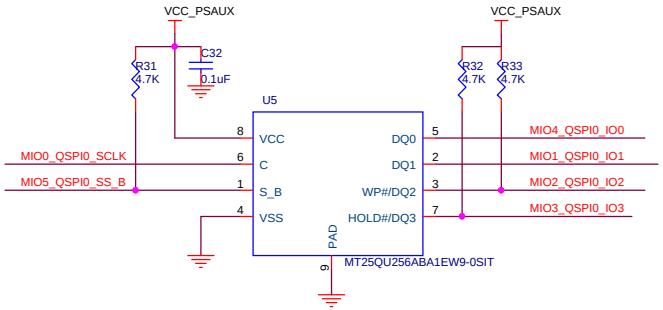

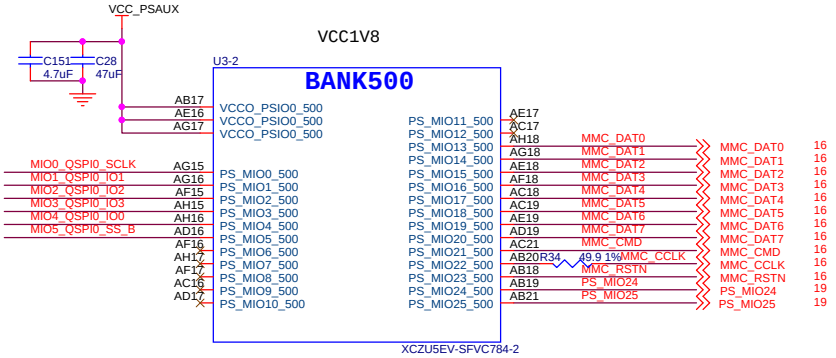

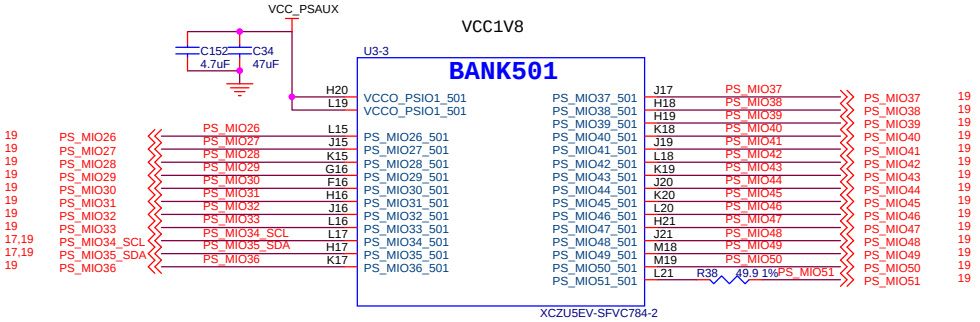

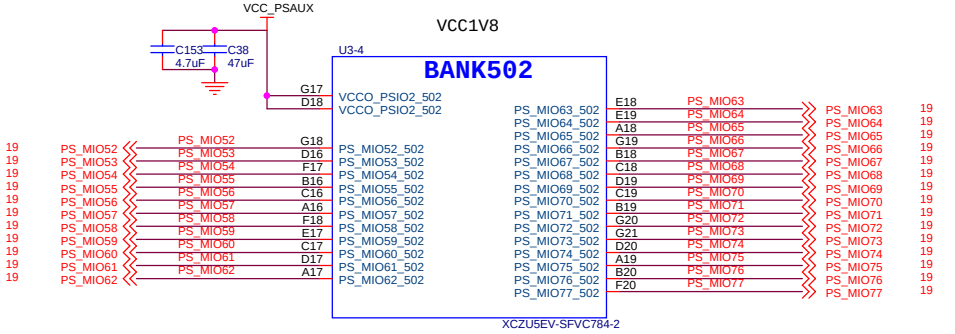

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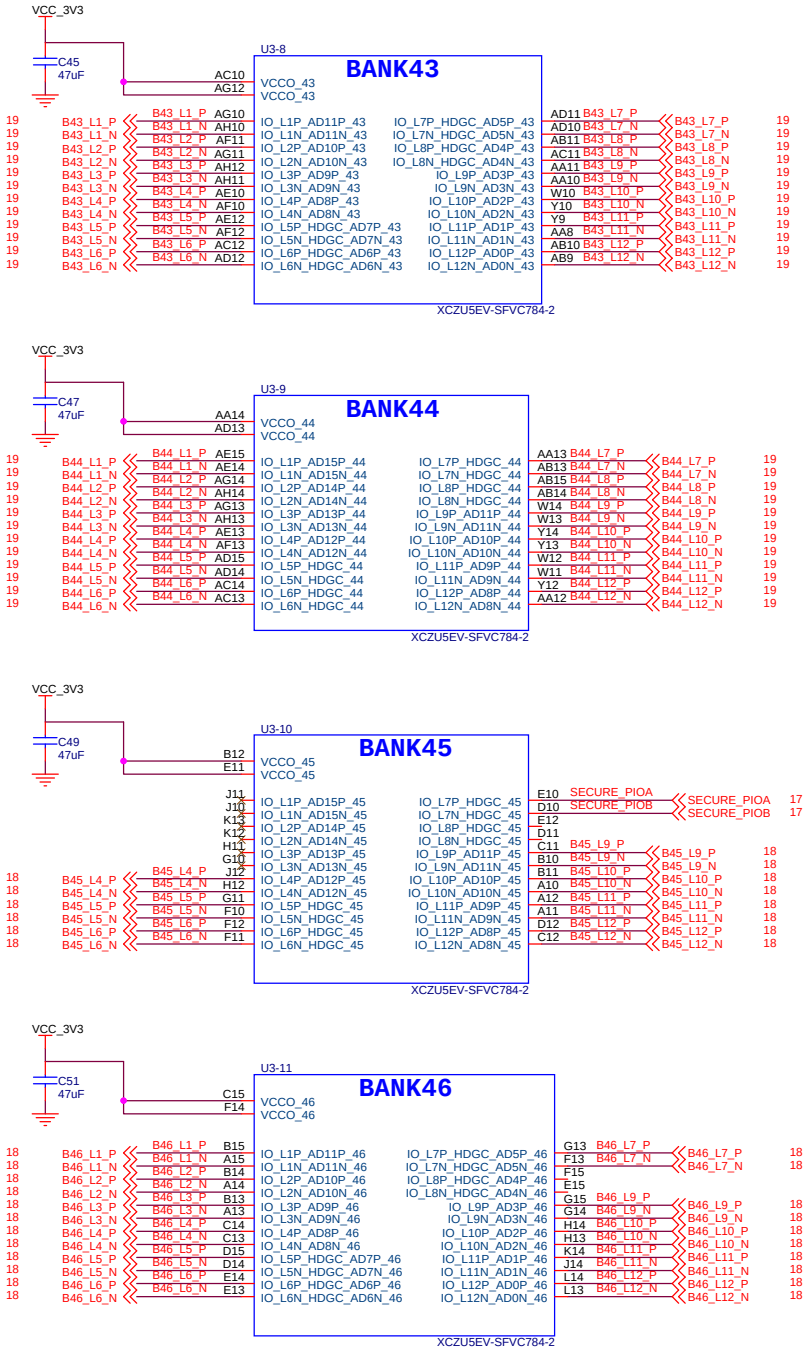

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Title: PAGE04 Z7 Bank43_44_45_46

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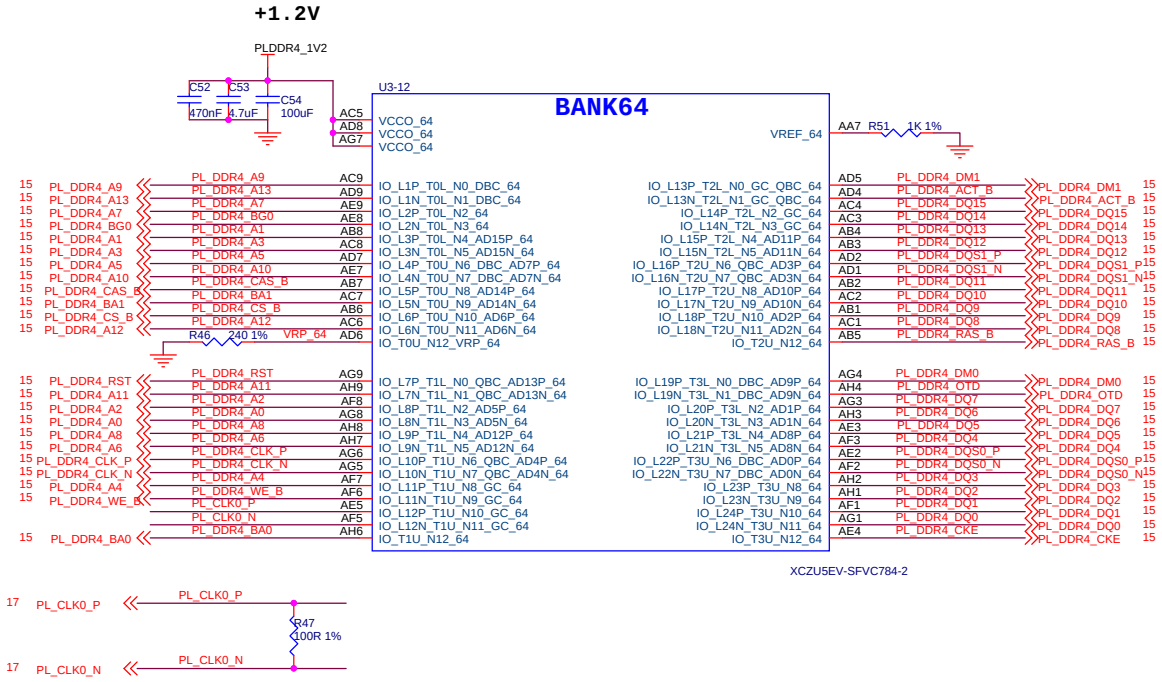

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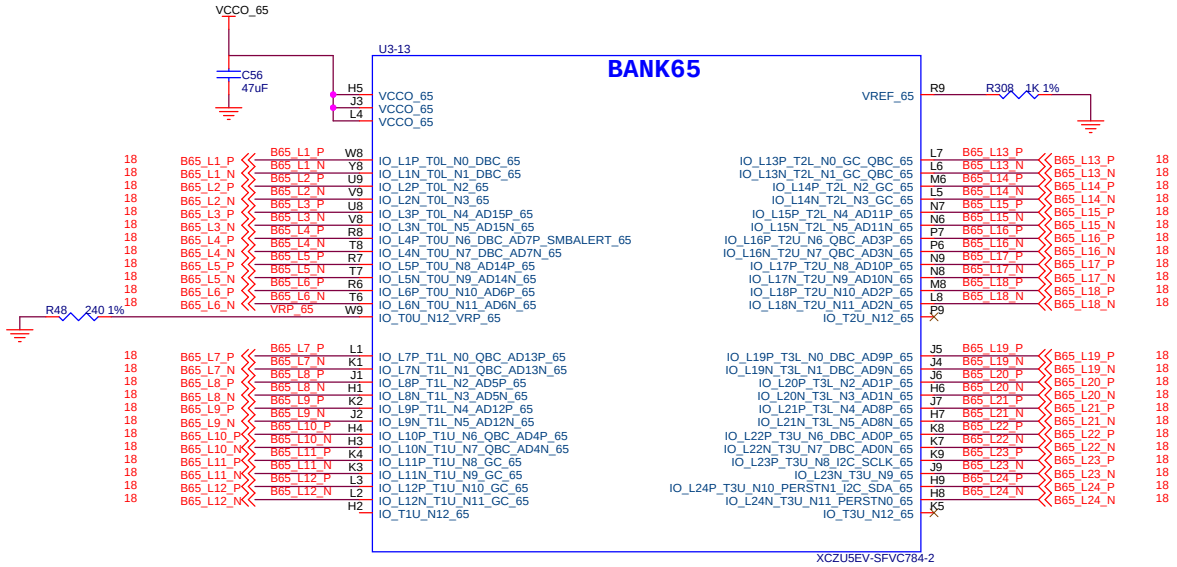

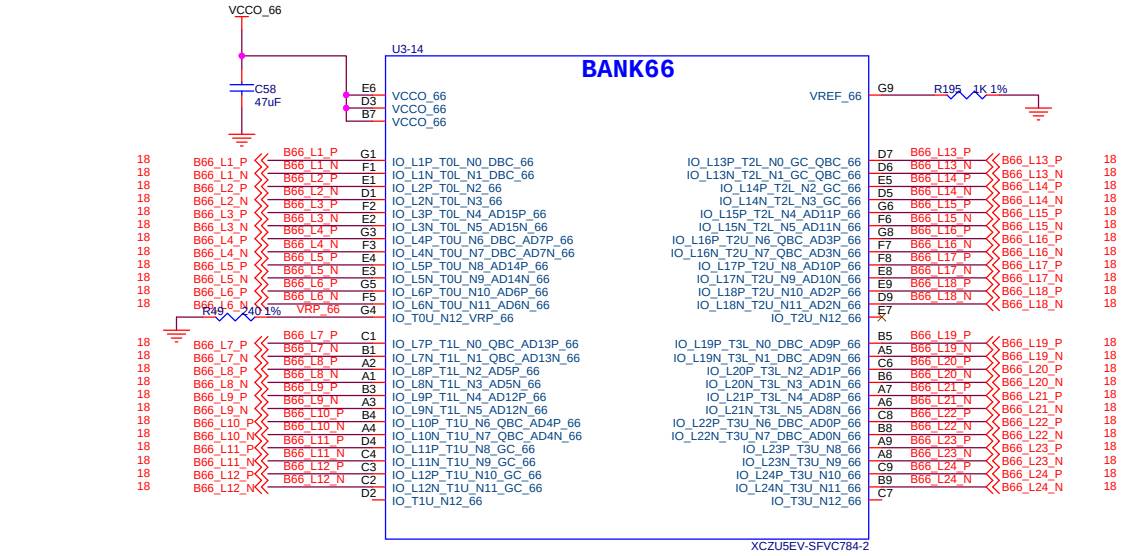

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Title	PAGE06 Z7 Bank65_66
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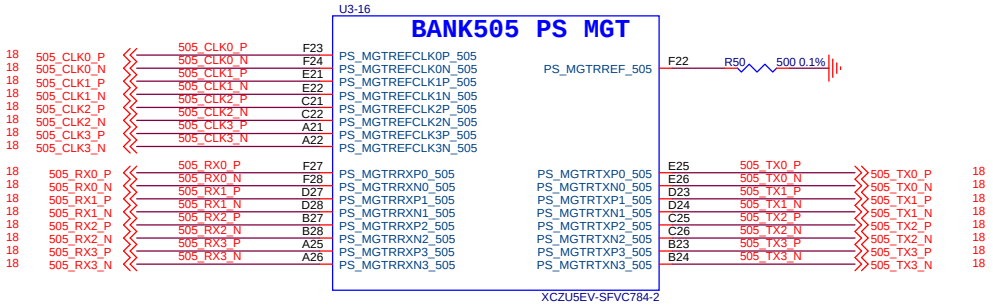

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Title: PAGE07 Z7 Bank505

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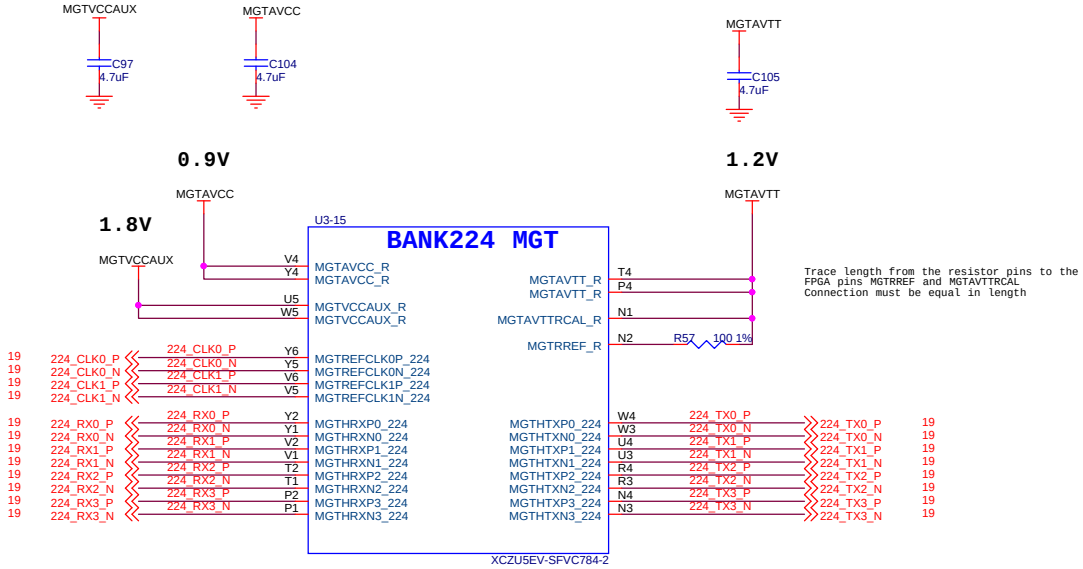

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ALINX	www.alinx.com
Title	PAGE08 Z7 Bank224
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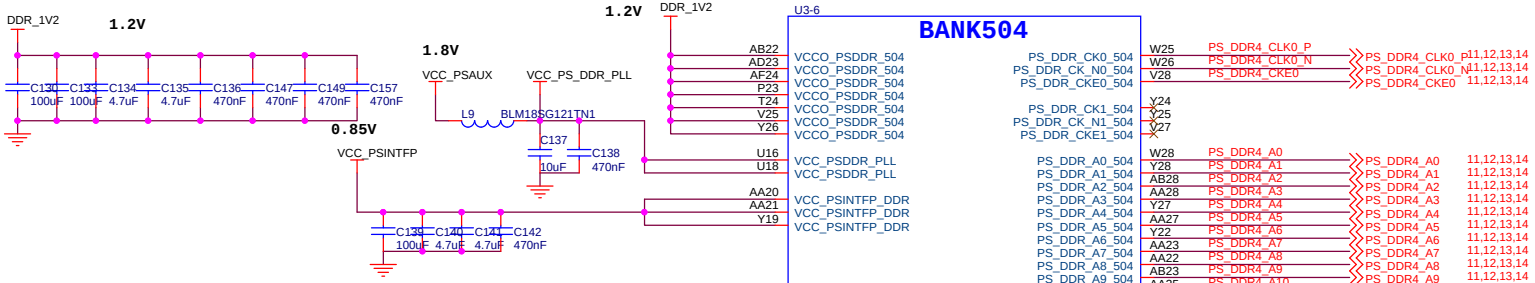

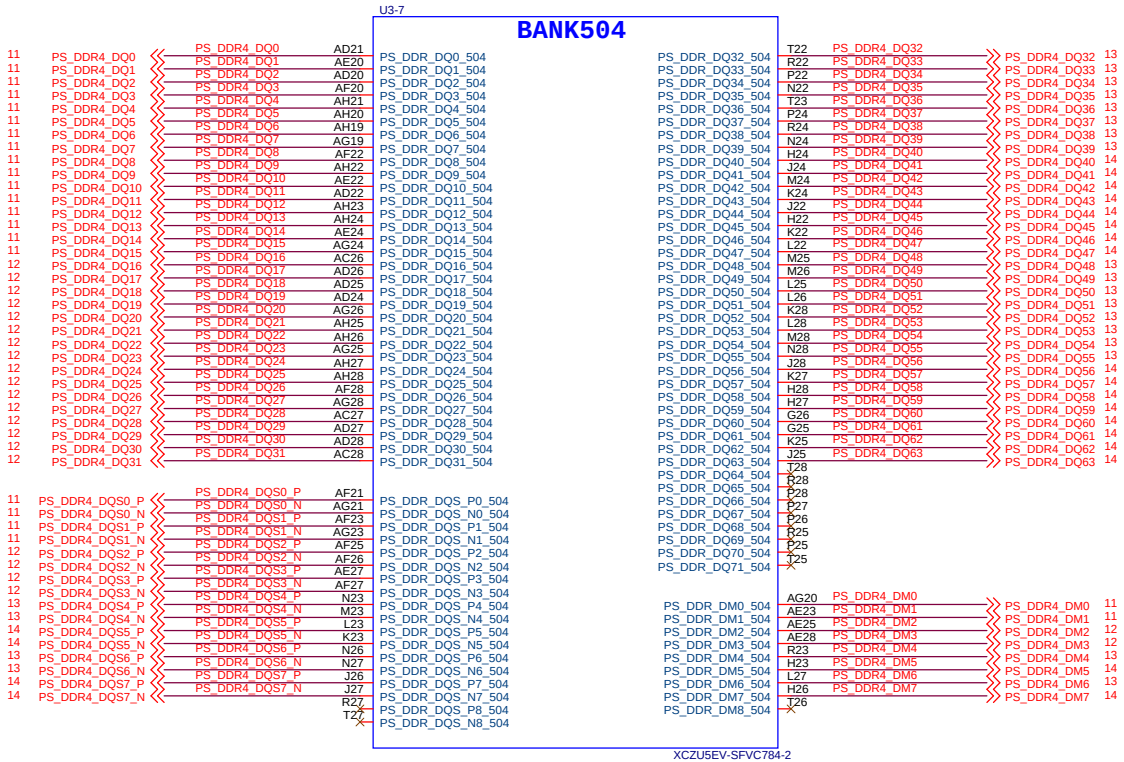

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Title: PAGE09 Z7 Bank504

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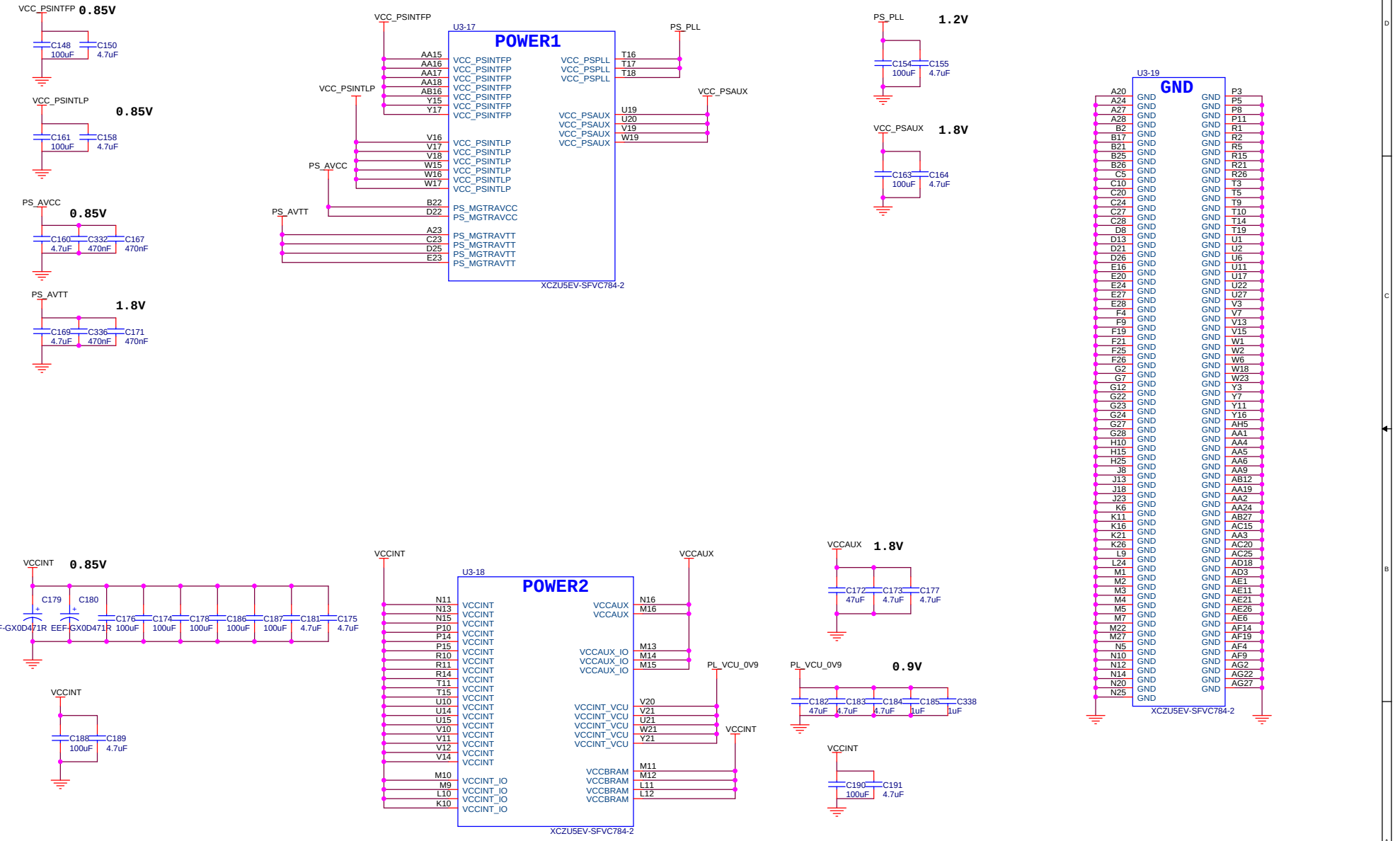

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Title	PAGE10 Z7 Power
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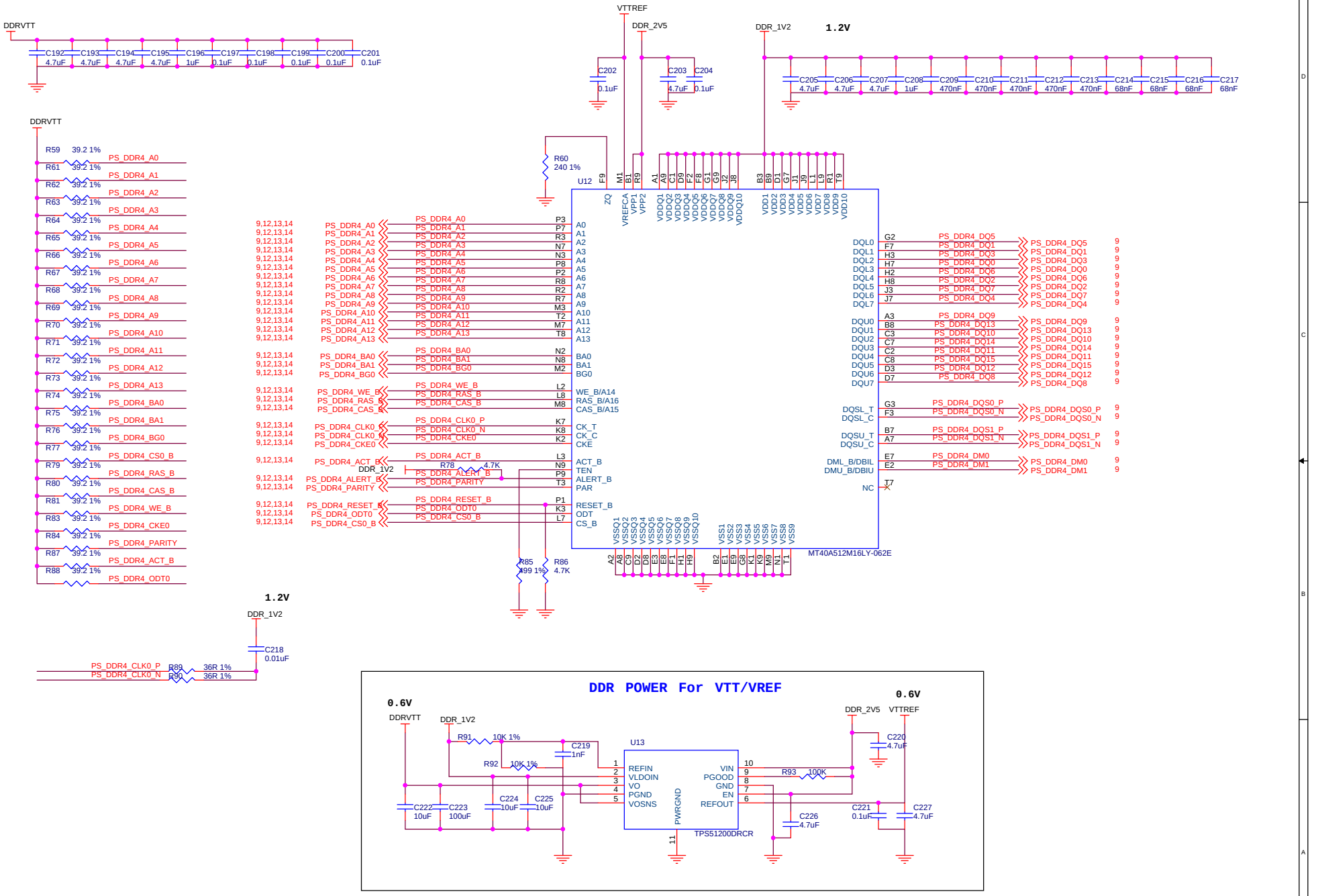

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Title	PAGE11 PS_DDR4_1
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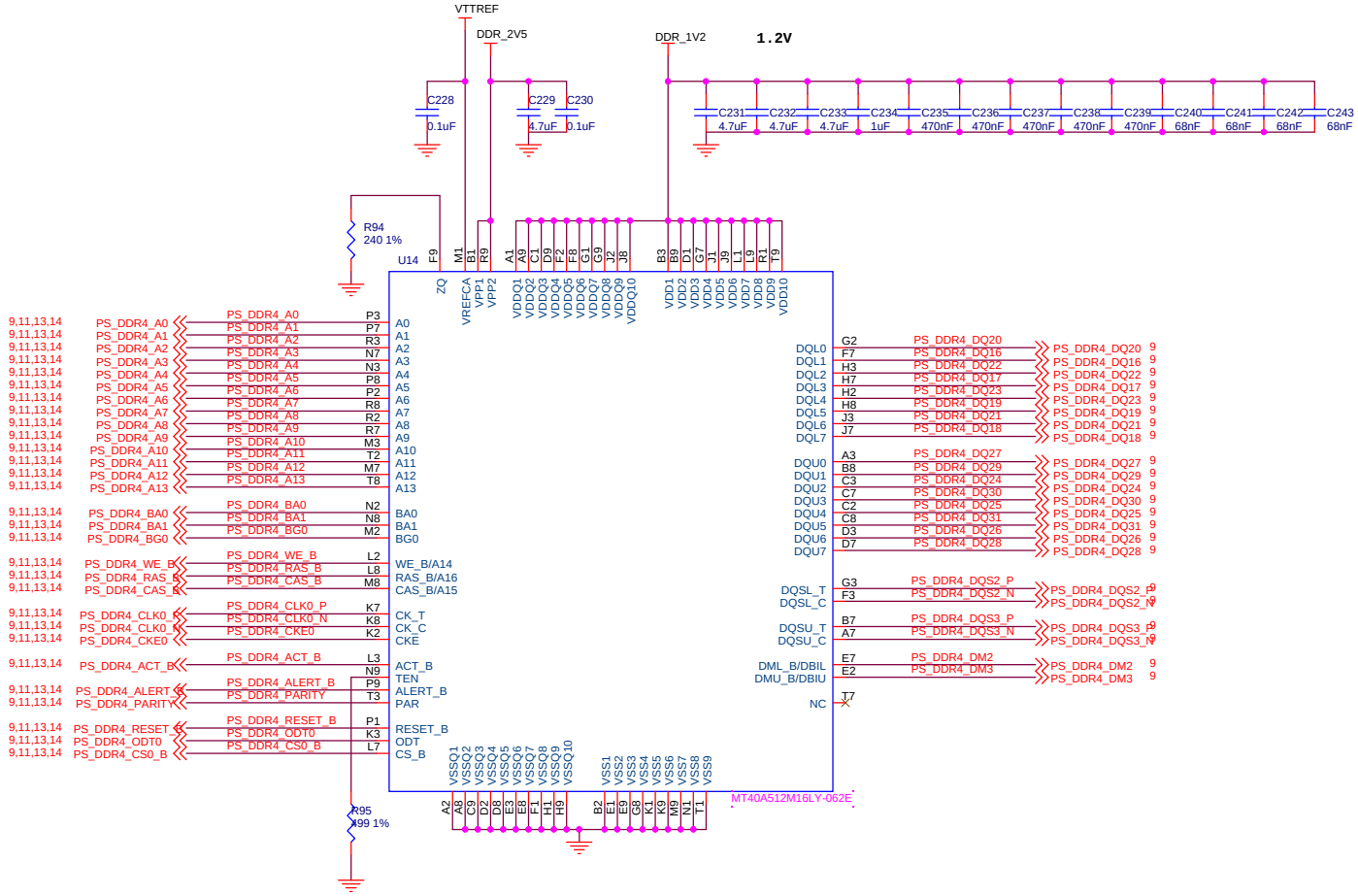

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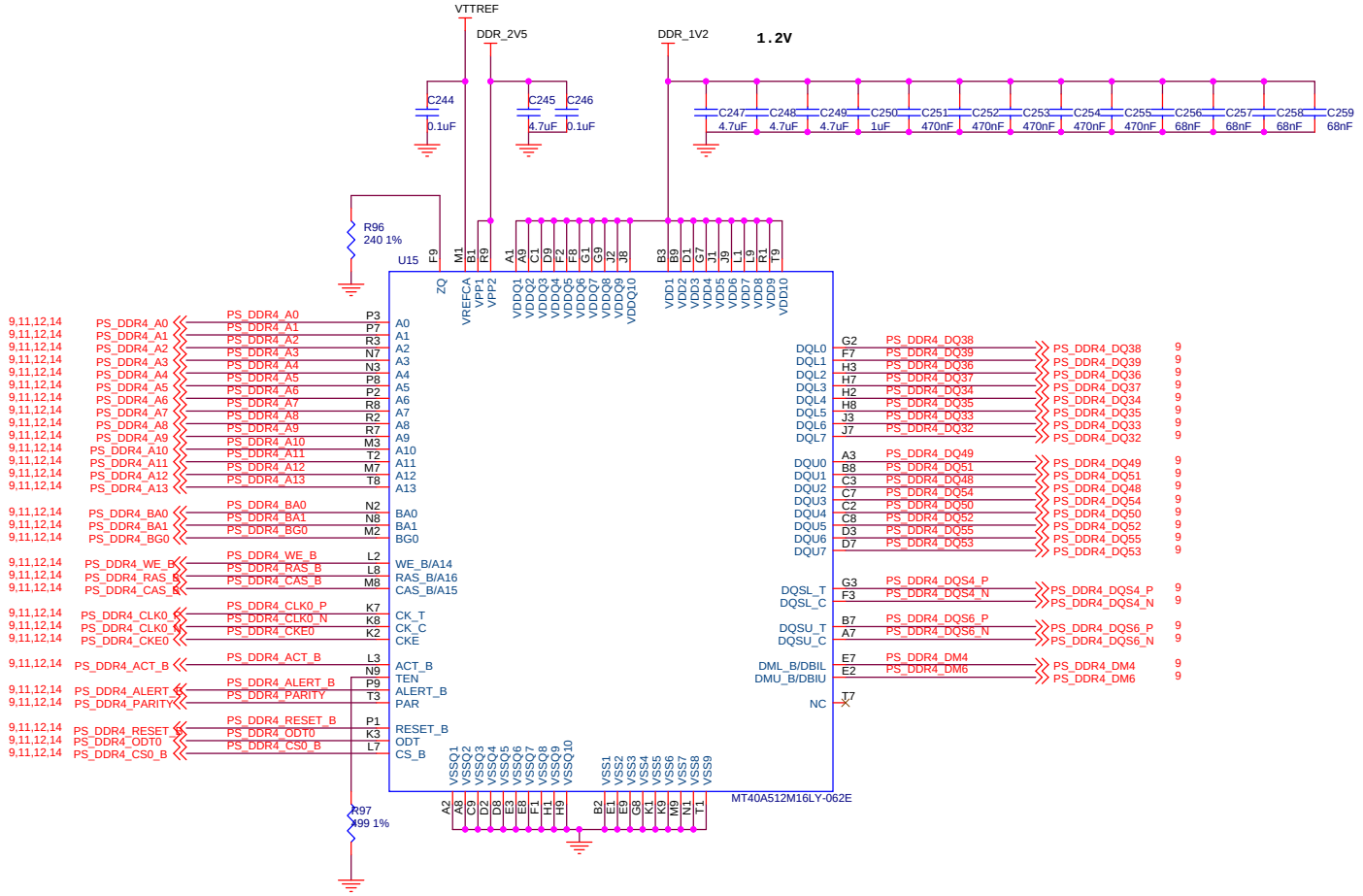

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Title: PAGE13 PS_DDR4_3

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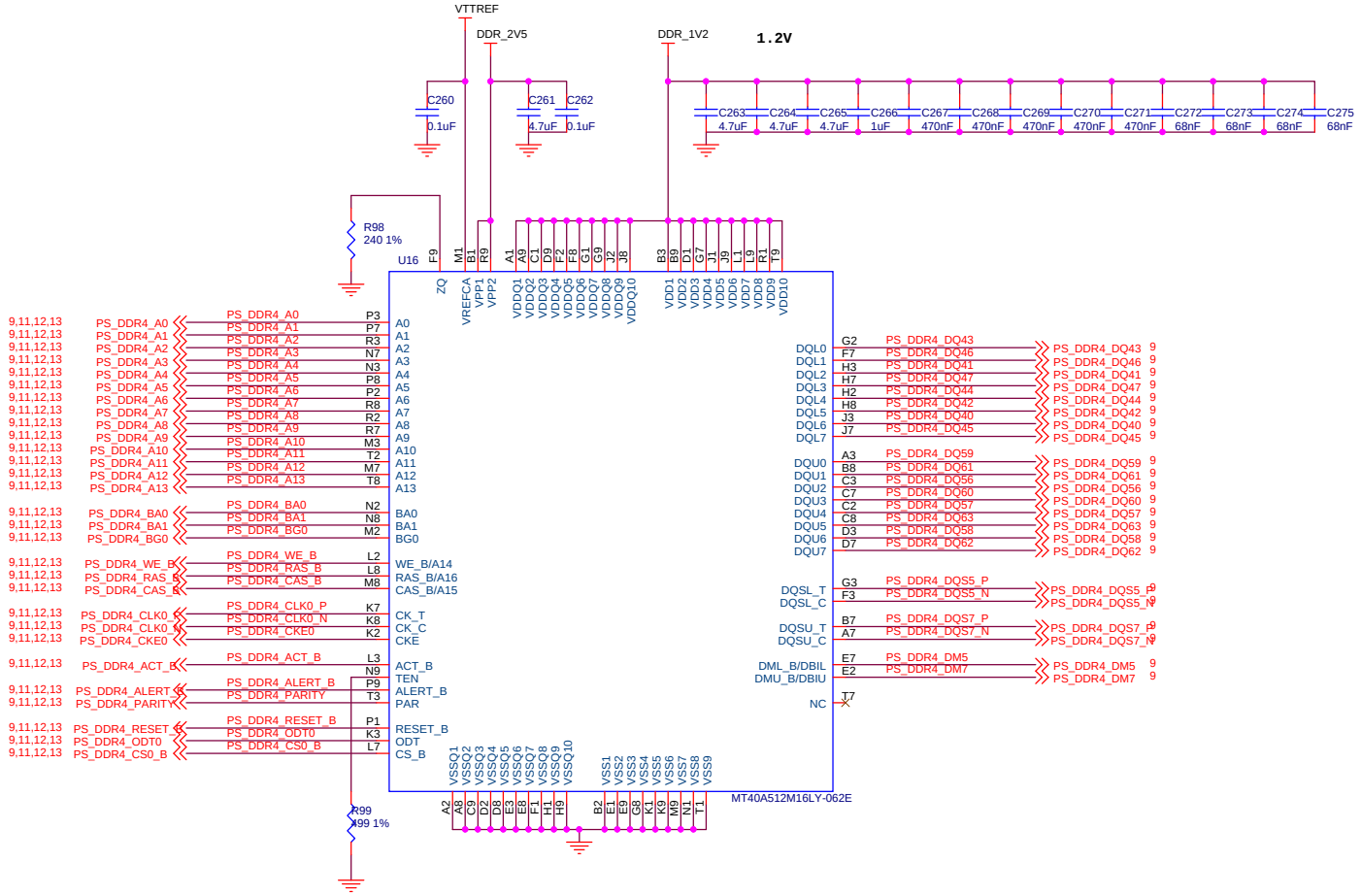

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Title	PAGE14 PS_DDR4_4	
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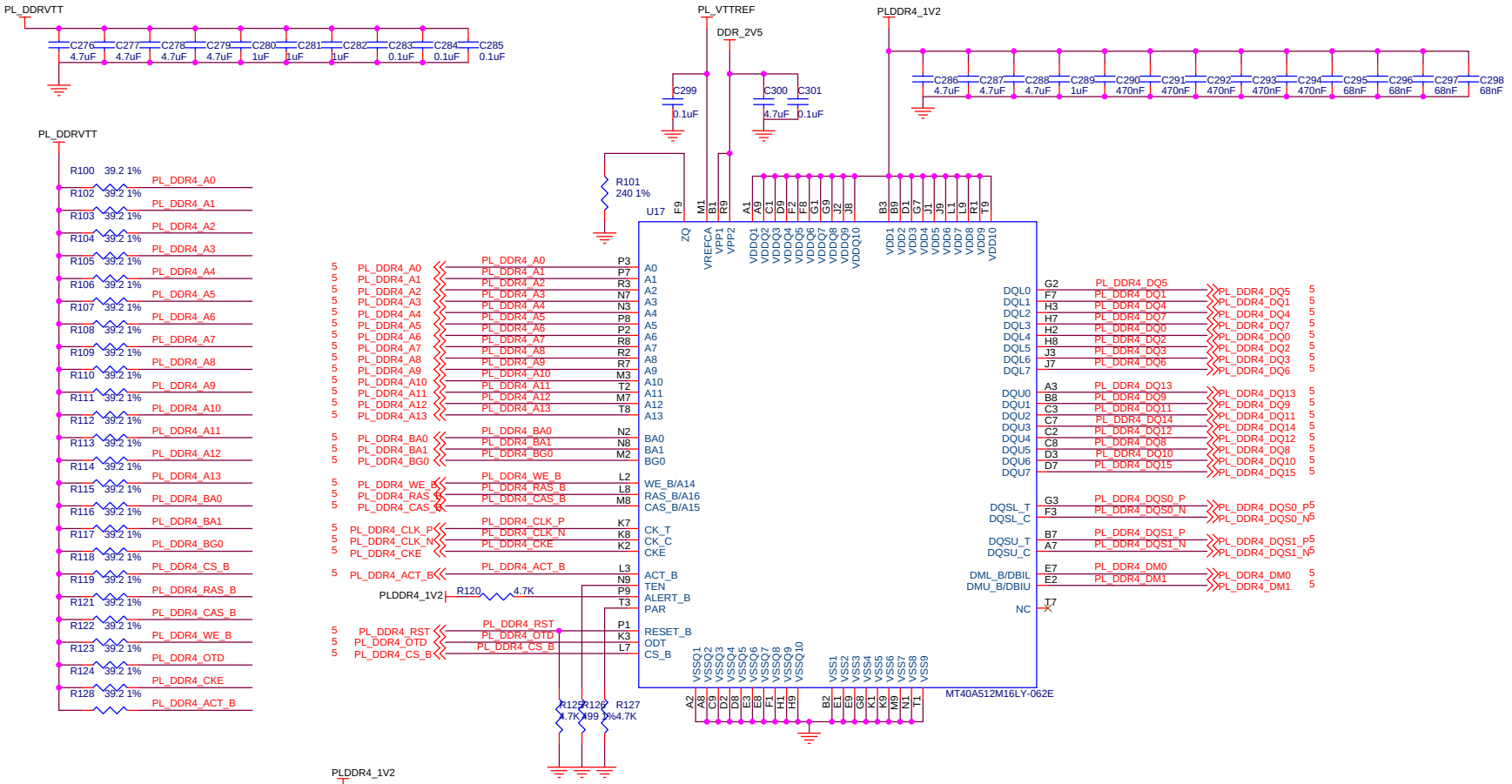

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Title	PAGE15 PL_DDR4
Size	Document Number: ACU5EV核心板 Schematics
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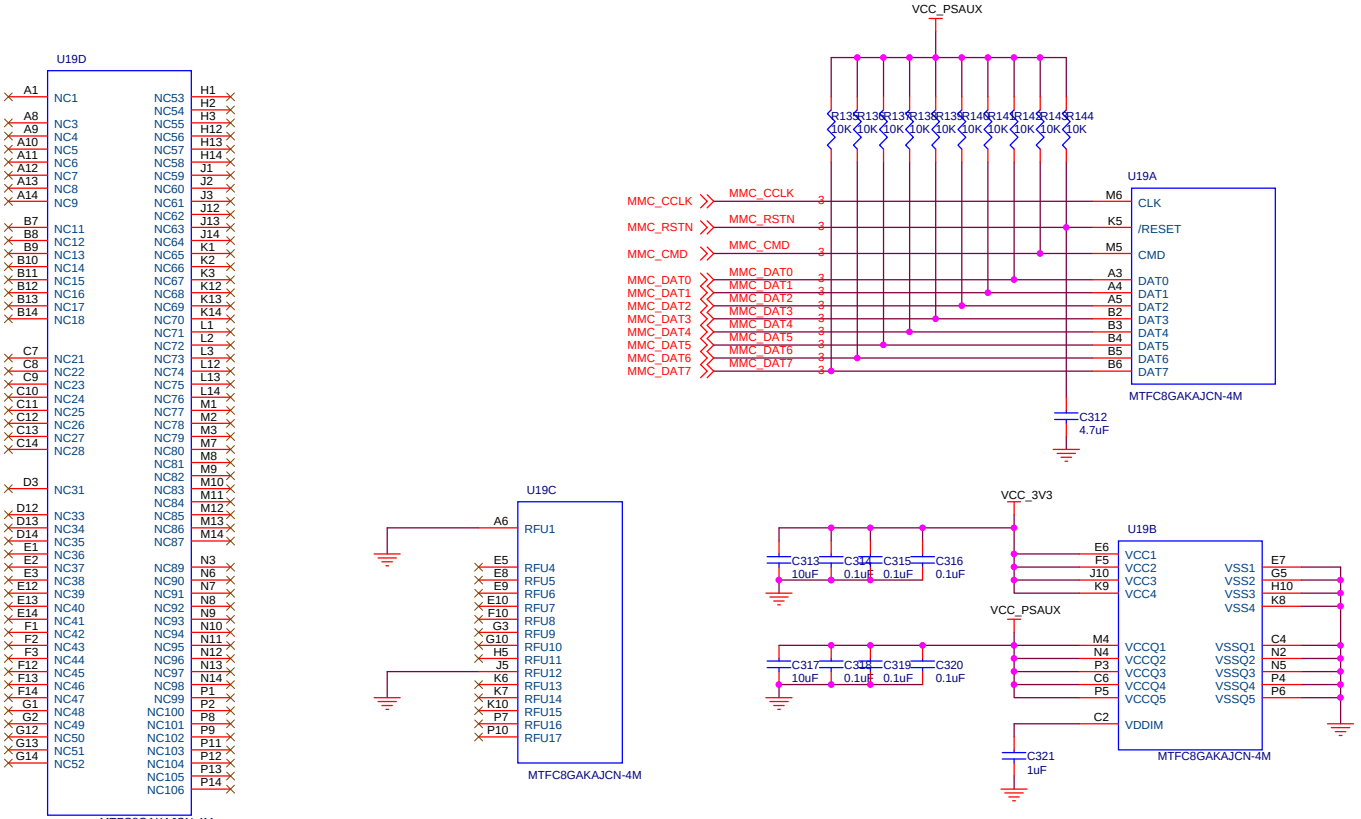

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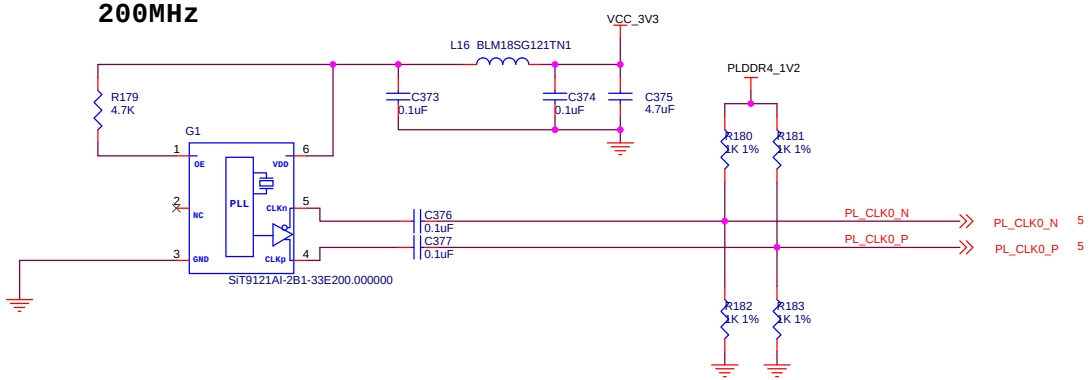
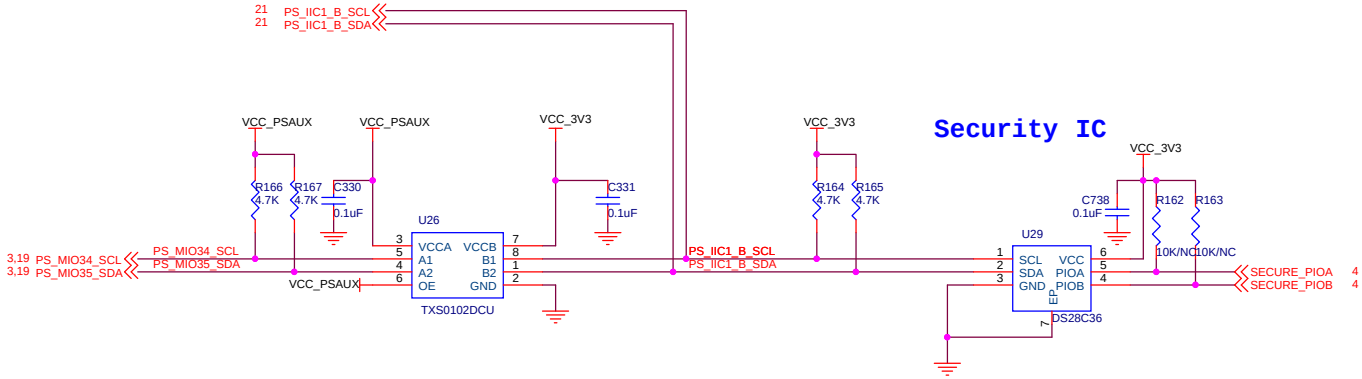
PL SYSTEM CLOCK

200MHz





PS_IIC1: IIC ADDRESS IS 0x1B

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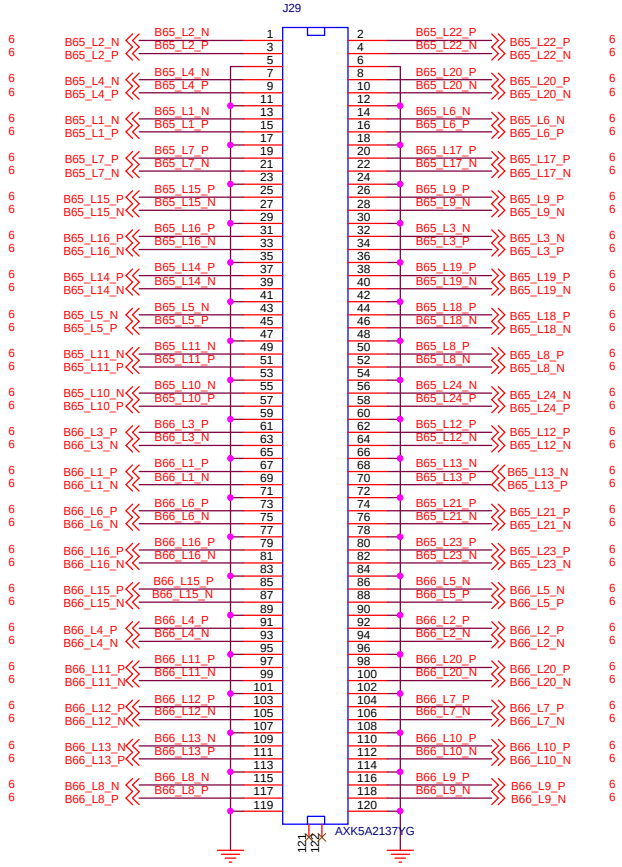
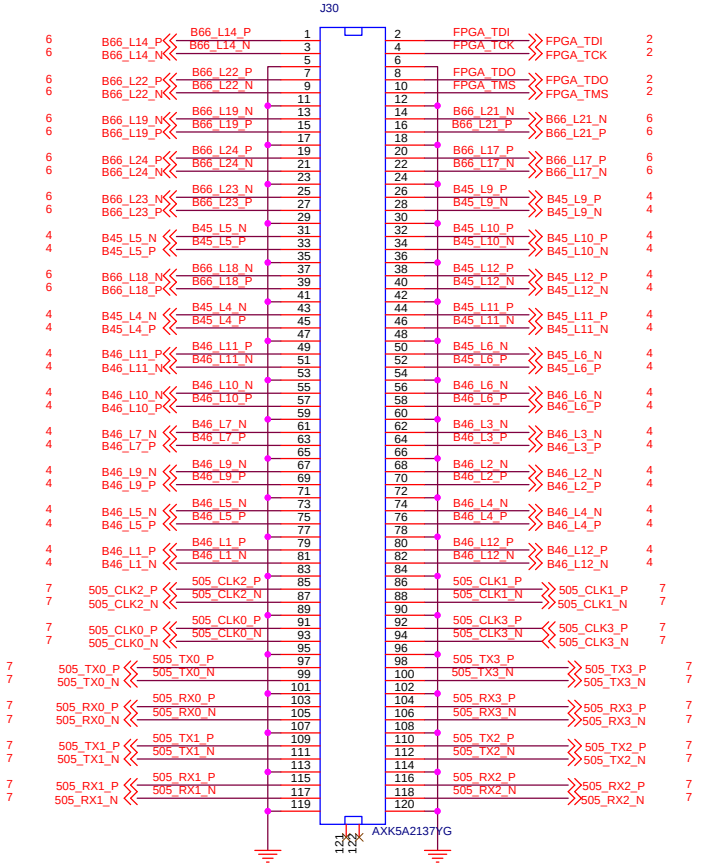
BANK65, BANK66 IO Voltage can not exceed +1.8V



BANK45, BANK46 IO Voltage is +3.3V Standard



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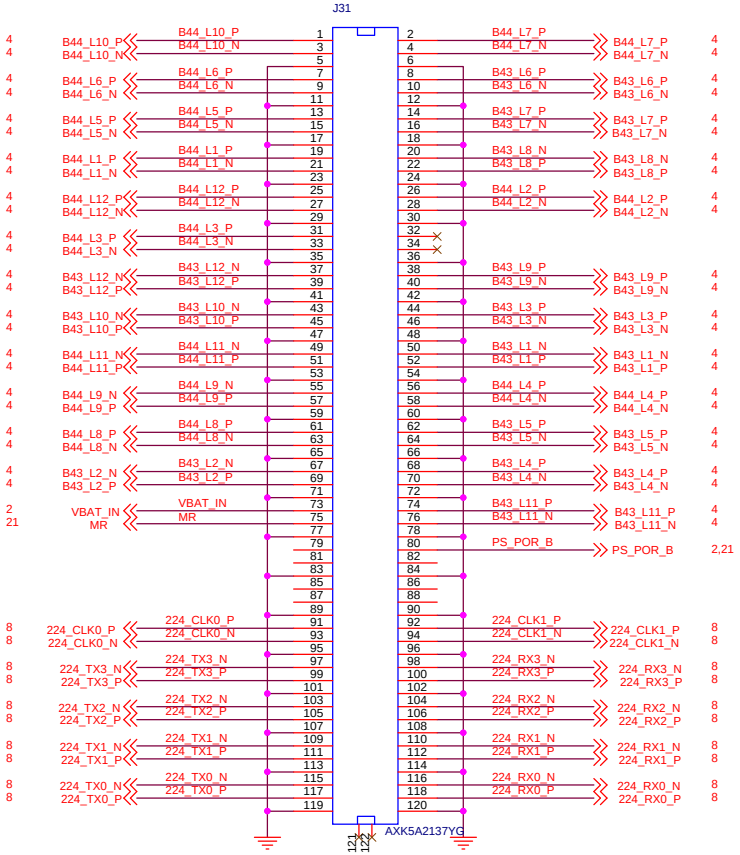
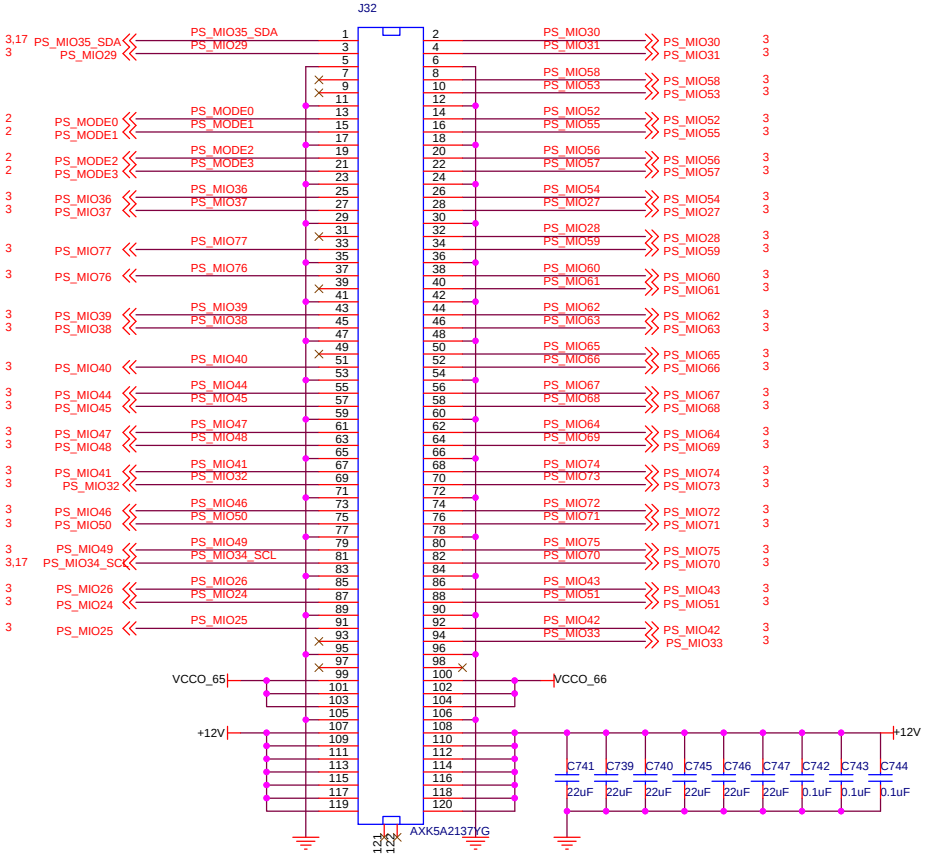
BANK43, BANK44 IO Voltage is +3.3V Standard



The MIO Voltage is +1.8V Standard



VCCO_65 VCCO_66 Power supply can not exceed 1.8V

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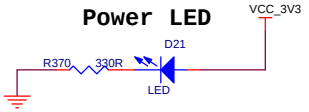
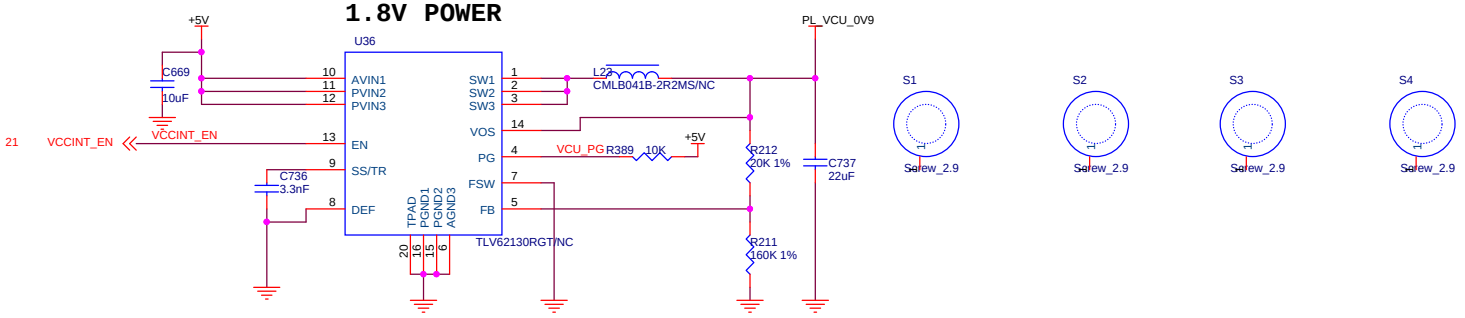
POWER ON: VCCINT/VCCINT_IO/VCCBRAM(+0.85V)->VCCINT_VCU(+0.9V)->VCCAUX/VCCAUX_IO(+1.8V)->VCCO(+3.3V, +1.8V)

POWER ON: VCCINT(+0.85V)->MGTAVCC(+09V)->MGTAVTT(+1.2V)

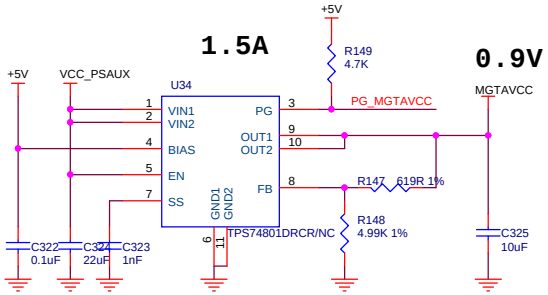
Power LED



1.8V POWER



1.5A



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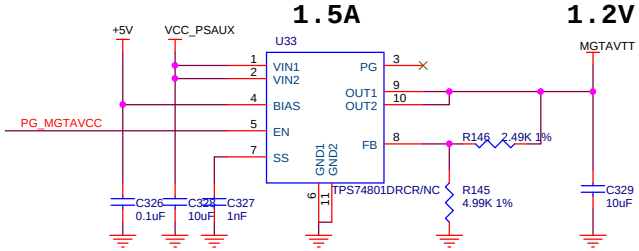
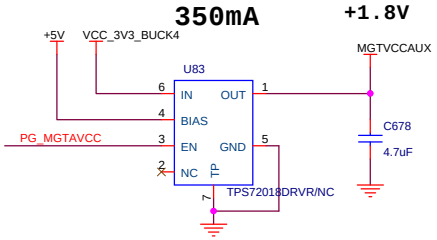


350mA



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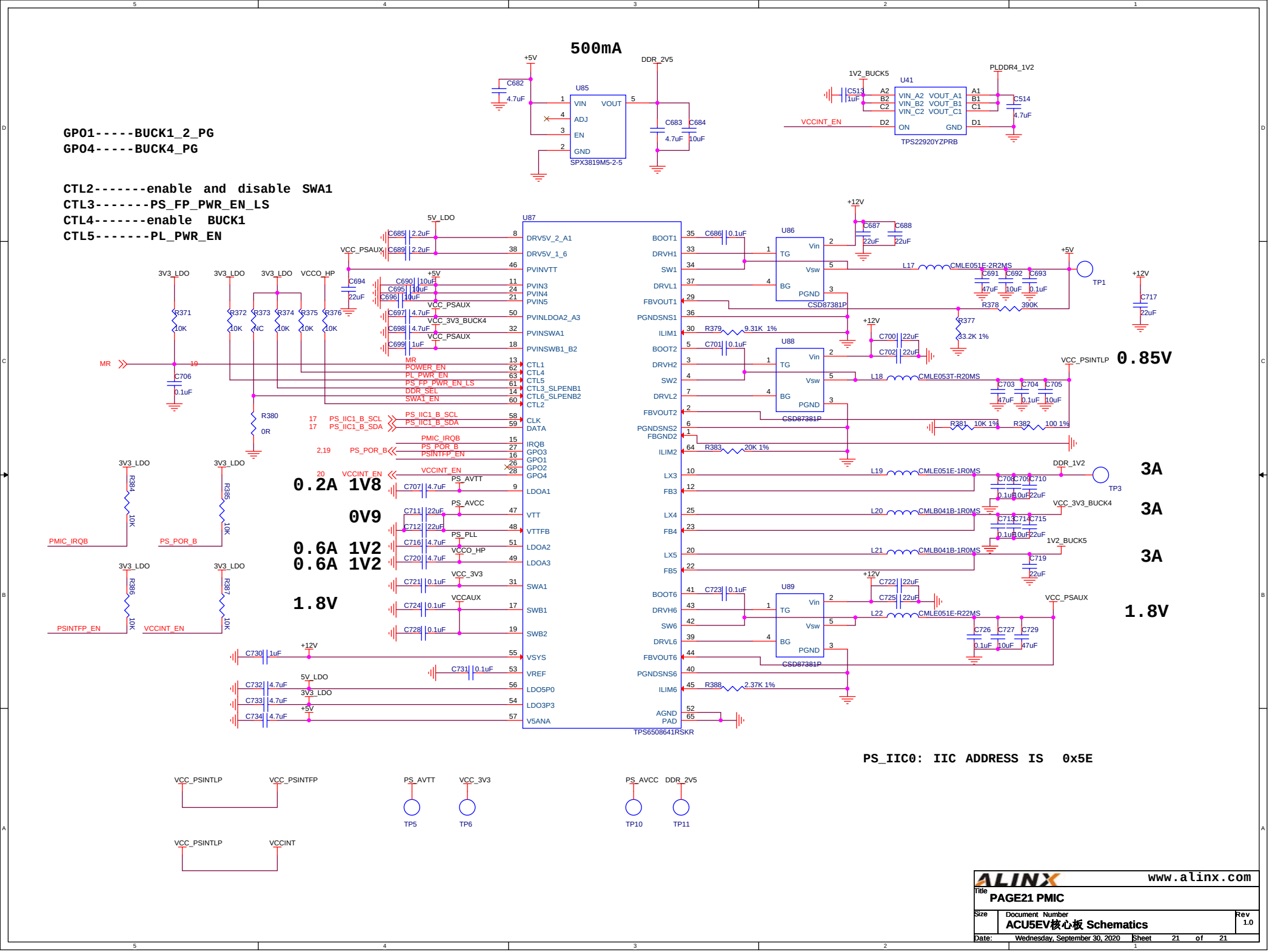
500mA
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GPO4-----BUCK4_PG
CTL2-------enable and disable SWA1
CTL3-------PS_FP_PWR_EN_LS
CTL4-------enable BUCK1
CTL5-------PL_PWR_EN
U85
SPX3819M5-2-5
U41
TPS22920YZPRB
U87
TPS6508641RSKR
U86
U88
U89
CSD87381P
0.85V
0.2A 1V8
0V9
0.6A 1V2
0.6A 1V2
1.8V
3A
3A
3A
1.8V
PS_IIC0: IIC ADDRESS IS 0x5E
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