Silicon Image™

SiI9013 HDMI Receiver

Programmer's Reference

Document # SiI-PR-1012-A01

October 2010

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Revision History

Revision	Date	Comment
0.90	11/06	Preliminary Release
A	05/07	Production Release
A01	10/2010	Inserted Export Control paragraph, patent information, updated entire layout to current Techpubs template.

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Purpose of This Document

This Programmer's Reference provides internal information on the SiI9013 HDMI receiver so that system designers and programmers can implement the firmware and software necessary to control all of the device's features in a system environment.

Detailed application information on how to use the registers and features of the SiI9013 HDMI receiver is available in the *SiI9011/9021/9031 HDMI PanelLink Receivers Application Note* (SiI-AN-0118).

Register Map

Registers not specifically listed in the following sections are reserved for Silicon Image use and should not be written. Values read from such addresses are not guaranteed. Register bits marked as RESERVED or RSVD should be written as zeros and are read as zeros unless otherwise noted.

The registers are described in groups according to their function. The registers are accessible through one of two I^{2}C ports on the SiI9013 HDMI receiver: a DDC bus connected to the Source and the local I^{2}C controller bus within the Sink (see Table 1).

Table 1. Register Address Groups

Address Range	Group Name	I^{2}C Device	I^{2}C Port Access		Purpose	Page
			DDC	Local		
0x00–0xFF	HDCP	0x74	X		HDCP operation	3
0x00–0x09	ID	0x60		X	Device ID and Initialization	8
0x1A–0x39	HDCP	0x60		X	HDCP Status	13
0x3A–0x6F	Video	0x60		X	Video Detection and Programming	18
0x70–0x7F	Interrupt	0x60		X	Interrupt Processing	25
0x80–0x87	TMDS	0x60		X	TMDS equalization and control	32
0x88–0x94	Audio In	0x60		X	Audio Clock Recovery Configuration	34
0xB5–0xBA	AEC	0x60		X	Auto Exception Control	33
0xBB–0xCE	ECC	0x60		X	ECC Processing	35
0xD4–0xF2	HDCP	0x60		X	HDCP Repeater Support	37
0x00–0x25	ACR	0x68		X	Audio Clock Generation	39
0x26–0x39	Audio Out	0x68		X	Audio Output Formatting	45
0x3C–0x3F	Power	0x68		X	Power Down Control	53
0x40–0xFF	Packets	0x68		X	Packet Contents and Control	55

The first section in this document defines the registers accessible only from the Source across the DDC bus. The second section defines the registers accessible only from the local I^{2}C bus in the Sink.

Note: The HDMI receiver is accessed through a pair of local I^{2}C device addresses according to the state of the CI2CA pin (see Table 2).

Table 2. Control of Local I^{2}C Address with CI2CA Pin

	CI2CA = LOW	CI2CA = HIGH
First Device Addr	0x60	0x62
Second Device Addr	0x68	0x6A

This document refers to registers using the device addresses 0x60 and 0x68. All such references are equivalent to using the device addresses 0x62 and 0x6A.

Unless otherwise noted, statements in this document apply to the SiI9013 HDMI receiver used in either an HDMI Sink or HDMI Repeater configuration.

Register addresses that are not described in this document should not be written using I^2C. Modifications to undocumented registers may cause unintended errors in the chip function.

Usages and Conventions

Table 3 provides information on the conventions used in this document.

Table 3. Usage and Conventions

Convention	Usage
Bit N	Bits are numbered in little-endian format. The LSB of a byte or word is referred to as bit 0.
0xNN	Hex representation of base-16 numbers are represented using C language notation, preceded by 0x.
0bNN	Binary (base-2) numbers are represented using C language notation, preceded by 0b.
NN	Decimal (base-10) numbers are represented using no additional prefixes or suffixes.
	Reserved register bits are shaded in the register description.
RSVD0	A bit in a register that is reserved and read-only, and returns a zero value.
RSVD1	A bit in a register that is reserved and read-only, and returns a one value.
RSVDRW	A bit in a register that is reserved and read-write, returning the value written to it.
RSVDRW0	A bit in a register that is reserved and read-write, and should always be written to zero.
RSVDRW1	A bit in a register that is reserved and read-write, and should always be written to one.
X	A register bit defaulting to X has no defined state after hardware reset.

DDC-Accessible Registers

The Source (for example, a DVD player or a set-top box) is the only controller that accesses the DDC-accessible registers; these registers are defined in the HDCP Specification. No firmware in the Sink is used to interact with these registers. For Sink-side control, see the descriptions beginning on page 8.

A Source can read all of the registers on the DDC bus at device address 0x74 if power is applied to the pins of the HDMI receiver. The following do not affect the ability to read registers on DDC (although some register values may be affected):

- State of the PD# bit or other power control bits (described on page 11 and 53)
- State of the RX_EN bit (TMDS Port Enable, described on page 12)
- State of the reset bits (described on page 9)

All registers can be read locally by the Sink's firmware whether PD#=0 or PD#=1. The values of other registers are not affected by assertion of PD# or the other power down bits (see page 53).

Device Identification Registers

DEVICE Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x74	0xFB	DEVICE			DEV_ID				DEV_REV	
Bit	**Label**	**R/W**	**Description**						**Default**	
7:3	DEV_ID	R	Device ID.						0b00110	
2:0	DEV_REV	R	Device Revision.						0b000	

HDCP Registers

HDCP BKSV Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x74	0x00	BKSV1				BKSV1				
0x74	0x01	BKSV2				BKSV2				
0x74	0x02	BKSV3				BKSV3				
0x74	0x03	BKSV4				BKSV4				
0x74	0x04	BKSV5				BKSV5				
Bit	**Label**	**R/W**	**Description**							**Default**
39:0	BKSV	R	HDCP-capable receiver's Key Selection Vector (KSV). **Note:** An HDCP reset causes the HDCP keys to load every time SCDT transitions from 0 to 1. Refer to register 0x60:0x05 on page 9.							

The BKSV register can also be read from the Sink-side in a BKSV Shadow register (see page 13).

Note: HDCP initialization requires an active video stream into the SiI9013 HDMI receiver. The Source must not read the HDCP BKSV value until it has been transmitting stable video to the HDMI receiver for a time period of at least $T_{BKSVINIT}$.

HDCP R$_i$ Register

The R$_i$ value is updated every 128 frames when HDCP decryption is enabled and running. It is recommended that the Source protect itself against errors in DDC/I^{2}C transmission by re-reading this register. The value in the R$_i$ register is always available. The initial value, R$_0$′, is to be available a maximum of 100 ms after the last byte of the Source's AKSV is written into the SiI9013 HDMI receiver (the actual calculation time depends on the frequency of the incoming TMDS clock). Subsequent values of R$_i$′ are available a maximum of 128 pixel clocks after the HDMI receiver detects the assertion of the decoded CTL3 signal (as defined by HDCP). Refer to the HDCP Specification for more details.

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x74	0x08	RI1				RI1				
0x74	0x09	RI2				RI2				
Bit	Label	R/W			Description					Default
15:0	RI	R	R$_i$ Register. The value of this register is read and compared in the firmware with the value of the R$_i$ register from the HDCP-capable transmitter.							0x0000

The R$_i$ register can also be read from the Sink in an R$_i$ Shadow register (see page 13).

HDCP AKSV Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x74	0x10	AKSV1				AKSV1				
0x74	0x11	AKSV2				AKSV2				
0x74	0x12	AKSV3				AKSV3				
0x74	0x13	AKSV4				AKSV4				
0x74	0x14	AKSV5				AKSV5				
Bit	Label	R/W			Description					Default
39:0	AKSV	W	HDCP-capable transmitter's Key Selection Vector (KSV).							

Byte AKSV1 is written first. Byte AKSV5 must be written last because it triggers the authentication logic in the SiI9013 HDMI receiver. The AKSV register can also be read from the Sink in an AKSV Shadow register (see page 13).

HDCP AN Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x74	0x18	AN1				AN1				
0x74	0x19	AN2				AN2				
0x74	0x1A	AN3				AN3				
0x74	0x1B	AN4				AN4				
0x74	0x1C	AN5				AN5				
0x74	0x1D	AN6				AN6				
0x74	0x1E	AN7				AN7				
0x74	0x1F	AN8				AN8				
Bit	Label	R/W			Description					Default
63:0	AN	W	HDCP 64-Bit Pseudo-Random Value. This multi-byte value must be written before the AKSV bytes are written to the HDMI receiver.							

The AN register can also be read from the Sink in an AN Shadow register (see page 14).

BCAPS Register

Dev	Addr	Name		7	6	5	4	3	2	1	0
0x74	0x40	BCAPS		HDMI_C	RPTR	FIFORDY	FAST	RSVD0			

Bit	Label	R/W	Description	Default
7	HDMI_C	R	HDMI capability. Always reads 1 as HDMI-capable device. 0 = Device supports DVI 1.0 but not HDMI 1 = Device supports HDMI This bit is available for diagnostic use only and should not be the indicator by the Source to determine if the Sink is used as an HDMI Sink. Consult the HDMI Specification for Vendor-Specific Data Block (VSDB) in the EDID. **Note**: This bit can be written to 0 after a hardware reset using the BCAPS_SET register (see page 14). Because this bit defaults to 1, it may be read as 1 across the DDC channel until explicitly written by the Sink's firmware.	1
6	RPTR	R	Repeater status: 0 = HDCP End Point (HDMI receiver) 1 = Device is a repeater **Note**: This bit can be written using the BCAPS_SET register (described on page 14) on the local I^2C bus. When enabled to support repeaters, the SiI9013 HDMI receiver can handle a list of up to 12 attached HDCP devices.	0
5	FIFORDY	R	KSV FIFO read status: 0 = FIFO not ready for read 1 = FIFO ready for read **Note**: This bit is set when the KSV FIFO is ready as part of the HDCP standard register set. This function is needed for HDCP repeaters so that the Source knows when to begin reading the KSV list. Refer to the HDCP Specification.	0
4	FAST	R	I^2C transfer speed capability: 0 = Supports only up to 100-kbps speed 1 = Supports 400-kbps speed **Note**: This bit must always be 0. The HDMI Specification requires the DDC bus be used at 100-kHz speed or less (standard mode I^2C).	0

The BCAPS register can also be read from the Sink in a BCAPS_SET register (0x60:0x2E) (see page 14).

BSTATUS Register

Dev	Addr	Name		7	6	5	4	3	2	1	0
0x74	0x41	BSTATUS1		DEV_EXC	DEV_COUNT						
0x74	0x42	BSTATUS2		RSVD0			HDMI_MODE	CAS_EXC	DEV_DEPTH		

Bit	Label	R/W	Description	Default
7	DEV_EXC	R	Device count exceeded.	0
6:0	DEV_COUNT	R	Device count.	0b0000000
4	HDMI_MODE	R	HDMI mode (set or cleared by writing to local bus): 0 = Device is in DVI mode 1 = Device is in HDMI mode	1
3	CAS_EXC	R	Cascade depth exceeded.	0
2:0	DEV_DEPTH	R	Cascade depth.	0b000

The values for DEV_EXC, DEV_COUNT, CAS_EXC, and DEV_DEPTH are set by writing into the BSTATUS_SET registers from the local I^{2}C bus. The bits DEV_EXC and CAS_EXC indicate to the Source that the HDMI receiver has too many devices attached in the HDCP repeater tree. Refer to the HDCP Specification.

HDCP Repeater Registers

The SiI9013 HDMI receiver supports the HDCP repeater function. Registers are provided to store the downstream KSV values from any attached repeater tree (up to 12 devices).

V.H Registers

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x74	0x20	V.H0.0	V.H0[7:0]							
0x74	0x21	V.H0.1	V.H0[15:8]							
0x74	0x22	V.H0.2	V.H0[23:16]							
0x74	0x23	V.H0.3	V.H0[31:24]							
0x74	0x24	V.H1.0	V.H1[7:0]							
0x74	0x25	V.H1.1	V.H1[15:8]							
0x74	0x26	V.H1.2	V.H1[23:16]							
0x74	0x27	V.H1.3	V.H1[31:24]							
0x74	0x28	V.H2.0	V.H2[7:0]							
0x74	0x29	V.H2.1	V.H2[15:8]							
0x74	0x2A	V.H2.2	V.H223[23:16]							
0x74	0x2B	V.H2.3	V.H2[31:24]							
0x74	0x2C	V.H3.0	V.H3[7:0]							
0x74	0x2D	V.H3.1	V.H3[15:8]							
0x74	0x2E	V.H3.2	V.H3[23:16]							
0x74	0x2F	V.H3.3	V.H3[31:24]							
0x74	0x30	V.H4.0	V.H4[7:0]							
0x74	0x31	V.H4.1	V.H4[15:8]							
0x74	0x32	V.H4.2	V.H4[23:16]							
0x74	0x33	V.H4.3	V.H4[31:24]							

Bit	Label	R/W	Description	Default
31:0	V_H0	R	HDCP Repeater V.H0 (stored LSB in first byte).	0x00000000
31:0	V_H1	R	HDCP Repeater V.H1 (stored LSB in first byte).	0x00000000
31:0	V_H2	R	HDCP Repeater V.H2 (stored LSB in first byte).	0x00000000
31:0	V_H3	R	HDCP Repeater V.H3 (stored LSB in first byte).	0x00000000
31:0	V_H4	R	HDCP Repeater V.H4 (stored LSB in first byte).	0x00000000

V_H0 to V_H4 are parts of the SHA−1 hash value used in the second part of the authentication protocol for HDCP repeaters. The HDMI receiver calculates this value in its hardware, which simplifies the firmware in the repeater.

KSV FIFO Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x74	0x43	KSV_FIFO	KSV_FIFO							

Bit	Label	R/W	Description	Default
7:0	KSV_FIFO	R	KSV data. Read this address repeatedly, without issuing an I^{2}C STOP to retrieve the entire KSV list from the SiI9013 HDMI receiver. The FIFO pointer to the beginning of this FIFO is reset to 0 by RESET# when the last byte of AN (0x74:0x1F) is written or by the next I^{2}C STOP condition on the DDC bus.	0x00

Sink-Accessible Registers (Device Address 0x60)

The state of the CI2CA pin selects between device address 0x60 and 0x62 for these registers (refer to page 1).

ID and Initialization Registers

ID Registers

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x00	VND_IDL				Vendor ID Low Byte				
0x60	0x01	VND_IDH				Vendor ID High Byte				
0x60	0x02	DEV_IDL				Device ID Low Byte				
0x60	0x03	DEV_IDH				Device ID High Byte				
0x60	0x04	DEV_REV				Device Revision Byte				

Bit	Label	R/W	Description	Default
15:0	VND_ID	R	Provides a unique vendor identification through I^{2}C.	0x0001
15:0	DEV_ID	R	Provides a unique device-type identification through I^{2}C.	0x9A 0xB3
7:0	DEV_REV	R	Allows a distinction between revisions of the same device.	0x00

Software Reset Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x05	SRST	HDCPRST _AUTO	ACRRST_ AUTO	AACRST	SWRST_ AUTO	HDCPRST	ACRRST	FIFORST	SW RST

Bit	Label	R/W	Description	Default
7	HDCPRST_AUTO	R/W	Auto HDCP Reset: 0 = Manual HDCP reset (see bit 3) (recommended setting) 1 = Auto HDCP reset whenever SCDT (0x60:0x06[0]) is set to 0 An HDCP Reset resets the cipher engine and reloads the HDCP keys every time SCDT transitions from 0 to 1.	0
6	ACRRST_AUTO	R/W	Auto Audio Clock Regeneration (ACR) reset: 0 = Manual ACR reset (see bit 2) (recommended setting) 1 = Auto ACR reset whenever SCDT (0x60:0x06[0]) is set to 0 ACR reset stops the MCLK output. Clear this bit to restart the MCLK output.	0
5	AACRST	R/W	Auto Audio Control (AAC) reset: 0 = Normal operation (recommended setting) 1 = Manual AAC logic reset	0
4	SWRST_AUTO	R/W	Auto software reset: 0 = Manual software reset (see bit 0) 1 = Auto software reset whenever SCDT (0x60:0x06[0]) is set to 0 An auto software reset stops Auto Audio and reduces the response time to an SCDT event. Silicon Image recommends using SWRST_AUTO instead of SWRST [0].	0
3	HDCPRST	R/W	HDCP reset: 0 = Normal operation 1 = Reset HDCP interface circuits An HDCP reset resets the cipher engine and reloads the BKSV from the embedded keys. This causes HDCP errors and may corrupt the video if HDCP is already enabled. **Note**: Only set this bit to 1 when the BKSV shadow register (0x60:0x1A – 0x60:0x1E) is not 20 1s when SCDT is 1.	0
2	ACRRST	R/W	Audio Clock Regeneration (ACR) reset: 0 = Normal operation 1 = Reset ACR clock divider circuits An ACR reset resets the Audio Clock Recovery system. Set this bit to 1 only when the Fs rate is changed. ACR reset stops the MCLK output. Clear this bit to restart the MCLK output.	0
1	FIFORST	R/W	Audio FIFO reset: 0 = Normal operation 1 = Reset audio FIFO **Note**: An audio FIFO reset clears the FIFO. You must perform an audio FIFO reset after the audio PLL is locked.	0
0	SWRST	R/W	Software reset: 0 = Normal operation 1 = Reset all sections, including audio FIFO, but not the HDCP, AAC, or ACR registers to which you can write A software reset immediately resets all sections. The Video Input Registers are *not* updated until the next VSYNC is detected. Silicon Image recommends using SWRST_AUTO [4] instead of SWRST.	0

When the auto reset bits are enabled, the HDMI receiver can reset its internal states as soon as there is no active TMDS arriving at the inputs. SCDT switches to LOW when the DE signal stops. Auto reset is faster than using the firmware to

detect the SCDT=LOW condition and it performs the reset with a register write across I^{2}C. Individual bits apply to HDCP, ACR, and software reset.

System Status Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x06	STATE	RSVD0				PWR5V	VSYNC	CKDT	SCDT
Bit	**Label**	**R/W**	**Description**							**Default**
3	PWR5V	R	State of the HDMI port's 5V power detect pin.							0
2	VSYNC	R	Current state of the VSYNC signal, as decoded from the TMDS stream.							0
1	CKDT	R	Clock detect: 0 = No clock 1 = Active decoded pixel clock							0
0	SCDT	R	SYNC detect: 0 = No DE 1 = Active decoded DE signal							0

System Control Register #1

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x08	SYS_CTRL1	OCLKDIV		ICLK		PIXS	BSEL	OCKINV	PD#

Bit	Label	R/W	Description	Default
7:6	OCLKDIV	R/W	Output pixel clock divider: 0b00 = No divider; OCLK is 1x frequency of incoming clock 0b01 = Divide by 2; OCLK is one-half the frequency of incoming clock 0b10 = RSVD 0b11 = Divide by 4; OCLK is one-fourth the frequency of incoming clock	0b00
5:4	ICLK	R/W	Input pixel clock replication: 0b00 = 1x clock (no replication) 0b01 = 2x clock (pixel data sent twice) 0b10 = RSVD 0b11 = 4x clock (pixel data sent four times) Write this field with the same value decoded from the AVI InfoFrame's pixel replication field.	0b00
3	PIXS	R/W	Pixel bus select. Select between 12-, 24-, and 48-bit output mode (see BSEL below).	0
2	BSEL	R/W	Video bus mode select. PIXS and BSEL work together to determine the output bus width: | PIXS	BSEL	Bus Width
---	---	---
1	X	48-bit mode
0	1	24-bit mode
0	0	12-bit mode		1
1	OCKINV	R/W	Output clock invert: 0 = Normal output clock (setup and hold to rising edge) 1 = Invert the output clock (setup and hold to falling edge)	0
0	PD#	R/W	Power-down mode: 0 = Power down everything except the functional blocks that are controlled independently: PD_OSC, PD_FULL, PD_PCLK, PD_MCLK 1 = Normal operation **Note**: PD# changes the behavior of the INT output pin.	0

TMDS Input Port Switch Registers

Port Switch Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x09	SYS_SW	DDCDLY_EN	RSVDR0		DDC_EN	RSVDR0			RX_EN

Bit	Label	R/W	Description	Default
7	DDCDLY_EN	R/W	DDC delay enable: 0 = Disable delay on SDA line 1 = Enable 300ns delay on SDA input line **Note**: Enabling this bit creates a 300ns delay for the falling edge of the DDC SDA signal to avoid an erroneous I^{2}C START condition. The start condition must have a setup time of 600 ns and the native circuitry must have a delay smaller that 600ns, but greater than 300ns. For normal operation, this bit must remain set to ensure I^{2}C compliance.	0
4	DDC_EN	R/W	DDC enable: 0 = Disable DDC 1 = Enable DDC	0
0	RX_EN	R/W	TMDS port enable: 0 = Disable TMDS port 1 = Enable TMDS port	0

The SiI9013 HDMI receiver enables its HDMI input port using the bits in the SYS_SW register.

Disabling the DDC port causes the DSDA pin to be tri-stated and the DSCL pin to be disconnected from the signal. If an I^{2}C transaction is ongoing, the HDMI receiver does not respond after the DDC port has been disabled. If the Source starts a new I^{2}C transaction, the SiI9013 HDMI receiver sends no ACK signal. The Source sees no attached device on the I^{2}C bus. Also, enabling a DDC port may cause the HDMI receiver to respond immediately to a Source attached at that port. The Source firmware is responsible for terminating any I^{2}C transaction immediately upon recognizing that the attached SiI9013 HDMI receiver is disabled. This is consistent with designing a Source to handle power-off of the attached Sink at any time and graceful handling of a subsequent power on.

HDCP Registers

HDCP Shadow BKSV Register (Equivalent to 0x74:0x00–0x04)

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x1A	HDCP_BKSV1	Video Receiver Key Selection Vector (KSV)							
0x60	0x1B	HDCP_BKSV2	Video Receiver Key Selection Vector (KSV)							
0x60	0x1C	HDCP_BKSV3	Video Receiver Key Selection Vector (KSV)							
0x60	0x1D	HDCP_BKSV4	Video Receiver Key Selection Vector (KSV)							
0x60	0x1E	HDCP_BKSV5	Video Receiver Key Selection Vector (KSV)							

Bit	Label	R/W	Description	Default
39:0	HDCP_BKSV	R	HDMI receiver's KSV. This value must always be available for reading, except for a time period of at least $T_{BKSVINIT}$ after RESET#. It can be used to determine if the HDMI receiver is HDCP capable.	0

HDCP Shadow Ri Register (Equivalent to 0x74:0x08–0x09)

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x1F	HDCP_RI1	Link Verification Response (Ri)							
0x60	0x20	HDCP_RI2	Link Verification Response (Ri)							

Bit	Label	R/W	Description	Default
15:0	HDCP_RI	R	Link Verification Response. Updated every 128 frames. R_0' is available a maximum of 100 ms after AKSV is received. Subsequent R_i' values are available a maximum of 128 pixel clocks following the assertion of CTL3.	0

The Sink's firmware may monitor the Shadow Ri register to determine whether the SiI9013 HDMI receiver is actively decrypting data. The R_i' value changes every 128 frames during active decryption (the R_i counter increments for frames that are not muted). However, the R_i' also changes if the Source repeatedly attempts an HDCP authentication, in which case the Shadow AN register also changes value. Shadow AN does not change value during normal decryption.

HDCP Shadow AKSV Register (Equivalent to 0x74:0x10–0x14)

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x21	HDCP_AKSV1	Video Transmitter Key Selection Vector (KSV)							
0x60	0x22	HDCP_AKSV2	Video Transmitter Key Selection Vector (KSV)							
0x60	0x23	HDCP_AKSV3	Video Transmitter Key Selection Vector (KSV)							
0x60	0x24	HDCP_AKSV4	Video Transmitter Key Selection Vector (KSV)							
0x60	0x25	HDCP_AKSV5	Video Transmitter Key Selection Vector (KSV)							

Bit	Label	R/W	Description	Default
39:0	HDCP_AKSV	R	HDMI transmitter's KSV.	0

HDCP Shadow AN Register (Equivalent to 0x74:0x18–0x1F)

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x26	HDCP_AN1	Session Random Number (An)							
0x60	0x27	HDCP_AN2	Session Random Number (An)							
0x60	0x28	HDCP_AN3	Session Random Number (An)							
0x60	0x29	HDCP_AN4	Session Random Number (An)							
0x60	0x2A	HDCP_AN5	Session Random Number (An)							
0x60	0x2B	HDCP_AN6	Session Random Number (An)							
0x60	0x2C	HDCP_AN7	Session Random Number (An)							
0x60	0x2D	HDCP_AN8	Session Random Number (An)							

Bit	Label	R/W	Description	Default
63:0	HDCP_AN	R	Session Random Number.	0

HDCP BCAPS Set Register (Equivalent to 0x74:0x40)

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x2E	BCAPS_SET	HDMI_CAPABLE	REPEATER	FIFORDY	FAST	RSVDRW0			

Bit	Label	R/W	Description	Default
7	HDMI_CAPABLE	R/W	HDMI capability: 0 = Device is not HDMI capable 1 = Device is HDMI capable	1
6	REPEATER	R/W	Video repeater capability: 0 = Device is a simple display 1 = Device is a repeater This bit can be set or cleared so that the HDMI receiver can be used where the firmware supports only an HDCP Sink or where the firmware supports HDCP repeaters. **Note**: Set this bit to 1 before the DDC bus is enabled. Set this bit to 1 after a hardware reset. This bit does *not* need to be set to 1 after a software reset.	0
5	FIFO_RDY	R/W	Set in an HDCP-capable repeater by Sink firmware; cleared by the hardware when last downstream AKSV byte is written. This bit should be set when the V′ bit and the KSV list are ready in the HDMI receiver.	0
4	FAST	R/W	I^{2}C fast support: 0 = Device supports up to 100-kbps I^{2}C transfers 1 = Device supports up to 400-kbps I^{2}C transfers **Note**: This bit must always be 0. The HDMI Specification requires the DDC bus be used at 100-kHz speed or less (standard mode I^{2}C).	0

Note: Only write to the BCAPS_SET register when the DDC bus is disabled to prevent an attached Source from reading the H SiI9013 DMI receiver's default BCAPS value (described on page 5), before it is initialized by the firmware. Control the DDC port with SYS_SW (described on page 12).

HDCP BSTATUS_SET Register (Equivalent to 0x74:0x41–0x42)

These registers set the fields for the HDCP Repeater tree and are read by the Source in the BSTATUS register on the DDC bus (see page 5).

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x2F	SHD_BSTAT1	DEV_EXCEED	DEVICE_CNT						
0x60	0x30	SHD_BSTAT2	RSVDRW0			HDMI_MODE	CASC_EXCEED	DEPTH		

Bit	Label	R/W	Description	Default
7	DEV_EXCEED	R/W	Maximum number of HDCP devices allowed in the tree exceeded. The HDMI receiver supports up to 12 devices in the KSV LIST.	0
6:0	DEVICE_CNT	R/W	Total number of HDCP devices attached in the repeater tree.	0b00 0000
4	HDMI_MODE	R	0 = DVI mode 1 = HDMI mode	0
3	CASC_EXCEED	R/W	Maximum number of cascade levels allowed in device tree exceeded.	0
2:0	DEPTH	R/W	Number of levels of HDCP devices cascaded to this repeater device.	0

HDCP Debug Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x31	HDCPDEBUG	STOPHDCP	RSVD0						

Bit	Label	R/W	Description	Default
7	STOPHDCP	R/W	Notify the Source to retry authentication: 0 = Normal operation, decrypt when enabled by authentication 1 = Clear the R_i' value in the HDMI receiver so that the Source retries authentication. This bit is cleared when the Source re-authenticates the HDMI receiver. **Note**: When errors in decrypted content are detected, set this bit to force the R_i' value to mismatch the R_i value in the HDMI transmitter. The HDMI receiver indicates in the Link Integrity Check that HDCP decryption has stopped. This bit is cleared by hardware when the AKSV is written to the DDC register.	0

HDCP Status Register

The HDCP_STAT register is used by the Sink's firmware to determine the status of HDCP.

Dev	Addr	Name		7	6	5	4	3	2	1	0
0x60	0x32	HDCP_STAT		RSVD0		DECRYPT	AUTHEN	RSVD0			
Bit	**Label**	**R/W**		**Description**							**Default**
5	DECRYPT	R		Used by the Sink's firmware to determine HDCP decryption status: 0 = HDCP decryption is inactive 1 = HDCP decryption is active This bit is set only when decryption is active. It is updated once per frame by checking for both an active VSYNC and a CTL3 pulse. If encryption has been disabled using General Control packets (no CTL3s), this bit is zero. It is set again when HDCP is un-muted.							0
4	AUTHEN	R		Used by the Sink's firmware to determine HDCP authentication status: 0 = HDCP authentication not attempted 1 = HDCP authentication attempted If authentication is attempted, this bit is set (even if authentication did not complete). This bit is set after R_0' calculation is complete, but this does not indicate if R_0' equals R_0 in the Source. Only the Source knows that result.							0

HDCP KSV/SHA Start Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x33	KSVSHA_ST1	KSVSHA_START[7:0]							
0x60	0x34	KSVSHA_ST2	RSVDRW0						KSVSHA_START[9:8]	
Bit	**Label**	**R/W**	**Description**							**Default**
9:0	KSVSHA_START	R/W	KSV FIFO / SHA start address.							0x0000

Note: Register 0x33 must be written before register 0x34. The values for these two bytes are not latched into the HDMI receiver until the end of the I2C WRITE command for address 0x34. Also, an active RxCLK (TMDS link pixel clock) is required when writing these two registers. An active RxCLK can be checked by reading the CKDT bit in the STATE register (0x60:0x06[1]).

HDCP SHA Length Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x35	SHA_LEN1	SHA_LENGTH[7:0]							
0x60	0x36	SHA_LEN2	RSVDRW0						SHA_LENGTH[9:8]	
Bit	**Label**	**R/W**	**Description**							**Default**
9:0	SHA_LENGTH	R/W	The number of KSVs to process, in bytes. The range is compatible with HDCP 1.1, but the KSV FIFO is only large enough for 12 KSVs (5x16 = 80 bytes).							0x000

HDCP SHA Control Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x37	SHA_CTRL	RSVDRW0					SHA_MODE	RSVD0	SHA_GO
Bit	**Label**	**R/W**	**Description**							**Default**
2	SHA_MODE	R/W	SHA mode: 0 = Upstream use. KSV_FIFO, SHD_BSTAT (0x60:0x2F–0x30), and an internal value of M0 is used for calculation. 1 = Downstream use. KSV_FIFO, DS_BSTAT (0x60:0xD5–0xD6), and DS_M0 (0x60:0xD7–0xDE) is used for calculation; the results are shown in DS_VH (0x60:0xDF–0xF2).							0
0	SHA_GO	R/W	Allow SHA to access KSV FIFO: 1 = Initiate an SHA calculation in the hardware. The firmware should then poll this bit: 0 implies the hardware is not ready, 1 implies SHA calculation is done. The calculation time is proportional to the pixel clock period. At the slowest speed (25 MHz), the time is approximately 15 µs.							0

HDCP Repeater KSV FIFO Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x38	KSV_FIFO	KSV_FIFO							
Bit	**Label**	**R/W**	**Description**							**Default**
7:0	KSV_FIFO	R/W	This address is a port for KSV FIFO access. When the firmware starts an I^{2}C transaction with the offset address set at 0x38, access control is transferred to the KSV FIFO. The address located inside the KSV Start Address registers (KSVSHA_ST1,2) acts as the start offset within the KSV FIFO space. Consecutive I^{2}C transactions to address 0x38 are auto-incremented in the KSV FIFO address space.							0x00

Video Input Registers

The SiI9013 HDMI receiver provides the logic to detect the details of the incoming video resolution. The clock used to count these pixel-related units counts at the rate after the RxCLK divider (see register 0x60:0x08[5:4] on page 11). If the input RxCLK stops, the values in these registers maintain their value. Use CKDT and SCDT to determine if the input stream is active video.

Video H Resolution Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x3A	H_RESL	H_RES[7:0]							
0x60	0x3B	H_RESH	RSVD0			H_RES[12:8]				
Bit	Label	R/W	Description						Default	
12:0	H_RES	R	Measured interval between two HSYNC active edges. The unit of measure is unique pixels. See the note on page 20.						0b0 0000 0000 0000	

Video V Refresh Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x3C	V_RESL	V_RES[7:0]							
0x60	0x3D	V_RESH	RSVD0						V_RES[10:8]	
Bit	Label	R/W	Description						Default	
10:0	V_RES	R	Measured interval between two VSYNC active edges. The unit of measure is lines (HSYNC pulses). **Note**: The value for V_RES, measured in lines, may change from field to field for interlaced formats. For example, 1080i has a total line count of 1125 but sends either 562 or 563 lines per field. Also, some ITU.656 sources may send active line counts in interlaced formats, which switch between two values. Firmware that reads this register to determine active video mode should allow for this variation.						0b000 0000 0000	

Video DE Pixels Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x4E	DE_PIXL	DE_PIX[7:0]							
0x60	0x4F	DE_PIXH	RSVD0				DE_PIX[11:8]			
Bit	Label	R/W	Description						Default	
11:0	DE_PIX	R	Defines the width of the active display. The unit of measure is unique pixels. See the note on page 20.						0b0000 0000 0000	

Video DE Line Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x50	DE_LINL	DE_LIN[7:0]							
0x60	0x51	DE_LINH	RSVD0						DE_LIN[10:8]	
Bit	**Label**	**R/W**	**Description**						**Default**	
10:0	DE_LIN	R	Defines the height of the active display. The unit of measure is lines (HSYNC pulses). **Note**: The value for DE_LIN, measured in lines, may change from field to field for interlaced formats. For example, 1080i has a total line count of 1125 but sends either 562 or 563 lines per field. Also, some ITU.656 sources may send active line counts in interlaced formats, which switch between two values. Firmware that reads this register to determine active video mode should allow for this variation.						0b000 0000 0000	

Video VSYNC to Active Video Lines Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x52	VID_VTAVL	RSVD0		VID_VTAVL[5:0]					
Bit	**Label**	**R/W**	**Description**						**Default**	
5:0	VID_VTAVL	R	VSYNC to Active Video Lines. Vertical sync width plus vertical back porch, measured in lines from the decoded TMDS input stream.						0b00 0000	

Video Vertical Front Porch Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x53	VID_VFP	RSVD0		VID_VFP[5:0]					
Bit	**Label**	**R/W**	**Description**						**Default**	
5:0	VID_VFP	R	VSYNC Front Porch. Vertical sync front porch time, measured in lines from the decoded TMDS input stream.						0b00 0000	

Video Status Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x55	VID_STAT	RSVD0					INTRL	VSPOL	HSPOL
Bit	**Label**	**R/W**	**Description**						**Default**	
2	INTRL	R	Interlace detected: 0 = Input progressive 1 = Input interlaced						0	
1	VSPOL	R	VSYNC polarity detected: 0 = Negative polarity (leading edge falls) 1 = Positive polarity (leading edge rises)						0	
0	HSPOL	R	HSYNC polarity detected: 0 = Negative polarity (leading edge falls) 1 = Positive polarity (leading edge rises)						0	

Note: The polarity of VSPOL and HSPOL is opposite that of the equivalent bits in the SiI9030 transmitter. The INTRL bit is set by internally checking for a varying VSYNC timing characteristic of interlaced field timings.

Video Horizontal Front Porch Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x59	VID_HFP				VID_HFP				
Bit	**Label**	**R/W**	**Description**						**Default**	
7:0	VID_HFP	R	Horizontal Front Porch. This is the number of pixel clocks between the end of data valid (falling edge of DE) and the start of the HSYNC pulse. This register does not wrap — it stops counting at 255 and remains at that value. See the note below.						0x00	

Video HSYNC Active Width Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x5B	VID_HSWIDL				HSWIDTH[7:0]				
0x60	0x5C	VID_HSWIDH			RSVD0				HSWIDTH[9:8]	
Bit	**Label**	**R/W**	**Description**						**Default**	
9:0	HSWIDTH	R	Width of HSYNC pulse in units of unique pixels. See the note below.						0b 00 0000 0000	

There is no register to indicate the vertical refresh rate (for example, 60-Hz NTSC), but the refresh rate can be calculated using the VID_XPCNT register.

Note: The values for H_RES, DE_PIX, VID_HFP, and HSWIDTH are measured after the link clock is divided by the pixel replication rate. The AVI InfoFrame carries a definition of the pixel replication rate (when the normal pixel rate is slower than 25 MHz, pixel replication is used). This value is to be written into the ICLK field in the SYS_CTRL1 register (0x60:0x08[5:4], described on page 11. Before the ICLK field is written, the values in H_RES, DE_PIX, VID_HFP, and HSWIDTH reflect the prior setting of ICLK. For example, if ICLK is set to 0 (no replication), then a 2x replication stream for 480i shows 1440 as the DE_PIX count. After setting ICLK to 1 (per the AVI InfoFrame information), the value in DE_PIX is 720. Vertical measurements in lines are not affected by pixel replication.

Video Pixel Clock Timing Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x6F	VID_XPCNT				VID_XPCNT				
Bit	**Label**	**R/W**	**Description**						**Default**	
7:0	VID_XPCNT	R	The number of crystal clocks (XCLK) per 127 video clock periods.						0x00	

VID_XPNT is read to determine the pixel clock rate in real units of time. This value translates into line time as follows:

$$T_{LINE} = \frac{\dfrac{H\_RES}{127} \times VID\_XPCNT}{F_{XTAL}}$$

When calculating line time from the value in register VID_XPCNT, remember that integer math should avoid overflow and underflow in the calculation. The firmware should calculate the line time in this sequence:

$$T_{LINE} = \frac{H\_RES}{F_{XTAL}} \times VID\_XPCNT \times \frac{1}{127}$$

Having determined the line time, the frame/field time may be calculated:

$$T_{Frame/Field} = T_{Line} * (V\_RES)$$

Refer to the *CEA-861B Specification* for more details on the complete set of CEA-861B timings.

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Video Processing Register Set

Video Mode #1 Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x4A	VID_MODE	INSSYNC	MUXYC	DITH	RNG_R2Y	CSC_R2Y	UPSMP	DNSMP	RSVDR0

Bit	Label	R/W	Description	Default
7	INSSYNC	R/W	Insert SYNC (SAV/EAV) into ITU.656 stream: 0 = Disable 1 = Enable	0
6	MUXYC	R/W	Multiplex YC 4:2:2 into a single channel: 0 = Disable 1 = Enable	0
5	DITH	R/W	10-bit to 8-bit dithering: 0 = Disable 1 = Enable **Note**: Only effective if the incoming color space is YCbCr 4:2:2.	0
4	RNG_R2Y	R/W	RGB-to-YCbCr range scaling: 0 = Bypass 1 = Compress 0–255 to 16–235	0
3	CSC_R2Y	R/W	RGB-to-YCbCr color-space convert: 0 = Bypass 1 = Convert RGB to YCbCr Use with CSP_R2Y (0x60:0x48[0]). **Note:** Writing this bit to 1 causes VRCHG and ILCHG interrupts (see page 31). This may also occur for certain settings of VID_AOF, which enable RGB-to-YCbCr conversion (see register 0x60:0x5F, described on page 24).	0
2	UPSMP	R/W	Upsample: 0 = Bypass 1 = 4:2:2 to 4:4:4 upsampler	0
1	DNSMP	R/W	Downsample: 0 = Bypass 1 = 4:4:4 to 4:2:2 downsampler	0

There is no programmability for F, V, and H bits in the SAV/EAV bytes. Out-of-range values 0x00 and 0xFF are converted to 0x01 and 0xFE when SAV/EAV codes are inserted.

The link never carries SAV/EAV encoded data. HSYNC and VSYNC states are carried on the link using either out-of-band TMDS characters (during DE low times), or as described in the HDMI Specification during data islands.

Video Mode #2 Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x49	VID_MODE2	RSVDRW0				RNG_Y2R	CSC_Y2R	RSVDR0	

Bit	Label	R/W	Description	Default
3	RNG_Y2R	R/W	Enable YCbCr-to-RGB data range scaling: 0 = Disable range scaling for color-space converter 1 = RGB data range scaling from 16–235 to 0–255	0
2	CSC_Y2R	R/W	YCbCr-to-RGB color-space convert: 0 = Bypass 1 = Convert YCbCr to RGB Use with CSP_Y2R (0x60:0x48[2]).	0

Video Output Composite Sync Generator

Video Control Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x48	VID_CTRL	IVS	IHS	RSVDR0			CSP_Y2R	BITM	CSP_R2Y

Bit	Label	R/W	Description	Default
7	IVS	R/W	Inverts the VSYNC signal that comes over the link before it exits the chip on the VSYNC output pin: 0 = Do not invert the VSYNC signal 1 = Invert the VSYNC signal **Note**: Before setting this bit to 1, check the VSPOL bit in the VID_STAT register (0x60:0x55[1]).	0
6	IHS	R/W	Inverts the HSYNC signal that comes over the link before it exits the chip on the HSYNC output pin: 0 = Do not invert the HSYNC signal 1 = Invert the HSYNC signal **Note**: Before setting this bit to 1, check the HSPOL bit in the VID_STAT register (0x60:0x55[0]).	0
2	CSP_Y2R	R/W	YCbCr-to-RGB color-space conversion: 0 = BT.601 1 = BT.709 Use with CSC_Y2R (0x60:0x49[2]).	0
1	BITM	R/W	Extended bit mode: 0 = Decoded pixel values are 8 bits wide, either RGB or YCbCr 1 = Decoded pixel values are YCbCr 4:2:2 and wider than 8 bits **Note**: BITM picks up LSB data from TMDS channel 0, then sends it to Channel 1 and Channel 2. Set this bit to 4 for YCbCr 4:2:2 color-space only.	0
0	CSP_R2Y	R/W	RGB-to-YCbCr color-space conversion: 0 = BT.601 1 = BT.709 Use with CSC_R2Y (0x60:0x4A[3]).	0

Video Field 2 Back Porch Mode Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x54	VID_F2BPM	RSVD0							BPM

Bit	Label	R/W	Description	Default
0	BPM	R/W	Adjusts the position of the active video lines during Field 2 of an interlaced field relative to Field 1: 0 = Back porch of Field 2 is one-half line shorter than the back porch of Field 1 1 = Back porch of Field 2 is one-half line longer than the back porch of Field 1 This information is used by the ITU.656 encoder to determine when to transition the F bit for Field 2.	1

Video Digital Blank Value Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x4B	VID_BLANK 1	VID_BLANK1[7:0]							
0x60	0x4C	VID_BLANK 2	VID_BLANK2[7:0]							
0x60	0x4D	VID_BLANK 3	VID_BLANK3[7:0]							

Bit	Label	R/W	Description	Default
7:0	VID_BLANK1	R/W	Video Blanking for Channel 1 (Blue).	0x00
7:0	VID_BLANK2	R/W	Video Blanking for Channel 2 (Green).	0x00
7:0	VID_BLANK3	R/W	Video Blanking for Channel 3 (Red).	0x00

These registers define the video level used during blanking times and are necessary because this value is not explicitly transported during data island times. These values should always be programmed to define the blanking level for video received from the HDMI transmitter.

These registers also define the video output value when muting video *except* when SAV/EAV syncs are enabled or downsampling is enabled, in which case, Y=16 and Cb=Cr=128 are output, regardless of the values in VID_BLANK.

Note: RGB is allowed in PC resolutions (with zero for blanking levels) and in CE resolutions (with 16 for blanking levels). See EIA/CEA-861B Section 5.1.

The actual video blanking values are affected by the CSC (Color Space Conversion) settings. If any CSC bits are enabled, the video blanking value is the value before CSC.

Video Channel Mapper Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x56	VID_CH_MAP	RSVD0					CH_MAP		

Bit	Label	R/W	Description	Default
2:0	CH_MAP	R/W	Video channel mapping. Swaps the 3-byte digital video output through the following six permutations onto the output package pins, calling the input Q[23:0]: 		Q[23:16]	Q[15:8]	Q[7:0]	 |---|---|---|---| 	0b000	RED	GREEN	BLUE	 	0b001	RED	BLUE	GREEN	 	0b010	GREEN	RED	BLUE	 	0b011	GREEN	BLUE	RED	 	0b100	BLUE	RED	GREEN	 	0b101	BLUE	GREEN	RED	 **Note**: 0b000 (the default) may be interpreted as *no swapping*; output = input. Also, permutations associated with 0b110 and 0b111 map to the default 0b000, and because of the redundancy, are not included in this list. This bit allows any of the three decoded TMDS video channels to be output on any of the three output channels. This facilitates connection to different downstream chips, which may expect Red, Green, or Blue on channels other than the default configuration.	0b000

Auto Video Configuration Registers

Auto Output Format Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x5F	VID_AOF				VID_AOF				

Bit	Label	R/W	Description	Default
7:0	VID_AOF	R/W	Specifies the auto video output format for AVC mode. Table 4 lists the allowed settings for this register. Values not listed are unsupported. AVC mode is enabled by setting AVC_EN in register 0x60:0xB5, described on page 34.	0x00

Table 4. Allowed Auto Output Format Register

Register VID_AOF	Color Space	Bits per Channel	4:4:4 or 4:2:2	Multiplexed	Embedded Syncs
0x00	RGB	8	4:4:4	NO	NO
0x80	YCbCr	8	4:4:4	NO	NO
0xC0	YCbCr	8	4:2:2	NO	NO
0xC8	YCbCr	10	4:2:2	NO	NO
0xD0	YCbCr	8	4:2:2	NO	YES
0xD8	YCbCr	10	4:2:2	NO	YES
0xE0	YCbCr	8	4:2:2	YES[1]	NO
0xE8	YCbCr	10	4:2:2	YES[1]	NO
0xF0	YCbCr	8	4:2:2	YES[1]	YES
0xF8	YCbCr	10	4:2:2	YES[1]	YES

Note 1: Valid only with 24-bit output bus (see System Control Register #1).

The HDMI receiver decodes the AVI InfoFrame and determines which features in the video processing path must be enabled or disabled to format the video into the output mode selected in VID_AOF.

Note: AVC is not affected directly by a change in video refresh rate. A change in video resolution (such as a switch from 480p to 1080i) with accompanying AVI InfoFrame change causes only the color-space converter to switch from BT.601 to BT.709 (register 0x60:0x48).

Refer to the *SiI9011/9021/9031 HDMI PanelLink Receivers Application Note* (SiI-AN-0118) for information on how AVC works without AVI InfoFrames and in DVI mode.

Interrupt Registers

Interrupt State Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x70	INTR_STATE	RSVD0							INTR

Bit	Label	R/W	Description	Default
0	INTR	R	Interrupt state. Whenever an interrupt is asserted, this bit is HIGH. The polarity of the INT pin output signal is applied after this bit. Refer to Figure 1 on page 26.	0

For registers INTR1 through INTR6, a bit is set when the interrupt is asserted and cleared by writing it to 1. The unmask registers are used to select which of the bits from INTR1 through INTR6 affect the INTR bit in register INTR_STATE.

Interrupt Unmask Registers

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x75	INTR1_UNMASK								
0x60	0x76	INTR2_UNMASK								
0x60	0x77	INTR3_UNMASK								
0x60	0x78	INTR4_UNMASK								
0x60	0x7D	INTR5_UNMASK								
0x60	0x7E	INTR6_UNMASK								

Bit	Label	R/W	Description	Default
		R/W	Each bit corresponds to the same bit in registers INTR1 to INTR6. When set, the corresponding interrupt can affect the state of INTR in INTR_STATE. When cleared in the unmask, the interrupt bit in INTR1 to INTR6 is still active but does not affect INTR in INTR_STATE. See page 26 for more information.	0

Interrupt Control Register

Note: The INT_CTRL register is affected by PD#, as described on page 11.

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x79	INT_CTRL	RSVD0				SOFT_INTR	OPEN_DRAIN	POLARITY#	RSVD0

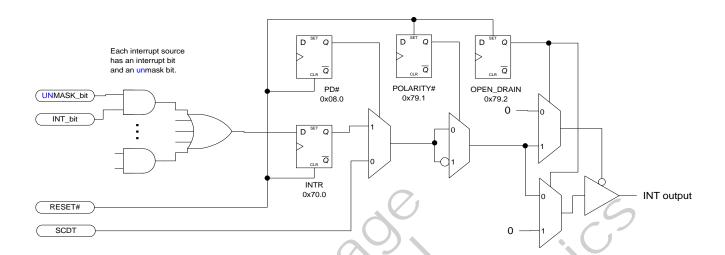| Bit	Label	R/W	Description	Default
3	SOFT_INTR	R/W	Set software interrupt: 0 = Clear interrupt 1 = Set	0
2	OPEN_DRAIN	R/W	INT pin output type: 0 = Push/Pull 1 = Open Drain pin	1
1	POLARITY#	R/W	INT pin assertion level: 0 = Assert HIGH 1 = Assert LOW	1

Figure 1. Interrupt Pin Control

The diagram in Figure 1 shows the control of the INT output pin. Each interrupt source has a bit (shown as INT_bit) and an unmask (shown as UNMASK_bit). These are logically ANDed, then ORed, then latched with the active output clock. During RESET#=LOW, PD# is reset to zero. In power-down mode (PD# asserted), the active level from the sync detect logic (SCDT) is output as the INT signal.

The POLARITY# and OPEN_DRAIN controls affect INT in all modes. RESET#=LOW loads PD#=0, POLARITY#=1, and OPEN_DRAIN=1 as a default. Therefore, the INT output will be open-drain, driven LOW when no TMDS signaling is received, and tri-stated when the TMDS inputs are active.

Avoiding Stuck Interrupts

Glitches caused by an unstable source or a hot plug event can cause the FIFO under-run interrupt (FIFO_UNDER at 0x60:0x74[0]) to be set but not cleared until you apply a hardware reset. Applying a hardware reset ensures that the interrupt is no longer in an invalid state. Using auto software reset (SWRST_AUTO) can also reduce stuck interrupts.

To avoid stuck interrupts, Silicon Image recommends performing a hardware reset after every board initialization, HDMI cable plug-in, and HDMI input change.

Important: After a hardware reset, the SiI9013 HDMI receiver uses the default configuration. Before performing the hardware reset, you must save your HDMI receiver register settings and then restore the settings after the hardware reset is complete. If hardware reset is shared among other devices, it needs to be used independently for the SiI9013 HDMI receiver.

Using Auto Software Reset

Some systems monitor error conditions (such as a FIFO_UNDER) with firmware and then react to a loss of sync by asserting SWRST through I^{2}C. This process is not fast enough to block all glitches and, therefore, allows occasional locking of a FIFO interrupt.

Silicon Image recommends enabling automatic software reset (SWRST_AUTO at 0x60:0x05[4]) in the firmware. SWRST_AUTO causes a software reset to be performed whenever the HDMI receiver detects a loss of TMDS clock (CKDT) or loss of video signals (SCDT). Because glitches occur most often during stabilization of the link clock (after a link mode change or a hot plug event), an active software reset that blocks such glitches protects the FIFO_UNDER logic from changes until both clocks and syncs are stable. After SWRST_AUTO is enabled, the firmware does not need to perform any manual resets (SWRST).

Interrupt Status #1 Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x71	INTR1	ACR HWCTS	ACR HWN	ACRERR	ACR PLLUL	AUDF ERR	ECCERR	AUTH START	AUTH DONE

Bit	Label	R/W	Description	Default
7	ACRHWCTS	R/W	1 = Most recent ACR hardware CTS value is different from previous value. Write 1 to clear.	0
6	ACRHWN	R/W	1 = Most recent ACR hardware N value is different from previous value. Write 1 to clear.	0
5	ACRERR	R/W	1 = Audio N/CTS packet decode error. Write to 1 to clear.	0
4	ACRPLLUL	R/W	1 = Audio PLL unlocked. Write 1 to clear.	0
3	AUDFERR	R/W	1 = Audio FIFO error (a one-bit error in an audio packet). Write 1 to clear.	0
2	ECCERR	R/W	1 = ECC error in any data island that also causes the error count to exceed the BCH threshold. Write 1 to clear.	0
1	AUTHSTART	R/W	1 = HDCP authentication has started. Authentication starts with receipt of the eighth byte of AN from the Source. Write 1 to clear.	0
0	AUTHDONE	R/W	1 = HDCP authentication done. Authentication ends with receipt of the first control pulse (encrypted frame). Write 1 to clear. **Note**: Software reset does not clear this interrupt.	0

For information on monitoring the status of HDCP decryption, see page 13.

Interrupt Status #2 Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x72	INTR2	HDMIMODE	VSYNCDET	SWINTR	CKDT	SCDT	GOTCTS	GOTAUD	VIDCHG

Bit	Label	R/W	Description	Default
7	HDMIMODE	R/W	1 = HDMI mode change detected (DVI-to-HDMI or HDMI-to-DVI). Write 1 to clear.	0
6	VSYNCDET	R/W	1 = VSYNC active edge recognized. Write 1 to clear.	0
5	SWINTR	R/W	1 = Software-induced interrupt. Write 1 to clear.	0
4	CKDT	R/W	1 = Clock detect change detected. Write 1 to clear.	0
3	SCDT	R/W	1 = Sync detect change detected (monitors DE signal). Write 1 to clear.	0
2	GOTCTS	R/W	1 = Received CTS packet. Write 1 to clear.	0
1	GOTAUD	R/W	1 = Received audio packet. Write 1 to clear.	0
0	VIDCHG	R/W	1 = Video clock frequency changed. Write 1 to clear.	0

Interrupt Status #3 Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x73	INTR3	NEW_GCP	SET MUTE	SPDIFERR	NEW_UNR	NEW_MPEG	NEW_AUD	NEWSP	NEW_AVI

Bit	Label	R/W	Description	Default
7	NEW_GCP	R/W	1 = New General Control Packet detected. Write 1 to clear. **Note**: This bit is set on *every* detected General Control Packet, regardless of whether the content of the packet changed. This behavior is different from the *on change only* behavior of the other packet detection interrupts.	0
6	SETMUTE	R/W	1 = General Control Packet set to mute. Write 1 to clear.	0
5	SPDIFERR	R/W	1 = S/PDIF parity error. Write 1 to clear.	0
4	NEW_UNR	R/W	1 = New/changed unrecognized packet detected. Write 1 to clear. This bit is set whenever a packet or InfoFrame is received that is not one of the known HDMI types or with values other than those set in the Packet Type Decode registers. See page 61 for more information.	0
3	NEW_MPEG	R/W	1 = New/changed MPEG InfoFrame detected. Write 1 to clear.	0
2	NEW_AUD	R/W	1 = New/changed audio InfoFrame detected. Write 1 to clear.	0
1	NEWSP	R/W	1 = New/changed Source Product Definition (SPD) InfoFrame detected. Write 1 to clear.	0
0	NEW_AVI	R/W	1 = New/changed AVI InfoFrame detected. Write 1 to clear.	0

Stopping and restarting transmission of InfoFrames or packets from the Source does not trigger any of the interrupts in INTR3 if the packet content is unchanged.

Interrupt Status #4 Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x74	INTR4	RSVDR0	HDCP ERR	T4ERR	NO_ AVI	CTS_DROP	CTS_ REUSE	FIFO_ OVER	FIFO_ UNDER

Bit	Label	R/W	Description	Default
6	HDCPERR	R/W	1 = HDCP error. Set when a BCH error is received but no TERC4 errors are received. Write 1 to clear.	0
5	T4ERR	R/W	1 = TERC4 error. Set when the number of corrected TERC4 errors exceeds the TERC4 corrected threshold or the number of uncorrected TERC4 errors exceeds the TERC4 uncorrected threshold during the data island period. The TERC4 corrected threshold is set in register 0x60:0xBD[6:0], described on page 35. The TERC4 uncorrected threshold is set in register 0x60:0xBE[6:0], described on page 35. Write 1 to clear.	0
4	NO_AVI	R/W	1 = No AVI received. Set when no AVI InfoFrame has been received for at least 2 consecutive fields. Write 1 to clear.	0
3	CTS_DROP	R/W	1 = CTS dropped. Set when the CTS value is dropped because a new packet value overwrites a CTS value before it is used to generate an NCLK period. $NCLK=128*F_S/N$. Write 1 to clear.	0
2	CTS_REUSE	R/W	1 = CTS reused. Set when the CTS value is reused because a new CTS value is not available when the previous NCLK period finishes. Write 1 to clear.	0
1	FIFO_OVER	R/W	1 = FIFO over-run. Write 1 to clear.	0
0	FIFO_UNDER	R/W	1 = FIFO under-run. This interrupt bit is not set for all under-run conditions. Write 1 to clear. See page 26 for information on stuck interrupts.	0

Interrupt Packet Control Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x7A	IP_CTRL	RSVDR0		NEW_ ACP	NEW_UNR	NEW_ MPEG	NEW_ AUD	NEW_ SPD	NEW_ AVI

Bit	Label	R/W	Description	Default
5	NEW_ACP	R/W	Interrupt on ACP packet: 0 = Set interrupt only on a new ACP packet 1 = Set interrupt on any received ACP packet	0
4	NEW_UNR	R/W	Interrupt on unrecognized packet: 0 = Set interrupt only on a new unrecognized packet 1 = Set interrupt on any received unrecognized packet	0
3	NEW_MPEG	R/W	Interrupt on MPEG InfoFrame: 0 = Set interrupt only on a new MPEG InfoFrame 1 = Set interrupt on any received MPEG InfoFrame	0
2	NEW_AUD	R/W	Interrupt on Audio InfoFrame: 0 = Set interrupt only on a new Audio InfoFrame 1 = Set interrupt on any received Audio InfoFrame	0
1	NEW_SPD	R/W	Interrupt on SPD InfoFrame: 0 = Set interrupt only on a new SPD InfoFrame 1 = Set interrupt on any received SPD InfoFrame	0
0	NEW_AVI	R/W	Interrupt on AVI InfoFrame: 0 = Set interrupt only on a new AVI InfoFrame 1 = Set interrupt on any received AVI InfoFrame	0

Interrupt Status #5 Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x7B	INTR5	FNCHG	AACDONE	AULERR	VRCHG	HRCHG	POCHG	ILCHG	FSCHG

Bit	Label	R/W	Description	Default
7	FNCHG	R/W	1 = Fn Change. Set when the ACR reference clock changes. Write 1 to clear. **Note**: This interrupt Indicates a change in the ratio 128Fs/N. A simultaneous FSCHG interrupt should occur.	0
6	AACDONE	R/W	1 = Auto Audio Control (AAC) muted the audio based on a selected interrupt condition. Write 1 to clear.	0
5	AULERR	R/W	1 = Audio link error. Set when the number of recorded BCH errors is greater than three and the BCH errors are received in at least half of all the recorded packets. Audio packet reception and BCH errors start recording when you set CAPCNT (0x60:0xBB[0]) to 1. Write 1 to clear.	0
4	VRCHG	R/W	1 = Vertical (VSYNC) resolution change. Write 1 to clear.	0
3	HRCHG	R/W	1 = Horizontal (HSYNC) resolution change. Write 1 to clear.	0
2	POCHG	R/W	1 = Polarity change on VSYNC or HSYNC. Write 1 to clear.	0
1	ILCHG	R/W	1 = Interlaced status change. Write 1 to clear.	0
0	FSCHG	R/W	1 = Audio Fs sample rate change. Write 1 to clear.	0

NOTE: VRCHG and ILCHG interrupts are also caused whenever the CSC_R2Y color-space converter is enabled (by writing 1 to register 0x60:0x4A[4], described on page 21). Such interrupts should be ignored until the video path is reprogrammed (in the VID_MODE and VID_MODE2 registers), then the interrupts should be cleared. VRCHG or ILCHG interrupts that occur after that point should be treated as valid changes in refresh rate or interlace state.

Interrupt Status #6 Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x7C	INTR6	RSVDRW0					NEW_ACP	RSVDRW0	UNPLUG

Bit	Label	R/W	Description	Default
2	NEW_ACP	R/W	1 = New/changed ACP packet detected. Write 1 to clear.	0
0	UNPLUG	R/W	1 = Cable unplug interrupt. Set when the PWR5V pin changes from 1 to 0 (see page 10). Write 1 to clear.	0

Bit 0x7C[1] is reserved. It may be set by the chip (and read back as a set bit), but a 1 value in bit 1 does not affect the INTR_STATE register (0x60:0x70). When polling INTR6, the firmware should ignore the state of bit 1.

Audio Input Configuration and Control Registers

TMDS Equalization Control Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x81	TMDS_ECTL1				TMDS_EQCTL				

Bit	Label	R/W	Description	Default
7:0	TMDS_EQCTL	R/W	Cable equalization. Equalization combines amplification and filtering to improve the response to weaker signals received from longer cables. A higher value in this register corresponds to more equalization, appropriate for longer cables. The value in this register should always be such that the value of the four upper bits added to the value of the four lower bits sums to 0x0F. Therefore, valid values for the register are (from lowest equalization to highest equalization): 0x0F, 0x1E, 0x2D, 0x3C, 0x4B, 0x5A, 0x69, 0x78, 0x87, 0x96, 0xA5, 0xB4, 0xC3, 0xD2, 0xE1, and 0xF0. Other values are not supported. Equalization cannot be turned off, but can be programmed to its lowest setting (0x0F).	0xC3

HDCP Key Registers

HDCP Key Status Register

Write a bit in this register to 0 to clear the corresponding condition bit.

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0xF9	KEY_STATUS	RSVD	BIST2_ERR	BIST1_ERR	KSV_DONE	ACK_ERR	SDA_ERR	CRC_ERR	CMD_DONE

Bit	Label	R/W	Description	Default
6	BIST2_ERR	R/W	1 = BIST self-authentication test 2 error.	0
5	BIST1_ERR	R/W	1 = BIST self-authentication test 1 error.	0
4	KSV_DONE	R/W	1 = KSV load is done.	0
3	ACK_ERR	R/W	1 = Acknowledge error (did not get acknowledge from ROM).	0
2	SDA_ERR	R/W	1 = SDA error (ROM still driving SDA line).	0
1	CRC_ERR	R/W	1 = CRC error.	0
0	CMD_DONE	R/W	1 = Command done (last operation completed successfully).	0

HDCP Key Command Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0xFA	KEY_COMMAND	RSVD0		LD_KSV	EPCM				

Bit	Label	R/W	Description	Default
5	LD_KSV	R/W	Enable KSV load from embedded keys: 0 = Disable 1 = Enable (write 0 before enabling again)	N/A
4:0	EPCM	R/W	I^2C master command to the embedded keys: 0b00000 = Run no BIST tests 0b00011 = Run all BIST tests 0b00100 = Run only CRC test 0b01000 = Run only BIST self-authentication test 1 (a 16-bit CRC to verify embedded key contents) 0b10000 = Run only BIST self-authentication test 2 (a 2-pass authentication that uses an inverted key selection vector to verify the HDCP cipher engine) Do not use any other values. Before writing a new value into this register, verify that the previous command is complete by checking the CMD_DONE bit (0x60:0xF9[0]) and then clearing it.	0b00000

You can perform the BIST command when:

1. RESET# pin is HIGH.
2. The TMDS port is enabled.
3. TMDSCLK is active.
4. The HDCP cipher engine is idle — there is no active HDCP authentication.
5. The chip is not accessing the embedded keys automatically, which occurs only when:
   a) The SiI9013 HDMI receiver reads BKSV from the embedded keys during the 2 ms directly after RESET# rising edge, when conditions #2 and #3 have also already been met.
   b) The HDMI receiver reads the embedded keys during authentication (after last byte of AKSV is written).

You *must* set PD# to 1 to perform the BIST command. Silicon Image recommends performing a software reset before performing the BIST command. The command can be executed multiple times by writing to the register as described above. A proper hardware reset must be performed after power on.

Auto Audio and Video Control

The SiI9013 HDMI receiver enhances control of the video and audio processing paths by providing an automatic mechanism for configuring those paths. Auto Audio Control (AAC) is used with the AEC registers, described on page 36. Auto Video Configuration (AVC) is used with register 0x60:0x5F, described on page 24.

Auto Control Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0xB5	AEC_CTRL	RSVDRW0		AAC_OE	RSVD0		AVC_EN	RSVDRW0	AAC_EN

Bit	Label	R/W	Description	Default
5	AAC_OE	R/W	AAC control of I^{2}S and S/PDIF output: 0 = AAC has no control of SD[3:0], SCK, or S/PDIF 1 = Enable AAC to control SD[3:0], SCK, and S/PDIF When enabled, AAC controls registers 0x68:0x27 and 0x68:0x29.	0
2	AVC_EN	R/W	0 = Disable AVC 1 = Enable AVC When this bit is set to 1, the read-back states of the following register fields are controlled by the AVC logic: 0x60:0x08[7:6,5:4] 0x60:0x48[2,1,0] 0x60:0x49[3,2] 0x60:0x4B[7:0] 0x60:0x4C[7:0] 0x60:0x4D[7:0] When this bit is set to 0, the read-back state of these registers is always the default or the value that was last written from the I^{2}C port. Setting AVC_EN to 1 does not affect the value in the registers after AVC_EN is later set to 0.	0
0	AAC_EN	R/W	0 = Disable AAC 1 = Enable AAC **Note**: This bit enables the AAC logic. This logic is reset in register 0x60:0x05 with AACRST[5] and not by SWRST[0] (see page 9).	0

Note: Bit 1 [RSVDRW0] must always be zero and never written to 1.

ECC Control Registers

ECC Control Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0xBB	ECC_CTRL	RSVDRW0							CAPCNT

Bit	Label	R/W	Description	Default
0	CAPCNT	R/W	Controls how BCH threshold errors (see register 0x60:0x71[2]) or T4 errors (see register 0x60:0x74[5] on page 29) are cleared: 0 = Continuously accumulate errors 1 = Clear error counters This bit should be written to 1 whenever audio processing is enabled in the HDMI receiver. This clears the error counters used within the AEC logic to flag audio packet reception errors before they overflow. The value for this bit becomes 0 automatically after clearing the counter.	0

ECC T4 Corrected Threshold Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0xBD	T4_THRES	RSVDRW0	T4_COR_THRES						

Bit	Label	R/W	Description	Default
6:0	T4_COR_THRES	R/W	Sets the threshold for TERC4 corrected errors.	0b000 0001

ECC T4 Uncorrected Threshold Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0xBE	T4_UNTHRES	RSVDRW0	T4_UNCOR_THRES						

Bit	Label	R/W	Description	Default
6:0	T4_UNCOR_ THRES	R/W	Sets the threshold for TERC4 uncorrected errors.	0b000 0001

AEC Exception Enable Registers

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0xB6	AEC_EN0	RSVD RW0	AEC06	AEC05	AEC04	AEC03	AEC02	AEC01	AEC00
0x60	0xB7	AEC_EN1	AEC15	AEC14	AEC13	AEC12	AEC11	AEC10	AEC09	AEC08
0x60	0xB8	AEC_EN2	RSVDRW0					AEC18	AEC17	AEC16

Bit	Label	R/W	Description	Interrupt Bit	Page	Default
7	RSVD	R/W	RESERVED.			0
6	AEC06	R/W	Exception #6: Sync Detect	INTR2[3]	27	0
5	AEC05	R/W	Exception #5: General Control Packet Set	INTR3[6]	28	0
4	AEC04	R/W	Exception #4: Video Clock Changed	INTR2[0]	27	0
3	AEC03	R/W	Exception #3: ACR CTS Changed	INTR1[7]		0
2	AEC02	R/W	Exception #2: ACR N Changed	INTR1[6]		0
1	AEC01	R/W	Exception #1: PLL Unlocked	INTR1[4]		0
0	AEC00	R/W	Exception #0: Cable Unplug **Note**: Cable unplug is detected only if the port is enabled.	INTR6[0]	31	0
7	AEC15	R/W	Exception #15: H Resolution Changed	INTR5[3]	31	0
6	AEC14	R/W	Exception #14: Sync Polarity Changed	INTR5[2]	31	0
5	AEC13	R/W	Exception #13: Interlace Changed	INTR5[1]	31	0
4	AEC12	R/W	Exception #12: Fs Changed	INTR5[0]	31	0
3	AEC11	R/W	Exception #11: CTS Reused	INTR4[2]	29	0
2	AEC10	R/W	Exception #10: Audio FIFO Overrun	INTR4[1]	29	0
1	AEC09	R/W	Exception #9: Audio FIFO Under-run	INTR4[0]	29	0
0	AEC08	R/W	Exception #8: HDMI Mode Change **Note**: Corresponds to the condition raised when the HDMI receiver switches in or out of HDMI mode.	See below.		0
2	AEC18	R/W	Exception #18: Fn Clock Changed	INTR5[7]	31	0
1	AEC17	R/W	Exception #17: Link Error	INTR5[5]	31	0
0	AEC16	R/W	Exception #16: V Resolution Changed	INTR5[4]	31	0

Each bit in the AEC_EN registers enables one condition to trigger the hardware soft mute. When a condition occurs, it sets the appropriate interrupt bit, except bit AEC08. The output of the interrupt register bit (or the internal condition) is then ANDed with the enable bit in AEC_EN. If hardware soft mute is enabled (MUTE_MODE – 0x68:0x29[5]) and the output of the AND is 1, hardware soft mute is triggered (see Figure 2). Un-mute is triggered by the firmware.
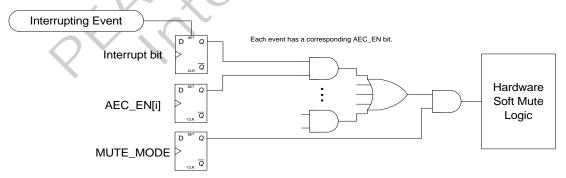

Figure 2. AEC Enable Control

HDCP Repeater Registers

The firmware uses these registers to obtain downstream information. Refer to page 17 for the SHA Control register (0x60:0x37).

Downstream BSTATUS Registers

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0xD5	DS_BSTAT1	DEVEXC	DEVICECNT						
0x60	0xD6	DS_BSTAT2	RSVDRW0			HDMI_MODE	CASEXC	DEPTH		

Bit	Label	R/W	Description	Default
7	DEVEXC	R/W	Maximum device count exceeded; more than 12 devices attached.	0
6:0	DEVICECNT	R/W	Number of devices attached downstream.	0
4	HDMI_MODE	R/W	0 = HDMI receiver is in DVI mode 1 = HDMI receiver is in HDMI mode	0
3	CASEXC	R/W	Maximum cascade depth exceeded.	0
2:0	DEPTH	R/W	Cascade depth.	0b000

Downstream M0 Registers

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0xD7	DS_M0_0								
0x60	0xD8	DS_M0_1								
0x60	0xD9	DS_M0_2								
0x60	0xDA	DS_M0_3				DS_M0				
0x60	0xDB	DS_M0_4								
0x60	0xDC	DS_M0_5								
0x60	0xDD	DS_M0_6								
0x60	0xDE	DS_M0_7								

Bit	Label	R/W	Description	Default
63:0	DS_M0	R/W	Downstream M0.	0

Downstream VH Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0xDF	DS_VH0_0								
0x60	0xE0	DS_VH0_1				DS_VH0				
0x60	0xE1	DS_VH0_2								
0x60	0xE2	DS_VH0_3								
0x60	0xE3	DS_VH1_0								
0x60	0xE4	DS_VH1_1				DS_VH1				
0x60	0xE5	DS_VH1_2								
0x60	0xE6	DS_VH1_3								
0x60	0xE7	DS_VH2_0								
0x60	0xE8	DS_VH2_1				DS_VH2				
0x60	0xE9	DS_VH2_2								
0x60	0xEA	DS_VH2_3								
0x60	0xEB	DS_VH3_0								
0x60	0xEC	DS_VH3_1				DS_VH3				
0x60	0xED	DS_VH3_2								
0x60	0xEE	DS_VH3_3								
0x60	0xEF	DS_VH4_0								
0x60	0xF0	DS_VH4_1				DS_VH4				
0x60	0xF1	DS_VH4_2								
0x60	0xF2	DS_VH4_3								
Bit	**Label**	**R/W**	**Description**							**Default**
31:0	DS_VH0	R/W	Downstream VH0.							0
31:0	DS_VH1	R/W	Downstream VH1.							0
31:0	DS_VH2	R/W	Downstream VH2.							0
31:0	DS_VH3	R/W	Downstream VH3.							0
31:0	DS_VH4	R/W	Downstream VH4.							0

Note: The values read back from these registers may not match the values written into them. When read, these registers return HDMI receiver status.

Sink-Accessible Registers (Device Address 0x68)

The state of the CI2CA pin selects between device address 0x68 and 0x6A for these registers (as described on page 1).

Audio Clock Recovery (ACR) Registers

The HDMI link does not transport an explicit audio master clock, but carries information describing the relationship of the audio sample rate to the pixel clock. The ratio of the current pixel clock frequency to the desired MCLK frequency is defined by a numerator, N, and a denominator, CTS. Whenever the pixel clock frequency changes (the video mode changes) or the audio clock changes (the audio sampling rate changes), the N and CTS values change accordingly.

ACR Control Register #1

Dev	Addr	Name		7	6	5	4	3	2	1	0
0x68	0x00	ACR_CTRL1		CTS_DROP_AUTO	POSTSEL	UPLLSEL	CTSSEL	NSEL	CTS_REUSED_AUTO	FSSEL	ACR_INIT

Bit	Label	R/W	Description	Default
7	CTS_DROP_AUTO	R/W	Enable automatic CTS drop: 0 = No ACR re-initialization is triggered if a CTS value is dropped 1 = If the CTS value is dropped because a new packet value overwrites a CTS value before it is used to generate an NCLK period, an ACR re-initialization is automatically triggered to realign the NCLK edge to the timing of the incoming ACR packets	0
6	POSTSEL	R/W	POST divider select: 0 = ACR uses hardware-determined POST divider value (POST_HVAL) 1 = ACR uses software-determined POST divider value (POST_SVAL)	0
5	UPLLSEL	R/W	Feedback divider UPLL select: 0 = ACR uses hardware-determined UPLL value (UPLL_HVAL) 1 = ACR uses software-determined UPLL value (UPLL_SVAL)	0
4	CTSSEL	R/W	CTS value select: 0 = ACR uses hardware-determined CTS value (CTS_HVAL) 1 = ACR uses software-determined CTS value (CTS_SVAL)	0
3	NSEL	R/W	N value select: 0 = ACR uses hardware-determined N value (N_HVAL) 1 = ACR uses software-determined N value (N_SVAL)	0
2	CTS_REUSED_AUTO	R/W	Enable automatic CTS reuse: 0 = No ACR re-initialization is triggered if a CTS value is reused 1 = If the CTS value is reused because a new packet value is not available when the previous NCLK period finishes, an ACR re-initialization is triggered automatically to realign the NCLK edge to the timing of the incoming ACR packets	0
1	FSSEL	R/W	Audio sample frequency select: 0 = ACR uses hardware-determined Fs value (CHST4[3:0]) extracted from HDMI audio packets 1 = ACR uses software Fs value (SW_FS on page 40) **Note**: This bit is useful only for diagnostics.	0
0	ACR_INIT	R/W	Generates a single-pixel-clock strobe that starts an ACR re-initialization to realign the NCLK edge to the timing of the incoming ACR packets. The NCLK is held LOW while the realignment occurs. NCLK Is an internal signal, $128*F_S/N$, generated from the pixel clock and the CTS value. Write 1 to this bit to generate the strobe. **Note**: The bit is automatically cleared back to 0.	0

ACR Audio Frequency Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x02	FREQ_SVAL	SWMCLKIN		SWMCLKOUT		SW_FS			

Bit	Label	R/W	Description	Default
7:6	SWMCLKIN	R/W	Audio MCLK input frequency mode software select: 0b00 = Fm is 128* Fs 0b01 = Fm is 256 * Fs 0b10 = Fm is 384 * Fs 0b11 = Fm is 512 * Fs **Important**: This field must always equal SWMCLKOUT.	0b01
5:4	SWMCLKOUT	R/W	Audio MCLK output frequency mode software select: 0b00 = Fm is 128* Fs 0b01 = Fm is 256 * Fs 0b10 = Fm is 384 * Fs 0b11 = Fm is 512 * Fs Used to determine the UPLL and POST divider values. **Important**: This field must always equal SWMCLKIN.	0b01
3:0	SW_FS	R/W	Audio sampling frequency (Fs) software select. These bits correspond to the channel status bits 27:24, where bit 24 is the LSB and 27 is the MSB. 0b0000 = Fs is 44.10 kHz 0b1000 = Fs is 88.20 kHz 0b1100 = Fs is 176.4 kHz 0b0010 = Fs is 48.0 kHz 0b1010 = Fs is 96.0 kHz 0b1110 = Fs is 192.0 kHz 0b0011 = Fs is 32.0 kHz This field is selected only if FSSEL is set to 1 in the ACR_CTRL1 register (0x68:0x00[1]). This field is useful only for diagnostics. Values not listed are reserved.	0b0010

ACR N Value Registers

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x03	N_SVAL1	N_SVAL[7:0]							
0x68	0x04	N_SVAL2	N_SVAL[15:8]							
0x68	0x05	N_SVAL3	RSVD0				N_SVAL[19:16]			
0x68	0x06	N_HVAL1	N_HVAL[7:0]							
0x68	0x07	N_HVAL2	N_HVAL[15:8]							
0x68	0x08	N_HVAL3	RSVD0				N_HVAL[19:16]			

Bit	Label	R/W	Description	Default
19:0	N_SVAL	R/W	N value for the audio clock regeneration method. This bit is set by software only if NSEL is set to 1 in the ACR_CTRL1 register (0x68:0x00[3]). It is useful for diagnostics only.	0
19:0	N_HVAL	R	The hardware value is received from the HDMI transmitter. Used only if NSEL is set to 0 in the ACR_CTRL1 register (0x68:0x00[3]).	0

ACR CTS Value Registers

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x09	CTS_SVAL1	CTS_SVAL[7:0]							
0x68	0x0A	CTS_SVAL2	CTS_SVAL[15:8]							
0x68	0x0B	CTS_SVAL3	RSVD0				CTS_SVAL[19:16]			
0x68	0x0C	CTS_HVAL1	CTS_HVAL[7:0]							
0x68	0x0D	CTS_HVAL2	CTS_HVAL[15:8]							
0x68	0x0E	CTS_HVAL3	RSVD0				CTS_HVAL[19:16]			

Bit	Label	R/W	Description	Default
19:0	CTS_SVAL	R/W	CTS value for the audio clock regeneration method. This bit is set by software only if CTSSEL is set to 1 in the ACR_CTRL1 register (0x68:0x00[4]). This bit is useful for diagnostics only.	0
19:0	CTS_HVAL	R	The hardware value is received from the HDMI transmitter. Used only if CTSSEL is set to 0 in the ACR_CTRL1 register (0x68:0x00[4]).	0x81000

ACR UPLL Value Registers

These registers are useful only for diagnostics.

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x0F	UPLL_SVAL	RSVD0	UPLL_SVAL						
0x68	0x10	UPLL_HVAL	RSVD0	UPLL_HVAL						

Bit	Label	R/W	Description	Default
6:0	UPLL_SVAL	R/W	The ACR PLL feedback value that determines, with N, the frequency of the PLL VCO. This bit is set by software only if UPLLSEL is set to 1 in the ACR_CTRL1 register (0x68:0x00[5]). This bit is useful for diagnostics only.	0
6:0	UPLL_HVAL	R	The hardware value is received from the HDMI transmitter. Used only if UPLLSEL is set to 0 in the ACR_CTRL1 register (0x68:0x00[5]).	0

ACR POST Value Registers

These registers are useful only for diagnostics.

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x11	POST_SVAL	RSVD0		POST_SVAL					
0x68	0x12	POST_HVAL	RSVD0		POST_HVAL					

Bit	Label	R/W	Description	Default
5:0	POST_SVAL	R/W	The ACR PLL feedback value that determines the frequency of MCLKOUT. This bit is set by software only if POSTSEL is set to 1 in the ACR_CTRL1 register (0x68:0x00[6]). This bit is useful for diagnostics only.	0
5:0	POST_HVAL	R	POST_HVAL is received from the HDMI transmitter. Used only if POSTSEL is set to 0 in the ACR_CTRL1 register (0x68:0x00[6]). The valid range is 0x02–0x3F. 0x01 is not a valid setting.	0

Table 5 shows the relationship of the UPLL and POST dividers to the ACR sample frequency Fs and intermediate frequency Fm.

Table 5: UPLL and POST Relationships to ACR

Fs	32.0 kHz		44.1 kHz		48.0 kHz		88.2 kHz		96.0 kHz		176.4 kHz		192.0 kHz	
	UPLL	POST	UPLL	POST	UPLL	POST	UPLL	POST	UPLL	POST	UPLL	POST	UPLL	POST
Fm = 128*Fs	72	24	48	12	48	12	24	6	24	6	12	4	12	4
Fm = 256*Fs	72	12	48	6	48	6	24	4	24	4	12	2	12	2
Fm = 384*Fs	72	8	48	4	48	4	24	2	24	2				
Fm = 512*Fs	72	6	48	4	48	4	24	2	24	2				

ACR PLL Lock Value Registers

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x13	LKWIN_SVAL	RSVD0			WINDIV				EXACT
0x68	0x14	LKTHRESH1	LKTHRESH[7:0]							
0x68	0x15	LKTHRESH2	LKTHRESH[15:8]							
0x68	0x16	LKTHRESH3	RSVDRW0				LKTHRESH[19:16]			

Bit	Label	R/W	Description	Default
4:1	WINDIV	R/W	When WIN_MODE is 0, the most recent count must be within prev_count +/− WINDIV of previous count for the stability counter to increment. When WIN_MODE is 1, the most recent count must be within $$\pm \frac{prev\_count}{2^{WINDIV}}$$ of previous count for the stability counter to increment: 0b0000 = window is +/− (previous count) 0b0001 = window is +/− (previous count) / 2 0b0010 = window is +/− (previous count) / 4 0b0011 = window is +/− (previous count) / 8 through 127 0b0111 = window is +/− (previous count) / 128, and so on. Silicon Image recommends leaving both WIN_MODE and WINDIV at the default values. WIN_MODE is described in the ACR_CTRL3 register on page 43.	0b0111
0	EXACT	R/W	0 = Range of stability is determined by WINDIV[4:1] 1 = Previous and current number of pixel clocks in a sampling period must match exactly to enable the stability duration counter to increment Silicon Image recommends leaving this bit at the default value.	1
19:0	LKTHRESH	R/W	PLL lock stability threshold. **Note**: When the internal stability counter exceeds the value in LKTHRESH, the ACR PLL is locked and the ACRPLLUL bit in the INTR1 register is not set again after it is cleared by the firmware. Silicon Image recommends setting LKTHRESH to 0x00020.	0

ACR Hardware Extracted Fs Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x17	PCLK_FS		RSVD0		FS_FEN		EXTRACTED_FS		

Bit	Label	R/W	Description	Default
4	FS_FEN	R/W	Fs filter enable: 0 = Update EXTRACTED_FS with any change from HDMI stream 1 = Update EXTRACTED_FS only if a new value for Fs is repeated on three consecutive frames	1
3:0	EXTRACTED_FS	R	Hardware extracted sampling frequency (Fs). This value is used by the HDMI receiver to reconstruct MCLK. These bits are extracted from channel status bits 27:24 in the HDMI audio packets and represent the Fs rate: 0b0000 = 44.1 kHz 0b1000 = 88.2 kHz 0b1100 = 176.4 kHz 0b0010 = 48 kHz 0b1010 = 96 kHz 0b1110 = 192 kHz 0b0011 = 32 kHz 0b0001 = Sample frequency not indicated These bits show the same value as AUD_FS in CHST4 (0x68:0x30[3:0]), described on page 50. Values not listed are reserved. The value for EXTRACTED_FS is written to the audio FIFO.	0b0000

ACR Control #3 Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x18	ACR_CTRL3	RSVDRW0		CTS_THRESH			MCLKLB	WIN_MODE	RSVDRW0

Bit	Label	R/W	Description	Default
6:3	CTS_THRESH	R/W	Threshold for CTS change: CTS must change by more than this value to update CTS_HVAL (0x68:0x0C–0E). The default is 1 so that any change in CTS is shown in CTS_HVAL.	0b0001
2	MCLKLB	R/W	MCLK loopback: 0 = Internal loopback disabled 1 = Internal loopback enabled **Important**: Silicon Image recommends leaving this bit at the default value.	1
1	WIN_MODE	R/W	Window detection of PLL unlocked state: 0 = Linear window mode 1 = Logarithmic window mode Silicon Image recommends leaving this bit at the default value.	0

ACR Configuration Registers

Note: These two registers are at device address 0x60, unlike the other ACR registers.

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x60	0x88	ACR_CFG1	ACR_CFG1							
0x60	0x89	ACR_CFG2	ACR_CFG2							

Bit	Label	R/W	Description	Default
7:0	ACR_CFG1	R/W	ACR PLL Configuration Byte #1. This bit should be written to 0x88 after each hardware reset.	0x00
7:0	ACR_CFG2	R/W	ACR PLL Configuration Byte #2. This bit should be written to 0x16 after each hardware reset.	0x00

Audio Output Formatting Registers

Audio Output I^{2}S Control Register #1

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x26	I2S_CTRL1	INV_EN	SCK	SIZE	MSB	WS	JUST	DIR	SHIFT1

Bit	Label	R/W	Description	Default
7	INV_EN	R/W	Send invalid data: 0 = Send only valid data 1 = Send all data, even invalid, according to the limits set by the AUD_LENGTH_MAX and AUD_LENGTH fields extracted from S/PDIF	0
6	SCK	R/W	Sample clock edge: 0 = Sample edge is rising (positive) 1 = Sample edge is falling (negative) **Note**: This bit defines the edge on which the WS and SDx data is sampled coming out of the HDMI receiver. The downstream chip should use the opposite SCK edge to sample the data arriving at its input pins.	1
5	SIZE	R/W	Word Size: 0 = 32 bits 1 = 16 bits	0
4	MSB	R/W	Most-Significant Bit Sign-Extended: 0 = Enabled 1 = Disabled	0
3	WS	R/W	Word Select left/right polarity: 0 = Left polarity when Word Select is LOW 1 = Left polarity when Word Select is HIGH	0
2	JUST	R/W	SD Justification: 0 = Data is left justified 1 = Data is right justified	0
1	DIR	R/W	SD data direction: 0 = Most-Significant Bit (MSB) first 1 = Least-Significant Bit (LSB) first	0
0	SHIFT1	R/W	WS to SD Shift First Bit: 0 = First Bit Shift (Philips Spec) 1 = No Shift	0

Audio Output I^{2}S Control Register #2

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x27	I2S_CTRL2	SD3	SD2	SD1	SD0	MCLKEN	RSVD0	VUCP	PCM

Bit	Label	R/W	Description		Default
7	SD3	R/W	SD3 Output Control	I^{2}S channel output control:	0
6	SD2	R/W	SD2 Output Control	0 = Channel disabled (always output LOW) (not tri-stated)	0
5	SD1	R/W	SD1 Output Control		0
4	SD0	R/W	SD0 Output Control	1 = Channel enabled	0
3	MCLKEN	R/W	MCLK enable: 0 = Tri-state MCLKOUT 1 = Enable MCLKOUT		0
1	VUCP	R/W	Send VUCP bits: 0 = Send only 24 real data bits through I^{2}S 1 = Send 28 bits of data with VUCP bits **Note**: VUCP are bits in the S/PDIF stream. Refer to details in the IEC-60958 Specification.		0
0	PCM	R/W	PCM only — I^{2}S data pass select: 0 = Pass whatever data is in the S/PDIF packets 1 = Pass only data from S/PDIF packets that are recognized as PCM data (when non-PCM data detected, send 0 data)		1

Audio Output I^{2}S Map Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x28	I2S_MAP	SD3		SD2		SD1		SD0	

Bit	Label	R/W	Description		Default
7:6	SD3	R/W	SD3 Map	For each 2-bit field, select one of four I^{2}S FIFO streams to be output on SD3, SD2, SD1, or SD0 output pin:	0b11
5:4	SD2	R/W	SD2 Map	0b00 = Select stream #0	0b10
3:2	SD1	R/W	SD1 Map	0b01 = Select stream #1	0b01
1:0	SD0	R/W	SD0 Map	0b10 = Select stream #2 0b11 = Select stream #3 By default, each stream is mapped to the corresponding SD[3:0] output.	0b00

Audio Output Control Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x29	AUD_CTRL	LENOV	RSVD RW	MUTE_ MODE	PSERR	PAERR	I2S MODE	SPMODE	SPEN

Bit	Label	R/W	Description	Default
7	LENOV	R/W	Enable overwrite of the audio sample length for the I^{2}S data: 0 = Take from the HDMI packet 1 = Take from the AUDO_MUTE register (0x68:0x32[7:4]), described on page 51	0
5	MUTE_MODE	R/W	Audio hardware mute mode: 0 = Repeat last sample when mute is triggered 1 = Ramp audio down (soft mute) when mute is triggered; ramp audio up (soft un-mute) when AUDM (0x68:37[1]) or CH3_MU – CH0_MU (0x68:0x32[3:0]) is cleared. **Note**: Soft mute works only for PCM audio. If the chip detects compressed audio by checking the channel status bits, it mutes the output on the selected triggering conditions.	0
4	PSERR	R/W	Pass S/PDIF error: 0 = Do not pass S/PDIF type of errors; conceal errors by repeating last good sample (see note below) 1 = Pass all audio data, regardless of errors	1
3	PAERR	R/W	Pass audio error: 0 = Do not pass errors; conceal by repeating last sample 1 = Pass all audio data, regardless of errors	1
2	I2SMODE	R/W	I^{2}S output: 0 = All I^{2}S outputs are grounded (SD[3:0], SCK, WS) (not tri-stated) 1 = SCK and WS toggle; SD is on or off depending on the value for SD0 in the I2S_CTRL2 register (0x68:0x27[4])	0
1	SPMODE	R/W	S/PDIF output grounding enabled: 0 = S/PDIF output always produces valid bi-phase mark encoded data, even during a *no input* condition 1 = S/PDIF output is zero (grounded) if no input is detected	0
0	SPEN	R/W	S/PDIF output enable: 0 = Disabled (output set as if *no input* according to SPMODE) (not tri-stated) 1 = Enabled	0

S/PDIF errors may come from parity errors (indicated by SPDIFERR in the INTR3 register) or from a mismatch in the VUC bits between left and right sub-frames. This register should be written to 0x15 after RESET to enable muting of I^{2}S on audio packet ECC errors.

Mute may be triggered by an AEC condition (described on page 36) or manually in register 0x68:0x32 and 0x68:0x37 (described on page 51 and 52, respectively).

Note: Channel status bits (registers 0x2A, 0x2B, 0x2C, 0x30, and 0x31) are extracted from the HDMI audio packets. The data in these registers is not accurate if audio is disabled by setting AUDM (0x68:0x37[1]) to 1 or MCLKEN (0x68:0x27[3]) to 0.

Audio Input Channel Status #1 Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x2A	CHST1	MODE0		PREEMPHASIS			SW_COPYRIGHT	AUD_SAMPLE	APP_TYPE

Bit	Label	R/W	Description	Default
7:6	MODE0	R	0b00 = Mode 0	0b00
5:3	PREEMPHASIS	R	0b000 = 2 audio channels without pre-emphasis	0b000
			0b001 = 2 audio channels with 50/15-μs pre-emphasis (see IEC-60958-3 Section 4.2.1)	
2	SW_COPYRIGHT	R	0 = Software for which copyright is asserted	0
			1 = Software for which no copyright is asserted	
1	AUD_SAMPLE	R	0 = Audio sample word represents linear PCM samples	0
			1 = Audio sample word used for other purposes	
0	APP_TYPE	R	0 = Consumer application	0
			1 = Professional application	

Audio Input S/PDIF Channel Status #2 Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x2B	CHST2	CAT_CODE							

Bit	Label	R/W	Description	Default
7:0	CAT_CODE	R	Category code (corresponds to channel status bits 15:8).	0

Audio Input S/PDIF Channel Status #3 Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x2C	CHST3	CHAN_NUM				SOURCE_NUM			

Bit	Label	R/W	Description	Default
7:4	CHAN_NUM	R	Channel number (corresponds to channel status bits 23:20).	0
3:0	SOURCE_NUM	R	Source number (corresponds to channel status bits 19:16).	0

See page 50 for CHST4 and CHST5 bytes.

Audio Swap and Overwrite Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x2E	SW_OW	SW3	SW2	SW1	SW0	RSVDRW	OW_B2	RSVDRW	OW_CHEN

Bit	Label	R/W	Description	Default
7	SW3	R/W	Swap left/right on I²S Channel 3: 0 = No swap 1 = Swap left and right channels on I²S Channel 3	0
6	SW2	R/W	Swap left/right on I²S Channel 2: 0 = No swap 1 = Swap left and right channels on I²S Channel 2	0
5	SW1	R/W	Swap left/right on I²S Channel 1: 0 = No swap 1 = Swap left and right channels on I²S Channel 1	0
4	SW0	R/W	Swap left/right on I²S Channel 0: 0 = No swap 1 = Swap left and right channels on I²S Channel 0	0
2	OW_B2	R/W	Channel status bit 2 overwrite data: This bit value is used in the CHST1 register (0x68:0x2A), described on page 48, when OW_CHEN [0] is set to 1.	0
0	OW_CHEN	R/W	Channel status overwrite enable: 0 = OW_B2 and CHST2 (0x68:0x2B) have no effect 1 = Channel status bits 2 and 15:8 are overwritten with the values in OW_B2 and CHST2	0

Audio CHST5 Overwrite Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x2F	OW_CHST5	OW15	OW14	OW13	OW12	OW11	OW10	OW09	OW08

Bit	Label	R/W	Description	Default
7:0	OW_CHST5	R/W	Channel status byte 5 overwrite. When OW_CHEN is set to 1 in register 0x2E, this bit is substituted for any CHST2 bits received in audio packets. Bit OW15 corresponds to channel status bit 15, and so on.	0x00

Audio Input S/PDIF Channel Status #4 Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x30	CHST4	RSVD0		AUD_ACCUR		AUD_FS			

Bit	Label	R/W	Description	Default
5:4	AUD_ACCUR	R	Clock accuracy (corresponds to channel status bits 29:28). These two bits define the sampling frequency tolerance. The bits are set in the HDMI transmitter. Refer to IEC-60958-3.	0
3:0	AUD_FS	R	Sampling frequency (channel status bits 27:24). Represents the Fs rate: 0b0000 = 44.1 kHz 0b0001 = Not Indicated 0b0010 = 48 kHz 0b0011 = 32 kHz 0b1000 = 88.2 kHz 0b1010 = 96 kHz 0b1100 = 176.4 kHz 0b1110 = 192 kHz These bits show the same value as EXTRACTED_FS in register 0x68:0x17[3:0], described on page 43. Values not listed are reserved. The value for EXTRACTED_FS is written to the audio FIFO and the value for AUD_FS is read from the audio FIFO.	0b0000

Audio Input S/PDIF Channel Status #5 Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x31	CHST5	RSVD0				AUD_LENGTH			AUD_MX

Bit	Label	R/W	Description		Default
3:1	AUD_LENGTH	R	Audio length (channel status bits 35:33): **AUD_MX=0**	**AUD_MX=1**	0b000
			0b000 = 20 (Max)	0b000 = 24 (Max)	
			0b001 = 16 bits	0b001 = 20 bits	
			0b010 = 18 bits	0b010 = 22 bits	
			0b100 = 19 bits	0b100 = 23 bits	
			0b101 = 20 bits	0b101 = 24 bits	
			0b110 = 17 bits	0b110 = 21 bits	
0	AUD_MX	R	Audio length max (channel status bit 32): 0 = Maximum sample word length is 20 bits 1 = Maximum sample word length is 24 bits		0

The audio length extracted from the HDMI audio packets may be overridden with the value in register AUDO_MUTE (0x68:0x32), described on page 51, when the LENOV bit is set in register AUD_CTRL (0x68:0x29), described on page 47.

Audio Output Channel Mute Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x32	AUDO_MUTE	LEN_OVERRIDE				CH3_MU	CH2_MU	CH1_MU	CH0_MU

Bit	Label	R/W	Description	Default
7:4	LEN_OVERRIDE	R/W	Audio sample length override. When LENOV is set to 1 in the AUD_CTRL register (described on page 47), the LEN_OVERRIDE value is used to set the sample length for I²S output instead of the length extracted from audio sample (channel status bits [35:33], reflected in CHST5).	0b0000
3	CH3_MU	R/W	Channel 3 mute: 0 = Unmute 1 = Mute	0
2	CH2_MU	R/W	Channel 2 mute: 0 = Unmute 1 = Mute	0
1	CH1_MU	R/W	Channel 1 mute: 0 = Unmute 1 = Mute	0
0	CH0_MU	R/W	Channel 0 mute: 0 = Unmute 1 = Mute	0

Unmute unused I²S output channels by setting the bits in the AUDO_MUTE register.

The relationship between SIZE in the I2S_CTRL1 register (0x68:0x26) and LEN_OVERRIDE in the AUDO_MUTE register is as follows:

- SIZE=16 (for 16-bit input DACs):
- I²S output contains 16 SCK each half WS period.
- Use high-order 16 bits of audio sample data from the HDMI packet.
- LENOV in the AUD_CTRL register (0x68:0x29) and LEN_OVERRIDE in the AUD_CTRL register are ignored.
- SIZE=32 & LENOV=0:
- I²S output contains 32 SCK each half WS period.
- Use all 32 bits of audio sample data from the HDMI packet.
- LEN_OVERRIDE is ignored.
- SIZE=32 & LENOV=1:
- I²S output contains 32 SCK each half WS period.
- Use from 16 to 24 high-order bits of audio sample data from the HDMI packet depending on LEN_OVERRIDE.

Note: WS is Word Select, as defined in the *Phillips Semiconductor I²S Bus* Specification.

HDMI Control and Status Registers

HDMI Status Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x34	HDMI_STAT	RSVD0				HDMI_LO	MUTE_STAT	MODE_EN	HDMI_DET
Bit	**Label**	**R/W**	**Description**							**Default**
3	HDMI_LO	R	HDMI audio packet layout indicator: 0 = Layout 0 (2 channels) 1 = Layout 1 (up to 8 channels)							0
2	MUTE_STAT	R	AV mute status.							0
1	MODE_EN	R	HDMI mode enabled: 0 = Disabled 1 = Enabled This bit is used to determine if incoming data is HDMI or DVI.							0
0	HDMI_DET	R	HDMI mode detected.							0

HDMI Mute Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x37	HDMI_MUTE	RSVD0					MUTE_POL	AUDM	VIDM
Bit	**Label**	**R/W**	**Description**							**Default**
2	MUTE_POL	R/W	MUTE_OUT polarity: 0 = Positive 1 = Negative **Note**: AUTO_SWRST resets the AAC block and may cause MUTE_OUT not to be asserted.							0
1	AUDM	R/W	Audio mute (repeat last good sample): 0 = Send normal audio data 1 = Initiate mute or un-mute process							0
0	VIDM	R/W	Video mute (send blanking value to output): 0 = Send normal video data 1 = Send values from VID_BLANK1, VID_BLANK2, and VID_BLANK3 (described on page 23)							0

HDMI FIFO Read/Write Pointer Difference Register

This register is provided for diagnostic use only and is not supported for general use.

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x39	FIFO_PTRDIFF	RSVD0	FIFO_PTRDIFF						
Bit	**Label**	**R/W**	**Description**							**Default**
6:0	FIFO_PTRDIFF	R/W	HDMI FIFO Read/Write pointer difference.							0x00

System Power Down Registers

Power Down Total Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x3C	PD_TOT	RSVDRW0							PDTOT#

Bit	Label	R/W	Description	Default
0	PDTOT#	R/W	Power down total: 0 = Power down everything with no exceptions; terminations to both TMDS cores are disconnected when PDTOT# = 0 1 = Normal operation	1

System Power Down #2 Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x3E	PD_SYS2	PD_PCLK#	PD_MCLK#	RSVDR0	PD_TERM#	PD_QO#	PD_QE#	PD_VHDE#	PD_ODCK#

Bit	Label	R/W	Description		Default
7	PD_PCLK#	R/W	Power down pixel clock tree.		1
6	PD_MCLK#	R/W	Power down MCLK clock tree.	0 = Power down 1 = Enable	1
4	PD_TERM#	R/W	Power down TMDS port termination. The 50Ω termination for the TMDS core is disconnected.		1
3	PD_QO#	R/W	Tri-State QO[23:0]. This bit defaults to 0 after reset to support 24-bit output mode. Set to 1 to support 48-bit output mode. This signal is also powered down with PD_VO.		0
2	PD_QE#	R/W	Tri-State QE[23:0]. This signal is also powered down with PD_VO.		1
1	PD_VHDE#	R/W	Tri-State VSYNC, HSYNC, and DE. This signal is also powered down with PD_VO.		1
0	PD_ODCK#	R/W	Tri-State ODCK This signal is also powered down with PD_VO.		1

System Power Down Register

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x3F	PD_SYS	PD_AO#	PD_VO#	PD_APLL#	RSVDR0	PD_12CH#	PD_FULL#	PD_OSC#	PD_XTAL#

Bit	Label	R/W	Description		Default
7	PD_AO#	R/W	Tri-state audio output. This bit tri-states the SD[3:0], WS, SCK, and S/PDIF outputs.	0 = Power down 1 = Enable	1
6	PD_VO#	R/W	Tri-state video output. This bit tri-states the ODCK, DE, HSYNC, VSYNC, QE[23:0], and QO[23:0] outputs.		1
5	PD_APLL#	R/W	Power down audio PLL.		1
3	PD_12CH#	R/W	Power down TMDS core — CKDT remains enabled. This bit powers down the TMDS core, except for the CKDT circuitry used to detect new active input clock.		1
2	PD_FULL#	R/W	Power down TMDS core fully — CKDT is disabled. This bit powers down the selected TMDS core completely for the lowest power in that core.		1
1	PD_OSC#	R/W	Power down internal oscillator.		1
0	PD_XTAL#	R/W	Power down crystal input and audio PLL.		1

The values of other registers are not affected by assertion of these power-down bits or the general PD# bit (see page 11).

Packet Registers

Refer to the HDMI and CEA-861B specifications for more details on these register fields.

HDMI Packet Types for packets carrying InfoFrames have the most-significant bit of the InfoFrame TYPE field set to 1. The lower 7 bits indicate the InfoFrame Type as defined by CEA-861B. Therefore, the PACKET_TYPE field should be calculated as 0x080 + *CEA-861B InfoFrame Type*. Refer to the HDMI Specification for more information.

HDMI includes a checksum byte in each InfoFrame. This byte is not included in the EIA/CEA-861B definitions of InfoFrames. The added checksum byte increases the size of the InfoFrame by one, but does not affect the xxx_LEN value listed in CEA-861B, which indicates the number of actual data bytes in the InfoFrame.

The SiI9013 HDMI receiver automatically detects and stores the InfoFrames and packets defined in the HDMI Specification. InfoFrames or packets that do not match any TYPE in the HDMI Specification or with values other than those set in the Packet Type Decode registers (0x60:0xBF, 0x7F, and 0xFF) are stored in the Unrecognized Packet registers. A bit in the INTR3 register (see page 28) is set whenever a new InfoFrame or packet is detected or whenever an InfoFrame or packet is stored in the Unrecognized Packet buffer.

Note: The NEW_GCP bit is set on every arriving General Control Packet, regardless of whether the content of the General Control Packet has changed.

The version and length fields for each InfoFrame should be ignored by the HDMI Sink. Future enhancements to the HDMI standard may change version or length, or both for any of these InfoFrames. Fields defined in HDMI 1.0 can be parsed from future versions using the same parsing algorithms so that, regardless of the version or length values, the fields can be found correctly.

AVI InfoFrame Registers

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x40	AVI_TYPE	AVI_HDR[7:0]							
0x68	0x41	AVI_VERS	AVI_HDR[15:8]							
0x68	0x42	AVI_LEN	AVI_HDR[23:16]							
0x68	0x43	AVI_CHSUM	AVI_DATA							
0x68	0x44	AVI_DBYTE1								
0x68	0x45	AVI_DBYTE2								
0x68	0x46	AVI_DBYTE3								
0x68	0x47	AVI_DBYTE4								
0x68	0x48	AVI_DBYTE5								
0x68	0x49	AVI_DBYTE6								
0x68	0x4A	AVI_DBYTE7								
0x68	0x4B	AVI_DBYTE8								
0x68	0x4C	AVI_DBYTE9								
0x68	0x4D	AVI_DBYTE10								
0x68	0x4E	AVI_DBYTE11								
0x68	0x4F	AVI_DBYTE12								
0x68	0x50	AVI_DBYTE13								
0x68	0x51	AVI_DBYTE14								
0x68	0x52	AVI_DBYTE15								

Bit	Label	R/W	Description	Default	Expected
7:0	AVI_TYPE	R	AVI InfoFrame Packet Type Code.	0x00	0x82
7:0	AVI_VERS	R	AVI InfoFrame Packet Version Code.	0x00	0x02
7:0	AVI_LEN	R	AVI InfoFrame Packet Length.	0x00	0x0D
7:0	AVI_CHSUM	R	AVI InfoFrame Packet Checksum.	0x00	
	AVI_DATA	R	AVI InfoFrame Packet Data Bytes.	0	

The HDMI Specification defines AVI_TYPE to be 0x82 and the AVI_VERS to be 0x02. Other values are from HDMI Table 8-1. Data bytes 14 and 15 are available in the HDMI receiver, but are not specified in the CEA-861B definition of the AVI InfoFrame. The AVI_LEN field indicates the CEA-861B data payload length of 13 bytes (0x0D). The checksum value must be calculated by firmware and written into AVI_CHSUM.

SPD InfoFrame Registers

Refer to the CEA-861B Specification for more details on these register fields.

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x60	SPD_TYPE	SPD_HDR[7:0]							
0x68	0x61	SPD_VERS	SPD_HDR[15:8]							
0x68	0x62	SPD_LEN	SPD_HDR[23:16]							
0x68	0x63	SPD_CHSUM	SPD_HDR[31:24]							
0x68	0x64	SPD_DBYTE1	SPD_DATA							
0x68	0x65	SPD_DBYTE2								
0x68	0x66	SPD_DBYTE3								
0x68	0x67	SPD_DBYTE4								
0x68	0x68	SPD_DBYTE5								
0x68	0x69	SPD_DBYTE6								
0x68	0x6A	SPD_DBYTE7								
0x68	0x6B	SPD_DBYTE8								
0x68	0x6C	SPD_DBYTE9								
0x68	0x6D	SPD_DBYTE10								
0x68	0x6E	SPD_DBYTE11								
0x68	0x6F	SPD_DBYTE12								
0x68	0x70	SPD_DBYTE13								
0x68	0x71	SPD_DBYTE14								
0x68	0x72	SPD_DBYTE15								
0x68	0x73	SPD_DBYTE16								
0x68	0x74	SPD_DBYTE17								
0x68	0x75	SPD_DBYTE18								
0x68	0x76	SPD_DBYTE19								
0x68	0x77	SPD_DBYTE20								
0x68	0x78	SPD_DBYTE21								
0x68	0x79	SPD_DBYTE22								
0x68	0x7A	SPD_DBYTE23								
0x68	0x7B	SPD_DBYTE24								
0x68	0x7C	SPD_DBYTE25								
0x68	0x7D	SPD_DBYTE26								
0x68	0x7E	SPD_DBYTE27								

Bit	Label	R/W	Description	Default	Expected
7:0	SPD_TYPE	R	SPD InfoFrame Type Code.	0x00	0x83
7:0	SPD_VERS	R	SPD InfoFrame Version Code.	0x00	0x01
7:0	SPD_LEN	R	SPD InfoFrame Length.	0x00	0x19
7:0	SPD_CHSUM	R	SPD InfoFrame Checksum.	0x00	
	SPD_DATA	R	SPD InfoFrame Data Bytes.	0	

The HDMI Specification defines SPD_TYPE to be 0x83 and the SPD_VERS to be 0x01. Other values are from CEA-861B Table 16. Data bytes 26 and 27 are available in the SiI9013 HDMI receiver, but are not specified in the CEA-861B definition of the SPD InfoFrame. The SPD_LEN field indicates the CEA-861B data payload length of 25 bytes (0x19). The checksum value must be calculated by firmware and written into SPD_CHSUM.

Note: You can repurpose the SPD InfoFrame registers by programming a different value into the SPD_DEC register (0x68:0x7F). It is common to alternate between SPD InfoFrames and ACP or ISRC1/2 packets. Refer to the HDMI Specification for details on ACP and ISRC1/2 packets.

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Audio InfoFrame Registers

Refer to the HDMI Specification for more details on these register fields.

Note: The definitions of the Audio InfoFrame are not identical in the CEA-861B and HDMI specifications. The information shown on this page is for HDMI 1.0, which modifies the Type Code (AUDIO_TYPE) to be 0x84 instead of the CEA-861B 0x04, and inserts a checksum byte (AUDIO_CHSUM) between the length and the data bytes. There is no checksum byte in the CEA-861B version. Also, the checksum byte is not included in the length value, so the overall payload is 11 bytes, of which 10 are data (0x84 through 0x8D).

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0x80	AUDIO_TYPE	AUDIO_HDR[7:0]							
0x68	0x81	AUDIO_VERS	AUDIO_HDR[15:8]							
0x68	0x82	AUDIO_LEN	AUDIO_HDR[23:16]							
0x68	0x83	AUDIO_CHSUM	AUDIO_HDR[31:24]							
0x68	0x84	AUDIO_DBYTE1	AUDIO_DATA							
0x68	0x85	AUDIO_DBYTE2								
0x68	0x86	AUDIO_DBYTE3								
0x68	0x87	AUDIO_DBYTE4								
0x68	0x88	AUDIO_DBYTE5								
0x68	0x89	AUDIO_DBYTE6								
0x68	0x8A	AUDIO_DBYTE7								
0x68	0x8B	AUDIO_DBYTE8								
0x68	0x8C	AUDIO_DBYTE9								
0x68	0x8D	AUDIO_DBYTE10								

Bit	Label	R/W	Description	Default	Expected
7:0	AUDIO_TYPE	R	Audio InfoFrame Type Code.	0x00	0x84
7:0	AUDIO_VERS	R	Audio InfoFrame Version Code.	0x00	0x01
7:0	AUDIO_LEN	R	Audio InfoFrame Length.	0x00	0x0A
7:0	AUDIO_CHSUM	R	Audio InfoFrame Checksum.	0x00	
	AUDIO_DATA	R	Audio InfoFrame Data Bytes.	0	

The HDMI Specification defines AUD_TYPE to be 0x84 and AUD_VERS to be 0x01. Other values are from HDMI Table 8-4. The checksum value must be calculated by the firmware and written into AUDIO_CHSUM.

MPEG InfoFrame Registers

Refer to the CEA-861B Specification and the HDMI Specification for more details on these register fields.

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0xA0	MPEG_TYPE	MPEG_HDR[7:0]							
0x68	0xA1	MPEG_VERS	MPEG_HDR[15:8]							
0x68	0xA2	MPEG_LEN	MPEG_HDR[23:16]							
0x68	0xA3	MPEG_CHSUM	MPEG_HDR[31:24]							
0x68	0xA4	MPEG_DBYTE1	MPEG_DATA							
0x68	0xA5	MPEG_DBYTE2								
0x68	0xA6	MPEG_DBYTE3								
0x68	0xA7	MPEG_DBYTE4								
0x68	0xA8	MPEG_DBYTE5								
0x68	0xA9	MPEG_DBYTE6								
0x68	0xAA	MPEG_DBYTE7								
0x68	0xAB	MPEG_DBYTE8								
0x68	0xAC	MPEG_DBYTE9								
0x68	0xAD	MPEG_DBYTE10								
0x68	0xAE	MPEG_DBYTE11								
0x68	0xAF	MPEG_DBYTE12								
0x68	0xB0	MPEG_DBYTE13								
0x68	0xB1	MPEG_DBYTE14								
0x68	0xB2	MPEG_DBYTE15								
0x68	0xB3	MPEG_DBYTE16								
0x68	0xB4	MPEG_DBYTE17								
0x68	0xB5	MPEG_DBYTE18								
0x68	0xB6	MPEG_DBYTE19								
0x68	0xB7	MPEG_DBYTE20								
0x68	0xB8	MPEG_DBYTE21								
0x68	0xB9	MPEG_DBYTE22								
0x68	0xBA	MPEG_DBYTE23								
0x68	0xBB	MPEG_DBYTE24								
0x68	0xBC	MPEG_DBYTE25								
0x68	0xBD	MPEG_DBYTE26								
0x68	0xBE	MPEG_DBYTE27								

Bit	Label	R/W	Description	Default	Expected
7:0	MPEG_TYPE	R	MPEG InfoFrame Type Code.	0x00	0x85
7:0	MPEG_VERS	R	MPEG InfoFrame Version Code.	0x00	0x01
7:0	MPEG_LEN	R	MPEG InfoFrame Length.	0x00	0x0A
7:0	MPEG_CHSUM	R	MPEG InfoFrame Checksum.	0x00	
	MPEG_DATA	R	MPEG InfoFrame Data Bytes.	0	

The HDMI Specification defines MPEG_TYPE to be 0x85 and MPEG_VERS to be 0x01. Other values are from CEA-861B Table 25. The checksum value must be calculated by the firmware and written into MPEG_CHSUM.

Note: You can repurpose the MPEG InfoFrame registers by programming a different value into the MPEG_DEC register (0x68:0xBF). It is common to alternate between MPEG InfoFrames and ACP or ISR1/2 packets. Refer to the HDMI Specification for details on ACP and ISR1/2 packets.

Audio Control Packet Registers

Refer to the HDMI Specification for more details on these register fields.

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0xE0	ACP_HB0	ACP_HDR[7:0]							
0x68	0xE1	ACP_HB1	ACP_HDR[15:8]							
0x68	0xE2	ACP_HB2	ACP_HDR[23:16]							
0x68	0xE3	ACP_DBYTE0	ACP_DATA							
0x68	0xE4	ACP_DBYTE1								
0x68	0xE5	ACP_DBYTE2								
0x68	0xE6	ACP_DBYTE3								
0x68	0xE7	ACP_DBYTE4								
0x68	0xE8	ACP_DBYTE5								
0x68	0xE9	ACP_DBYTE6								
0x68	0xEA	ACP_DBYTE7								
0x68	0xEB	ACP_DBYTE8								
0x68	0xEC	ACP_DBYTE9								
0x68	0xED	ACP_DBYTE10								
0x68	0xEE	ACP_DBYTE11								
0x68	0xEF	ACP_DBYTE12								
0x68	0xF0	ACP_DBYTE13								
0x68	0xF1	ACP_DBYTE14								
0x68	0xF2	ACP_DBYTE15								
0x68	0xF3	ACP_DBYTE16								
0x68	0xF4	ACP_DBYTE17								
0x68	0xF5	ACP_DBYTE18								
0x68	0xF6	ACP_DBYTE19								
0x68	0xF7	ACP_DBYTE20								
0x68	0xF8	ACP_DBYTE21								
0x68	0xF9	ACP_DBYTE22								
0x68	0xFA	ACP_DBYTE23								
0x68	0xFB	ACP_DBYTE24								
0x68	0xFC	ACP_DBYTE25								
0x68	0xFD	ACP_DBYTE26								
0x68	0xFE	ACP_DBYTE27								

Bit	Label	R/W	Description	Default	Expected
7:0	ACP_HB0	R	ACP Packet Header Byte 0.	0x00	0x04
7:0	ACP_HB1	R	ACP Packet Header Byte 1.	0x00	
7:0	ACP_HB2	R	ACP Packet Header Byte 2.	0x00	
	ACP_DATA	R	ACP Packet Data Bytes.	0	

Note: You can repurpose the ACP packet registers by programming a different value into the ACP_DEC register (0x68:0x0FF). It is common to use the ACP registers for ISRC1/2 packets. Refer to the HDMI Specification for details on ACP and ISR1/2 packets.

Unrecognized Packet Registers

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0xC0	UNR_DBYTE1								
0x68	0xC1	UNR_DBYTE2								
0x68	0xC2	UNR_DBYTE3								
0x68	0xC3	UNR_DBYTE4								
0x68	0xC4	UNR_DBYTE5								
0x68	0xC5	UNR_DBYTE6								
0x68	0xC6	UNR_DBYTE7								
0x68	0xC7	UNR_DBYTE8								
0x68	0xC8	UNR_DBYTE9								
0x68	0xC9	UNR_DBYTE10								
0x68	0xCA	UNR_DBYTE11								
0x68	0xCB	UNR_DBYTE12								
0x68	0xCC	UNR_DBYTE13								
0x68	0xCD	UNR_DBYTE14								
0x68	0xCE	UNR_DBYTE15								
0x68	0xCF	UNR_DBYTE16				UNR_DATA				
0x68	0xD0	UNR_DBYTE17								
0x68	0xD1	UNR_DBYTE18								
0x68	0xD2	UNR_DBYTE19								
0x68	0xD3	UNR_DBYTE20								
0x68	0xD4	UNR_DBYTE21								
0x68	0xD5	UNR_DBYTE22								
0x68	0xD6	UNR_DBYTE23								
0x68	0xD7	UNR_DBYTE24								
0x68	0xD8	UNR_DBYTE25								
0x68	0xD9	UNR_DBYTE26								
0x68	0xDA	UNR_DBYTE27								
0x68	0xDB	UNR_DBYTE28								
0x68	0xDC	UNR_DBYTE29								
0x68	0xDD	UNR_DBYTE30								
0x68	0xDE	UNR_DBYTE31								

Bit	Label	R/W	Description	Default
	UNR_DATA	R	Unrecognized Packet Data Bytes.	0

The SiI9013 HDMI receiver recognizes the following InfoFrame and packet types:

    0x01   Audio Clock Regeneration (N/CTS) Packet
    0x02   Audio Sample Packet
    0x03   General Control Packet
    0x82   AVI InfoFrame
    0x83   Source Product Descriptor InfoFrame
    0x84   Audio InfoFrame
    0x85   MPEG Source InfoFrame
    0x04   Audio Content Protection (ACP) Packet
    0x05   ISRC1 Packet
    0x06   ISRC2 Packet

All InfoFrames and packets received with types not listed above or with values other than those set in the Packet Type Decode registers (0x60:0xBF, 0x7F, and 0xFF) are stored in the Unrecognized Packet registers. If the content differs from the previous unrecognized packet, the interrupt bit NEW_UNR in the INTR3 register (0x60:0x73[4]) is set (see page 28).

General Control Packet Register

Refer to the HDMI Specification for more details on the use of the General Control Packet for muting audio and video. HDMI does not allow the SET_AVMUTE and CLR_AVMUTE bits to have the same value at the same time.

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0xDF	GCP_DBYTE1	RSVD0			CLR_AV MUTE	RSVD0			SET_AV MUTE

Bit	Label	R/W	Description	Default
4	CLR_AVMUTE	R	Clear the AVMUTE flag. Unmutes both audio and video.	0
0	SET_AVMUTE	R	Set the AVMUTE flag. Mutes both audio and video.	0

The HDMI receiver reacts automatically on receipt of a General Control Packet to mute or enable the output audio stream. The mute state can also be controlled by the SiI9013 HDMI receiver's firmware with register 0x68:0x32, described on page 51.

Packet Type Decode Registers

Dev	Addr	Name	7	6	5	4	3	2	1	0
0x68	0xBF	MPEG_DEC	Decode Value used for Loading this InfoFrame (default MPEG)							
0x68	0x7F	SPD_DEC	Decode Value used for Loading this InfoFrame (default SPD)							
0x68	0xFF	ACP_DEC	Decode Value used for Loading this Packet (default ACP)							

Bit	Label	R/W	Description	Default
7:0	MPEG_DEC	R/W	MPEG InfoFrame decode. When set to 0x85, the MPEG InfoFrame is stored in 0xA0–0xAD. Registers 0xAE–0xBE are unmodified. When set to any other value, only an InfoFrame received with that value as its first byte is stored in 0xA0–0xBE.	0x85
7:0	SPD_DEC	R/W	SPD InfoFrame decode. When set to 0x83, the SPD InfoFrame is stored in 0x60–0x7E. When set to any other value, only an InfoFrame received with that value as its first byte is stored in 0x60–0x7E.	0x83
7:0	ACP_DEC	R/W	ACP Packet decode. When set to 0x04, the ACP packet is stored in 0xE0–0xFE. When set to any other value, only a packet received with that value as its first byte is stored in 0xE0–0xFE.	0x04

Appendix: Differences between SiI9013 and SiI9031

Table 6. Differences Between SiI9013 and SiI9031

Feature	Register	Change from SiI9031	Page
Device ID	0x74:0xFB	Changed value.	3
	0x60:0x02–0x03	Changed value.	8
Reset	0x60:0x05	Added manual reset bit for AAC.	9
System Status	0x60:0x06	Limited to one 5V status bit for one port.	10
SYS_CTRL1	0x60:0x08	Added PIXS to select 24-bit and 48-bit output modes.	11
DDC Delay	0x60:0x09	Added select to insert 300ns delay in SDA line.	12
Video Control	0x60:0x48	Removed ICS, CHA, and CVS bits formerly for DAC.	22
Video Mode #2	0x60:0x49	Removed PED_EN and DACRGB bits formerly for DAC.	21
Video Mode #1	0x60:0x4A	Removed INCSYNC bit formerly for DAC.	21
Auto Output Format	0x60:0x5F	Reduced choices for AOF to just digital modes.	24
Auto Exception	0x60:0xB6	Removed "clock switch" AEC07 bit.	36
System Power Down	0x68:0x3E–0x3F	Removed power-down bits related to second input port.	53

References

Standards Documents

Table 7 lists the standards abbreviations used in this document. Contact the responsible standards groups listed in Table 8 for more information on these specifications.

Table 7. Referenced Documents

Abbreviation	Specification
HDMI CTS	*HDMI Compliance Test Specification, Revision 1.1. HDMI Consortium; June 2004.*
HDCP 1.1	*High-bandwidth Digital Content Protection, Revision 1.1, Digital-Content Protection, LLC; June 2003.*
DVI	*Digital Visual Interface, Revision 1.0, Digital Display Working Group; April 1999.*
E-EDID	*Enhanced Extended Display Identification Data Standard, Release A Revision 1, Video Electronics Standards Association (VESA); February 2000.*
CEA861B	*A DTV Profile For Uncompressed High Speed Digital Interfaces, EIA/CEA; May 2002.*
EDDC	*Enhanced Display Data Channel Standard, Version 1, VESA; September 1999.*

Table 8. Standards Groups Contact Information

Standards Group	Web URL	e-mail	Phone
ANSI/EIA/CEA	http://global.ihs.com	global@ihs.com	800-854-7179
VESA	http://www.vesa.org	—	408-957-9270
HDCP	http://www.digital-cp.com	info@digital-cp.com	—
DVI	http://www.ddwg.org	ddwg.if@intel.com	—
HDMI	http://www.hdmi.org	admin@hdmi.org	—

Silicon Image Documents

Table 9 lists the documents available from your Silicon Image sales representative.

Table 9. Silicon Image Documents

Document	Document Name
SiI-AN-0118	*SiI9011/9021/9031 HDMI PanelLink Receivers Application Note*
SiI-AN-0111	*SiI9031 - 9030 HDMI PanelLink Repeater Application Note*

Disclaimers

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