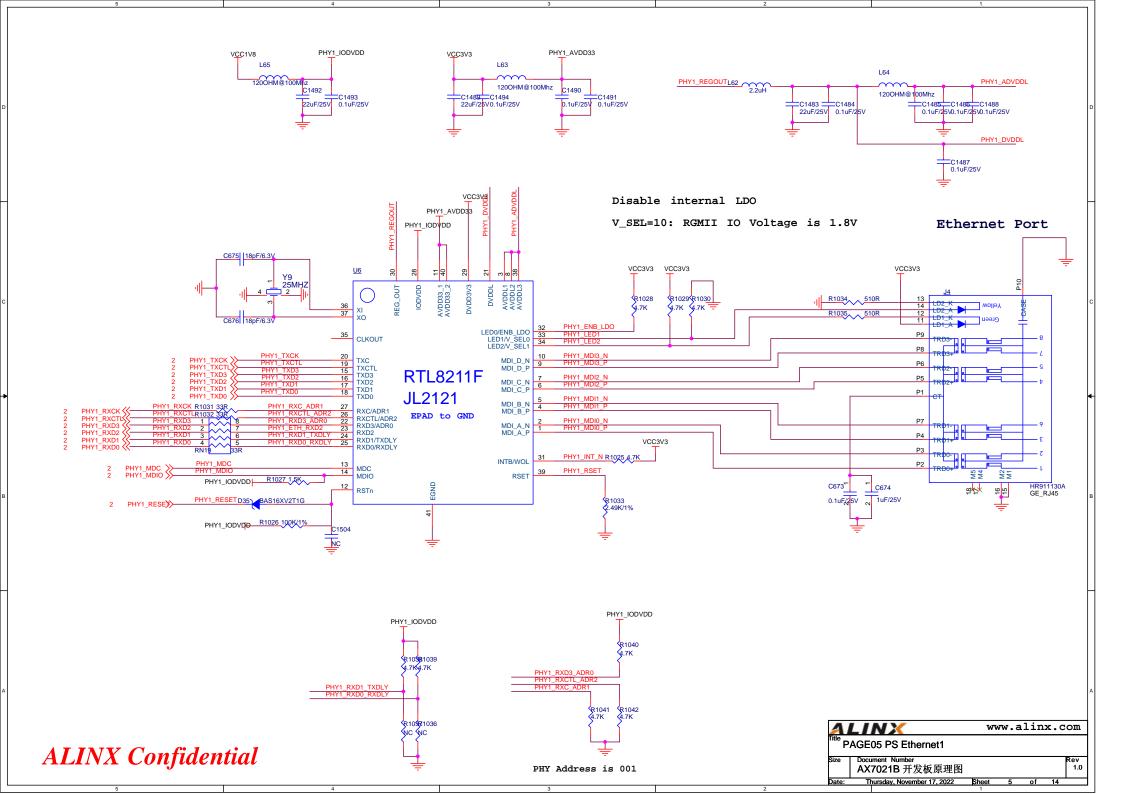
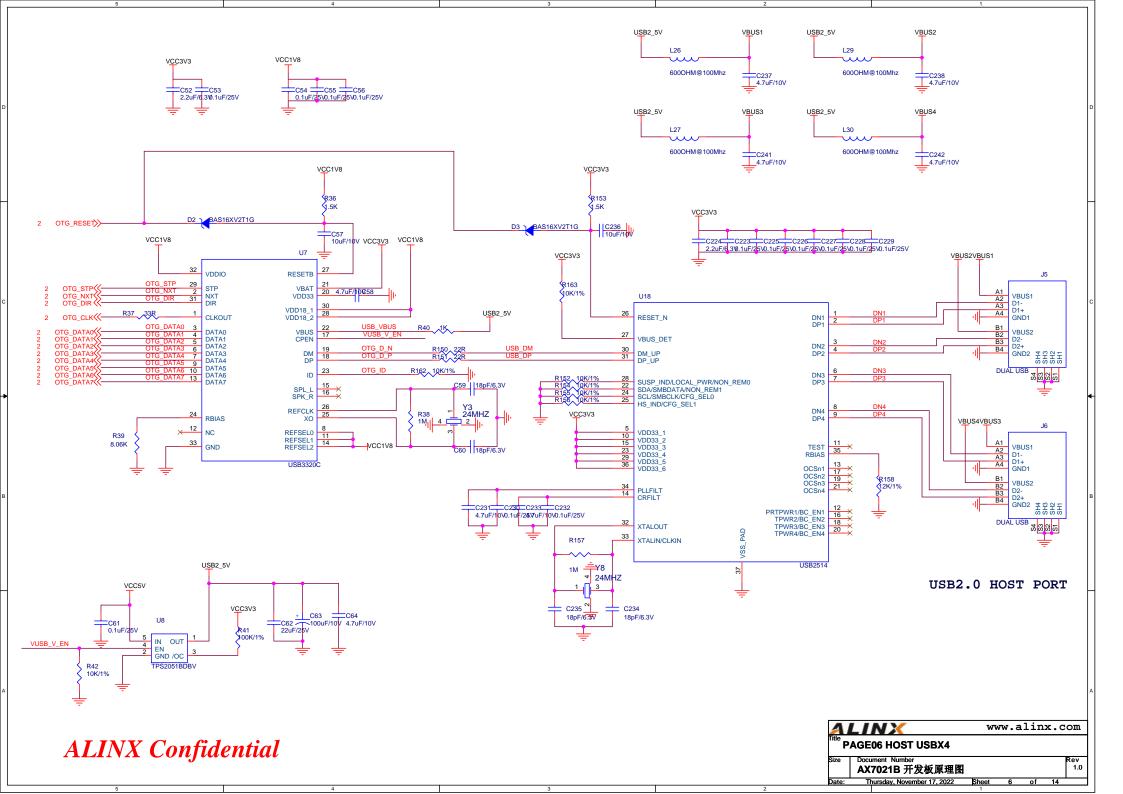


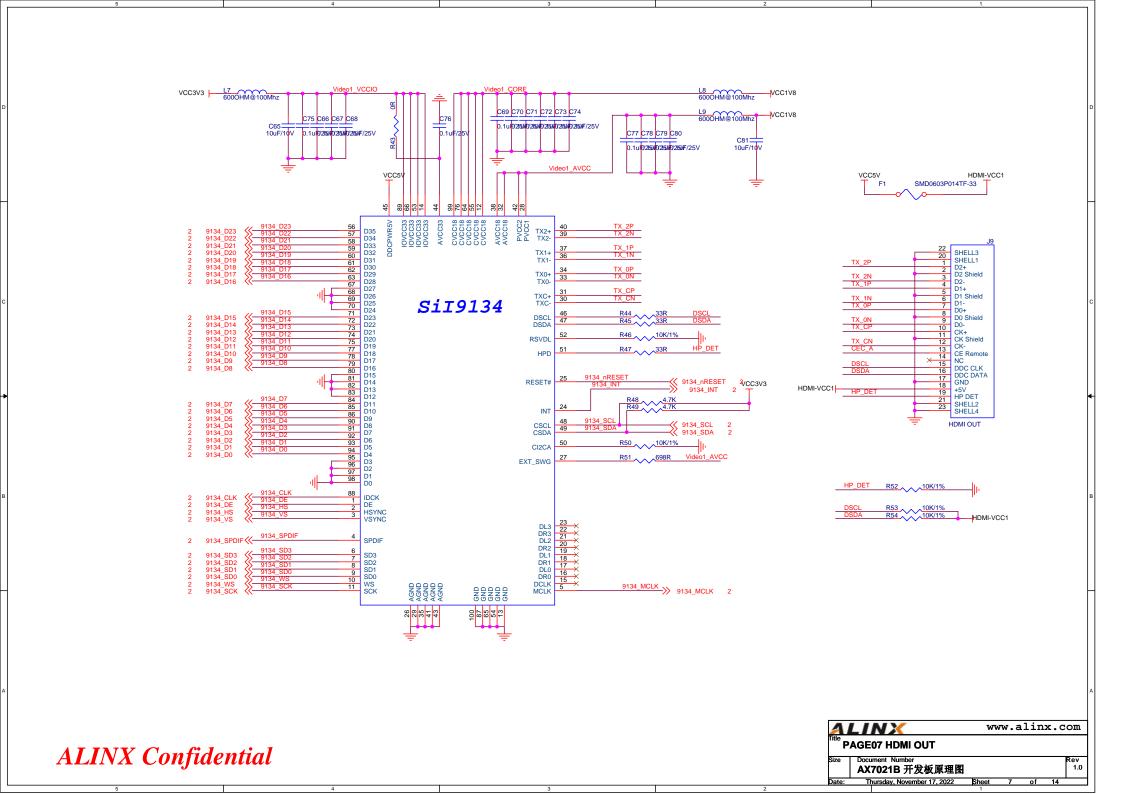
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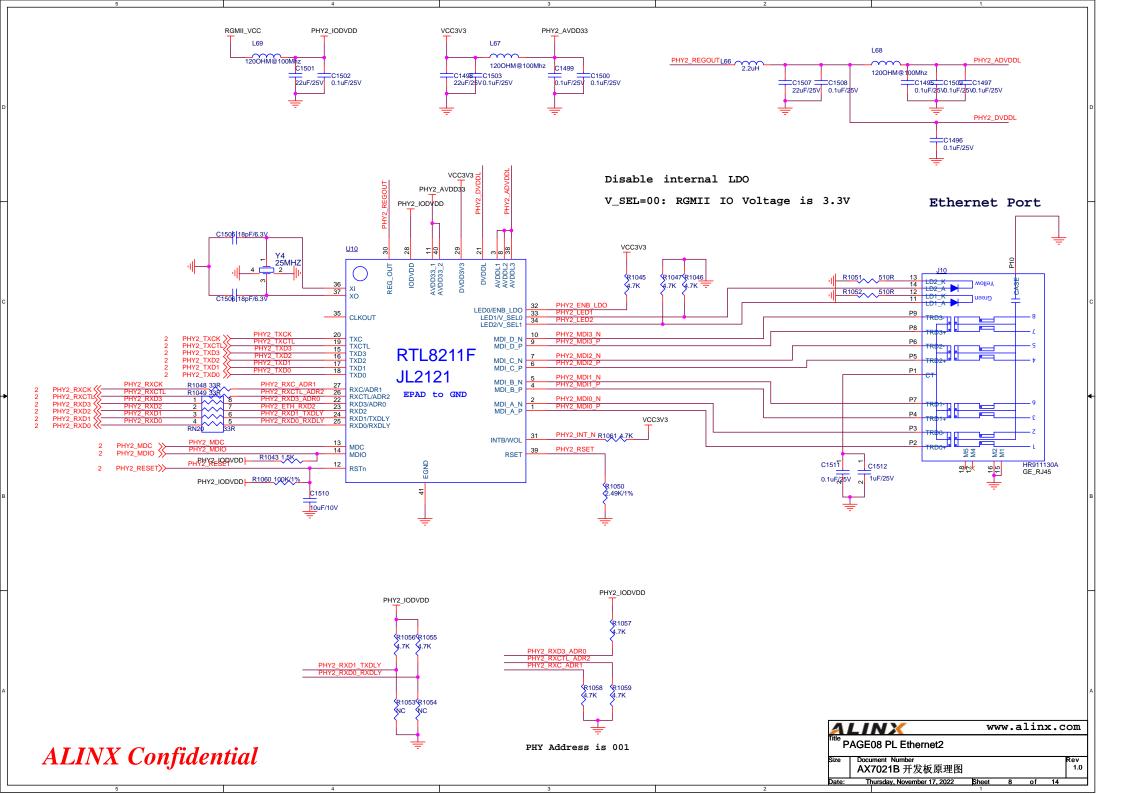
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Title P	AGE03 JTAG						
Size	Document Number AX7021B 开发板原理图					Rev 1.0	
Date:	Thursday, November 17, 2022	Sheet	3	of	14		

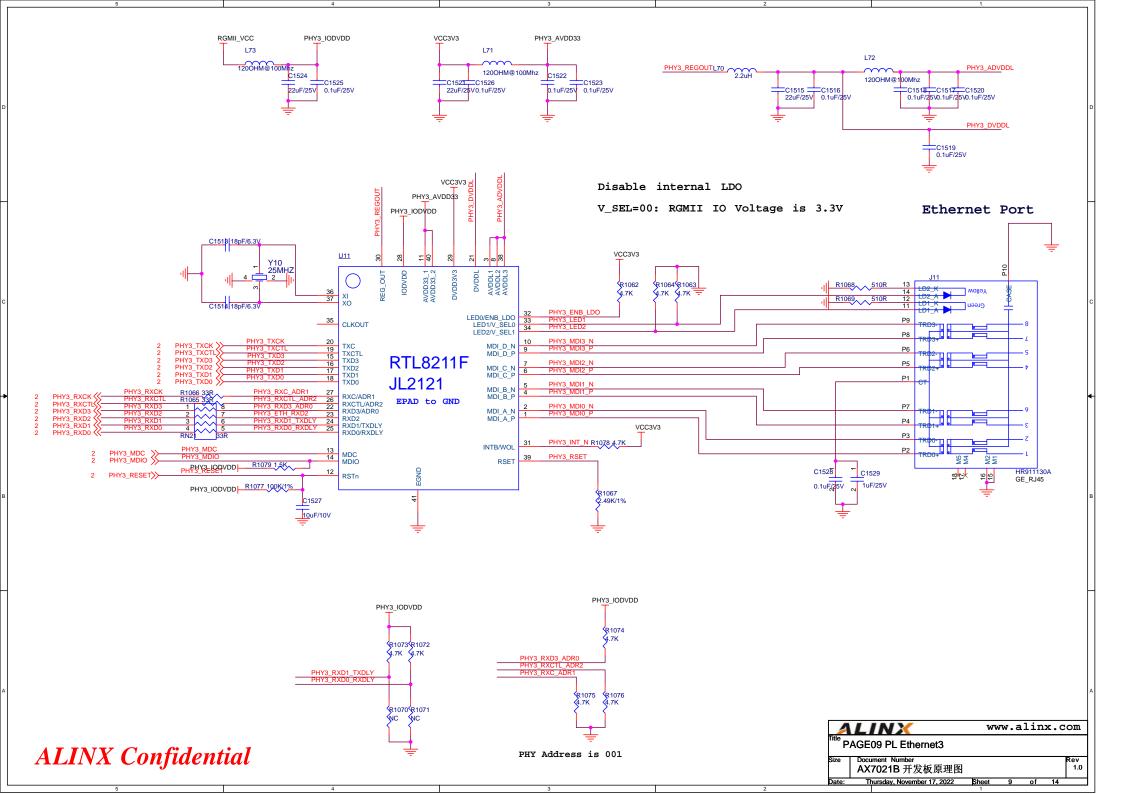
# **USB Uart** R159 10K/**3**% VCC3V3 VCC3V3 C240 0.1uF/25V C239 0.1uF/25V C222 C221 1uF/25V10uF/10V U4 GND R160 1 VBUS REGIN VCC3V3 SD Card Connector VCC1V8 VCC3V3 C22 \_\_\_\_C23 10uF/10V0.1uF/25V C25 0.1uF/25V U5 VCCA SD\_D0 SD\_D1 SD\_D2 SD\_D3 SD\_CLK SD\_CMD DATOA DAT1A DAT2A DAT3A CLKA CMDA DAT0B0 DAT1B0 DAT2B0 DAT3B0 CLKB0 CMDB0 DAT2 CD/DAT3 CMD VDD CLK VSS DAT0 DAT1 VCCB1 DAT0B1 DAT1B1 DAT2B1 DAT3B1 CLKB1 CMDB1 SEL VCC3V3 2 11 25 GND1 GND2 EPAD CD QQQQ TXS02612RTWR R20 330R 2 SD\_CD <<www.alinx.com PAGE04 SD Card and UART **ALINX Confidential** Document Number AX7021B 开发板原理图 Rev 1.0

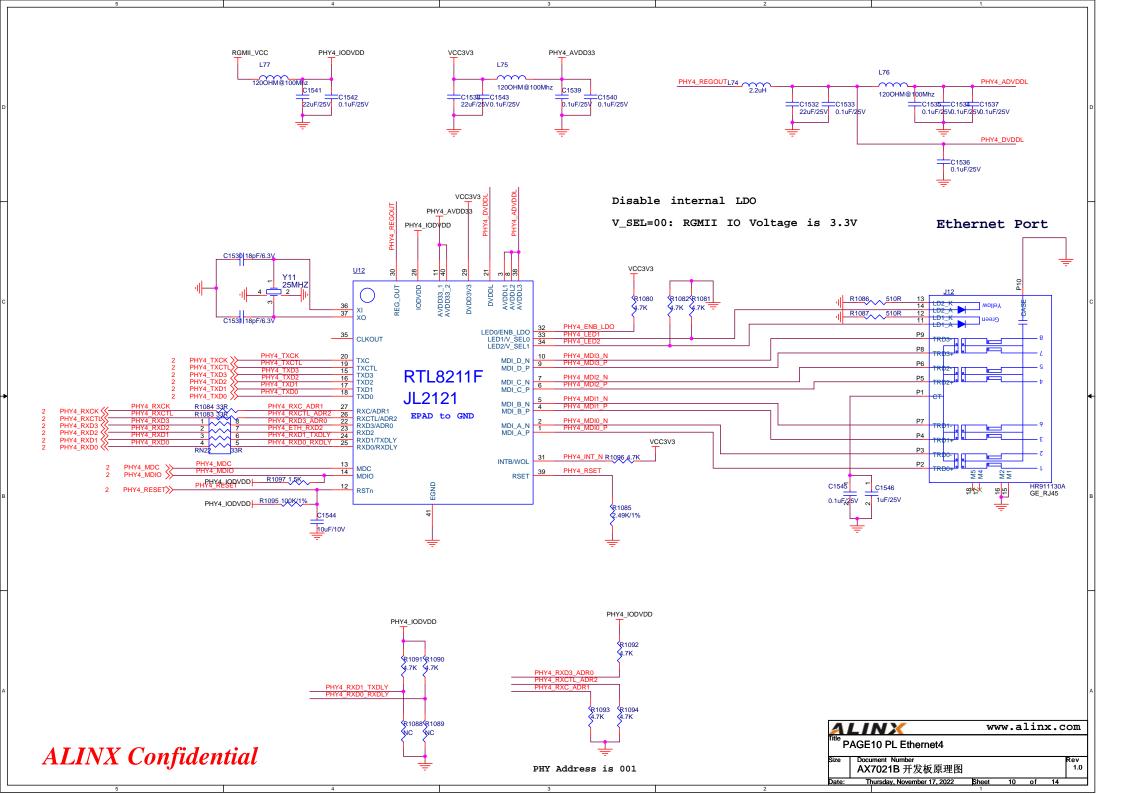


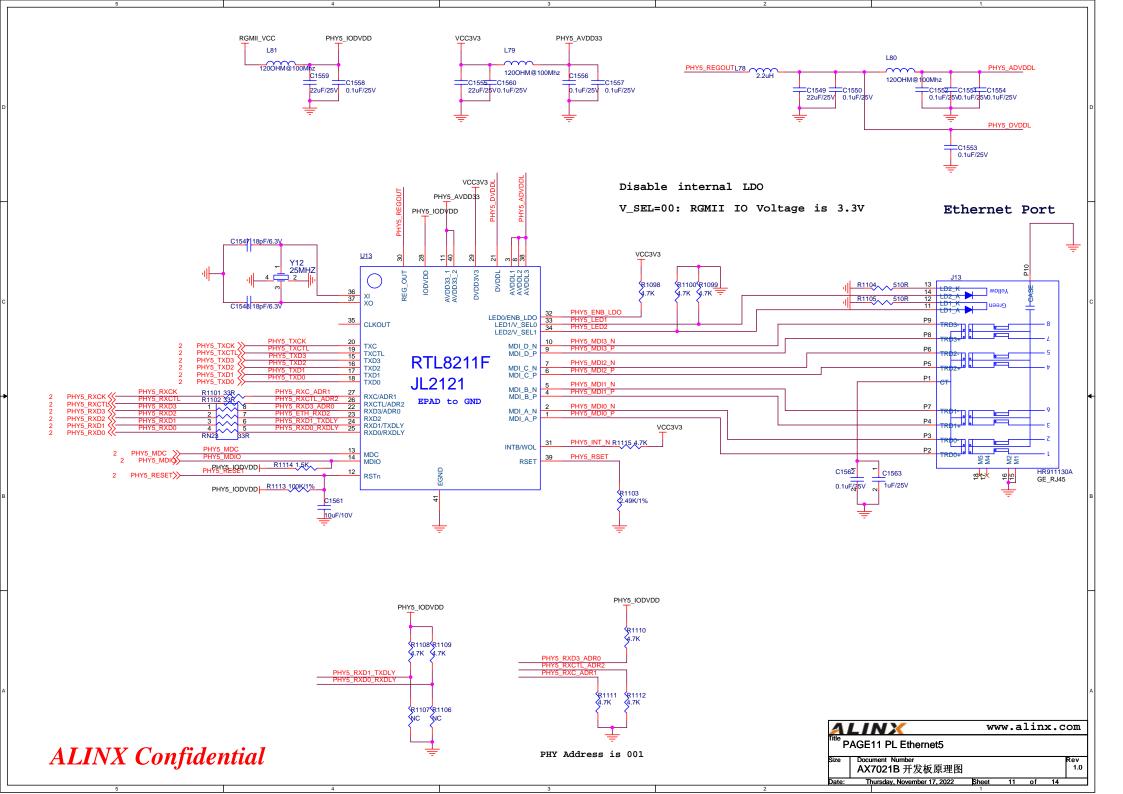


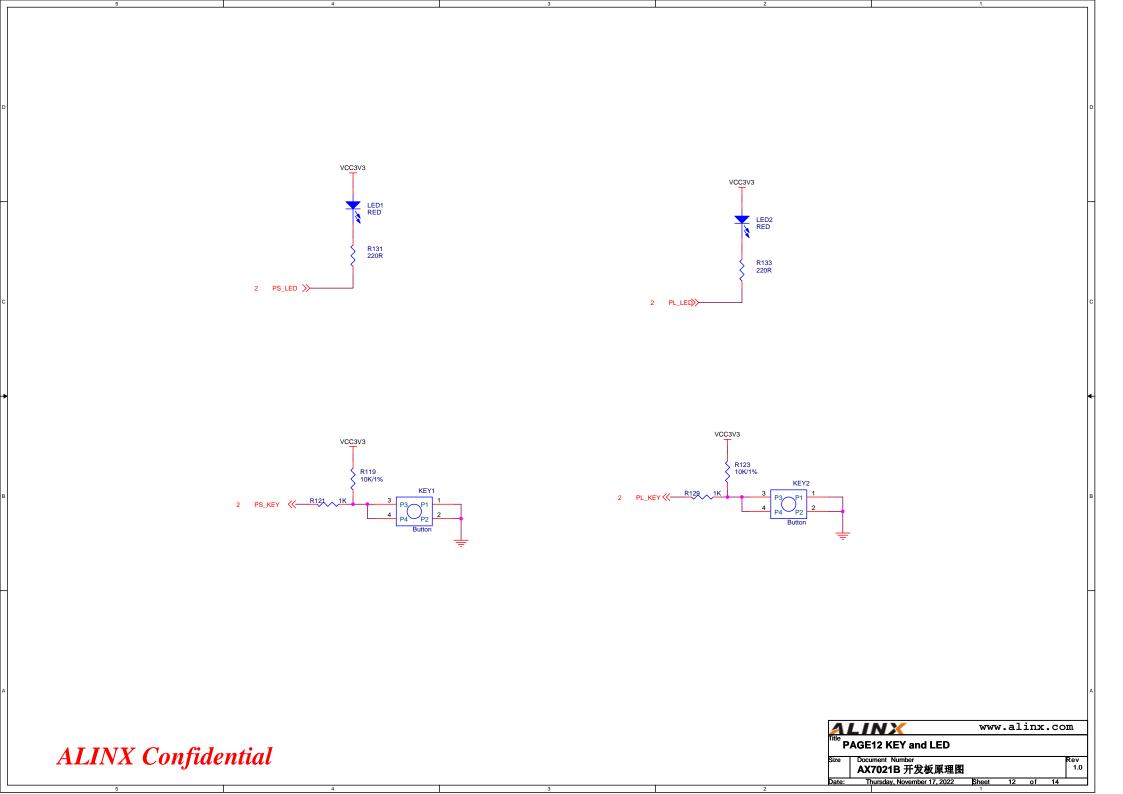


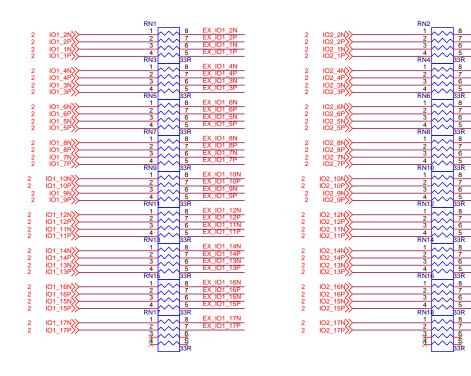




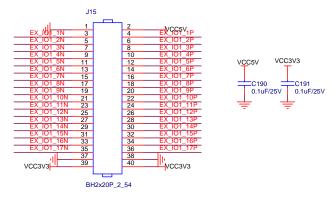




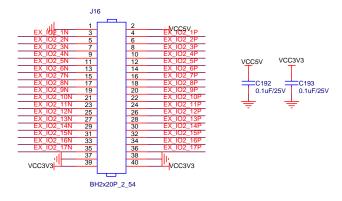


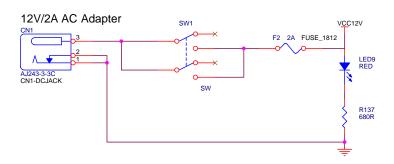


# FPGA 40 PIN External IO

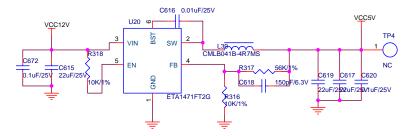


# FPGA 40 PIN External IO



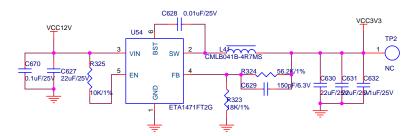


## +5V POWER

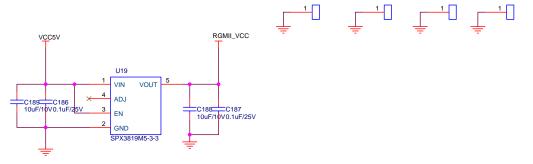


 $Vout=0.8 \times (1 + R1/R2)$ 

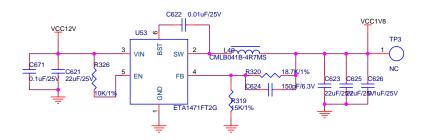
### +3.3V POWER



 $Vout=0.8 \times (1 + R1/R2)$ 



#### +1.8V POWER



 $Vout=0.8 \times (1 + R1/R2)$ 

