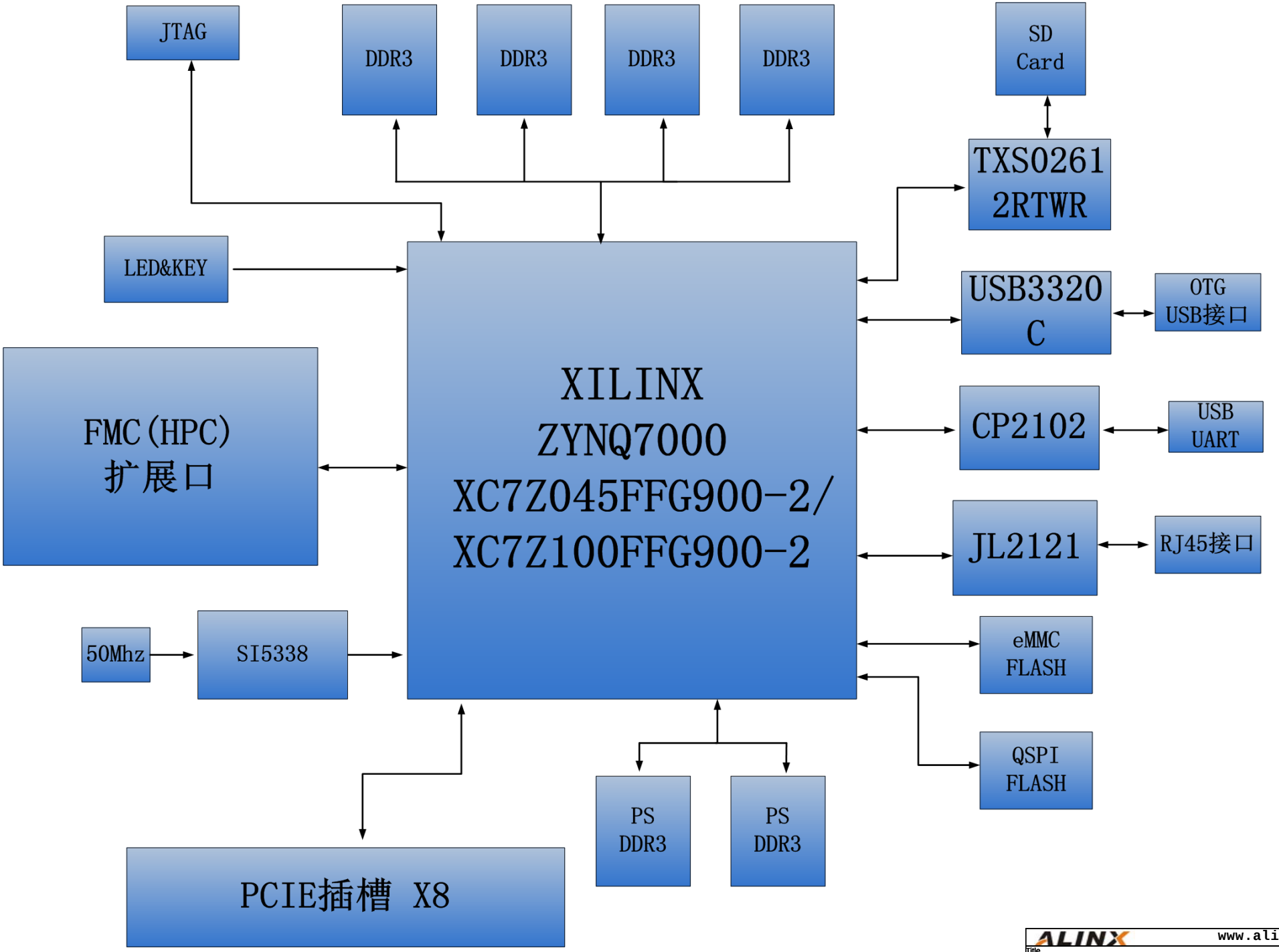

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Title: PAGE01 Block diagram

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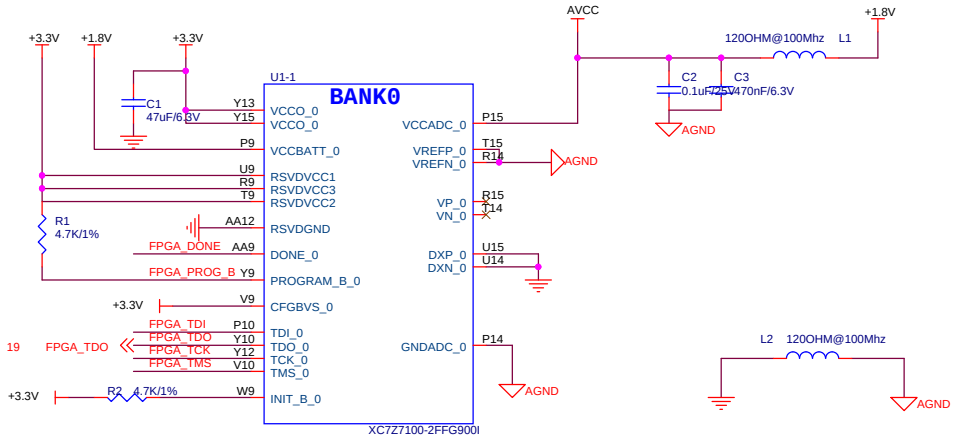
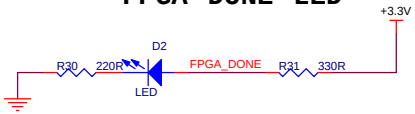
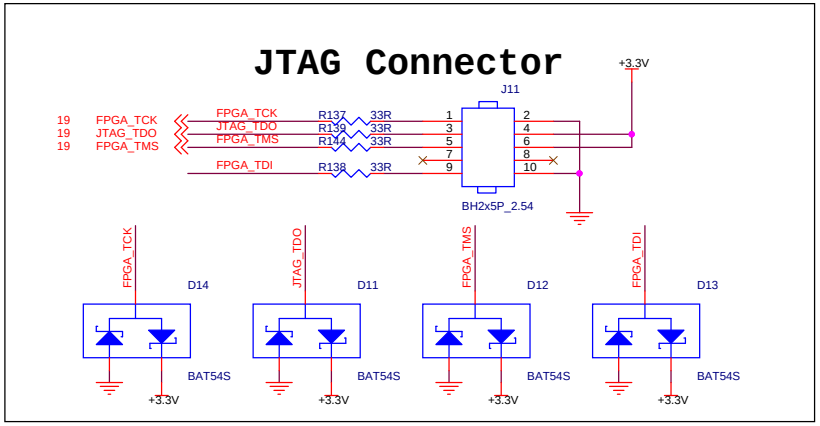


FPGA DONE LED



JTAG Connector



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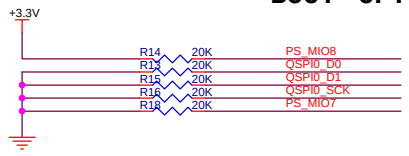
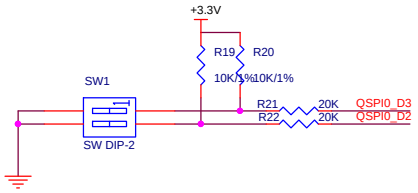
BOOT OPTION

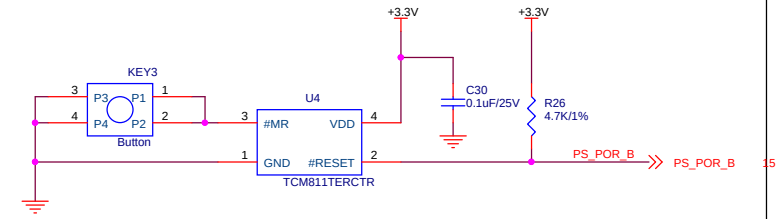


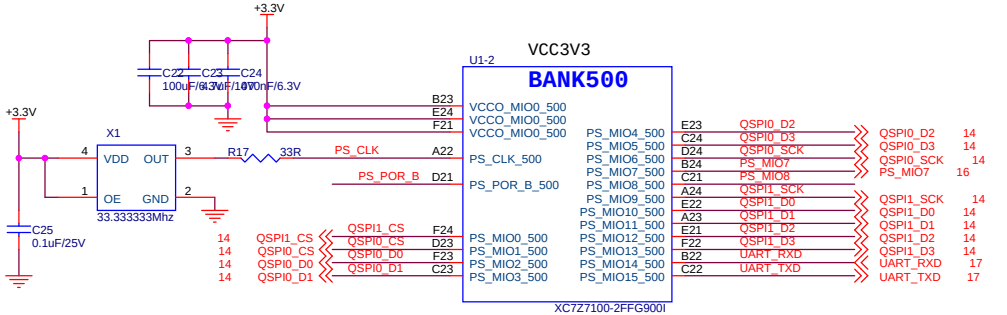
MIO[8] =1 ----MIO bank1 voltage=1.8V
MIO[2] =0 ----cascaded JTAG
MIO[3] =0 ----JTAG/NAND/Quad-SPI/SD
MIO[6] =0 ----PLL used
MIO[7] =0 ----MIO bank0 voltage=3.3V

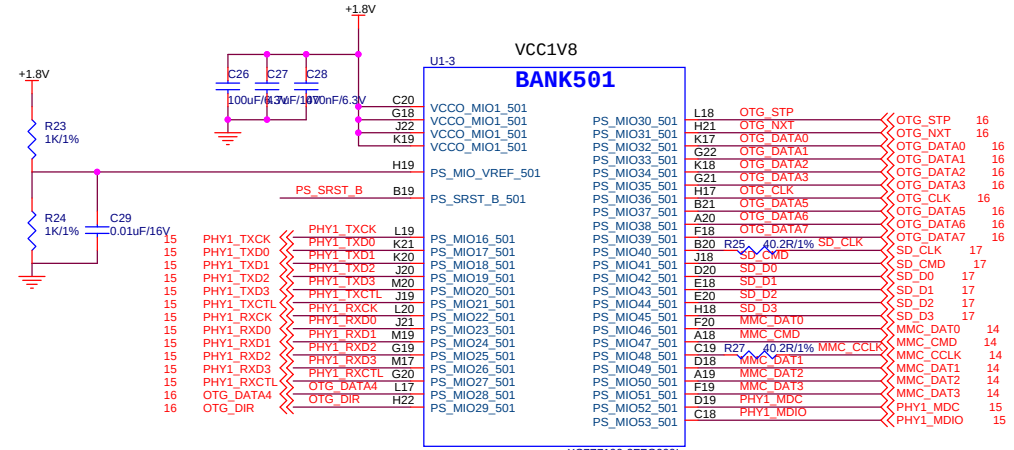


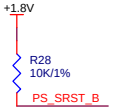
Boot Mode	MIO[5] (QSPI_D3)	MIO[4] (QSPI_D2)
JTAG	0	0
NAND	0	1
QSPI-FLASH	1	0
SD Card	1	1

POWER ON RESET









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Title: PAGE03 Z7 MIO-Config

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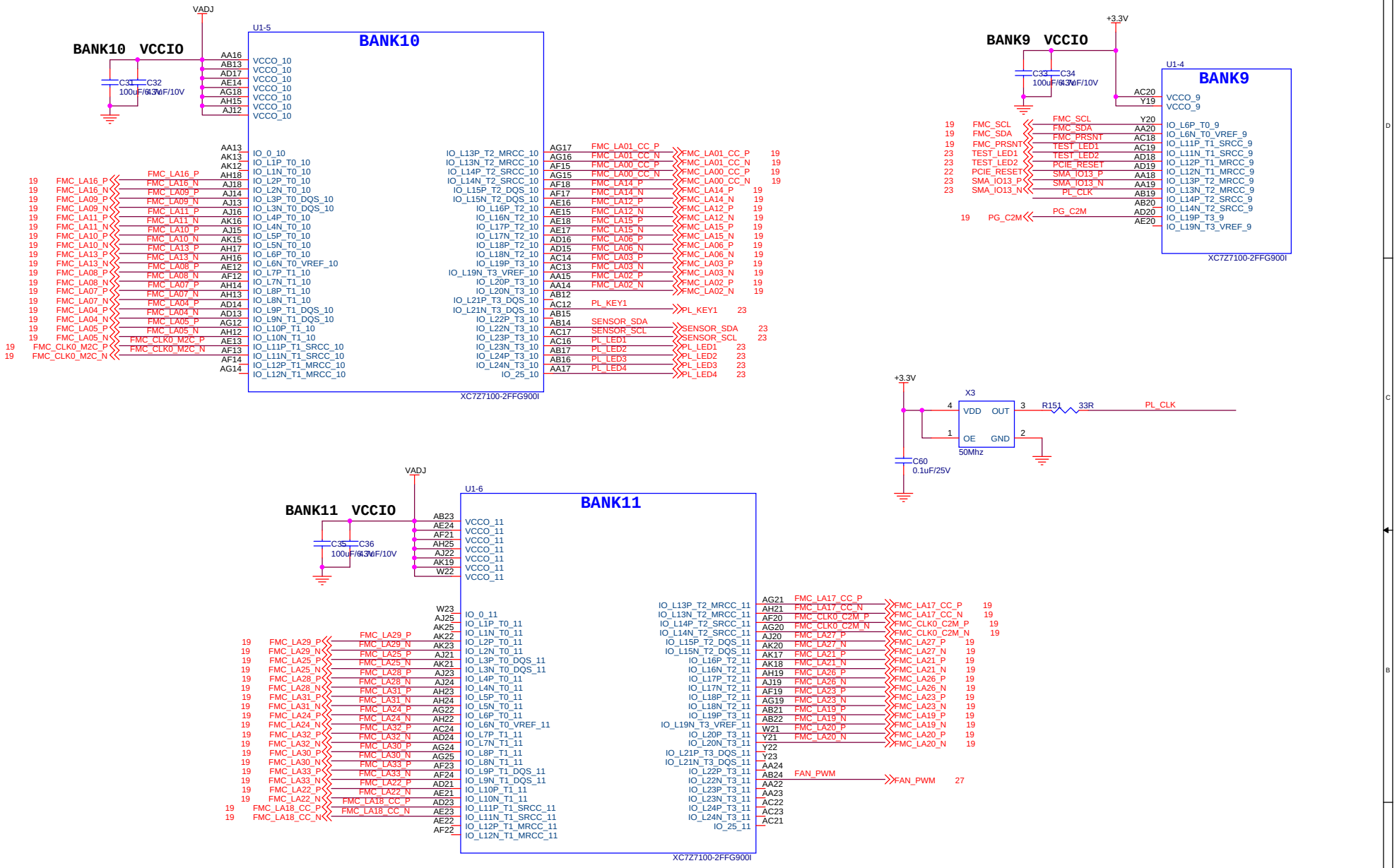
BANK10 VCCIO
VADJ
U1-5
BANK10
C31 100uF/6.3V
C32 0.1uF/10V
AA16 AB13 AD17 AE14 AG18 AH15 AJ12
VCCO_10
XC7Z7100-2FFG900I
BANK9 VCCIO
+3.3V
U1-4
BANK9
C33 100uF/6.3V
C34 0.1uF/10V
AC20 Y19
VCCO_9
XC7Z7100-2FFG900I
BANK11 VCCIO
U1-6
BANK11
C35 100uF/6.3V
C36 0.1uF/10V
AB23 AE24 AF21 AH25 AJ22 AK19 W22
VCCO_11
XC7Z7100-2FFG900I
X3
VDD OUT OE GND
50Mhz
R151 33R
PL_CLK
C60 0.1uF/25V
FAN_PWM
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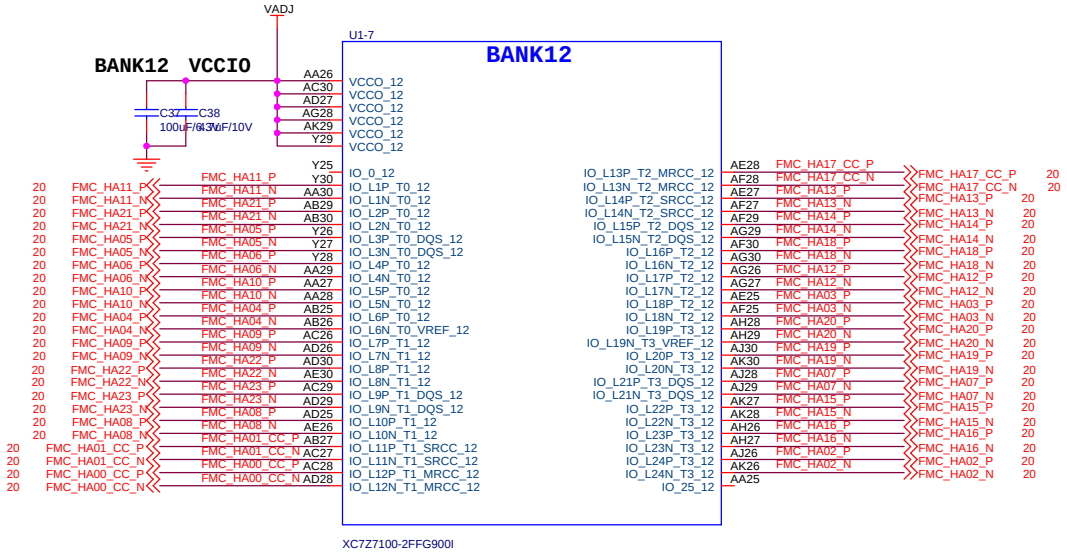

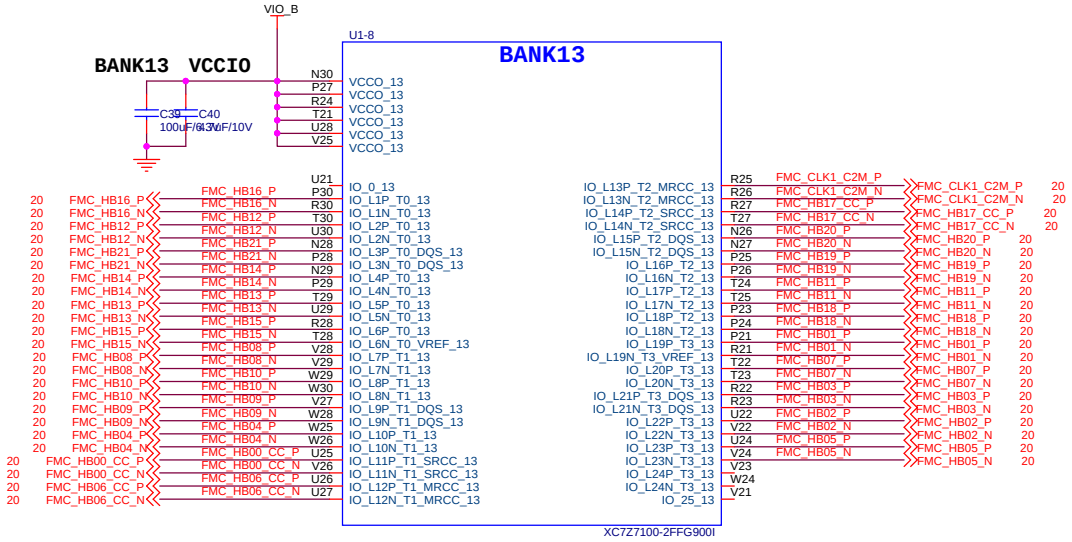

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Title: PAGE05 Z7 Bank12 & Bank13

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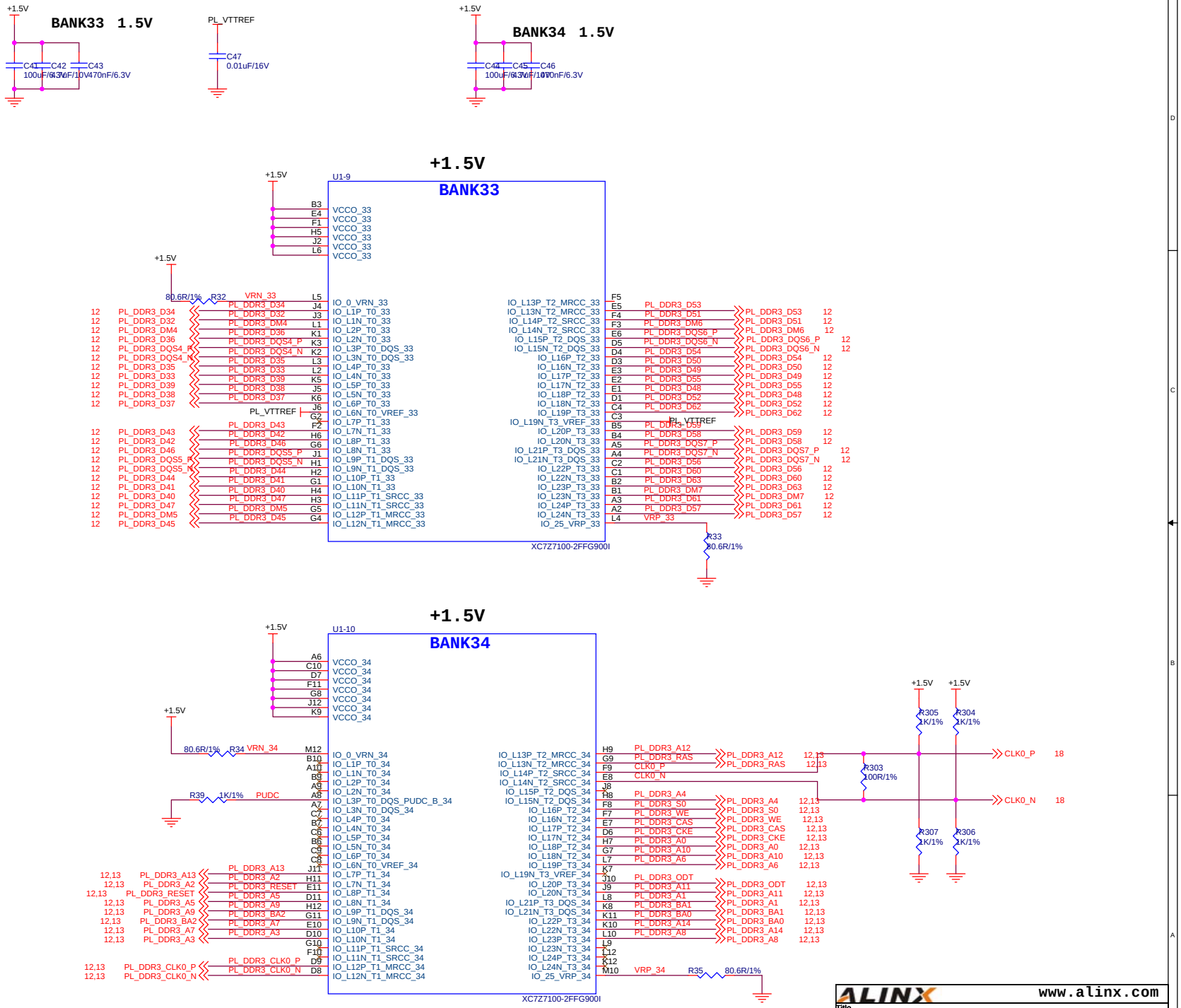
BANK33 1.5V
+1.5V
C41 100uF/6.3V
C42 47uF/10V
C43 470nF/6.3V
PL_VTTREF
C47 0.01uF/16V
BANK34 1.5V
C44 100uF/6.3V
C45 47uF/10V
C46 470nF/6.3V
+1.5V
BANK33
U1-9
VCCO_33
IO_0_VRN_33
IO_L1P_T0_33
IO_L1N_T0_33
IO_L2P_T0_33
IO_L2N_T0_33
IO_L3P_T0_DQS_33
IO_L3N_T0_DQS_33
IO_L4P_T0_33
IO_L4N_T0_33
IO_L5P_T0_33
IO_L5N_T0_33
IO_L6P_T0_33
IO_L6N_T0_VREF_33
IO_L7P_T1_33
IO_L7N_T1_33
IO_L8P_T1_33
IO_L8N_T1_33
IO_L9P_T1_DQS_33
IO_L9N_T1_DQS_33
IO_L10P_T1_33
IO_L10N_T1_33
IO_L11P_T1_SRCC_33
IO_L11N_T1_SRCC_33
IO_L12P_T1_MRCC_33
IO_L12N_T1_MRCC_33
IO_L13P_T2_MRCC_33
IO_L13N_T2_MRCC_33
IO_L14P_T2_SRCC_33
IO_L14N_T2_SRCC_33
IO_L15P_T2_DQS_33
IO_L15N_T2_DQS_33
IO_L16P_T2_33
IO_L16N_T2_33
IO_L17P_T2_33
IO_L17N_T2_33
IO_L18P_T2_33
IO_L18N_T2_33
IO_L19P_T3_33
IO_L19N_T3_VREF_33
IO_L20P_T3_33
IO_L20N_T3_33
IO_L21P_T3_DQS_33
IO_L21N_T3_DQS_33
IO_L22P_T3_33
IO_L22N_T3_33
IO_L23P_T3_33
IO_L23N_T3_33
IO_L24P_T3_33
IO_L24N_T3_33
IO_25_VRP_33
XC7Z7100-2FFG900I
80.6R/1% R32 VRN_33
PL_VTTREF
R33 80.6R/1%
PL_DDR3_D34
PL_DDR3_D32
PL_DDR3_DM4
PL_DDR3_D36
PL_DDR3_DQS4_P
PL_DDR3_DQS4_N
PL_DDR3_D35
PL_DDR3_D33
PL_DDR3_D39
PL_DDR3_D38
PL_DDR3_D37
PL_DDR3_D43
PL_DDR3_D42
PL_DDR3_D46
PL_DDR3_DQS5_P
PL_DDR3_DQS5_N
PL_DDR3_D44
PL_DDR3_D41
PL_DDR3_D40
PL_DDR3_D47
PL_DDR3_DM5
PL_DDR3_D45
PL_DDR3_D53
PL_DDR3_D51
PL_DDR3_DM6
PL_DDR3_DQS6_P
PL_DDR3_DQS6_N
PL_DDR3_D54
PL_DDR3_D50
PL_DDR3_D49
PL_DDR3_D55
PL_DDR3_D48
PL_DDR3_D52
PL_DDR3_D62
PL_DDR3_D59
PL_DDR3_D58
PL_DDR3_DQS7_P
PL_DDR3_DQS7_N
PL_DDR3_D56
PL_DDR3_D60
PL_DDR3_D63
PL_DDR3_DM7
PL_DDR3_D61
PL_DDR3_D57
VRP_33
+1.5V
BANK34
U1-10
VCCO_34
IO_0_VRN_34
IO_L1P_T0_34
IO_L1N_T0_34
IO_L2P_T0_34
IO_L2N_T0_34
IO_L3P_T0_DQS_PUDC_B_34
IO_L3N_T0_DQS_34
IO_L4P_T0_34
IO_L4N_T0_34
IO_L5P_T0_34
IO_L5N_T0_34
IO_L6P_T0_34
IO_L6N_T0_VREF_34
IO_L7P_T1_34
IO_L7N_T1_34
IO_L8P_T1_34
IO_L8N_T1_34
IO_L9P_T1_DQS_34
IO_L9N_T1_DQS_34
IO_L10P_T1_34
IO_L10N_T1_34
IO_L11P_T1_SRCC_34
IO_L11N_T1_SRCC_34
IO_L12P_T1_MRCC_34
IO_L12N_T1_MRCC_34
IO_L13P_T2_MRCC_34
IO_L13N_T2_MRCC_34
IO_L14P_T2_SRCC_34
IO_L14N_T2_SRCC_34
IO_L15P_T2_DQS_34
IO_L15N_T2_DQS_34
IO_L16P_T2_34
IO_L16N_T2_34
IO_L17P_T2_34
IO_L17N_T2_34
IO_L18P_T2_34
IO_L18N_T2_34
IO_L19P_T3_34
IO_L19N_T3_VREF_34
IO_L20P_T3_34
IO_L20N_T3_34
IO_L21P_T3_DQS_34
IO_L21N_T3_DQS_34
IO_L22P_T3_34
IO_L22N_T3_34
IO_L23P_T3_34
IO_L23N_T3_34
IO_L24P_T3_34
IO_L24N_T3_34
IO_25_VRP_34
XC7Z7100-2FFG900I
80.6R/1% R34 VRN_34
R39 1K/1% PUDC
R35 80.6R/1%
VRP_34
PL_DDR3_A13
PL_DDR3_A2
PL_DDR3_RESET
PL_DDR3_A5
PL_DDR3_A9
PL_DDR3_BA2
PL_DDR3_A7
PL_DDR3_A3
PL_DDR3_CLK0_P
PL_DDR3_CLK0_N
PL_DDR3_A12
PL_DDR3_RAS
CLK0_P
CLK0_N
PL_DDR3_A4
PL_DDR3_S0
PL_DDR3_WE
PL_DDR3_CAS
PL_DDR3_CKE
PL_DDR3_A0
PL_DDR3_A10
PL_DDR3_A6
PL_DDR3_ODT
PL_DDR3_A11
PL_DDR3_A1
PL_DDR3_BA1
PL_DDR3_BA0
PL_DDR3_A14
PL_DDR3_A8
R305 1K/1%
R304 1K/1%
R303 100R/1%
R307 1K/1%
R306 1K/1%
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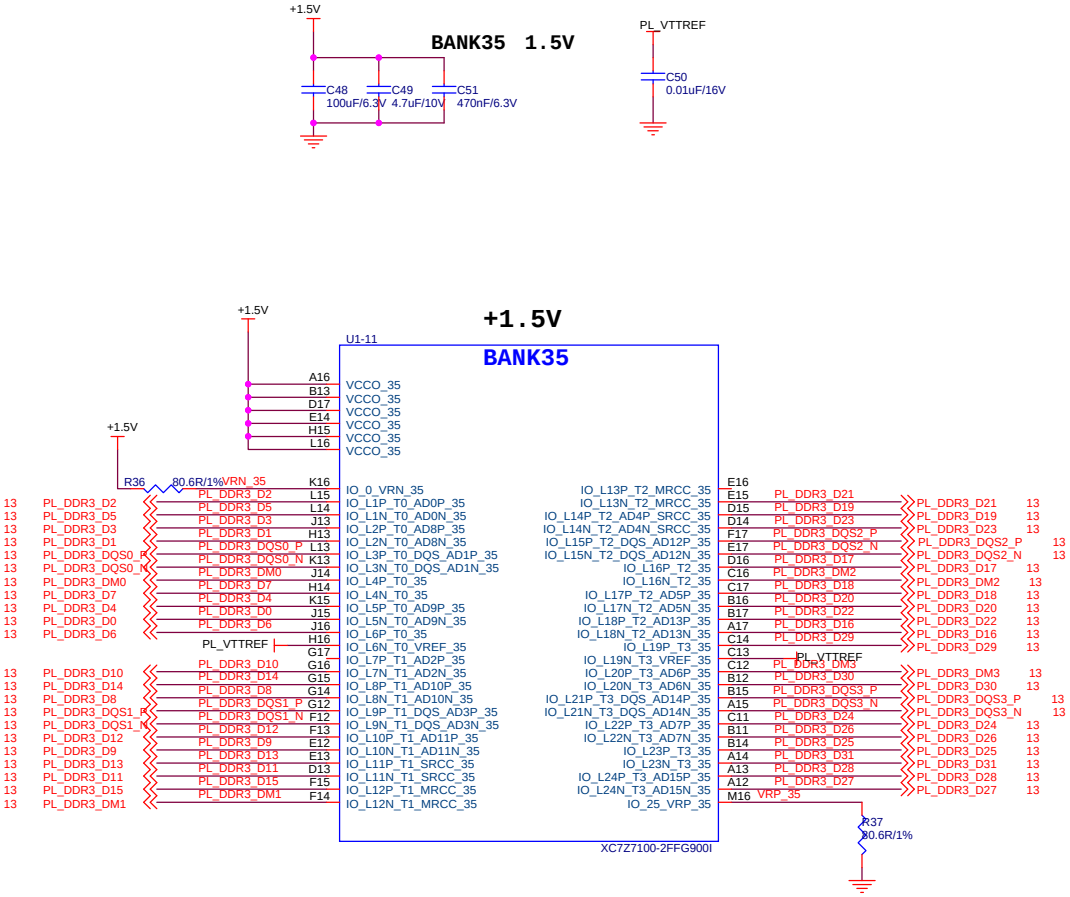

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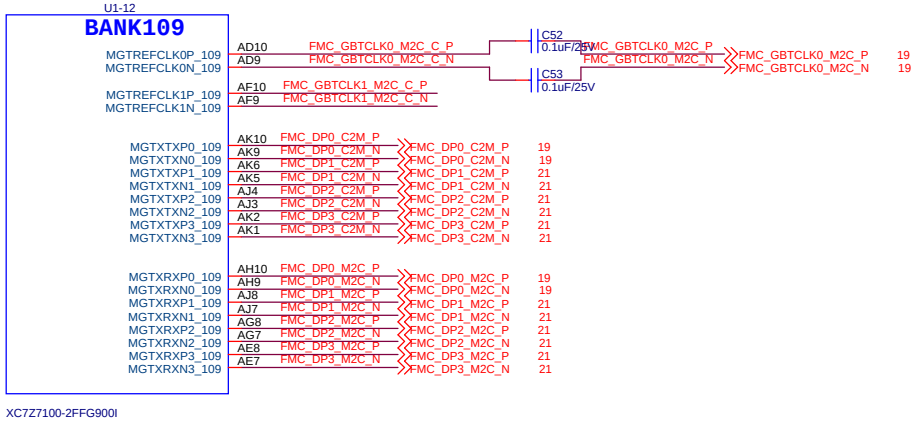

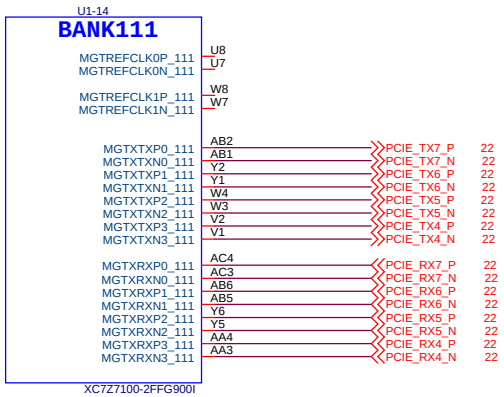

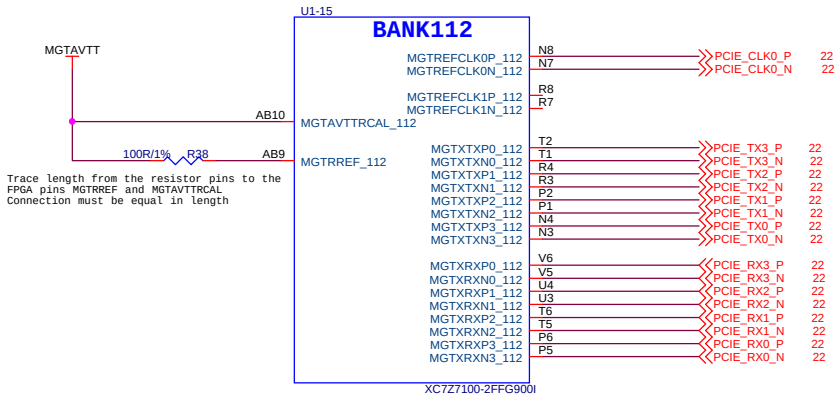

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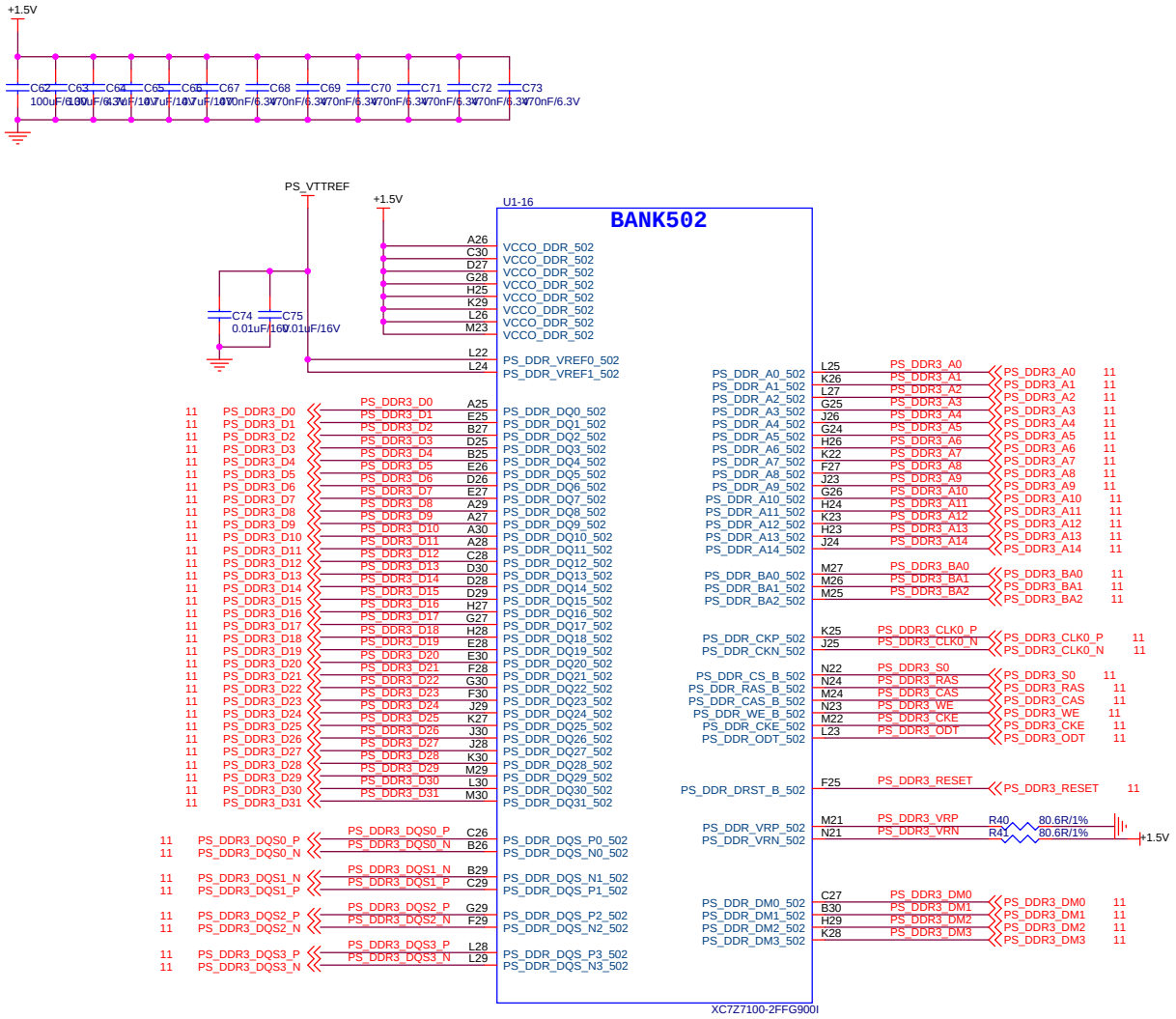

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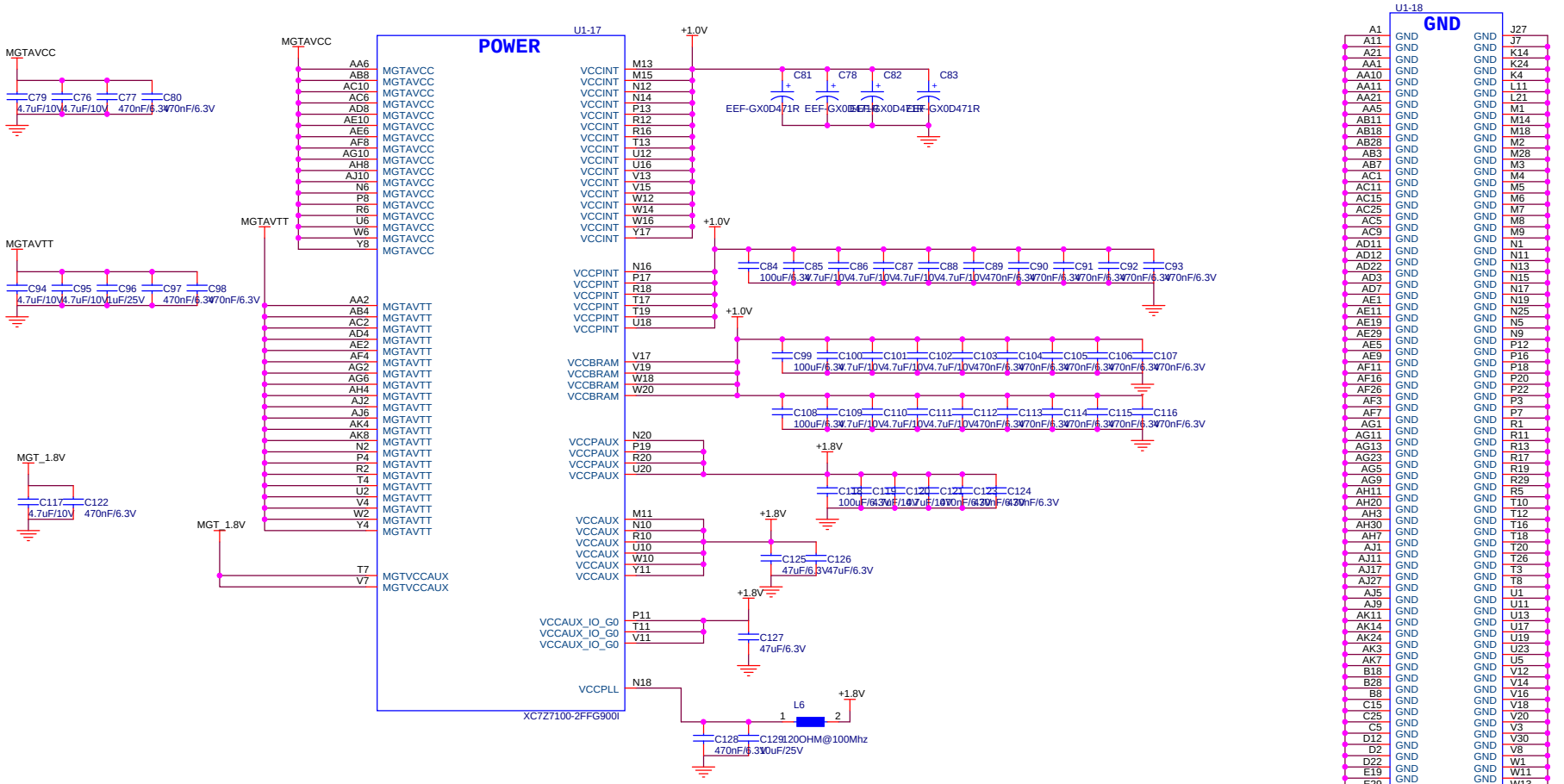

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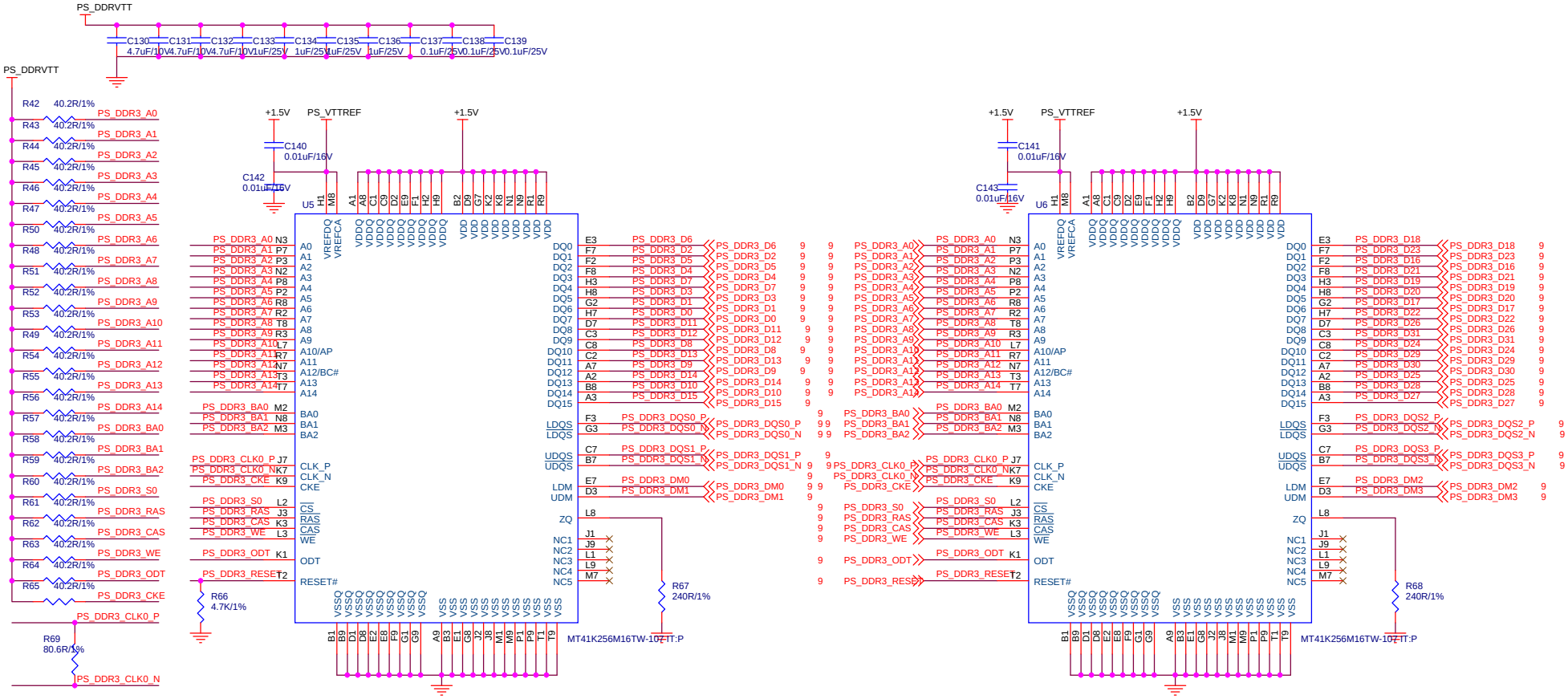
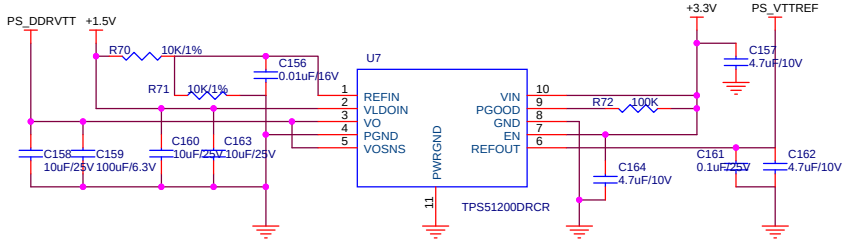


DDR POWER For VTT/VREF



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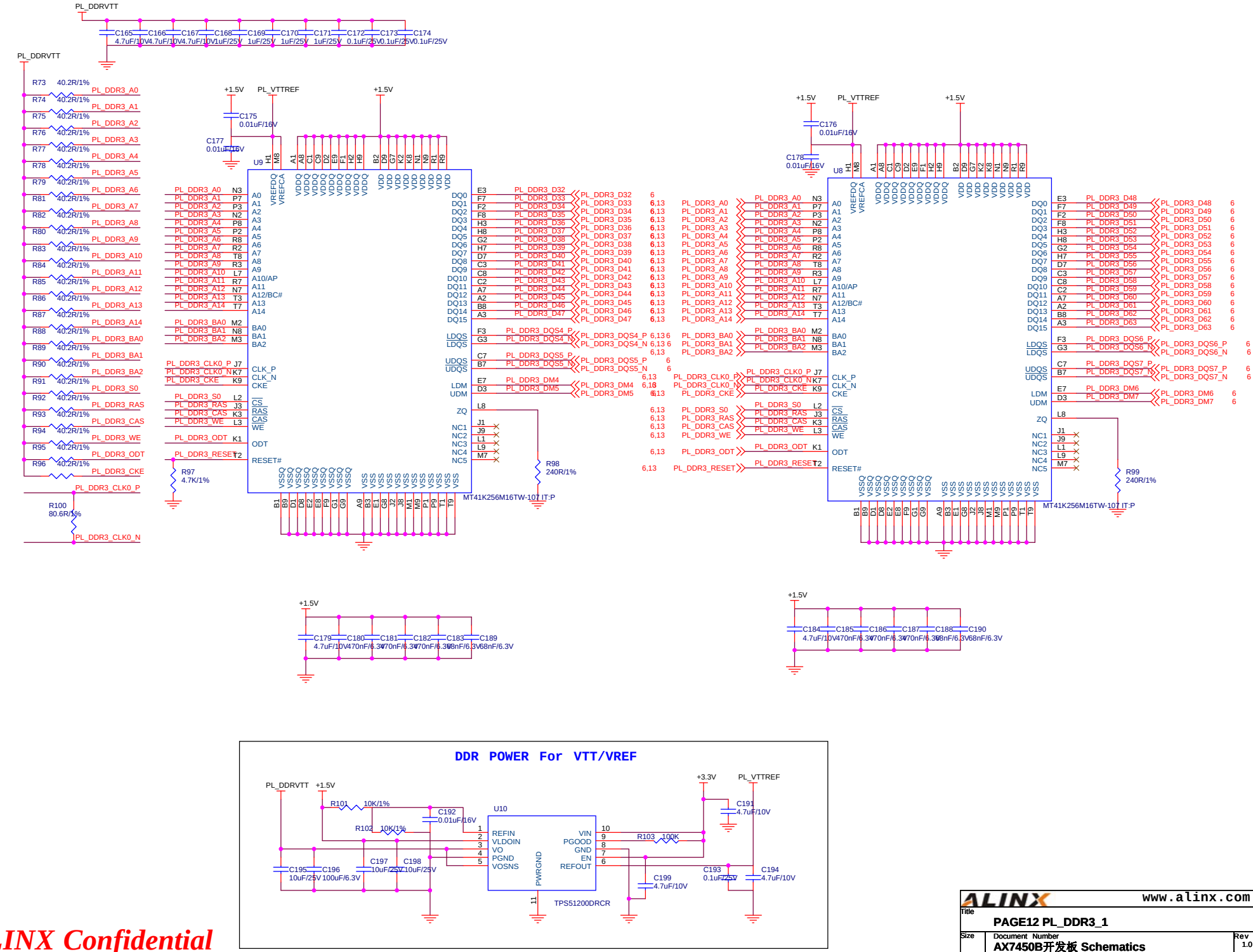
PL_DDRVTT
C165 4.7uF/10V
C166 4.7uF/10V
C167 4.7uF/10V
C168 1uF/25V
C169 1uF/25V
C170 1uF/25V
C171 1uF/25V
C172 0.1uF/25V
C173 0.1uF/25V
C174 0.1uF/25V
R73 40.2R/1%
R74 40.2R/1%
R75 40.2R/1%
R76 40.2R/1%
R77 40.2R/1%
R78 40.2R/1%
R79 40.2R/1%
R81 40.2R/1%
R82 40.2R/1%
R80 40.2R/1%
R83 40.2R/1%
R84 40.2R/1%
R85 40.2R/1%
R86 40.2R/1%
R87 40.2R/1%
R88 40.2R/1%
R89 40.2R/1%
R90 40.2R/1%
R91 40.2R/1%
R92 40.2R/1%
R93 40.2R/1%
R94 40.2R/1%
R95 40.2R/1%
R96 40.2R/1%
PL_DDR3_A0
PL_DDR3_A1
PL_DDR3_A2
PL_DDR3_A3
PL_DDR3_A4
PL_DDR3_A5
PL_DDR3_A6
PL_DDR3_A7
PL_DDR3_A8
PL_DDR3_A9
PL_DDR3_A10
PL_DDR3_A11
PL_DDR3_A12
PL_DDR3_A13
PL_DDR3_A14
PL_DDR3_BA0
PL_DDR3_BA1
PL_DDR3_BA2
PL_DDR3_S0
PL_DDR3_RAS
PL_DDR3_CAS
PL_DDR3_WE
PL_DDR3_ODT
PL_DDR3_CKE
PL_DDR3_CLK0_P
PL_DDR3_CLK0_N
R100 80.6R/1%
+1.5V
PL_VTTREF
C175 0.01uF/16V
C177 0.01uF/16V
U9
MT41K256M16TW-107 IT:P
R97 4.7K/1%
R98 240R/1%
C176 0.01uF/16V
C178 0.01uF/16V
U8
R99 240R/1%
C179 4.7uF/10V
C180 470nF/6.3V
C181 470nF/6.3V
C182 470nF/6.3V
C183 68nF/6.3V
C189 68nF/6.3V
C184 4.7uF/10V
C185 470nF/6.3V
C186 470nF/6.3V
C187 470nF/6.3V
C188 68nF/6.3V
C190 68nF/6.3V
DDR POWER For VTT/VREF
+3.3V
R101 10K/1%
R102 10K/1%
C192 0.01uF/16V
U10
REFIN
VLDOIN
VO
PGND
VOSNS
PWRGND
VIN
PGOOD
GND
EN
REFOUT
TPS51200DRCR
R103 100K
C191 4.7uF/10V
C193 0.1uF/25V
C194 4.7uF/10V
C195 10uF/25V
C196 100uF/6.3V
C197 10uF/25V
C198 10uF/25V
C199 4.7uF/10V
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Title
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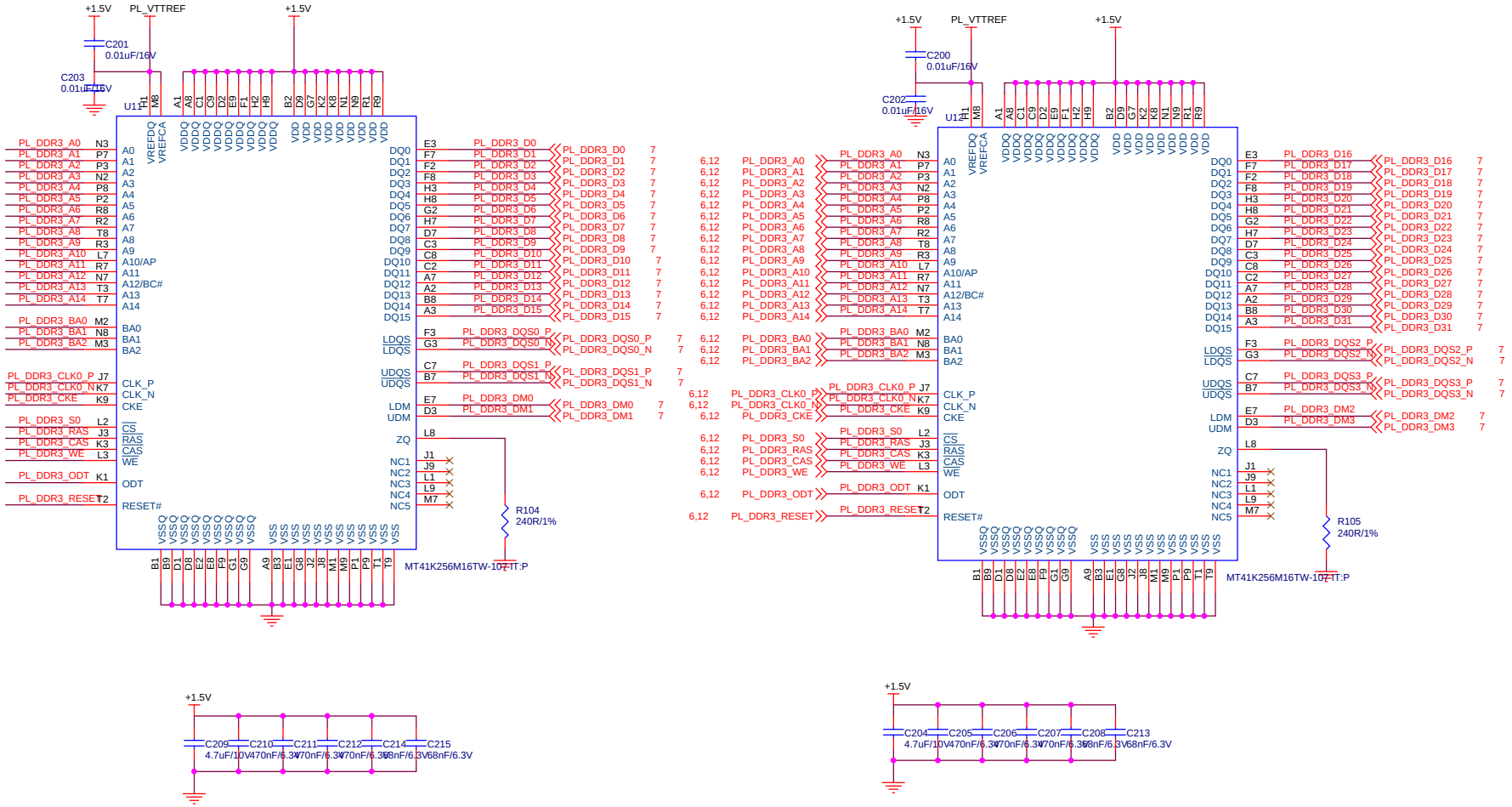

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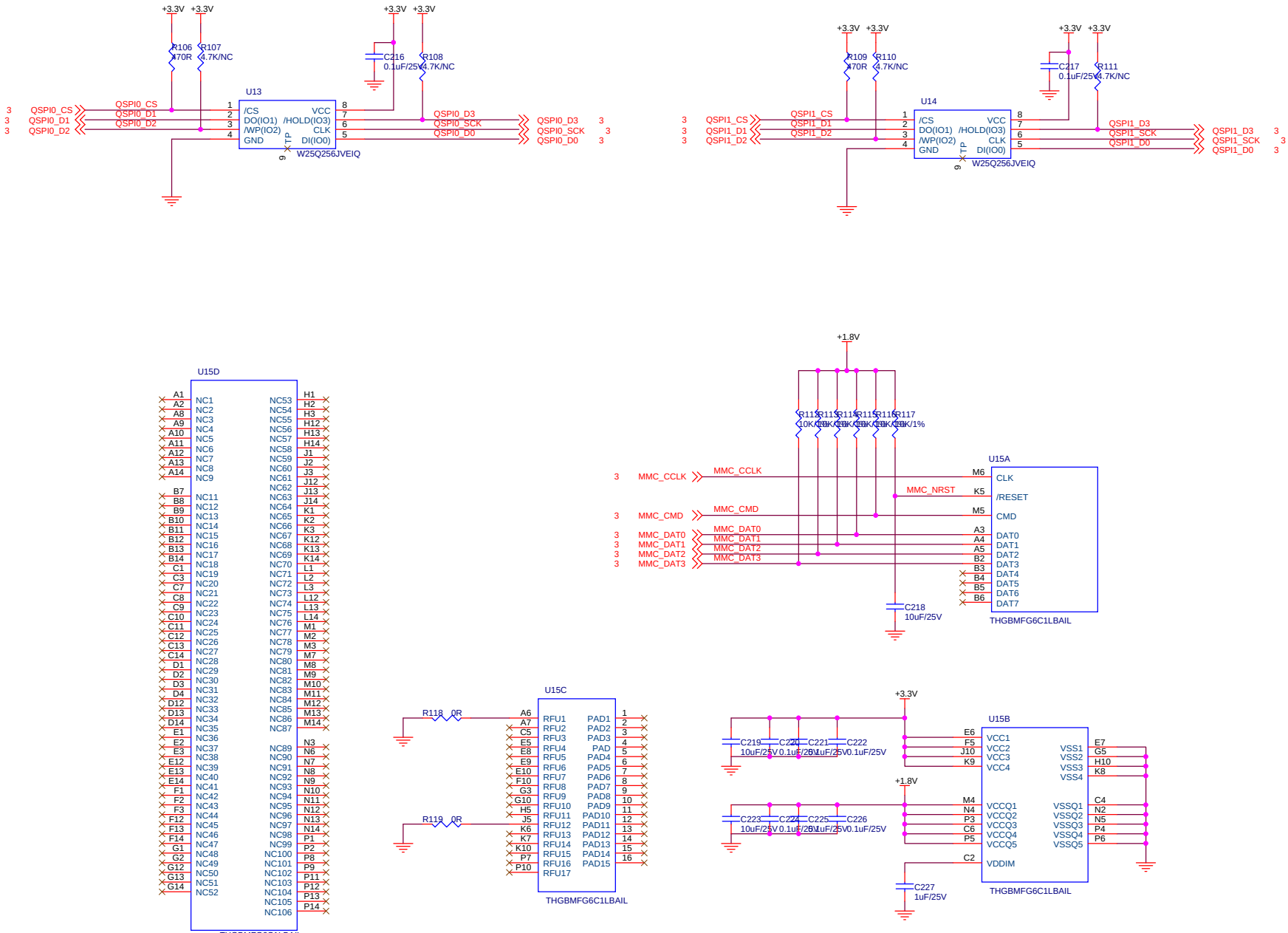

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Title	PAGE14 eMMC & QSPI FLASH
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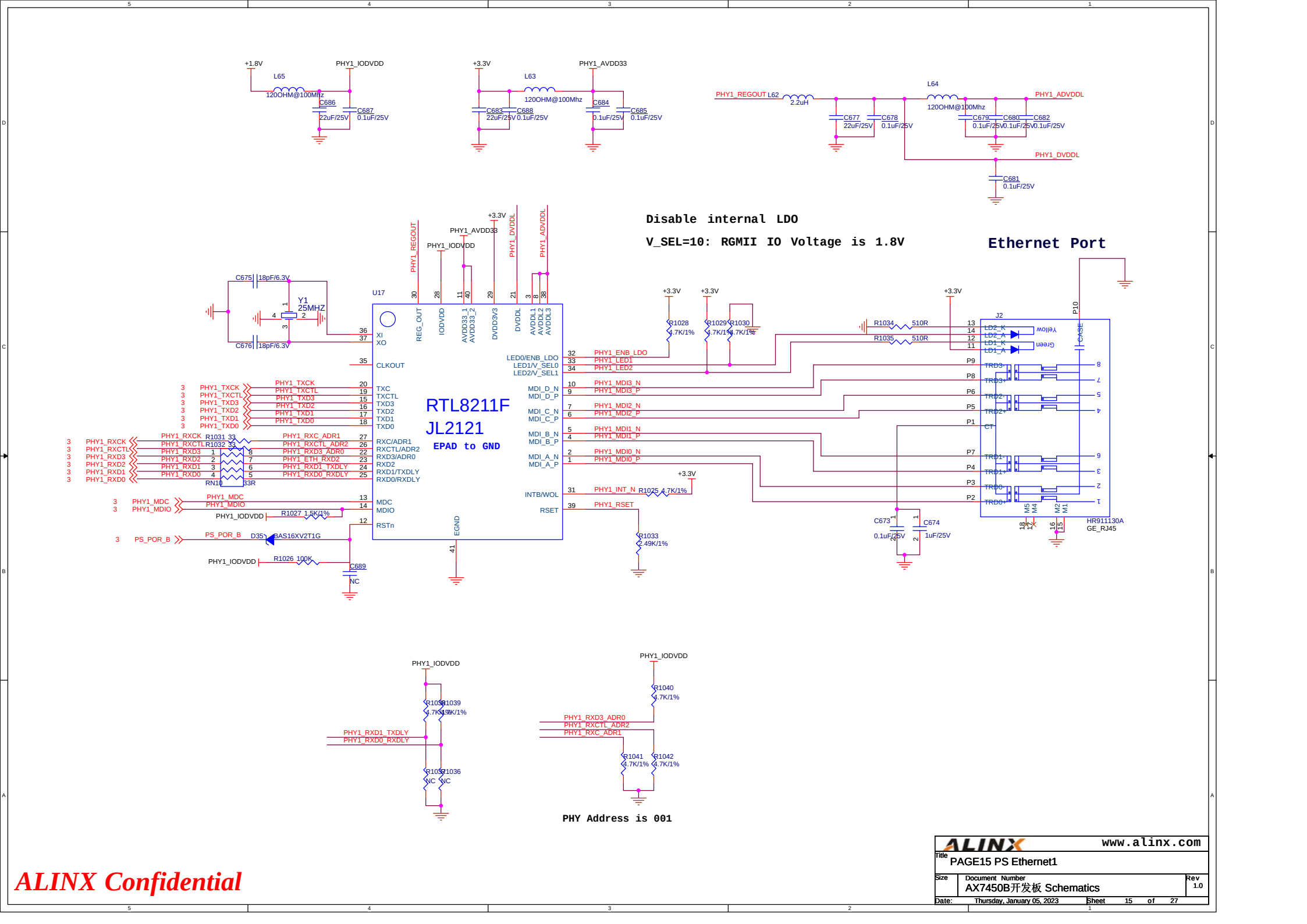
Disable internal LDO
V_SEL=10: RGMII IO Voltage is 1.8V
Ethernet Port
RTL8211F
JL2121
EPAD to GND
PHY Address is 001
HR911130A
GE_RJ45
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PAGE15 PS Ethernet1
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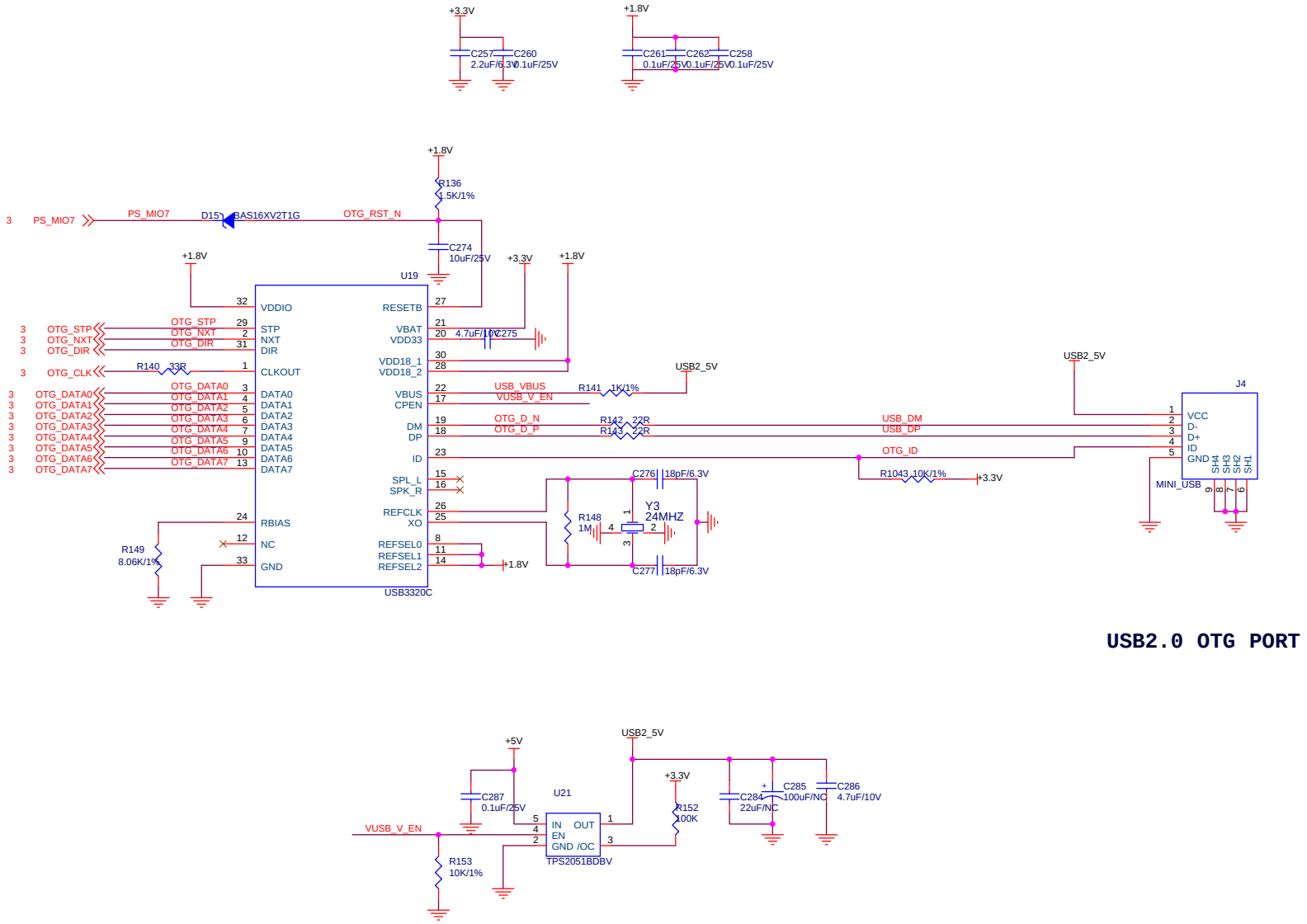

USB2.0 OTG PORT

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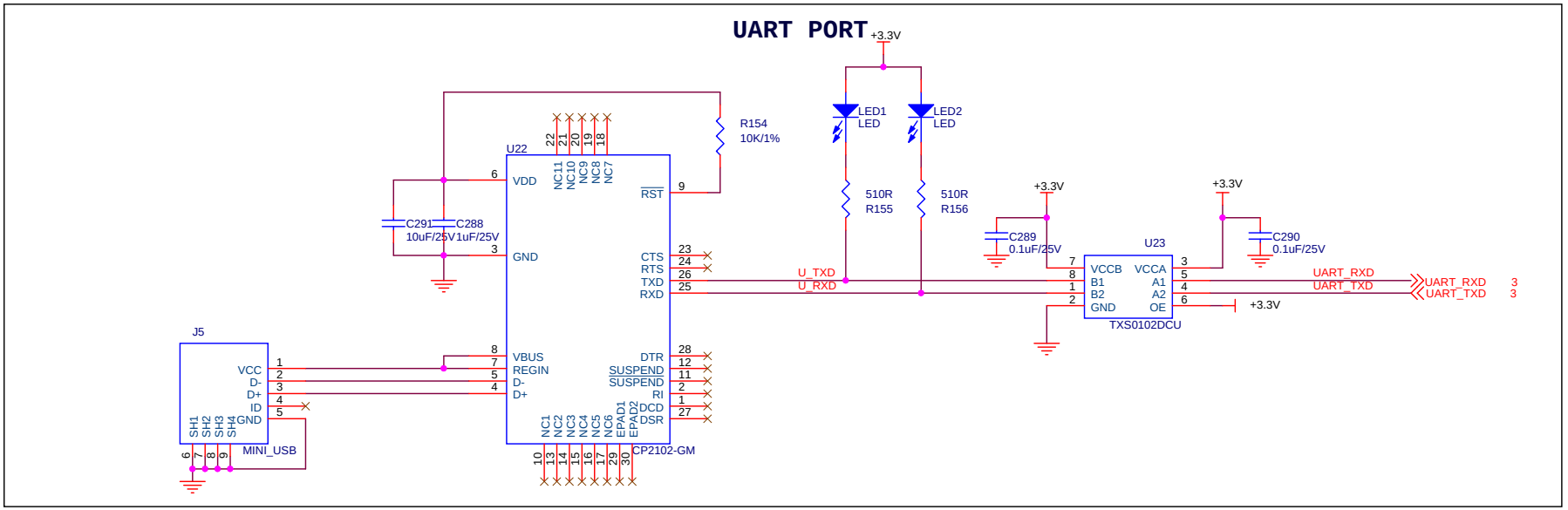

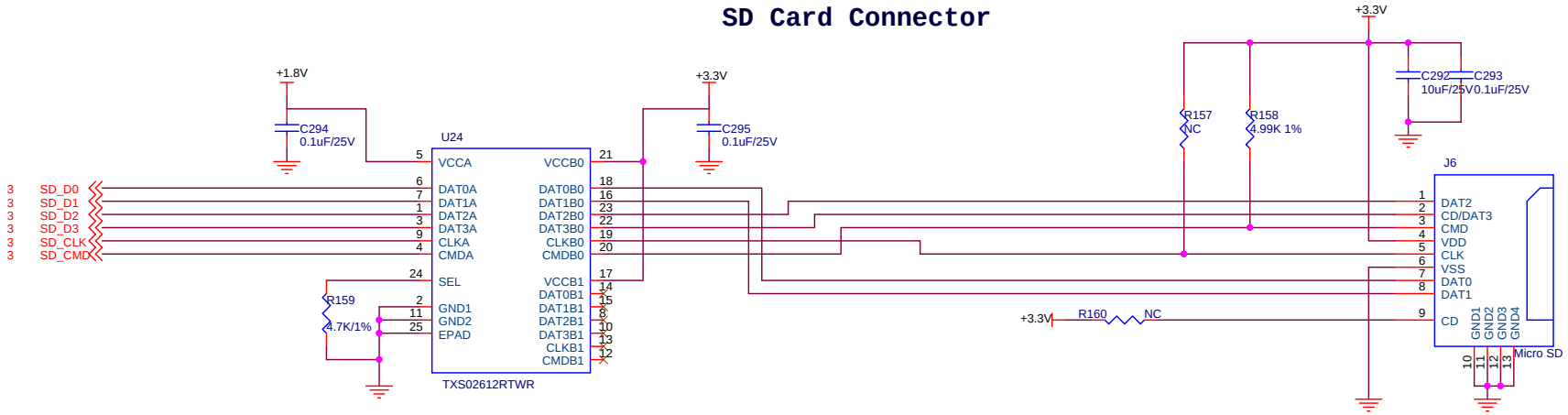

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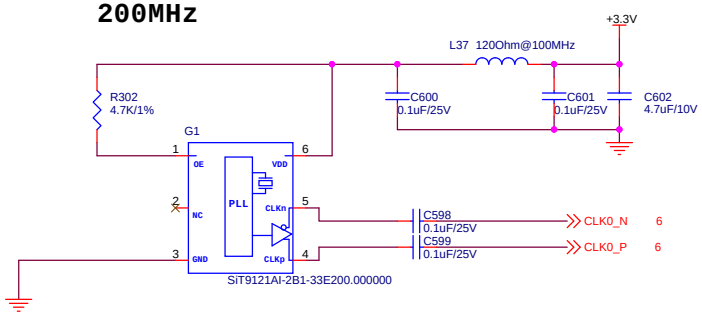
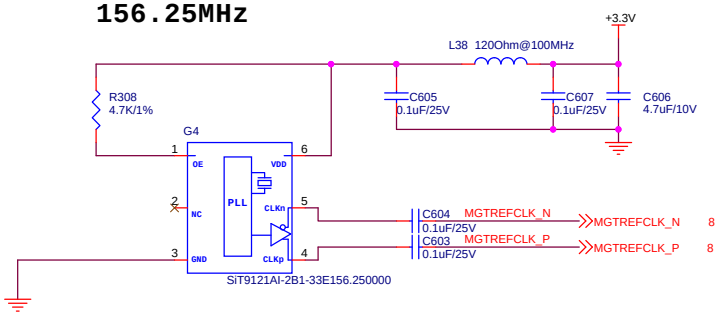
SYSTEM CLOCK

200MHz



156.25Mhz for GTX

156.25MHz



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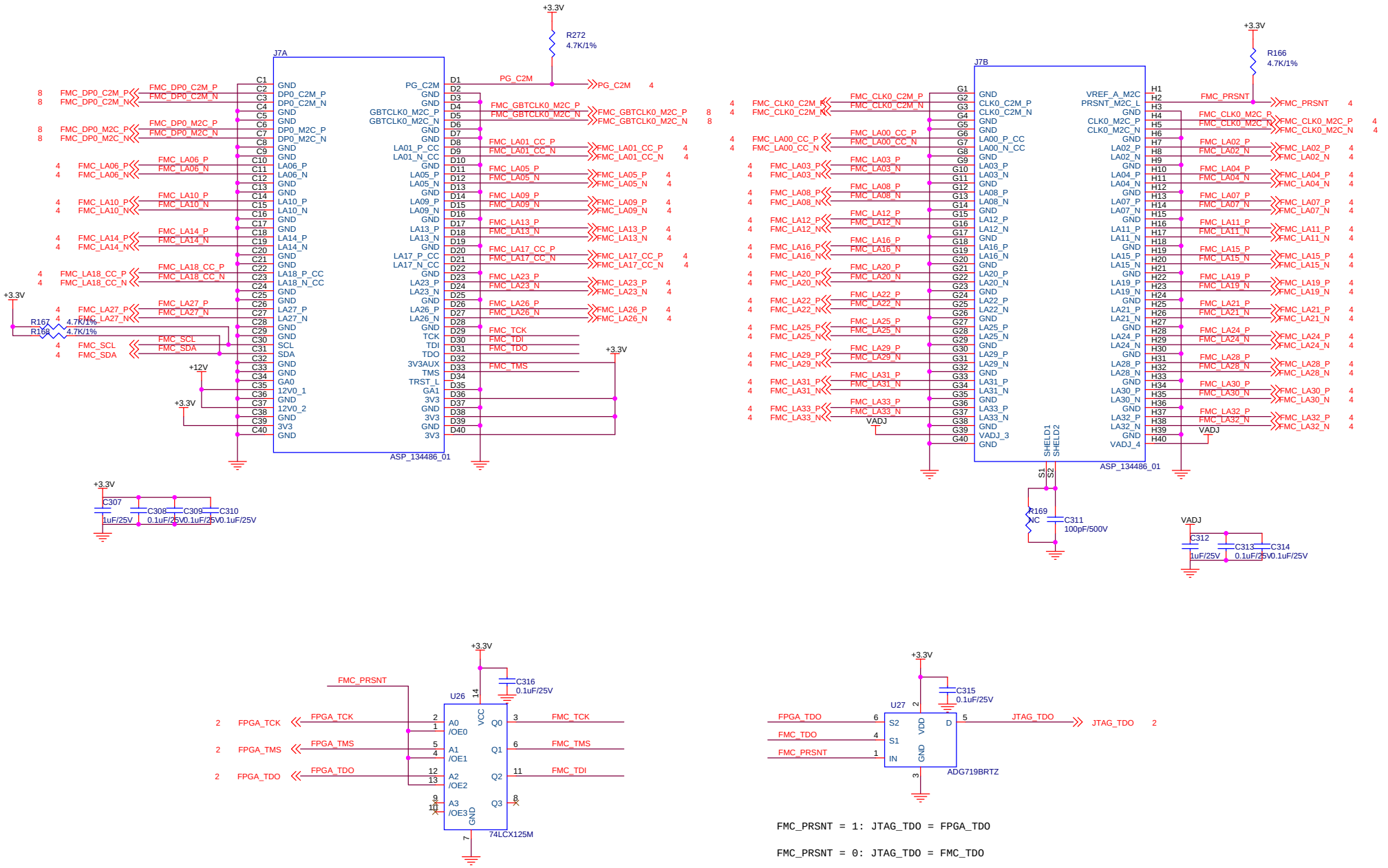

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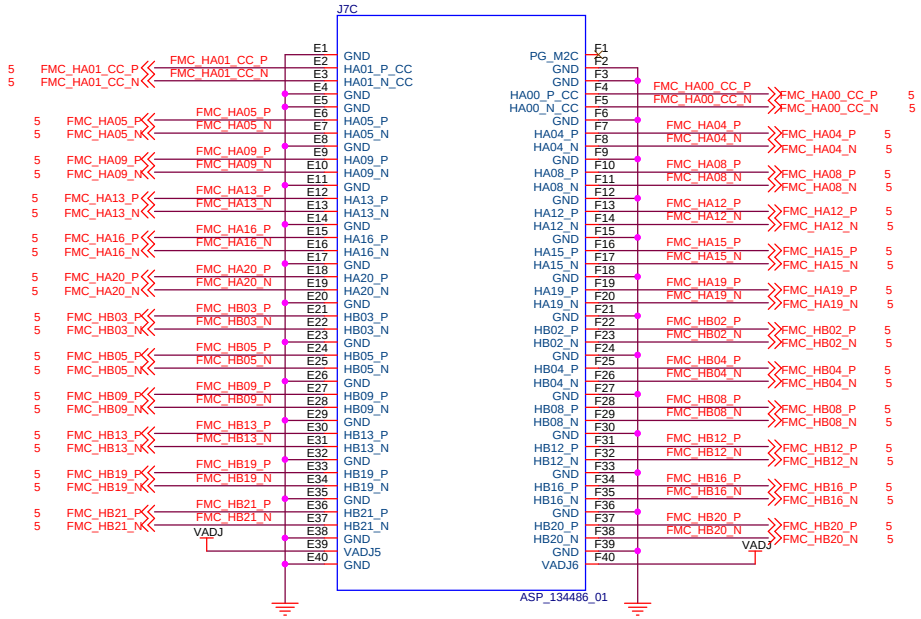

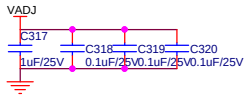

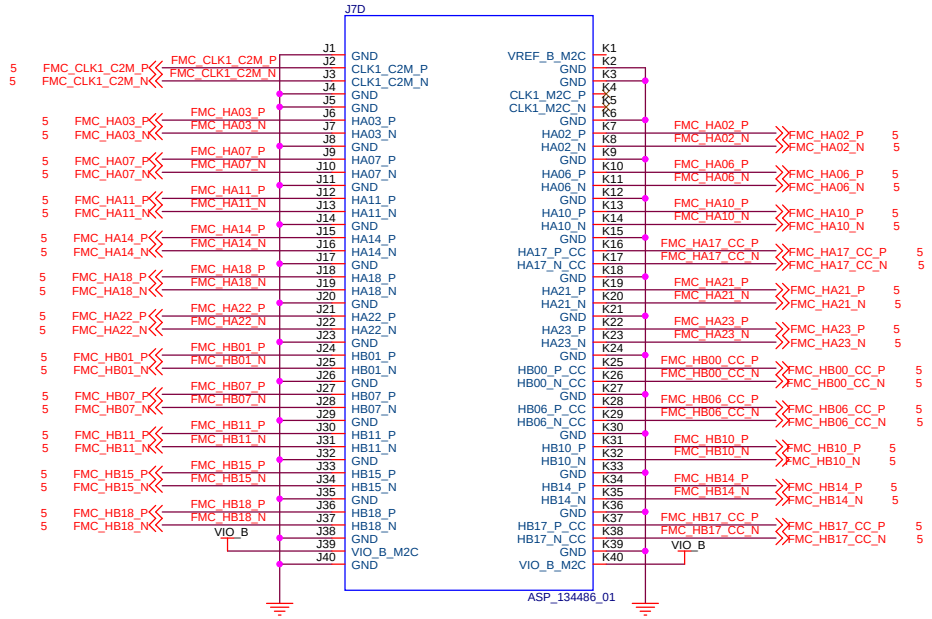

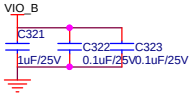

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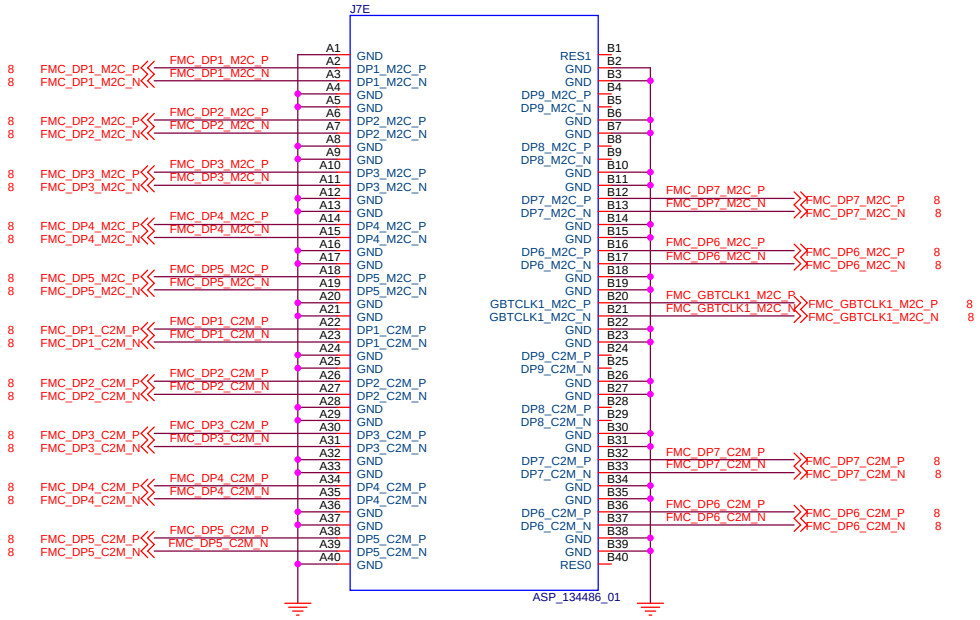

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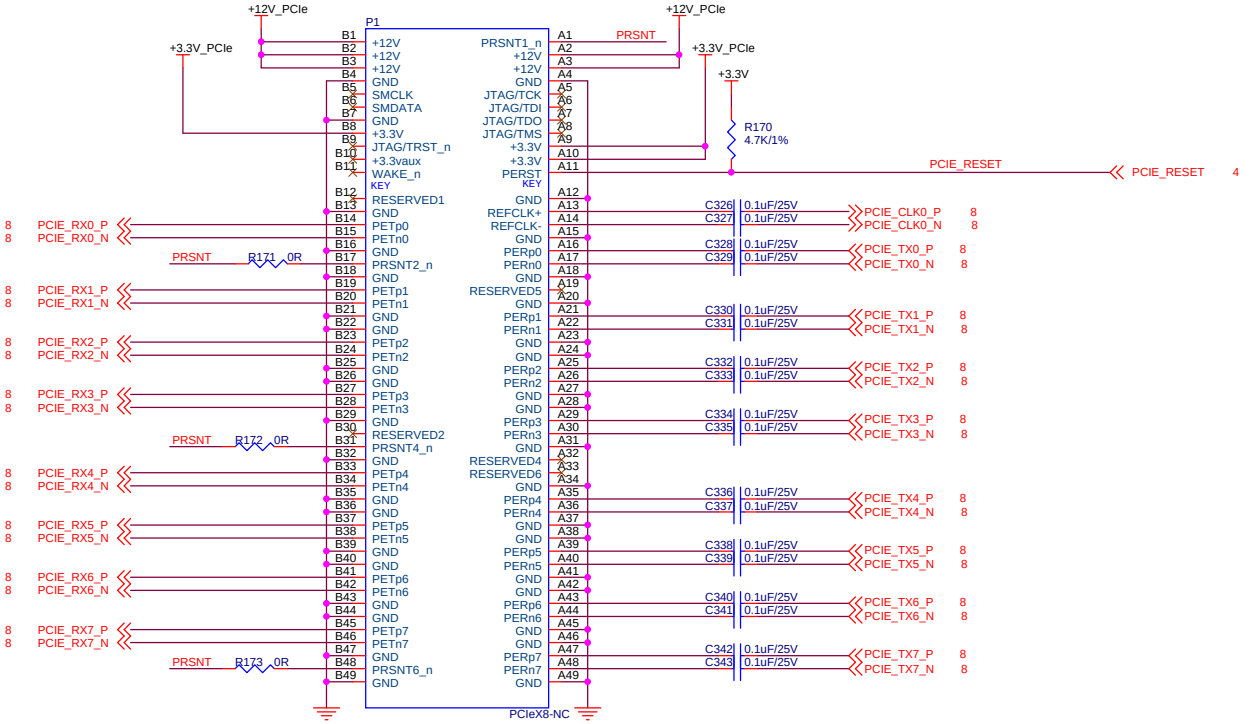
PCIE X8 SLOT



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Title: PAGE22 PCIEX8

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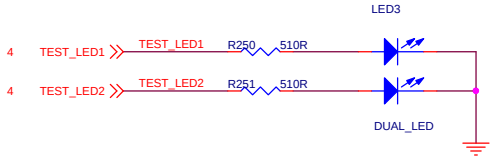

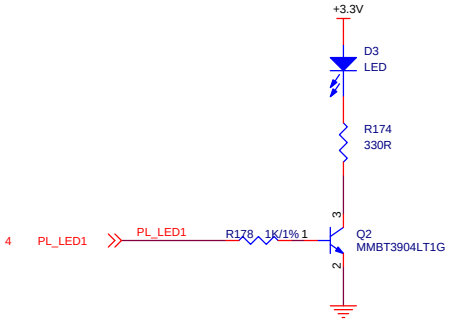

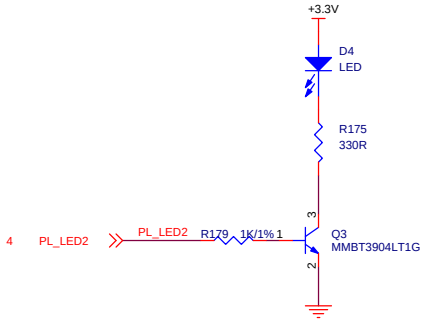

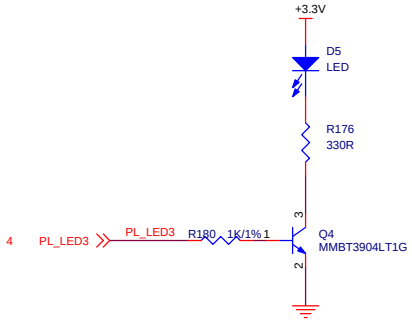

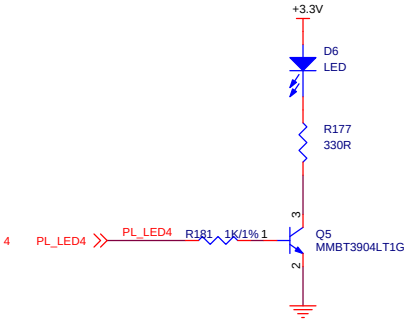

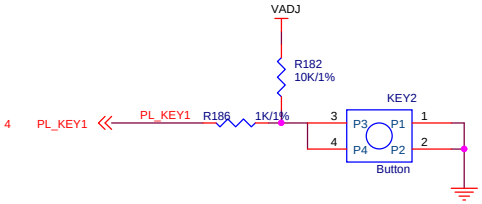

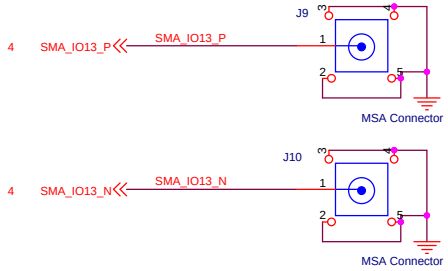

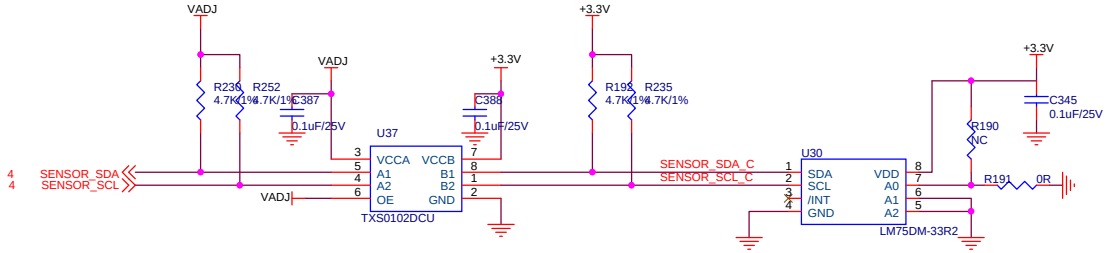

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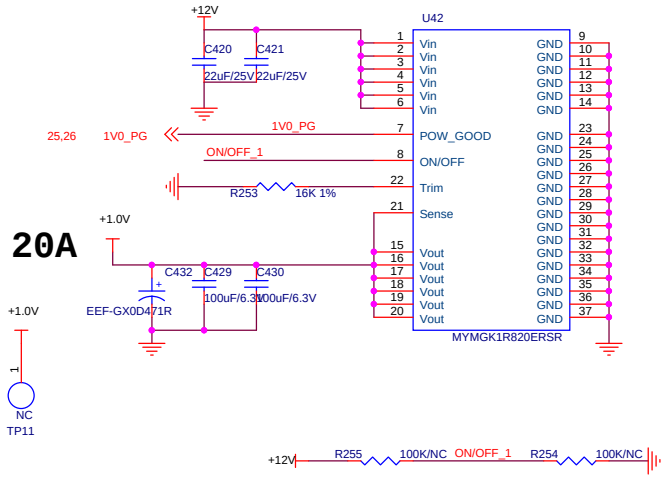
+1.0V 20A



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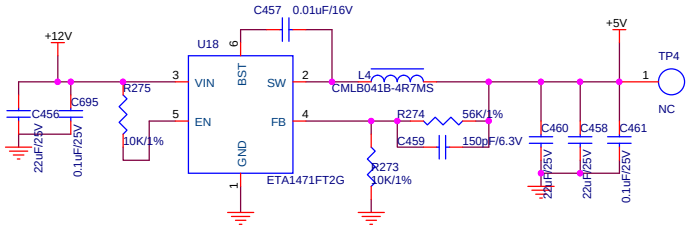
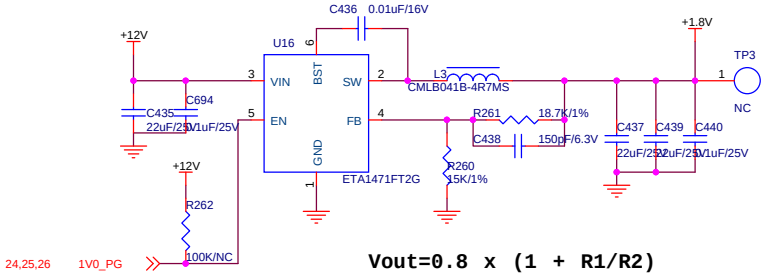


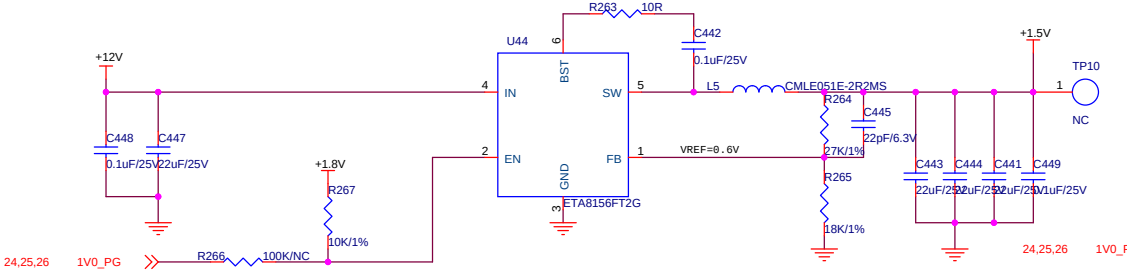
Vout=0.8 x (1 + R1/R2)



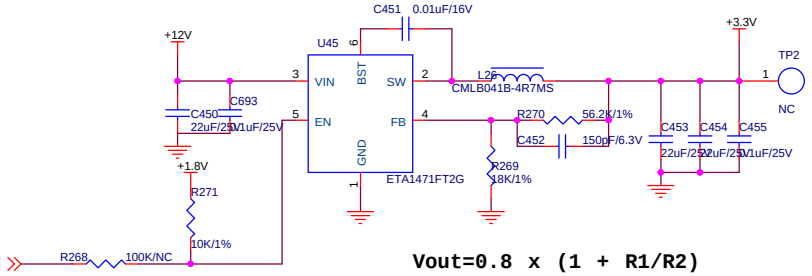
Vout=0.8 x (1 + R1/R2)

Vout=0.8 x (1 + R1/R2)

1.5V POWER 6A



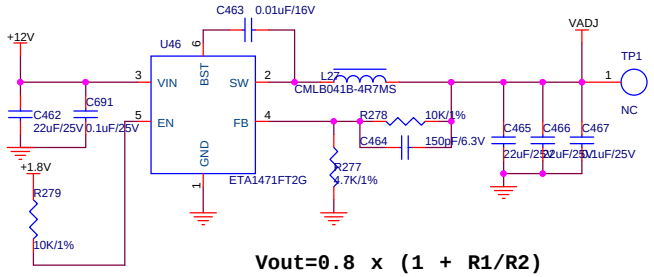
Vout=0.6 x (1 + R1/R2)



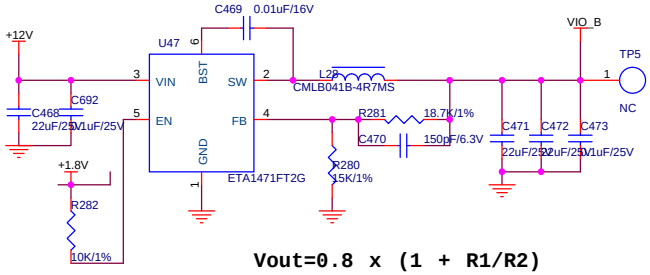
Vout=0.8 x (1 + R1/R2)

Default is 2.5V

Default is 1.8V

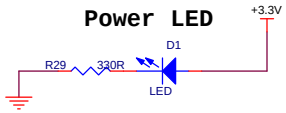


Vout=0.8 x (1 + R1/R2)



Vout=0.8 x (1 + R1/R2)

Power LED



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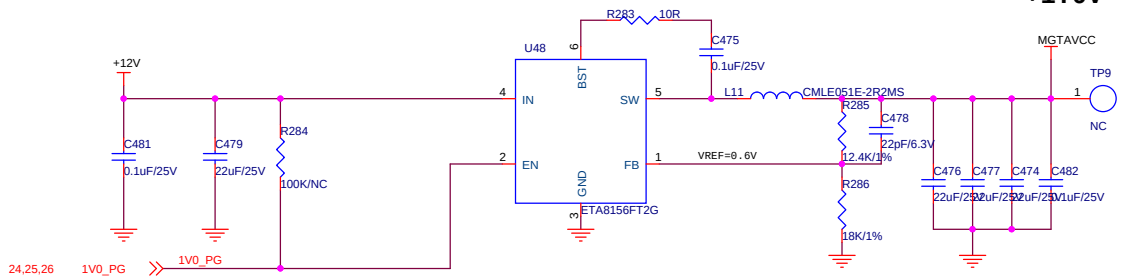
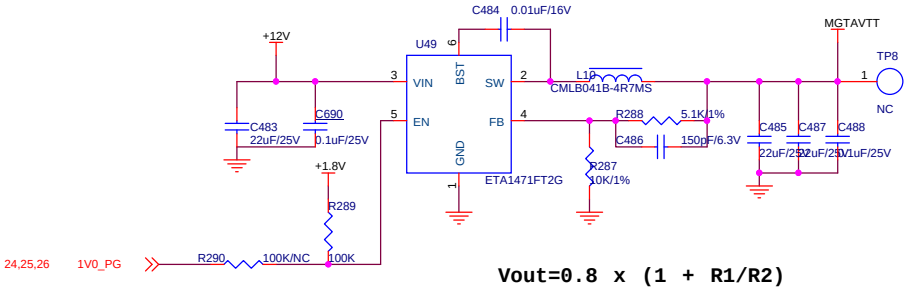
1.0V POWER 6A

+1.0V

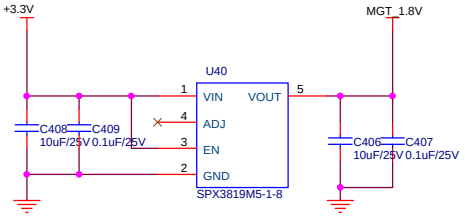


Vout=0.6 x (1 + R1/R2)

+1.2V



Vout=0.8 x (1 + R1/R2)



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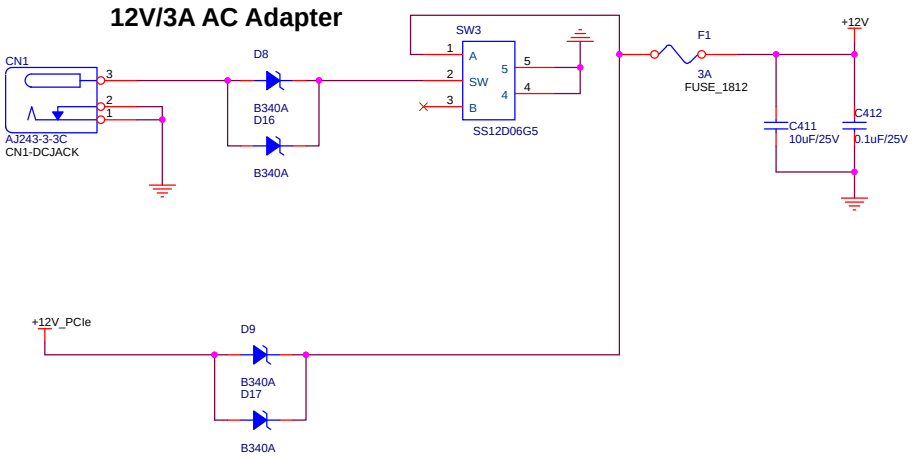

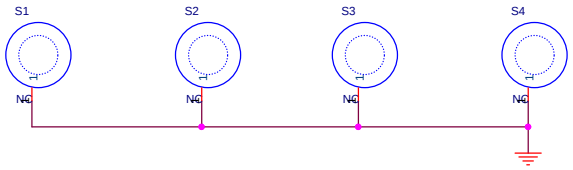

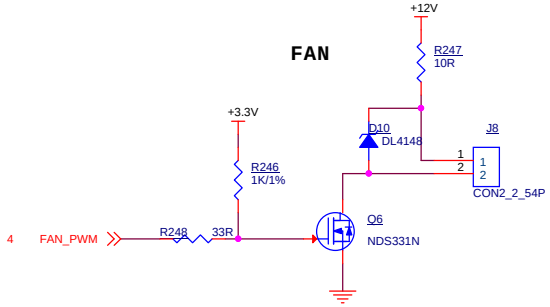

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