REV	Description	Date
V1.0	First Release	2019-6-21

AC7Z010/AC7Z020 Schematics
ZYNQ硬件平台

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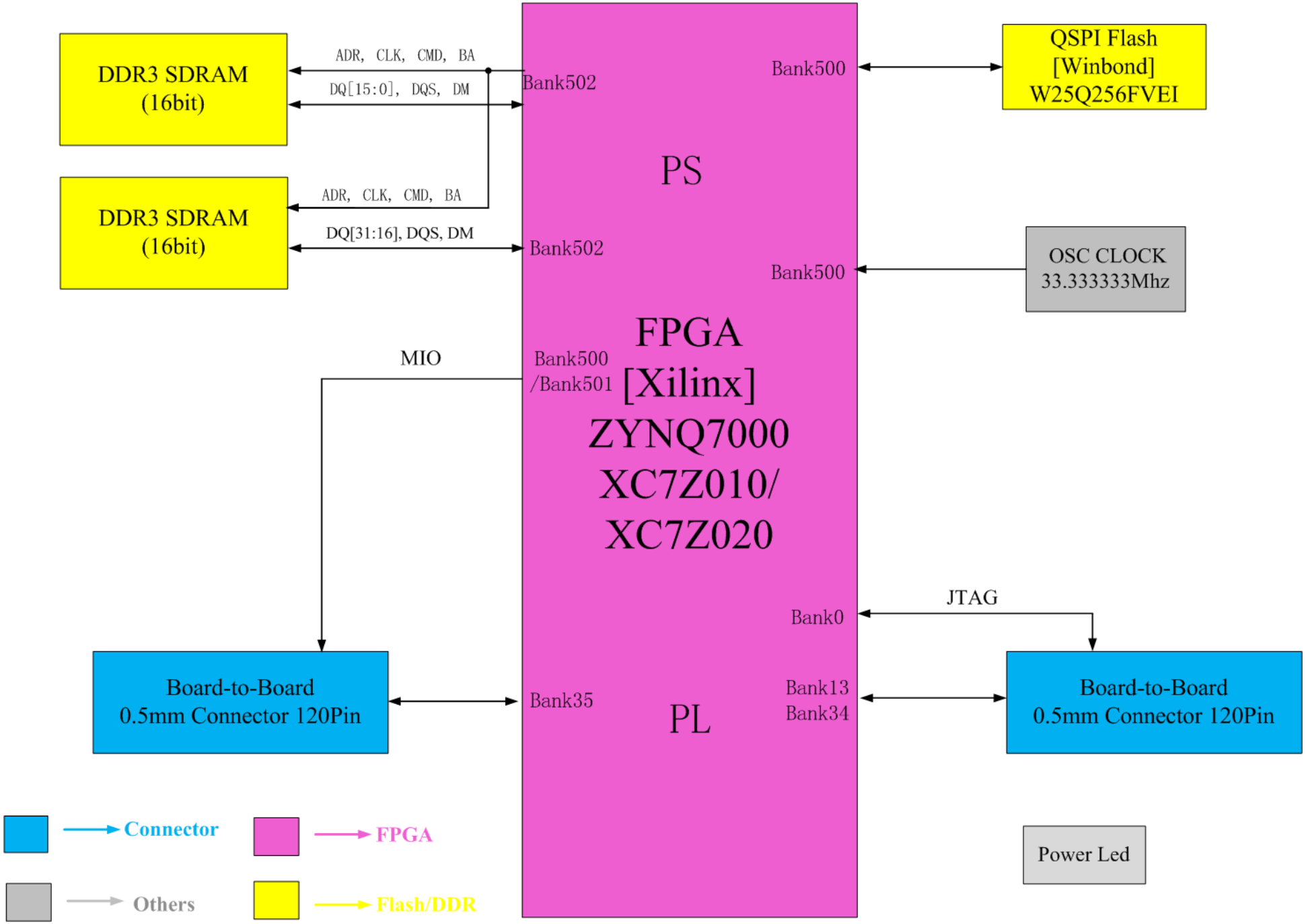
ALINX

Title: Zynq-7000 Cover Page

Size | Document Number: AC7Z010/AC7Z020 核心板原理图 | Rev: 1.0

Date: Wednesday, August 21, 2019 | Sheet 1 of 13



ALINX		
Title	Zynq-7000 Block diagram	
Size	Document Number: AC7Z010/AC7Z020 核心板原理图	Rev: 1.0
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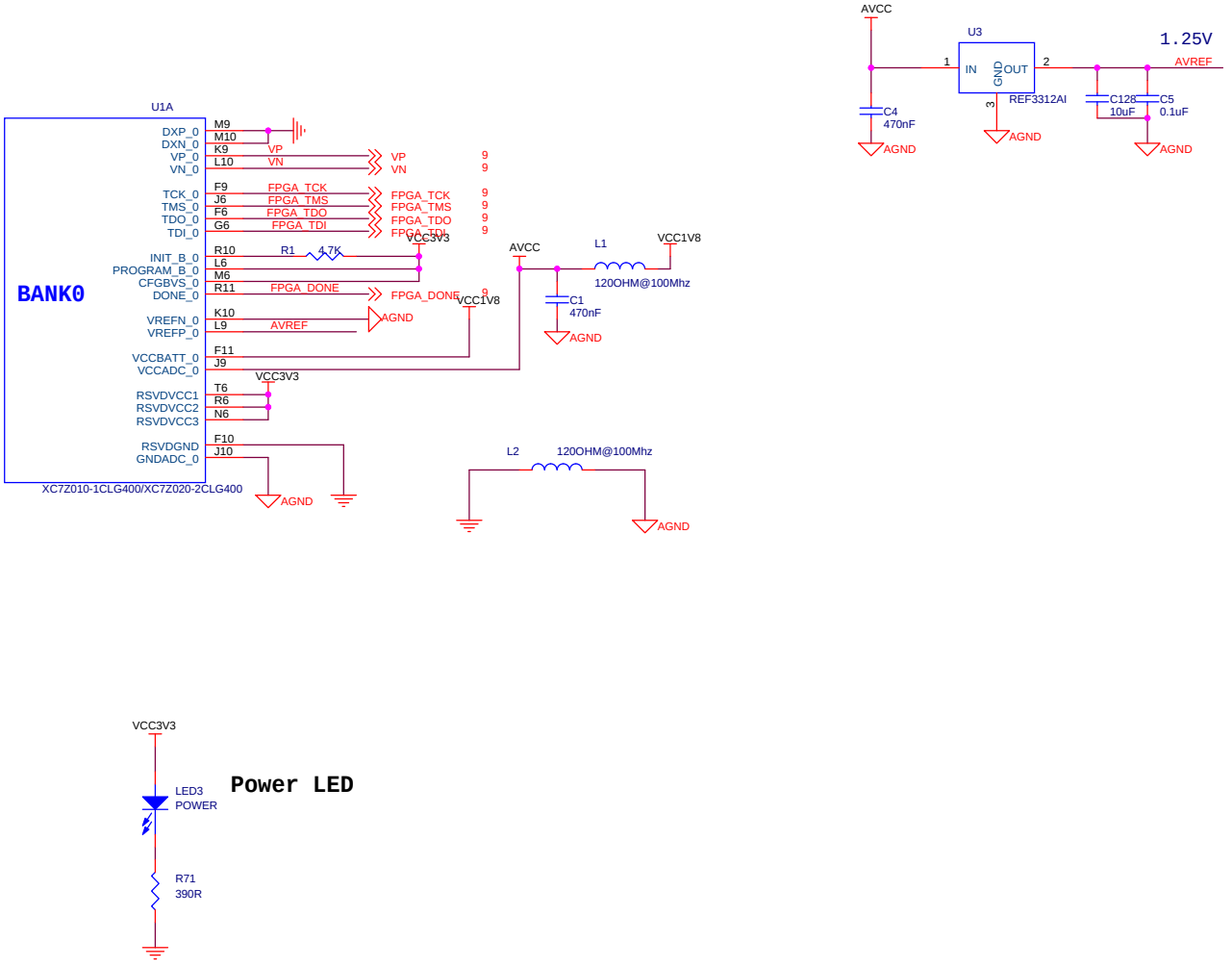

Power LED

Title	Zynq-7000 JTAG & Bank0	
Size	Document Number: AC7Z010/AC7Z020 核心板原理图	Rev: 1.0
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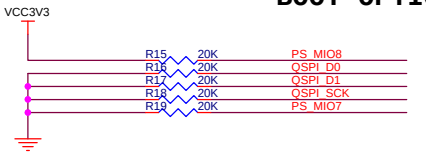
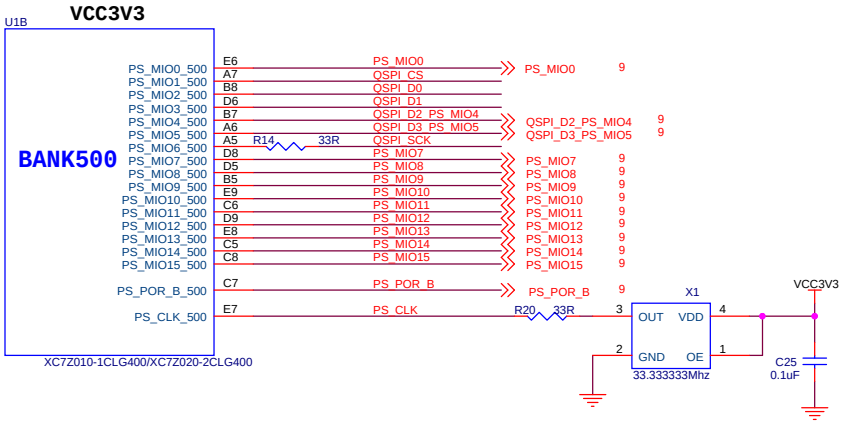
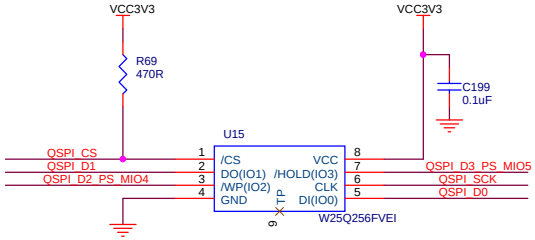
BOOT OPTION

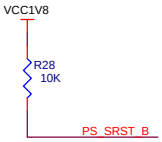


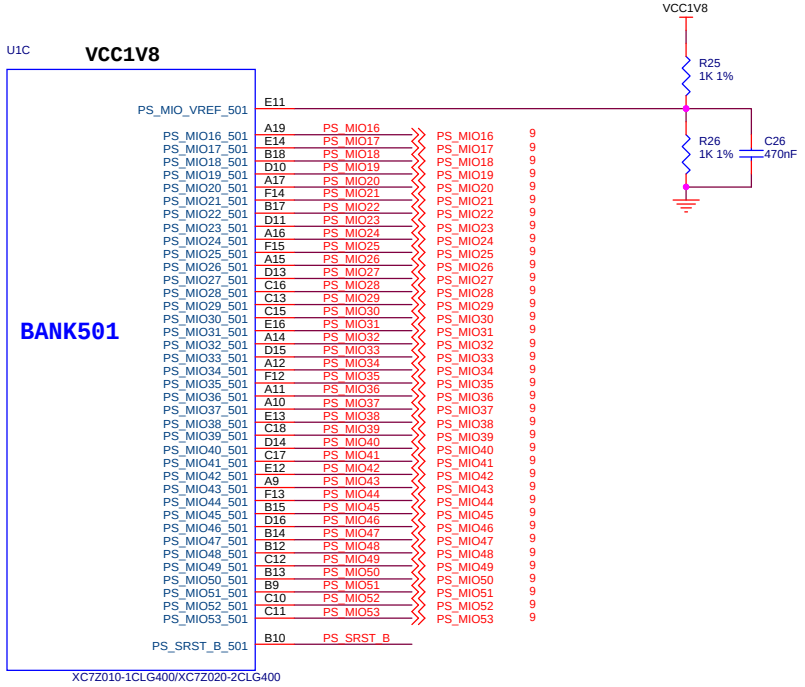

```
MIO[8] =1 ----MIO bank501 voltage=1.8V
MIO[2] =0 ----cascaded JTAG
MIO[3] =0 ----JTAG/NAND/Quad-SPI/SD
MIO[6] =0 ----PLL used
MIO[7] =0 ----MIO bank0 voltage=3.3V
```





QSPI FLASH





Title	Zynq-7000 PS MIO	
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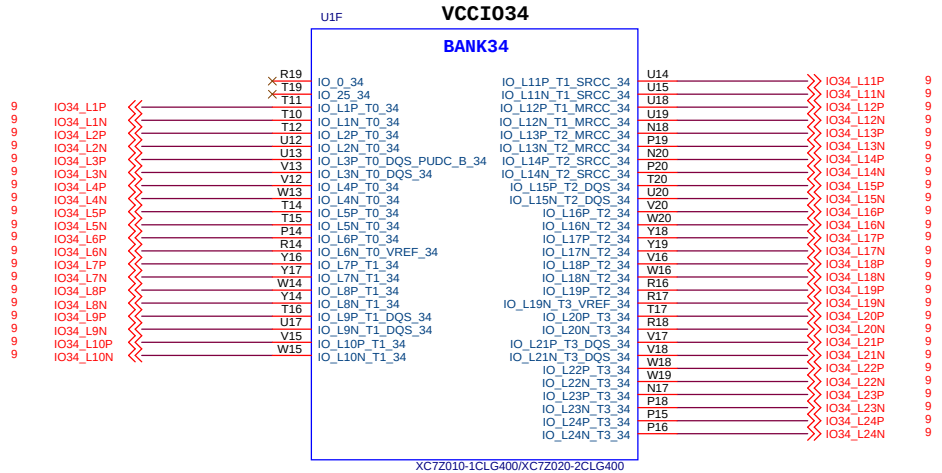

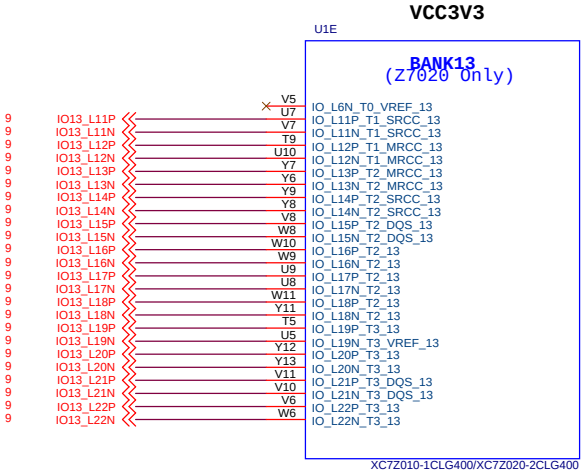

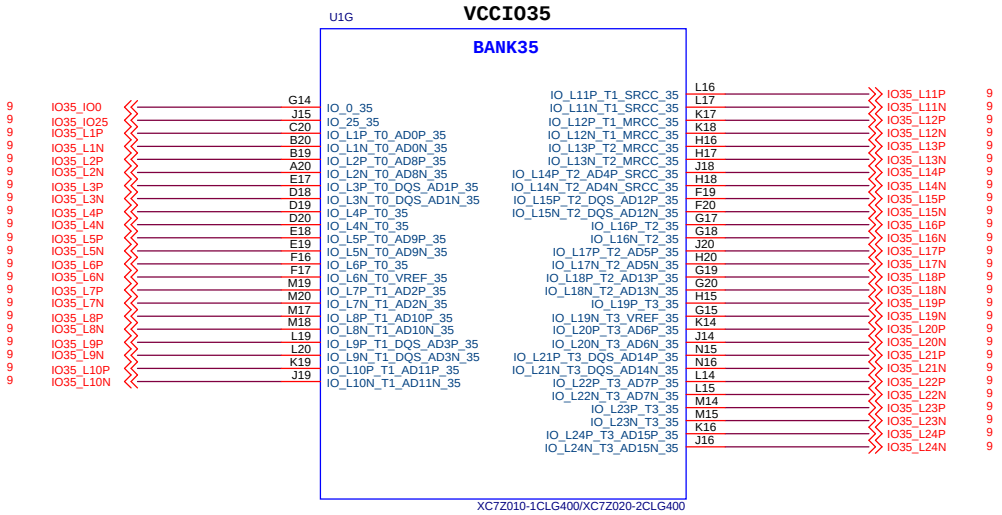

ALINX

Title: Zynq-7000 Bank13 & 34 & 35

Size	Document Number	Rev
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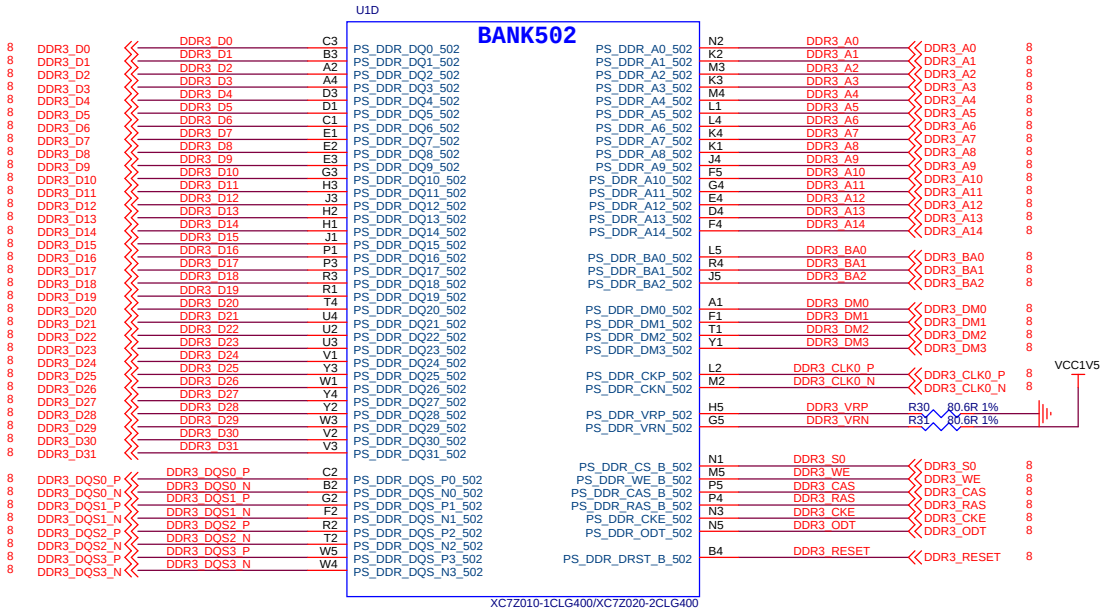

Title	Zynq-7000 Bank502
Size	
Document Number	AC7Z010/AC7Z020 核心板原理图
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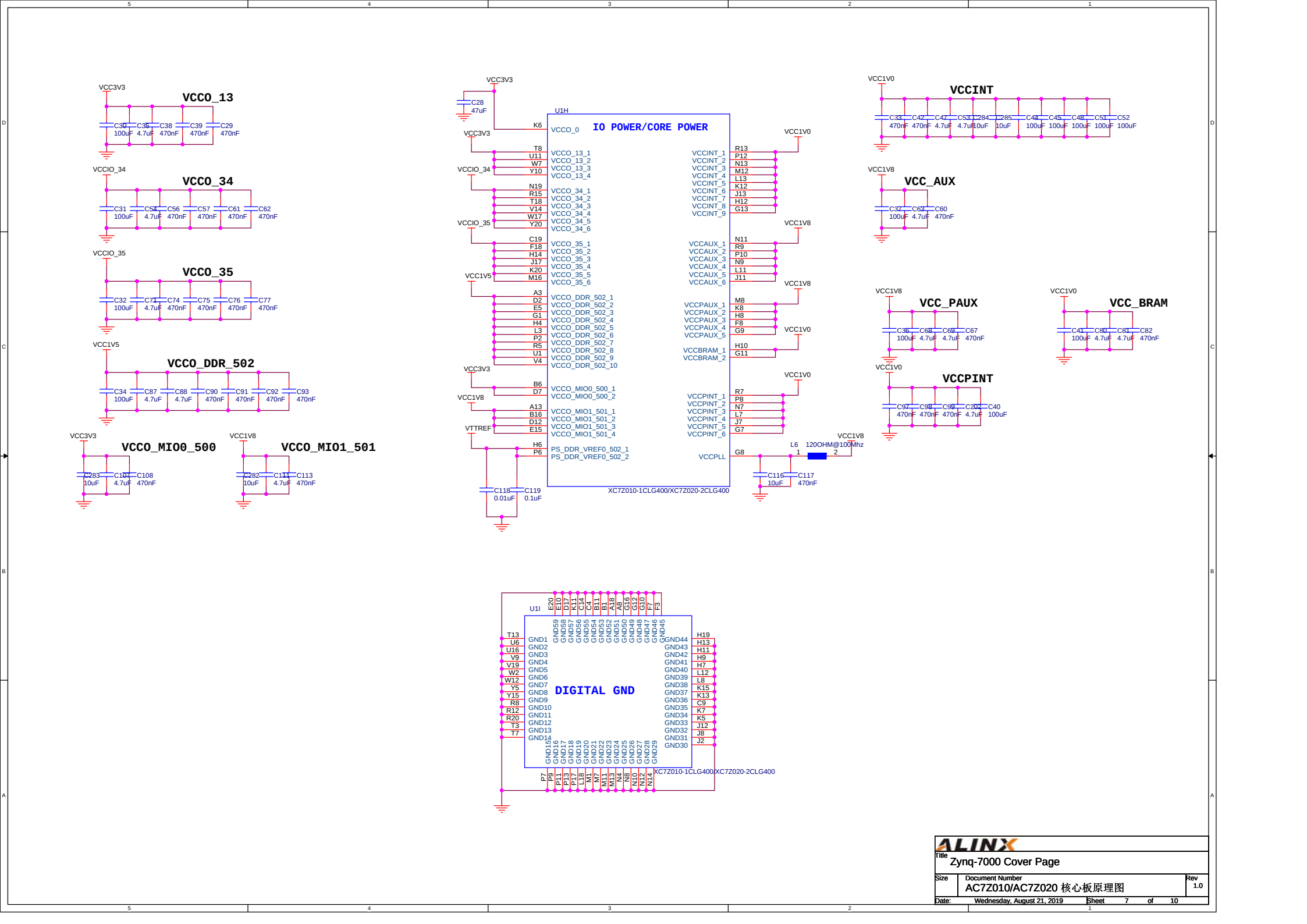
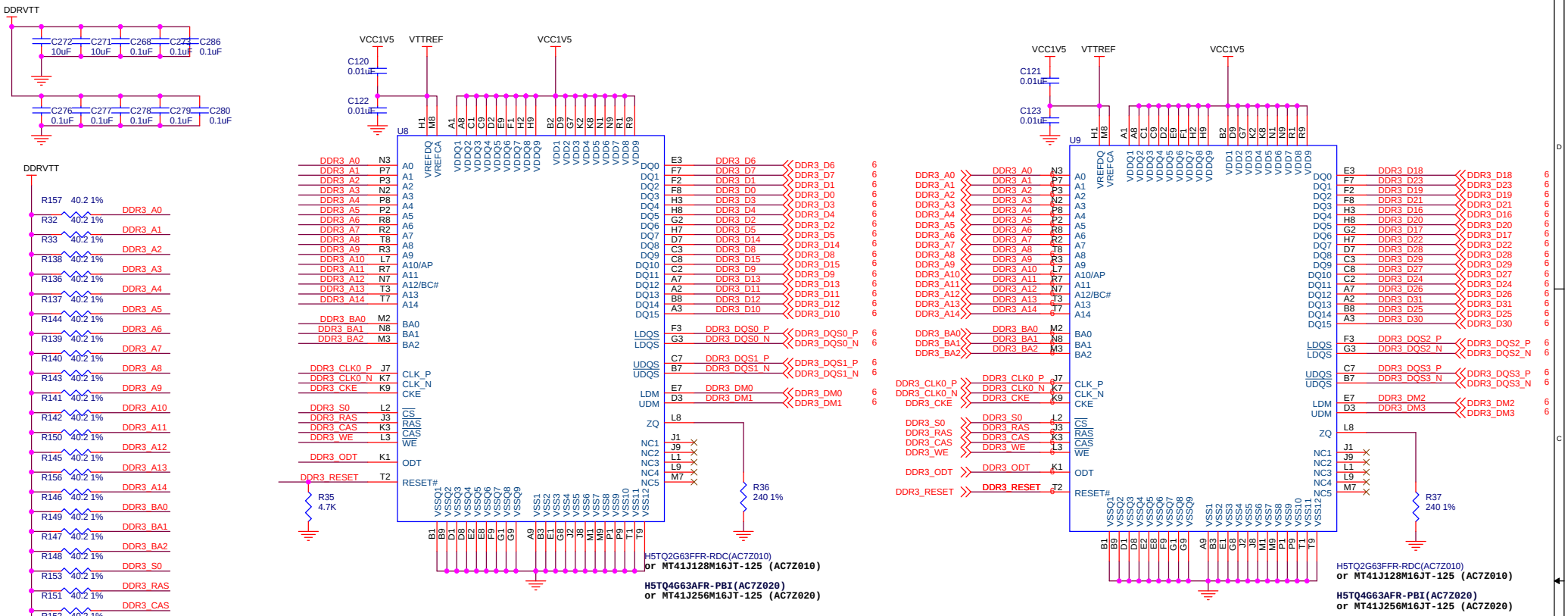
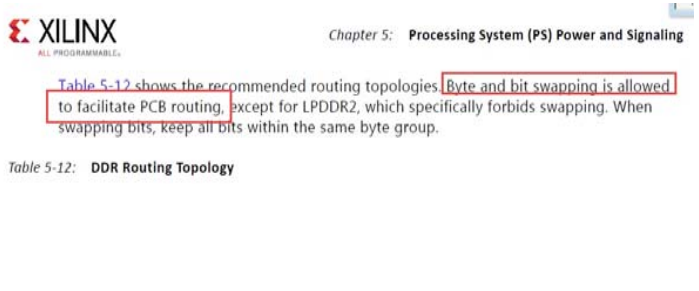


Title	Zynq-7000 Cover Page	
Size	Document Number: AC7Z010/AC7Z020 核心板原理图	Rev: 1.0
Date: Wednesday, August 21, 2019	Sheet 7 of 10	



为了PCB走线方便，DDR3数据线组内（DQS除外）可以任意交换。
XILINX 的UG933文档的PAGE66有以下说明：

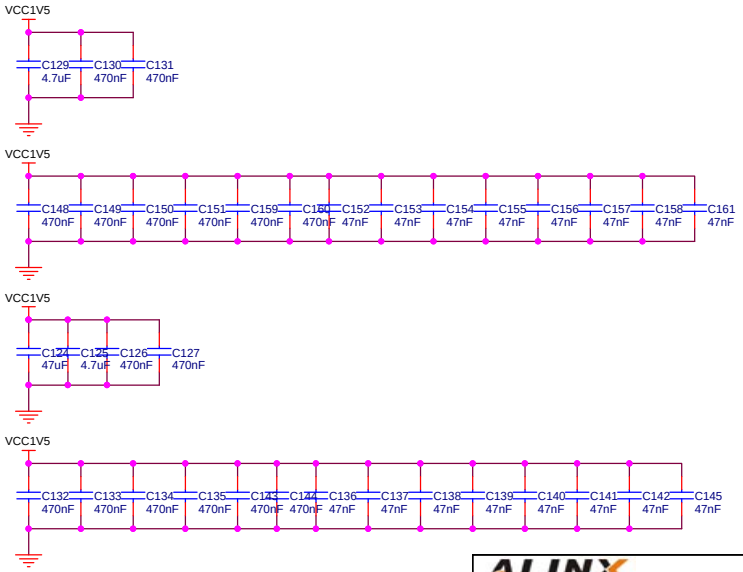


XILINX
ALL PROGRAMMABLE.

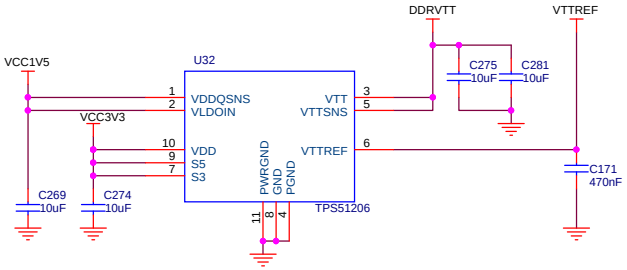
Chapter 5: **Processing System (PS) Power and Signaling**

Table 5-12 shows the recommended routing topologies. Byte and bit swapping is allowed to facilitate PCB routing, except for LPDDR2, which specifically forbids swapping. When swapping bits, keep all bits within the same byte group.

Table 5-12: **DDR Routing Topology**



DDR POWER For VTT/VREF



Title	Zynq-7000 DDR		
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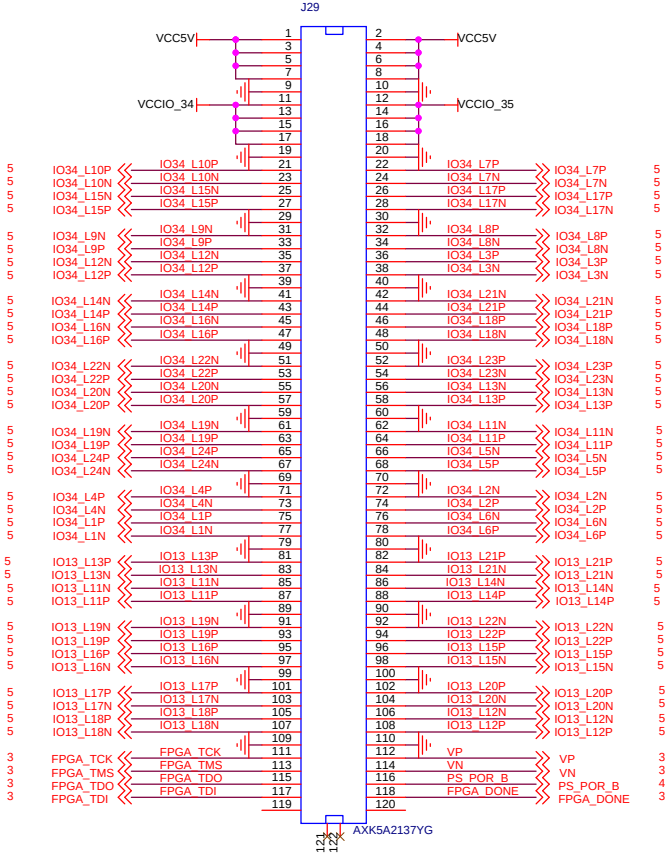
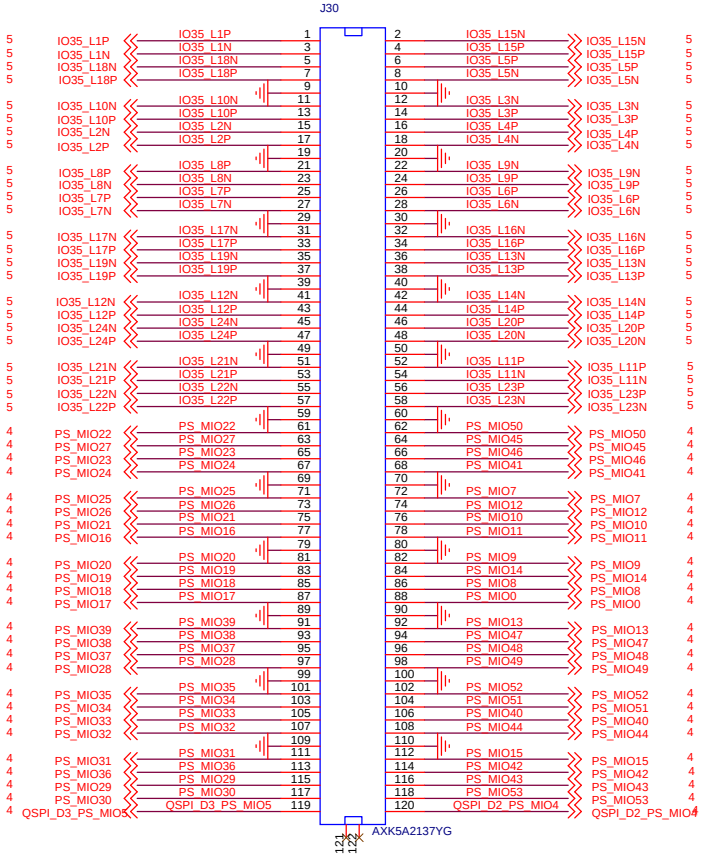
VCCIO34，VCCIO35的电源由底板提供，不能超过3.3V，上电顺序要求5V先供电，然后再供VCCIO34和VCCIO35





BANK13的IO管脚只有AC7Z020的板子才有， AC7Z010的核心板无法使用这些IO

PS_MIO0,MIO7~15为3.3V电平标准
PS_MIO16~53为1.8V电平标准

ALINX		
Title: Zynq-7000 LED & KEY & IO		
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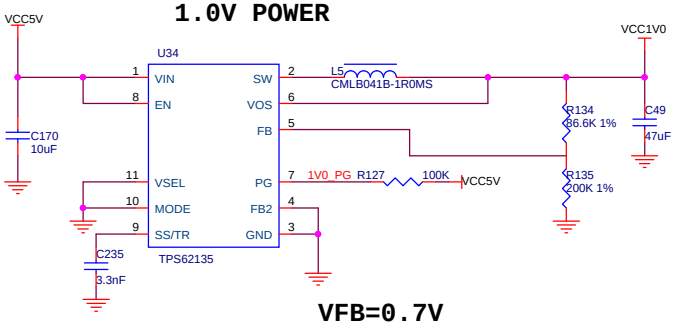
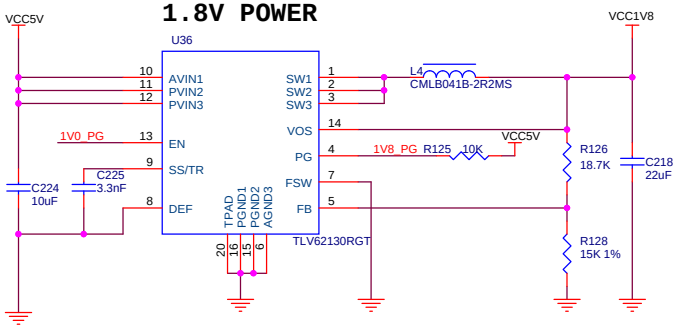
1.0V POWER

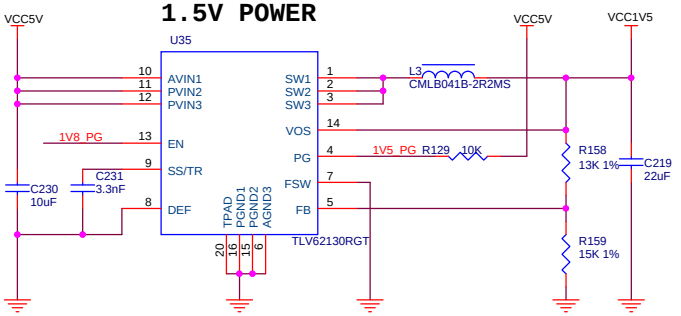


VFB=0.7V

1.8V POWER

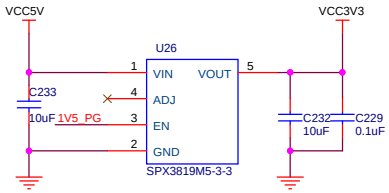


1.5V POWER



Power On Sequnce:

1.0V -> 1.8V -> 1.5 V -> 3.3V -> VCCIO



Title	Power	
Size	Document Number: AC7Z010/AC7Z020 核心板原理图	Rev: 1.0
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