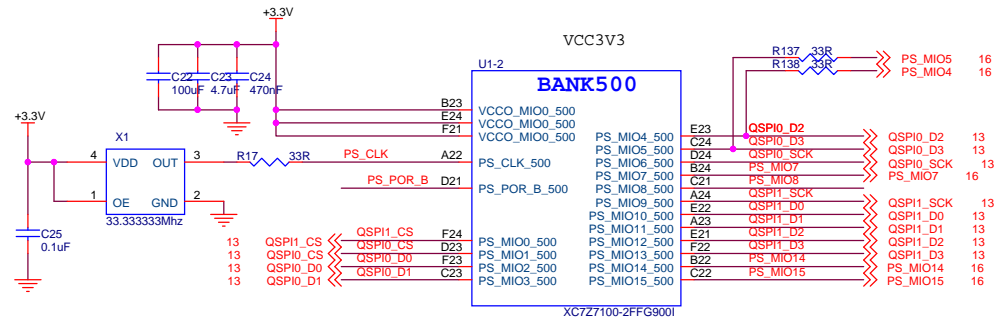


BOOT OPTION

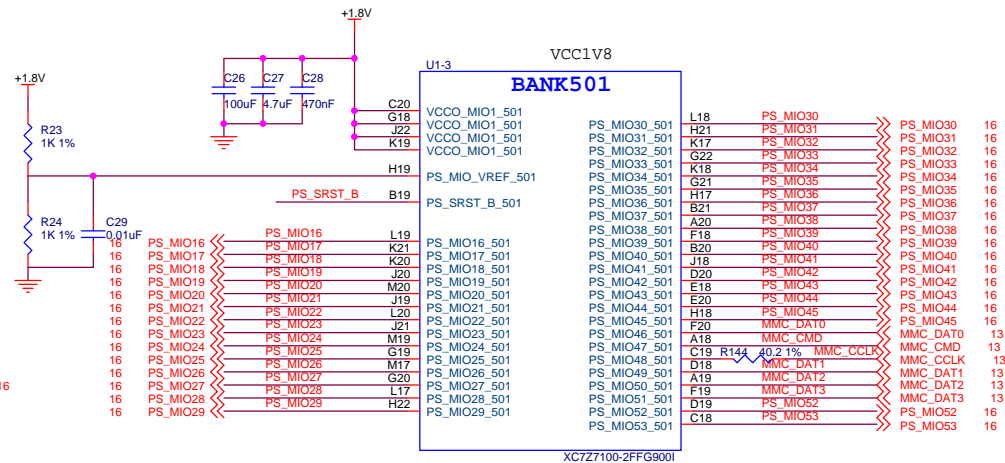
MIO[8]	=1	---MIO bank1 voltage=1.8V
MIO[2]	=0	---cascaded JTAG
MIO[3]	=0	---JTAG/NAND/Quad-SPI/SD
MIO[6]	=0	---PLL used
MIO[7]	=0	---MIO bank0 voltage=3.3V

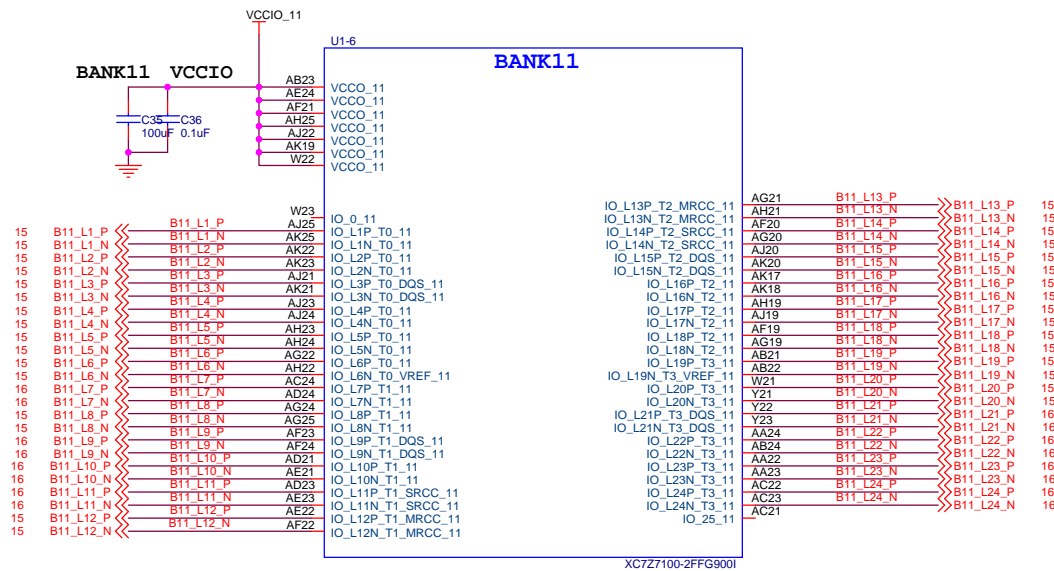
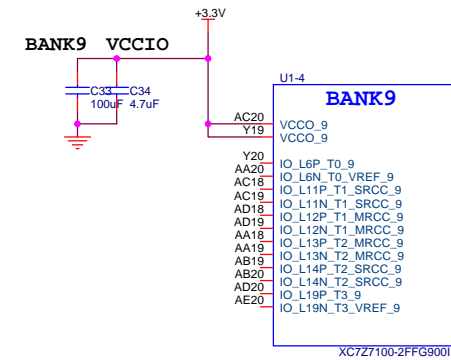
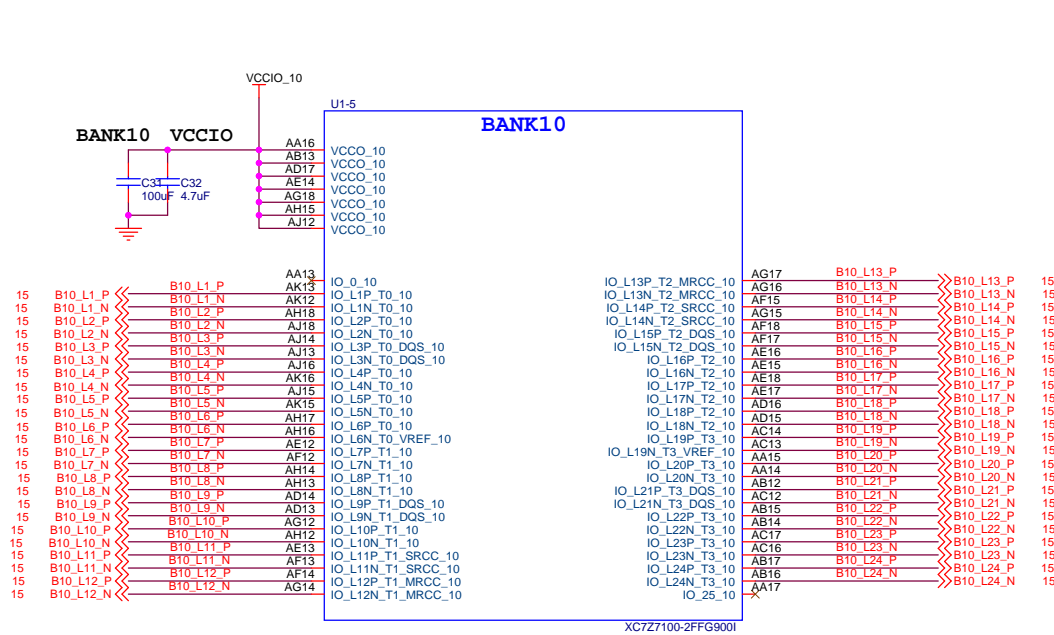


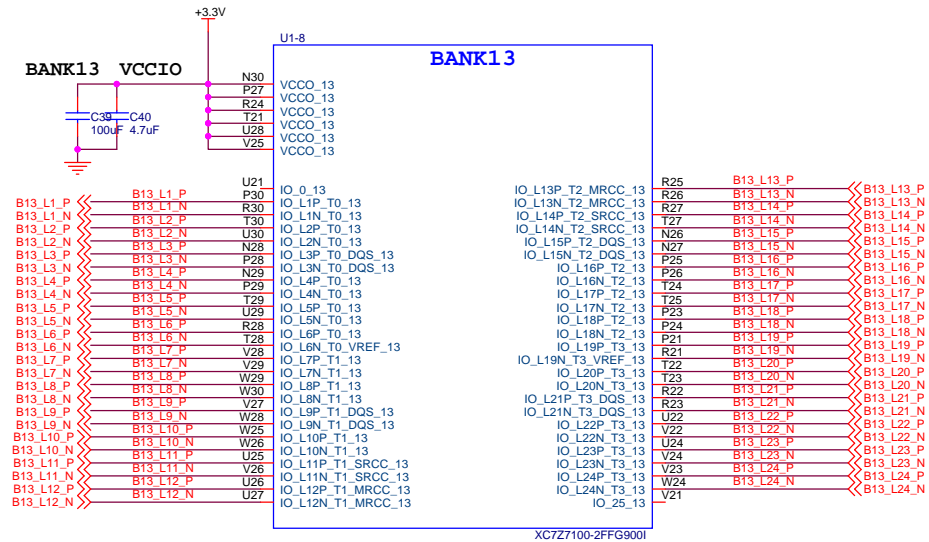
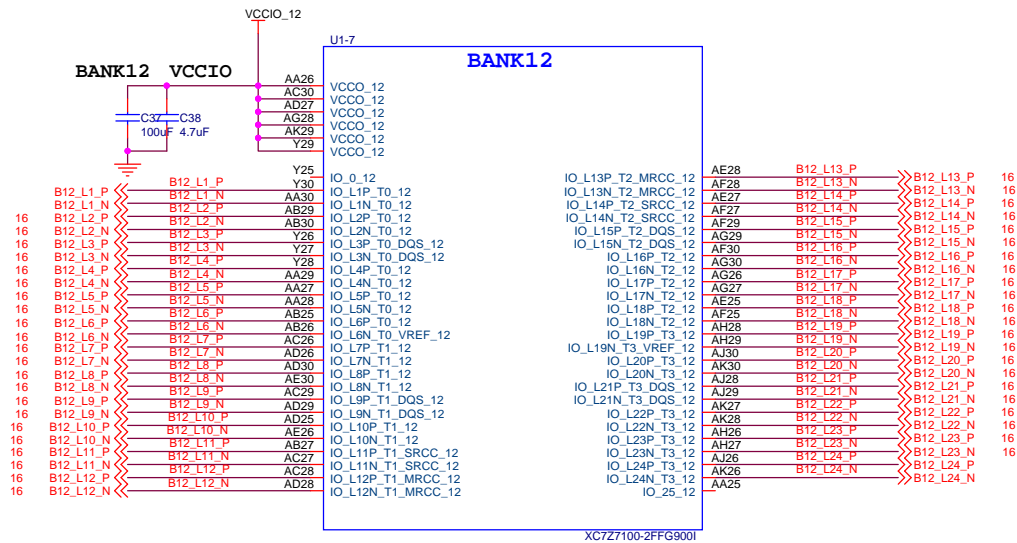
POWER ON RESET

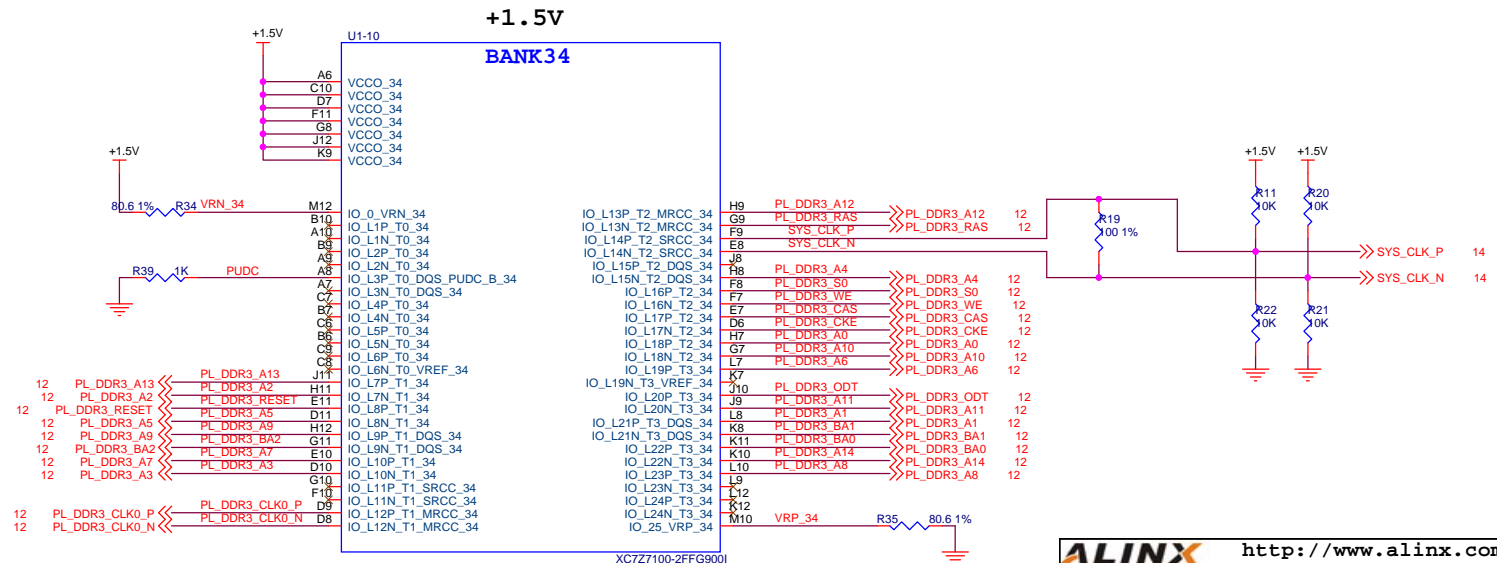
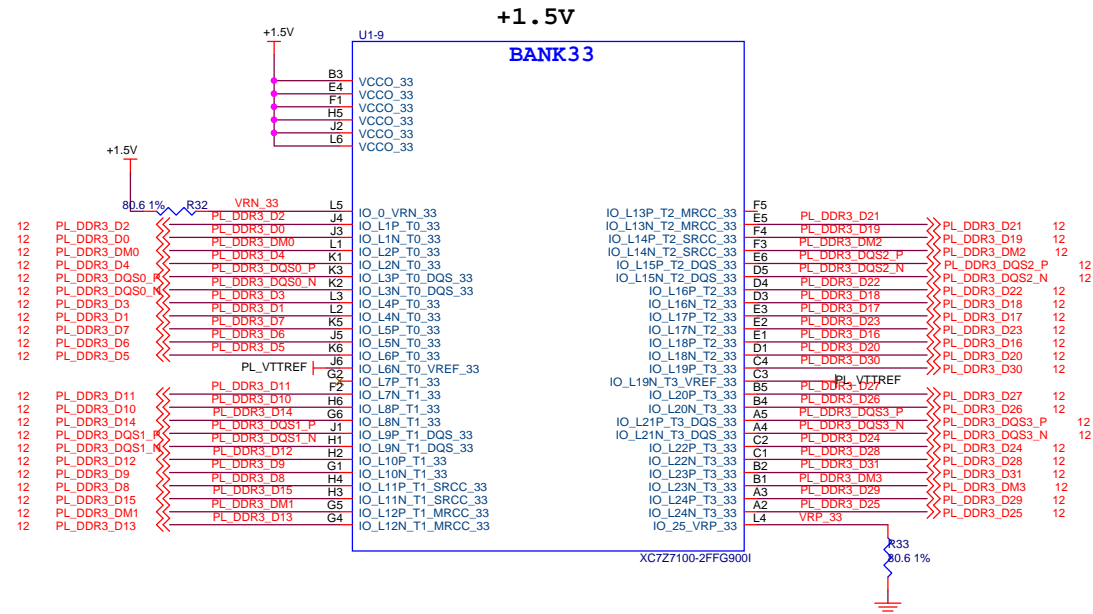
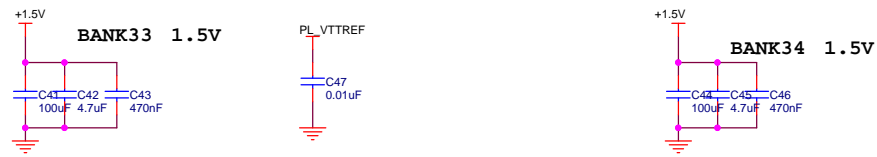
The diagram illustrates the Power On Reset circuit. It features a TCM811TERCTR chip (U4) with the following connections:

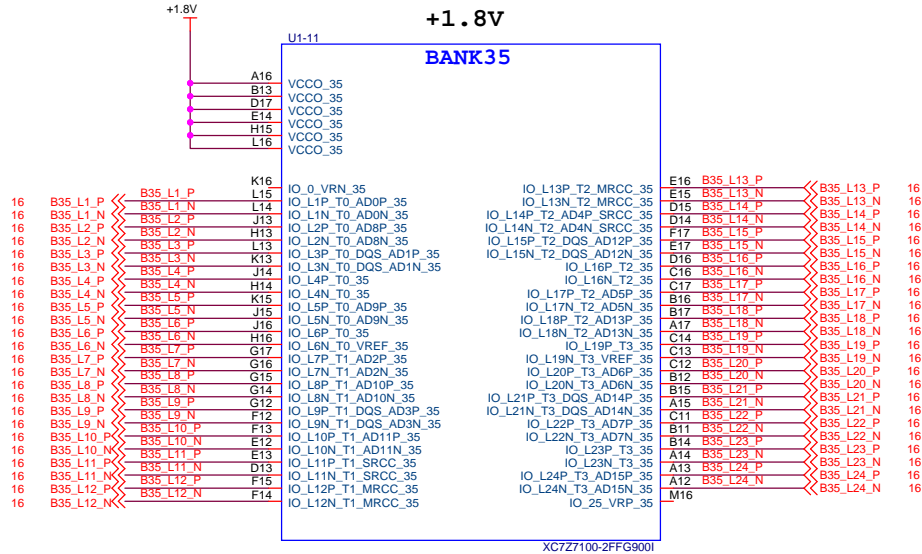
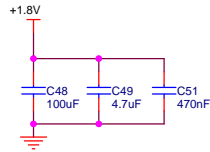
- Pin 3 (#MR):** Connected to a +3.3V supply through a 4.7K resistor (R139) and to the SYS_RESET signal.
- Pin 4 (VDD):** Connected to a +3.3V supply through a 0.1uF capacitor (C30) and to the VDD pin.
- Pin 2 (#RESET):** Connected to a +3.3V supply through a 4.7K resistor (R26) and to the PS_POR_B signal.
- Pin 1 (GND):** Connected to GND.

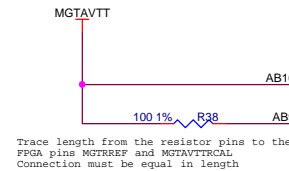
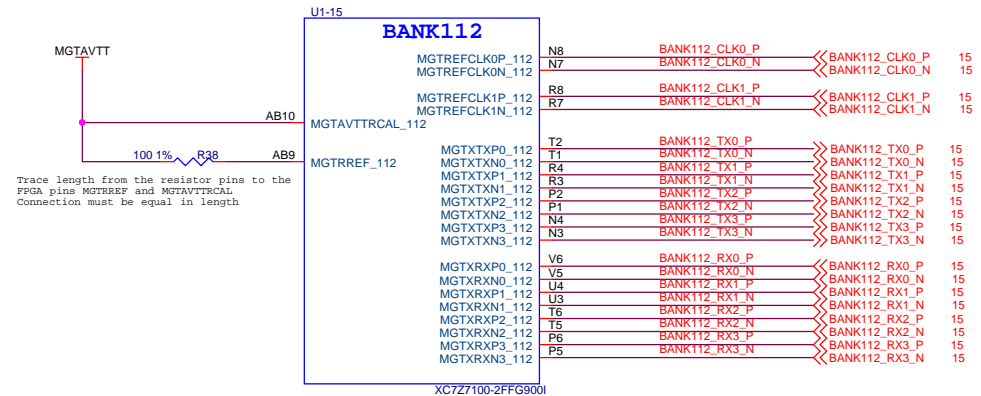
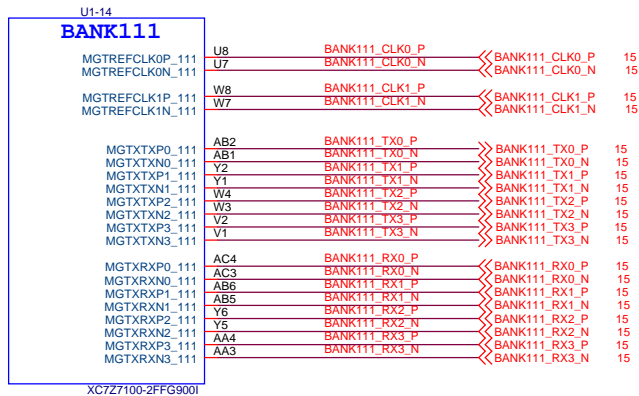
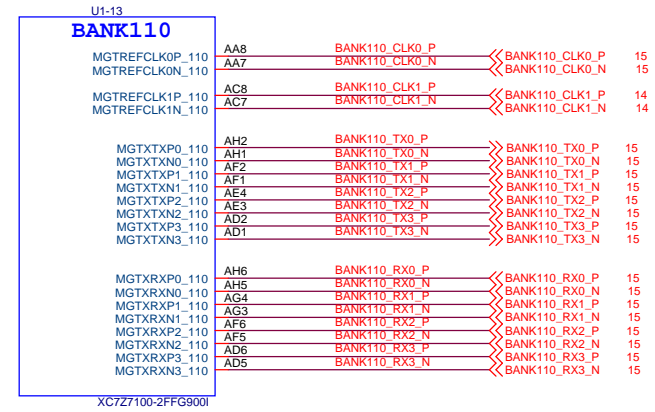
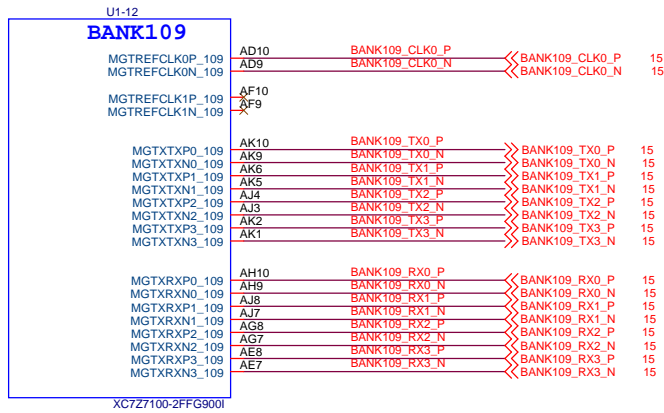


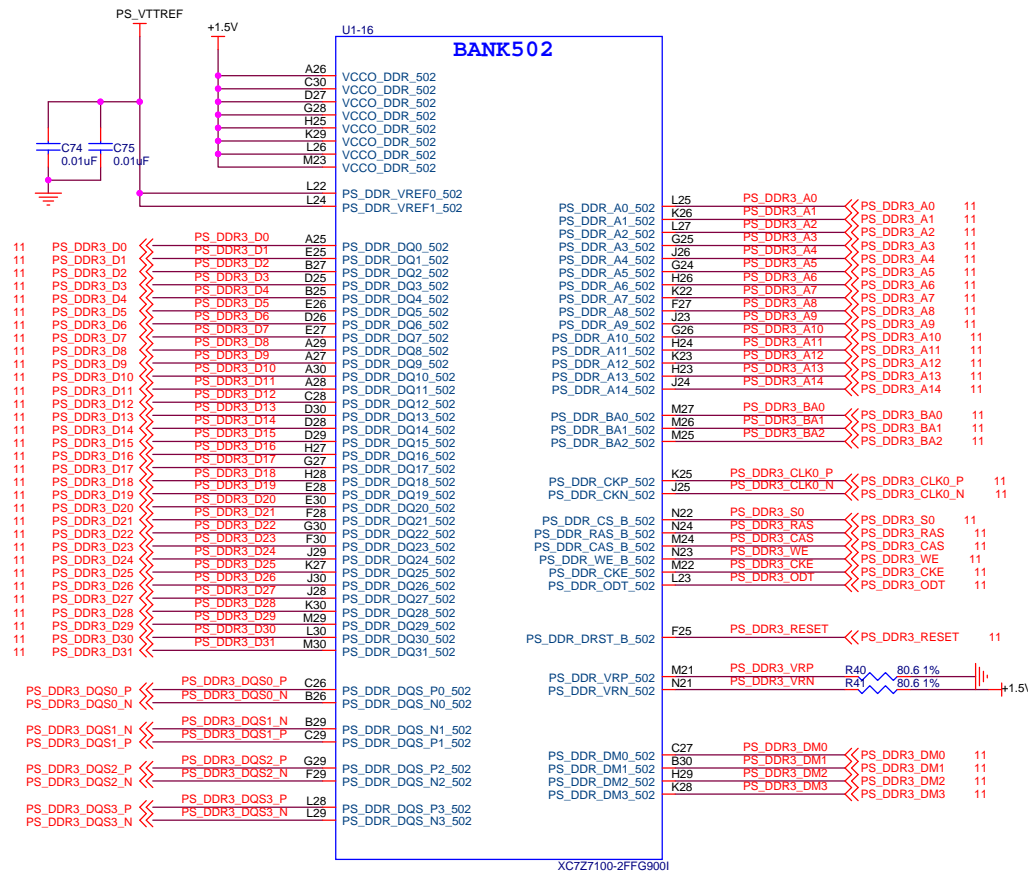





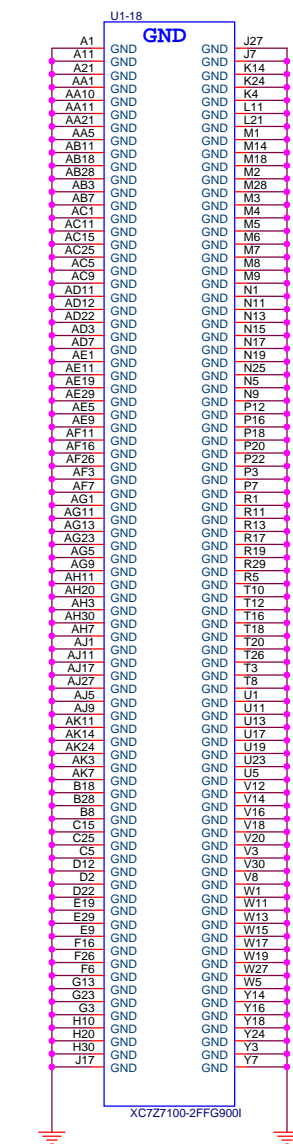


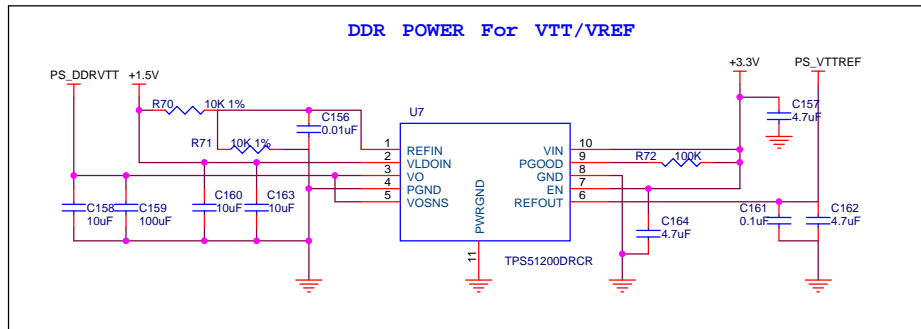
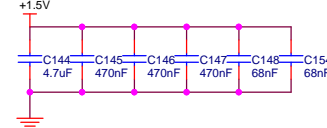
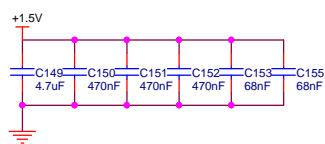
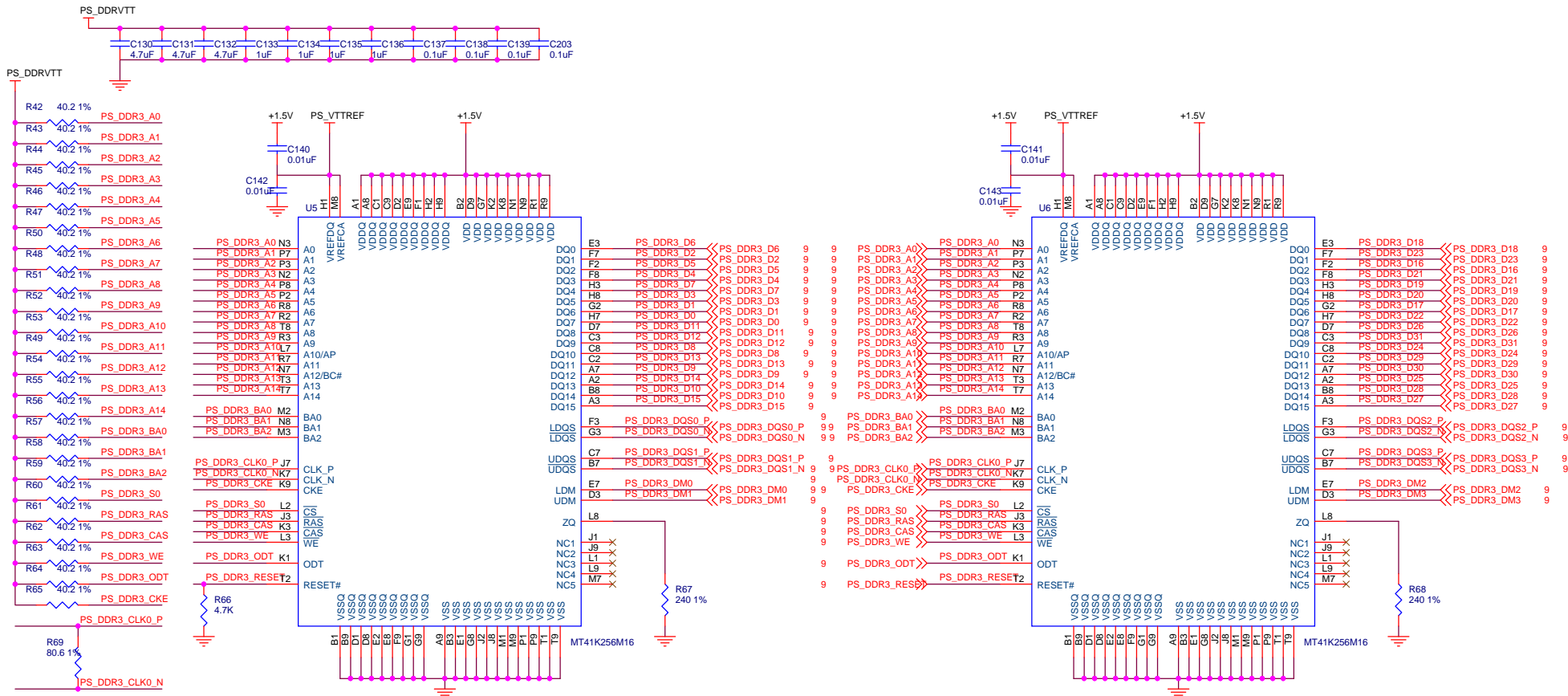


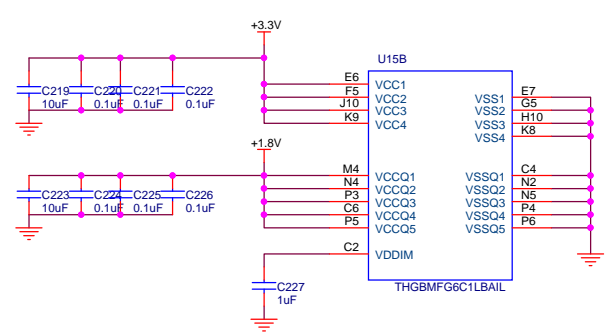
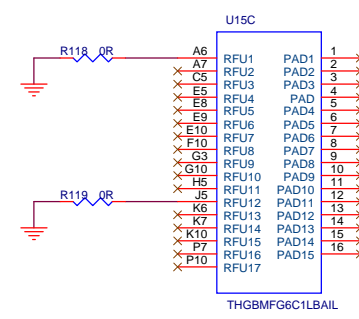
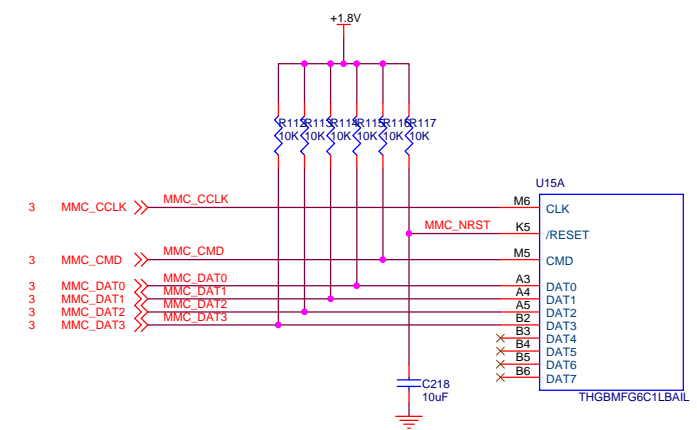
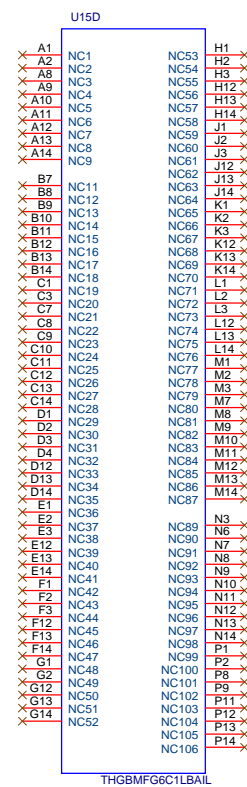
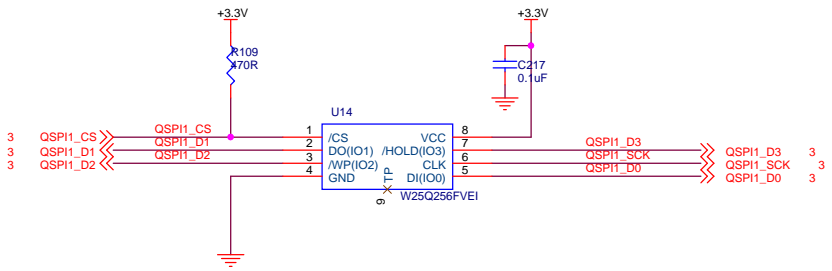
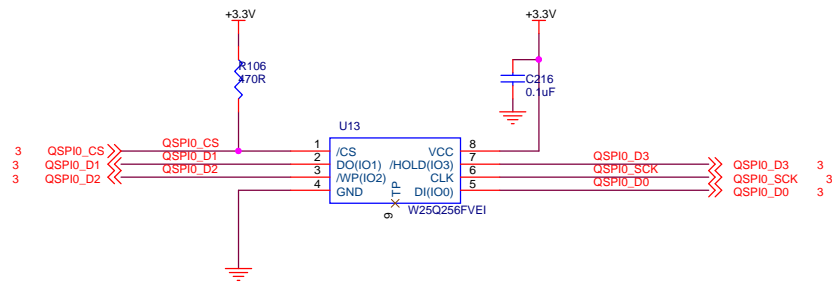




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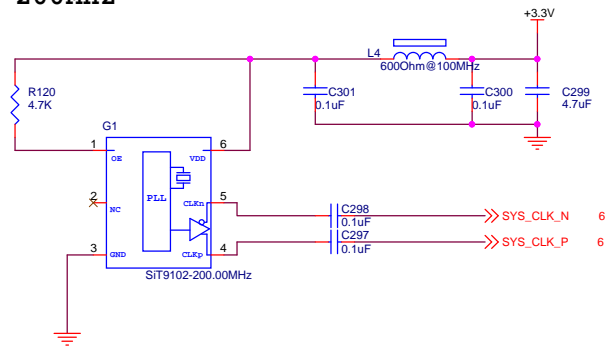






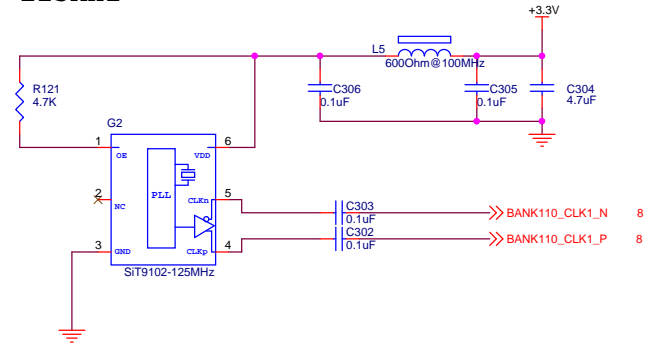
SYSTEM CLOCK

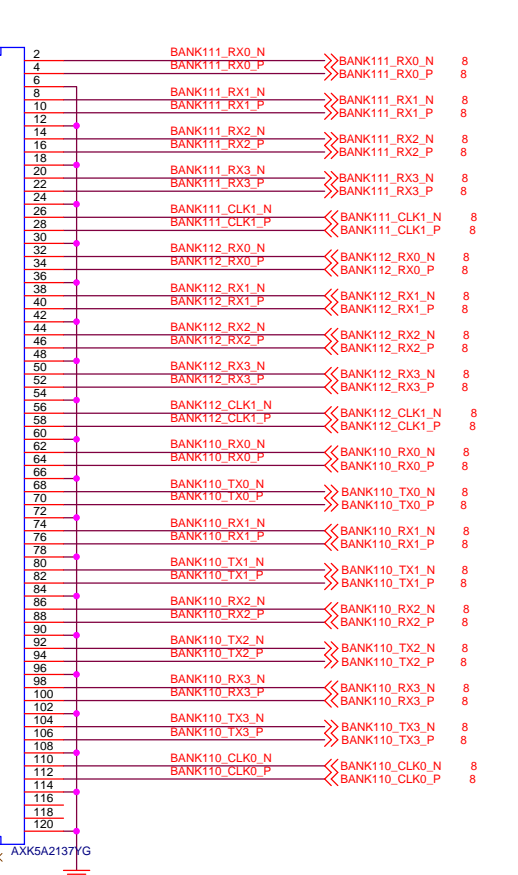
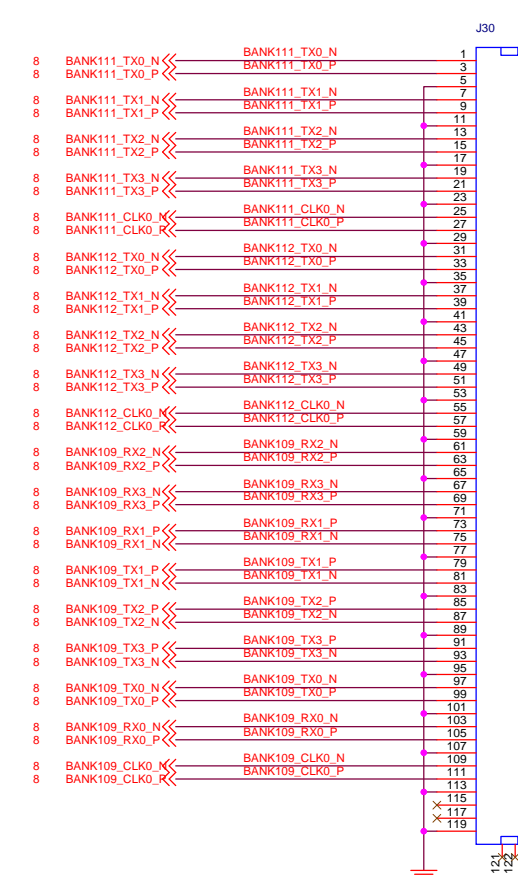
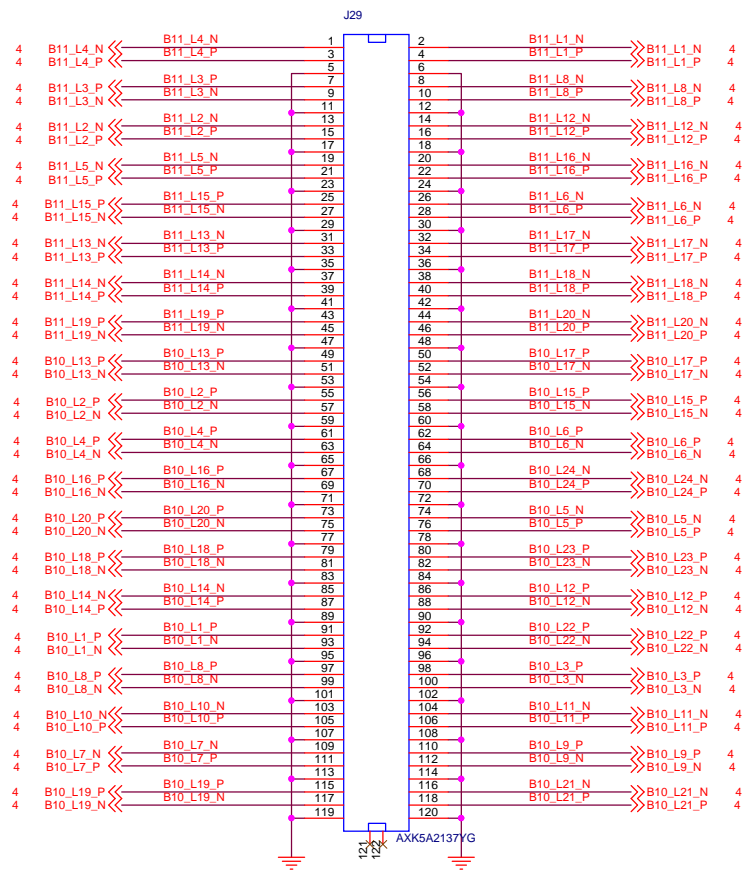
200MHz



GTX CLOCK

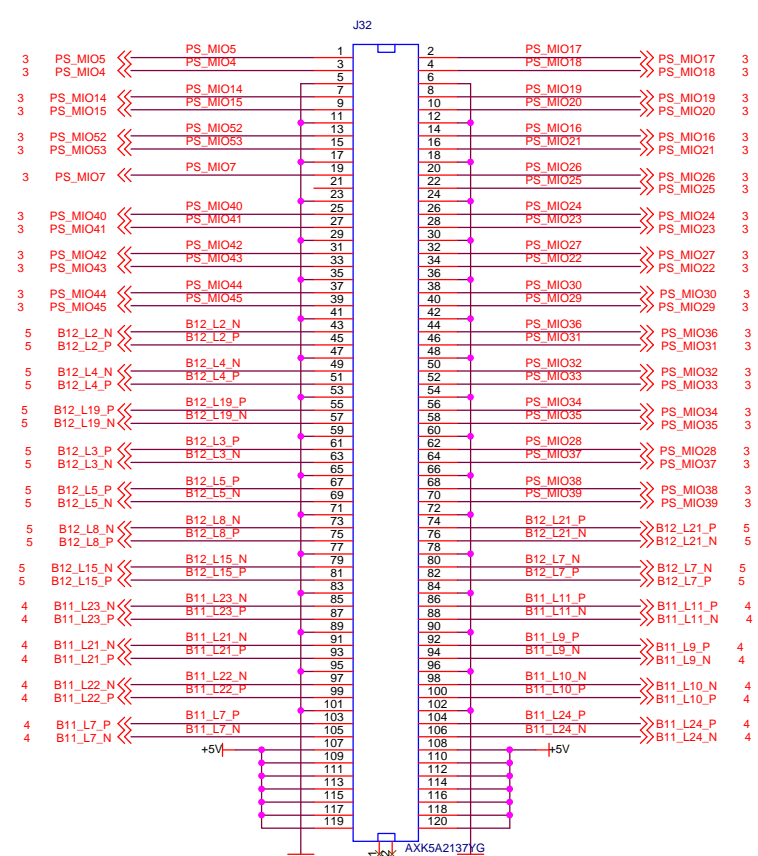
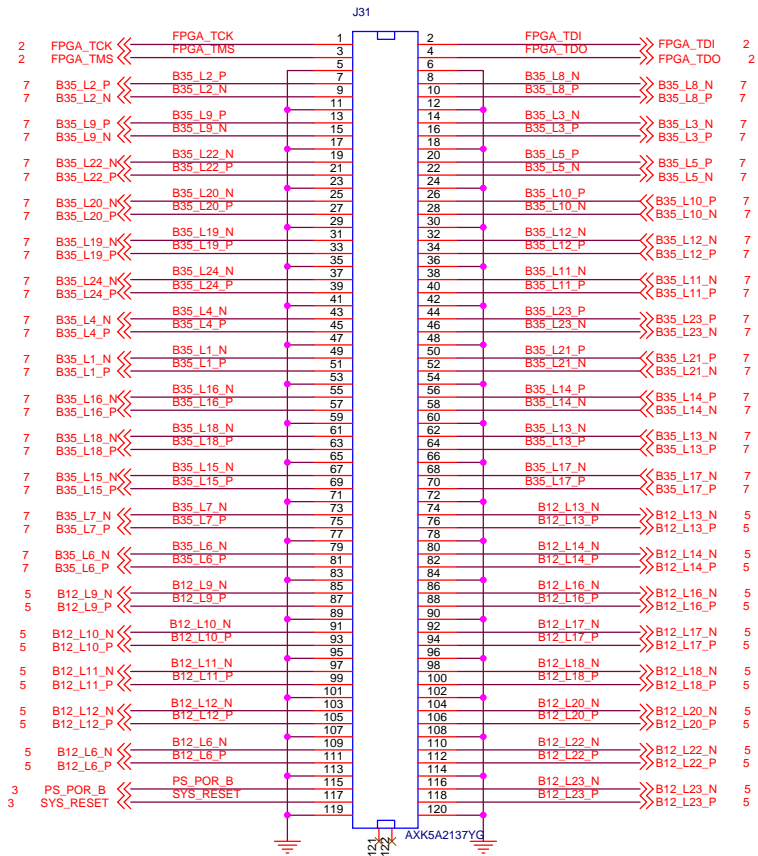
125MHz



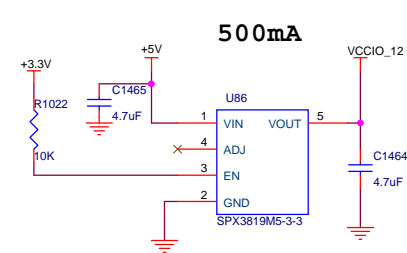
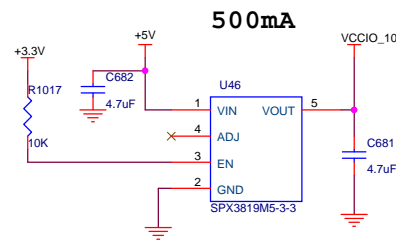
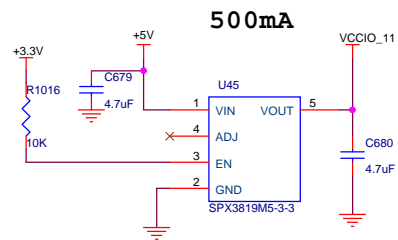
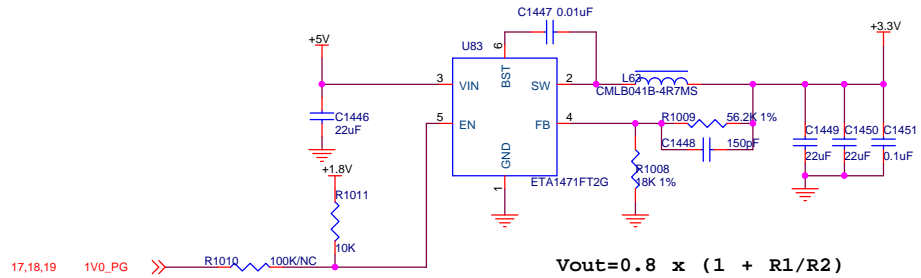
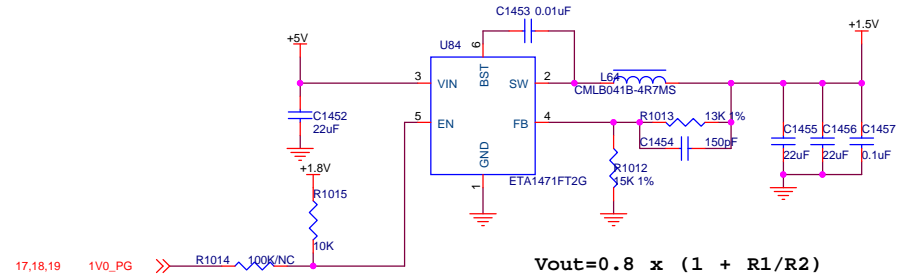
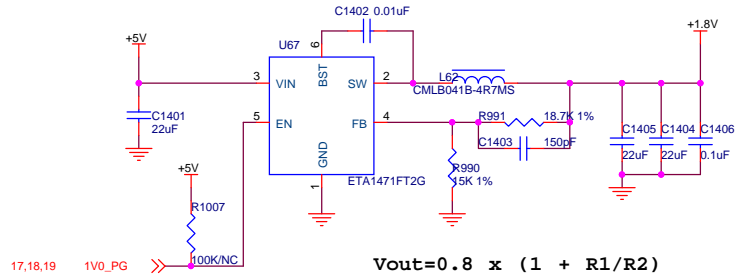


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BANK35 IO is 1.8V



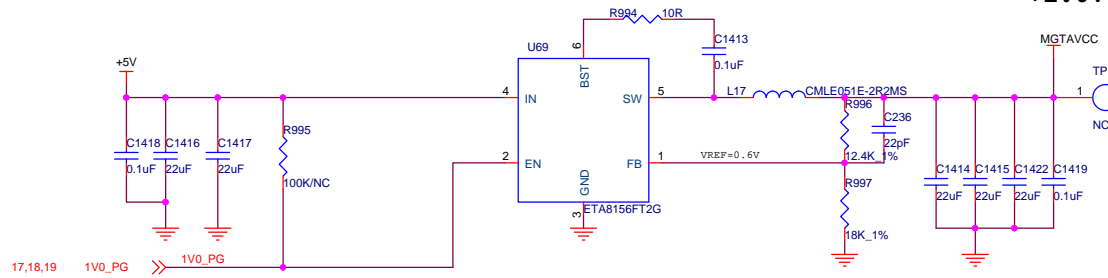
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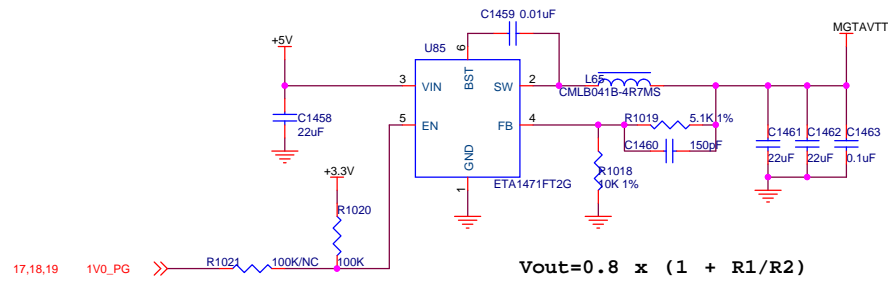
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1.0V POWER 6A

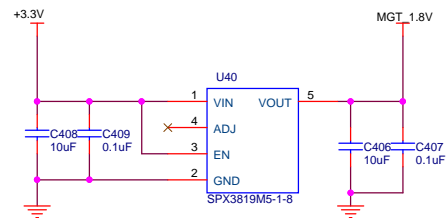
+1.0V



$$V_{out} = 0.6 \times (1 + R_1/R_2)$$



$$V_{out} = 0.8 \times (1 + R_1/R_2)$$



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