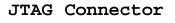
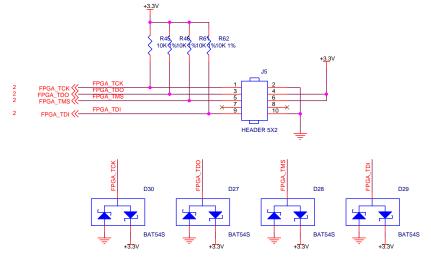
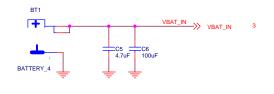
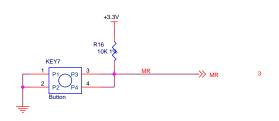


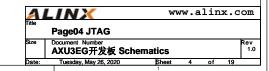
MODE[3:0]	BOOT MODE	Descritpion
0000	PS JTAG	PS JTAG Interface
0001	Quad_SPI(24b)	24-Bit addresssing(QSPI24)
0010	Quad_SPI(32b)	32-Bit addresssing(QSPI32)
0011	SD0(2.0)	SD2.0
0100	NAND	Requires 8-bit data bus width
0101	SD1(2.0)	SD2.0
0110	eMMC(1.8V)	eMMC version 4.5 at 1.8V
0111	USB0(2.0)	USB 2.0 only
1000	PJTAG(MIO #0)	PJTAG connection 0 option
1001	PJTAG(MIO #1)	PJTAG connection 1 option
1110	SD1 LS(3.0)	SD 3.0



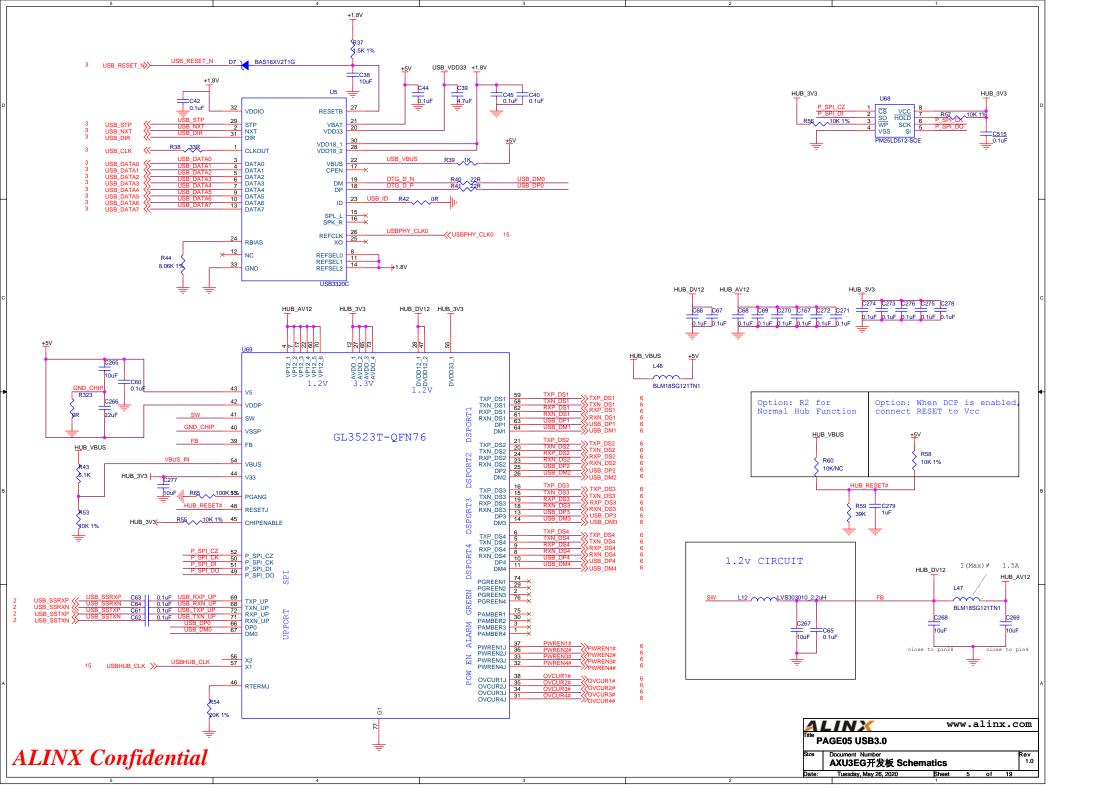


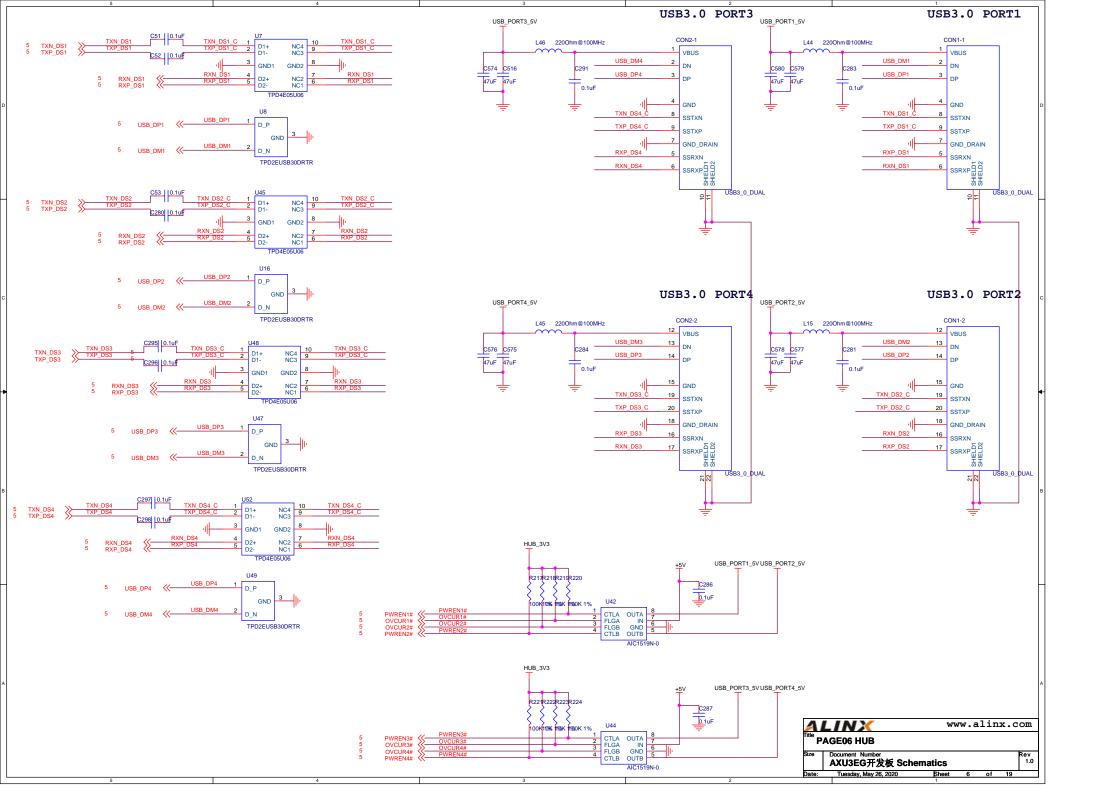


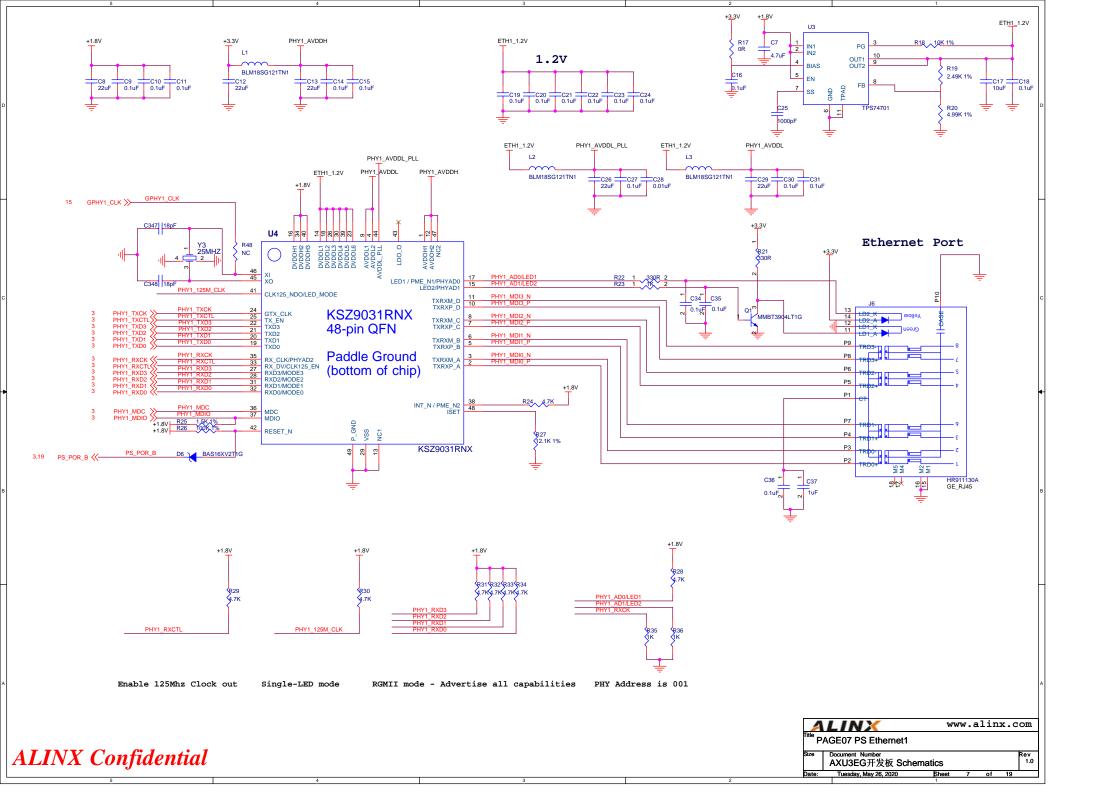


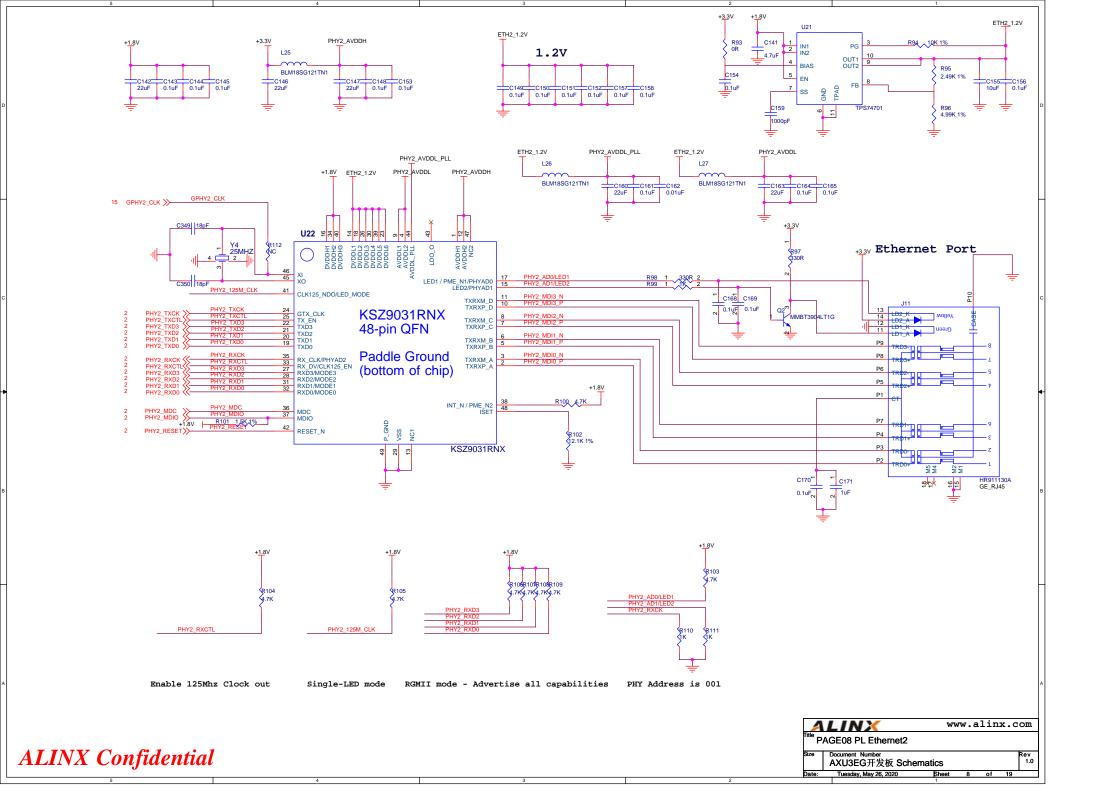


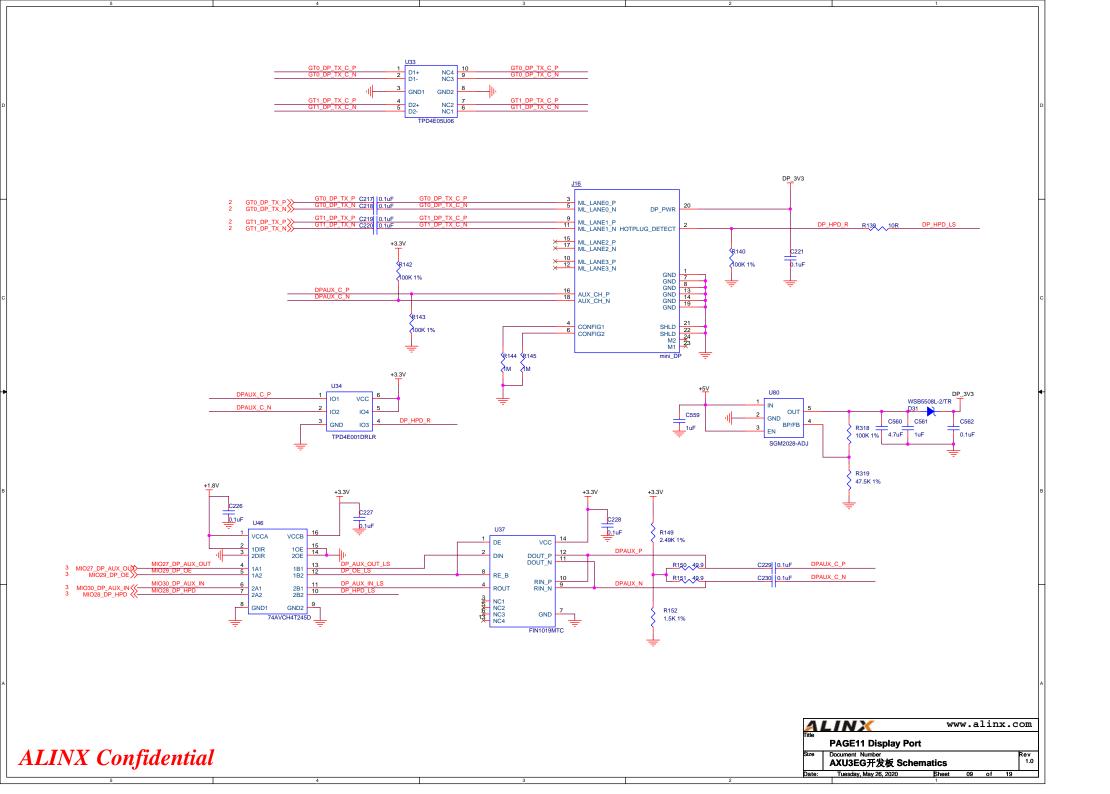
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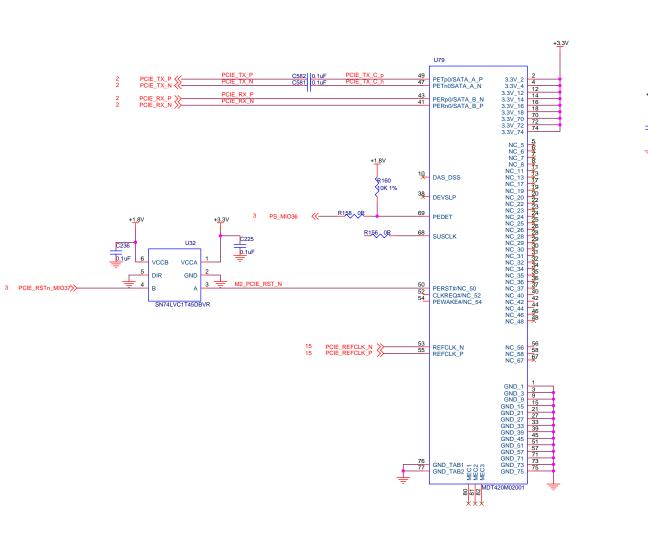


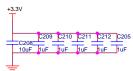








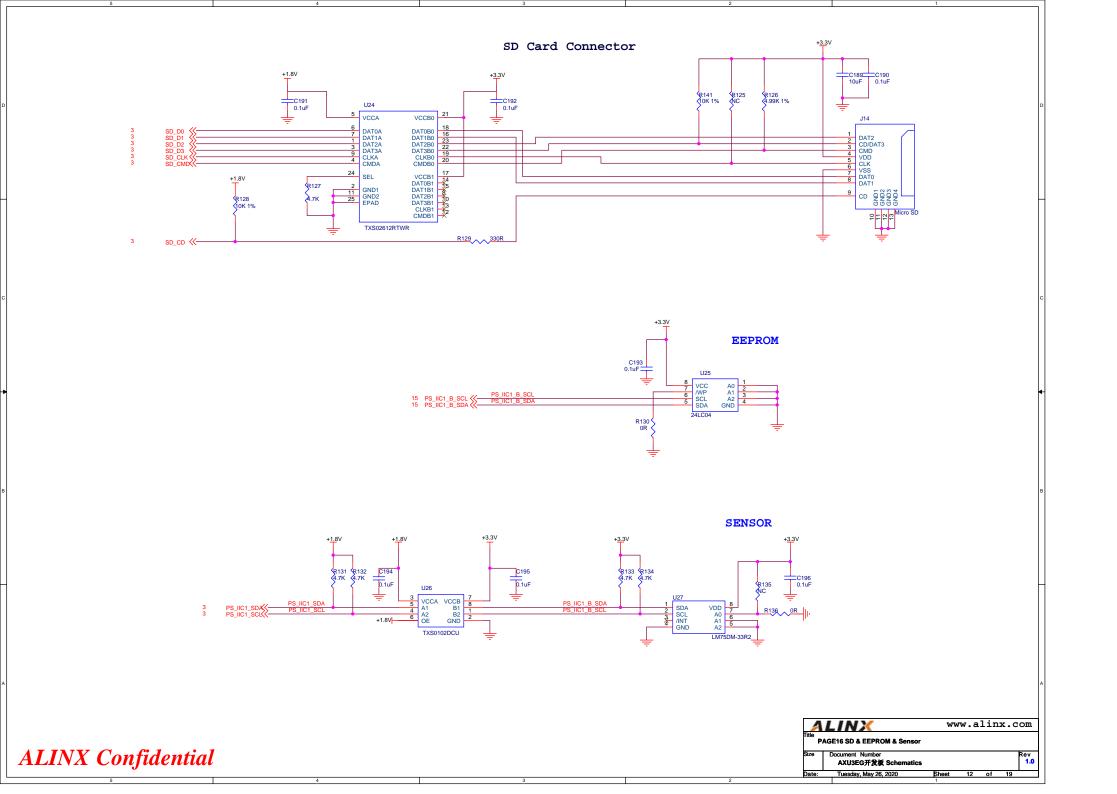


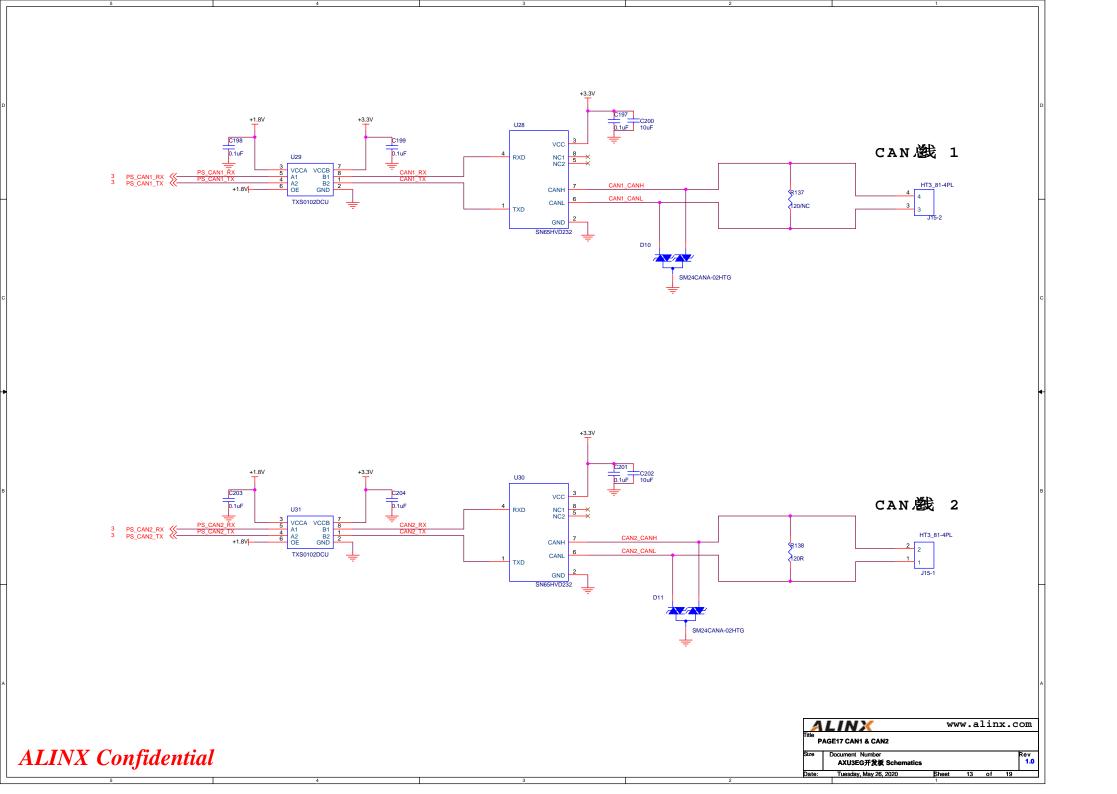


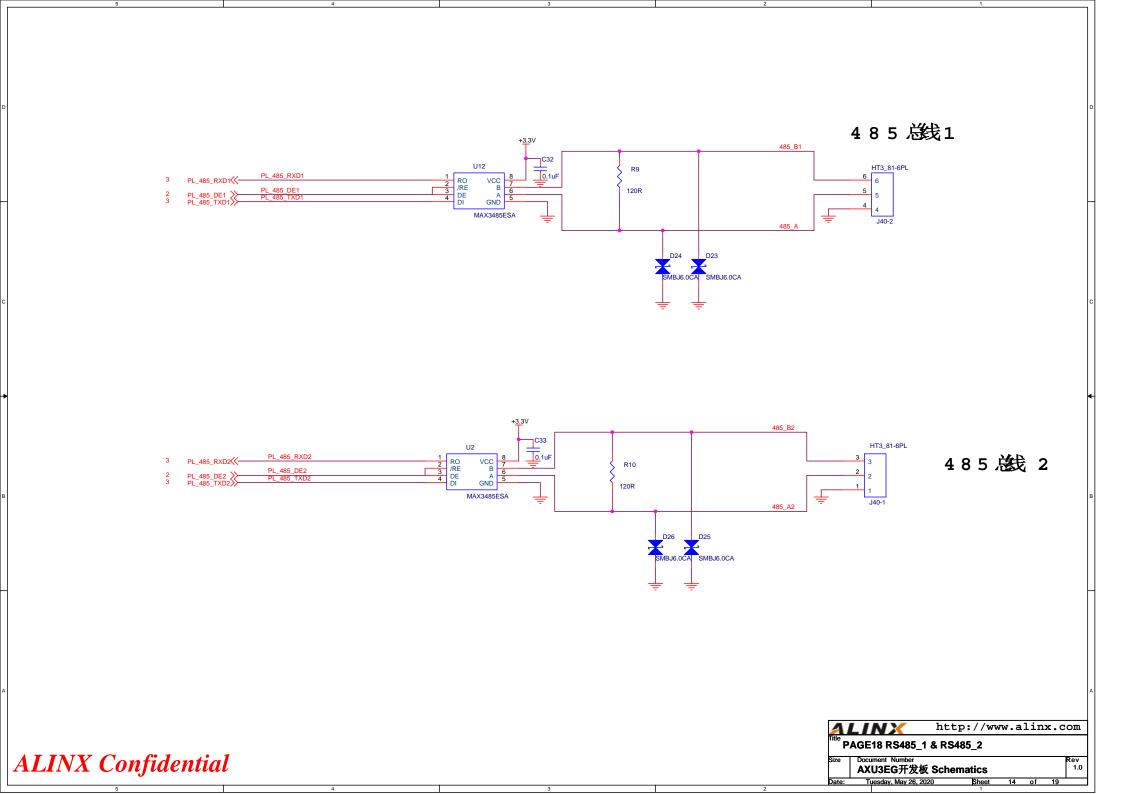
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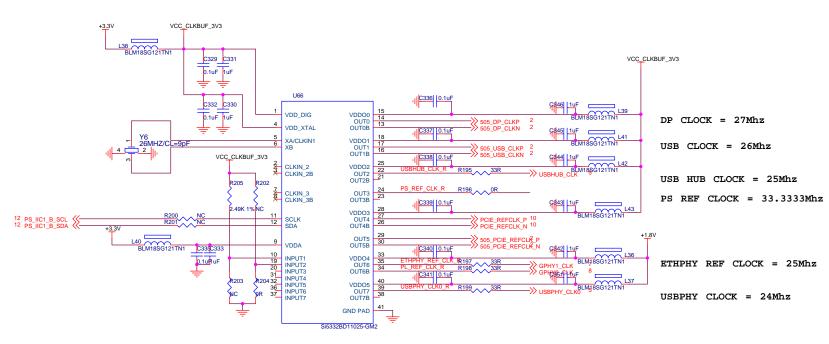
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PS UART PORT R47 10K 1% C55 = 10uF U10 CTS RTS TXD RXD VCCB B1 B2 GND VCCA A1 A2 OE TXS0102DCU 7 VBUS REGIN PL UART PORT 10K 1% NC10 NC30 NC30 NC3 C58 10uF CTS 23 × 24 × 26 × TXD RXD 25 GND PL_UART_RX SOONS D-D-D-D-D-ALINX www.alinx.com PAGE15 UART ALINX Confidential Document Number AXU3EG开发板 Schematics Rev 1.0









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