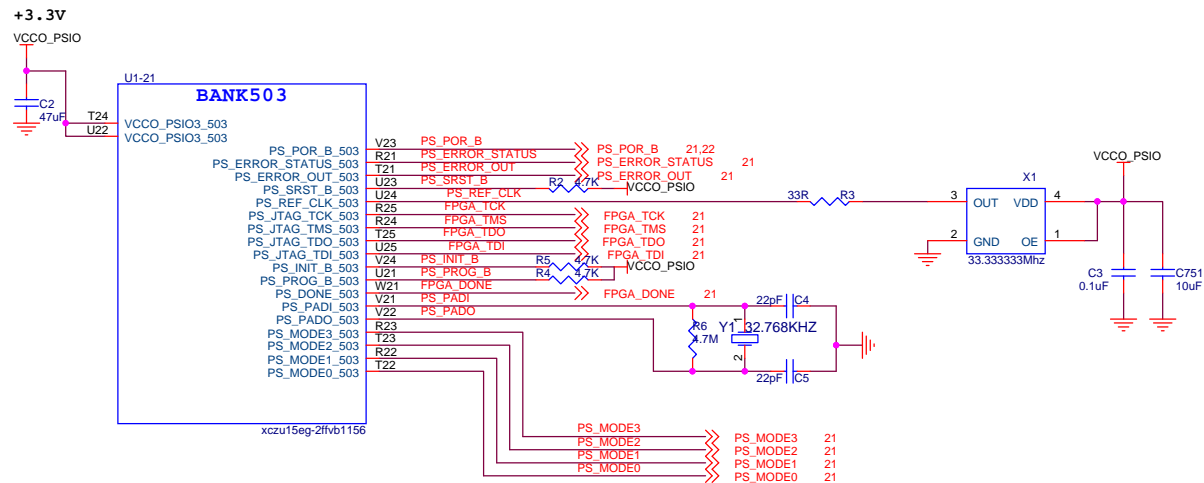
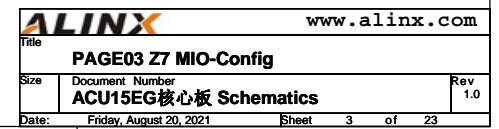
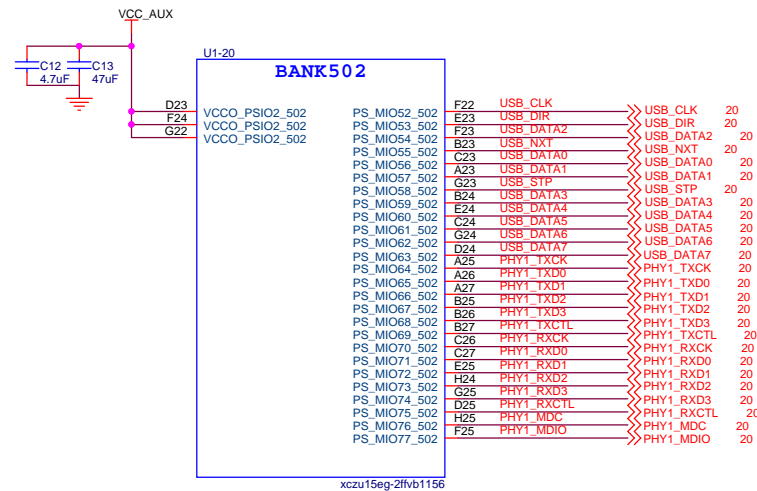
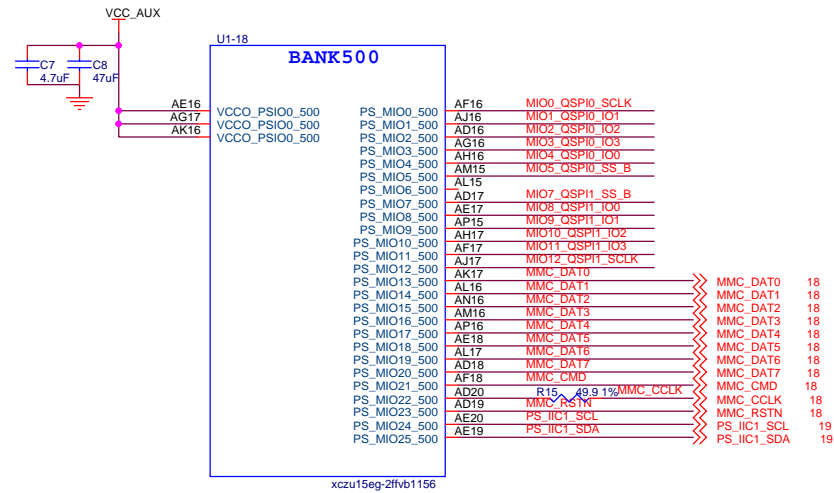
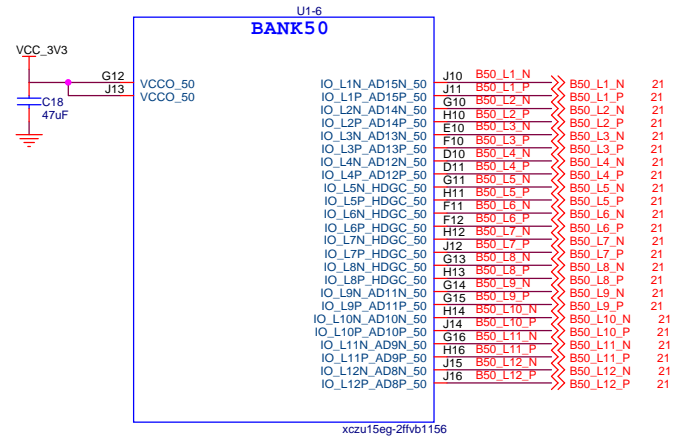
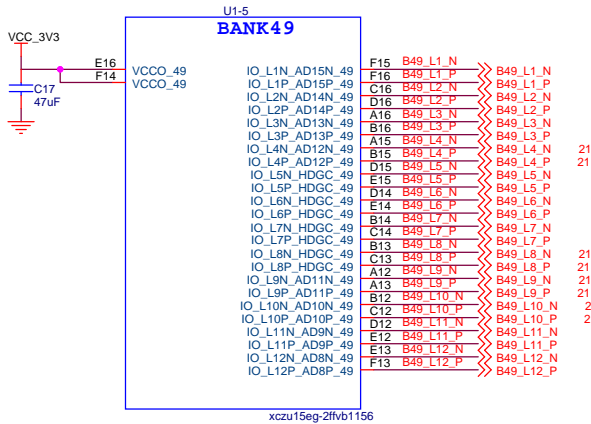
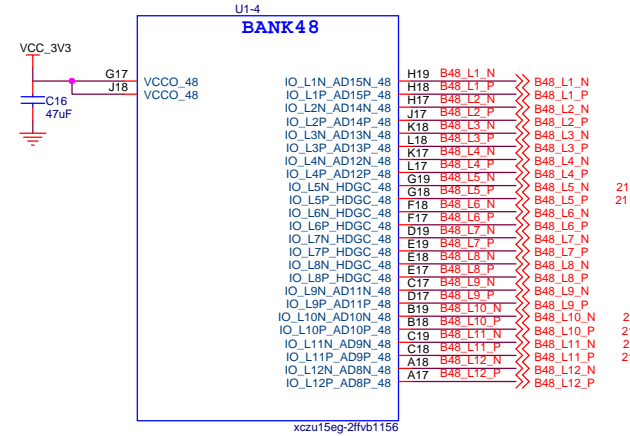
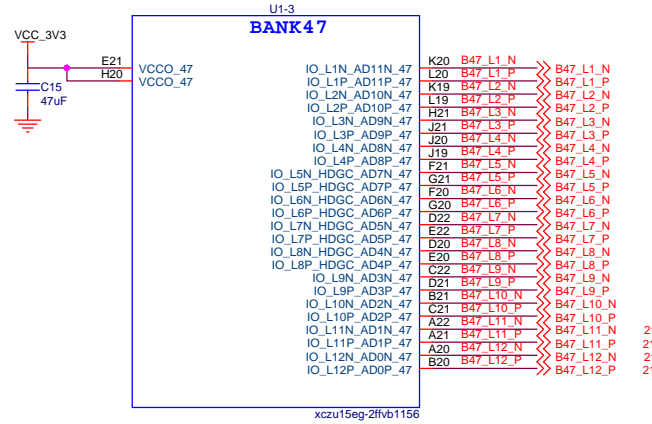
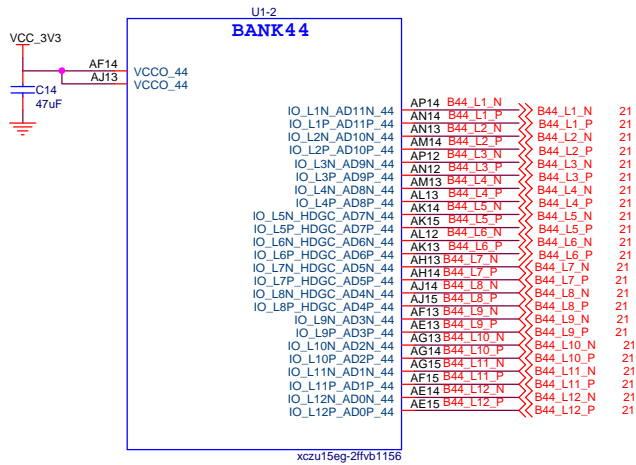


MODE[3:0]	BOOT MODE	Descritpion
0000	PS JTAG	PS JTAG Interface
0001	Quad_SPI(24b)	24-Bit addresssing(QSPI24)
0010	Quad_SPI(32b)	32-Bit addresssing(QSPI32)
0011	SD0(2.0)	SD2.0
0101	SD1(2.0)	SD2.0
0110	eMMC(1.8V)	eMMC version 4.5 at 1.8V
0111	USB0(2.0)	USB 2.0 only
1110	SD1 LS(3.0)	SD 3.0



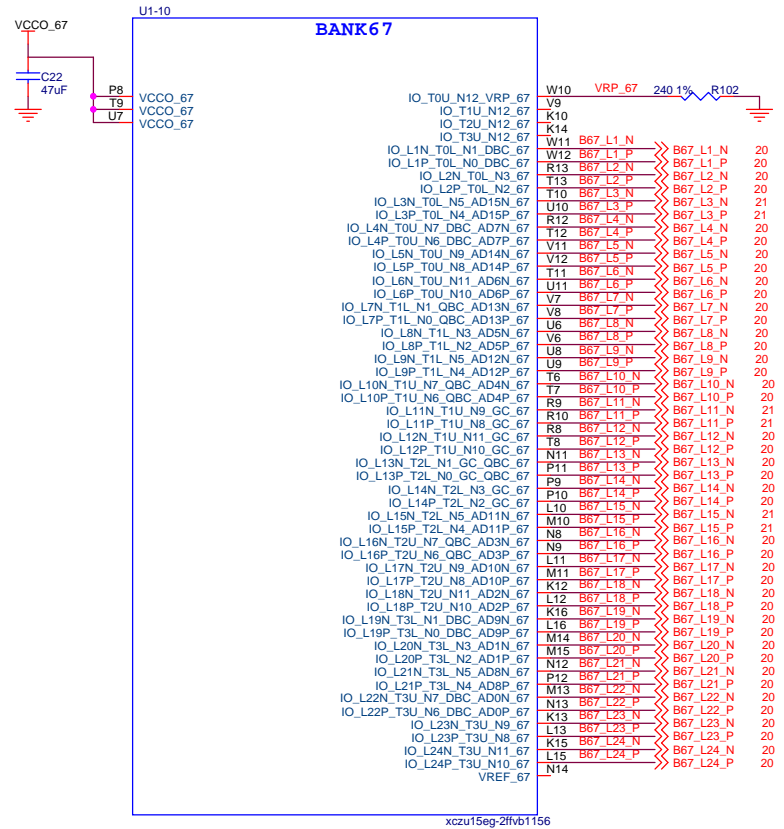


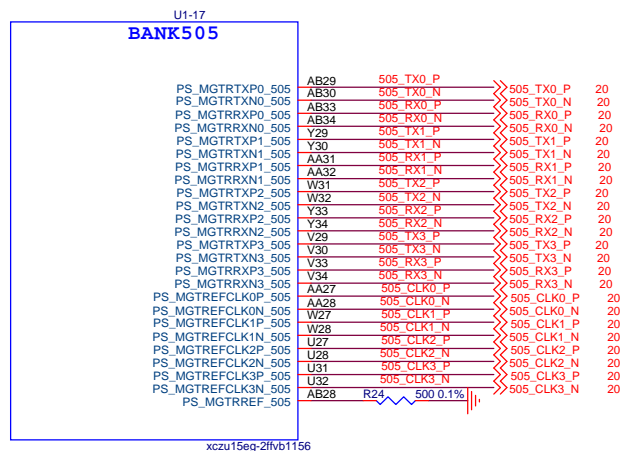
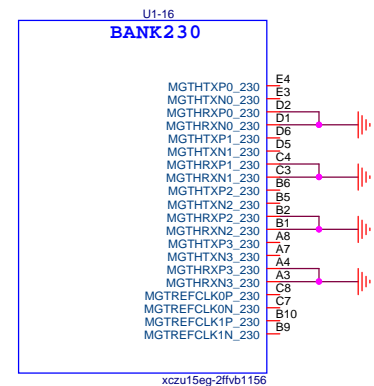
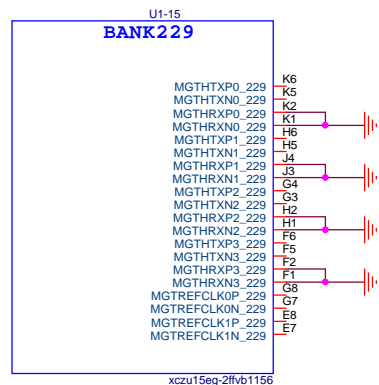
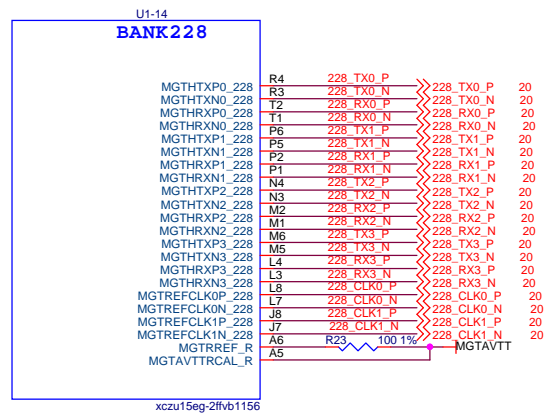
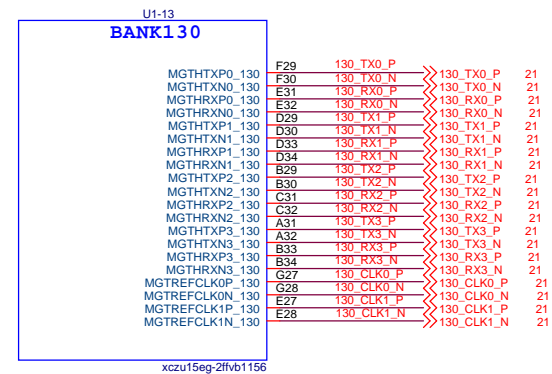
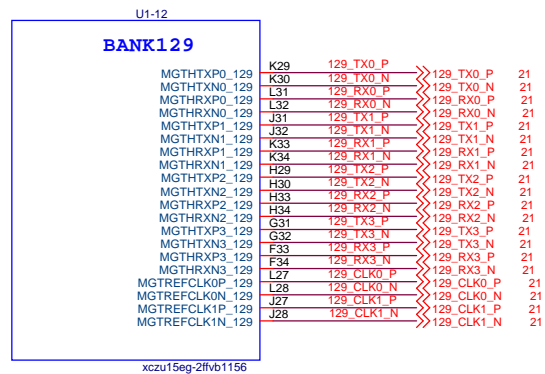
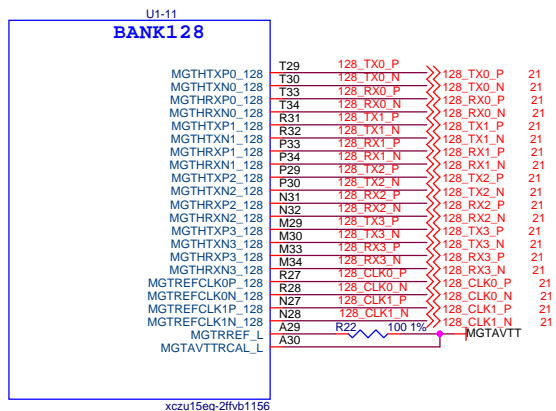


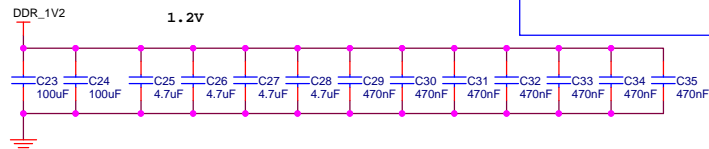
1.2V~1.8V



1.2V~1.8V







U1-22

BANK504

12,13,14,15 PS_DDR4_A0 << PS_DDR4_A0 AP29 PS_DDR_A0_504
12,13,14,15 PS_DDR4_A1 << PS_DDR4_A1 AP30 PS_DDR_A1_504
12,13,14,15 PS_DDR4_A2 << PS_DDR4_A2 AP26 PS_DDR_A2_504
12,13,14,15 PS_DDR4_A3 << PS_DDR4_A3 AP27 PS_DDR_A3_504
12,13,14,15 PS_DDR4_A4 << PS_DDR4_A4 AP25 PS_DDR_A4_504
12,13,14,15 PS_DDR4_A5 << PS_DDR4_A5 AN24 PS_DDR_A5_504
12,13,14,15 PS_DDR4_A6 << PS_DDR4_A6 AM29 PS_DDR_A6_504
12,13,14,15 PS_DDR4_A7 << PS_DDR4_A7 AM28 PS_DDR_A7_504
12,13,14,15 PS_DDR4_A8 << PS_DDR4_A8 AM26 PS_DDR_A8_504
12,13,14,15 PS_DDR4_A9 << PS_DDR4_A9 AM25 PS_DDR_A9_504
12,13,14,15 PS_DDR4_A10 << PS_DDR4_A10 AL28 PS_DDR_A10_504
12,13,14,15 PS_DDR4_A11 << PS_DDR4_A11 AK27 PS_DDR_A11_504
12,13,14,15 PS_DDR4_A12 << PS_DDR4_A12 AJ25 PS_DDR_A12_504
12,13,14,15 PS_DDR4_A13 << PS_DDR4_A13 AL25 PS_DDR_A13_504
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12,13,14,15 PS_DDR4_CAS_B << PS_DDR4_CAS_B AK24 PS_DDR_A15_504
12,13,14,15 PS_DDR4_RAS_B << PS_DDR4_RAS_B AM24 PS_DDR_A16_504
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12,13,14,15 PS_DDR4_ACT_B << PS_DDR4_ACT_B AG25 PS_DDR_BA1_504
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12,13,14,15 PS_DDR4_PARITY_B << PS_DDR4_PARITY_B AF20 PS_DDR_ALERT_N_504
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12,13,14,15 PS_DDR4_BG0 << PS_DDR4_BG0 AK28 PS_DDR_RAM_RST_N_504
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12 PS_DDR4_DQS0_N << PS_DDR4_DQS0_N AN19 PS_DDR_DQS_N0_504
12 PS_DDR4_DQS1_P << PS_DDR4_DQS1_P AN21 PS_DDR_DQS_P1_504
12 PS_DDR4_DQS1_N << PS_DDR4_DQS1_N AN22 PS_DDR_DQS_N1_504
12 PS_DDR4_DQS2_P << PS_DDR4_DQS2_P AH19 PS_DDR_DQS_P2_504
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DDR_1V2

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AJ24 VCC0_PSDDR_504
AJ28 VCC0_PSDDR_504
AL24 VCC0_PSDDR_504
AL29 VCC0_PSDDR_504
AN25 VCC0_PSDDR_504
AN30 VCC0_PSDDR_504

PS_DDR_DQ0_504 AP20 PS_DDR4_DQ0 >>> PS_DDR4_DQ0 12
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PS_DDR_ZQ_504

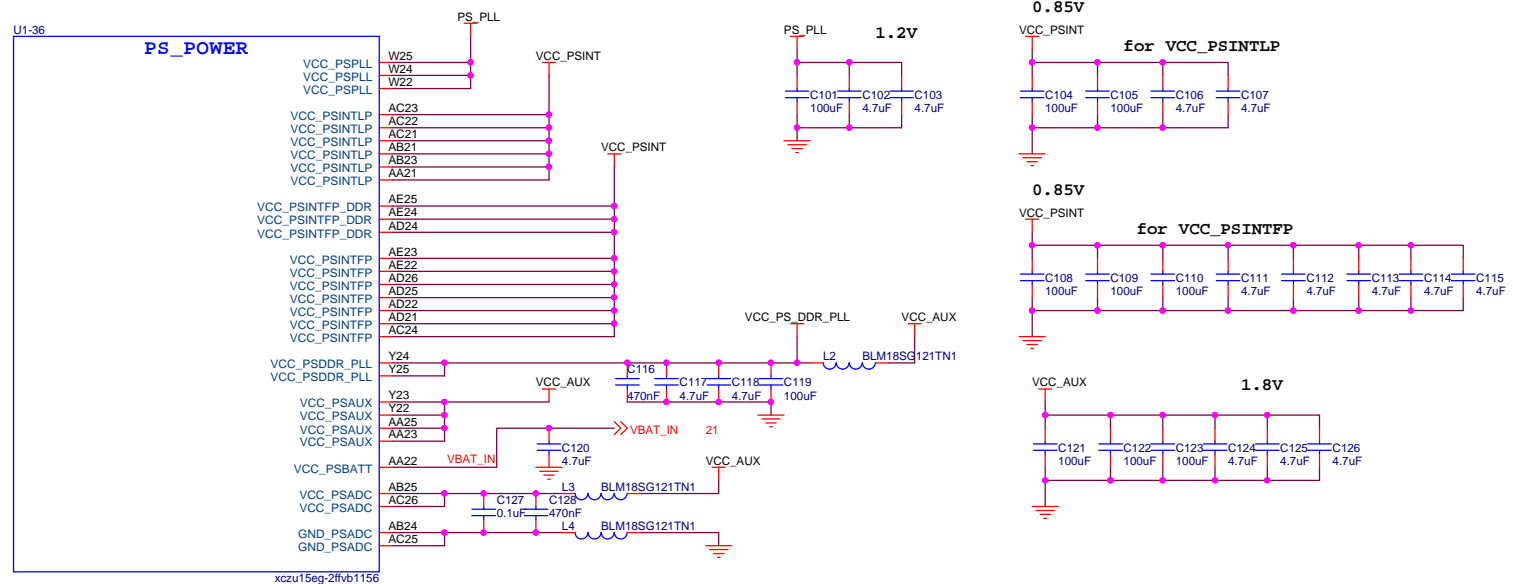
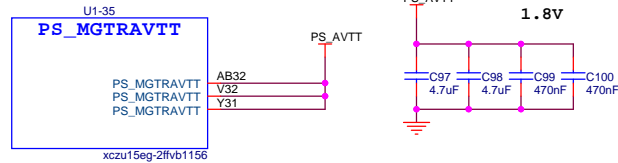
AF23 PS_DDR4_ZQ_504 R25 240 1%

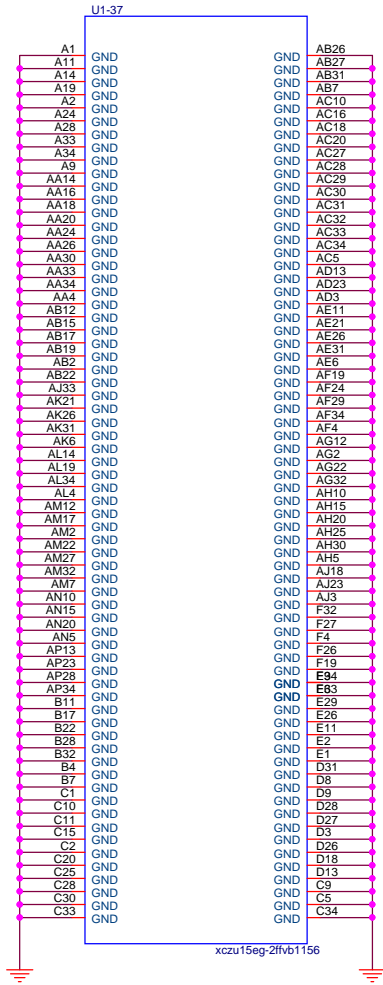
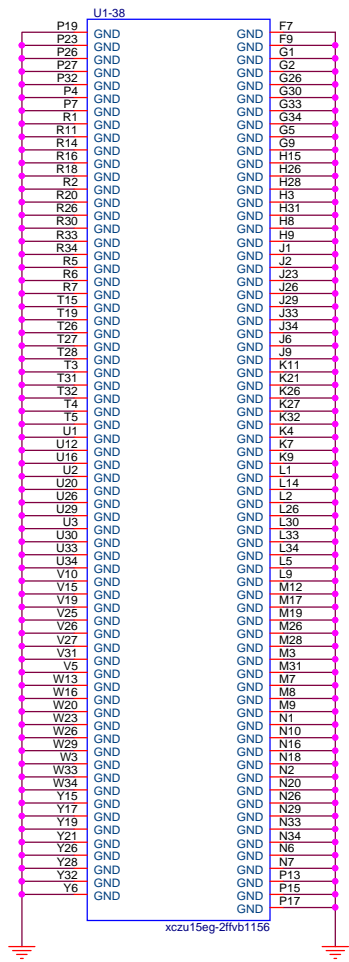
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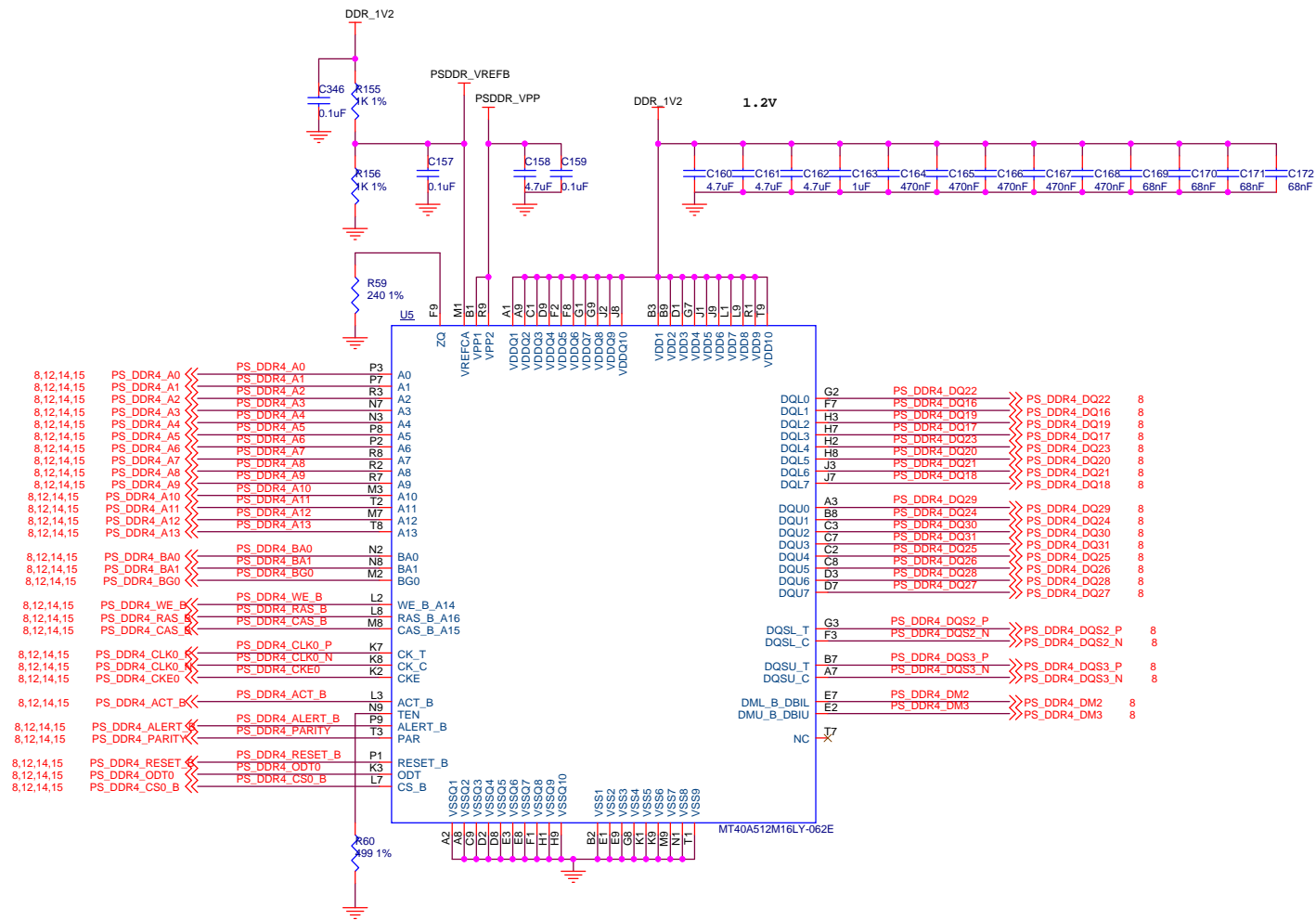
NC2

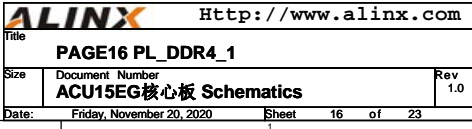
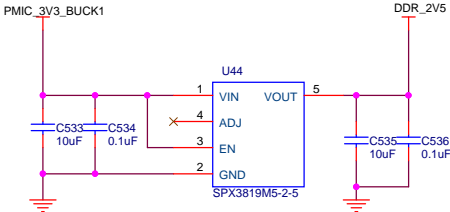
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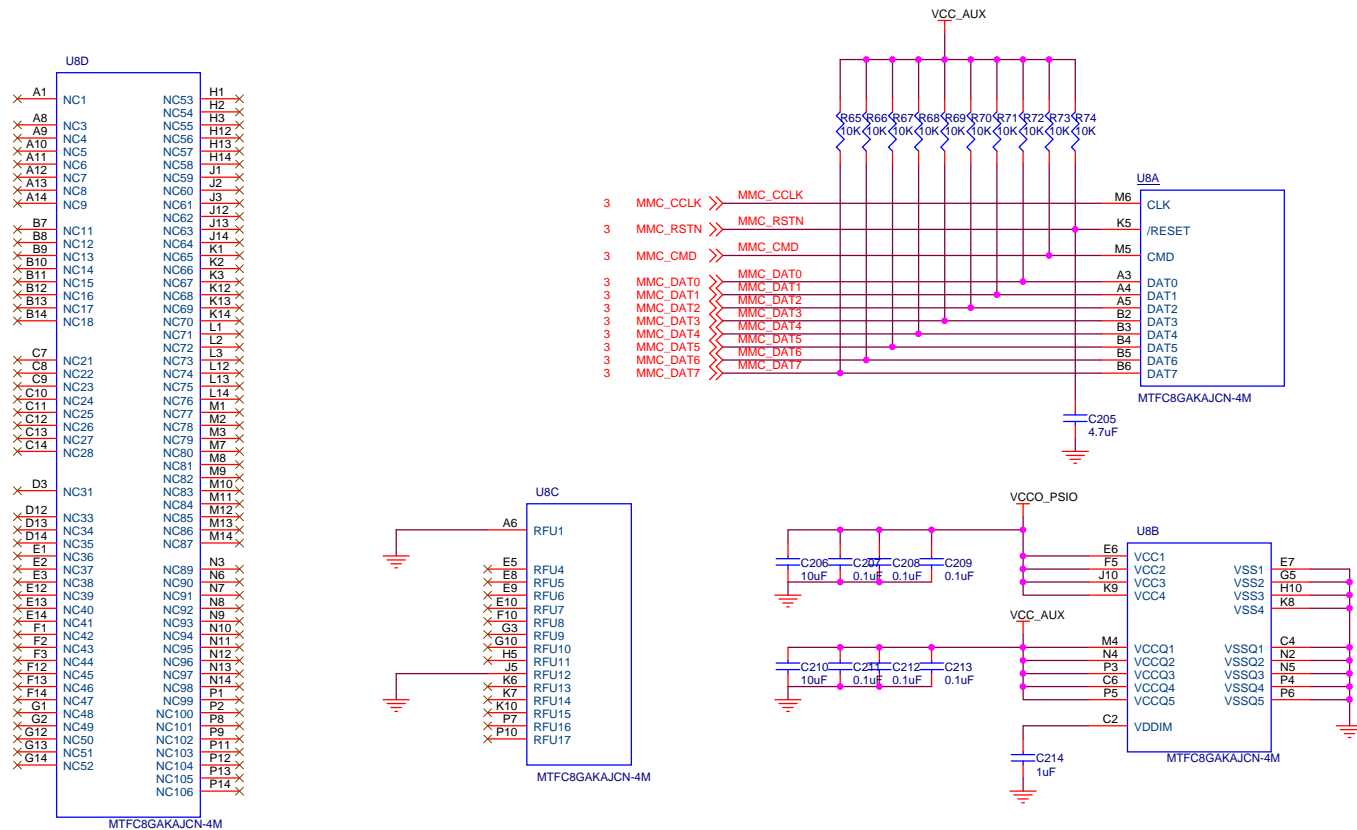
POWER ON: VCC_PSINTLP(+0.85V)->VCC_PSAUX(+1.8V),VCC_PSADC(+1.8V),VCC_PSPLL(+1.2V)->VCCO_PSI0(+1.8V)





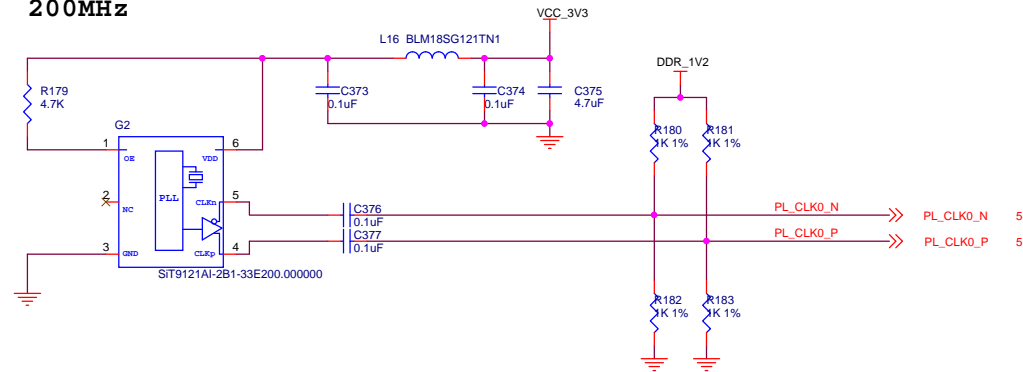






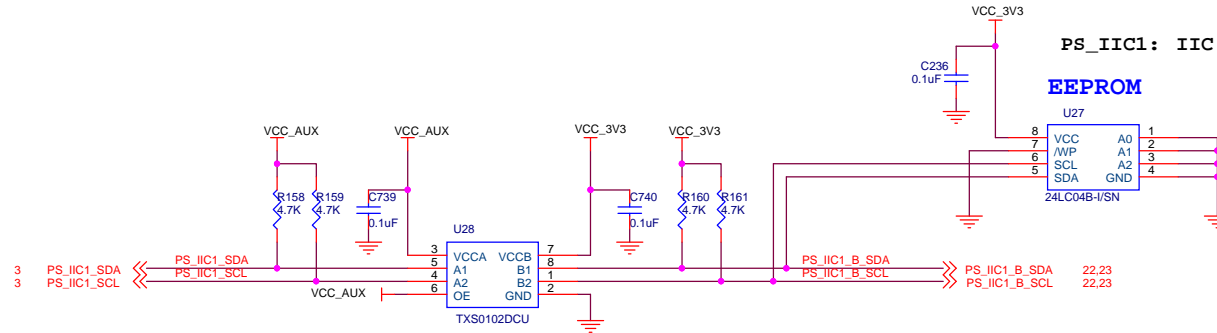
PL SYSTEM CLOCK

200MHz

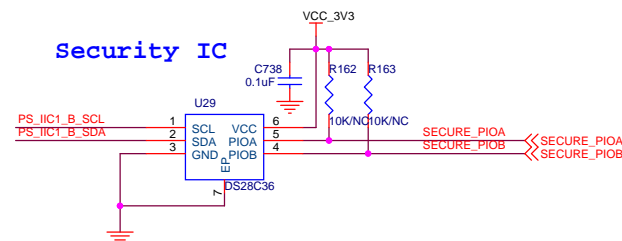


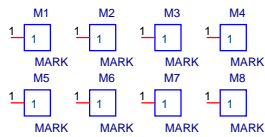
PS_IIC1: IIC ADDRESS IS 0x50

EEPROM



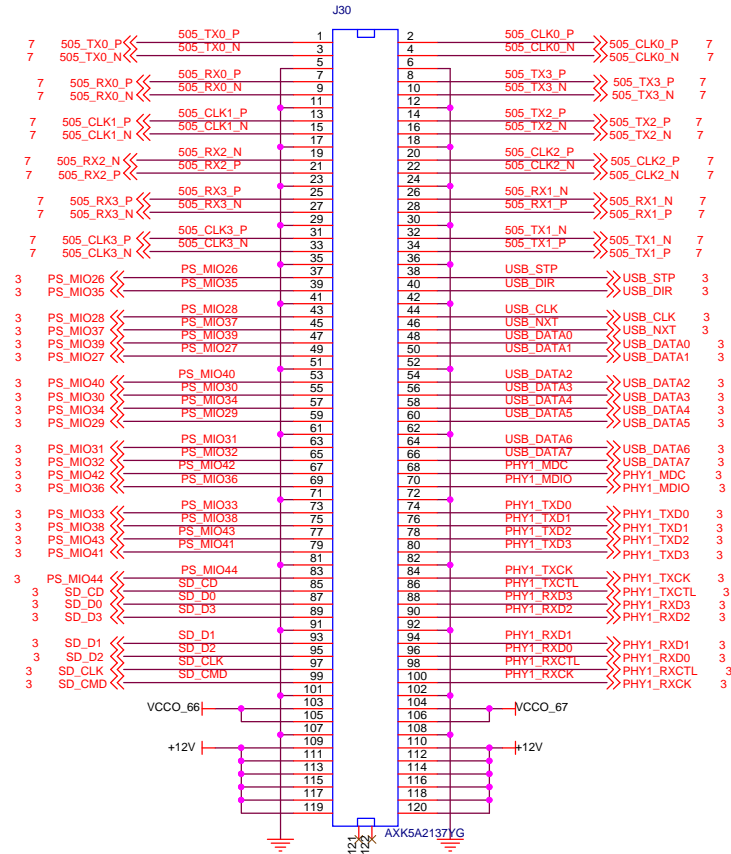
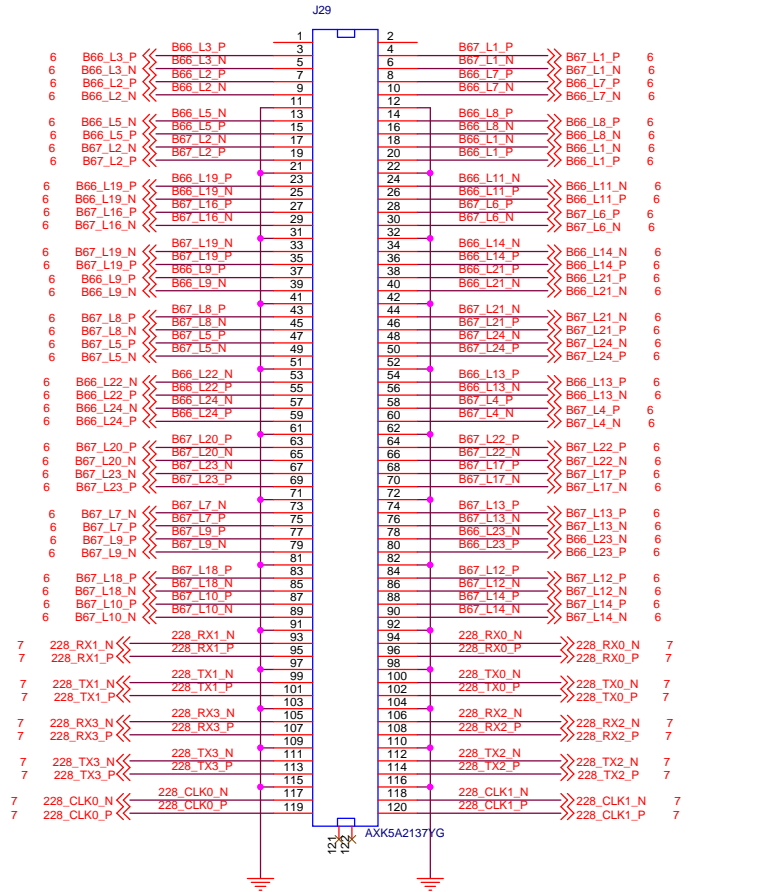
Security IC



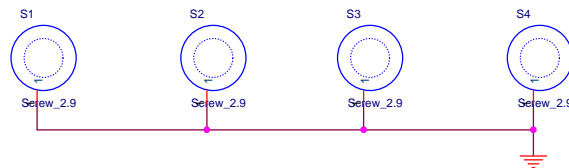


B67,B66 is 1.8V(Default) IOs
228 is PL GTX Transceivers

505 is PS-GTR Transceivers
PS IO is 1.8V standard

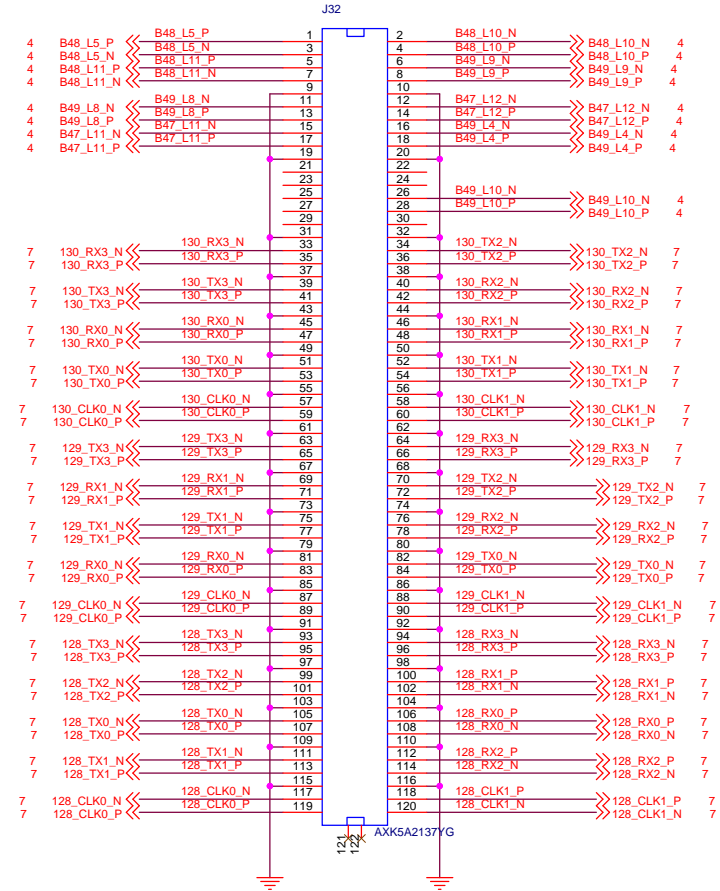
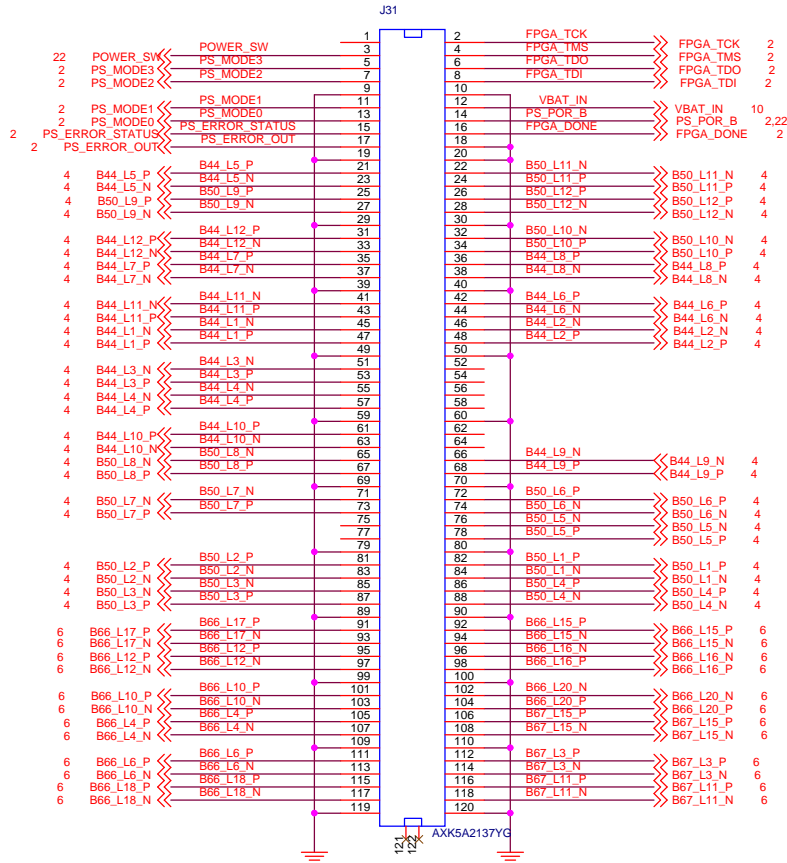


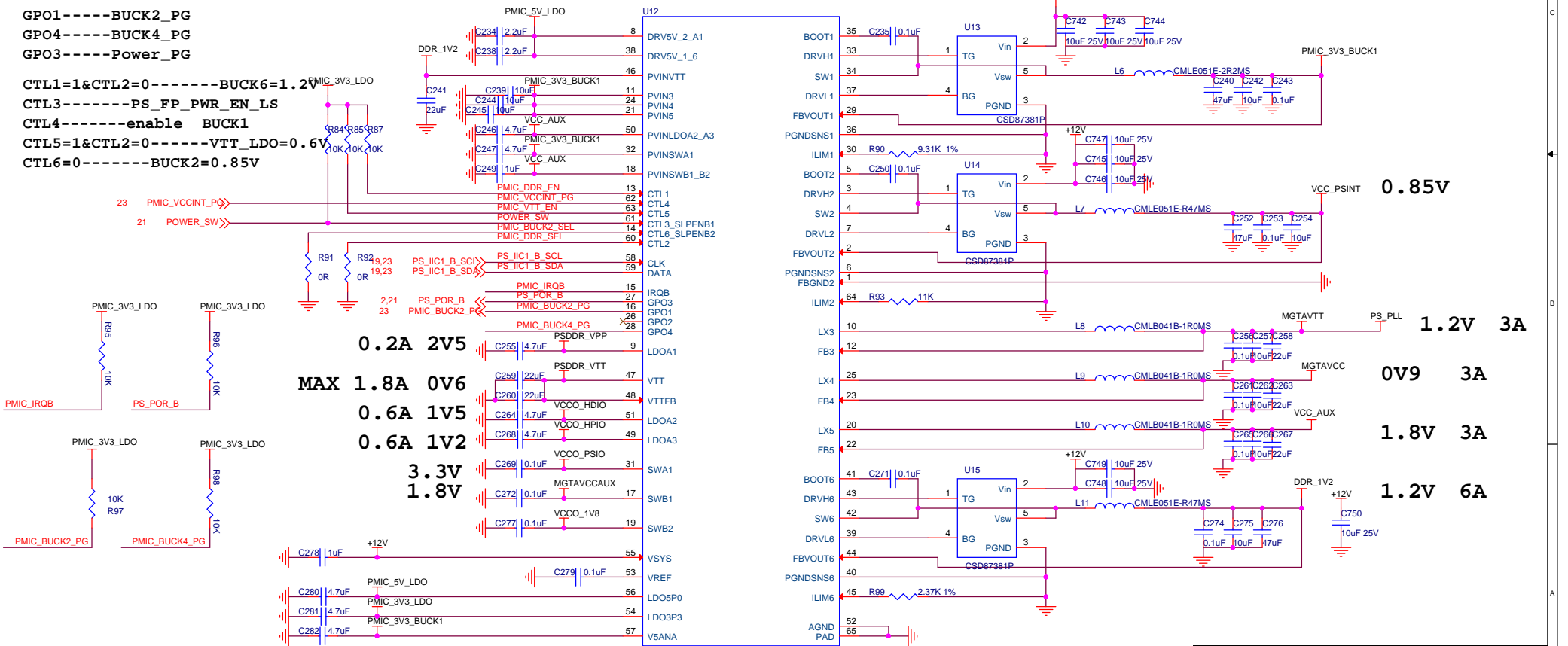
VCCO_66, VCCO_67 is provided from mainboard (not exceed 1.8V)



B44,B50 is 3.3V IOs
B67,B66 is 1.8V(Default) IOs

B48,B49 is 3.3V IOs
128,129,130 is PL GTX Transceivers





+0.85V 25A

