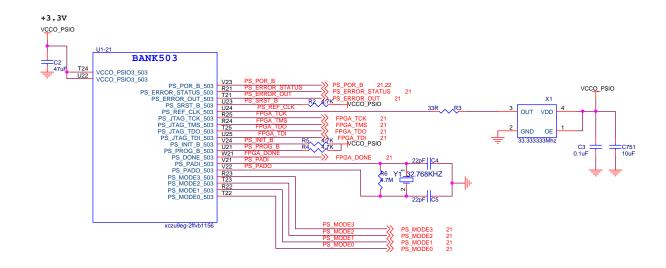
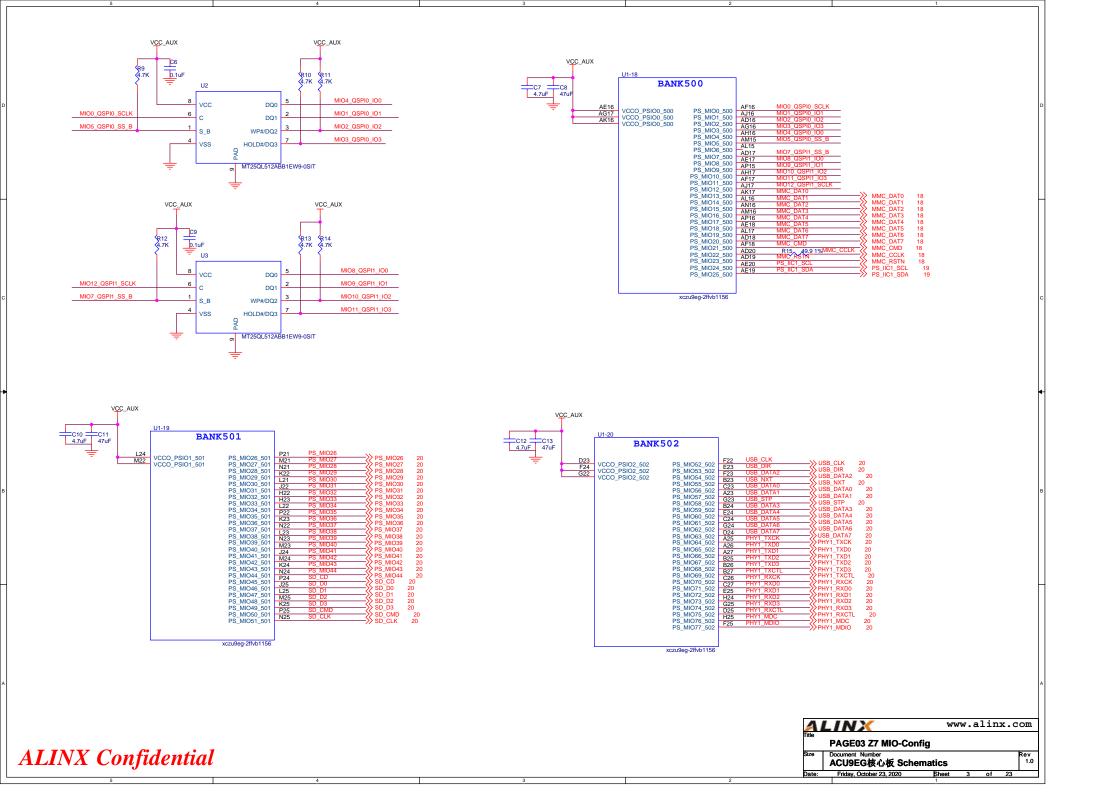
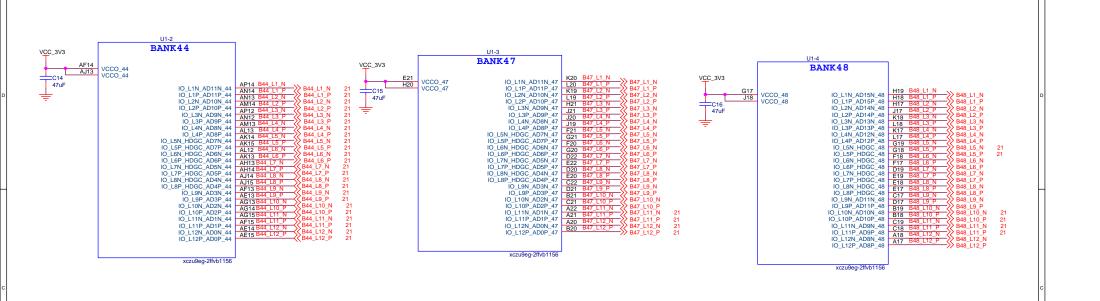


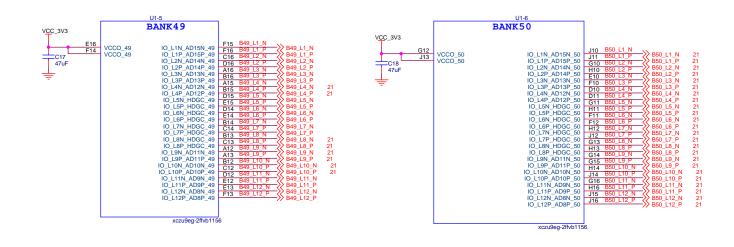


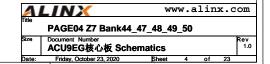
MODE[3:0]	BOOT MODE	Descritpion
0000	PS JTAG	PS JTAG Interface
0001	Quad_SPI(24b)	24-Bit addresssing(QSPI24)
0010	Quad_SPI(32b)	32-Bit addresssing(QSPI32)
0011	SD0(2.0)	SD2.0
0101	SD1(2.0)	SD2.0
0110	eMMC(1.8V)	eMMC version 4.5 at 1.8V
0111	USB0(2.0)	USB 2.0 only
1110	SD1 LS(3.0)	SD 3.0

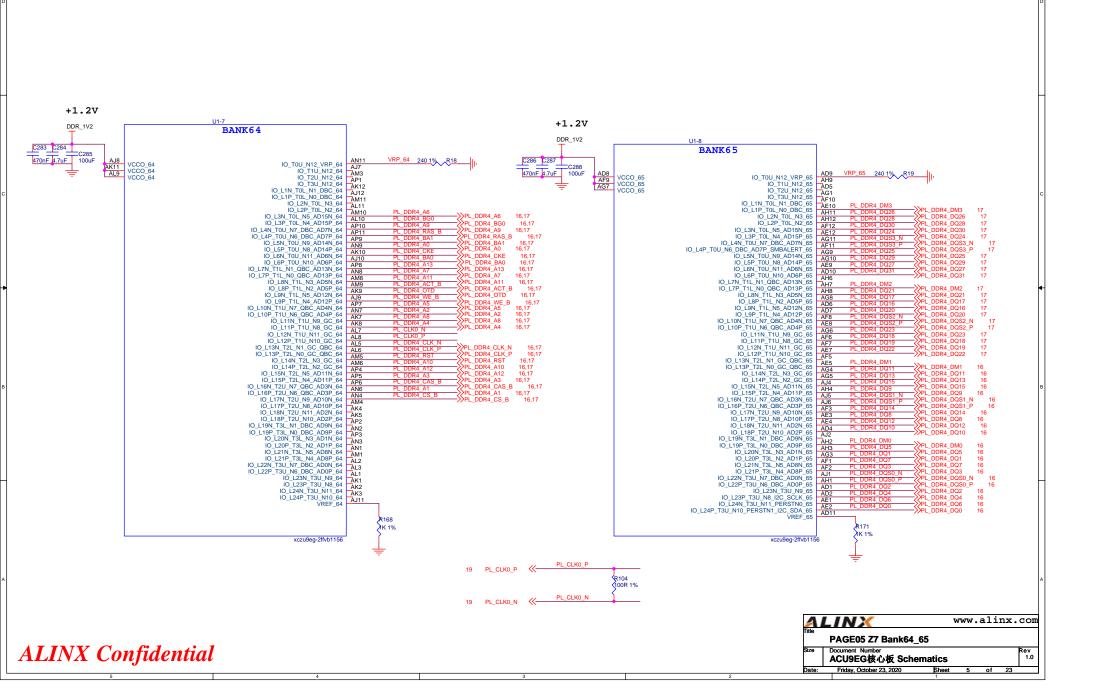


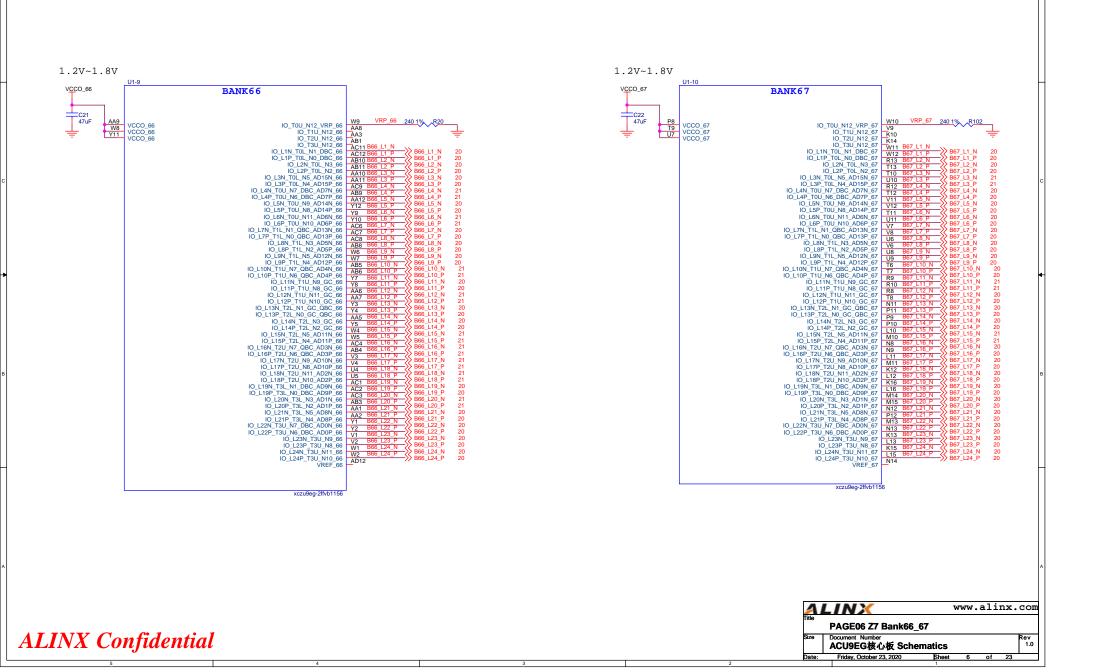


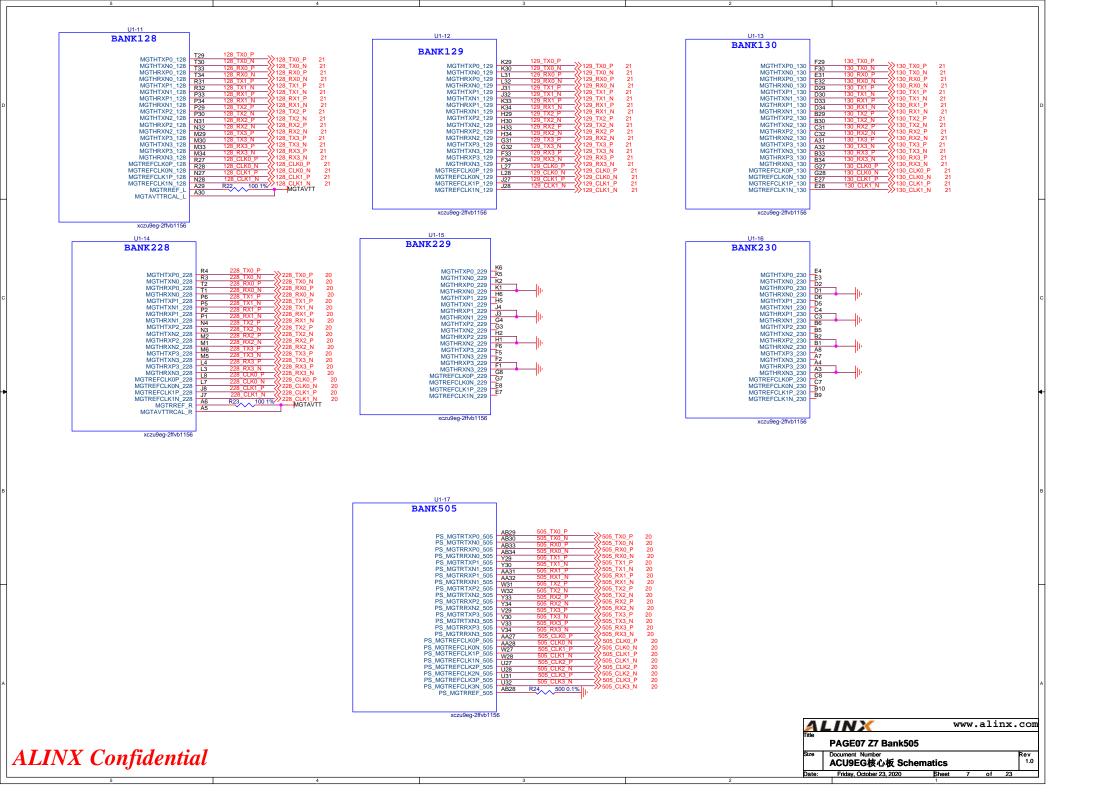


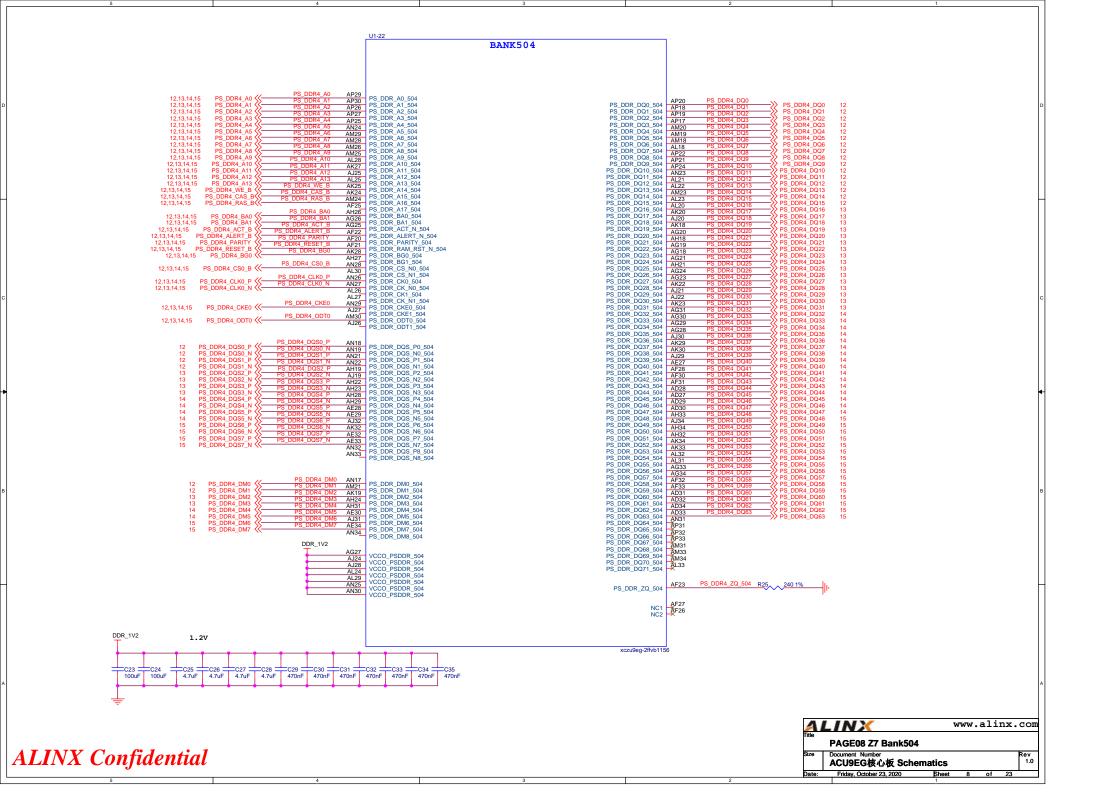


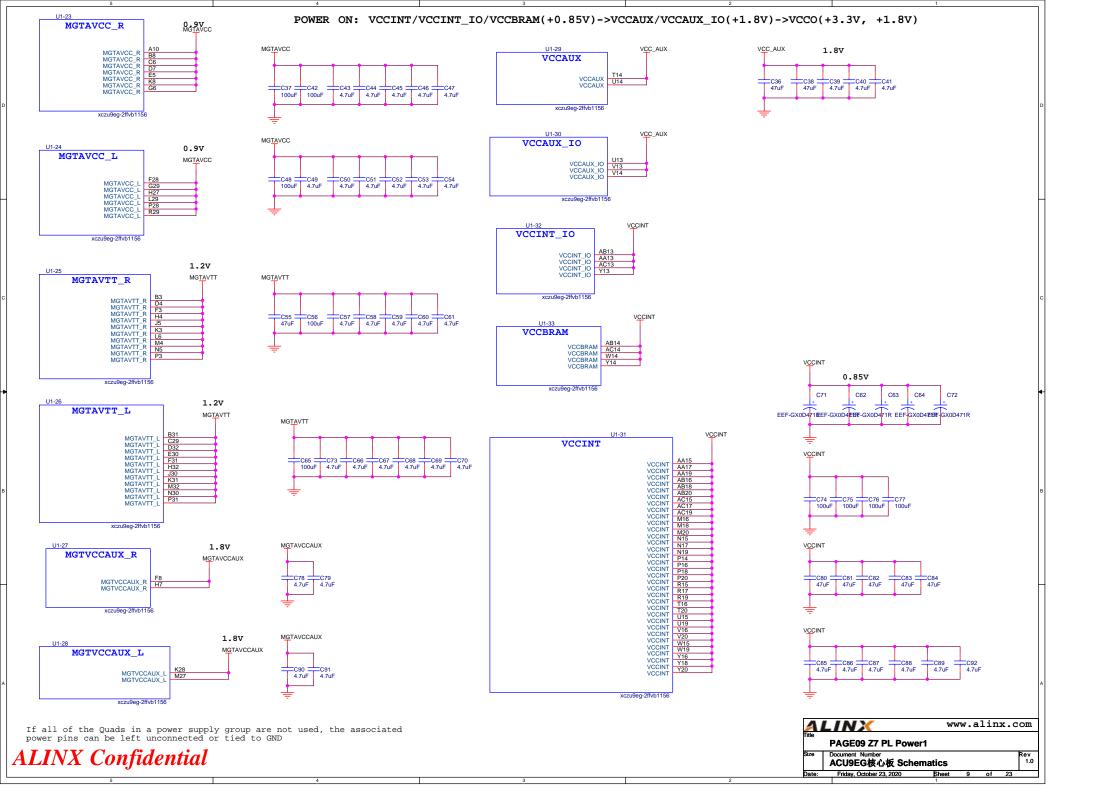




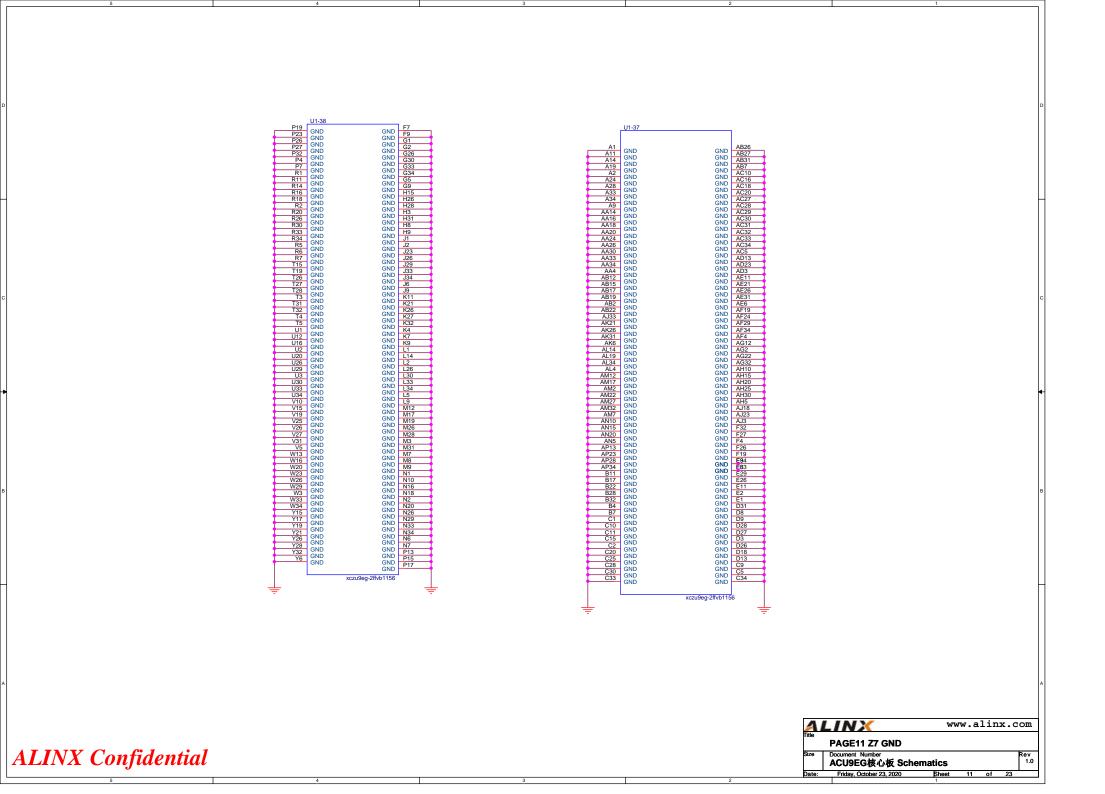


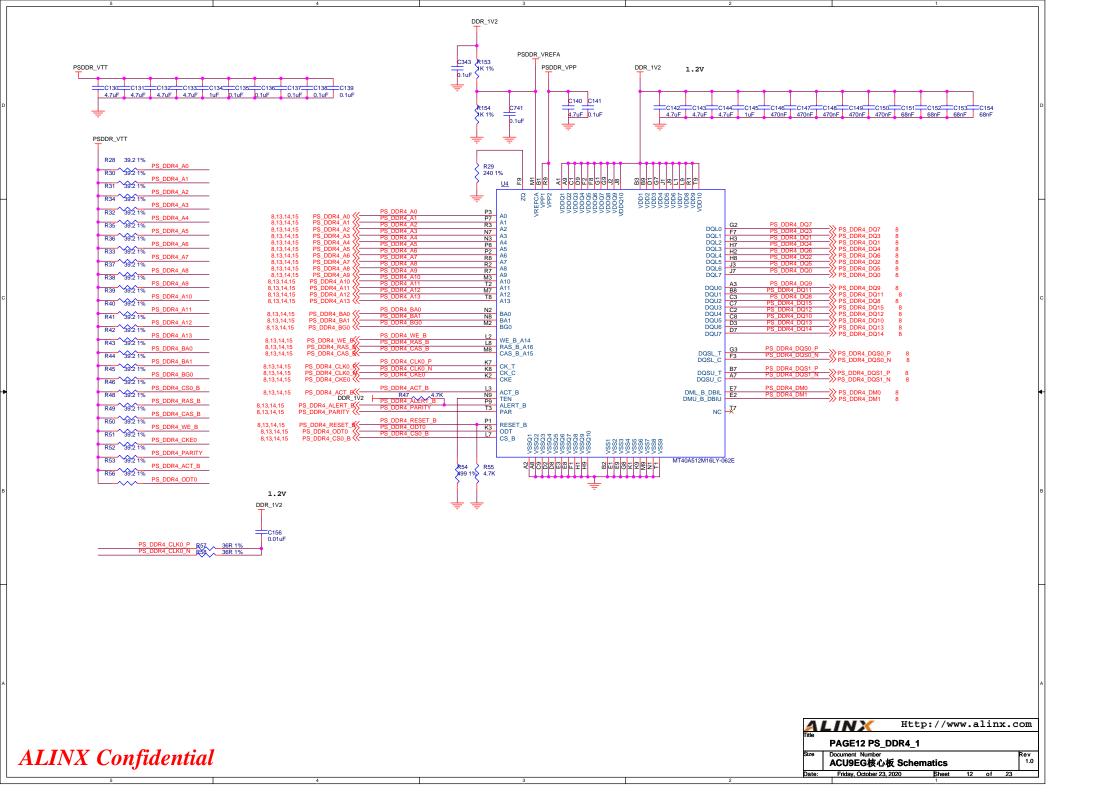


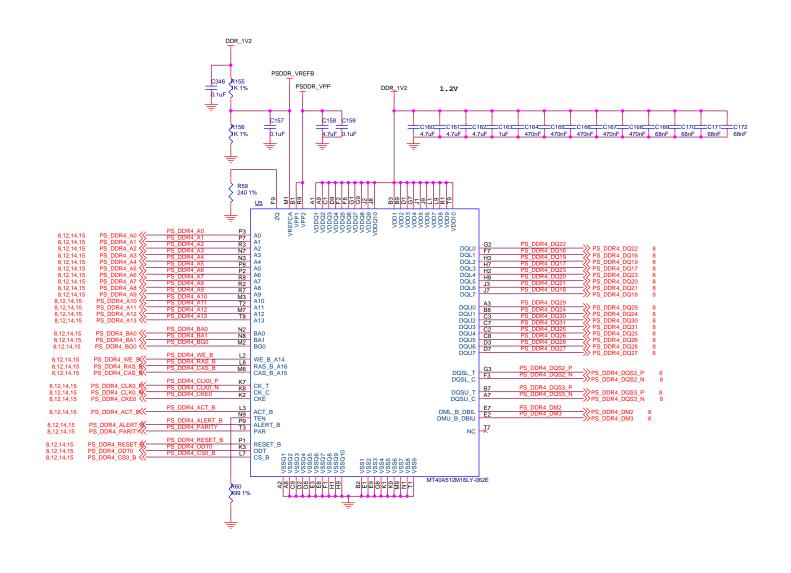




POWER ON: VCC\_PSINTFP\_VCC\_PSINTFP\_DDR(+0.85V)->VPS\_MGTRAVCC(+0.9V), VCC\_PSDDR\_PLL(+1.8V)->VPS\_MGTRAVTT(+1.8V), VCCO\_PSDDR() POWER ON: VCC\_PSINTLP(+0.85V)->VCC\_PSAUX(+1.8V), VCC\_PSADC(+1.8V), VCC\_PSPLL(+1.2V)->VCCO\_PSIO(+1.8V) U1-34 PS\_AVCC PS\_MGTRAVCC PS\_AVCC 0.85V PS MGTRAVCC PS\_MGTRAVCC PS\_MGTRAVCC PS\_MGTRAVCC 4.7uF 4.7uF 470nF 470nF xczu9eg-2ffvb1156 PS\_AVTT U1-35 1.8V PS\_MGTRAVTT PS\_AVTT PS\_MGTRAVTT 470nF 4.7uF 4.7uF PS\_MGTRAVT xczu9ea-2ffvb1156 0.85V PS\_PLL PS\_PLL VCC\_PSINT 1.2V PS\_POWER for VCC\_PSINTLP VCC\_PSINT VCC\_PSPLL VCC\_PSPLL VCC\_PSPLL VCC\_PSINTLP
VCC\_PSINTLP
VCC\_PSINTLP
VCC\_PSINTLP
VCC\_PSINTLP
AC23
AC22
AC21
AC21
AB21 100uF 4.7uF 4.7uF 100uF 100uF 4.7uF 4.7uF VCC\_PSINT VCC\_PSINTLP AB23
VCC\_PSINTLP AA21 VCC PSINTLP 0.85V VCC\_PSINTFP\_DDR VCC\_PSINTFP\_DDR VCC\_PSINT for VCC\_PSINTFP VCC\_PSINTFP\_DDR VCC\_PSINTFP VCC\_PSINTFP VCC\_PSINTFP VCC\_PSINTFP VCC\_PSINTFP AE22 C108 100uF C109 100uF C110 100uF C112 4.7uF =C111 4.7uF 4.7uF 4.7uF VCC\_PS\_DDR\_PLL VCC\_AUX VCC\_PSINTFP VCC\_PSINTFP BLM18SG121TN1 VCC\_PSDDR\_PLL VCC\_PSDDR\_PLL C116 C117 C118 C119 470nF 4.7uF 4.7uF 100uF VCC\_AUX VCC\_AUX 1.8V VCC\_PSAUX VCC\_PSAUX VCC\_PSAUX VCC\_PSAUX →>> VBAT\_IN C120 4.7uF 100uF 4.7uF 4.7uF AA22 VCC\_AUX 100uF 100uF VCC\_PSBATT L3 BLM18SG121TN1 C128 VCC\_PSADC VCC\_PSADC GND\_PSADC GND\_PSADC xczu9eg-2ffvb1156 www.alinx.com ALINX PAGE10 Z7 PS Power2 **ALINX** Confidential Rev 1.0 ACU9EG核心板 Schematics Friday, October 23, 2020





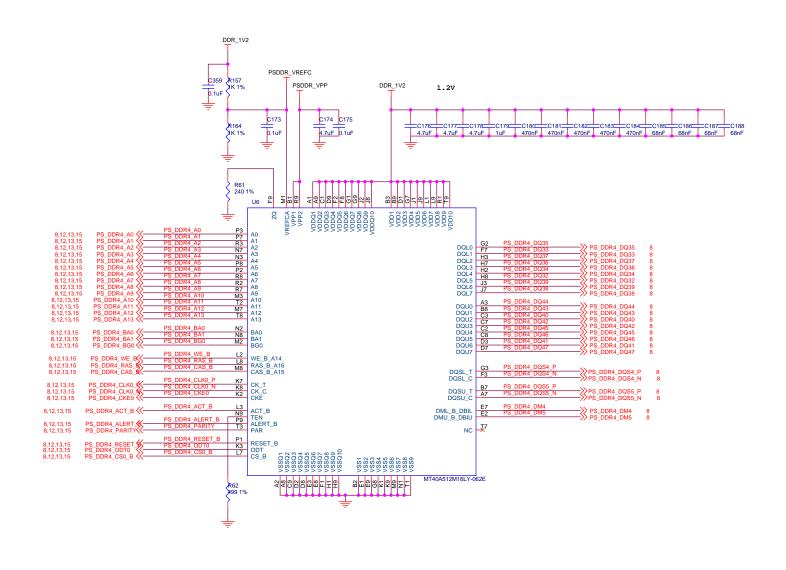


Http://www.alinx.com
Title

PAGE13 PS\_DDR4\_2

Size Document Number ACU9EG核心板 Schematics

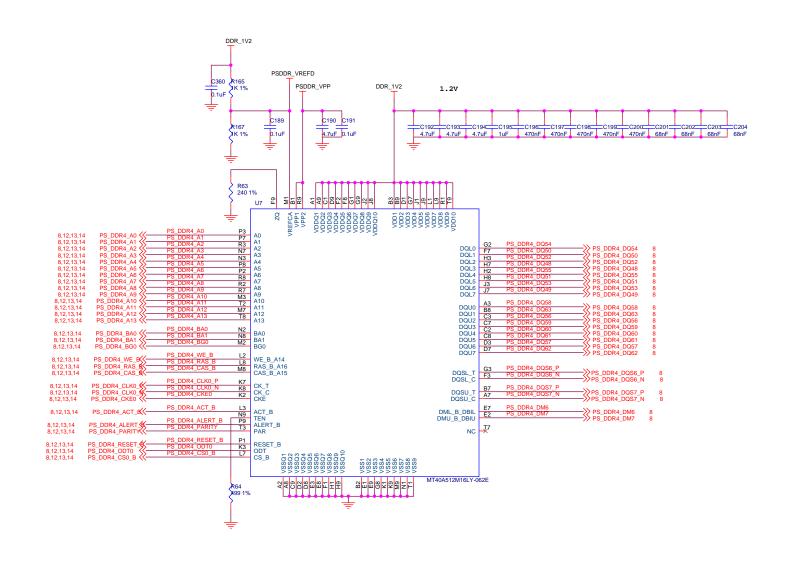
Date: Friday, October 23, 2020 Sheet 13 of 23

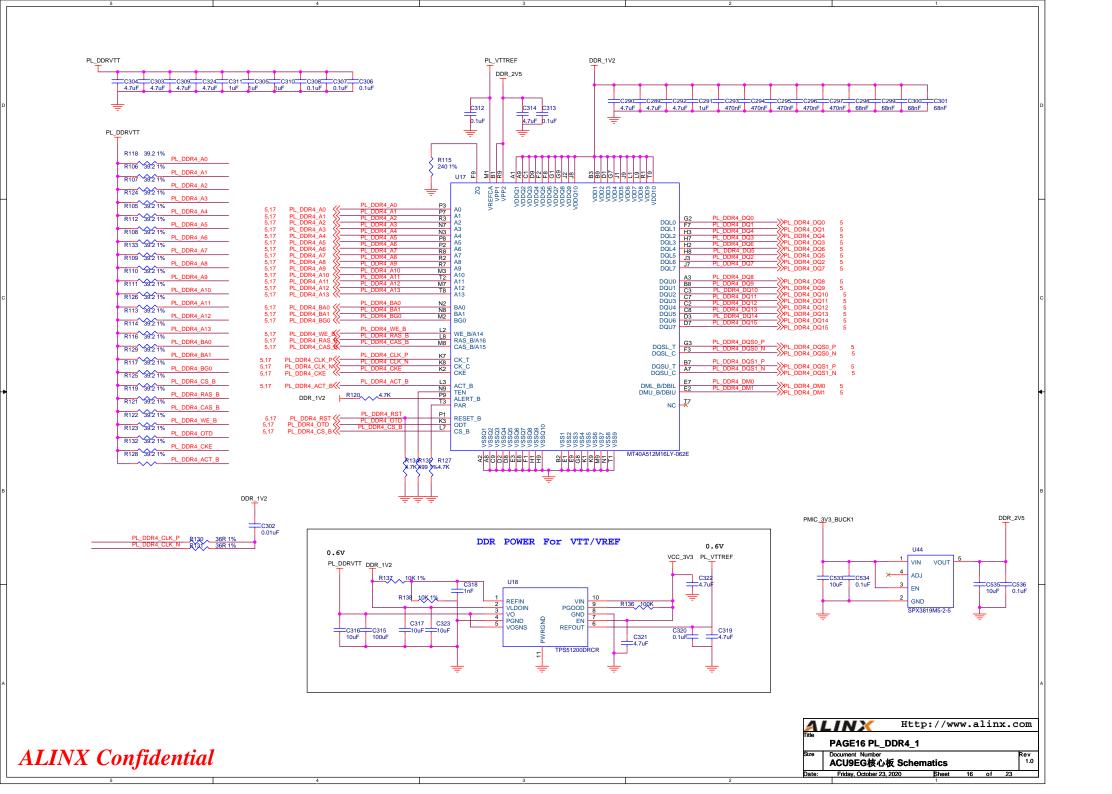


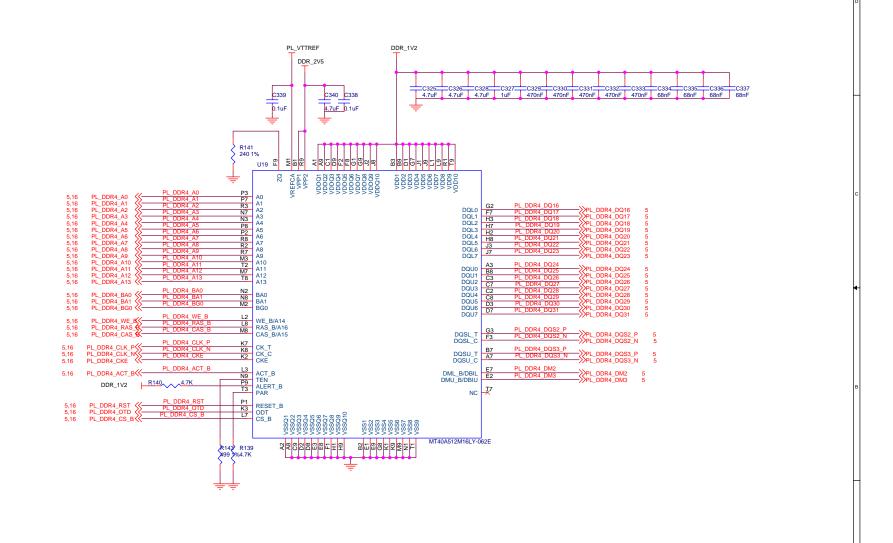
Http://www.alinx.com
Title

PAGE14 PS\_DDR4\_3

Size Document Number ACUSEG核心板 Schematics
Date: Friday, October 23, 2020 Sheet 14 of 23







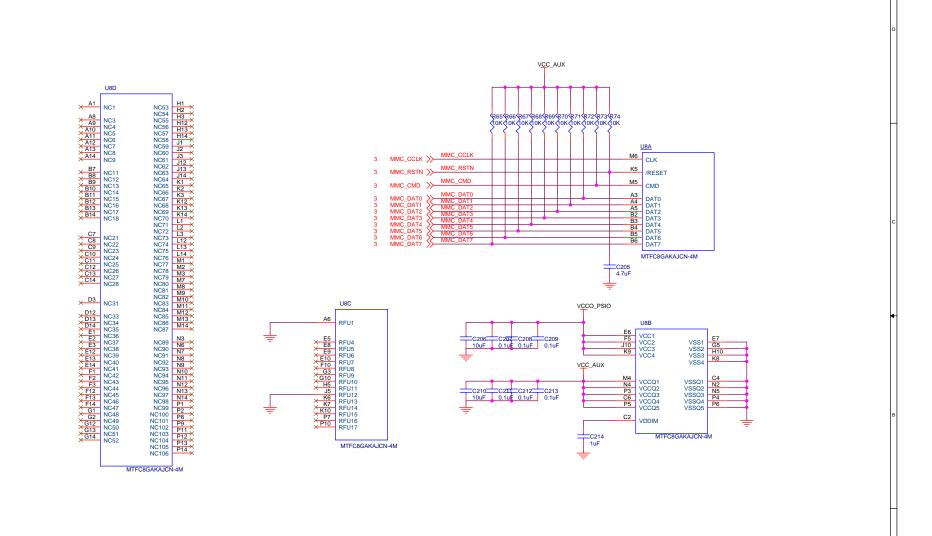
Http://www.alinx.com

Fite

PAGE17 PL\_DDR4\_2

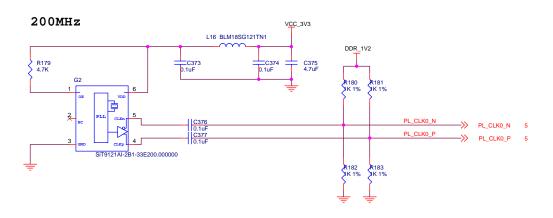
Size
Document Number
ACU9EG核心板 Schematics
Date: Friday, October 23, 2020 Sheet 17 of 23

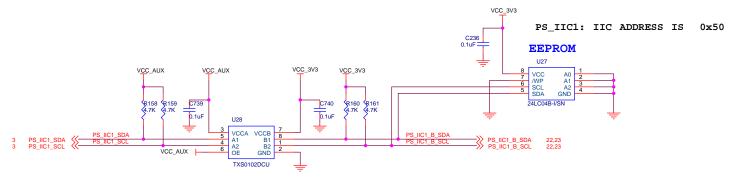
**ALINX Confidential** 

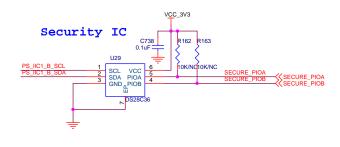


**ALINX Confidential** 

## PL SYSTEM CLOCK







**ALINX Confidential** 

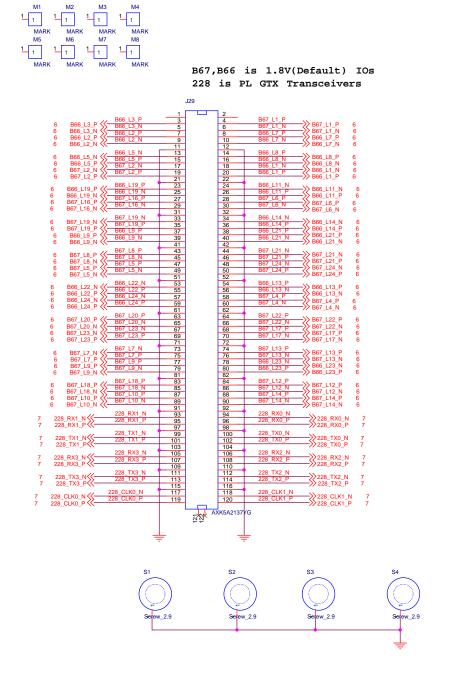
www.alinx.com

Fitle

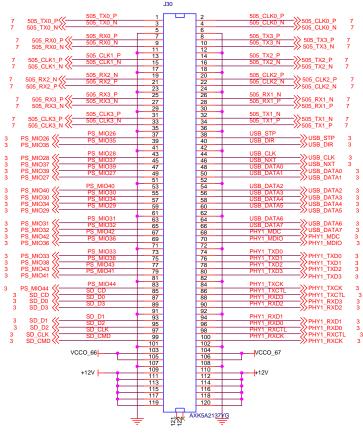
PAGE19 CLOCK

Size Document Number ACU9EG核心板 Schematics

Date: Friday, October 23, 2020 Sheet 19 of 23

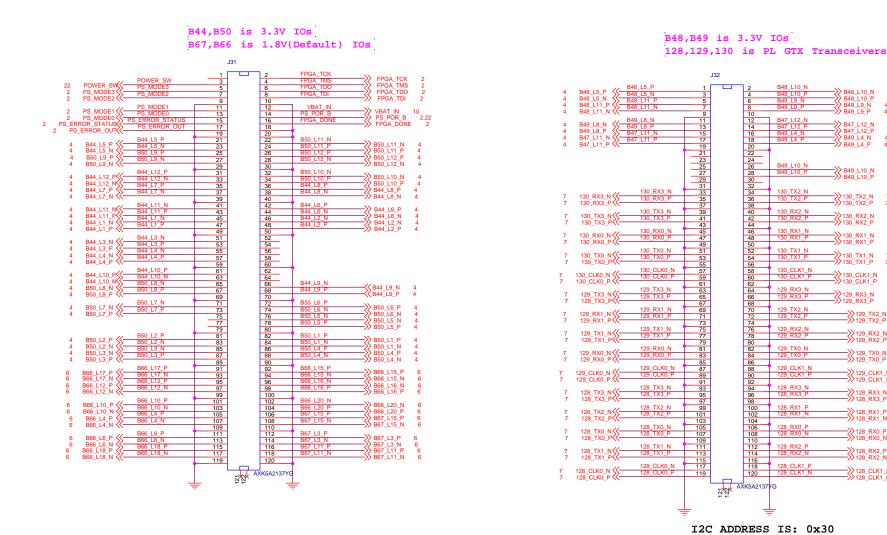


505 is PS-GTR Transceivers PS IO is 1.8V standard



VCCO\_66, VCCO\_67 is provided from mainboard (not exceed 1.8V)

**ALINX Confidential** 





B48\_L10\_N B48\_L10\_P B49\_L9\_N B49\_L9\_P

B47\_L12\_N B47\_L12\_P B49\_L4\_N ₩ B49\_L4\_P

B49\_L10\_N B49\_L10\_P

130\_TX2\_N 130\_TX2\_P

130\_RX2\_N 130\_RX2\_P

130\_RX1\_N 130\_RX1\_P

130\_TX1\_N 130\_TX1\_P

->> 130\_CLK1\_N ->> 130\_CLK1\_P

->> 129\_RX3\_N ->> 129\_RX3\_P

129\_TX2\_N 129\_TX2\_P 129\_RX2\_N 129\_RX2\_P

129\_TX0\_N 129\_TX0\_P

129\_CLK1\_N 129\_CLK1\_P 128\_RX3\_N 128\_RX3\_P

128\_RX1\_P 128\_RX1\_N

128\_RX0\_P 128\_RX0\_N

128\_RX2\_P 128\_RX2\_N

128\_CLK1\_P 128\_CLK1\_N

**ALINX Confidential** 

