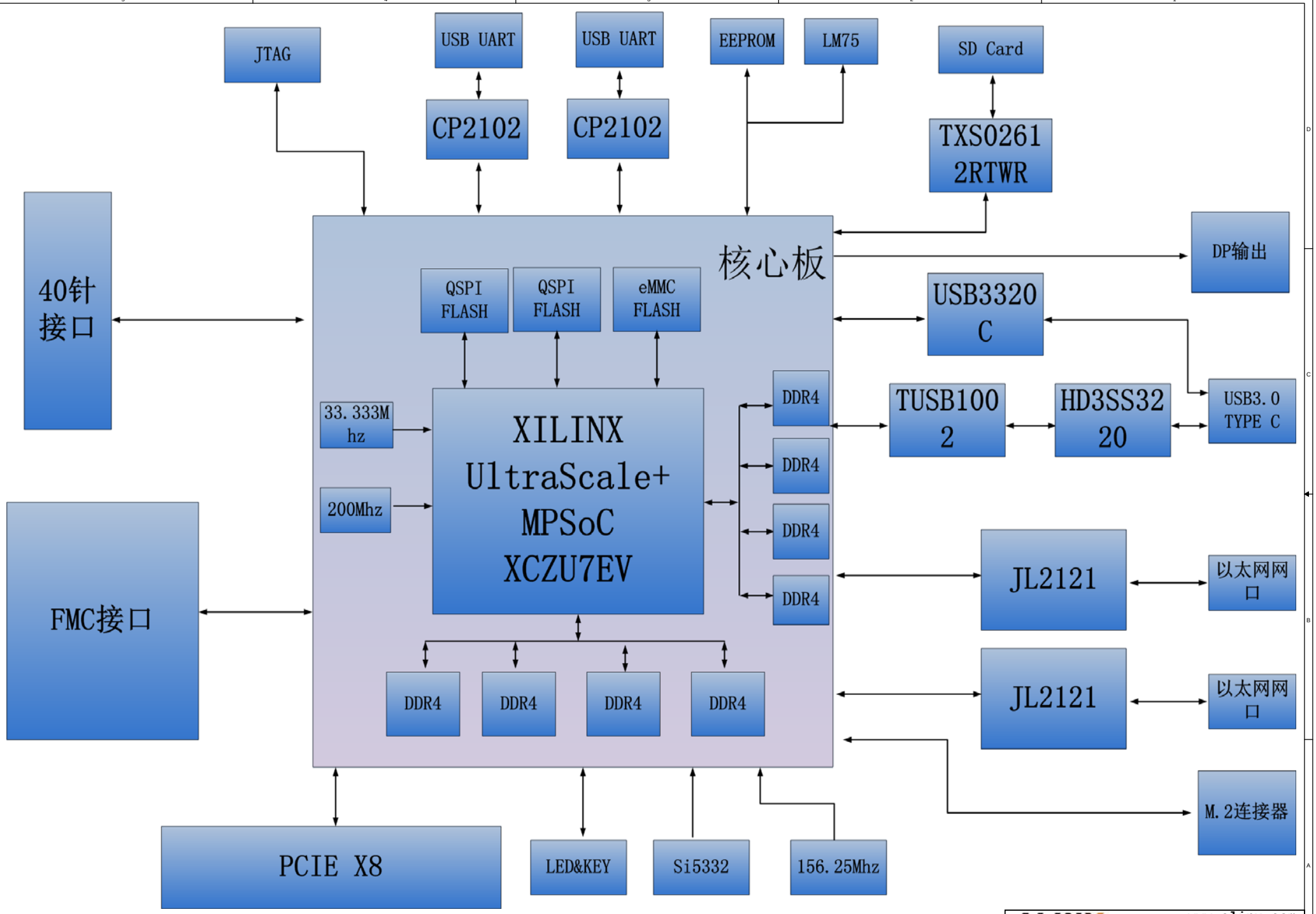

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Title: PAGE01 Block diagram

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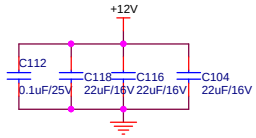
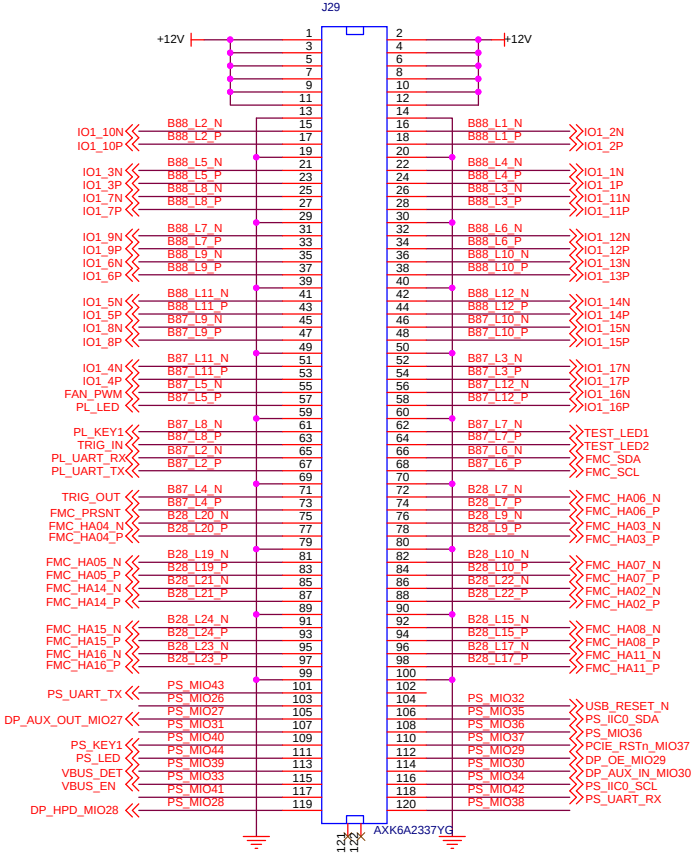
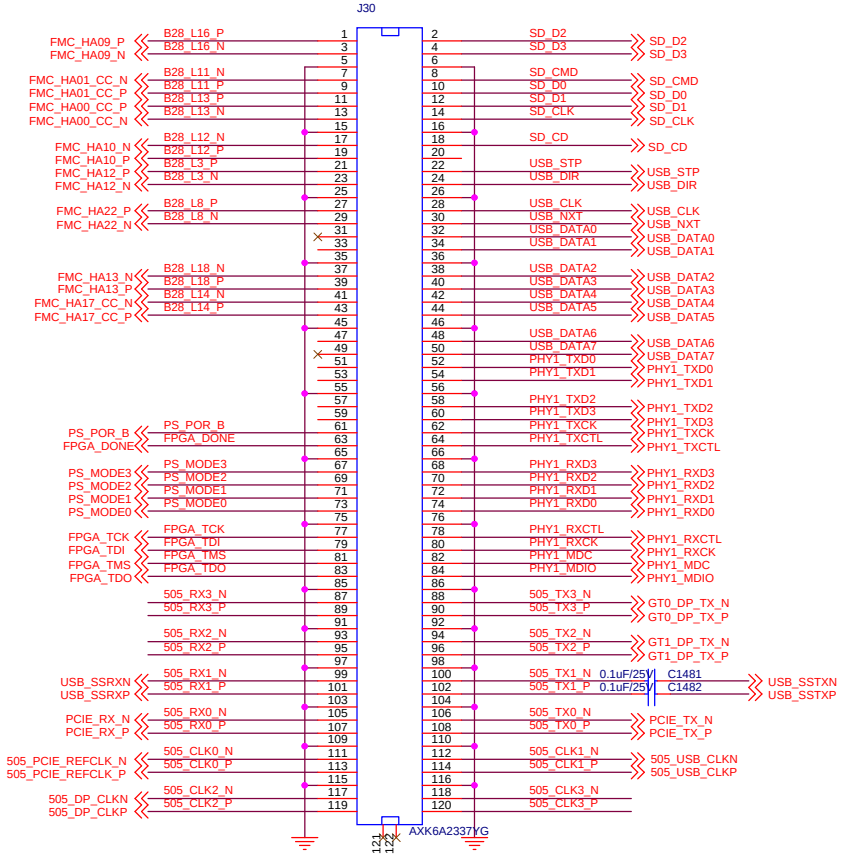


BANK28 IO Voltage is 1.8V Stardard
BANK87,88 IO Voltage is 3.3V Stardard

MIO/SD/USB/ETH IO Voltage is 1.8V Stardard





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Title	PAGE02 Connector_1
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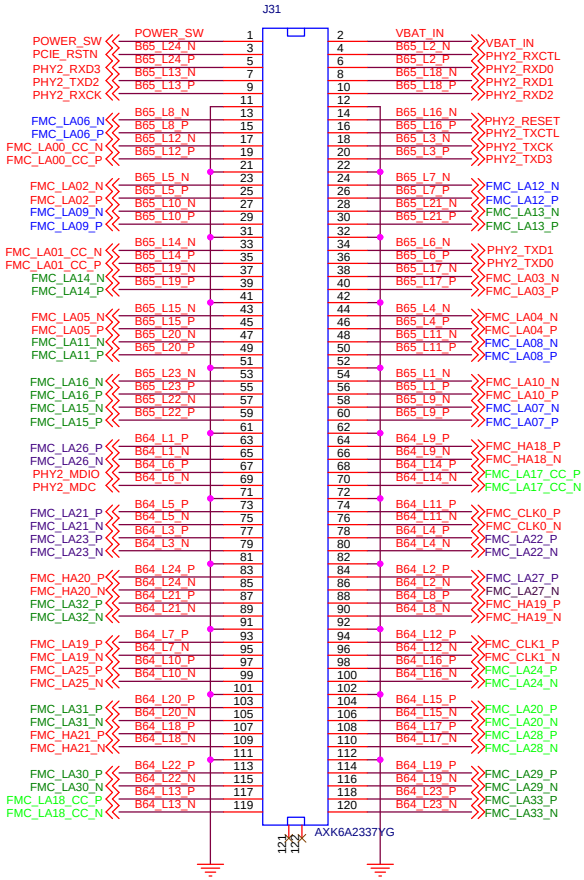

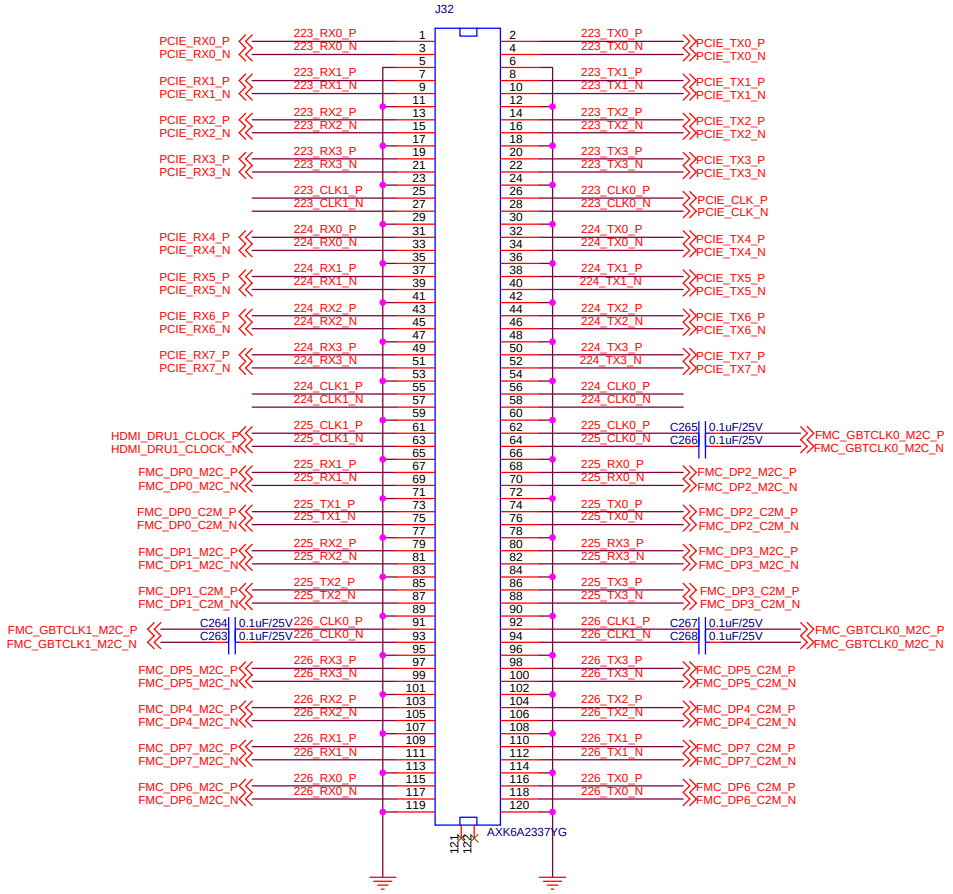

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Title: PAGE03 Connector_2

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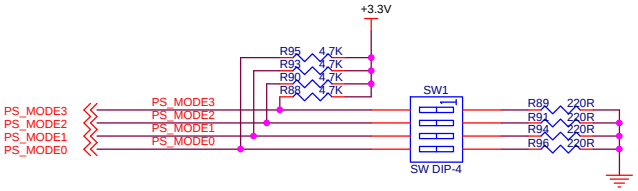
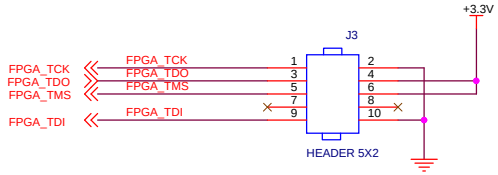
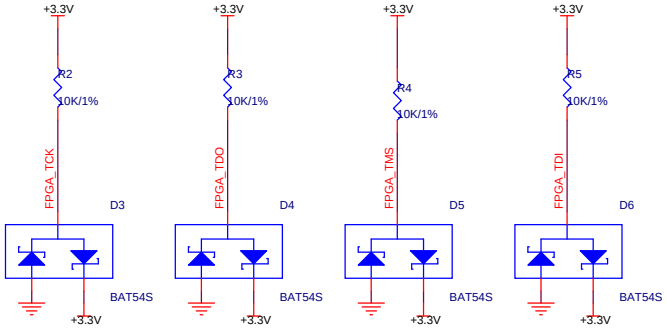
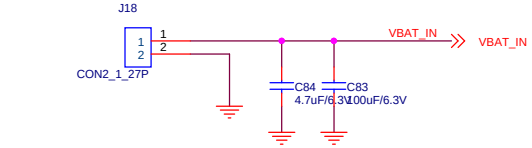
MODE[3:0]	BOOT MODE	Descritpion
0000	PS JTAG	PS JTAG Interface
0001	Quad_SPI(24b)	24-Bit addresssing(QSPI24)
0010	Quad_SPI(32b)	32-Bit addresssing(QSPI32)
0011	SD0(2.0)	SD2.0
0100	NAND	Requires 8-bit data bus width
0101	SD1(2.0)	SD2.0
0110	eMMC(1.8V)	eMMC version 4.5 at 1.8V
0111	USB0(2.0)	USB 2.0 only
1000	PJTAG(MIO #0)	PJTAG connection 0 option
1001	PJTAG(MIO #1)	PJTAG connection 1 option
1110	SD1 LS(3.0)	SD 3.0

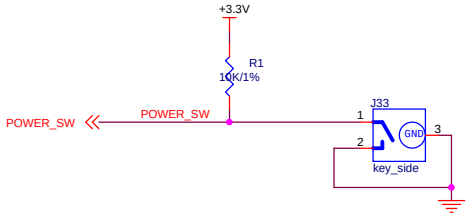


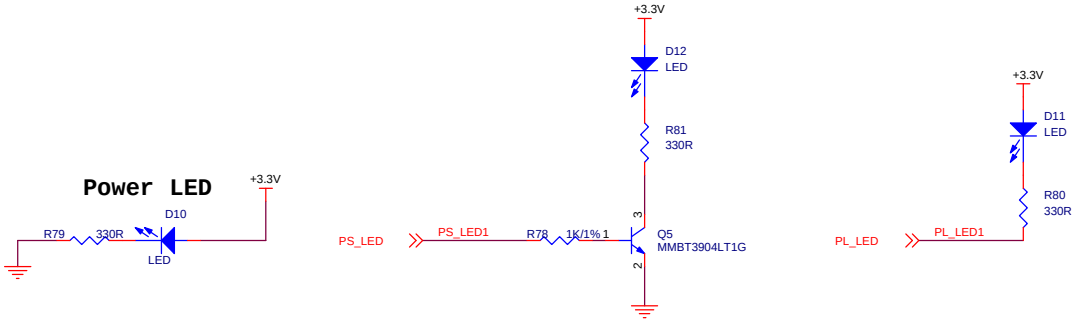
JTAG Connector

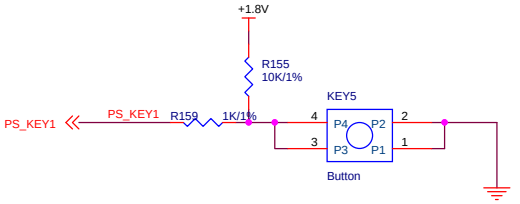




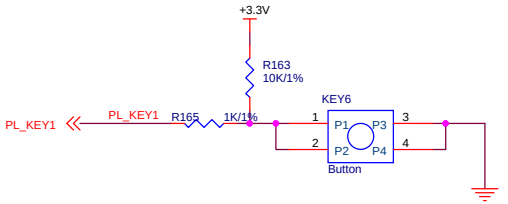








FPGA DONE LED



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Title: Page04 JTAG

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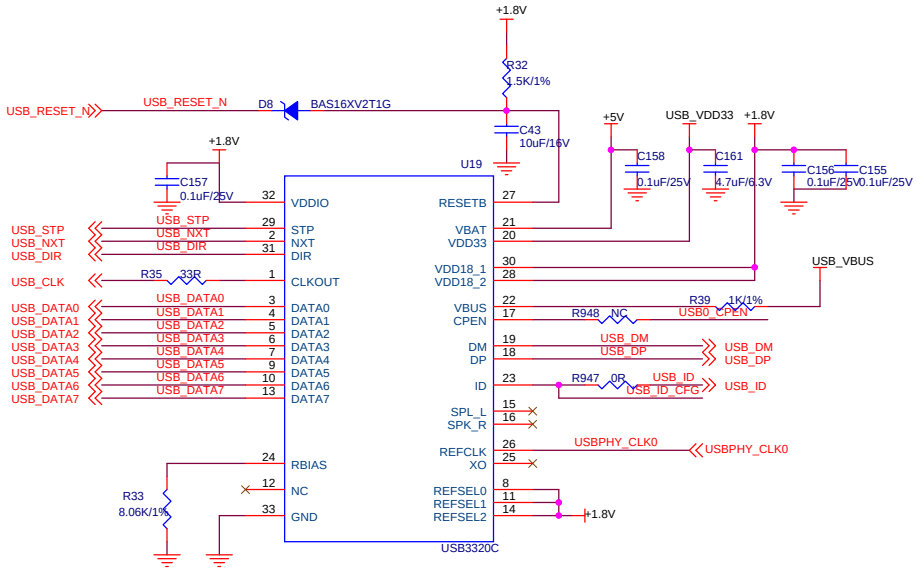
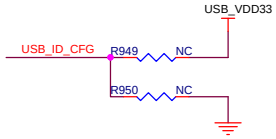
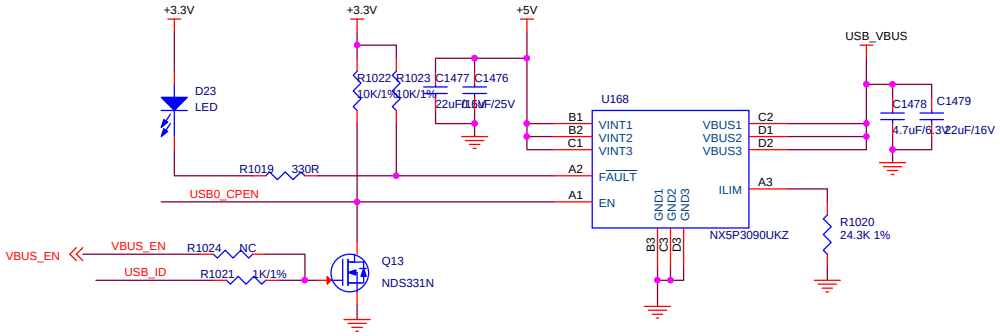
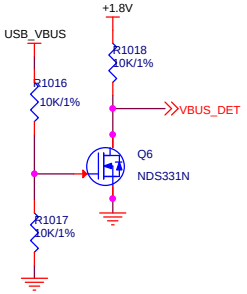


R39=1K: OTG Mode
R39=10K: Slave or HOST Mode







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Title: PAGE05 USB3.0

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U166 TUSB1002RGER

U45 12401610E4#2A

U161 HD3SS3220IRNHR

U163 U164 U162 TPD4E05U06DQAR

I2C 7-bit address is 0x67

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Title	PAGE06 HUB
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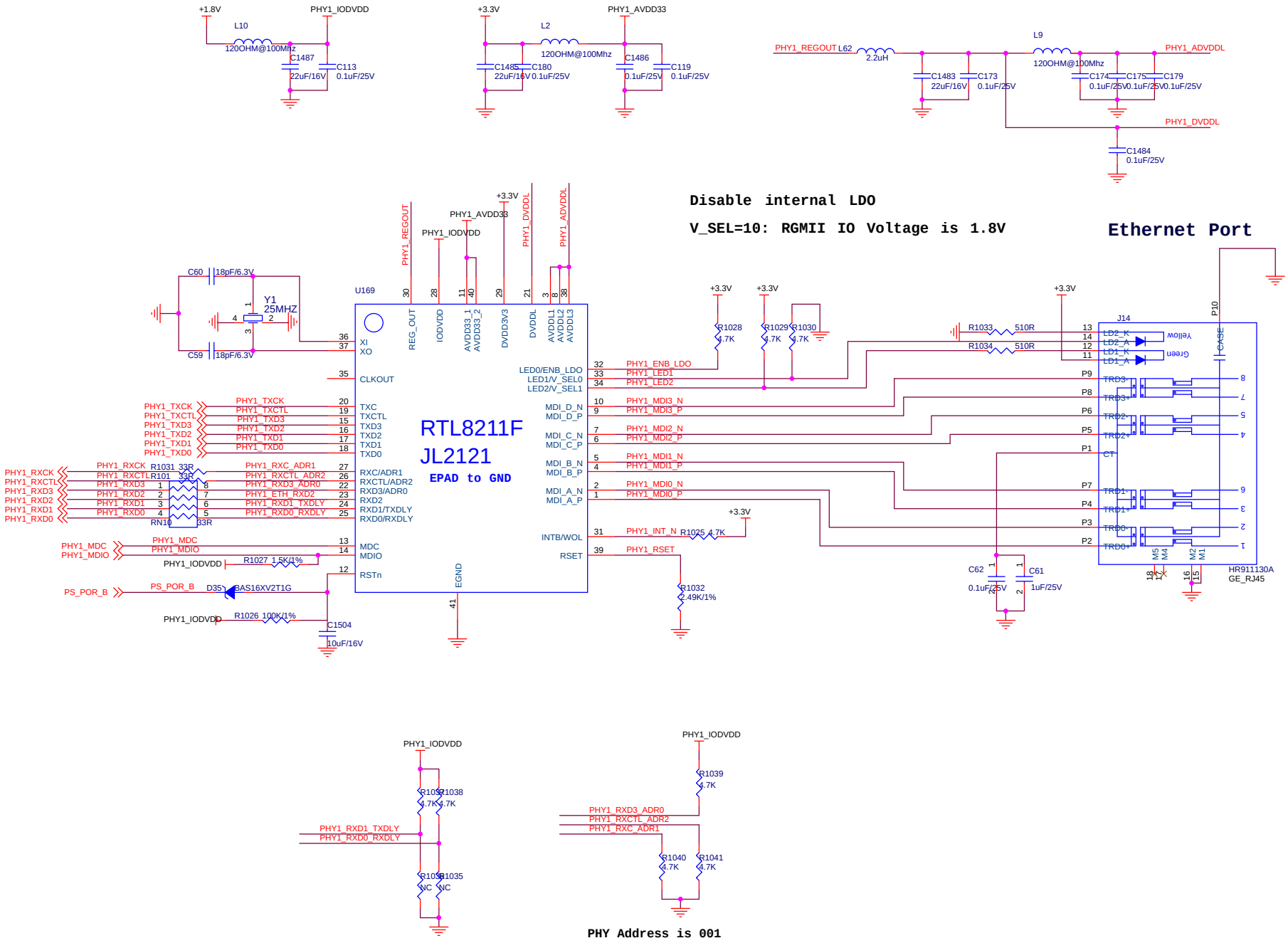

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Title	PAGE07 PS Ethernet1
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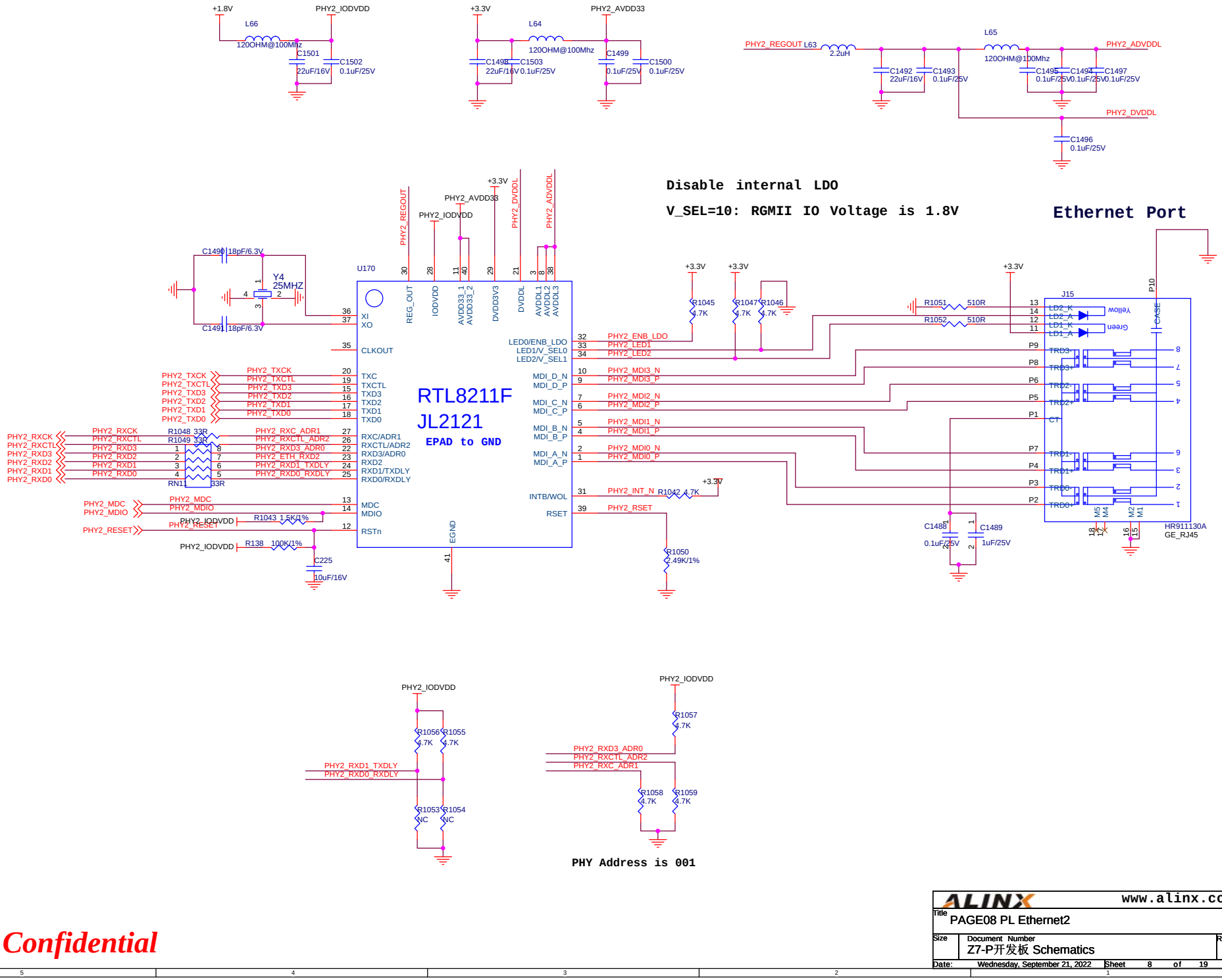

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ALINX	www.alinx.com
Title	PAGE08 PL Ethernet2
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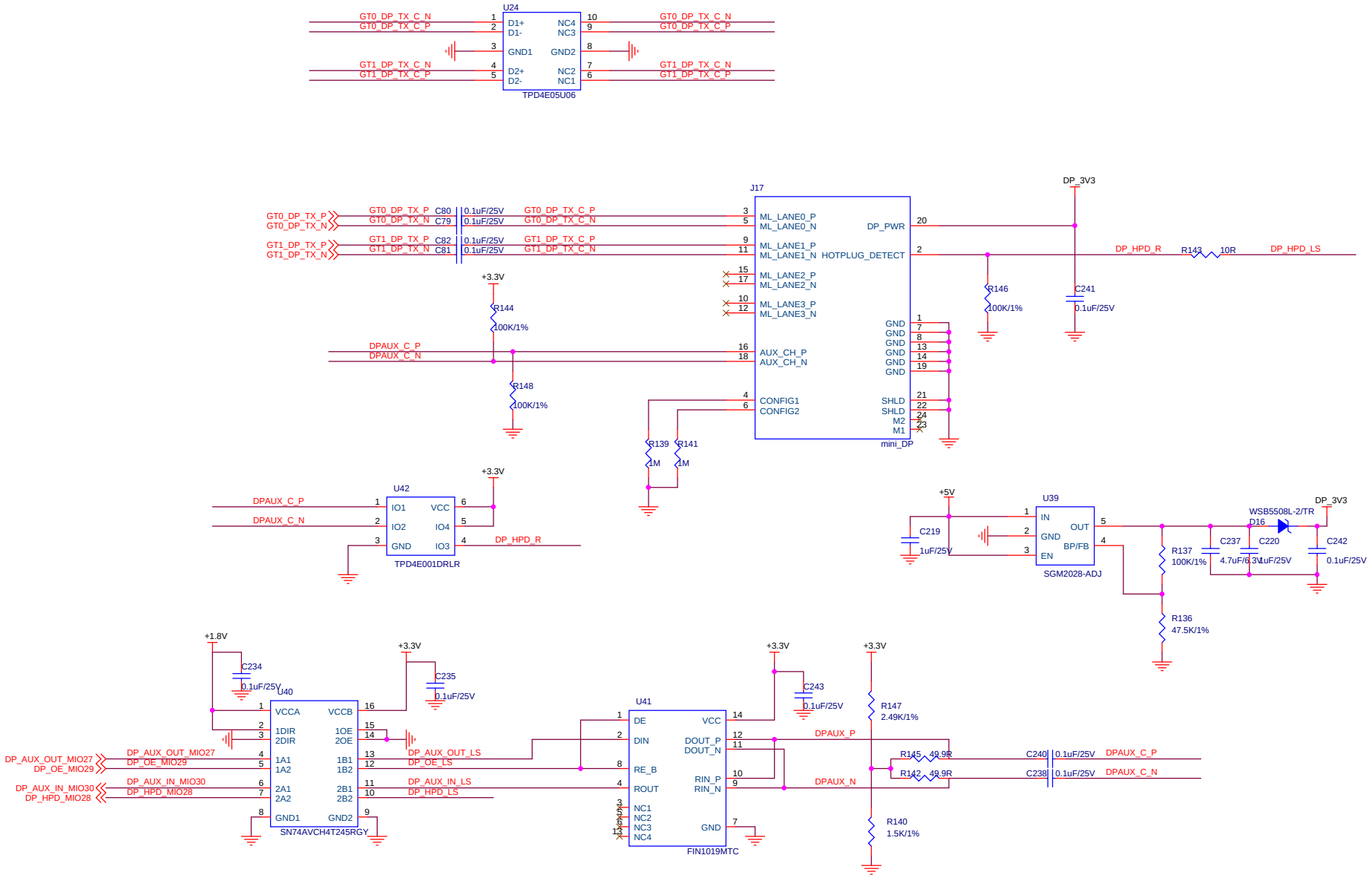

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Title: PAGE09 Display Port

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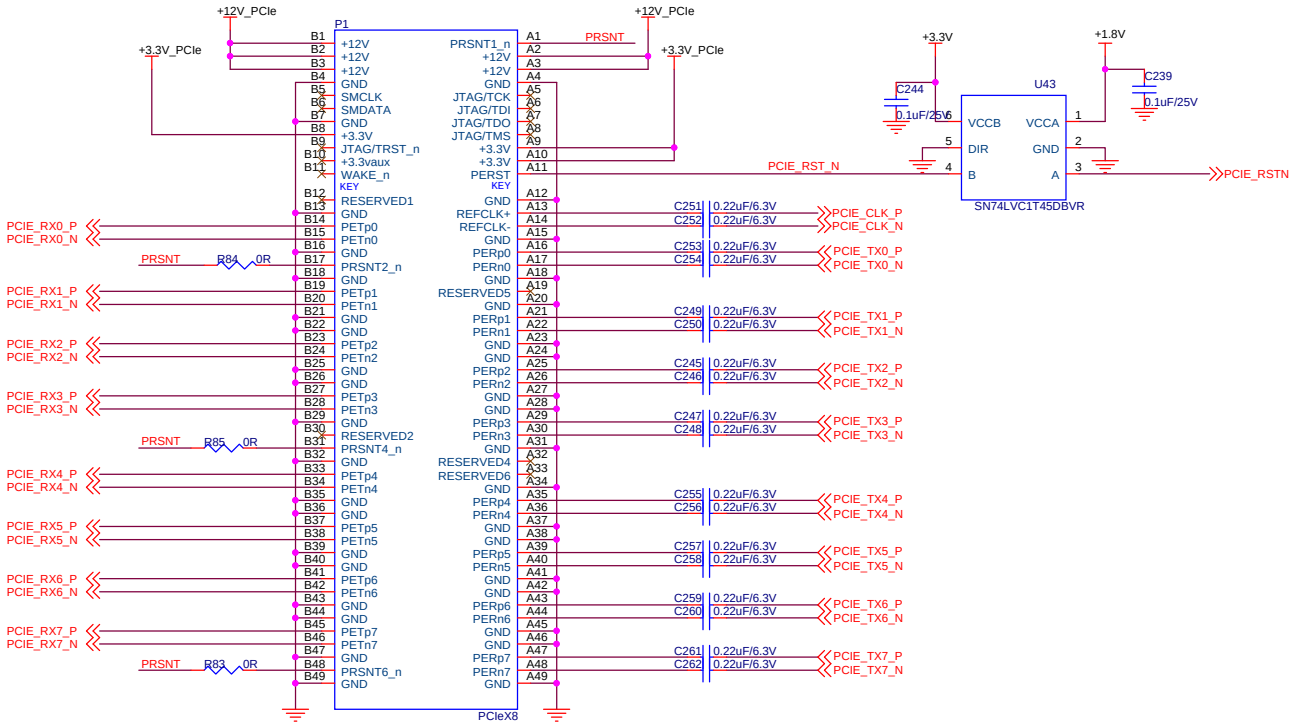
PCIE X8 SLOT



ALINX	www.alinx.com	
Title: PAGE10 PCIE		
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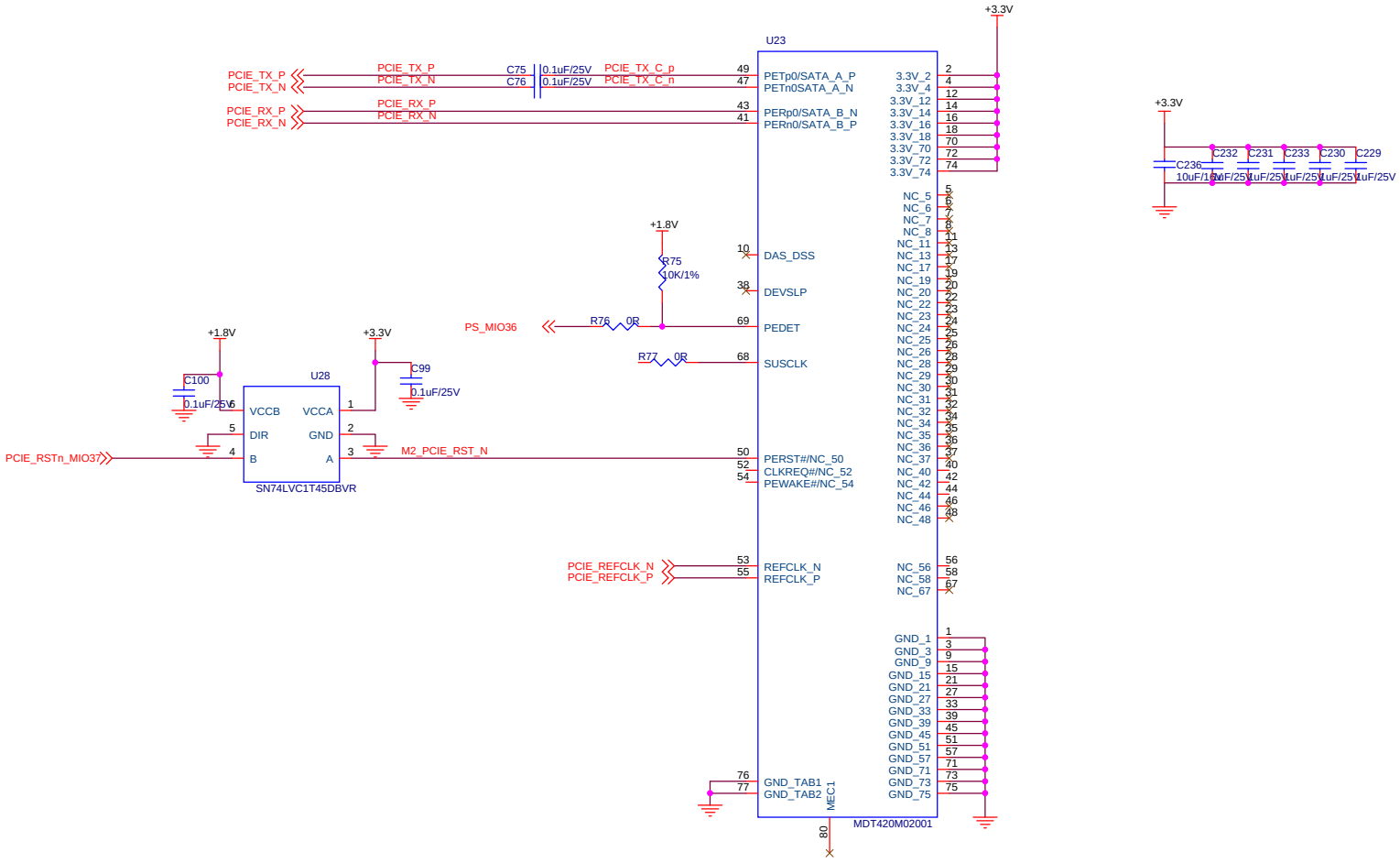

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Title	PAGE11 M.2
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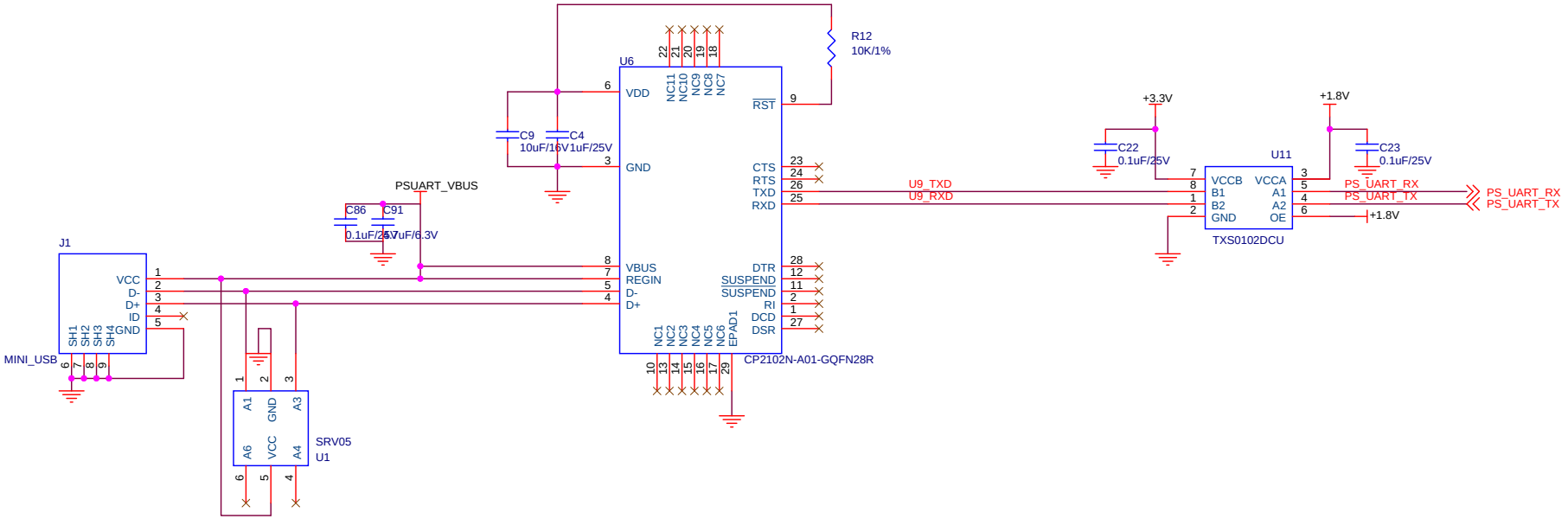
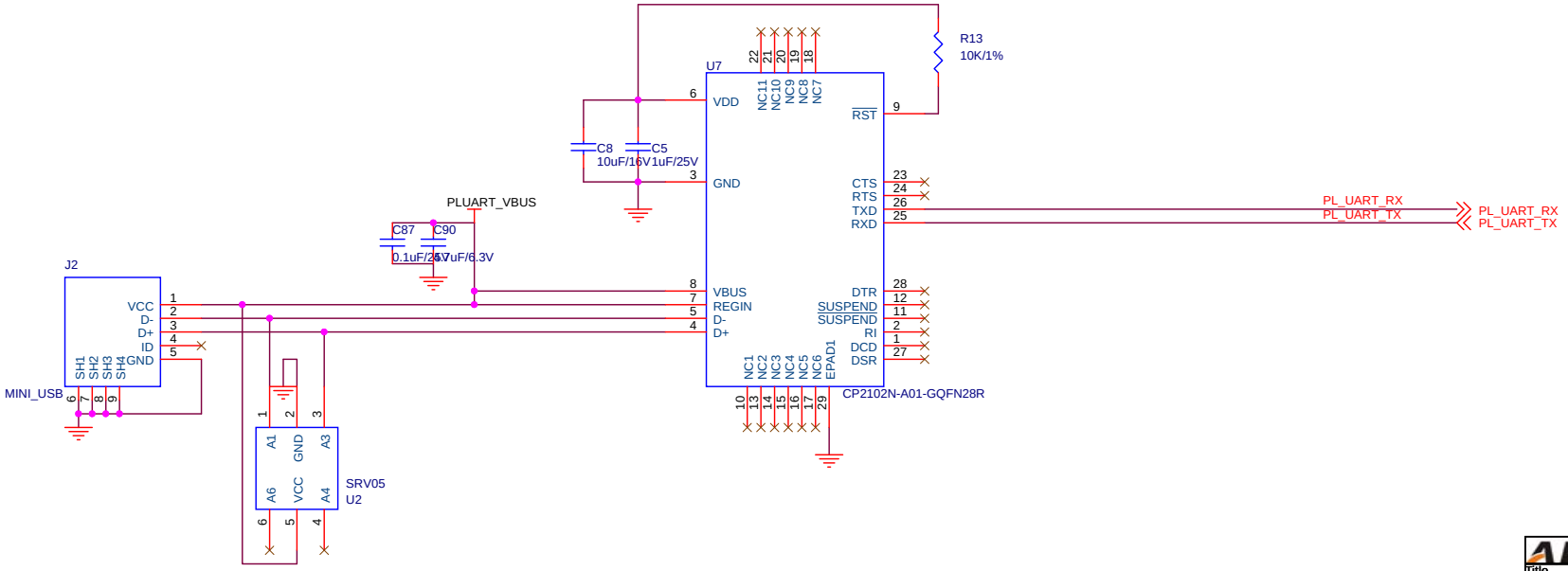
PS UART PORT



PL UART PORT



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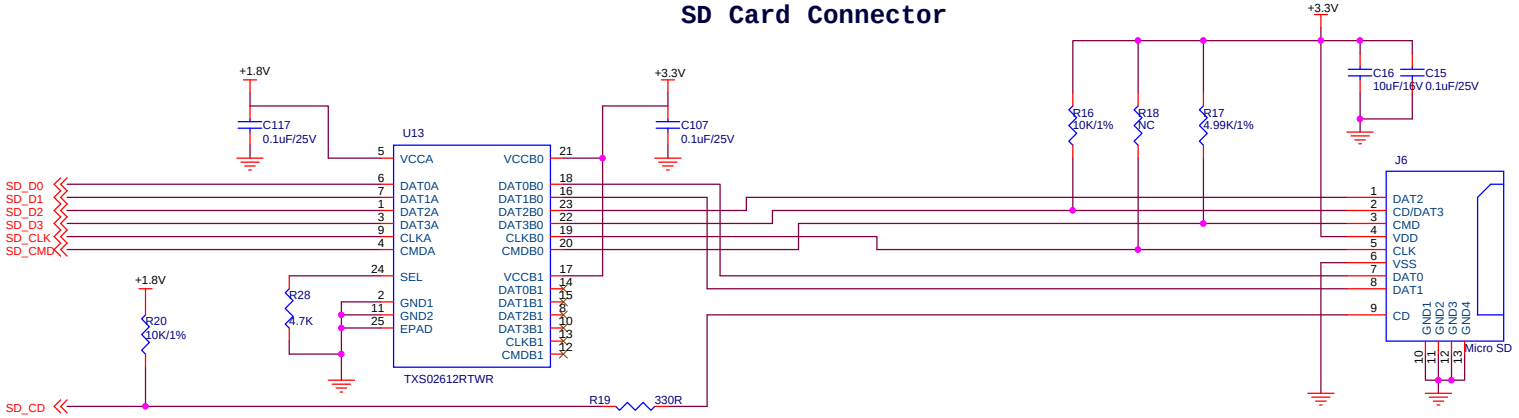
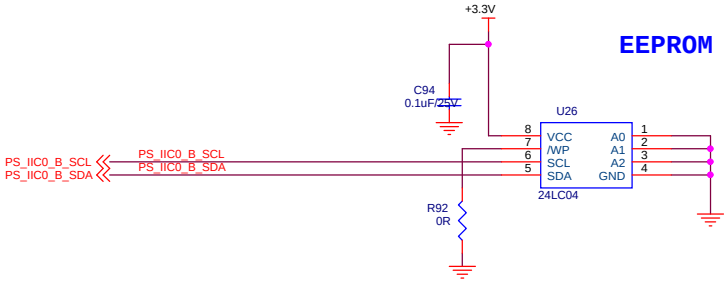
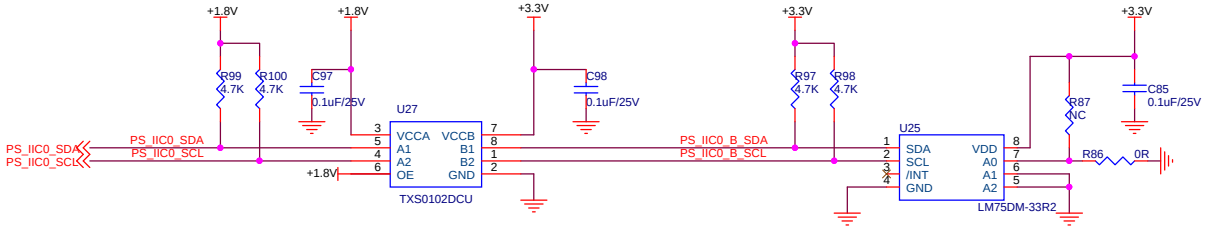
SD Card Connector



EEPROM



SENSOR



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Title: PAGE13 SD & EEPROM & Sensor

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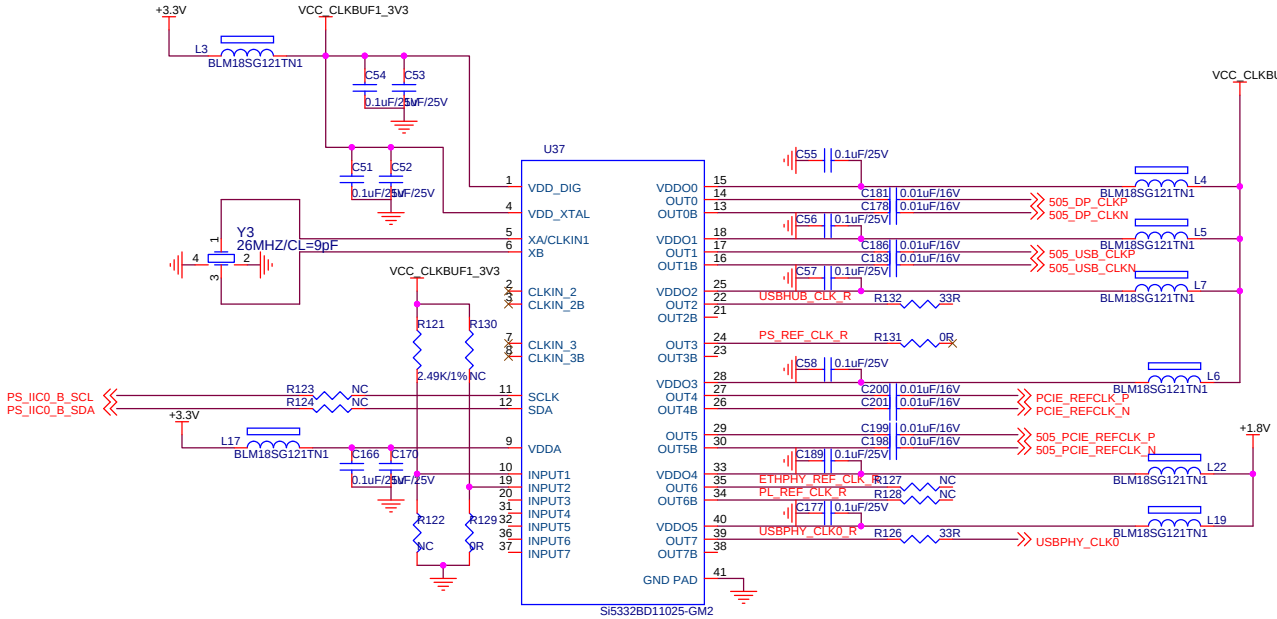


DP CLOCK = 27Mhz

USB CLOCK = 26Mhz

USB HUB CLOCK = 25Mhz

PS REF CLOCK = 33.3333Mhz

PCIE REF CLOCK = 100Mhz

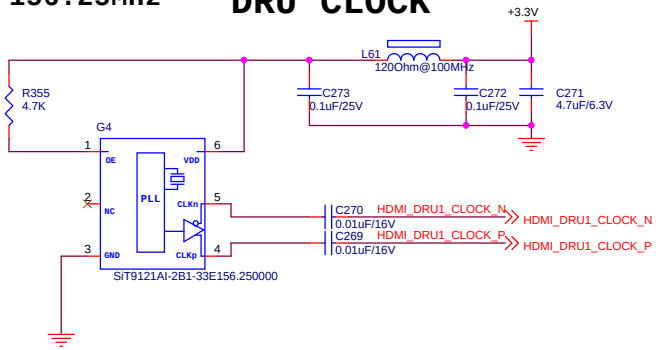
PCIE REF CLOCK = 100Mhz

ETHPHY REF CLOCK = 25Mhz

USBPHY CLOCK = 24Mhz

PS_IIC1: IIC ADDRESS IS 0x76

156.25MHz DRU CLOCK



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Title: PAGE15 CLOCK

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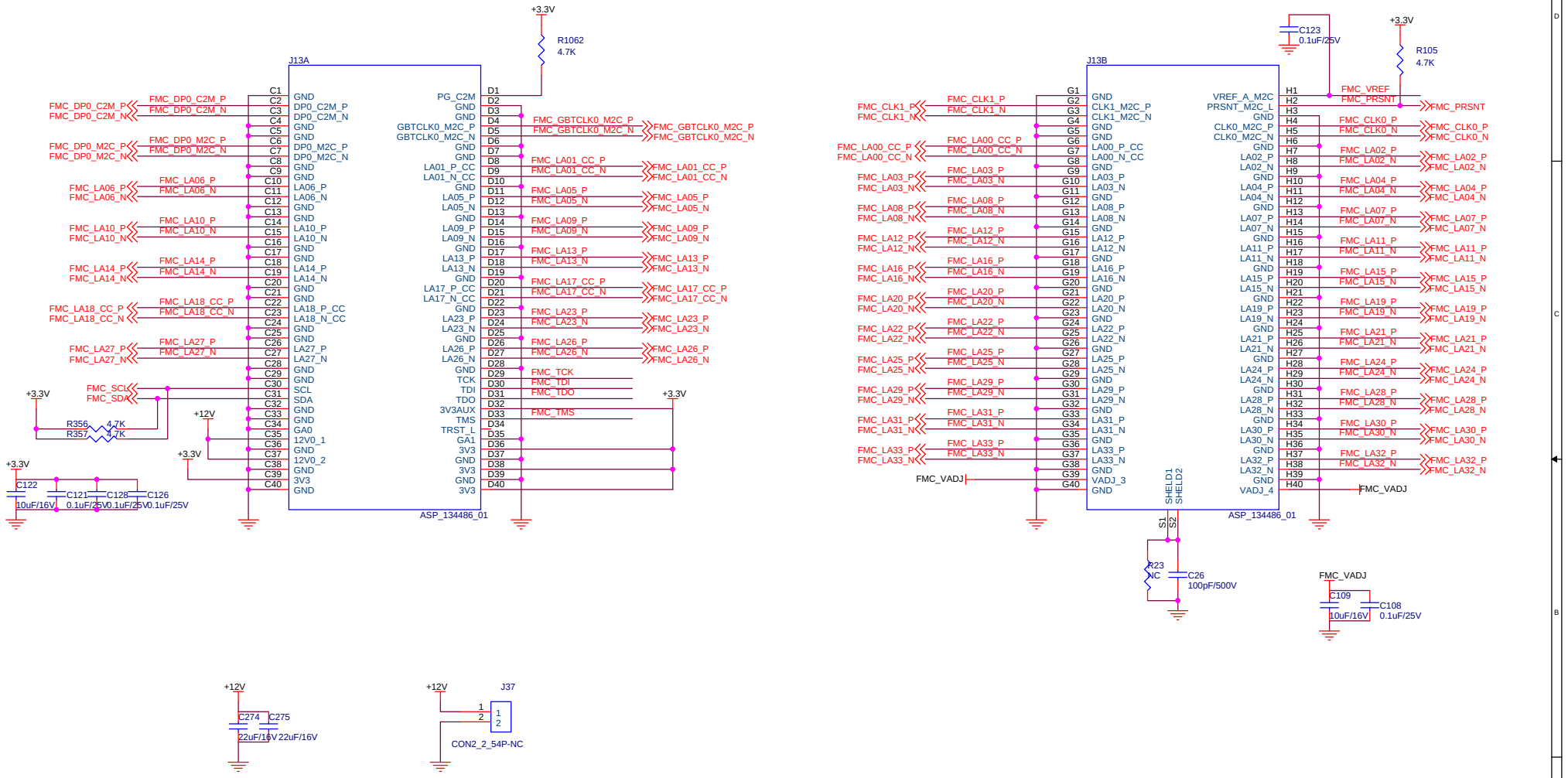

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Title: PAGE16 FMC_HPC1

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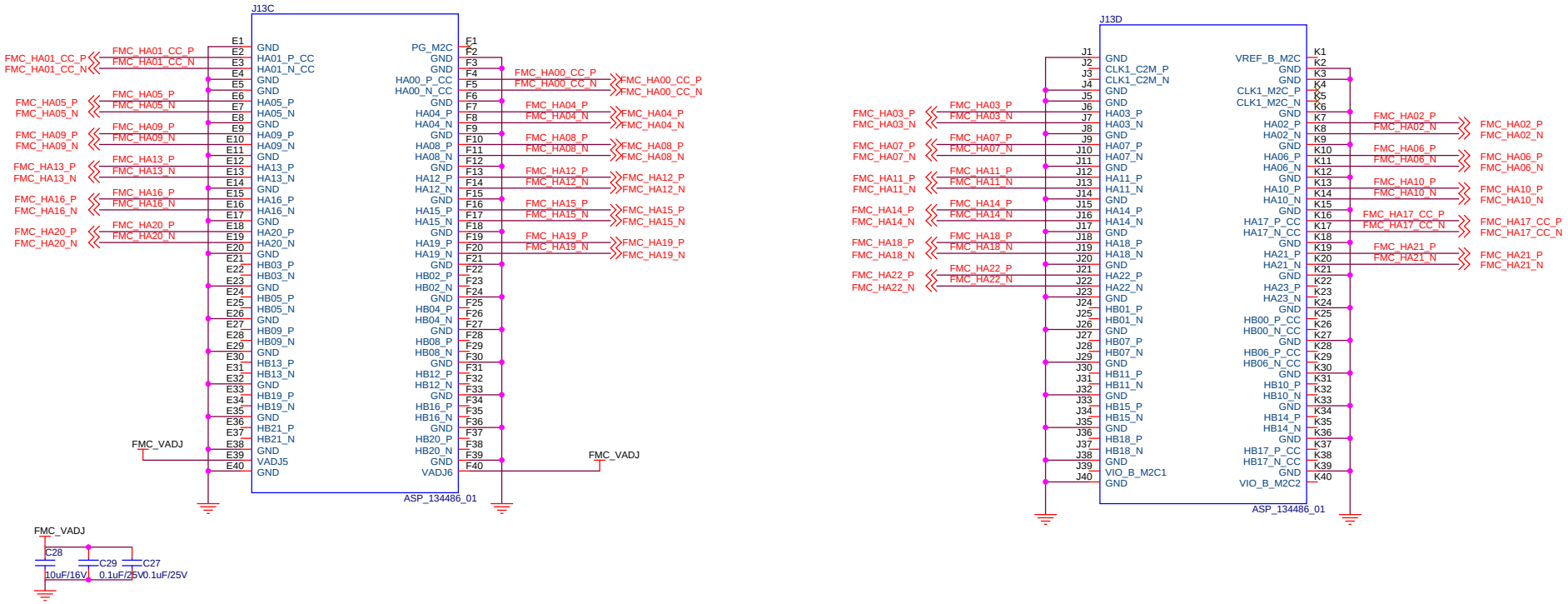

ALINX www.alinx.com		
Title: PAGE17 FMC_HPC2		
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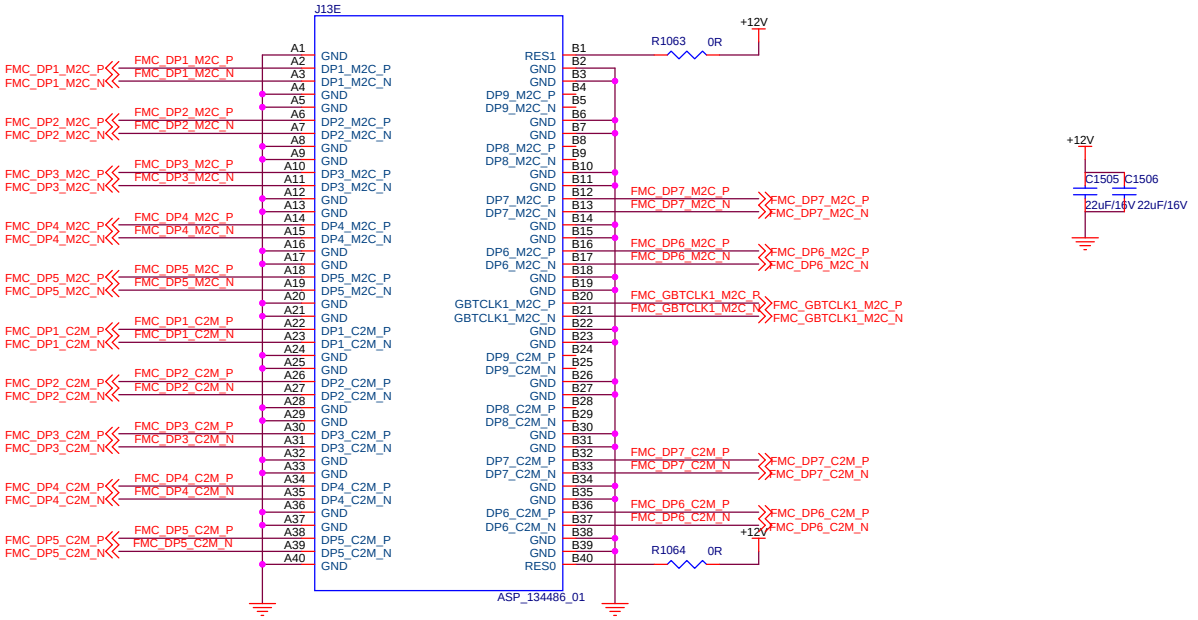

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Title: PAGE18 FMC_HPC3		
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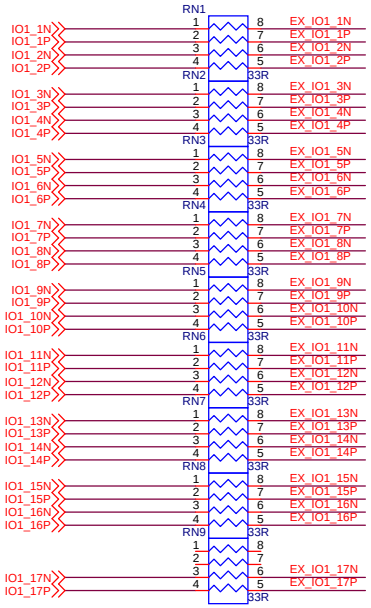
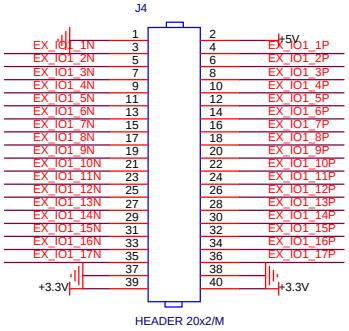
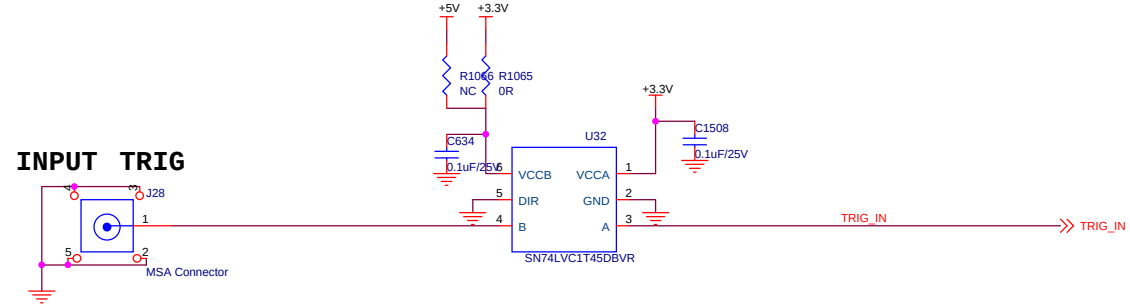


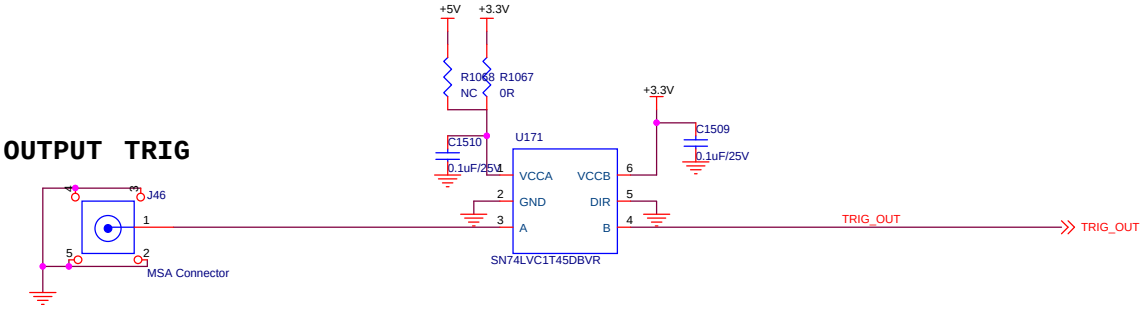
FPGA 40 PIN External IO



INPUT TRIG



OUTPUT TRIG



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Title	PAGE22 EXTEND IO	
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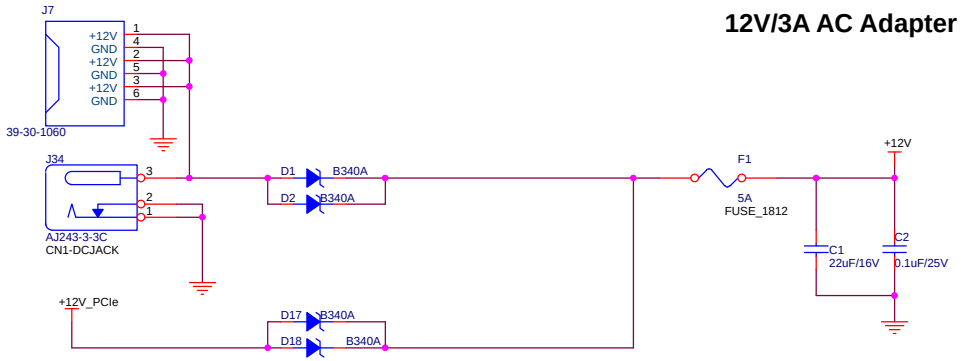
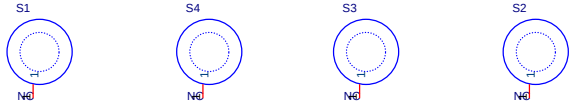
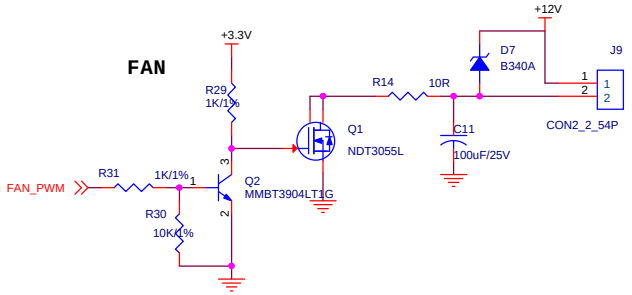
12V/3A AC Adapter

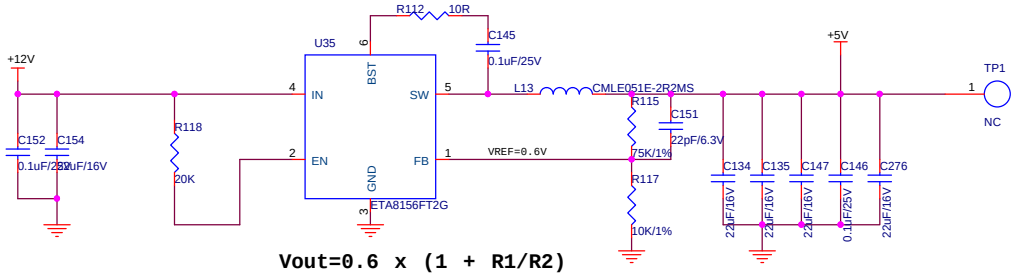




FAN

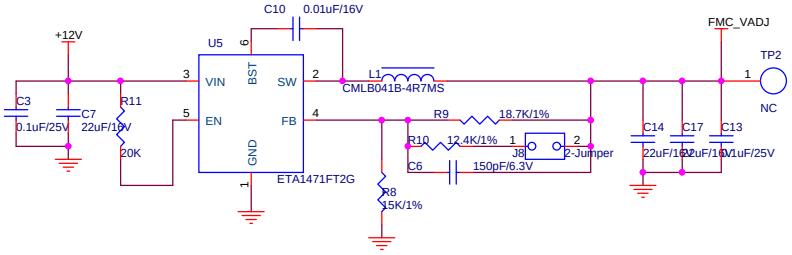


+5V POWER



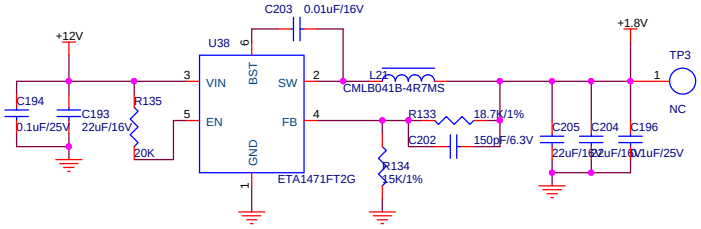
Vout=0.6 x (1 + R1/R2)

1.8V or 1.2V POWER 3A



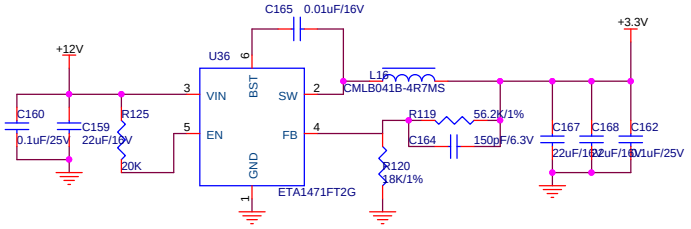
Vout=0.8 x (1 + R1/R2)

+1.8V POWER

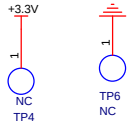


Vout=0.8 x (1 + R1/R2)

+3.3V POWER



Vout=0.8 x (1 + R1/R2)



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