NTNU

Norwegian University of
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NFC PCB with external Antenna
Project report in TTK8

Ali Aljumaili

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Norwegian University of Science and Technology
Department of Engineering Cybnertics

Summary

Near field communication (NFC) allows two electronic devices to communicate wirelessly by bringing them close to each other. NFC has become widely used in applications such as personal electronics, industrial, medical, fitness and much more. There were already more than 500 million NFC-enabled devices in 2015 [1], and this number has only increased since then.

The RF430CL330H Dynamic NFC Interface Transponder chip uses this technology to communicate over radio frequency, as well to having an I^2C interface. Allowing the possibility for adding a diagnostic interface to configure and retrieve data from a host system. This report explains the procedure to design a PCB containing the RF430CL330H and evaluates the chip using an EVM (evaluation module) offered by Texas Instruments. The design is then integrated into a larger system.

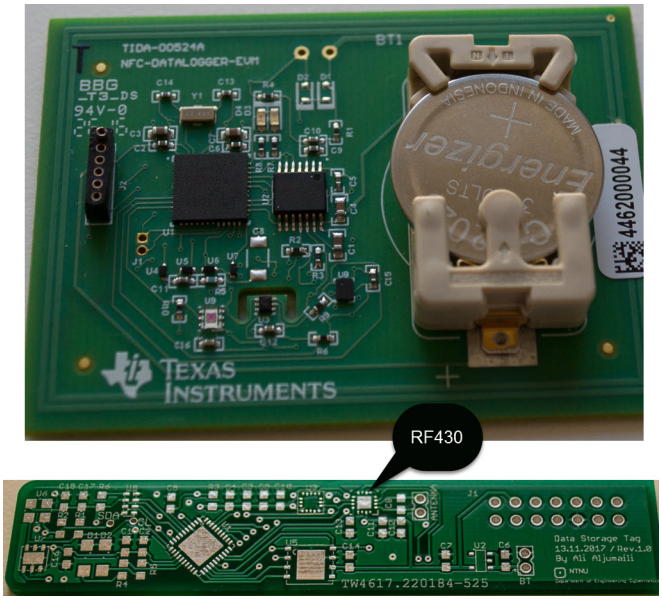

Figure 1: Evaluation kit and prototype

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Chapter 1

System description

1.1 Project description

The objective of this project is to integrate an NFC Transponder chip into a larger system. Designing a printed circuit board (PCB) containing an NFC chip and an external antenna.

1.2 System specifications

The system specifications are as follows. The NFC chip must have an I^2C interface for communication. Be Compatible with a 2.5 V power rating. Support ISO/IEC 14443 that defines transmission protocols for communicating with contactless integrated circuit cards. 13.56 MHz communication frequency. Support an external antenna. The cost should be kept to a minimum.

Having this as a start point, it was concluded that the RF430CL330H chip would be a good choice. A table of specification for this chip is shown in Table 1.1.

1.3 Block Diagram

The block diagram shows the communication between the NFC Transponder and the host system. Using the Nexus 5X phone as an NFC reader.

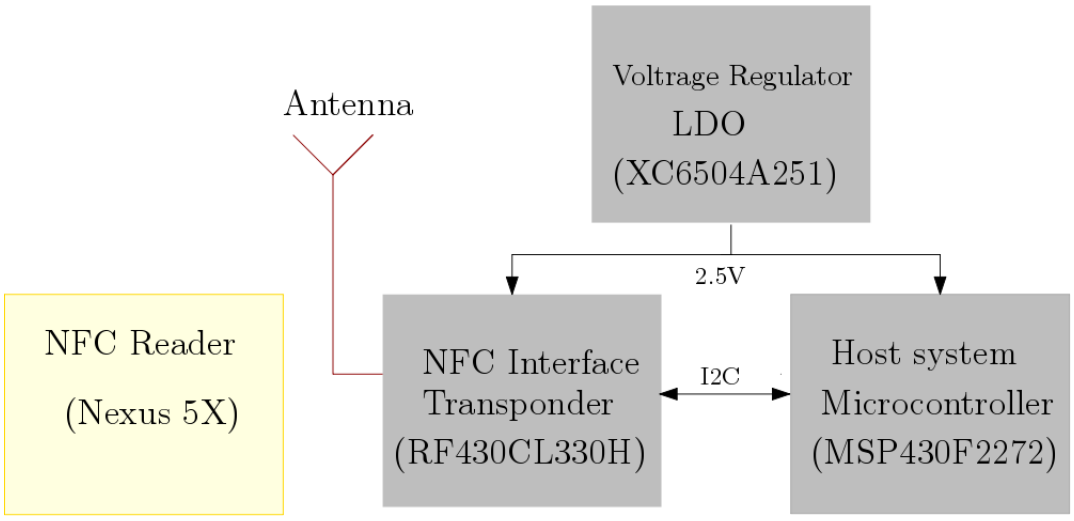

Figure 1.1: System's Block Diagram

1.4 Introduction to RF430CL330H

The RF430CL330H NFC Transponder chip offers read/write possibility in NDEF (NFC Data Exchange Format) which is a standard data format maintained by the NFC Forum. Table 1.1 shows the parameters of interest, taking the specifications in mind.

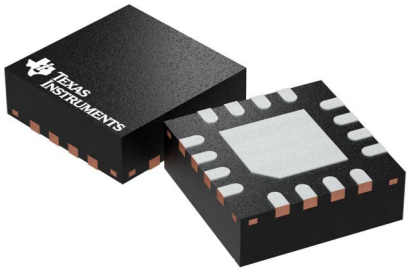

Figure 1.2: `VQFN package from [2]`

Parameter	Specification
Power supply range	2 V - 3.6 V
Communcation	SPI and I^2C
RF standard support	ISO/IEC 14443B and NFC Tag Type 4B
Radio Frequency	13.56 MHz
Antenna connection	Differential
Data rate	848 kbps
Package size	9 mm2: 3 x 3(VQFN)
Unit price	$1.53

Table 1.1: RF430CL330H specifications

Chapter 2

PCB design procedure

This chapter explains the workflow used to create the PCB prototype in Eagle and visualize it into a 3D model using Fusion 360. Three parts are necessary to create a PCB in eagle:

1. The schematics which is a diagram with electrical connections to the different components in the circuit.
2. The board shows the physical representation of the electrical connections between the different components
3. The library contains the components used to create both the schematics (diagrams) and board (footprint).

We start by creating a new project by adding a new folder under projects and add all of the 3 parts above. This is done by clicking on File → New → then choosing the three options above.

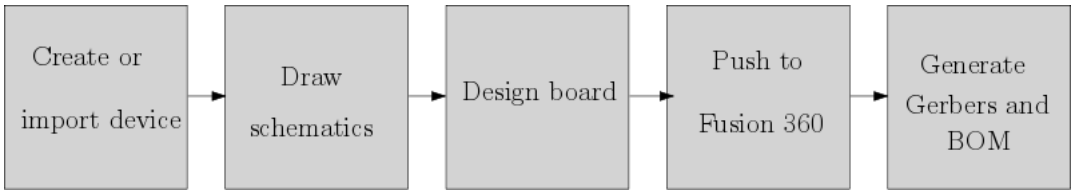

Figure 2.1: Design workflow in Eagle

2.1 EAGLE's schematics

In order to draw the schematics, the right components must be found or created. Standard components like capacitors, resistors, voltage sources and ground can be found in standard libraries and can easily be imported to a library or used in the schematics. The full board schematics is shown in Appendix A.3.

2.1.1 Creating a component in Eagle

Eagle's component logic is **Symbol + Package = Device.** These three parts are described and created for the RF430CL330H chip.

1. The symbol will be shown on the schematics.
2. The package contain the footprint of the component and will be shown in the board.
3. The device combines both the symbol and package into one component.

2.1.2 Creating the Symbol

The datasheet for the RF430CL330H [2] is used to create a new symbol with correct pin numbers and description.

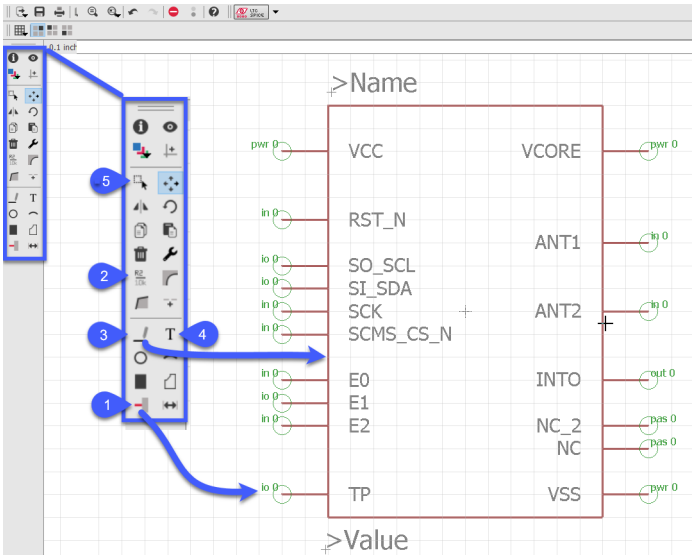

Figure 2.2: Creating a symbol in eagle

1. Add the pins, we can find this information in the datasheet. This chip has 15-pin.
2. Select the name tool to add a name to each pin.
3. Create an outline using the line tool, and move the components as shown in the Figure 2.2
4. Add text with >Name and >Value. This will be used later when creating the device.
5. Move the components to the desired positions as shown in step **(5)** and save.

2.1.3 Creating the Package

In the library editor choose library → table of contents. Then add a new package named **VQFN-16 (RGT)** and follow the steps shown in Figure 2.3.

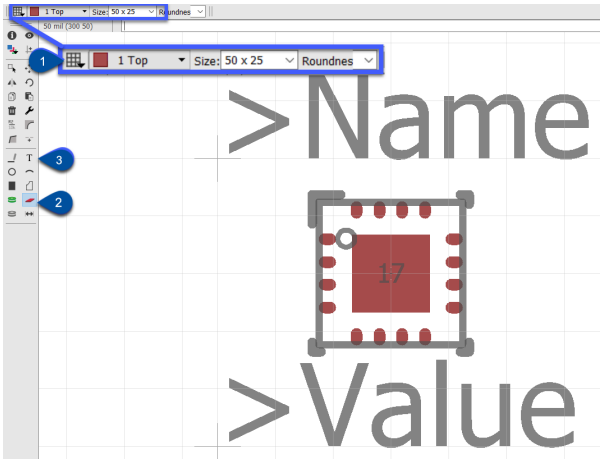

Figure 2.3: Creating a package in Eagle

1. It's important to choose the right grid size, the correct spacing is given in the datasheet [2].
2. Choose the SMD tool and add 17 pads to the top layer.
3. Add text >Name and >Value to layers **tNames** and **tValues** respectively. The outline is done using the line tool to the **tDoc** laye. Save the new footprint.

2.1.4 Creating the Device

In order to create the device we go to the library → table of content, then click add device.

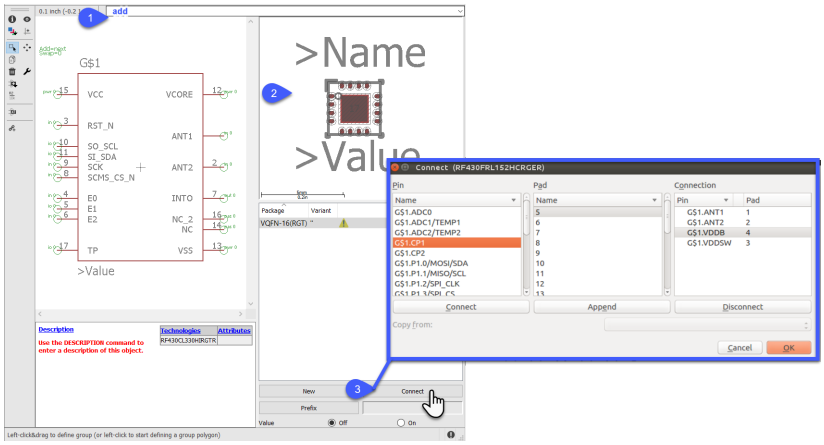

Figure 2.4: Creating a device in Eagle

1. Type **add** and place the symbol.
2. Type **add** and place the package.
3. Select the package and connect all of the created pins to the corresponding pad. Save the library.

2.1.5 Add an existing device to a managed library

A library with all necessary component is created. A managed library creates a connection between Eagle and Fusion 360 and is used to create a3D model of the board. The creation of such a library is done as shown in Figure 2.6.

The MSP430F2274 chip symbol and footprint were downloaded using Webench [**TexasInstruments**] and imported into Eagle as shown in Figure 2.5.

2.2 Creating the board outline

A 2 layer board is developed with the following considerations:

- 1 oz copper stackup to keep the price to a minimum.
- Trace width depends heavily on the current, traces carrying high amount of currents should have larger trace width.
- No right angles in traces, this is to avoid any logical faults in signals where most signals are dependent on edges.
- Decoupling capacitors placed as closed to the power pins as possible.

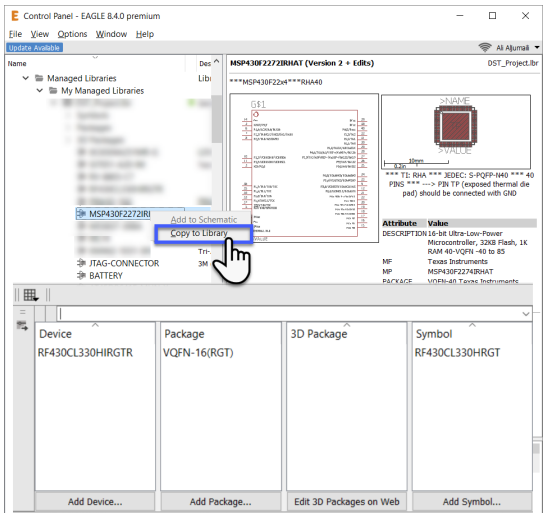

Figure 2.5: Adding an existing component to a library

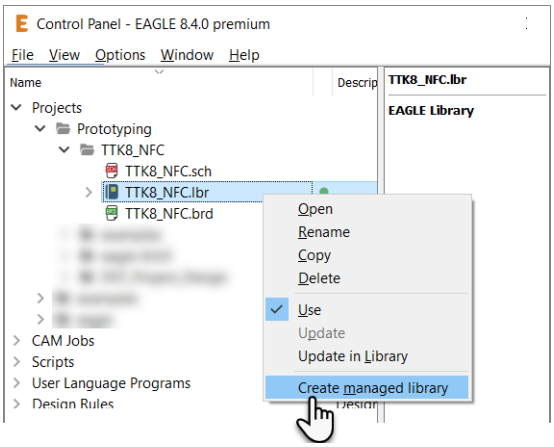

Figure 2.6: Creating a manged library library

- Design check rules to check for air wires and margin faults.
- No autorouter. This is mainly because the autorouter is terrible, as well to avoid any ”antenna” looking routes.

Figure 2.7 and shows the final board outline as well to an explanation to what the different layers are.

2.3 Board 3D model

The managed library can be found by right clicking on the library and choosing view on web. The 3D model is called ”Package” in Fusion 360. One must click Edit then choose upload .step to upload the 3D model for the packages. This is done to all of the missing packages as shown in Figure 2.9.

2.3.1 Generating the 3D model

The 3D model is generated after updating all of the packages with a .step (3D) package and pushing the board outline from Eagle to Fusion 360 as shown in Figure 2.10.

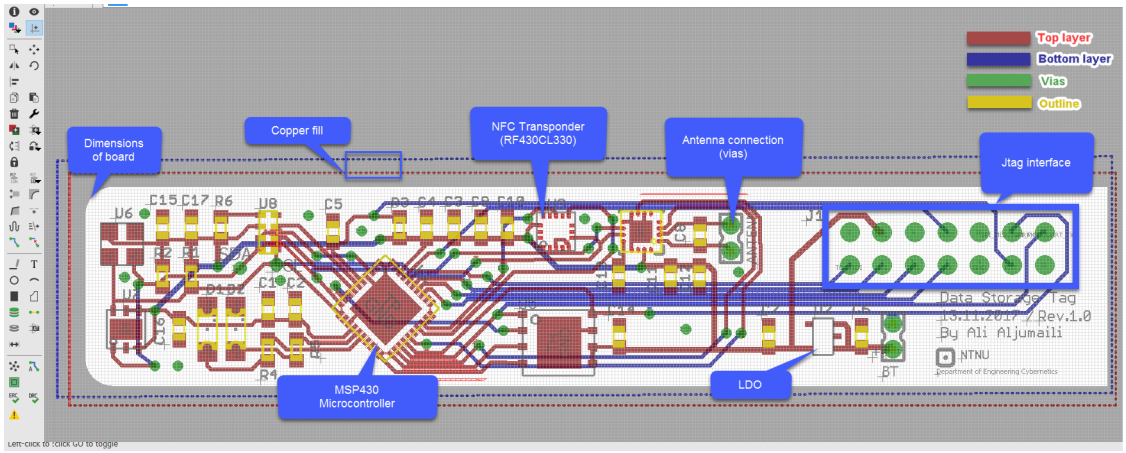

Figure 2.7: Board layout explained

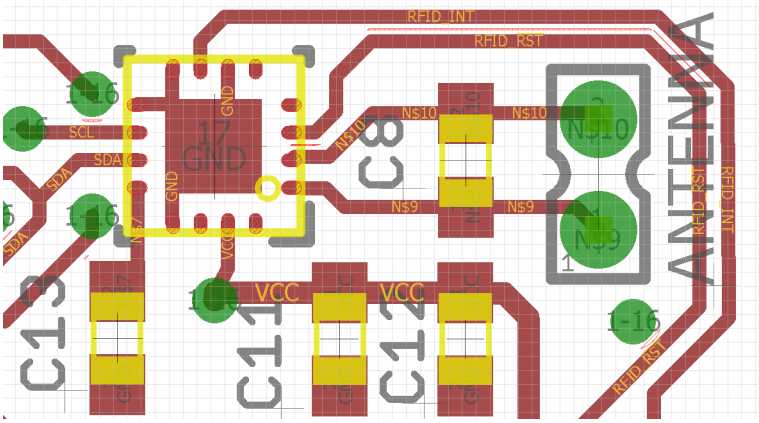

Figure 2.8: Top board layout for NFC chip

2.4 Eagle Design directory explained

All of the design files will be found under: **[Installation-folder]/Eagle-design**

File name	Description
TTK8-NFC.lbr	Contains an Eagle library with the created components
NFC-Schematics.sch	Contains the schematics for the project
DST-project.brd	Contains the board layout, this is used to generate the gerber files
DST-project.sch	Contains symbols for the corresponding board layout

Table 2.1: Project design files and description

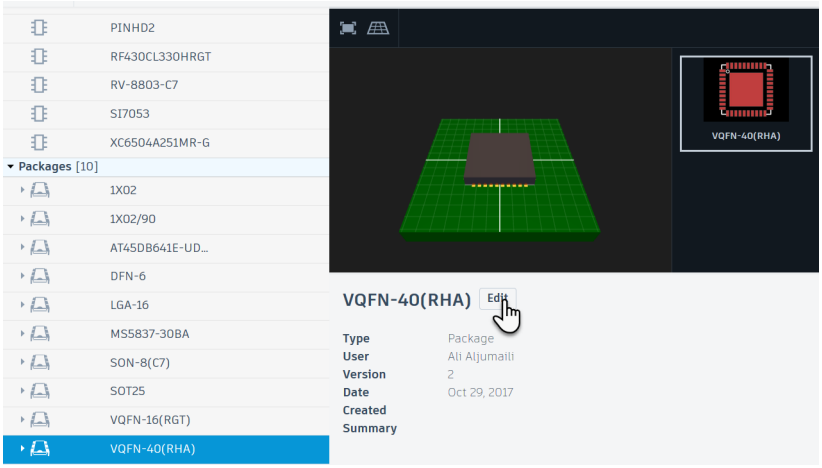

Figure 2.9: Adding missing packages

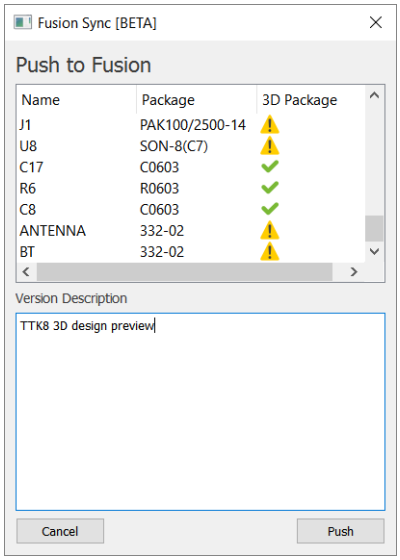

Figure 2.10: Pushing 3D model to Fusion 360

Chapter 3

Preparing the PCB for manufacturing

This chapter explains how to export the gerber files, which are needed by the manufacturer to produce the PCB. As well as creating a BOM (bill of material) to order all of the needed components.

3.1 Exporting Gerber files

To export the gerber files the Make function in Eagle is used to create a .zip file with the gerbers. The files can be found under **[Installation-folder]/Gerbers** directory and selected layers can be seen in Appendix A.5.

File name	Description
brd.boardoutline.ger	Helps the manfacturer (Elprint) automatically detect the board outline/dimensions
brd.bottomlayer.ger	The copper bottom layer tells the manufacturer where to lays copper on the bottom.
brd.bottomsoldermask.ger	Bottom solder mask is a thin layer that protects against oxidations and helps preventing solder bridges between solder pads.
brd.drills.xln	The drill file contains drilling details for production of the PCB.
brd.toplayer.ger	Contains the top copper layer.
brd.topsilkscreen.ger	contains text and outline for the components drawn
brd.topsoldermask.ger	This covers all vias and component traces to protect from corrosion and accidental electrical shorts

Table 3.1: Gerber files and description

3.2 Bil of Materials section

A bill of material (BOM) can be found in Appendix B

Chapter 4

Testing and Conclusion

This chapter shows the results from testing the NFC evaluation module [3] in addition to a small conclusion with future improvements to the produced PCB.

4.1 Testing TI datalogger

The evaluation kit from Texas Instruments was used to test the NFC transponder chip capabilities in the following areas:

1. Operating modes.
2. Memory
3. Data transfer

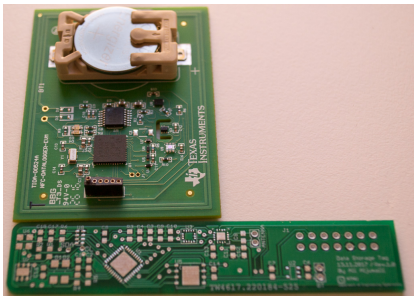

Figure 4.1: Evaluation kit and prototype

4.1.1 Operating mode

The evaluation kit demonstrated successful behaviour when both reading and writing to the chip. The NFC Transponder chip showed that it supports ISO1443B, being able to both read and write to it using an android application and an Nexus 5X NFC enabled smartphone.

4.1.2 Memory

The 64 KB onboard FRAM memory was capable of storing 1853 samples of time and temperature. It was tested by placing the EVM inside of a refrigerator and letting it log overnight in the cold. The memory was successfully full and all data was retrieved in the morning. Figure 4.2 shows the application used to read and write to the chip.

4.1.3 Data transfer

It took around 12 seconds to read the whole 64KB memory. Giving a read rate of around 5.3 KBps. This is consistent with typical data throughput of 3.2 - 5.8 KBps mentioned in the datasheet.

Reading speed was also reasonable. The chip responded within 1-3 seconds to the written commands.

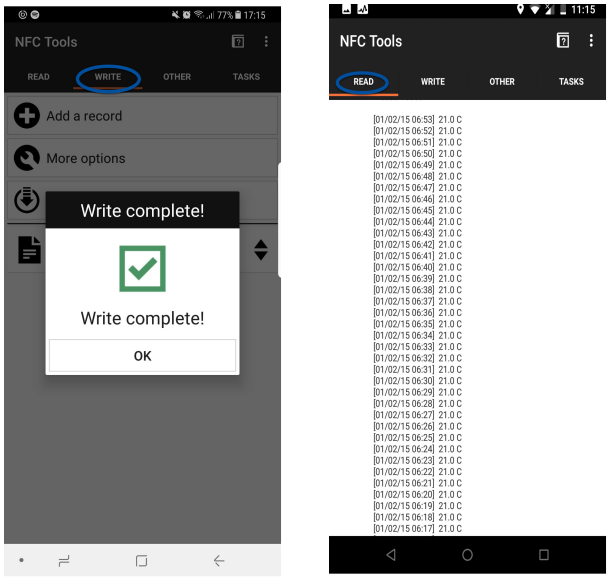

Figure 4.2: Writing to the NFC Transponder using NFC tools

4.2 Testing the PCB

The PCB was tested virtually by using eagle's DRC (design rules check) to detect any air wires, crossing clearances or other showstopper mistakes. These DRC were set to match the manufacturer's capabilities and are included in the delivered board file. An online simulator from 4pcb.com was also used to check for any showstoppers.

Testing the PCB physically was done using a multimeter, checking the copper paths for any short circuits. Multiple test points were added when designing the board to make it easy to test VCC, I^2C and ground lines. A zoom camera was also used for virtual inspection of the board.

4.3 Conclusion

After testing the NFC development kit it is shown that the RF430 NFC transponder was a good choice with reliable behaviour and low energy consumption, it was easily integrated to the I^2C bus on the prototype. The PCB board was challenging because the size of the PCB, it would have been easier to use a 4 layers board with dedicated VCC and ground planes. The copper fill on the board were lacking on the edges, this should be improved in future revisions of the board.

This project provided a good introduction to PCB design as well a good purpose for NFC technology. That can act as a debugging and configuration interface inside of a small devices that are sealed from the outside world, like an underwater data storage tag (DST).

Appendix A

Board layout and 3D model

A.1 Fusion 360 3D model

A.2 Full schematics

A.3 Board layers

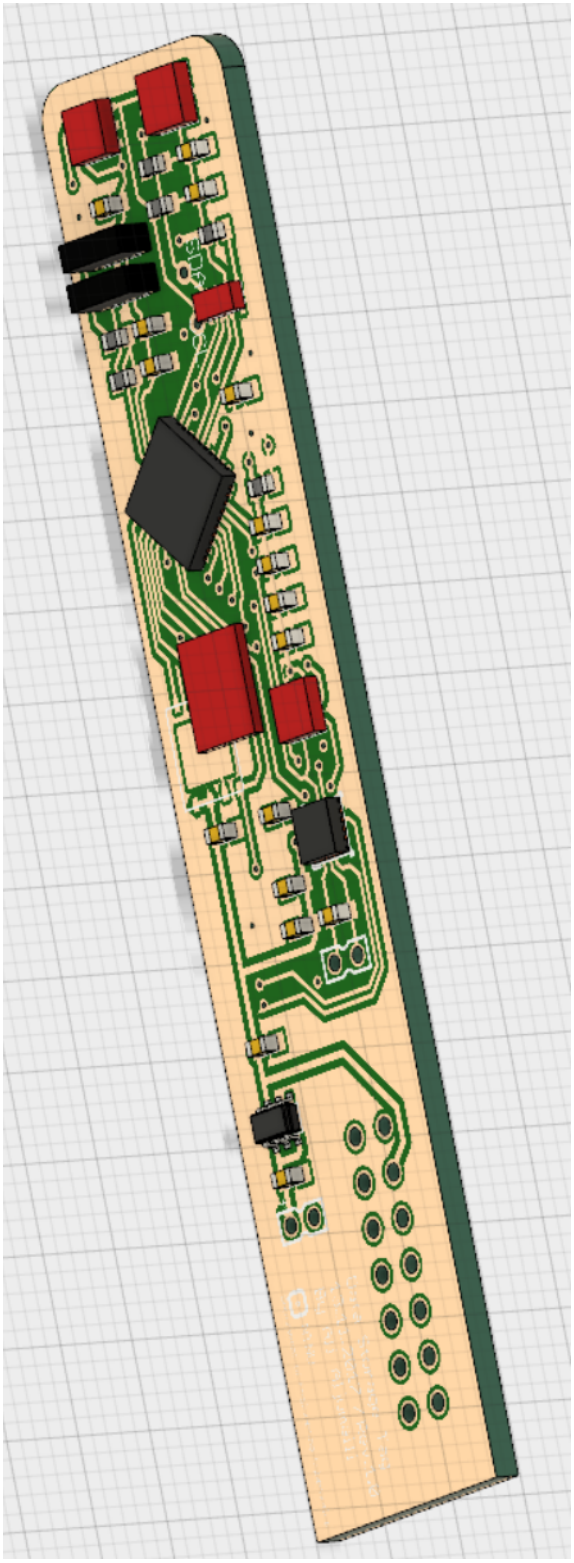

Figure A.1: Board 3D model

A.4 Produced PCB

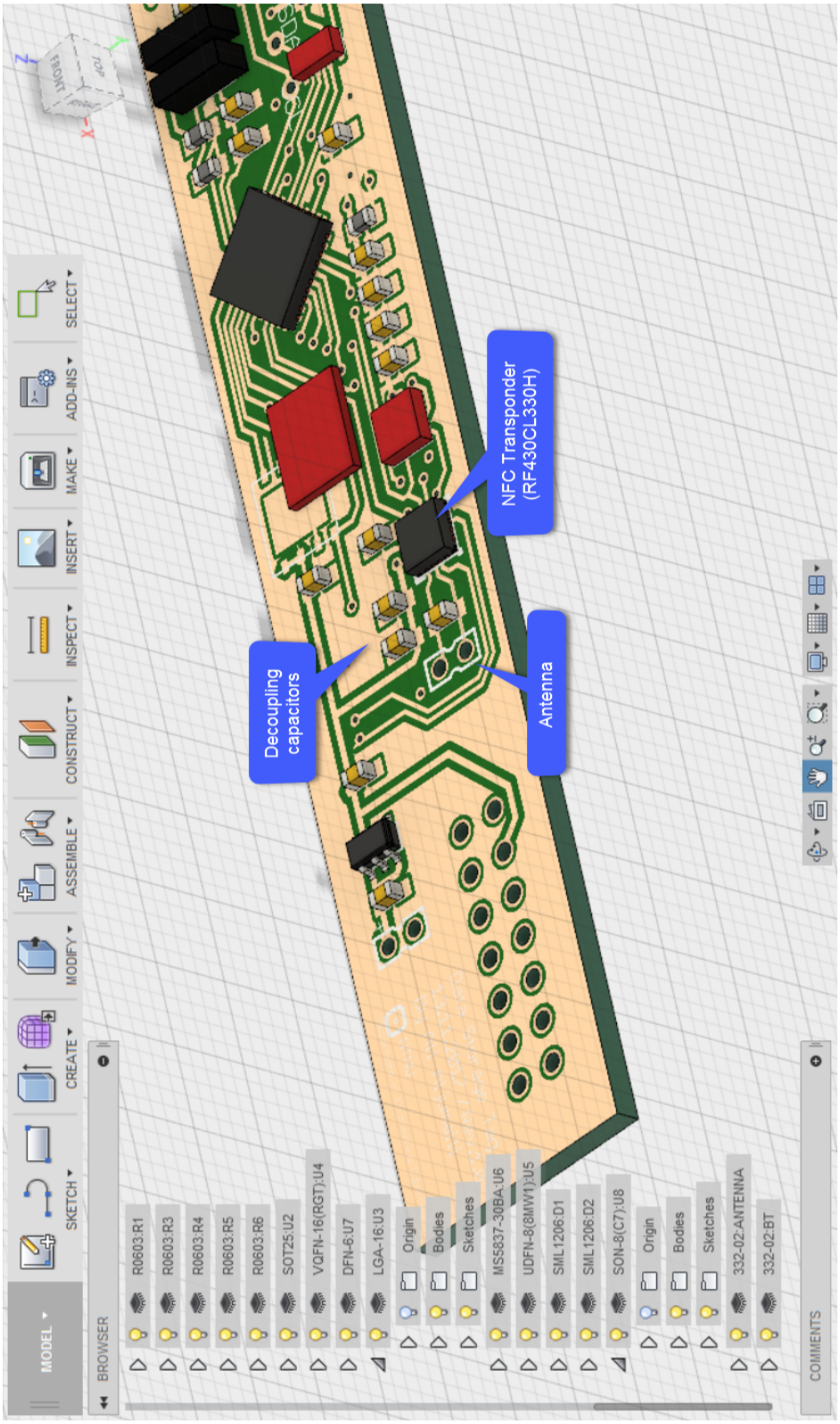

Figure A.2: Board 3D model explained

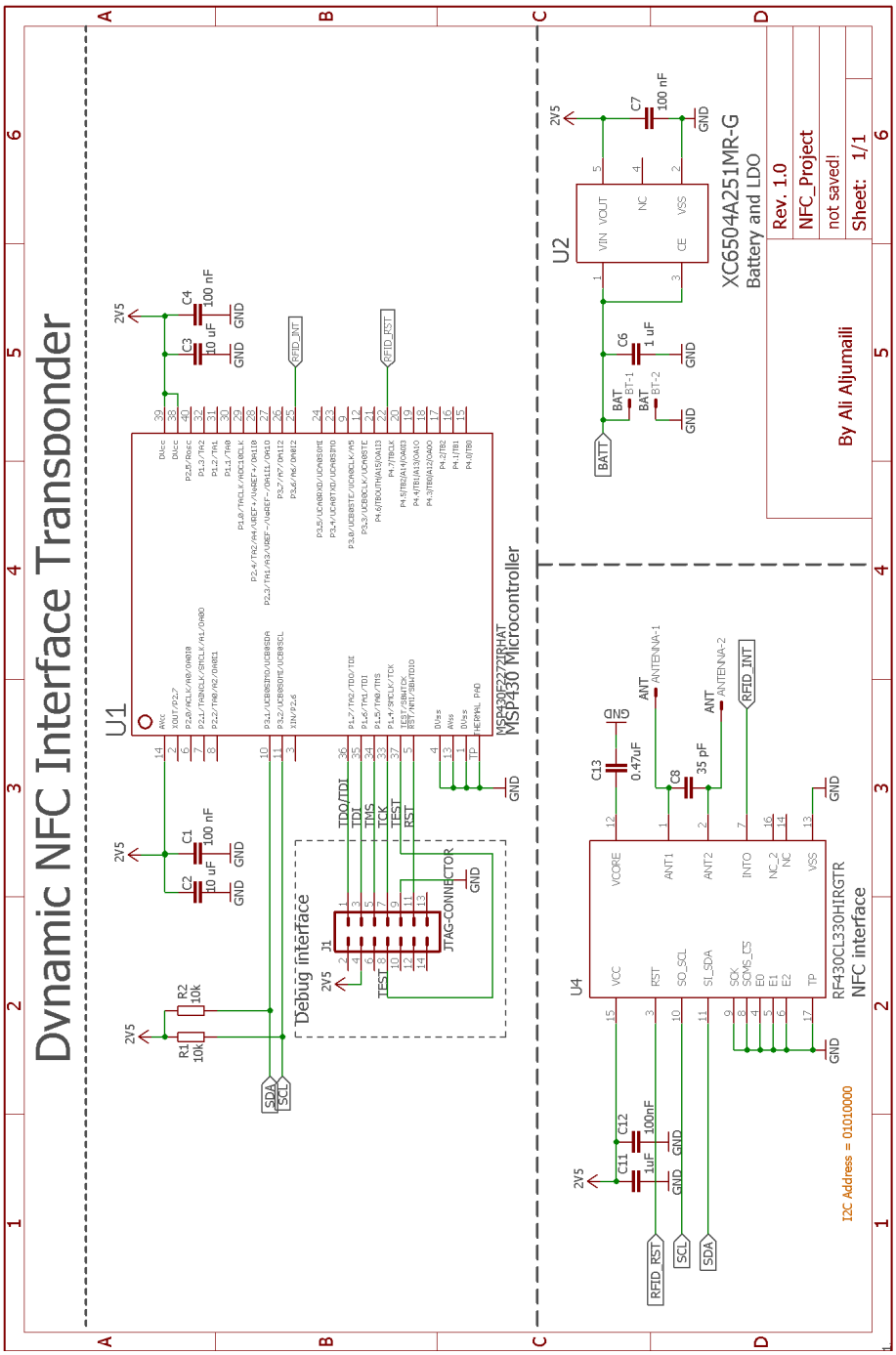

Figure A.3: Full project schematics

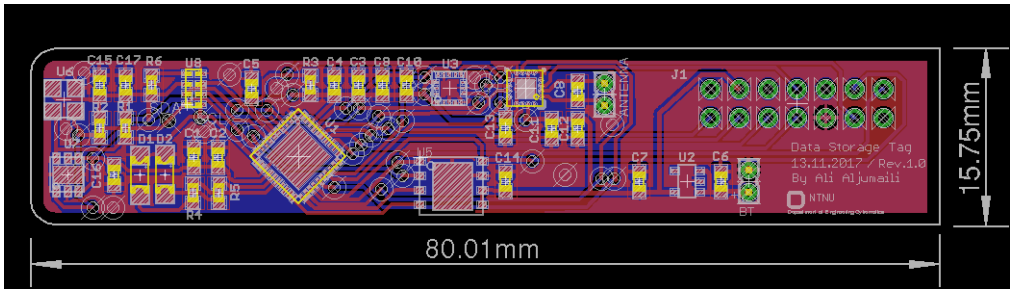

Figure A.4: Board layout

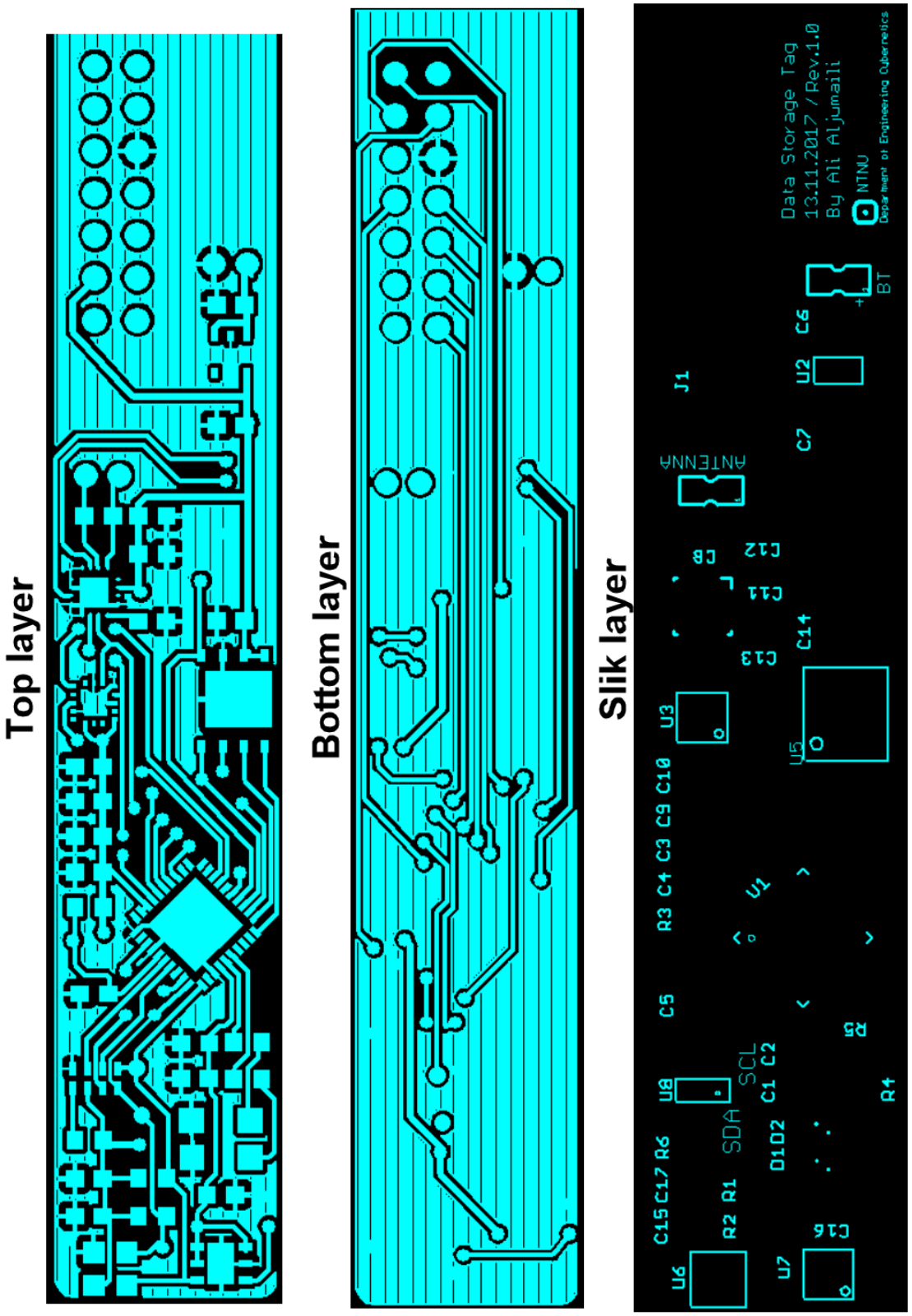

Figure A.5: Board layouts

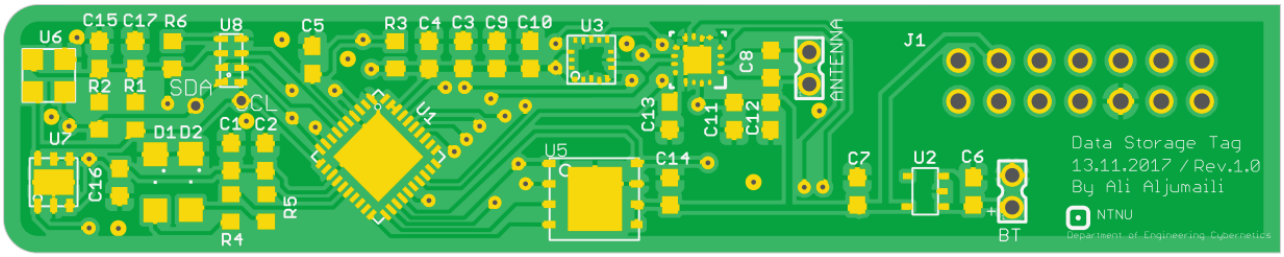

Figure A.6: Eagle's Board Layout

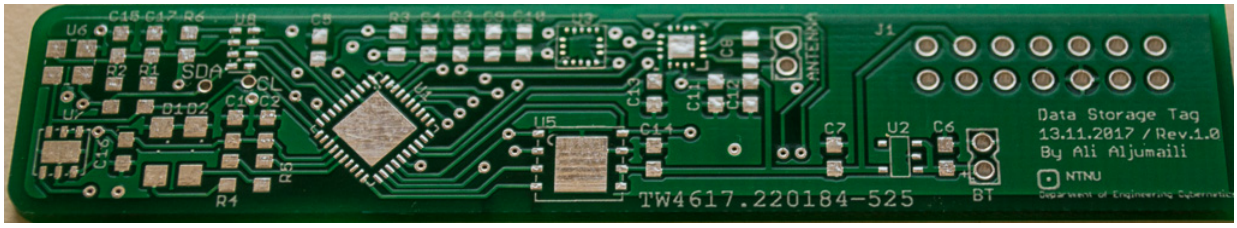

Figure A.7: PCB front

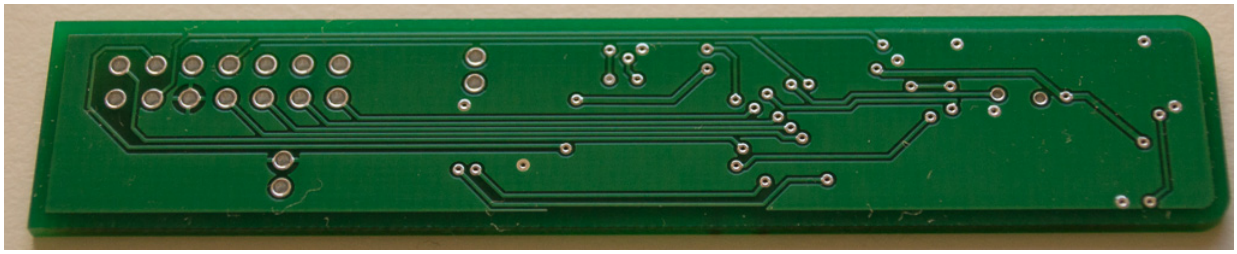

Figure A.8: PCB back

Appendix B

Bill of Materials

Item	Qty	Designator	Value and Description	Manufacturer	Part Number	Supplier
1	10	C1,C4,C7,C9,C10, C12,C14,C15,C16,C17	0.1uF SMD Ceramic Capacitor	KEMET	C0603C104K5RECTU	Mouser
2	2	C2,C3	10 uF SMD Ceramic Capacitor	KEMET	C0603C106M9PACTU	Mouser
3	2	C6, C11	1 uF SMD Ceramic Capacitor	KEMET	C0603C105K8PACTU	Mouser
4	1	C8	35 pF SMD Ceramic Capacitor	KEMET	C0603C360J5GACTU	Mouser
5	1	C13	0.47 uF SMD Ceramic Capacit	TDK	CGA3E3X7R1H474K080AE	Mouser
6	1	C5	10 nF SMD Ceramic Capacit	KEMET	C0603C103J5REC7411	Mouser
7	1	D1	Red SMD LED	Broadcom	HSMC-C191-T0000	Mouser
8	1	D2	Green SMD LED	Lumex	SML-LX1206GC-TR1	Mouser
9	1	J1	14P header	3m	N2514-6002RB	Mouser
10	3	R1,R2,R6	10k SMD resistor	Bourns	CR0603-FX-1002GLF	Mouser
11	2	R4,R5	470	Bourns	CR0603-FX-5100ELF	Mouser
12	1	R3	47k	Bourns	CR0603-JW-473GLF	Mouser
13	1	U1	16-bit MCU Ultra-Lo-pwr	Texas Instruments	MSP430F2274IRHAT	Mouser
14	1	U2	LDO Voltage Regulator, SOT-25-5 package	Torex Semiconductor	XC6504A251MR-G	Mouser
15	1	U3	Real Time Clock	Micro Crystal	RV-8803-C7-32.768kHz-3PPM-TA-QC	Mouser
16	1	U4	Accelerometers 16 bit LGA 6 degree Tri-axis Digtl Mgnt	Kionix	KMX62-1031-SR	Mouser
17	1	U5	DynamicNFC Interface Transponder	Texas Instruments	RF430CL330HIRGTR	Mouser
18	1	U6	Flash Memory 64Mb, SPI, UDFN-8	Adesto Technologies	AT45DB641E-MHN-Y	Mouser
19	1	U7	Pressure Sensor	Measurement Specialties	MS583730BA01-50	Mouser
20	1	U8	Digital Temp Sensor High Accuracy, I2C, DFN-6	Silicon Labs	SI7051-A20-IM	Mouser
21	1	Antenna	Flexible NFC antenna (13.56 MHz)	Tacoglas	FXR.06.A	Mouser
22	1	Antenna	Flexible NFC antenna (13.56 MHz)	Tacoglas	FXR.07.A	Mouser

Appendix C

Project work breakdown

C.1 Work breakdown structure

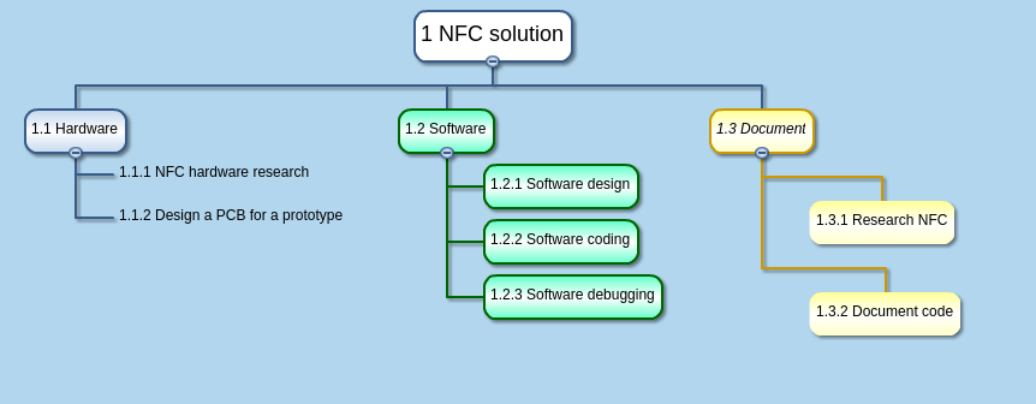

Figure C.1: WBS for project

C.2 Progress plan

WEEK	COMMENT	DEADLINE
40	Start documentation of report	8.10.2017
41	NFC hardware Research	15.10.2017
42	NFC antenna research and test of debugger kit	22.10.2017
43	Start PCB design	
44	Finish up PCB design, order should be placed	1.11.2017
45	Away, waiting for PCB	
46	Install components and test the PCB	19.11.2017
47	Documentation	
48	Deadline for delivery	23.11.2017

Figure C.2: Progress plan