SYSC 4001 Operating Systems Fall 2025

Assignment 1

SYSC4001 L3 – Group 3

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https://github.com/aliooo36/SYSC4001_A1

Analysis of Simulation Test Cases:

This report analyzes 22 interrupt simulation test cases examining various aspects in processing performance. The tests reveal insight into context switching overhead, ISR timing, CPU scaling effects, and workload characteristics that influence overall system performance.

1. Context Switching Tests (3 tests)

Purpose: Analyze impact of context save/restore time variations

- test_context_10ms.txt (Baseline)
  This test establishes the baseline performance for efficient context switching with a total overhead of 13ms, demonstrating optimal interrupt handling. This result indicates that the 10ms save/restore context time represents a well-made, standard operating system configuration.

- test_context_20ms.txt
  Switching the context time variable to 20ms, we can see a 77% increase in interrupt overhead, totalling 23ms. This confirms the linear relationship between context switching time and interrupt latency. This shows that an increase in switching time directly contributes increased system latency, potentially affecting real-time responsiveness and throughput.

- test_context_30ms.txt
  This case revealed a substantial 154% increase in interrupt overhead, reaching 33ms, this result further confirms our findings in the previous tests, and underscores context switching optimization as high priority for performance tuning.

Overall Analysis: Context switching time has linear impact on interrupt overhead. Each 10ms increase in context time adds exactly 10ms to total interrupt latency.

2. ISR Timing Tests (4 tests)

Purpose: Analyze impact of ISR execution time variations

- test_isr_40ms.txt (Baseline)
  Establishes baseline for standard ISR execution with predictable 40ms processing time as stated in the assignment.

- test_isr_80ms.txt
  This test shows that doubling the ISR execution time directly affects SYSCALL duration while END_IO remains device dependent.

- test_isr_120ms.txt
  The simulation test indicates that tripling the ISR execution time creates noticeable system call delays, for establishing the correlation between ISR complexity and system responsiveness.

- test_isr_200ms.txt
  This test reveals that extremely long ISR execution times create substantial delays in system service availability. The extreme case highlights the importance of implementing interrupt prioritization mechanisms.

Overall Analysis: ISR execution time directly impacts system call performance but doesn't affect hardware interrupt timing (END_IO uses device delays).

3. CPU Speed Tests (3 tests)

Purpose: Analyze CPU speed scaling effects

- test_cpu_normal.txt
  This test provides the baseline metrics (100ms) for CPU-bound task completion times under standard operating conditions.

- test_cpu_fast.txt
  This simulation demonstrates a 50% reduction in CPU execution time when processor speed doubles, while I/O and interrupt overhead remain unchanged Amdahl's law. The result clearly shows how I/O bound operations limit the maximum speedup in a computing system.

- test_cpu_slow.txt
  This specific simulation reveals that quarter-speed processor operation results in four times longer the CPU execution, being 400ms. This demonstrates the CPU-bound limitation scenario where I/O and interrupt overhead become negligible by comparison.

Overall Analysis: CPU speed scaling affects only CPU activities. I/O and interrupt overhead remain constant, demonstrating Amdahl's Law - speedup limited by non-CPU components.

4. **Address Size Tests (2 tests)**

Purpose: Analyze vector table addressing differences

- test_addr_2bytes.txt
  This simulation confirms that compact 2-byte vector addressing provides optimal memory usage for table vector storage without impacting execution timing performance.

- test_addr_4bytes.txt
  This test demonstrates that an expanded 4-byte addressing doubles memory usage for vector tables but still maintains execution timing when compared to the 2-byte system.

Overall Analysis: Vector size affects memory layout but not execution timing. 4-byte addresses use 2x more memory but provide larger address space for ISRs.

5. Workload Pattern Tests (3 tests)

Purpose: Analyze different workload characteristics

- test_workload_cpu.txt
  This simulation demonstrates CPU-bound workloads that maintain minimal interrupt overhead (approx. 10%), resulting in maximized CPU utilization with minimal kernel transitions.

- test_workload_io_balanced.txt
  The test represents an ideal general-purpose scenario with equal CPU and I/O distribution, showing well-balanced resource utilization across components.

- test_workload_io_intensive.txt
  This simulation reveals I/O-bound workloads experiencing high interrupt overhead of 80% due to frequent I/O operations. This results in kernel mode dominance with continuous context switching.

Overall Analysis: Different workload patterns show varying interrupt overhead percentages. I/O-intensive workloads spend more time in kernel mode handling interrupts.

6. **Device Performance Tests (6+ tests)**

Purpose: Analyze device timing impacts and edge cases

- test_edge_fast_devices.txt

The simulation demonstrates how strategic device selection with fast I/O can minimize I/O wait times, significantly reducing overall execution time, as we can see in the times listed below:
Devices: 1 (100ms), 15 (68ms), 7 (152ms)

- test_mixed_device_speeds.txt
  This test examines device environments where varying performance characteristics create execution bottlenecks, particularly with slow peripheral devices.

- test_burst_io.txt
  This simulation analyzes concentrated I/O activity patterns that generate temporary high interrupt loads. This tests system capability to handle peak demand. High interrupt frequency can be seen during the I/O bursts.

- test_variable_bursts.txt
  The simulation evaluates system behaviour under dynamic workloads with unpredictable I/O patterns. The testing validated the adaptive capabilities of interrupt handling mechanisms.

- test_long_running.txt
  This test validates system stability and consistent interrupt handling over extended operational periods.

- test_edge_highfreq.txt & test_edge_slow_devices.txt
  These two simulations examine the extreme operating conditions that validate the strong capabilities of the interrupt handling system under stress.

The simulations show that system performance depends on context switching, ISR timing, CPU speed, and workload type. Context and ISR times linearly increase latency, CPU speed mainly affects CPU-bound tasks, and I/O-bound workloads cause high interrupt overhead. Address size affects memory use but not timing.