Application Note

Power Solutions for Xilinx Artix-7 and Zynq-7000

AN-PM-106

Abstract

This application note provides information on powering the Xilinx Artix-7 and Zynq-7000 family of devices.

Contents

Figures

Tables

1 Terms and Definitions

GUI	Graphical User Interface
PMIC	Power Management Integrated Circuit
DA906x	Dialog DA9061, DA9062, DA9063, and DA9063L
DVC	Dynamic Voltage Control
DVS	Dynamic Voltage Scaling, Analogous to DVC
MPSoC	Multiprocessor System-on-Chip
OTP	One-Time Programmable (Memory)
RTC	Real-Time Clock
SoC	System-on-Chip
PL	Programmable Logic
PS	Processor System

2 References

[1] Xilinx Power Estimator (XPE), http://www.xilinx.com/products/technology/power/xpe.html (Accessed 21-May-2018)

[2] Philofsky, B., Seven Steps to an Accurate Worst-Case Power Analysis Using Xilinx Power Estimator (XPE), WP353, v1.0, Xilinx Inc., 2008.

[3] DA9061, Datasheet, Dialog Semiconductor, Dialog Website Link

[4] DA9062, Datasheet, Dialog Semiconductor, Dialog Website Link

[5] DA9063, Datasheet, Dialog Semiconductor, Dialog Website Link

[6] DA9063L, Datasheet, Dialog Semiconductor, Dialog Website Link

[7] AN-PM-080, In-Circuit Programming of DA9061/2/3, Dialog Semiconductor, 2016, Dialog Website Link

[8] UM-PM-008, SmartCanvas™ DA9061/2 User Manual, Dialog Semiconductor, Dialog Website Link

[9] UG583, UltraScale Architecture PCB Design User Guide (ver1.10)

[10] Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics, Xilinx, Link

[11] DA9062 Performance Board Schematic, Dialog Semiconductor, Dialog Website Link

3 Introduction

The Xilinx Artix-7 family of FPGA devices provide the highest performance-per-watt fabric, transceiver line rates, DSP processing, and AMS integration in a cost-optimized FPGA. The Xilinx Zync-7000 family of devices further extend this flexibility to include an Arm based processor sub-system alongside the programmable logic. To fully realize the performance of a Artix -7 or Zynq-7000 device requires an optimized power management solution. Dialog offers a range of power management solutions that will provide flexibility to match the requirements of most FPGA designs while maximizing performance and integration, and minimizing the PCB footprint.

4 The Artix-7

The following sections introduce the basic power rail requirements of the Artix-7 devices along with the capabilities of the Dialog DA9062 and DA9063L PMICs, and show why they can be the perfect partner to and Artix-7.

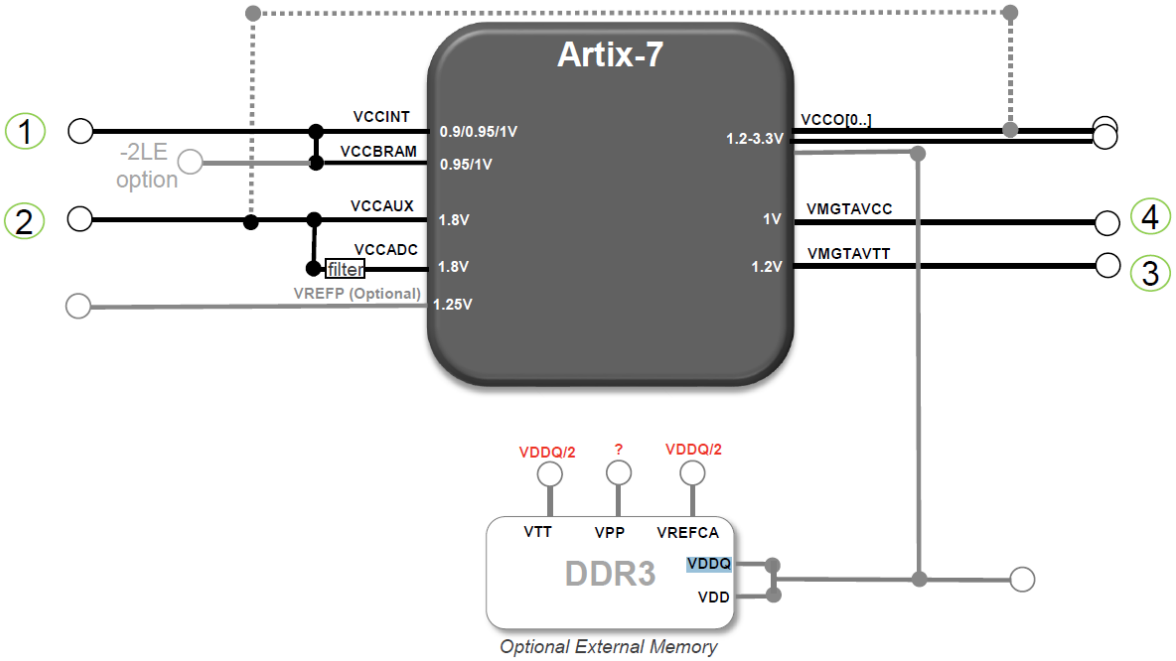

Figure 1: Artix-7 Power Rail Requirements

Table 1: Artix-7 Power Rail Requirements

Rail	Voltage	Load (A)
VCCINT	0.95 or 1 V ±5 %,0.9 V ±3 % (-2LE)	0.3 to 6
VCCBRAM	0.95 or 1 V ±5 %	0.1
VCCAUX and VCCADC	1.8 V ±5 %	0.15 to 0.35
VMGTAVCC	1.2 V ±3 %	0.15 to 1
VMGTAVTT	1 V ±2.5 %	0.05 to 0.4
VCC_IO	1.8 or 2.5 or 3.3 V ±5 %	0.2 to 2.5
VCC_DDR	1.5 or 1.35 V ±5 %	2
DDR_VTT	VCC_DDR/2	
DDR_VREF		

4.1 The Dialog DA9062

DA9062 flexible power management IC integrates four bucks and four LDOs capable of supplying individual rails of up to 2.5 A. This device ideally matches the requirements of the smaller members of the Artix-7 family of devices.

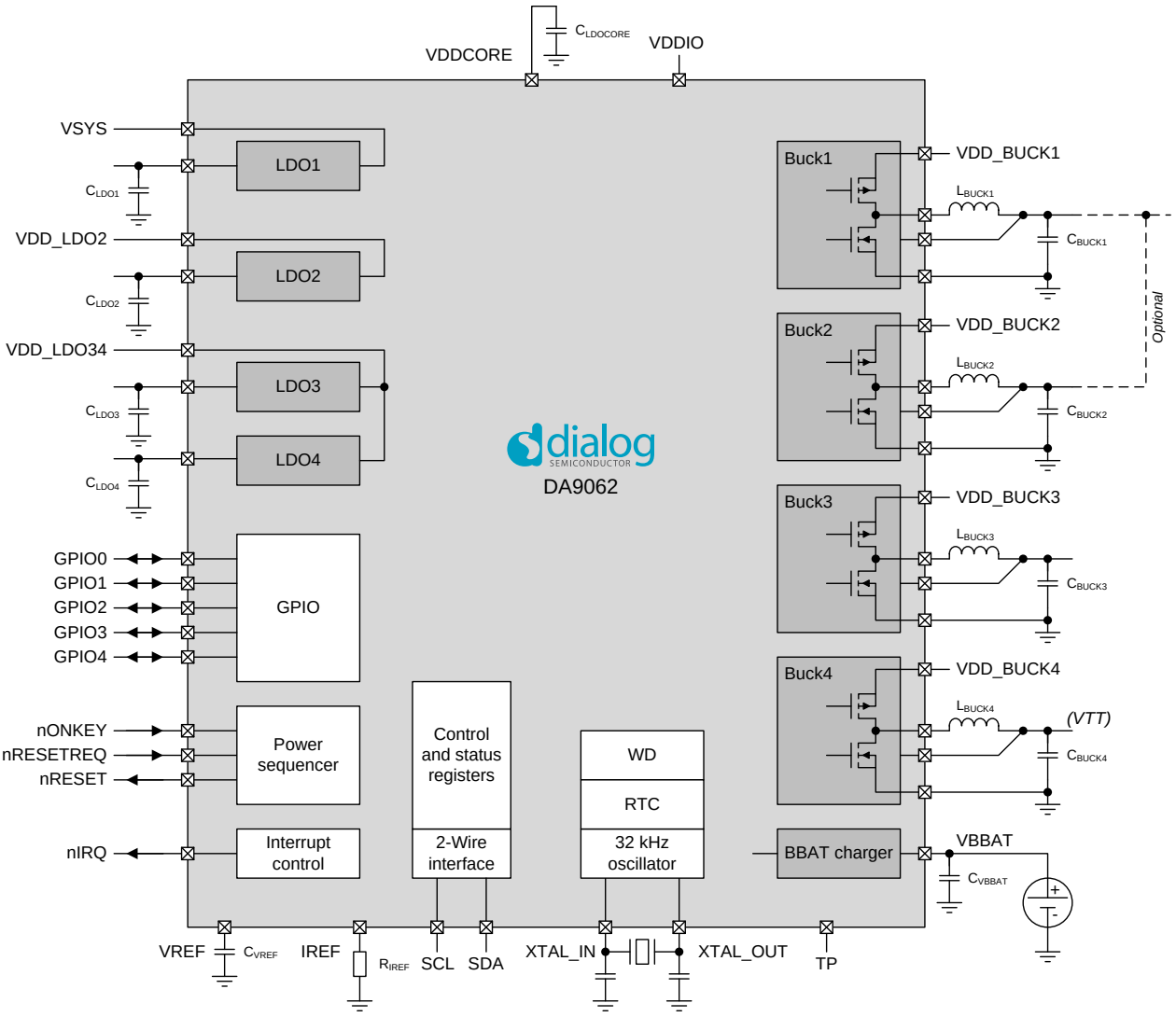

Figure 2: DA9062 Block Diagram

4.1.1 The DA9062 Regulators

Table 2: DA9062 Regulator Summary

Regulator	Supplied Voltage (V)	Supplied Max. Current (A)	External Component	Notes
Buck1	0.3 to 1.57	2.5	1.0 µH/2 x 47 µF	3 MHz, DVS with variable slew rate, 10 mV steps
Buck2	0.3 to 1.57	2.5	1.0 µH/2 x 47 µF	3 MHz, DVS with variable slew rate, 10 mV steps, can be combined with Buck1 as a 5 A dual-phase buck
Buck3	0.8 to 3.34	2.0	1.0 µH/2 x 22 µF or 2 x 47 µF	3 MHz, DVS with variable slew rate, 20 mV steps
Buck4	0.53 to 1.8	1.5	1.0 µH/2 x 22 µF or 2 x 47 µF	3 MHz, DVS with variable slew rate, 10 mV steps, can be used as a DDR VTT supply
LDO1	0.9 to 3.6	0.1	1.0 µF	Programmable in 50 mV steps, can be configured as an Always-on supply
LDO2	0.9 to 3.6	0.3	2.2 µF	Programmable in 50 mV steps
LDO3	0.9 to 3.6	0.3	2.2 µF	Programmable in 50 mV steps
LDO4	0.9 to 3.6	0.3	2.2 µF	Programmable in 50 mV steps

4.1.2 The DA9062 PCB Footprint

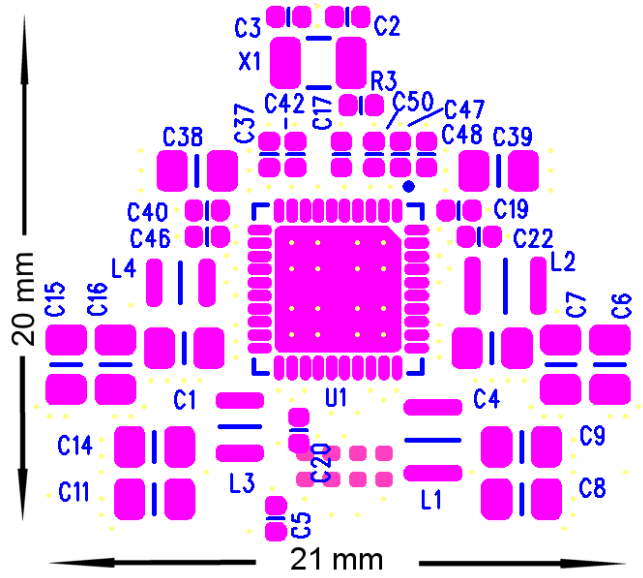

Figure 3: DA9062 Solution Footprint

The high level of integration along with the 3 MHz switching frequency results in a compact footprint. Figure 3 is an example footprint including all of the required passive components. The total area is less than 420 mm^2. This is achieved with all of the components on the top side of the PCB and without the use of over-aggressive placement. This area could be further reduced by placing some of the capacitors on the reverse of the PCB and by more aggressive spacing rules. As shown, there is significant unused space in the calculated area, possibly up to 25 %, see the DA9062 Performance board data pack for more details [11].

4.2 DA9063 and DA9063L Devices

DA9063 flexible PMIC integrates 6 bucks and 11 LDOs capable of supplying individual rails of up to 2.5 A. The DA9063 also includes an RTC. This device ideally matches many of the requirements the of the larger members of the Artix-7 family of devices.

The DA9063L is the lite version of the DA9063 which has a slightly reduce feature set. The DA9063L integrates 6 bucks and 5 LDOs.

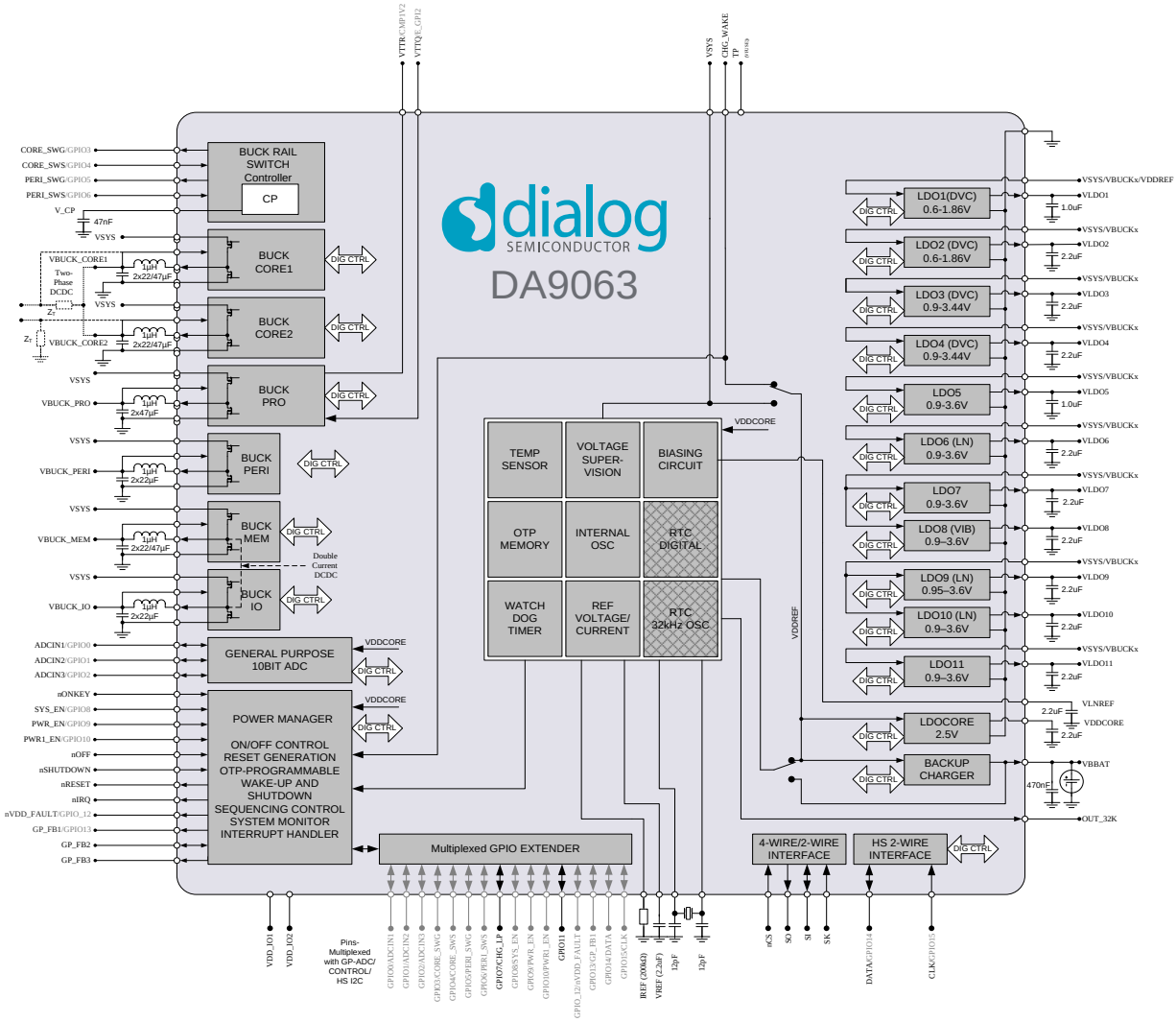

Figure 4: DA9063 Block Diagram

4.2.1 DA9063 Regulators

Table 3: DA9063 Regulator Summary

Regulator	Supplied Pins	Supplied Voltage (V)	Supplied Max Current (mA)	External Component	Notes
BUCKCORE1	VBUCKCORE1	0.3 to 1.57	1250/2500 (full-current mode)	1.0 µH/ 44 µF/ 88 µF	DVC 10 mV steps < 0.7 V PFM mode only 5 A dual-phase buck when combined with BUCKCORE2
BUCKCORE2	VBUCKCORE2	0.3 to 1.57	1250/2500 (full-current mode)	1.0 µH/ 44 µF/ 88 µF	DVC 10 mV steps < 0.7 V PFM mode only 5 A dual-phase buck when combined with BUCKCORE1
BUCKPRO	VBUCKPRO	0.53 to 1.80	1250/2500 (full-current mode)	1.0 µH/ 44 µF/ 88 µF	DVC 10 mV steps and VTT regulator mode < 0.7 V PFM mode only
BUCKMEM	VBUCKMEM	0.8 to 3.34	1500	1.0 µH/ 44 µF	DVC 20 mV steps 3 A (merge mode with BUCKIO)
BUCKIO	VBUCKIO	0.8 to 3.34	1500	1.0 µH/ 44 µF	DVC 20 mV steps 3 A (merge mode with BUCKMEM)
BUCKPERI	VBUCKPERI	0.8 to 3.34	1500	1.0 µH/ 44 µF	DVC 20 mV steps
LDO1	VLDO1	0.6 to 1.86	100	1.0 µF	DVC 20 mV steps Optional voltage tracking of BUCKCORE or BUCKPRO
LDO2	VLDO2	0.6 to 1.86	200	2.2 µF	DVC 20 mV steps
LDO3	VLDO3	0.9 to 3.44	200	2.2 µF	Bypass mode DVC 20 mV steps
LDO4	VLDO4	0.9 to 3.44	200	2.2 µF	Bypass mode DVC 20 mV steps
LDO5	VLDO5	0.9 to 3.6	100	1.0 µF	50 mV steps
LDO6	VLDO6	0.9 to 3.6	200	2.2 µF	50 mV steps, Low noise
LDO7	VLDO7	0.9 to 3.6	200	2.2 µF	Bypass mode 50 mV steps Common supply with LDO8
LDO8	VLDO8	0.9 to 3.6	200	2.2 µF	Bypass and switching

Regulator	Supplied Pins	Supplied Voltage (V)	Supplied Max Current (mA)	External Component	Notes
					vibration motor driver mode 50 mV steps Common supply with LDO7
LDO9	VLDO9	0.95 to 3.6	200	2.2 µF	Low noise 50 mV steps OTP trimmed Common supply with LDO10
LDO10	VLDO10	0.9 to 3.6	300	2.2 µF	Low noise LDO 50 mV steps Common supply with LDO9
LDO11	VLDO11	0.9 to 3.6	300	2.2 µF	Bypass mode 50 mV steps
BACKUP	VBBAT	1.1 to 3.1	6	470 nF	100 mV/200 mV steps Configurable charge current between 100 µA and 6000 µA Reverse current protection (RCP)
LDOCORE	Internal PMIC supply	2.5 ±2 % accuracy	4	2.2 µF	Internal LDO

4.3 Dialog Sub-PMIC Options

For individual high current rails that cannot be met by the integrated regulators of one of the system PMICs, Dialog has the DA921x family of Sub-PMICs. These can be enabled from the sequencer in the system PMIC see Table 4 for the currently available devices.

Table 4: Dialog Sub-PMIC Options

Device	Current (A)	Phase
DA9210	12	4
DA9211	12	4
DA9212	6 + 6	2, 2
DA9213	20	4
DA9214	15 + 5	3, 1
DA9215	10 +10	2, 2

4.4 Example Artix-7 Power Mapping

Comparing the Artix-7 power rail requirements from Table 1 with the DA9062 available regulators in Table 2, it is clear that the DA9062 is a good match for designs using the smaller members of the Artix-7 family. For the larger devices requiring VCCINT up to 5.5 A we can use a DA9063L. For the largest devices and for designs where extra margin is required we can pair up either a DA9063L or a DA9062 along with a Dialog sub-PMIC such as the DA9212 to meet the higher current requirements.

Sections 4.4.1, 4.4.2 and 4.4.3 provide example mapping for each of the above three scenarios.

4.4.1 Lower Power Artix-7 Designs

See Table 5 for mapping the Artix-7 on to the DA9062 rails.

Table 5: DA9062 Mapping

	Artix-7			DA9062	
		Voltage	Load (A)	Rail	Max (A)
1	VCCINT	0.9/0.95/1	0.3 to 6	Buck1	2.5
2	VCCBRAM	0.95/1	0.1	LDO1	0.1
3	VCCAUX	1.8	0.15 to 0.35	LDO2	0.3
3	VCCADC	1.8			
	VREFP	1.25			
4	VCCIO	1.2-3.3	0.2 to 2.5	Buck3	2
5	VMGTAVCC	1	0.15 to 1	LDO3	0.3
6	VMGTAVTT	1.2	0.05 to 0.4	LDO4	0.3
7	VDDQ	1.35 or 1.5	2	Buck2	2.5
8	VREFCA		0.01	VTTREF	0.01
9	VTT		1	Buck4	

4.4.2 Medium Power Artix-7 Mapping

Table 6: DA9063L Mapping

	Artix-7			DA9063L	
		Voltage	Load(A)	Rail	Max.(A)
1	VCCINT	0.9/0.95/1	0.3 to 6	VCORE1 and 2	5+
2	VCCBRAM	0.95/1	0.1	LDO9	0.1
3	VCCAUX	1.8	0.15 to 0.35	LDO11	0.3
3	VCCADC	1.8			
	VREFP	1.25			
4	VCCIO	1.2 - 3.3	0.2 to 2.5	PERI	1.5
5	VMGTAVCC	1	0.15 to 1	IO	1.5
6	VMGTAVTT	1.2	0.05 to 0.4	LDO7 and 8	0.4
7	VDDQ	1.35 or 1.5	2	MEM	1.5
8	VREFCA		0.01	VTTREF	0.01
9	VTT		1	VPRO	

4.4.3 High Power Artix-7 Mapping

Table 7: DA9063L + DA9211 Mapping

	Artix-7			DA9063L and DA9211	
		Voltage	Load (A)	Rail	Max (A)
1	VCCINT	0.9/0.95/1	0.3 to 6	DA9211	12
2	VCCBRAM	0.95/1	0.1	LDO7	0.1
3	VCCAUX	1.8	0.15 to 0.35	LDO11	0.3
3	VCCADC	1.8			
	VREFP	1.25			
4	VCCIO	1.2 to 3.3	0.2 to 2.5	MEM and IO	3
5	VMGTAVCC	1	0.15 to 1	PERI	1.5
6	VMGTAVTT	1.2	0.05 to 0.4	VCORE1	1.5
7	VDDQ	1.35 or 1.5	2	VCORE2	2.5
8	VREFCA		0.01	VTTREF	0.01
9	VTT		1	VPRO	

5 The Xilinx Zynq-7000 SoC Family

The Zynq-7000 family combines the power of an FPGA with the programmability of an ARM Cortex™-A9 processor.

The Smaller devices in the Zynq-7000 family, up to the Z-7020, integrate the equivalent of an Artix-7 device alongside either a single or dual core ARM processor system. As a result, the power requirements are similar between the Artix-7 and the Z-7000. It is recommended that designers refer to the Xilinx XPE,[1] to estimate the actual current requirements for any given design.

The Zynq-7000 design will have very similar current requirements to the similar sized Artix-7 device, with the addition of the current required for the processor system.

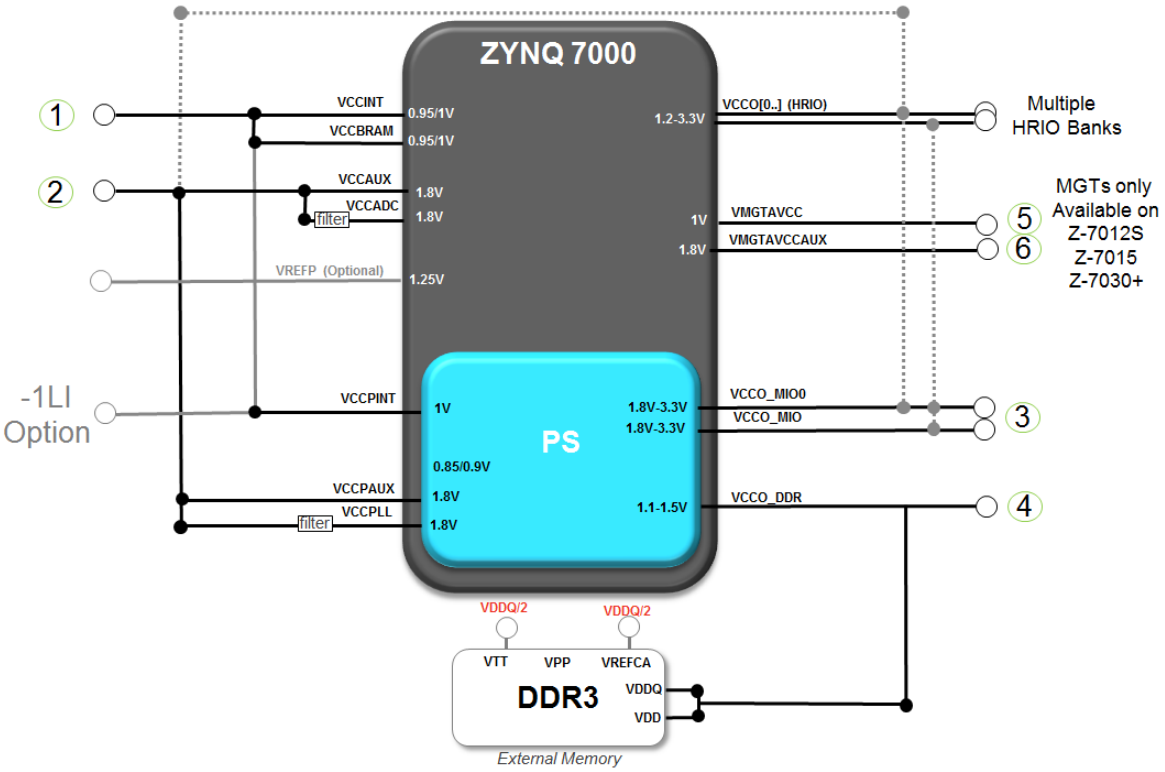

Figure 5: Xilinx Zynq-7000 Power Supply Consolidation

As shown in Figure 5, the addition of the processor sub-system requires four additional rails, VCCPINT, VCCPAUX and VCCPLL, VCCO_MIO, and VCCO_DDR in additional to the rails used by the programmable logic in the Artix-7 device. These rails can be consolidated with existing rails, see Table 8 for example requirements for these additional rails.

Table 8: Zynq-7000 Additional Rail Requirements

Rail	Voltage	Load
VCCPINT (Single Core)	1 V ±5 %	0.7 A
VCCPINT (Dual Core)		1 A
VCCPAUX and VCCPLL	1.8 V ±5 %	0.1 A
VCCO_MIO	1.8/2.5/3.3 V ±5 %	USER
VCCO_DDR	1.5/1.35 V ±5 %	USER

Table 9 provides a list of the supply rails for a Zynq-7000 device including those required for the PS and PL domains.

Table 9: Zynq 7000 Consolidated Supply Rails

	Rail	Voltage
	VIN	12 V
1	VCCINT	0.95/1 V ±5 %,0.9 V ±3 % (-2LE)
	VCCBRAM	
	VCCPINT	1 V ±5 %
2	VCCAUX	1.8 V ±5 %
	VCCADC	
	VCCPAUX	
	VCCPLL	
3	VCCO_MIO0	1.8/2.5/3.3 V ±5 %
	VCCO_MIO	
	VCCO	
4	VCCO_DDR	1.5/1.35 V ±5 %
5	VMGTAVCC	
6	VMGTAVCCAUX	
7	DDR_VTT	VCCO_DDR/2
8	DDR_VREF	VCCO_DDR/2

Table 10 provides an example Mapping for a Xilinx Zynq Z-7020. In the example the Zynq-7020 is mapped on to DA9062, which is able to supply all of the core rails and has two spare LDO that can be utilized elsewhere in the design.

Table 10 Example Z-7020 Mapping

	Rail	Voltage	Load	Comment	DA9062	
1	VCCPINT, VCCINT, VCCBRAM	1 V ± 5 %	2 A		Buck1	2.5 A
2	VCCPAUX, VCCPLL, VCCAUX, VCCADC	1 V ±5 %	0.5 A		LDO2 and 3	0.3 A x2
4	VCCO_DDR	1.5/1.35 V ±5 %	2 A	DDR3 or DDR3L	Buck2	2.5 A
7	DDR_VTT	VCC_DDR/2		USER defined	Buck4	1.5 A
8	DDR_VREF	VCC_DDR/2			GPIO1	0.01 A
3	VCCO_MIO, VCCO	1.8/2.5/3.3 V ±5 %	1.5 A		Buck3	2 A

6 Working with the DA9062

6.1 The DA9062 Evaluation Kit

The DA9062 Evaluation kit includes a flexible evaluation board to allow access to all of the key features of the part. The evaluation kit also includes the Dialog SmartCanvas™ GUI which simplifies the control and configuration of the DA9062.

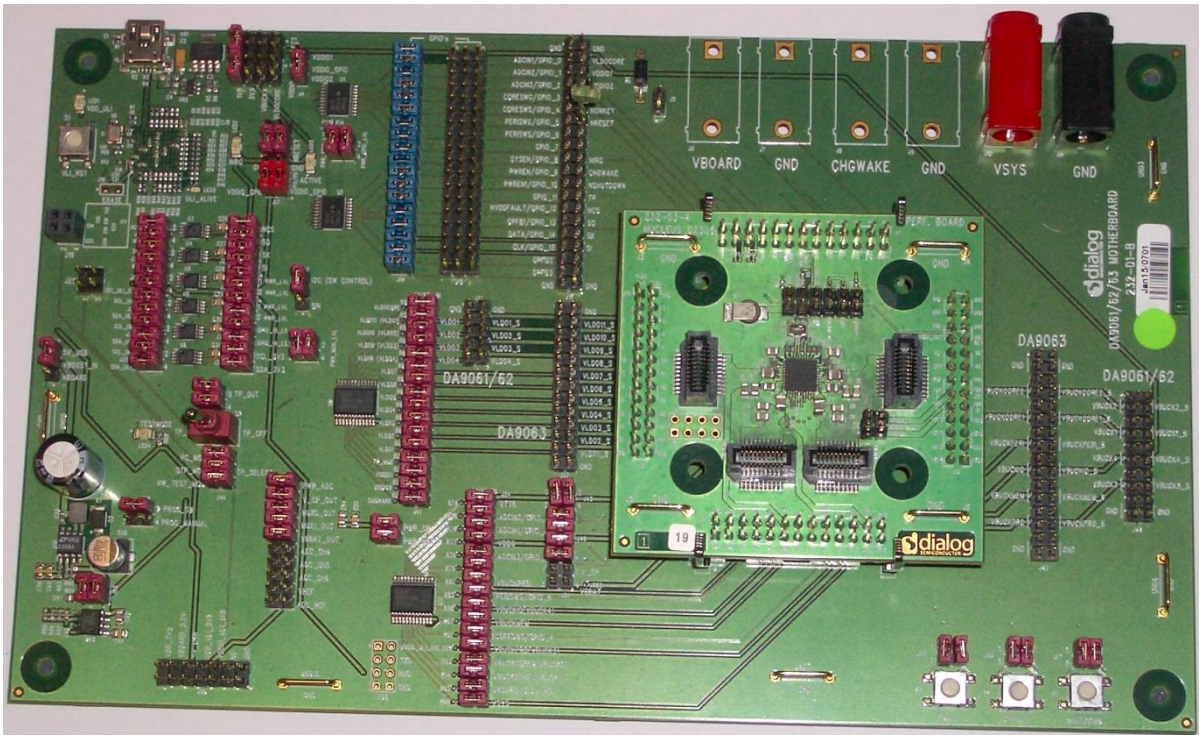

Figure 6: The DA9062 Evaluation Board

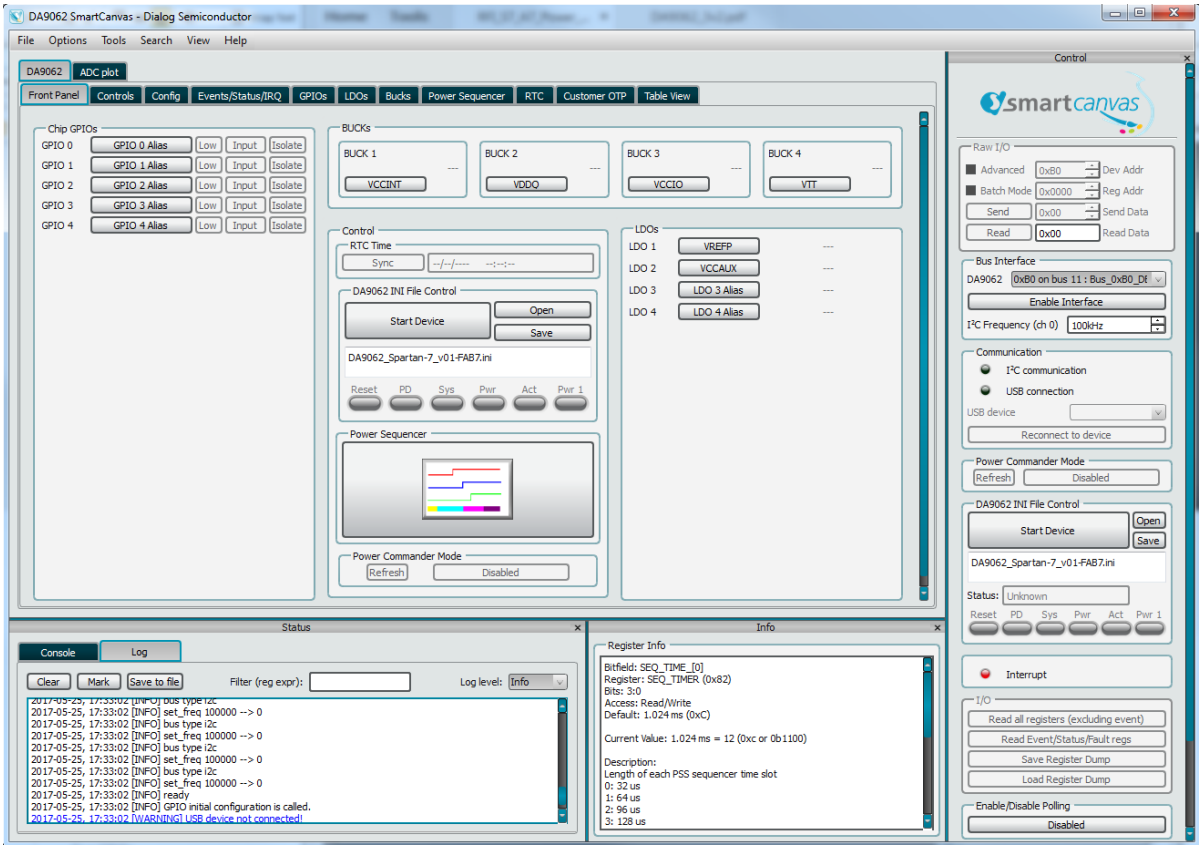

Figure 7: The DA9062 SmartCanvas GUI

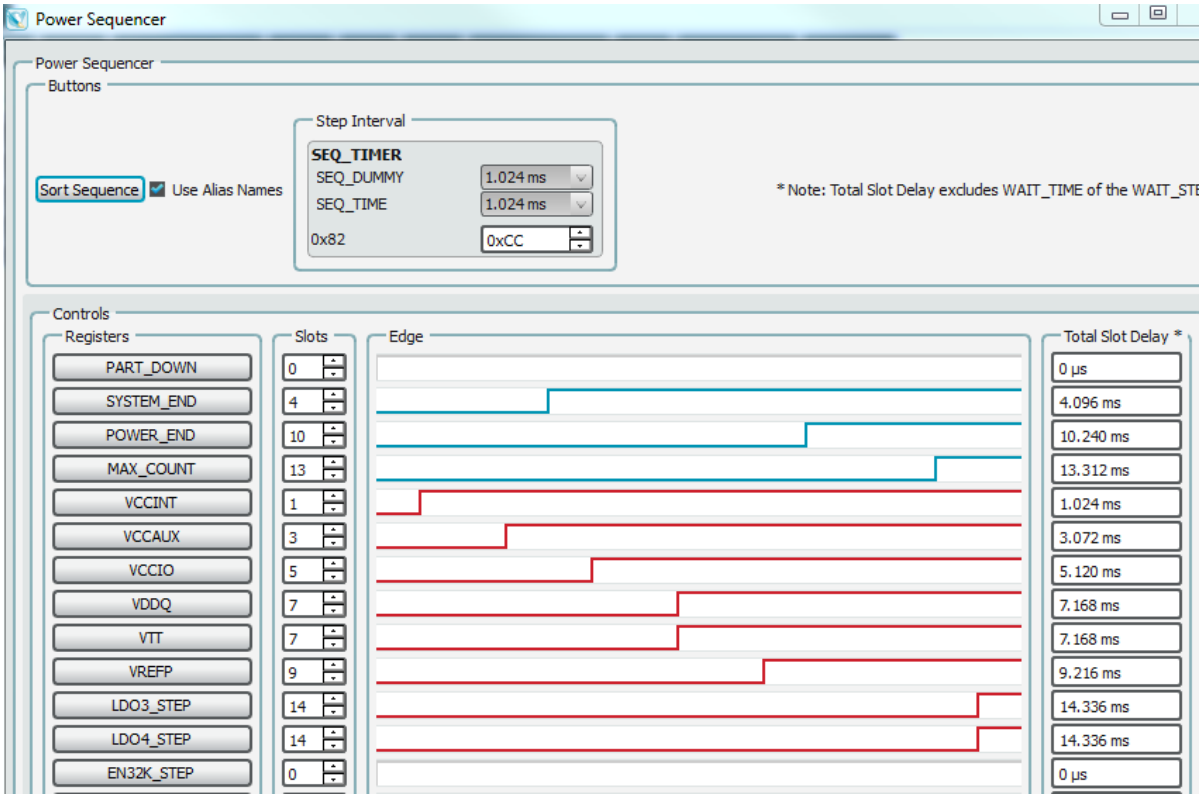

Figure 8: The SmartCanvas Drag and Drop Sequence Tool

6.2 DA9062 Bench Measurements

This section provides some basic performance measurements made using the DA9062 Evaluation kit.

The following measurements are included:

- power-on sequence
- buck efficiency
- static load regulation.
- buck transient load regulation
- reference measurements

6.2.1 Power-On Sequence

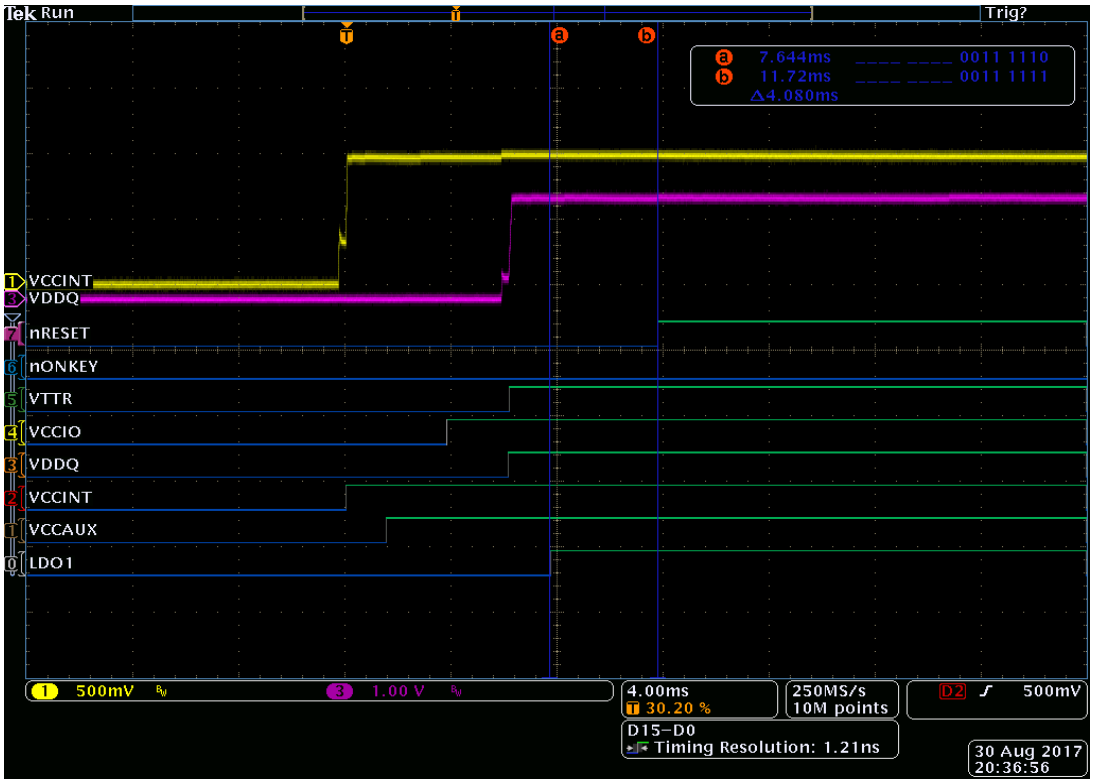

Figure 9: Possible Artix-7 Power-On Sequence

6.2.2 Buck Efficiency

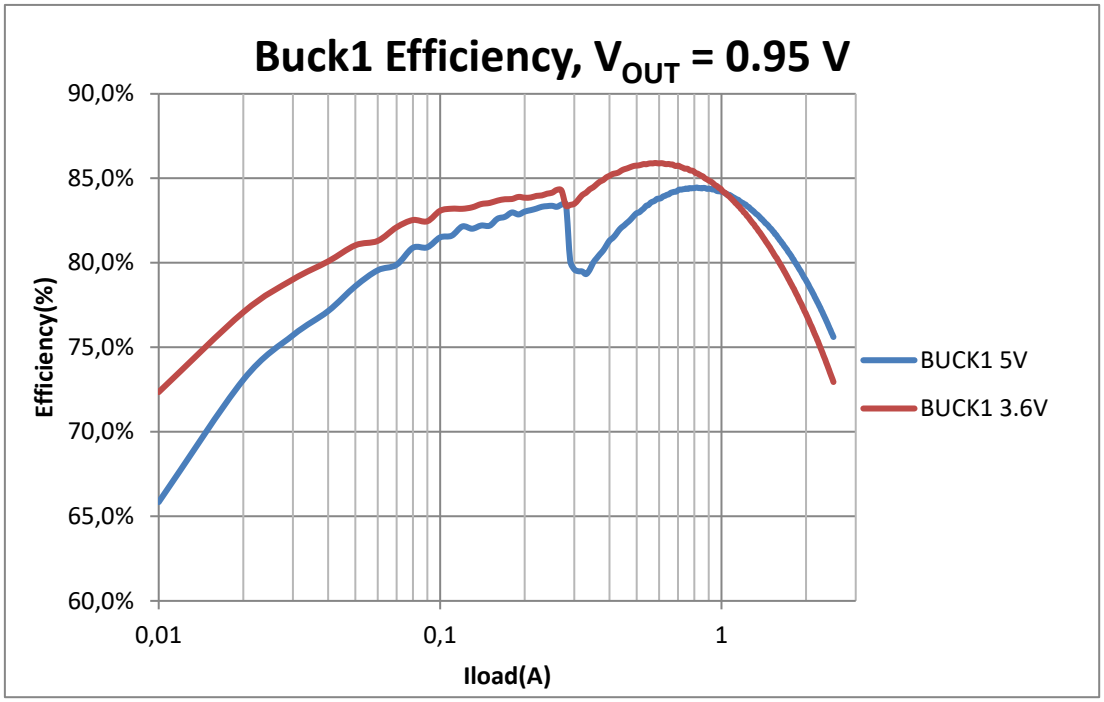

Figure 10: Buck1 Efficiency with V_{OUT} = 0.95 V and V_{IN} = 5 V and 3.6 V

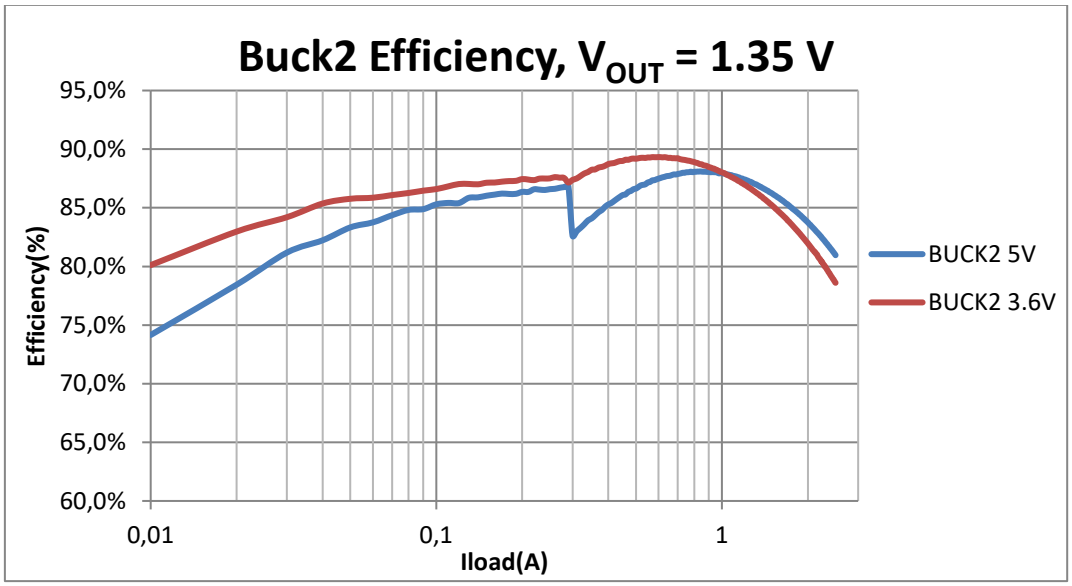

Figure 11: Buck2 Efficiency with V_{OUT} = 1.35 V and V_{IN} = 5 V and 3.6 V

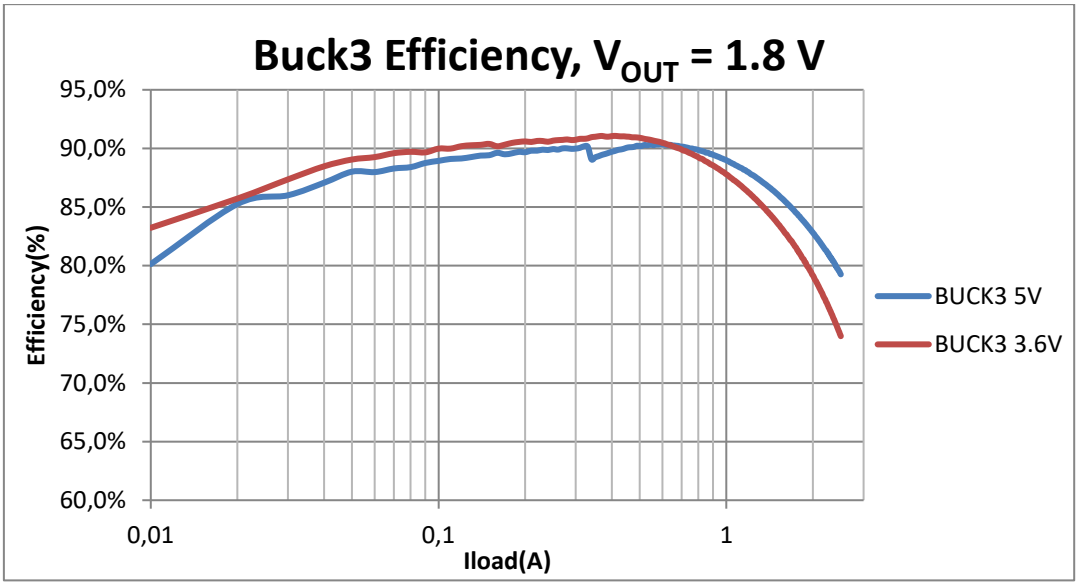

Figure 12: Buck3 Efficiency with V_{OUT} = 1.8 V and V_{IN} = 5 V and 3.6 V

6.2.3 Static Load Regulation

The following static load regulation plots show the variation on the output voltage over a sweep of the load. The buck regulators were running in Auto mode. The change in slope at approximately 300 mA is where the buck transitions from PFM to PWM.

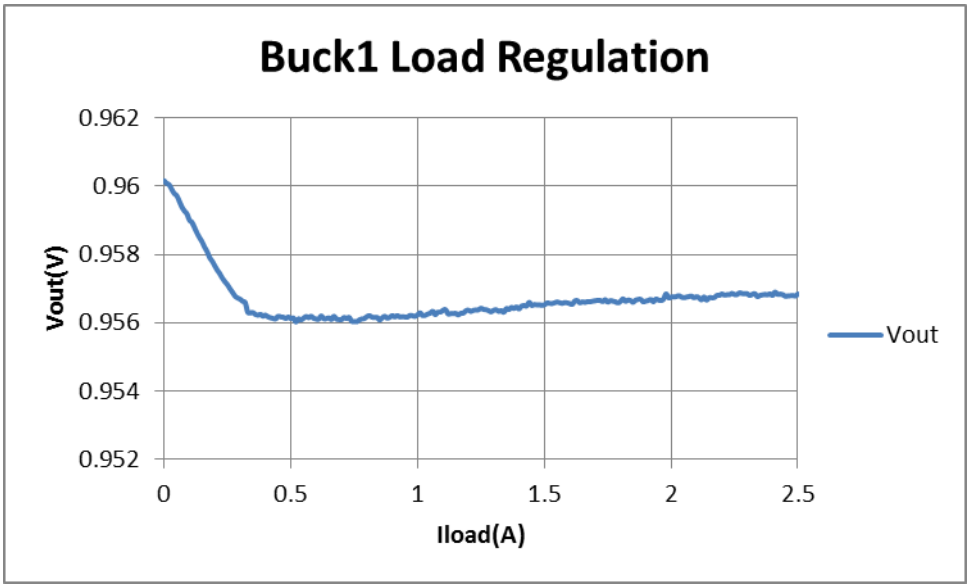

Figure 13: Buck1 Static Load Regulation

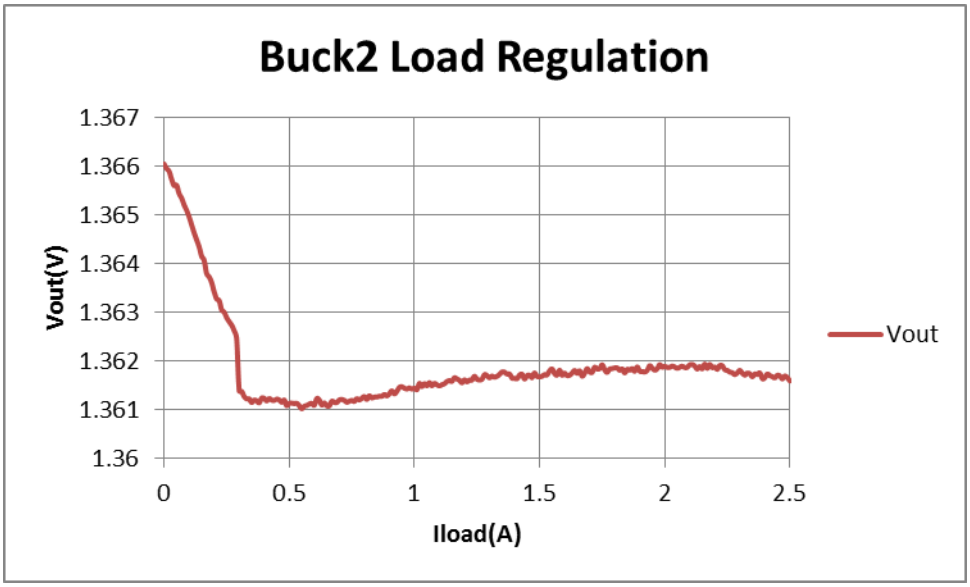

Figure 14: Buck2 Static Load Regulation

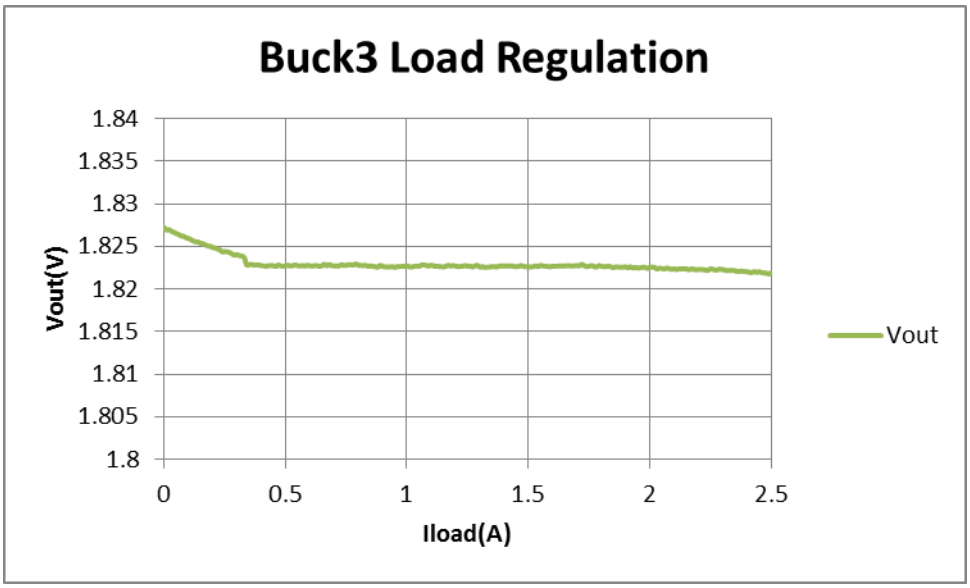

Figure 15: Buck3 Static Load Regulation

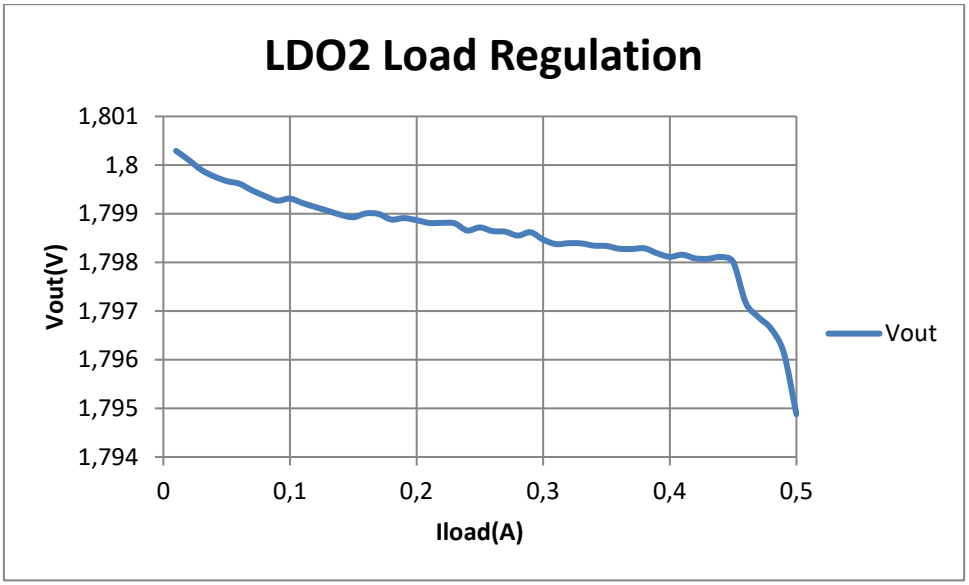

Figure 16: LDO2 Static Load Regulation

6.2.4 Buck Transient Load Regulation

For the transient measurements in this section, the oscilloscope is configured as follows:

- Channel1 (Yellow) shows the regulator output.
  The output was AC coupled, the buck was set to 0.95 V. The Min and Max measurements show the maximum excursion during the transient event.
- Channel 2 (Blue) shows the transient load being applied.
  The Low and High measurements were configured to show the levels of the current pulse waveform. The pulse duration was set to 10 µs.
- Channel 3 (Magenta), where shown, displays the DC coupled output voltage.
- The a and b horizontal cursors show the Xilinx specification limits for the specific voltage rail.

In Table 11, Table 12, and Table 13, the results are given for the transient as a percentage of the maximum load for the regulator. For example, 625 mA is 25 % of 2.5 A. The ±3 % specification is then calculated in mV for comparison against the measured result.

Table 11: VCCINT Transient Load Results

VCCINT (V)	Transient Load			Specification Limit (mV)		Measured (mV)	
	Low (mA)	High (mA)	%	-3 %	3 %	Min	Max
0.95	310	990	25 %	-28.5	28.5	-14	13.2
0.95	310	1310	40 %	-28.5	28.5	-20.8	18.4

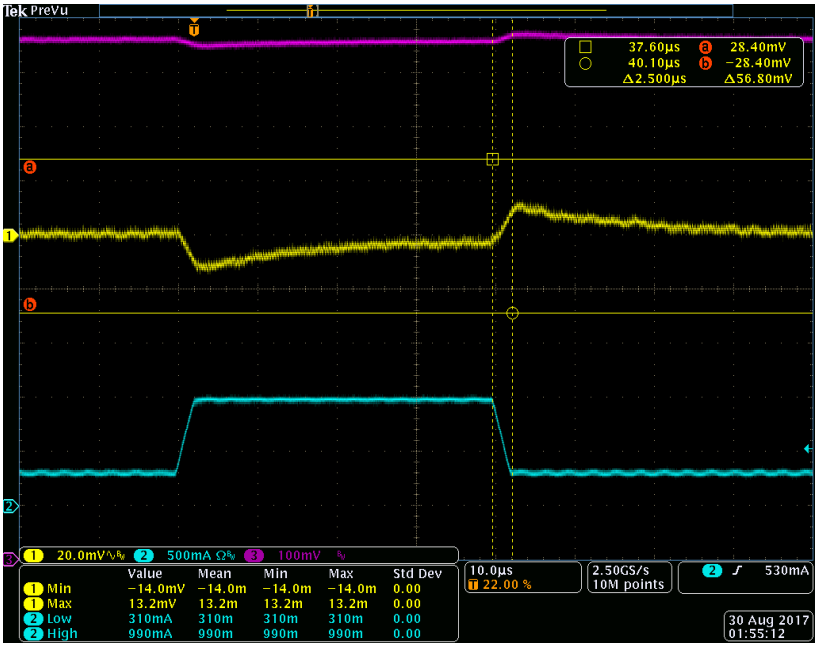

Figure 17: Buck1 Transient Response, 680 mA Step

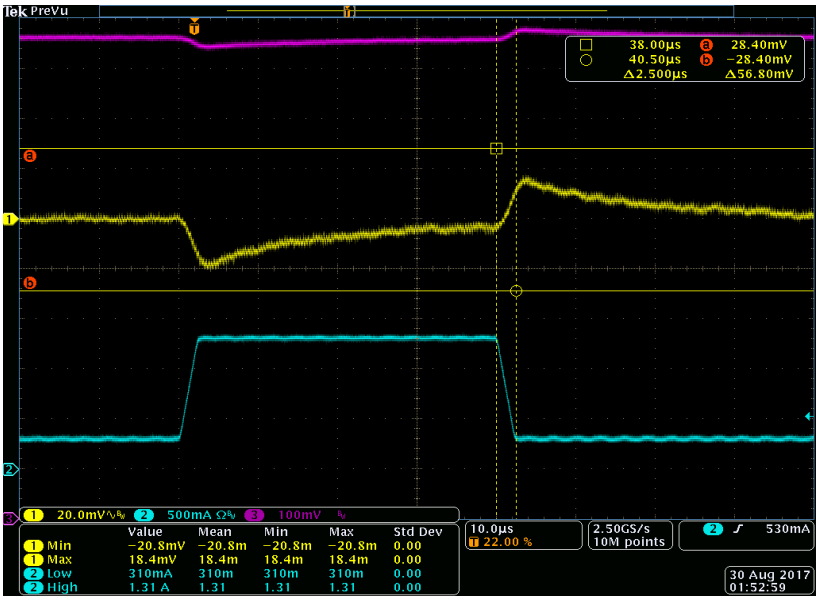

Figure 18: Buck1 Transient Response, 1 A Step

Table 12: Buck2 Transient Load Results

Buck2	Transient Load			Specification Limit (mV)		Measured (mV)	
	Low (mA)	High (mA)	%	-3 %	3 %	Min	Max
1.35	310	1310	40 %	-40.5	40.5	21.2	20.4
1.5	310	1310	40 %	-45	45	-20.4	21.2

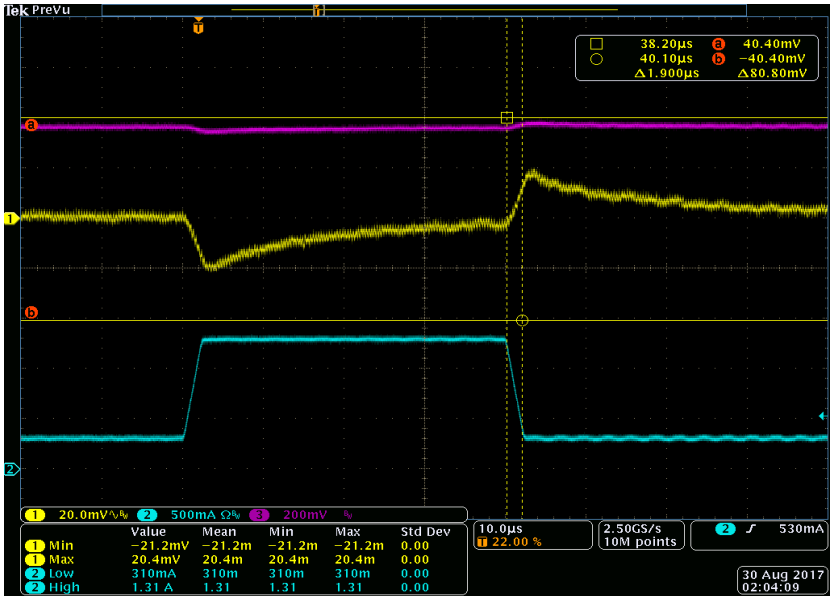

Figure 19: Buck2 Transient Response, V_{OUT} = 1.35 V, 1 A Step

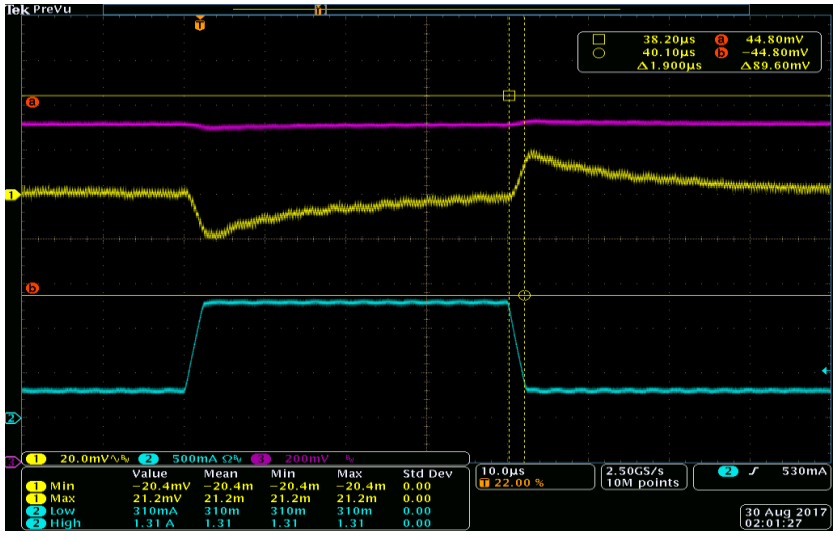

Figure 20: Buck2 Transient Response, V_{OUT} = 1.5 V, 1 A Step

Table 13: Buck3 Transient Load Results

Buck3	Transient Load			Specification Limit (mV)		Measured (mV)	
	Low (mA)	High (mA)	%	-3 %	3 %	Min	Max
2.5	310	1310	40 %	-75	75	-41	35
2.5	310	1570	50 %	-75	75	-55	49
3.3	310	1310	40 %	-99	99	-45	37
3.3	310	1570	50 %	-99	99	-55	51

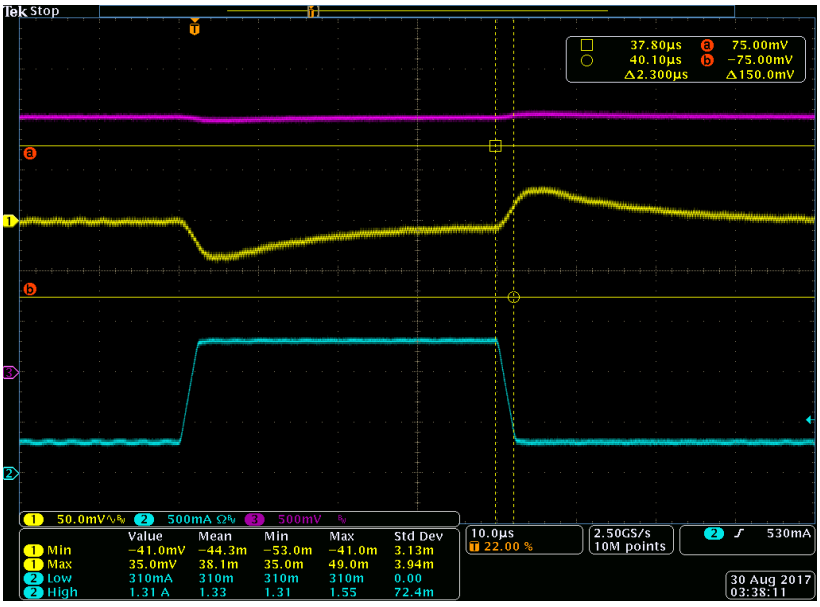

Figure 21: Buck3 Transient Response, V_{OUT} = 2.5 V, 1 A Step

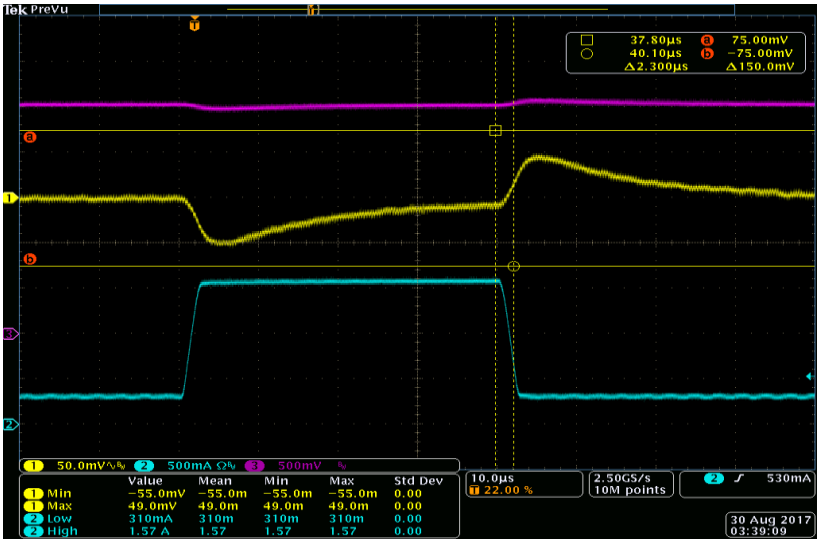

Figure 22: Buck3 Transient Response, V_{OUT} = 2.5 V, 1.25 A Step

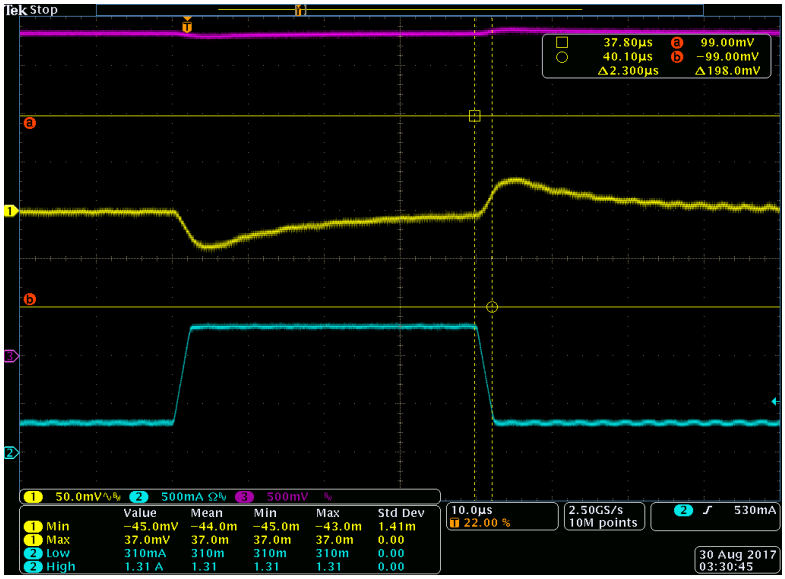

Figure 23: Buck3 Transient Response, V_{OUT} = 3.3 V, 1 A Step

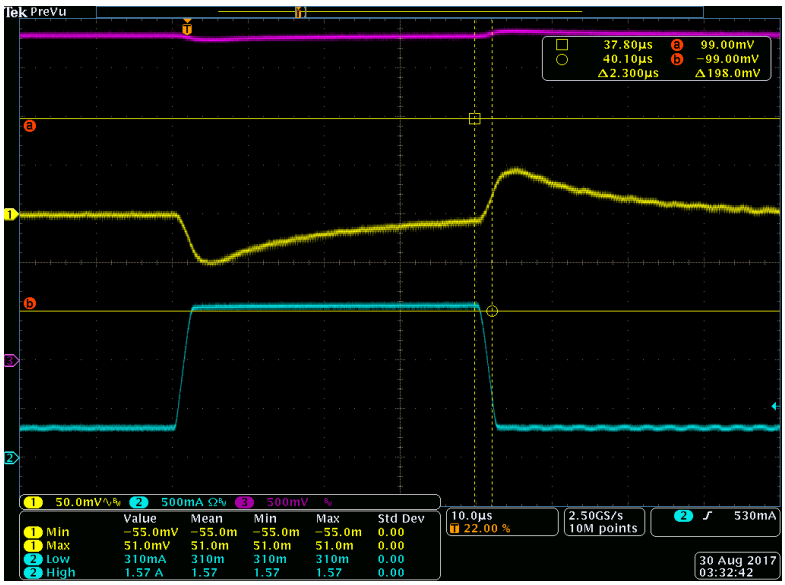

Figure 24: Buck3 Transient Response, V_{OUT} = 3.3 V, 1.25 A Step

6.2.5 Reference Measurements

The operating performance of the PMIC is affected by the performance of the voltage and current references. This section shows the performance of the voltage and current references over temperature.

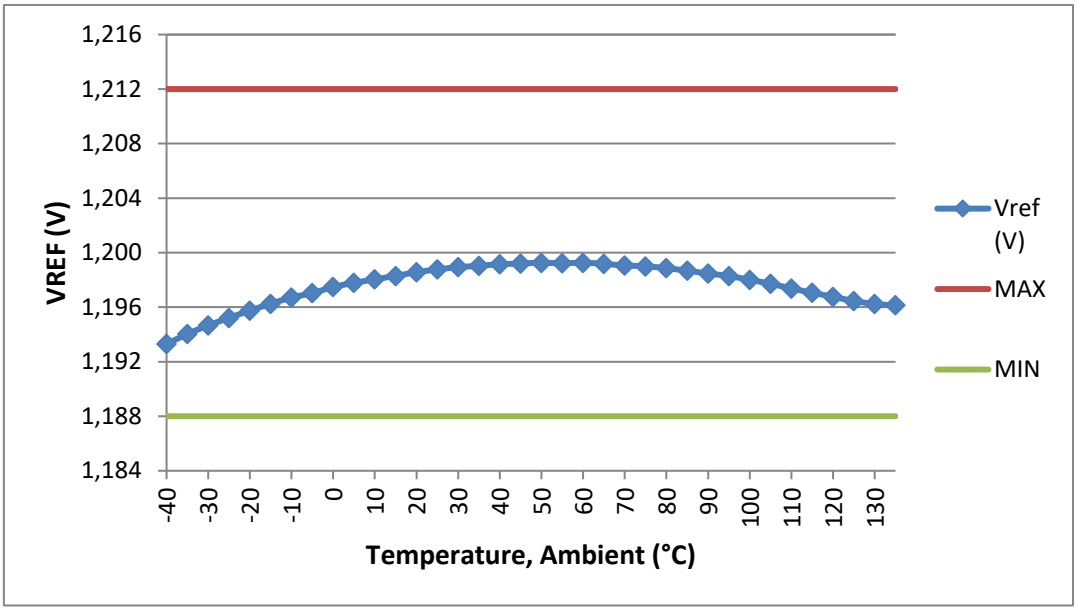

Figure 25: V_{REF} Over Temperature

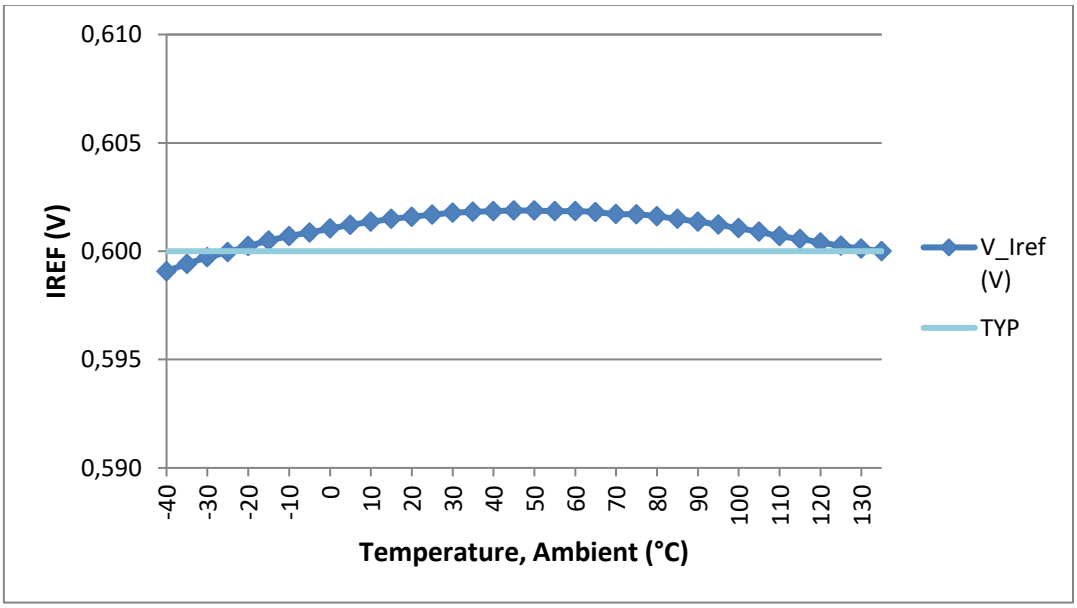

Figure 26: I_{REF} Over Temperature

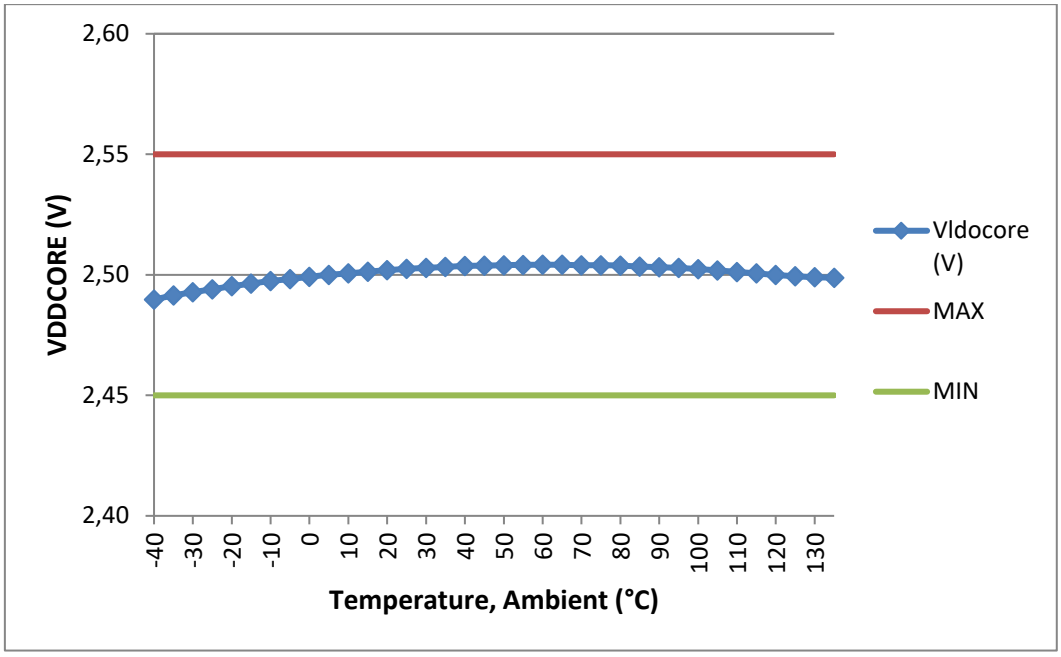

Figure 27: VDDCORE Over Temperature

7 Conclusions

The Dialog range of system PMICs can support the whole Artix-7 family of devices from Xilinx. From the DA9062 which is ideal for the smaller members of the Artix-7 family, to a combination of the DA9063L and a DA9211 sub-PMIC which, when combined, can service the requirements of the largest member of the Artix-7 family. This flexibility can also be extended to support the Zynq -7000 family of devices.The Dialog system PMICs, through the use of OTP, provides the ability to customize the power solution to optimally meet the needs of the most complex system.

Revision History

Revision	Date	Description
1.0	08-May-2018	Initial version.
1.1	24-Feb-2022	File was rebranded with new logo, copyright and disclaimer

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
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