ac_controller Project Status (07/16/2022 - 00:51:24)			
Project File:	HW6_99109393.xise	**Parser Errors:**	No Errors
Module Name:	ac_controller	**Implementation State:**	Synthesized
Target Device:	xc3s50-5pq208	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	14 Warnings (12 new)
Design Goal:	Balanced	• **Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	1137	768	148%
Number of Slice Flip Flops	75	1536	4%
Number of 4 input LUTs	2083	1536	135%
Number of bonded IOBs	42	124	33%
Number of GCLKs	1	8	12%

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Sat Jul 16 00:51:22 2022	0	14 Warnings (12 new)	0
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
ISIM Simulator Log	Out of Date	Sat Jul 16 00:47:18 2022	

Date Generated: 07/16/2022 - 00:51:24