UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Object-Oriented Modeling of Electronic Circuits, Spring 1401
Computer Assignment 3 (version 0.9)
RTL Design and SystemC Simulation

In this assignment, you are to design and simulate "*Least Recently Used Updater"* circuit (**LRU**), which is used in page replacement of memory management. Page replacement is a widely used approach in memory management. The idea is simple: the main memory cannot hold all the referred pages in memory. So whenever a new page is referenced, an existing page is replaced by the page that was newly called. The goal of any page replacement mechanism is to minimize the number of page faults.

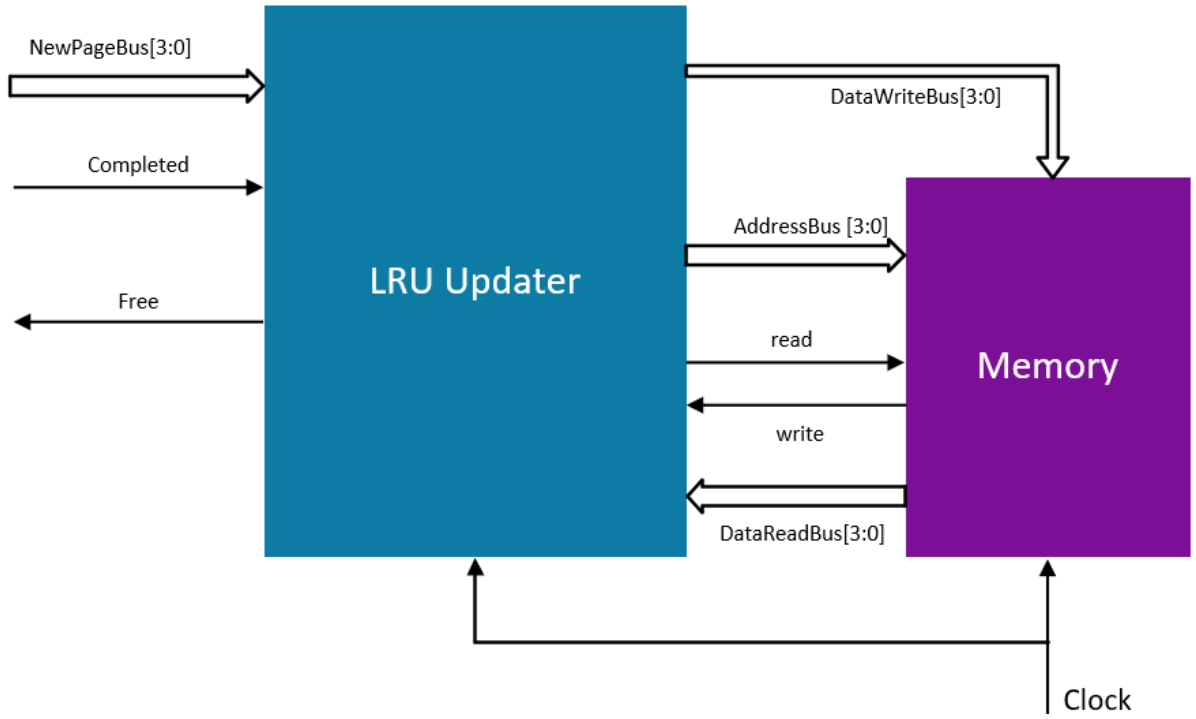

Figure 1. LRU Updater

Consider that We have sixteen pages with tags from 0 to 15 (0 is the most recently used and 15 is the least recently used). The tag of each page is defined using a 4-bit binary number that are kept in a Memory. As shown in figure 1, the Memory needs a 4-bit address bus and two 4-bit data buses. *NewPageBus* input provides the ID of the current page that has just been accessed. A pulse on the *completed* input shows that the page access has been completed and the LRU memory needs to be updated. All pages with lower tag than the tag of the recently accessed page must increment their

tag by one. To do this, you can examine all entries of the memory one by one and increment tags that are lower than that of the current page. The entry that corresponds to the current page should be set to zero indicating this page will be the most recently used. Other entries that have higher tag values should be kept intact. After updating the Memory, the output free signal becomes one. (as an example see figure 2)

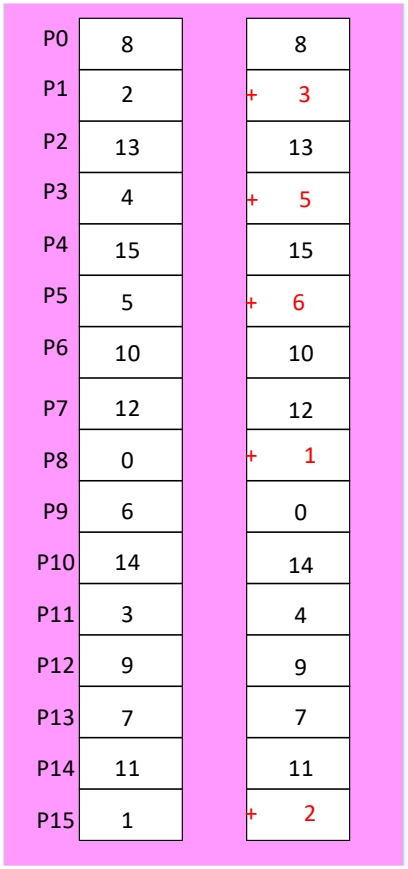

Figure 2. Before and after P9 is accessed

a) Using signals shown in the figure 1, design a datapath and a controller for the LRU Updater box. Show the components of your datapath and the necessary internal signals. Draw a state diagram that clearly describes the behavior of your controller and issuance of control signals. (**Hint:** use a counter for addressing the memory in your datapath.)

b) Write the SystemC RTL description of the LRU Updater and its memory. Wire these two modules and create a top level module with the inputs and output mentioned above.

c) Write a testbench to simulate your design and generate a VCD file. Examine your design with multiple instances and Add waveforms to your report.

d) Consider the LRU circuit discussed above and design another solution, in which updating is completed in one clock cycle. Use shift registers with enable input and comparators. Each register stores the page number and has a fixed tag which is from 0 to 15 (0 is MRU and 15 is LRU). This circuit has two inputs named *NewPageBus* and *completed* and no output. Add your design in the report. (no code is required for this part)

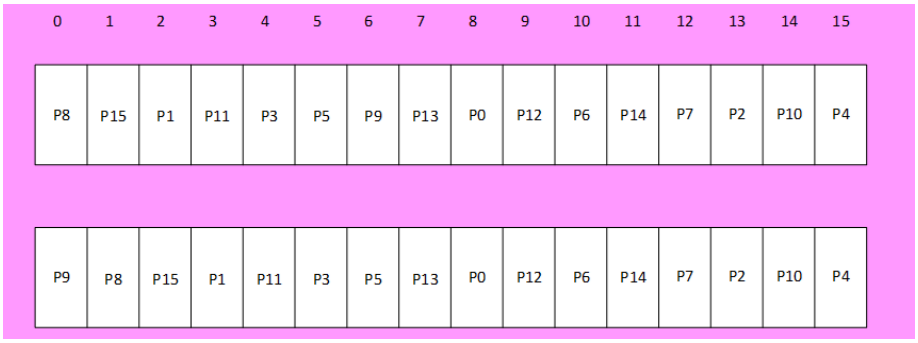

Figure 3. Before and after P9 is accessed in the second solution

e) Write a functional SystemC description of LRU Updater and simulate it. In your report compare the waveform with part c.

Deliverables:

a) Generate a report that includes item discussed below:
   1) Show complete circuit diagram that you are analyzing. Draw datapath and state diagram in RTL design.
   2) Add images of test bench and output wave forms with signal names being displayed.

b) Include your codes in a folder beside your report.

Make a .zip file and name it with the format shown below:

LastName_Studentnumber_CAnn-ECE01