UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Object-Oriented Modeling of Electronic Circuits, Spring 1401
Computer Assignment 2
Gate Level Simulation with Timing

Name
Date

In this homework, you will be developing gate classes for performing time simulation on the input circuit. The gate-list input is to be taken from a Verilog file with the format discussed in Computer Assignment 1, which only uses NOT, AND, NAND, OR, NOR, and XOR primitives with a single delay value that is followed by a sharp-sign (#).
Use your internal structure, you will be doing several works, including outputting C++ classes for event-based timing simulation in a C++ environment, developing a gate-level simulator with timing in C++, and calculation of controllability and observability. In addition, you will output your simulation reports in a text file.

The following tasks are to be performed in this assignment:

Task 1) Develop C++ gate classes which have delay parameter and time scheduling. The time scheduling shows next propagation with timing details. Also, write a wire class which saves all events on the wire.

Task 2) Write a C++ program with global variables named '*present_time'* and '*time_resolution'*. Include a main While loop in which time increases by the resolution. In each iteration check all the gates' time schedule and evaluate those with less last event time. Take a text file as the input of the circuit with each line specifying an input test value set at a given time, e.g., #16 0110, for 0110 applied to the inputs 16 time units after the previous one.

Task 3) Generate an output text file similar the input file.

Task 4) Calculate controllability and observability values.

Task 5) Trace critical path to find longest active path.

Deliverables:

Generate a report that includes item discussed below:

A. Show the circuit diagram that you are analyzing. Show gates and/or transistors according to the specified delays.

B. Hand-simulate the circuit you have shown in Part A and write your expected values. For example, indicate what values you expect for the worst-case delays and express your reason for that.
C. Show an image of the project that you have created for the simulation of your circuit.
D. Include an image of the output file showing signal names being displayed.

Make a PDF file of your report and name it with the format shown below:

FirstinitialLastname-Studentnumber-CAnn-ECEmmm

Where *nn* is a two-digit number for the Computer Assignment, *mmm* is the three-digit course number under which you are registered, and hopefully you know the rest. For the *Firstinitial* use only one character. For *Lastname* and for the multi-part last names use the part you are most identified with. Use the last five digits of your student id (exclude 8101) for the *Studentnumber* field of the report file name.