UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Object-Oriented Modeling of Electronic Circuits, Spring 1401
Computer Assignment 1
Gate Level Analysis in C++ (Preliminary, More to come)

Name:
Date:

In this assignment, you will read a gate-level circuit written in Verilog and translate it to an internal structure in C++. Using this internal structure, you will be doing several analyses including a gate level simulation. This input netlist is a line-oriented Verilog gate-level description that only uses NOT, AND, NAND, OR, NOR, and XOR primitives. Gate primitive instantiations are considered concurrent statements and no assumption is made on the ordering of the gates. An example circuit from the ISCAS'85 benchmark circuits[1] is made available for you to use for testing your programs. For the purpose of this assignment:

1- Timing details are not considered.
2- There is no feedback in the circuits.
3- All the circuits are combinational.

The following tasks are to be performed in this assignment:

Task 1) Take the Verilog gate-level description as the input file and write a Verilog Reader Program to translate this to an internal C++ structure. You will mature this internal structure as you progress through this homework and perhaps on other programming homeworks in this course.

Task 2) In your data structure, include a *Level* for each gate. Circuit primary inputs are at Level 0, and gate levels increase as they get farther away from the inputs and closer to the outputs of the circuit. A gate *Level* is the largest level of all its inputs plus 1.

Task 3) Write a code that generates a Verilog file in which gates are listed according to their level numbers.

[1] The ISCAS'85 benchmark circuits are ten combinational networks provided to authors at the 1985 International Symposium on Circuits And Systems. They subsequently have been used by many researchers as a basis for comparing results in the area of test generation.

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Task 4) Using the internal data structure, write a gate level simulator with input data read from a file and output written into an external file. The simulator stimuli are specified in a text file with each line indicating an input test value set, e.g. 0010 can be applied to a 4 input circuit. Write a program which simulates the input circuit with the help of "*Level"* variable. The simulator generates an output text file similar to the input file.

Task 5) Controllability of a line in a digital circuit is defined as the difficulty of setting a particular logic signal to 0 or 1. Compute the 1-controllability of each gate's output and print them as comments after each gate's description in a Verilog output file, like that of Task 3.