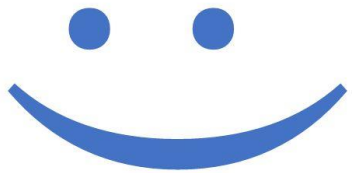
*In the name of God*




علیرضا کاویان

Alireza Kavian

استاد مسعود ده یادگاری

Professor Deh Yadegari

# پروژه ی طراحی پردازنده
# Cpu design project

## طراحی مولتی سایکل با وی اچ دی ال
## Multi cycle design with VHDL

توضیحات، کد، شبیه سازی، دیاگرام موج زمانی
Explanation, Code, Simulation, time wave

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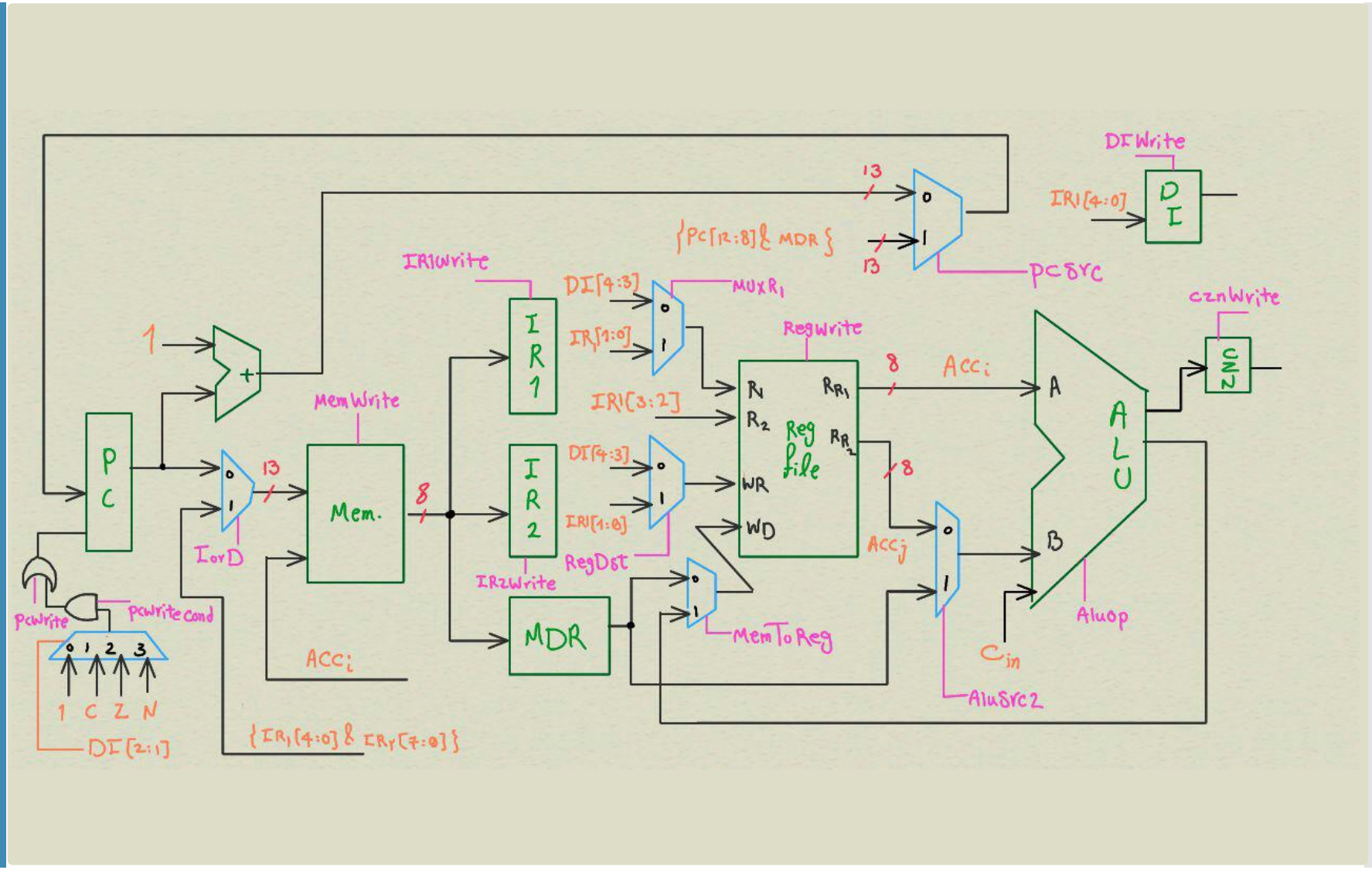
#CPU

#Designing

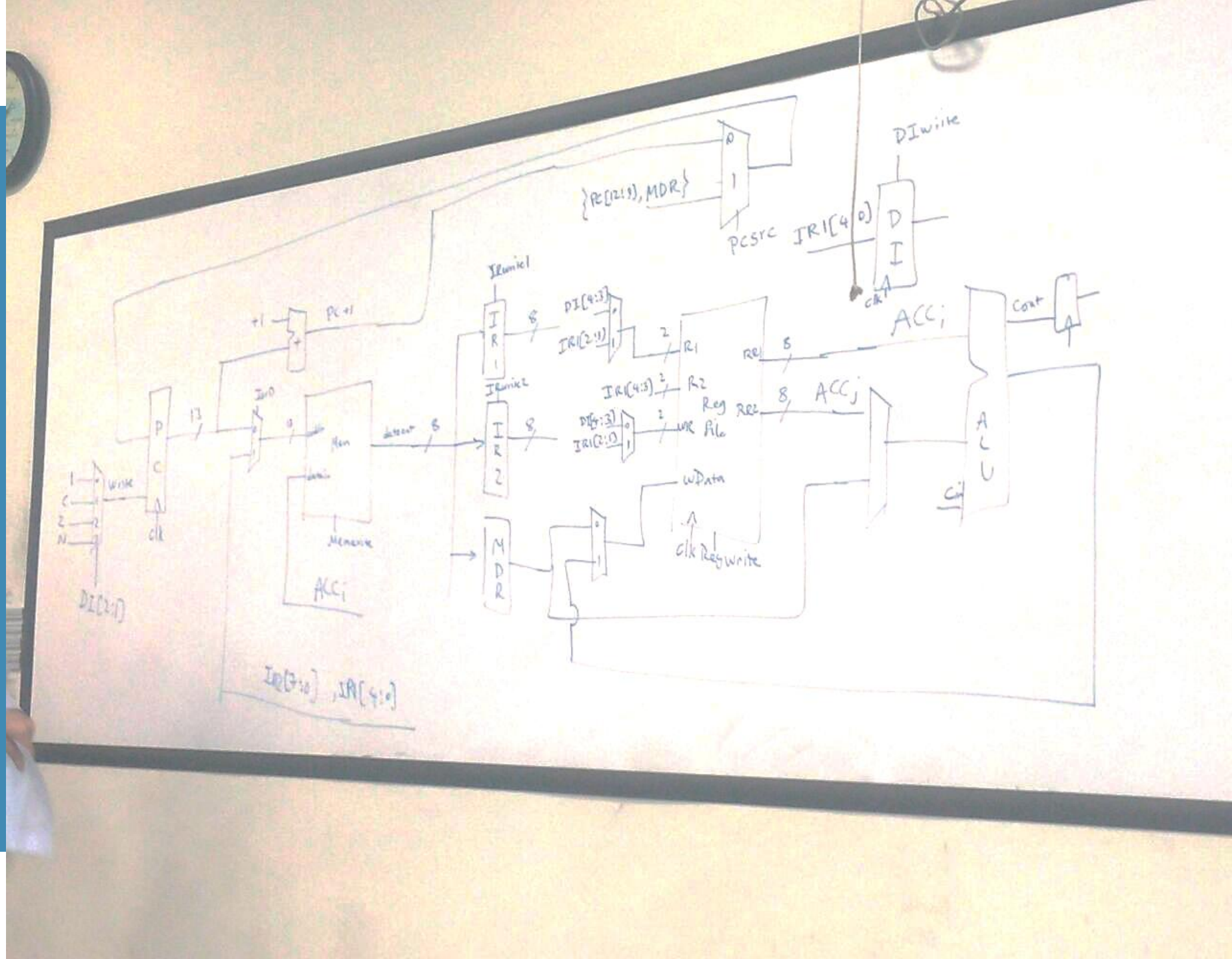
#MultiCycle

#MidTerm2

#ComputerArchitecture



#DataPath

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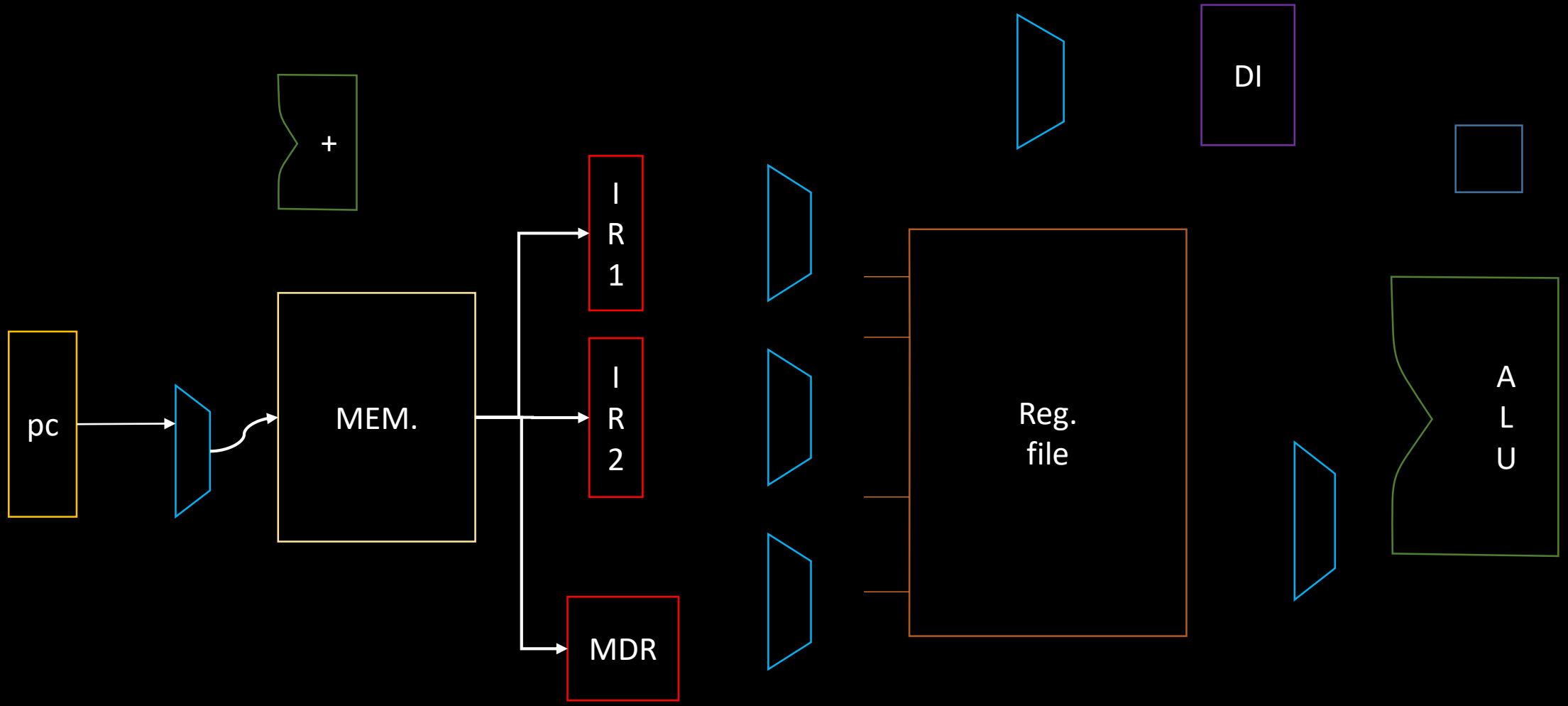
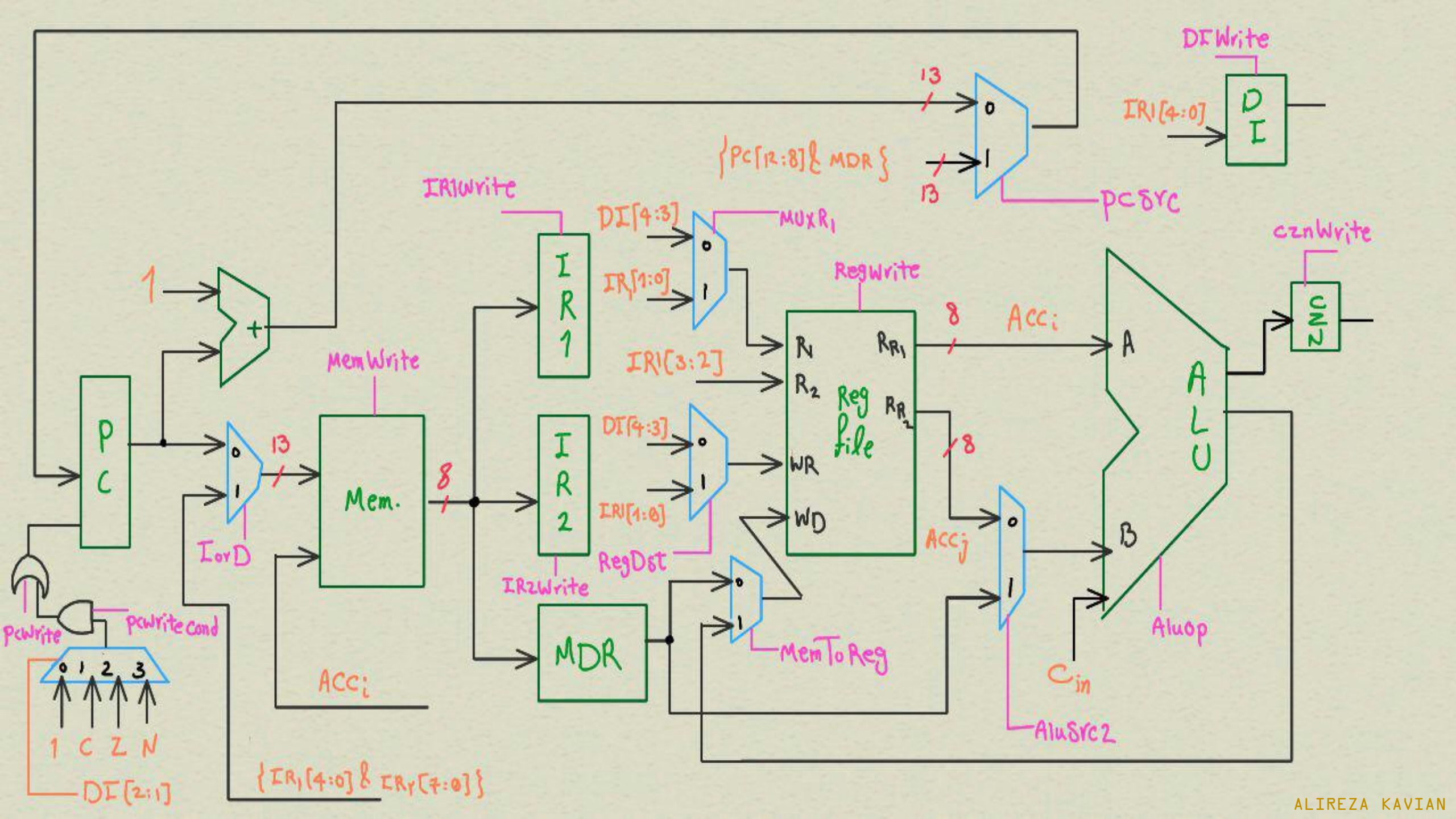

+
DI
I
R
1
I
R
2
pc
MEM.
Reg.
file
A
L
U
MDR

# Instruction Set Architecture

| Instruction Mnemonic and Definition | | Bits 7:4 | RTL Notation |
|---|---|---|---|
| **Address Instruction** | | | |
| LDA | Load Addressed | 000 | $Ac_i$ <- (Address) |
| STA | Store Addressed | 001 | (Address) <- $Ac_i$ |
| ADA | Add Addressed | 010 | $Ac_i$ <- $Ac_i$ + (Address) + C |
| ANA | AND Addressed | 011 | $Ac_i$ <- $Ac_i$ & (Address) |
| **Accumulator Instruction** | | | |
| MVR | Move Registers | 1000 | $Ac_i$ <- $Ac_j$ |
| ADR | Add Registers | 1001 | $Ac_i$ <- $Ac_i$ + $Ac_j$ + C |
| ANR | AND Registers | 1010 | $Ac_i$ <- $Ac_i$ & $Ac_j$ |
| ORR | OR Registers | 1011 | $Ac_i$ <- $Ac_i$ \| $Ac_j$ |
| **Addressed Jump** | | | |
| JMP | Jump Addressed | 110 | PC <- (Address) based on flags and DI |
| **LDI Instruction** | | | |
| LDI | Load Direction | 111 | DI <- IR[4:0] |

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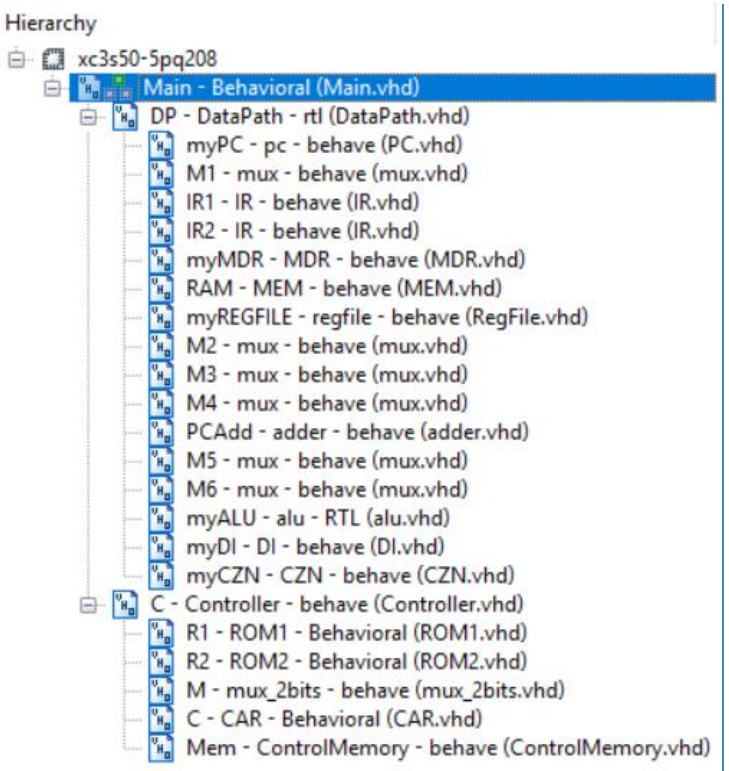
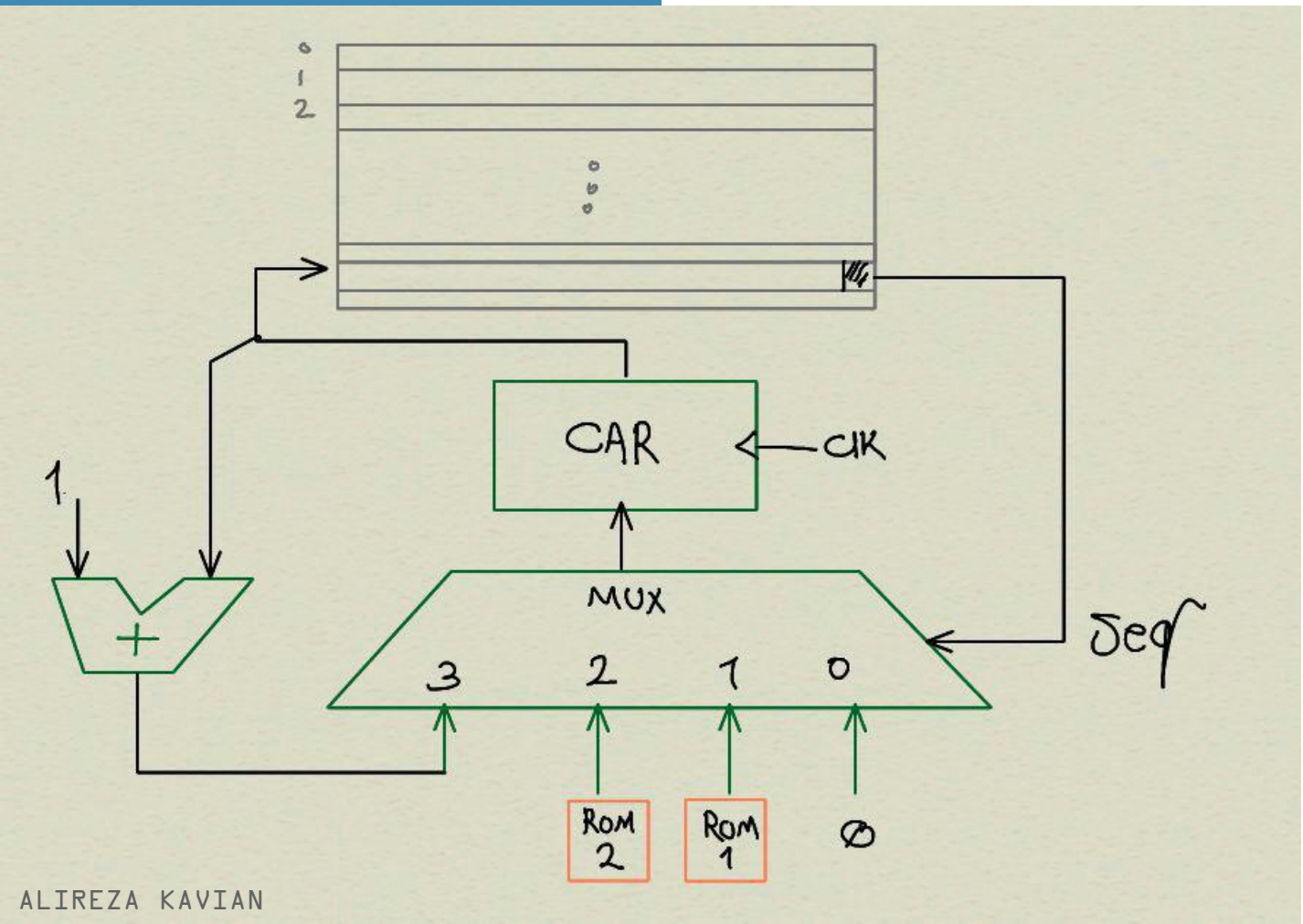



#Hierarchy

ابتدا برای هر باکس در datapath یک فایل جداگانه ی vhdl تعریف کردم؛
سپس همه ی آنها را در فایل DataPath.vhd به هم وصل کردم.
برای این پروژه نیاز به کنترل داریم ، که من از روش micro programming استفاده کردم و بدین منظور یک فایل Controller.vhd نیز تعریف کردم که در آن ، کامپوننت ها متناظر به هم وصل شده اند.
در انتها یک فایل Main.vhd ایجاد کرده و فایل های DataPath.vhd و Controller.vhd به هم map شده اند!

At first, we initialize a separate file for each module (component) in the datapath.
Then we connect all of them in file: DataPath.vhd.
For this Project, we'll need a controller I have used micro programming controller and I initialized a file (Controller.vhd) and the corresponding needed components is connected to each other.
At the end, I've created a top module named: Main.vhd and two last components are connected in it. I mean DataPath.vhd and Controller.vhd

#MicroProcessing




برای ساخت کنترلر بایستی از یک حافظه ی اضافی برای ذخیره ی بیت های کنترلی استفاده شود. و همچنین از چند Rom کمکی استفاده میکنیم تا شماره خطی باید پردازش شود را به دست دهد!

To create a controller, we should use another memory to save the controlling bits.
And so we use two ROMs to help us for finding the current line (row) on the controller memory.

#Rom1

#Rom2

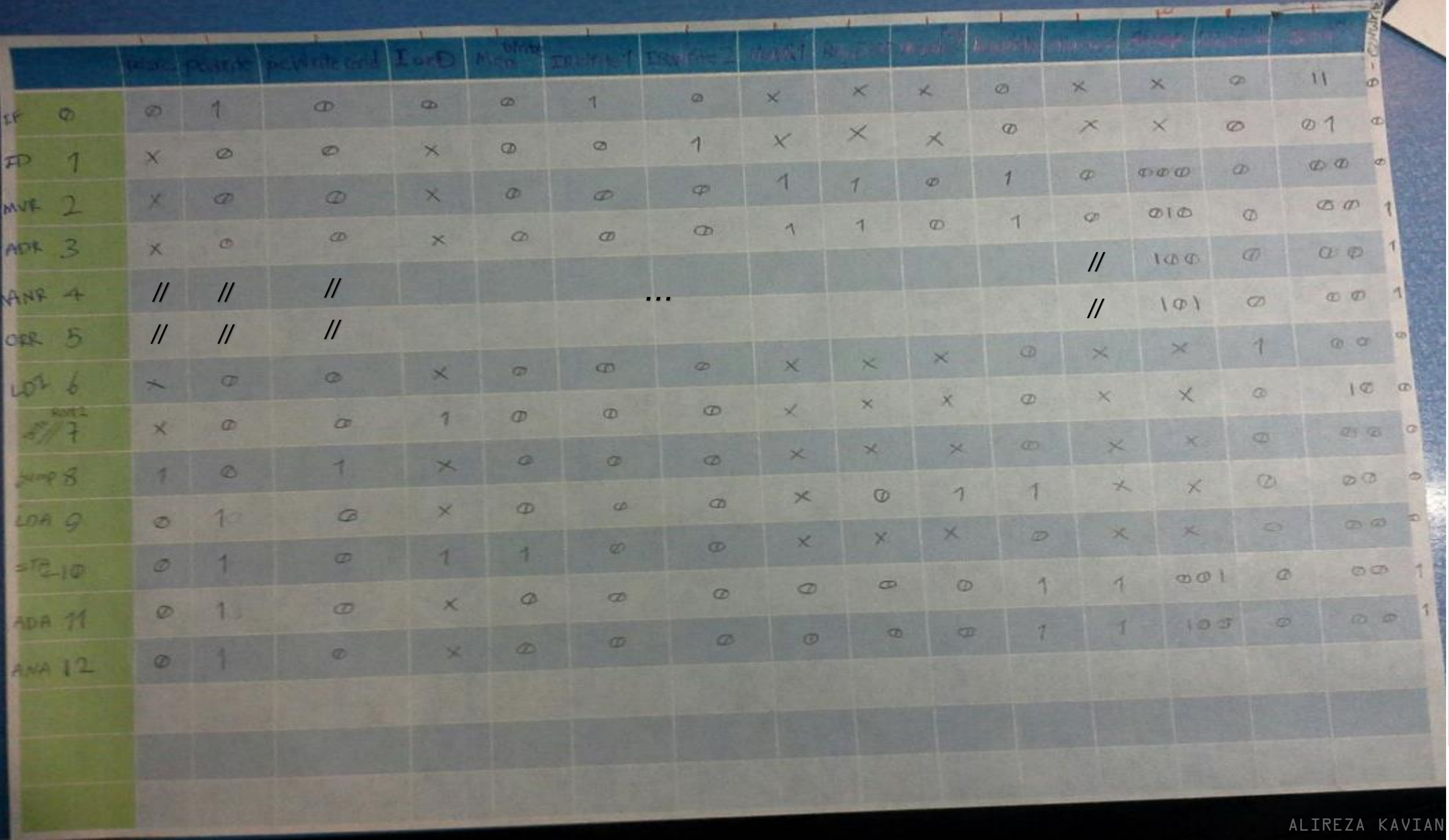
#ControlMemory contents

| op code | Name | ROM Content |
|---|---|---|
| 1000 | Accum. R-type | 2 |
| 1001 | | 3 |
| 1010 | | 4 |
| 1011 | | 5 |
| 111 | LDI | 6 |
| 110 | JMP | 7 |
| 000 | Load store | 7 |
| 001 | | 10 |
| 010 | | 7 |
| 011 | | 7 |

ROM1

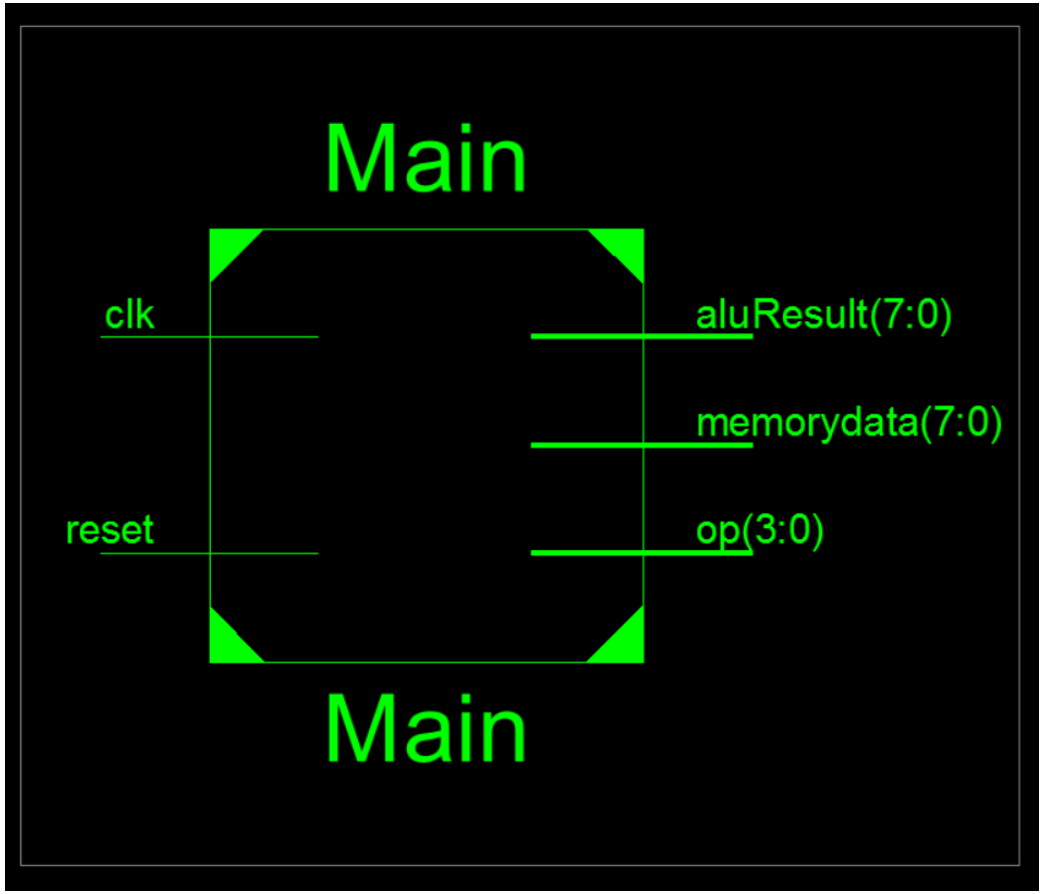
| opcode | name | ROM Content |
|---|---|---|
| 110 | JMP | 8 |
| 000 | LDA | 9 |
| 010 | ADA | 11 |
| 011 | ANA | 12 |

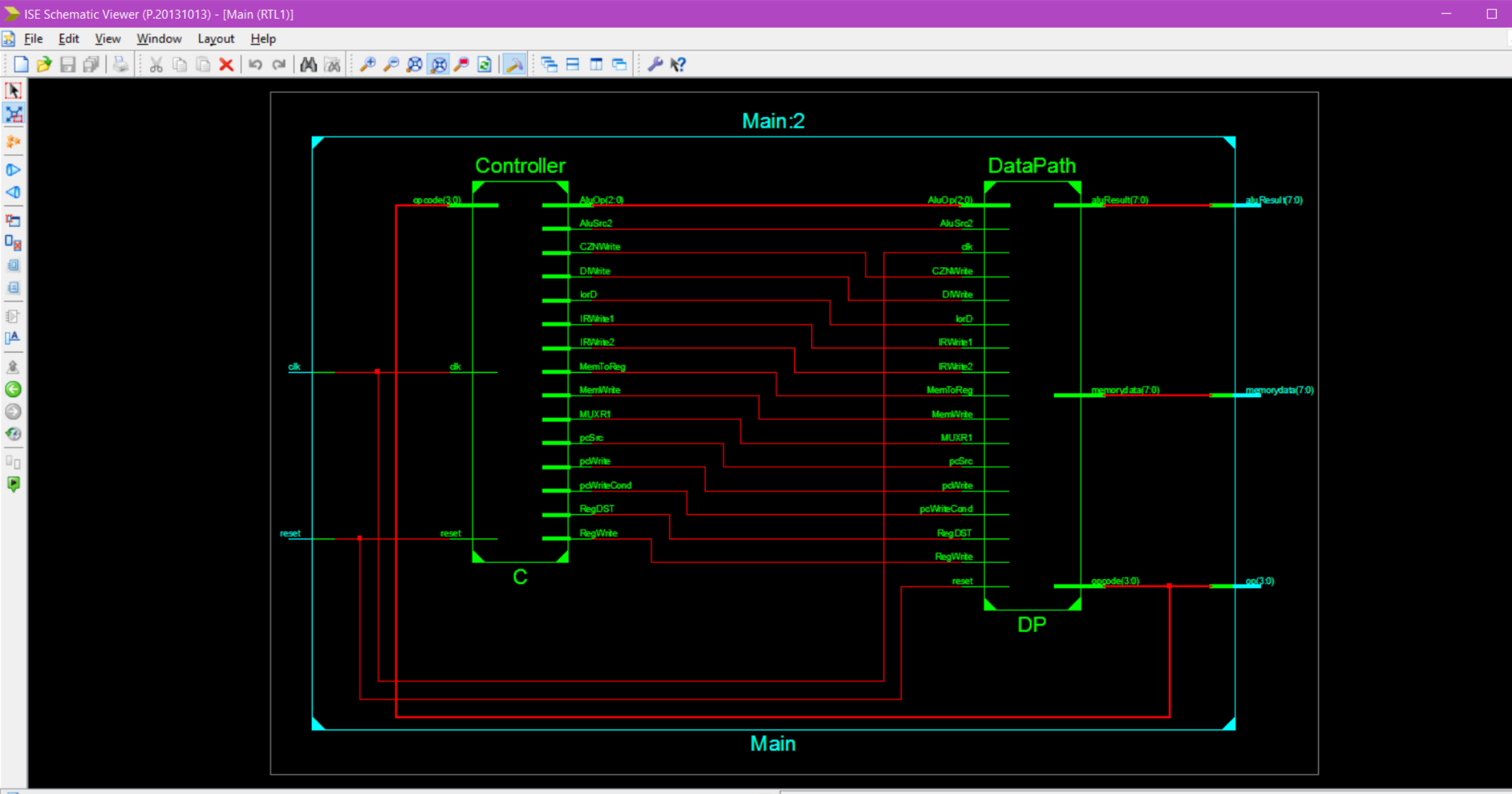
ROM2




Control Memory Contents

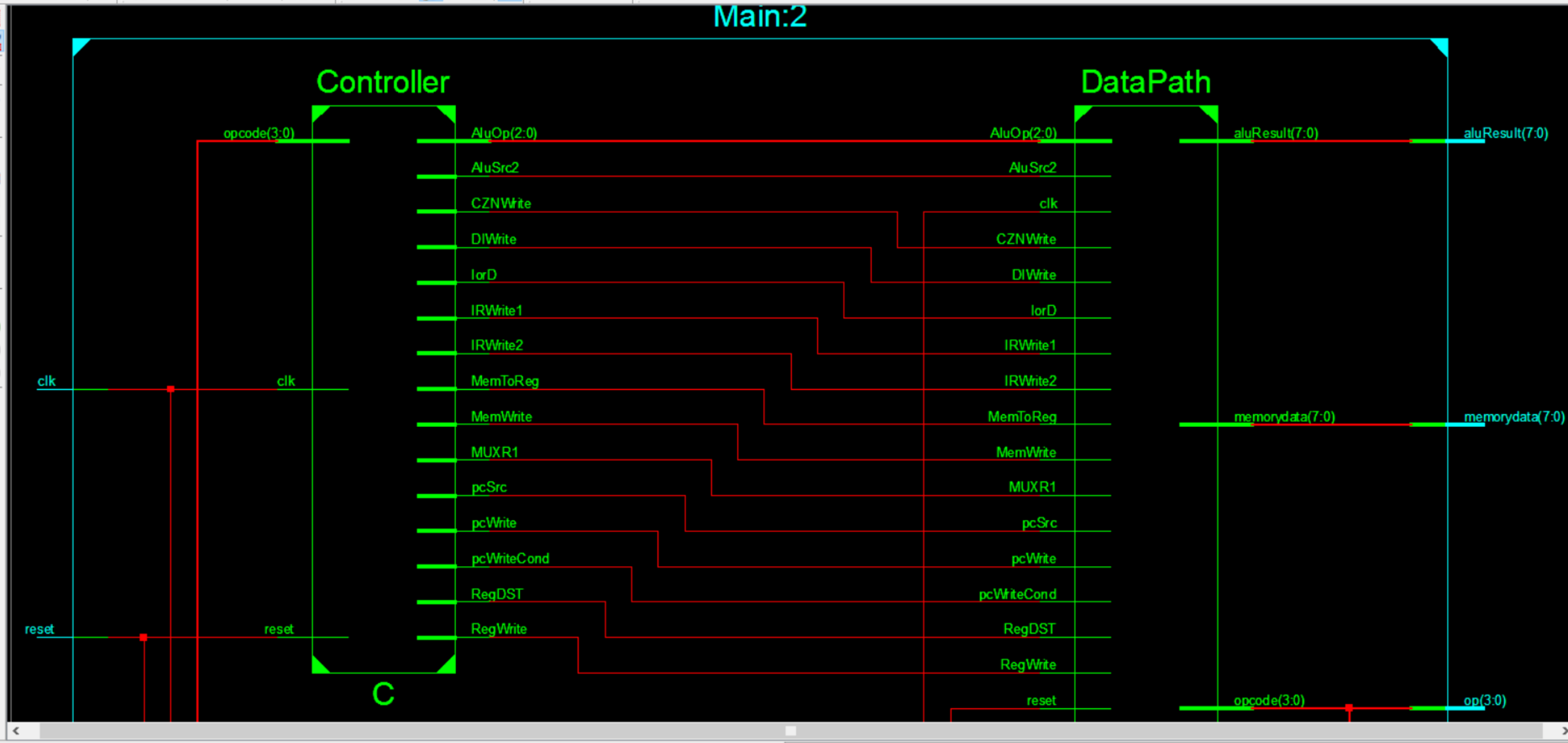
# #Main Module
# #schematic
# #components




ISE Schematic Viewer (P.20131013) - [Main (RTL1)]
File
Edit
View
Window
Layout
Help
Main:2
Controller
DataPath
op code(3:0)
AluOp(2:0)
AluSrc2
CZNWrite
DIWrite
IorD
IRWrite1
IRWrite2
MemToReg
MemWrite
MUXR1
pcSrc
pcWrite
pcWriteCond
RegDST
RegWrite
clk
reset
C
aluResult(7:0)
memorydata(7:0)
opcode(3:0)
op(3:0)
DP
Main
Main (RTL1)
View by Category
Design Objects of Top Level Block
Properties of Instance: Main

ISE Schematic Viewer (P.20131013) - [Main (RTL1)]

File Edit View Window Layout Help




Main (RTL1)

View by Category

Design Objects of Top Level Block

Properties of Instance: Main

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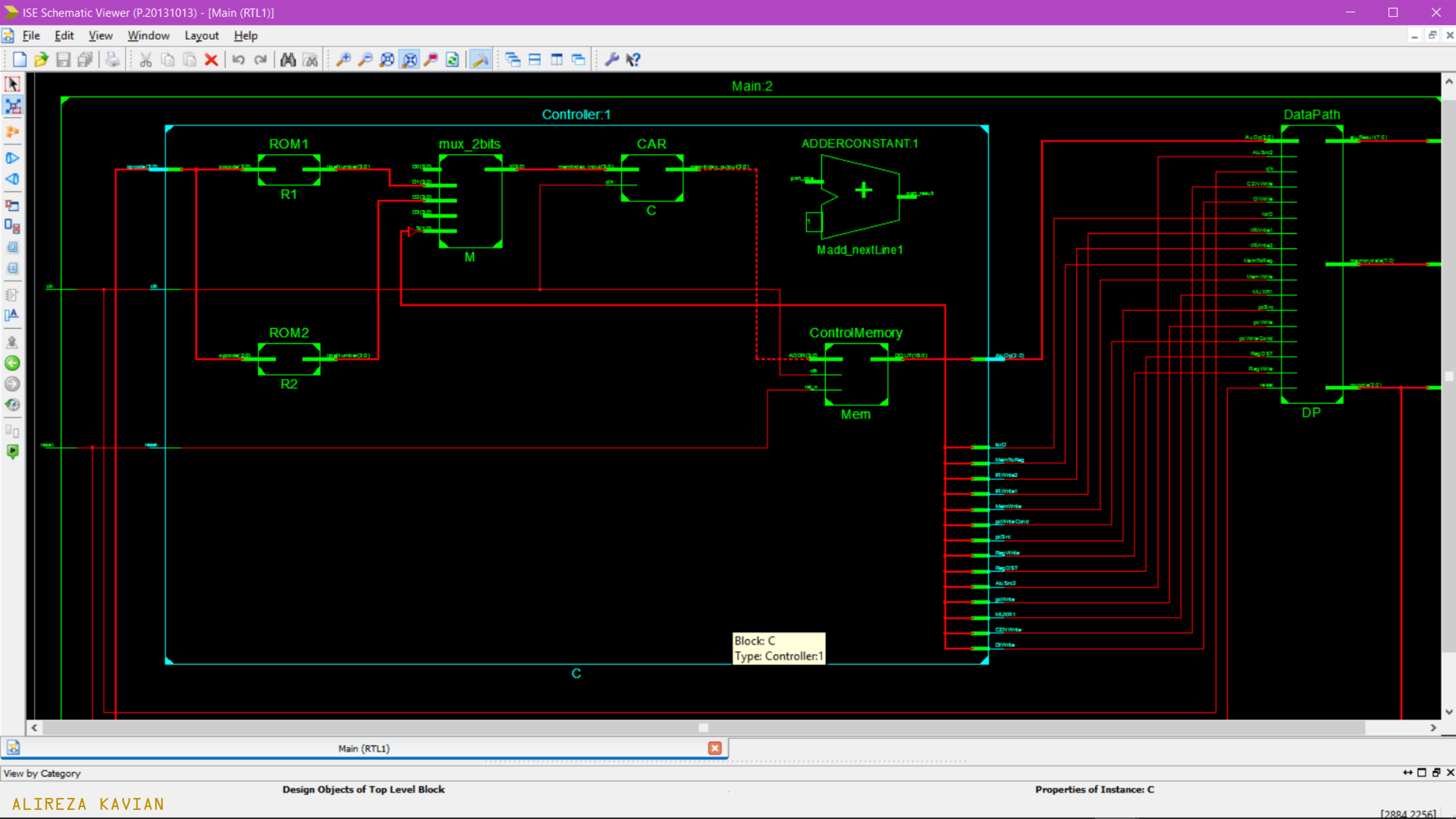
[2108,64]


ISE Schematic Viewer (P.20131013) - [Main (RTL1)]
File Edit View Window Layout Help
Main:2
Controller:1
ROM1
R1
mux_2bits
M
CAR
C
ADDERCONSTANT:1
Madd_nextLine1
ROM2
R2
ControlMemory
Mem
DataPath
DP
Block: C
Type: Controller:1
C
Main (RTL1)
View by Category
Design Objects of Top Level Block
Properties of Instance: C
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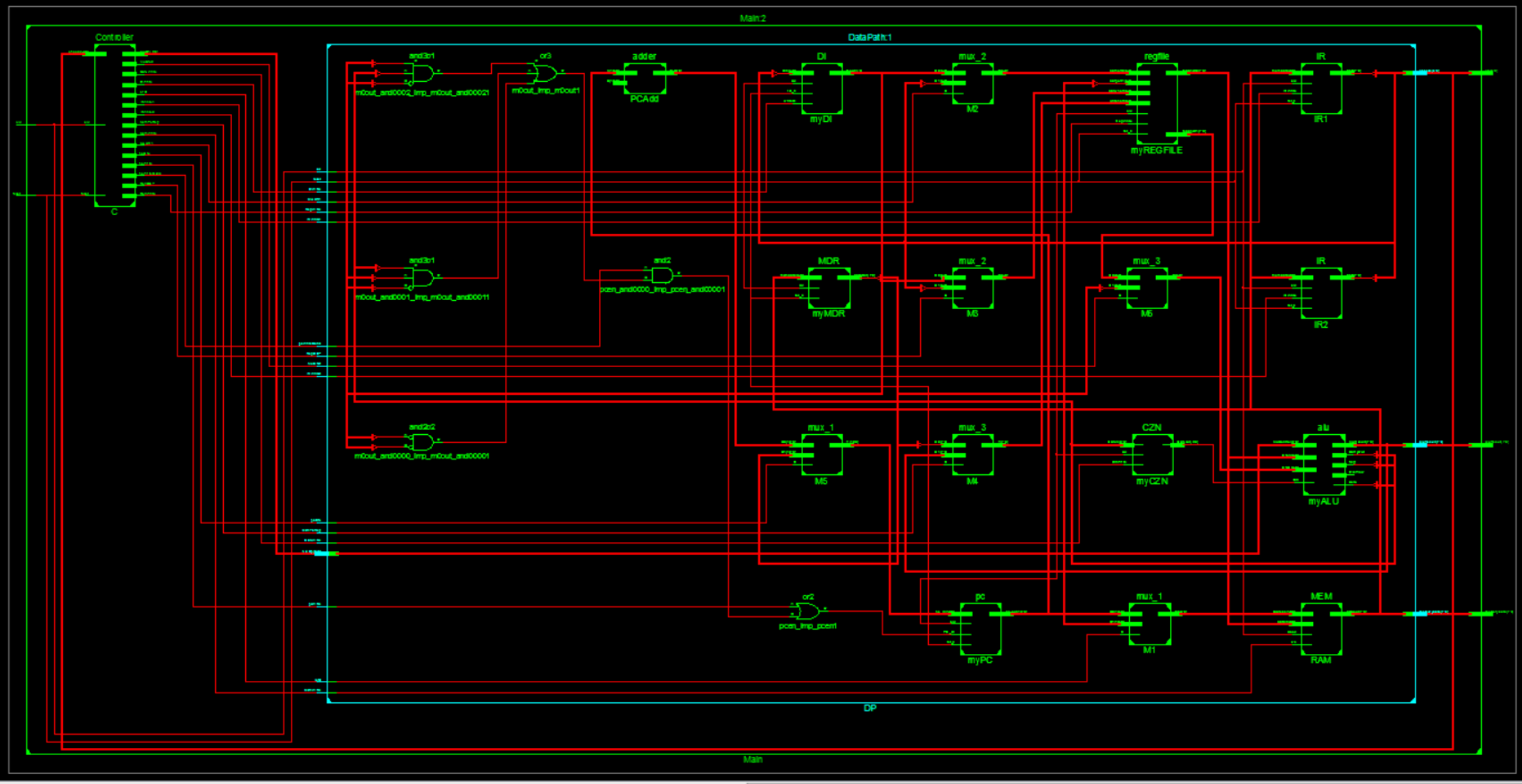
ISE Schematic Viewer (P.20131013) - [Main (RTL1)]

File Edit View Window Layout Help




Main (RTL1)

View by Category

Design Objects of Top Level Block

Properties of Instance: DP

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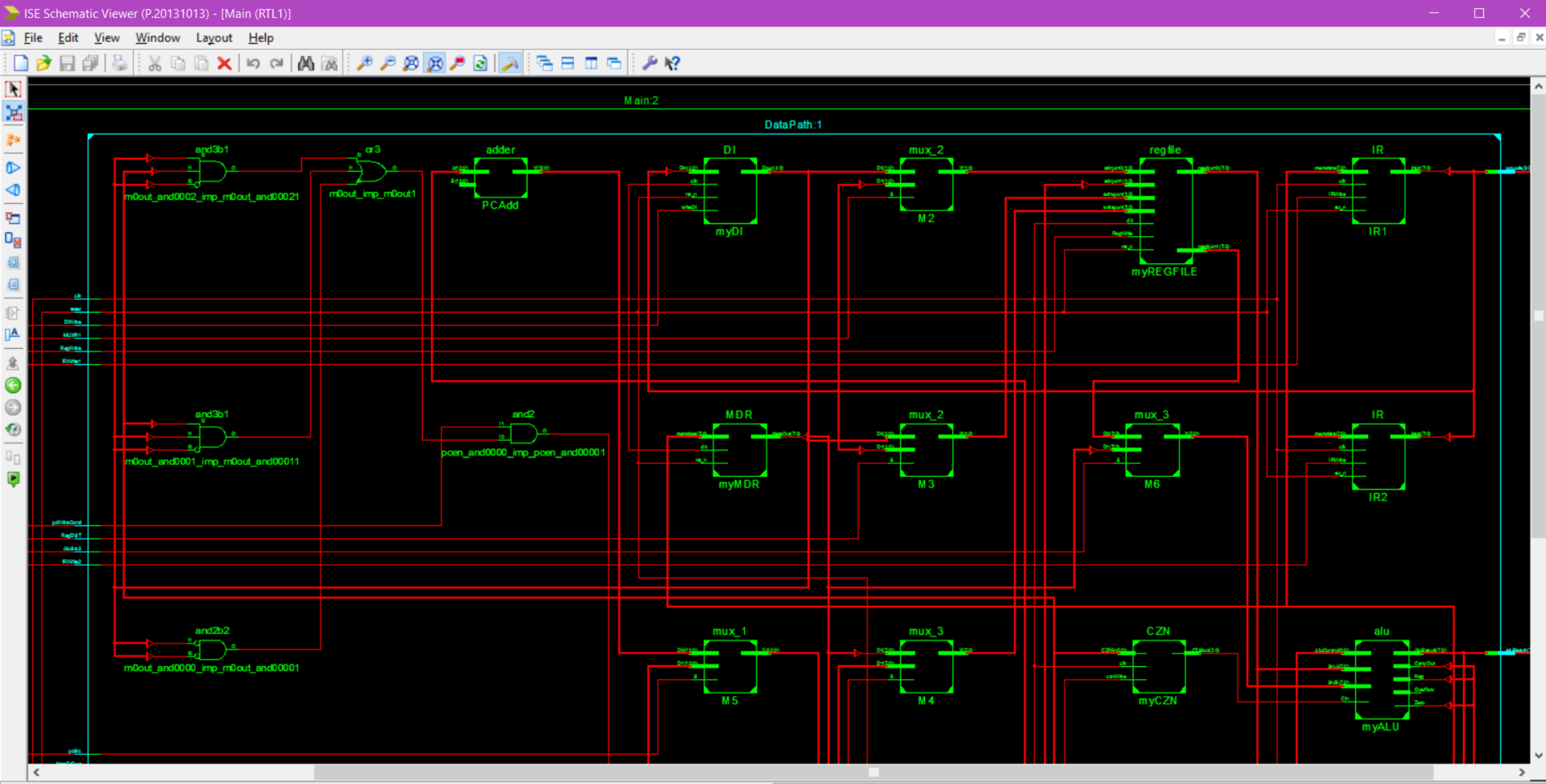
[9624 1948]


ISE Schematic Viewer (P.20131013) - [Main (RTL1)]
File Edit View Window Layout Help
Main:2
DataPath:1
and3b1
m0out_and0002_imp_m0out_and00021
or3
m0out_imp_m0out1
adder
PCAdd
DI
myDI
mux_2
M2
regfile
myREGFILE
IR
IR1
and3b1
m0out_and0001_imp_m0out_and00011
and2
pcen_and0000_imp_pcen_and00001
MDR
myMDR
mux_2
M3
mux_3
M6
IR
IR2
and2b2
m0out_and0000_imp_m0out_and00001
mux_1
M5
mux_3
M4
CZN
myCZN
alu
myALU
Main (RTL1)
View by Category
Design Objects of Top Level Block
Properties of Instance: DP
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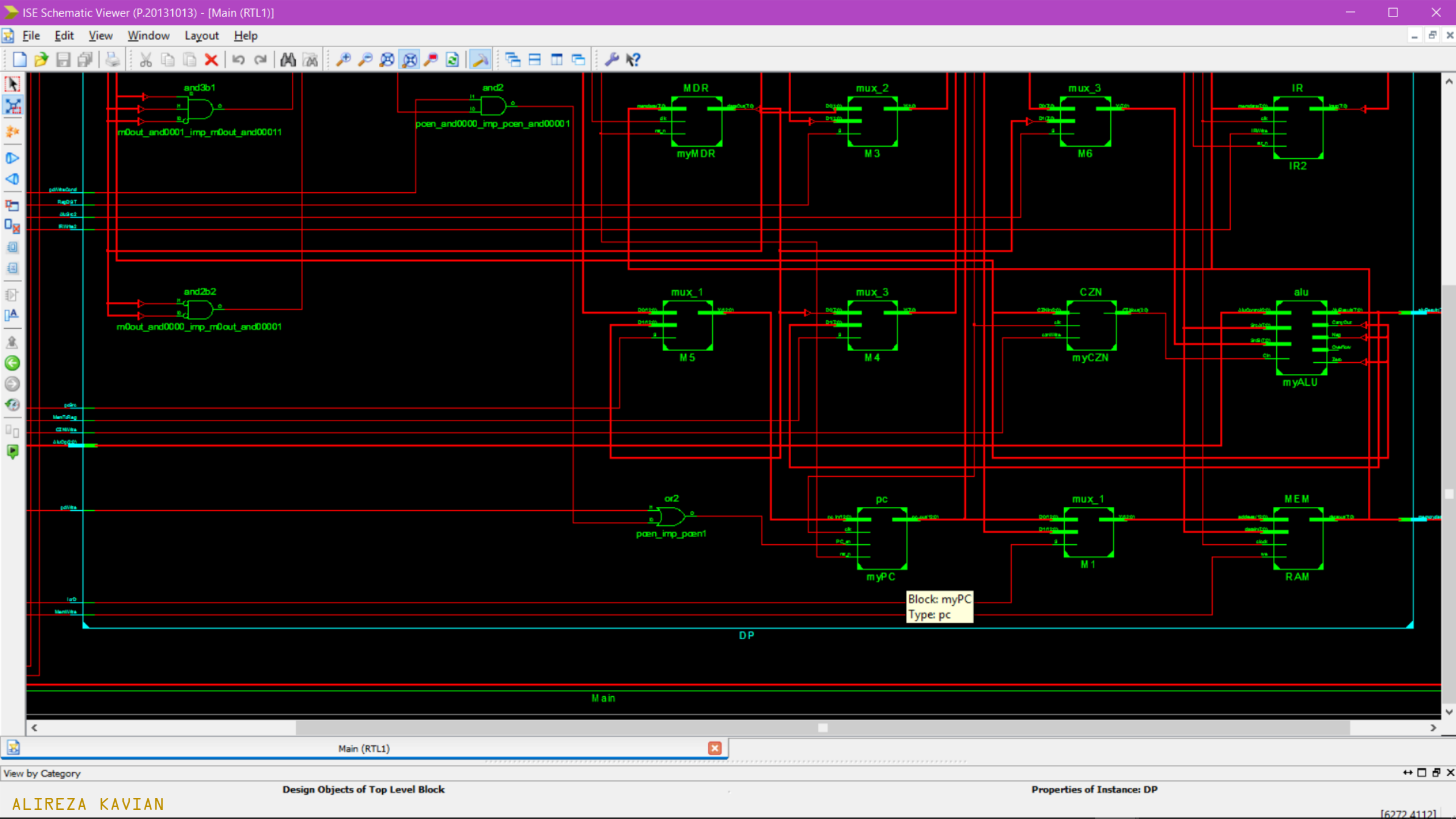
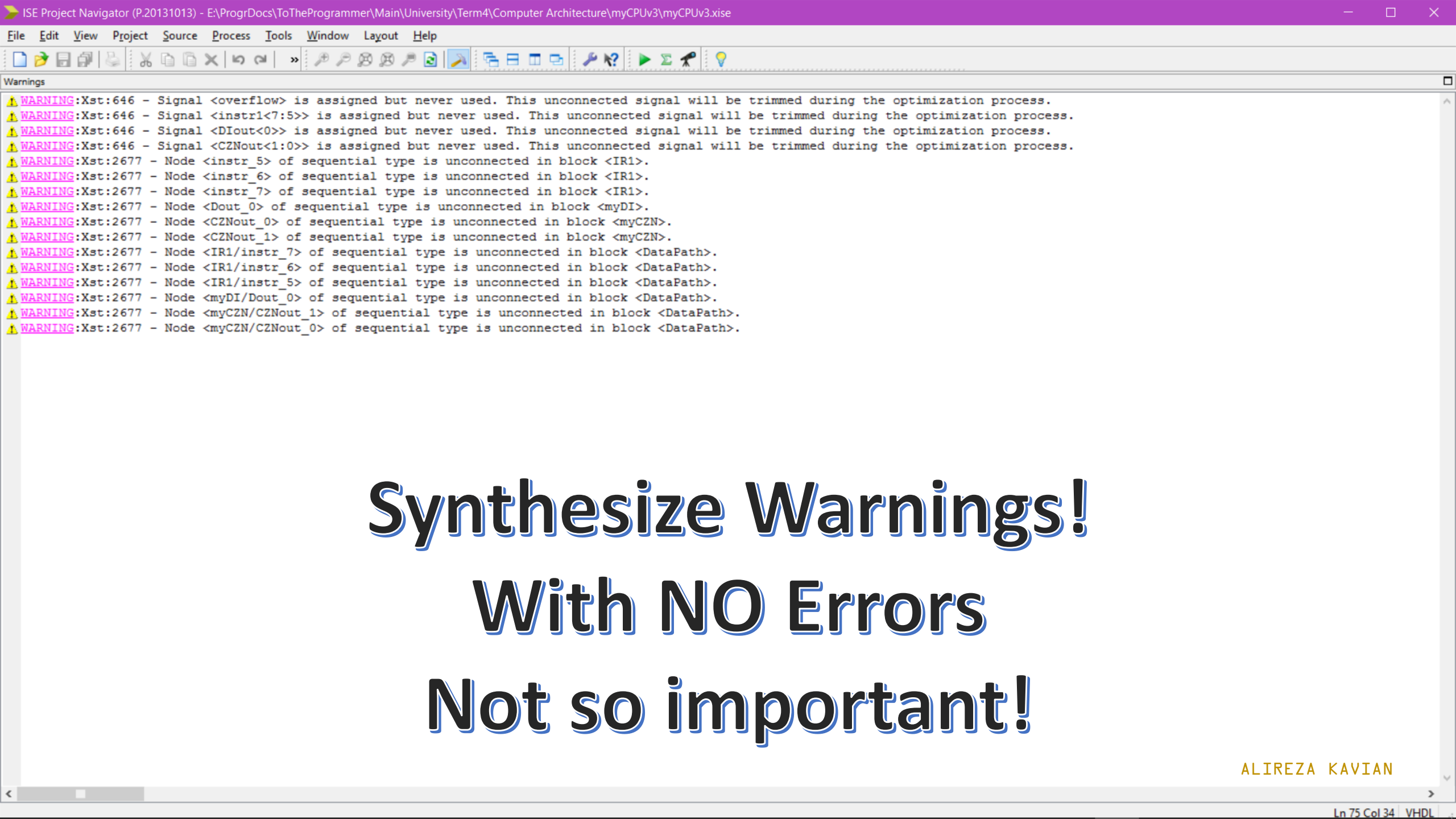

ISE Schematic Viewer (P.20131013) - [Main (RTL1)]
File
Edit
View
Window
Layout
Help
and3b1
m0out_and0001_imp_m0out_and00011
and2
pcen_and0000_imp_pcen_and00001
MDR
myMDR
mux_2
M3
mux_3
M6
IR
IR2
and2b2
m0out_and0000_imp_m0out_and00001
mux_1
M5
mux_3
M4
CZN
myCZN
alu
myALU
or2
pcen_imp_pcen1
pc
myPC
mux_1
M1
MEM
RAM
Block: myPC
Type: pc
DP
Main
Main (RTL1)
View by Category
Design Objects of Top Level Block
Properties of Instance: DP
ALIREZA KAVIAN


ISE Project Navigator (P.20131013) - E:\ProgrDocs\ToTheProgrammer\Main\University\Term4\Computer Architecture\myCPUv3\myCPUv3.xise
File Edit View Project Source Process Tools Window Layout Help
Warnings
WARNING:Xst:646 - Signal <overflow> is assigned but never used. This unconnected signal will be trimmed during the optimization process.
WARNING:Xst:646 - Signal <instr1<7:5>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.
WARNING:Xst:646 - Signal <DIout<0>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.
WARNING:Xst:646 - Signal <CZNout<1:0>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.
WARNING:Xst:2677 - Node <instr_5> of sequential type is unconnected in block <IR1>.
WARNING:Xst:2677 - Node <instr_6> of sequential type is unconnected in block <IR1>.
WARNING:Xst:2677 - Node <instr_7> of sequential type is unconnected in block <IR1>.
WARNING:Xst:2677 - Node <Dout_0> of sequential type is unconnected in block <myDI>.
WARNING:Xst:2677 - Node <CZNout_0> of sequential type is unconnected in block <myCZN>.
WARNING:Xst:2677 - Node <CZNout_1> of sequential type is unconnected in block <myCZN>.
WARNING:Xst:2677 - Node <IR1/instr_7> of sequential type is unconnected in block <DataPath>.
WARNING:Xst:2677 - Node <IR1/instr_6> of sequential type is unconnected in block <DataPath>.
WARNING:Xst:2677 - Node <IR1/instr_5> of sequential type is unconnected in block <DataPath>.
WARNING:Xst:2677 - Node <myDI/Dout_0> of sequential type is unconnected in block <DataPath>.
WARNING:Xst:2677 - Node <myCZN/CZNout_1> of sequential type is unconnected in block <DataPath>.
WARNING:Xst:2677 - Node <myCZN/CZNout_0> of sequential type is unconnected in block <DataPath>.
Synthesize Warnings!
With NO Errors
Not so important!
ALIREZA KAVIAN
Ln 75 Col 34 VHDL

در مرحله ی آخر ، یک تست بنچ نوشتم که درستی کارکرد ماژول هارو بررسی کنم!
ابتدا در موری اصلی با توجه نوع دستورات تعریف شده، چند instruction را به عنوان مقدار های اولیه ی چند خونه از موری تعریف کردم که هر کدام 8 بیت است! سپس با توجه به موج زمانی، مقادیر رجیستر ها و  موری را بررسی کردم که به درستی عمل میکرد..
اگر دستورات را در نظر بگیریم ، رجیستر شماره ی 3 (آخری) پس از چندی لود و استور شدن ، باید مقدار 9 (1001) را بگیرد؛ با trace کردن کد میتوان به درستی آن پی برد!

At the last stage, I wrote a testbench for hot module validation.
In the main memory, we initialized some instructions in some first rows in which each one is 8bits.
At last, I traced the wave form to validate the tasks.

#TestBench

#Waves

#memory

Initialization

```
38    signal ram : ram_type := (0 => "10000000", --(arithmetic opcode:4)(Acj:2)->(Aci:2); //overall 8bits
39                             1 => "10000100",
40                             2 => "10010100",
41                             3 => "10110100",
42                             4 => "10000011",
43                             5 => "11111000",
44
45                             6 => "00100000", --instr. STA (store addressed)
46                             7 => "00001111",
47
48                             8 => "01000000", --instr. ADA (add addressed)
49                             9 => "00001111",
50
51                             10 => "11000000", --instr. JMP ( here : jump to mem(8) )
52                             11 => "00001100",
53
54                             12 => "00001000", --for jumping to this address (here : pc[12:8]&"00001000")
55
56                             others => "10000000"
57                         );
```

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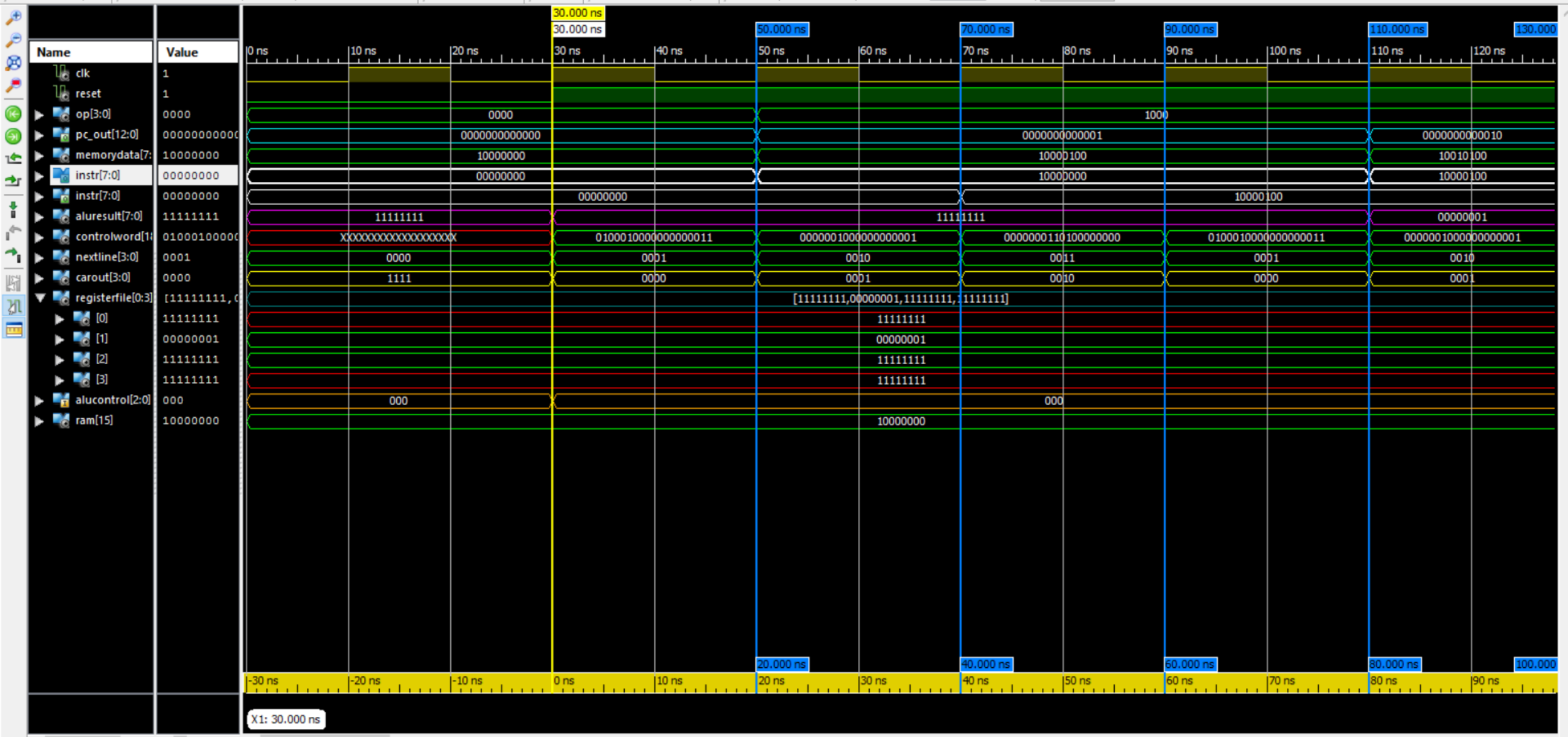
Float (P.20131013) - [wave1.wcfg*]

File Edit View Simulation Window Layout Help




wave1.wcfg*

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Sim Time: 1,000,000 ps

# For more information Contact with

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