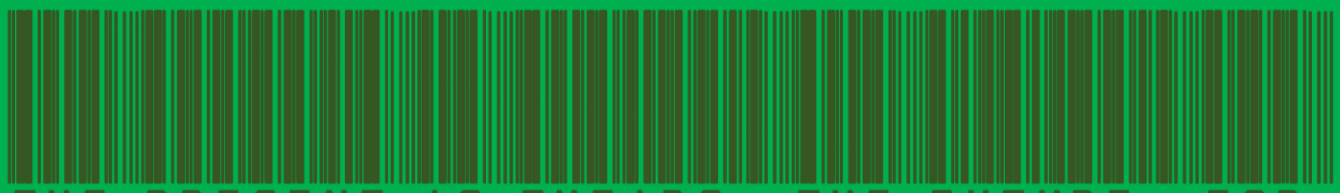
آزمایشگاه مدار منطقی

نویسنده:

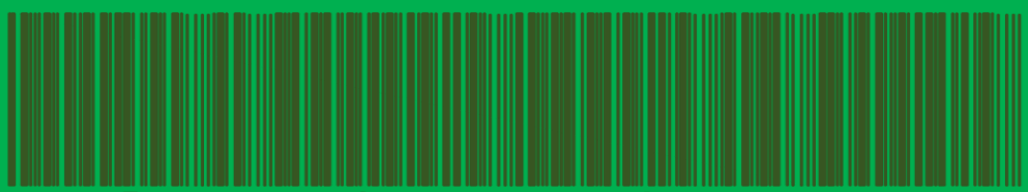
علیرضا طباطبائیان(9723052)

Amirkabir University of Technology
(Tehran Polytechnic)

استاد آزمایشگاه:
دکتر علیرضا
طاهری نوید

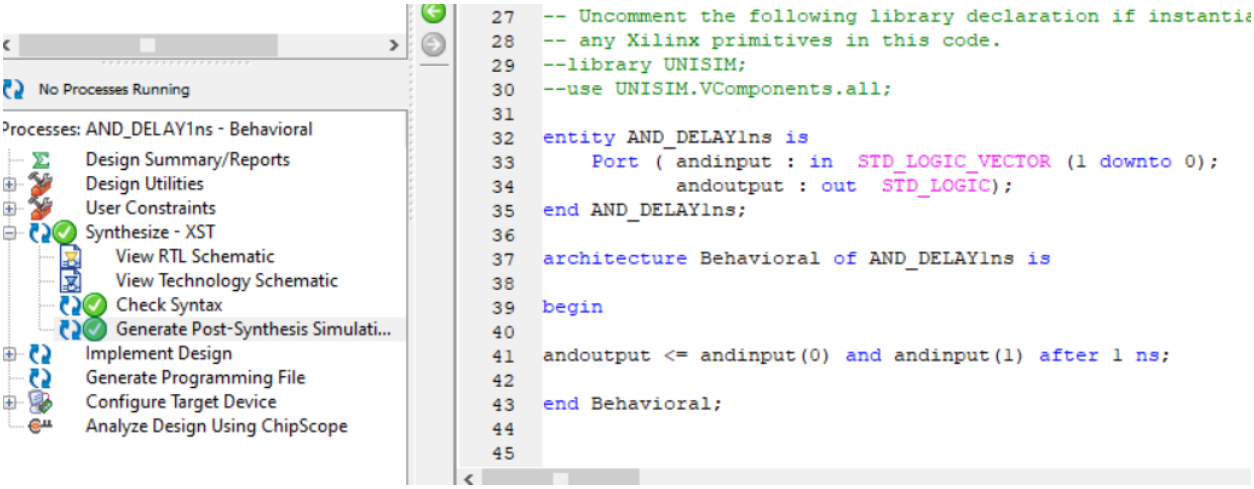


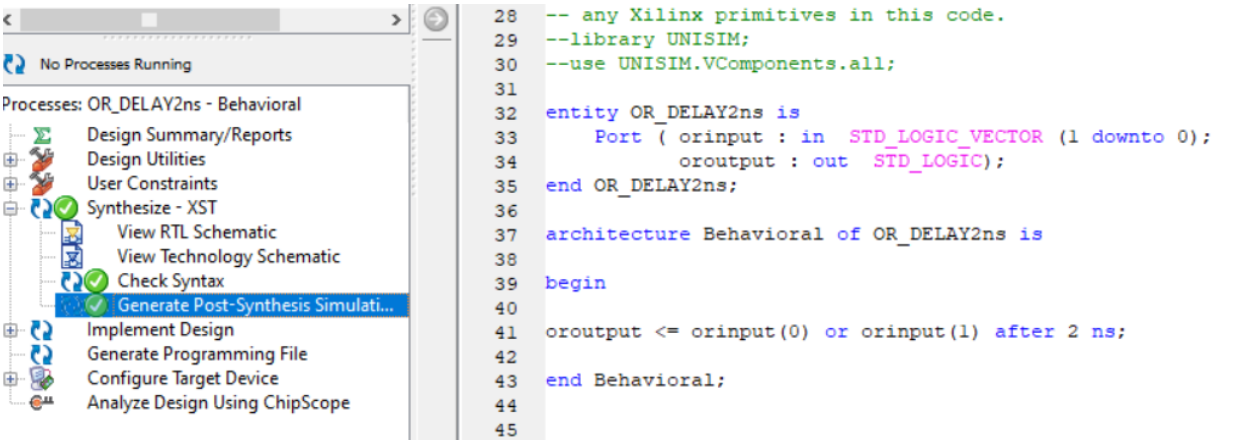
THE PRESENT IS THEIRS, THE FUTURE, FOR

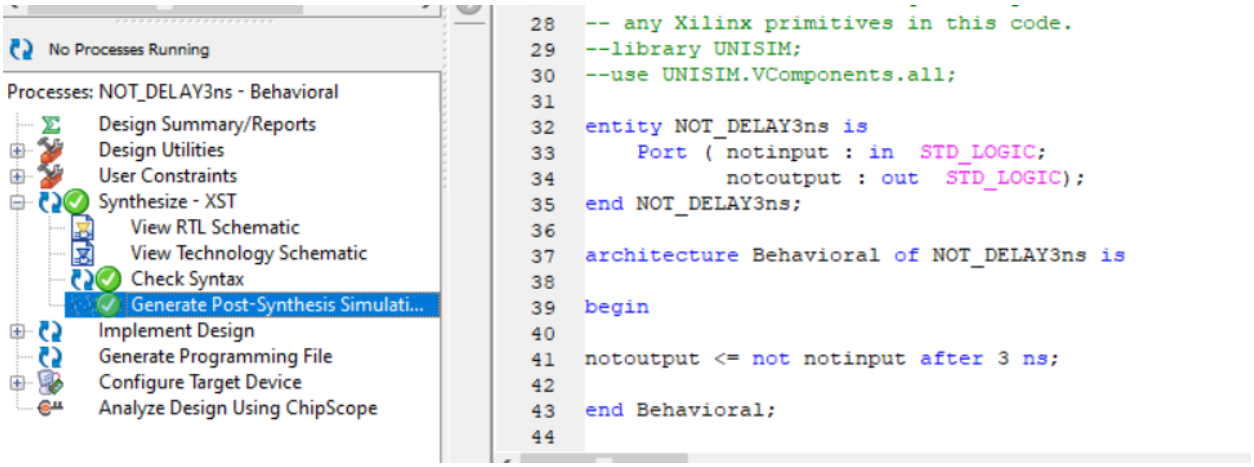


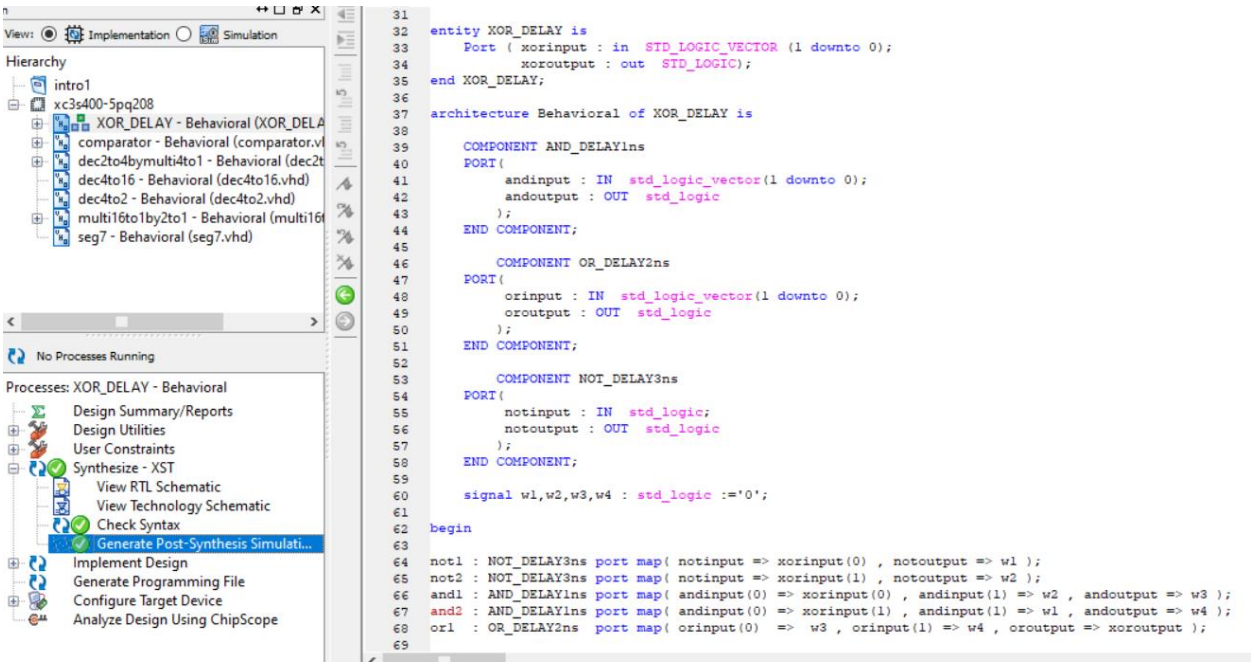
WHICH I REALLY WORK, IS MINE.

تمرین اول: ساخت گیت های AND OR NOT XOR بهمراه تاخیر:



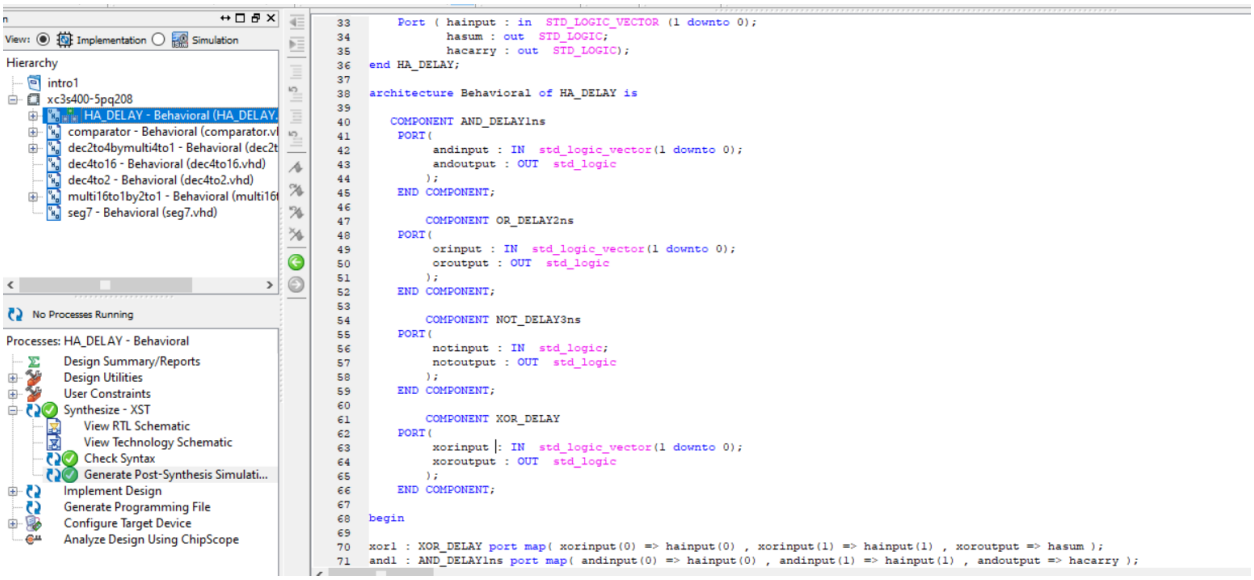


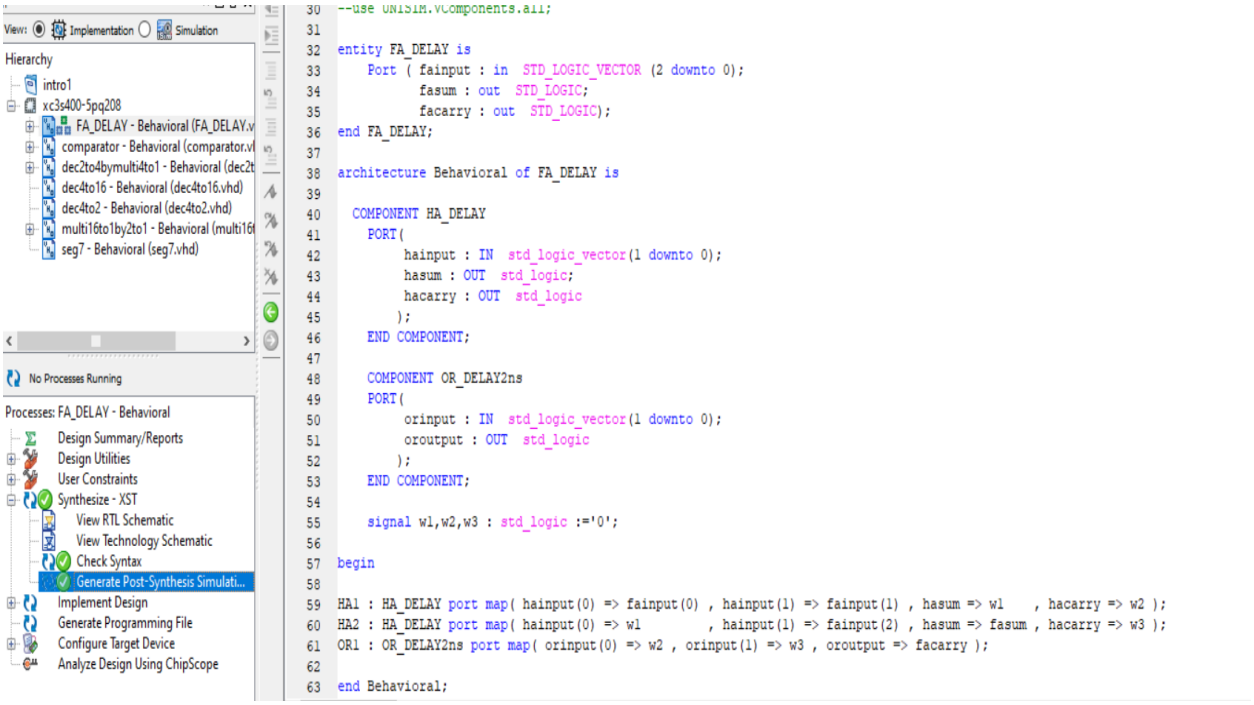




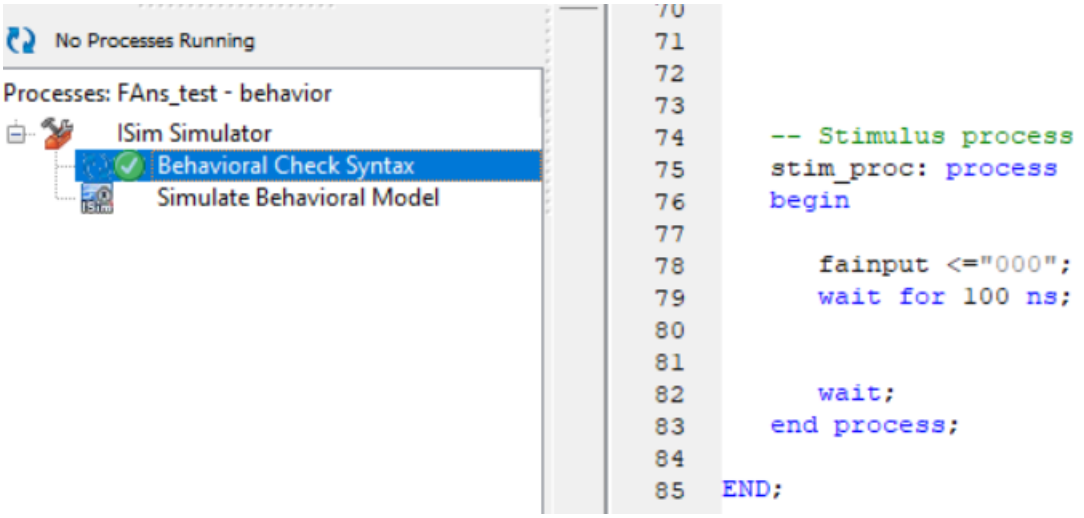
ساخت نیم جمع کننده و تمام جمع کننده با تاخیر:

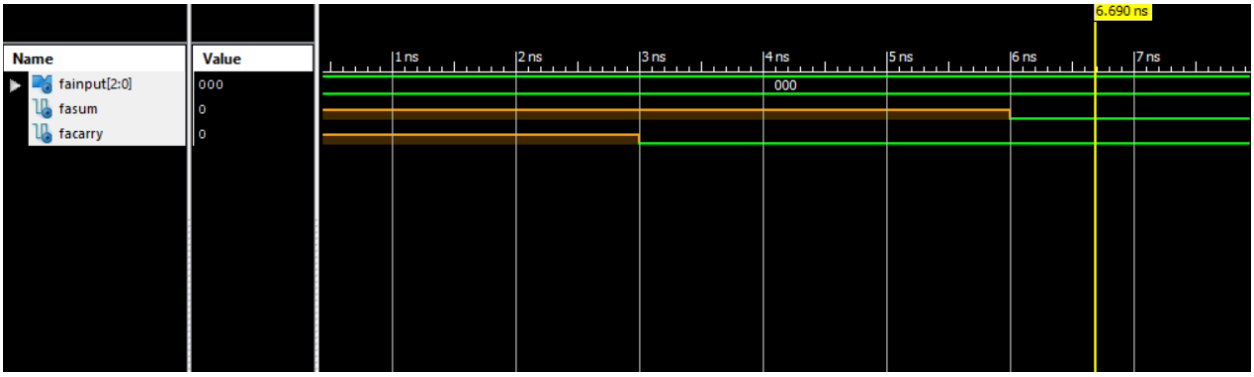
جداول کارنو و ... آن در تکلیف شماره 1 موجود میباشد.



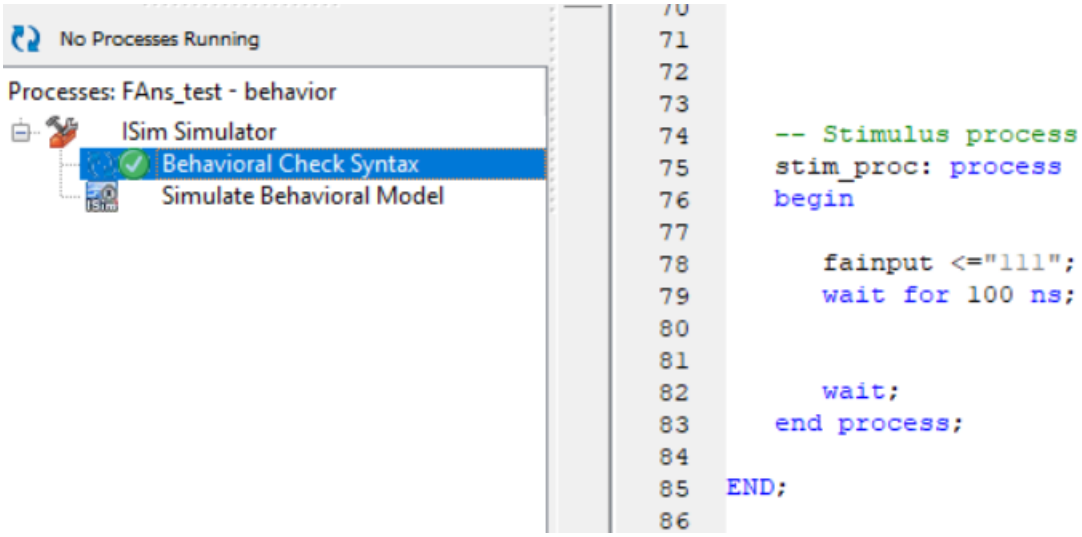


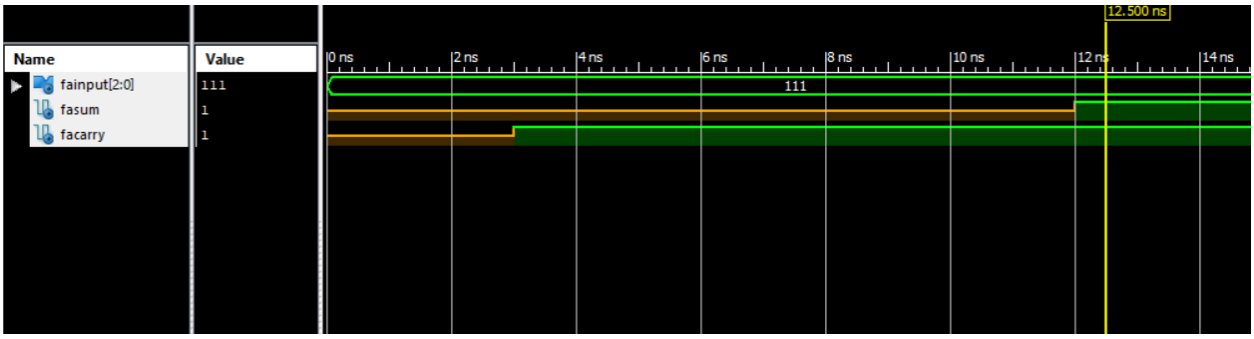
تست بنچ های FA برای ورودی 000 :





تست بنچ های FA برای ورودی 111 :

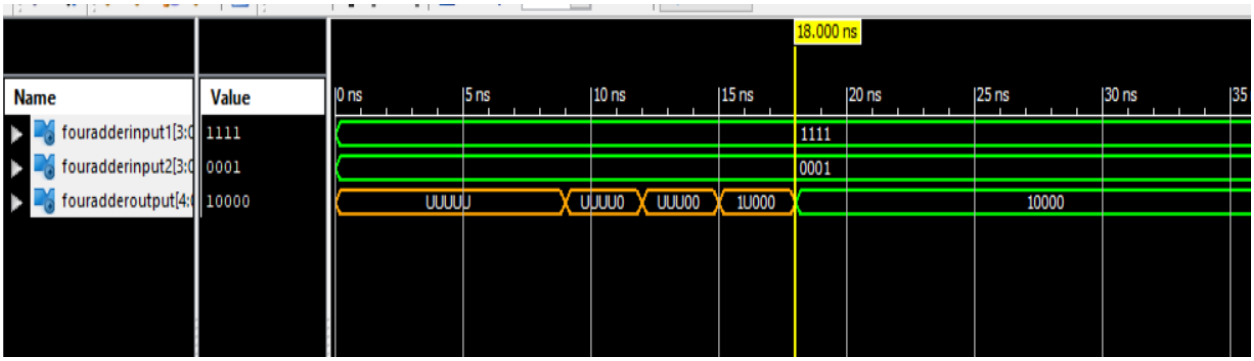


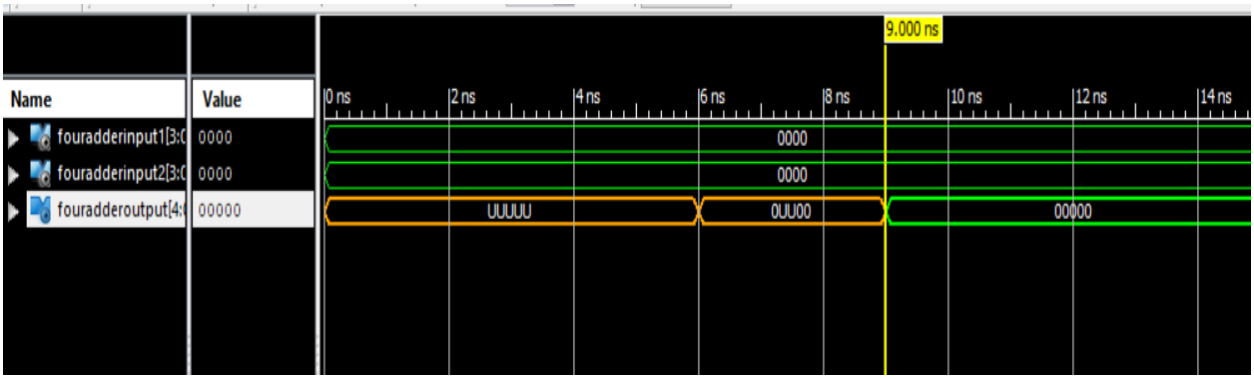


جمع کننده 4 بیتی:

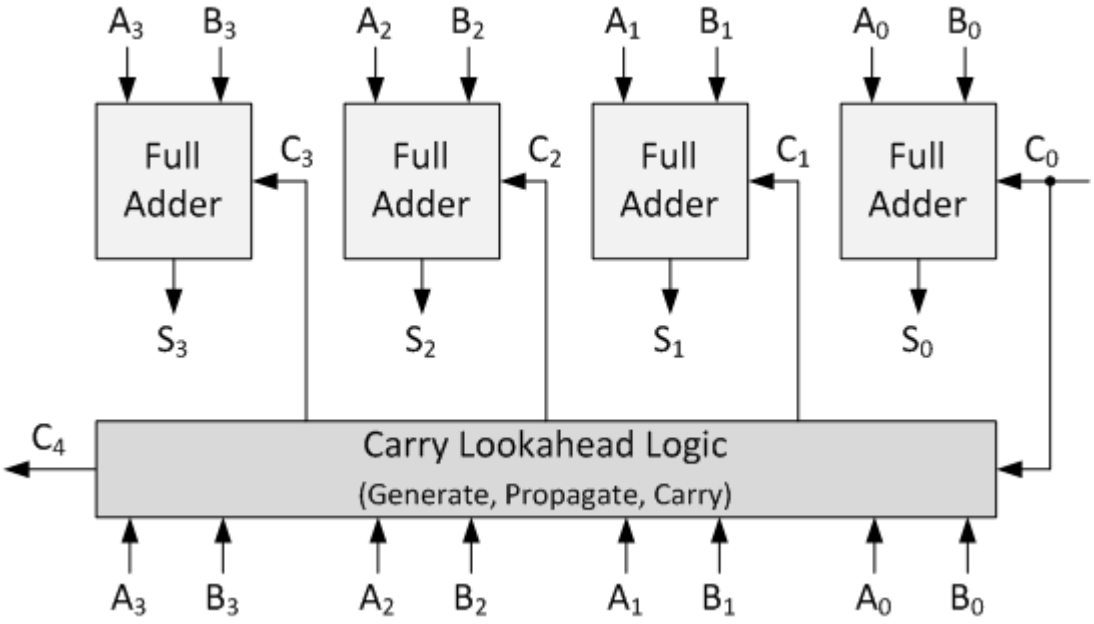
بیشترین تاخیر به ازای جمع 1111 با 0001 بود برابر 18 نانوثانیه و کمترین مربوط به جمع 0000 با 0000 بود برابر 9 نانو ثانیه.

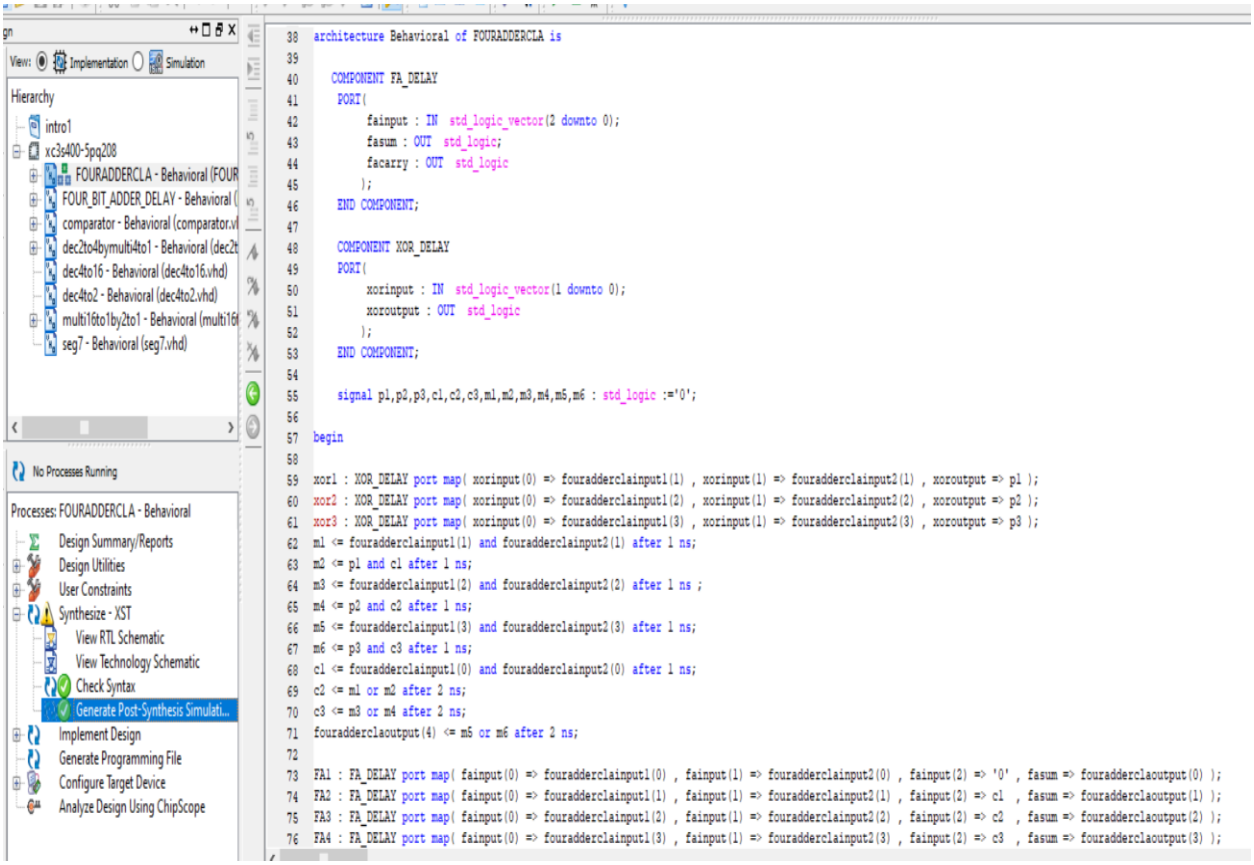
روش بدست آوردن: برای بیشترین، باید بیشترین تعداد بیت ها تغییر کند و برای کمترین باید کمترین تعداد بیت ها تغییر کند.





جمع کننده lookahead :





```
architecture Behavioral of FOURADDERCLA is

   COMPONENT FA_DELAY
    PORT(
         fainput : IN  std_logic_vector(2 downto 0);
         fasum : OUT  std_logic;
         facarry : OUT  std_logic
        );
   END COMPONENT;

   COMPONENT XOR_DELAY
   PORT(
        xorinput : IN  std_logic_vector(1 downto 0);
        xoroutput : OUT  std_logic
       );
   END COMPONENT;

   signal p1,p2,p3,c1,c2,c3,m1,m2,m3,m4,m5,m6 : std_logic :='0';

begin

xor1 : XOR_DELAY port map( xorinput(0) => fouradderclainput1(1) , xorinput(1) => fouradderclainput2(1) , xoroutput => p1 );
xor2 : XOR_DELAY port map( xorinput(0) => fouradderclainput1(2) , xorinput(1) => fouradderclainput2(2) , xoroutput => p2 );
xor3 : XOR_DELAY port map( xorinput(0) => fouradderclainput1(3) , xorinput(1) => fouradderclainput2(3) , xoroutput => p3 );
m1 <= fouradderclainput1(1) and fouradderclainput2(1) after 1 ns;
m2 <= p1 and c1 after 1 ns;
m3 <= fouradderclainput1(2) and fouradderclainput2(2) after 1 ns ;
m4 <= p2 and c2 after 1 ns;
m5 <= fouradderclainput1(3) and fouradderclainput2(3) after 1 ns;
m6 <= p3 and c3 after 1 ns;
c1 <= fouradderclainput1(0) and fouradderclainput2(0) after 1 ns;
c2 <= m1 or m2 after 2 ns;
c3 <= m3 or m4 after 2 ns;
fouradderclaoutput(4) <= m5 or m6 after 2 ns;

FA1 : FA_DELAY port map( fainput(0) => fouradderclainput1(0) , fainput(1) => fouradderclainput2(0) , fainput(2) => '0' , fasum => fouradderclaoutput(0) );
FA2 : FA_DELAY port map( fainput(0) => fouradderclainput1(1) , fainput(1) => fouradderclainput2(1) , fainput(2) => c1  , fasum => fouradderclaoutput(1) );
FA3 : FA_DELAY port map( fainput(0) => fouradderclainput1(2) , fainput(1) => fouradderclainput2(2) , fainput(2) => c2  , fasum => fouradderclaoutput(2) );
FA4 : FA_DELAY port map( fainput(0) => fouradderclainput1(3) , fainput(1) => fouradderclainput2(3) , fainput(2) => c3  , fasum => fouradderclaoutput(3) );
```

مقایسه تاخیر جمع 0000 با 0000 :

در قبلی 9 و در این یکی 6 نانو ثانیه است.

مقایسه تاخیر جمع 0001 با 1111 :

در قبلی 18 و در این یکی همچنان 18 نانو ثانیه است.