آنزعا يسكاه مداله منطقه

نو پسنده:

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Amirkabir University of Technology (Tehran Polytechnic)





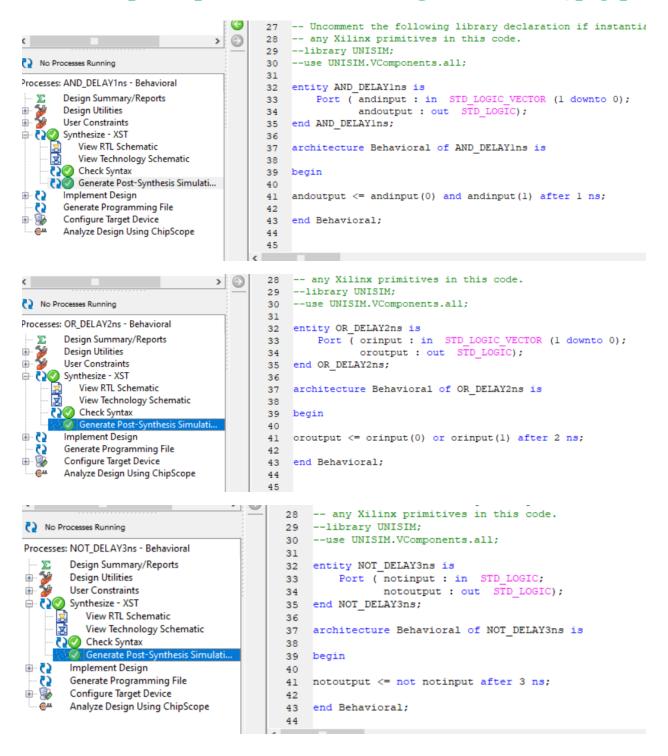


THE PRESENT IS THEIRS, THE FUTURE, FOR



REALLY WORK, IS MINE.

تمرین اول: ساخت گیت های AND OR NOT XOR بهمراه تاخیر:



```
entity XOR_DELAY is
   Port ( xorinput : in STD_LOGIC_VECTOR (1 downto 0);
        xoroutput : out STD_LOGIC);
                                                                               32
View: 

Implementation 

Simulation
                                                                                34
    intro1
                                                                                      end XOR_DELAY;
xc3s400-5pq208
        xc3s400-5pq208

AVOR_DELAY - Behavioral (XOR_DELAY - Behavioral)

comparator - Behavioral (comparator.v)

dec2to4bymulti4to1 - Behavioral (dec2tof dec4to16 - Behavioral (dec4to16.vhd)

dec4to2 - Behavioral (dec4to2.vhd)

multi16to1by2to1 - Behavioral (multi16tof by2to1 - Behavioral)

seg7 - Behavioral (seg7.vhd)
                                                                                      architecture Behavioral of XOR DELAY is
                                                                                37
                                                                                               COMPONENT AND_DELAYIns
                                                                                39
                                                                                40
                                                                                              PORT (
                                                                                                       andinput : IN std_logic_vector(1 downto 0);
andoutput : OUT std_logic
                                                                    1
                                                                                42
                                                                    %
                                                                                43
                                                                                             END COMPONENT;
                                                                    74
                                                                                45
                                                                    74
                                                                                46
47
                                                                                                     COMPONENT OR DELAY2ns
                                                                    (
                                                                                                      orinput : IN std_logic_vector(1 downto 0);
oroutput : OUT std_logic
                                                                                48
                                                                                             END COMPONENT;
                                                                                51
No Processes Running
                                                                                                     COMPONENT NOT_DELAY3ns
Processes: XOR DELAY - Behavioral
                                                                                54
                                                                                              PORT (
            Design Summary/Reports
                                                                                55
56
                                                                                                       notinput : IN std_logic;
notoutput : OUT std_logic
             Design Utilities
                                                                                57
             User Constraints
                                                                                              END COMPONENT;
Synthesize - XST
                                                                                59
                 View RTL Schematic
                                                                                              signal w1, w2, w3, w4 : std logic :='0';
                  View Technology Schematic
         Check Syntax
                                                                                62
                                                                                                   NOT_DELAY3ns port map( notinput => worinput(0) , notoutput => w1 );
NOT_DELAY3ns port map( notinput => worinput(1) , notoutput => w2 );
€5 €
             Implement Design
             Generate Programming File
                                                                                65
                                                                                       not2 :
                                                                                       and: AND_DELAYIns port map( andinput(0) => xorinput(0), andinput(1) => w2, andoutput => w3);
and: AND_DELAYIns port map( andinput(0) => xorinput(0), andinput(1) => w1, andoutput => w4);
or1: OR_DELAYIns port map( orinput(0) => w3, orinput(1) => w4, oroutput => xoroutput );
             Configure Target Device
             Analyze Design Using ChipScope
                                                                                68
```

ساخت نیم جمع کننده و تمام جمع کننده با تاخیر:

جداول کارنو و ... آن در تکلیف شماره 1 موجود میباشد.

```
↔ 🗆 🗗 ×
                                                                                                     View: 

Implementation 

Simulation
                                                                                                                  hacarry : out STD LOGIC);
    Hierarchy
                                                                                             end HA_DELAY;
                                                                                      36
    intro1

xc3s400-5pq208
         x <3s400-5pq208
x : HA_DELAY - Behavioral (HA_DELAY)
comparator - Behavioral (Behavioral (dec2to-1)
dec4to16 - Behavioral (dec4to16x/hd)
dec4to2 - Behavioral (dec4to2x/hd)
multiflot 1by2to1 - Behavioral (multiflot |
seg7 - Behavioral (seg7.whd)
                                                                                            architecture Behavioral of HA_DELAY is
                                                                                                  COMPONENT AND_DELAYIns
                                                                                                             andinput : IN std_logic_vector(1 downto 0);
andoutput : OUT std_logic
                                                                                                   END COMPONENT;
                                                                                                            COMPONENT OR DELAY2ns
                                                                                                             orinput : IN std_logic_vector(1 downto 0);
oroutput : OUT std_logic
                                                                          <u>G</u>
                                                                                                    END COMPONENT;
    No Processes Running
                                                                                                            COMPONENT NOT_DELAY3ns
Design .

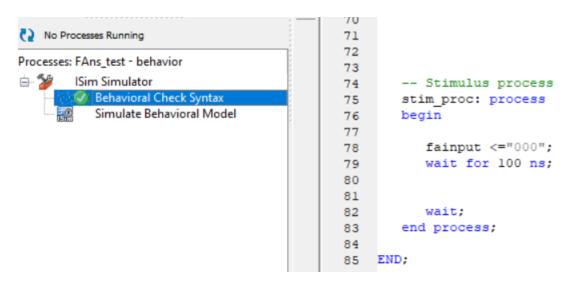
Design Utilitus.
User Constraints
View RTL Schematic
View RTL Schematic
View Technology Schematic
View Generate Post-Synthesis Simulati...
Implement Design
Annerate Programming File
"e Target Device
"Using ChipScope
    Processes: HA_DELAY - Behavioral
                                                                                                             notinput : IN std_logic;
notoutput : OUT std_logic
                                                                                                    );
END COMPONENT;
                                                                                                            COMPONENT XOR_DELAY
                                                                                                             to xorinput |: IN std_logic_vector(1 downto 0);
xoroutput : OUT std_logic
                                                                                                    END COMPONENT:
                                                                                             xor1 : XOR_DELAY port map( xorinput(0) => hainput(0) , xorinput(1) => hainput(1) , xoroutput => hasum );
and1 : AND_DELAYIns port map( andinput(0) => hainput(0) , andinput(1) => hainput(1) , andoutput => hacarry );
```

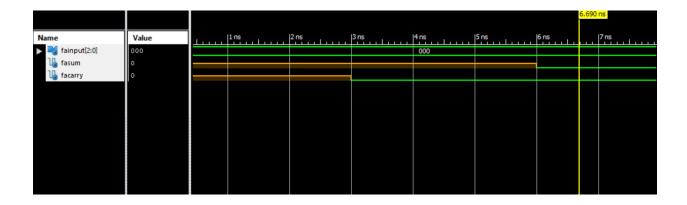
```
30 --use UNISIM.VComponents.aii;
View: 

Implementation 

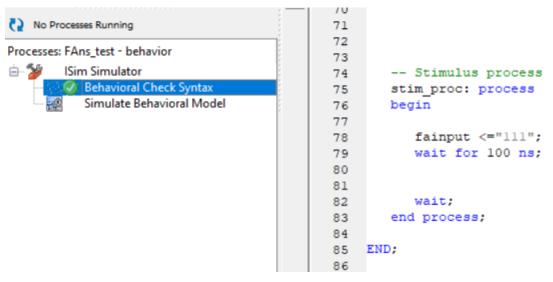
Simulation
                                                      31
                                                      32 entity FA_DELAY is
Hierarchy
                                                                 Port (fainput : in STD LOGIC VECTOR (2 downto 0);
                                                      33
 -- 🥘 intro1
                                                                          fasum : out STD LOGIC;
                                                      34
facarry : out STD LOGIC);
  x3400-5pq208
x3400-5pq208
comparator - Behavioral (FA_DELAY.)
dec2to4bymulti4to1 - Behavioral (dec2t)
dec4to16 - Behavioral (dec4to1.0hd)
dec4to2 - Behavioral (dec4to2.vhd)
multi16to1by2to1 - Behavioral (multi16)
seg7 - Behavioral (seg7.vhd)
                                                      35
                                                      36 end FA DELAY;
                                                      37
                                                      38 architecture Behavioral of FA_DELAY is
                                                      39
                                                              COMPONENT HA_DELAY
                                                      40
                                                      41
                                                                 PORT (
                                                      42
                                                                       hainput : IN std_logic_vector(1 downto 0);
                                                                      hasum : OUT std_logic;
hacarry : OUT std_logic
                                              *
                                                      43
                                                      44
                                              (
                                                      45
                                                                END COMPONENT;
                                              0
                                                      46
                                                      47
                                                                 COMPONENT OR DELAY2ns
No Processes Running
                                                      48
                                                      49
Processes: FA_DELAY - Behavioral
                                                                       orinput : IN std_logic_vector(1 downto 0);
                                                      50
       Design Summary/Reports
                                                      51
                                                                       oroutput : OUT std_logic
         Design Utilities
                                                      52
                                                                 END COMPONENT;
         User Constraints
                                                      53
Synthesize - XST
                                                      54
            View RTL Schematic
                                                      55
                                                                 signal w1,w2,w3 : std_logic :='0';
            View Technology Schematic
                                                      56
      Check Syntax
                                                      57 begin
                                                      58
                                                     59 HA1: HA_DELAY port map( hainput(0) => fainput(0) , hainput(1) => fainput(1) , hasum => wl , hacarry => w2 );
60 HA2: HA_DELAY port map( hainput(0) => wl , hainput(1) => fainput(2) , hasum => fasum , hacarry => w3 );
⊕ (3)
         Implement Design
         Generate Programming File
         Configure Target Device
                                                      61 OR1 : OR DELAY2ns port map ( orinput(0) => w2 , orinput(1) => w3 , oroutput => facarry );
         Analyze Design Using ChipScope
```

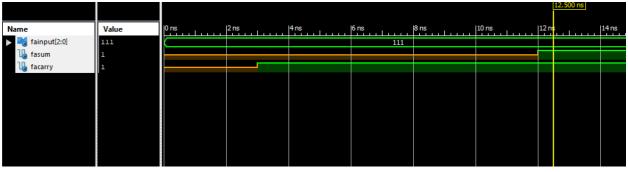
تست بنچ های FA برای ورودی 000:





تست بنچ های FA برای ورودی 111:





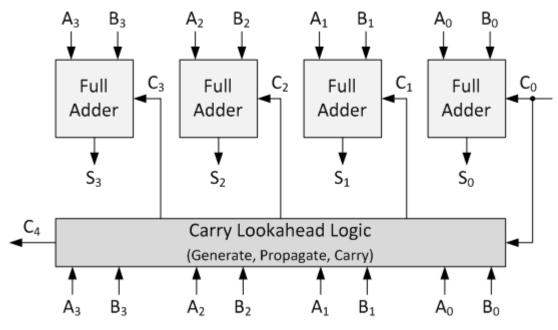
جمع كننده 4 بيتي:

بیشترین تاخیر به ازای جمع 1111 با 0001 بود برابر 18 نانوثانیه و کمترین مربوط به جمع 0000 با 0000 بود برابر 9 نانو ثانیه.

روش بدست آوردن: برای بیشترین، باید بیشترین تعداد بیت ها تغییر کند و برای کمترین باید کمترین تعداد بیت ها تغییر کند.



: lookahead



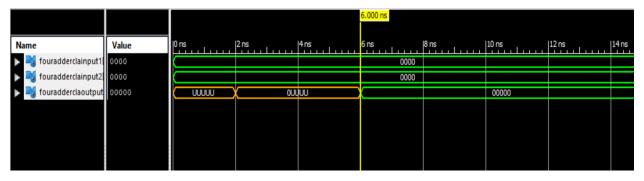
```
↔ 🛮 🗗 X
                                               38 architecture Behavioral of FOURADDERCLA is
39
                                                       COMPONENT FA DELAY
                                               40
Hierarchy
                                               41
                                                             fainput : IN std logic vector(2 downto 0);
   intro1
                                               42
                                                             fasum : OUT std_logic;
43
                                                             facarry : OUT std logic
                                               44
      FOURADDERCLA - Behavioral (FOUR
                                               45
     FOUR_BIT_ADDER_DELAY - Behavioral ( )
comparator - Behavioral (comparator.v)
                                                        END COMPONENT;
                                               46
                                               47

dec4to16 - Behavioral (dec4to16.vhd)
dec4to2 - Behavioral (dec4to2.vhd)

dec4to2 - Behavioral (dec4to2.vhd)
                                                        COMPONENT XOR_DELAY
                                               48
                                               49
                                                             xorinput : IN std_logic_vector(1 downto 0);
                                               50
     multi16to1by2to1 - Behavioral (multi16t  % seg7 - Behavioral (seg7.vhd)
                                                             xoroutput : OUT std logic
                                               51
                                               52
                                                        END COMPONENT;
                                               53
                                               54
                                                        signal p1,p2,p3,c1,c2,c3,m1,m2,m3,m4,m5,m6 : std_logic :="0";
                                               55
                                               56
                                     > 0
                                               57 begin
No Processes Running
                                               59 xorl : XOR_DELAY port map( xorinput(0) => fouradderclainput1(1) , xorinput(1) => fouradderclainput2(1) , xoroutput => pl );
                                               60 xor2 : NOR DELAY port map( xorinput(0) => fouradderclainput1(2) , xorinput(1) => fouradderclainput2(2) , xoroutput => p2 );
Processes: FOURADDERCLA - Behavioral
                                               61 xor3 : XOR DELAY port map( xorinput(0) => fouradderclainput1(3) , xorinput(1) => fouradderclainput2(3) , xoroutput => p3 );
 Design Summary/Reports
                                               62 ml <= fouradderclainput1(1) and fouradderclainput2(1) after 1 ns;
       Design Utilities
                                               63 m2 <= pl and cl after 1 ns;
                                               64 m3 <= fouradderclainput1(2) and fouradderclainput2(2) after 1 ns;
       User Constraints
                                               65 m4 <= p2 and c2 after 1 ns;
⊕ 🔃 Synthesize - XST
                                               66 m5 <= fouradderclainput1(3) and fouradderclainput2(3) after 1 ns;
           View RTL Schematic
                                               67 m6 <= p3 and c3 after 1 ns;
           View Technology Schematic
                                               68 cl <= fouradderclainputl(0) and fouradderclainput2(0) after 1 ns;
      Check Syntax
                                               69 c2 <= ml or m2 after 2 ns;
                                                70 c3 <= m3 or m4 after 2 ns;
⊕ 🚺 Implement Design
                                               71 fouradderclaoutput(4) <= m5 or m6 after 2 ns;
       Generate Programming File
                                                73 FAL: FA_DELAY port map( fainput(0) => fouradderclainputl(0) , fainput(1) => fouradderclainput2(0) , fainput(2) => '0' , fasum => fouradderclainput1(0) );
       Configure Target Device
                                               74 FA2: FA_DELAY port map( fainput(0) => fouradderclainput(1) , fainput(1) => fouradderclainput2(1) , fainput(2) => cl , fasum => fouradderclainput1(1) );
        Analyze Design Using ChipScope
                                                75 FA3 : FA_DELAY port map( fainput(0) => fouradderclainput(2) , fainput(1) => fouradderclainput2(2) , fainput(2) => c2 , fasum => fouradderclainput2(2) );
                                                76 FA4 : FA DELAY port map( fainput(0) => fouradderclainput(3) , fainput(1) => fouradderclainput2(3) , fainput(2) => c3 , fasum => fouradderclainput2(3) );
```

مقايسه تاخير جمع 0000 با 0000:

در قبلی 9 و در این یکی 6 نانو ثانیه است.



مقايسه تاخير جمع 0001 با 1111:

در قبلی 18 و در این یکی همچنان 18 نانو ثانیه است.

