

Alireza Zakeri

EMBEDDED SYSTEM DEVELOPER ENGINEER · HARDWARE DESIGNER ON FPGAS

Antwerpen, Belgium

☎ +32472897157 | ✉ Alireza_zak@yahoo.com | 🌐 Alireza Zakeri

Summary

Experienced FPGA and Embedded Systems Developer with over 8 years of hands-on expertise in HDL design targeting both Intel and Xilinx FPGAs and SoCs. Skilled in customizing and optimizing Linux-based and real-time embedded systems, with a strong background in microcontroller programming and a broad familiarity with both low- and high-speed communication protocols. A collaborative team player with a passion for solving complex engineering challenges, continuously seeking to improve solutions and adapt to new technologies and tools as needed.

Skills

Hardware Development

- Proficient in RTL design with VHDL and SystemVerilog targeting Xilinx and Intel FPGA platforms.
- Skilled at identifying and resolving common HDL design issues such as timing violations and lint errors.
- Proficient in addressing debugging, testing, simulation, and board bring-up challenges throughout the HDL design and deployment process.
- Familiar with Analog Devices ADCs, STM32, and Atmel microcontrollers and their peripherals configuration (UART, I2C, SPI, and etc).

System Development

- Development and customization of Linux kernel, U-Boot, RTOS and firmware on Xilinx and TI SoCs (Zynq, ZynqMP, Keystone I&I and Sitara).
- Familiar with Linux devicetree structure and development driver in kernel.
- Experienced with the Yocto Project build system, rootfs customization, and Jenkins CI/CD pipeline.
- Had a study on network concepts and protocols such as TCP/IP.

Softwares

- C, VHDL, SystemVerilog, MATLAB, Yocto Project, OpenCL, Git, crosstool-NG
- Familiar with C++, OOP, Python, SQLite, CMake, UVM, Xen hypervisor

Personal Skills

- Punctuality, Teamwork, Flexibility, and Adaptability
- Skilled in Agile methodologies with hands-on use of JIRA, Confluence, Bitbucket, and GitLab for project management and version control

Languages

- Persian (native), English (fluent)

Experience

Dekimo Experts Gent

CONSULTANT (FULL-TIME)

Gent, Belgium

July 2023 – Present

Sony Depthsensing Solutions (SDS)

EXPERT RTL DESIGNER (FULL-TIME)

Brussels, Belgium

January 2025 – July 2025

- Developed and optimized a complete controller system based on the Nios II processor on Intel FPGAs with a wide variety of peripherals (SD card reader, DDR4, I2C, UART, etc)

CarUX

EXPERT RTL DESIGNER (FULL-TIME)

Heerlen, Netherlands

July 2023 – November 2024

- Developed and optimized a complete controller system based on the Nios II processor on Intel FPGAs with a wide variety of peripherals (SD card reader, DDR4, I2C, UART, etc)
- Developed a video stream generator system based on DisplayPort on Intel FPGAs using Multi-Stream Transport (MST) for transmission of high-resolution video streams.
- Implemented a video stream transmitter based on DisplayPort with Display Stream Compression (DSC), live compressor, and playback pre-compressed image loader for high resolution images.

Sina Innovative Communication Systems

Tehran, Iran

EXPERT EMBEDDED FIRMWARE DEVELOPER (FULL-TIME)

May 2021 – June 2023

- Restored interfaces based on Command Line Interface (CLI) and SNMP protocols for optical network systems (as a team member refactor most of cisco 4120 commands on the company's new product).
- Developed, maintained, and debugged framing, mapping, and multiplexing codes of optical framer chips and modules (as a team member in charge of development and maintenance in the new kernel version).
- Implemented and modified FPGA codes on optical telecommunication cards.
- Developed Linux drivers and apps for boards with the Yocto project and Jenkins pipeline.
- Handled project management with Scrum methodology, Jira, and Redmine platforms.

Simorgh Intelligent Sky

Tehran, Iran

PROJECT CONSULTANT AND EXPERT EMBEDDED SYSTEM DEVELOPER (PART-TIME)

September 2020 – March 2023

- Designed GPS and GLONASS acquisition and tracking algorithms on Zynq7020 based on freeRTOS and Max2769. All codes were done both in PL and PS parts (25s sweep 32 satellites with 82 frequency bins).
- Implemented and tested anti-jamming technique for GPS on Zynq7020 based on embedded Linux, AD9361, LTC2174, and NT1065 in PL and PS parts (with four antennas, each lane 800Mbps rate).
- Optimized mentioned algorithms in MATLAB by cooperation with the system designer to achieve the optimal solution, to implement on PL and PS parts of Zynq.

Yasin Engineering developers Co

Tehran, Iran

MIDLEVEL EMBEDDED FIRMWARE AND HARDWARE DEVELOPER (FULL-TIME)

September 2017 – May 2021

- Upgraded SATA2 to SATA3 HDL code based on 7 series Xilinx FPGAs with 470MB/s write rate.
- Developed SRIO (4x6Gb/s) and EMIF (16x200Mb/s) link between K2H and XCKU115 based on RTOS.
- Developed a 10G link on ZynqMP based on VPX protocols with almost 8Gb/s data rate.
- Customized and configured embedded Linux for designed boards based on ZynqMP and K2H.
- Customized and Enabled Linux drivers based on the device tree: KSZ9893 and Si5341.
- Enabled si5341 configuration code on ZynqMP FSBL to solve Highspeed IPs' clock demands in PL.
- Optimized and tested algorithms (MUSIC) on K2H by OpenCL (CBLAS and LAPACK libs).
- Configured ADC ICs by STM32 and Atmel microcontrollers (AD9680).

Projects

Other projects:

- Implemented HDL codes of configuration and transferred data from ADC to PC by TCP protocol based on FPGA.
- Designed a target detector radar simulator on MATLAB GUI based on Adaptive Pulse Compression Algorithms.
- Optimized and implemented some Adaptive Pulse Compression (APC) algorithms on MATLAB and FPGAs (using Vivado HLS).
- Tutored a workshop on "Hands-on TI keystone II processors" in Iran Electronics Industries (Introduction of ProcessorSDKs, config, modify and compile of the kernel, U-boot, drivers and kernel modules, examples about OpenCL, OpenMP, Cblas and LAPACK, Some topics about TI-RTOS).
- Created a TCP network between 13 client boards and two server boards with STM32H750 microcontrollers (With STM32CubeIDE and Keil IDE). A computer program was designed as a client with LabVIEW that sent configuration board data to the config server. Alarms were sent to the other server.

Education

Iran University of Science and Technology

Iran, Tehran

MASTER OF SCIENCE IN ELECTRONIC ENGINEERING

September 2012 – March 2015

- Master's thesis: An integrated ultra-wideband low-phase noise oscillator circuit design – GPA: 18.30/20.00

Shahid Beheshti University

Iran, Tehran

BACHELOR OF SCIENCE IN TELECOMMUNICATION ENGINEERING

September 2007 – September 2012

- Bachelor's thesis: Power management module design based on GSM network – GPA: 15.39/20.00

Sony Depthsensing Solutions
Rue Jules Cockx 8
1160 Brussels

Brussels, 10 July 2025

Recommendation for Alireza

It is my pleasure to endorse Alireza for any future career opportunities that come his way. Throughout 7 months of collaboration at Sony Depthsensing Solutions (IC Design Center) on a SERDES project, Alireza impressed me with his strong foundational knowledge in digital design and his ability to quickly learn and adapt to new challenges.

Alireza's initiative and autonomy were evident as he tackled the complexities of RTL design in SystemVerilog using UVM methodology. He embraced the learning curve associated with the MIPI standard and effectively applied his newfound knowledge to our project. His positive attitude and willingness to listen to feedback ensured that the final results consistently met our high standards.

Moreover, Alireza is an excellent team player who balances collaboration with independent work. His skills extend beyond design; he is also adept at writing clear and comprehensive documentation, which greatly benefits the entire team.

I am confident that Alireza will excel in any future role he pursues. If you have any questions or would like further insights into his capabilities, please do not hesitate to contact me at arnaud.withoeck@sony.com.

Best regards,

Arnaud Withoeck
Digital Design & Verification Engineer
Sony Depthsensing Solutions



Bart Peters

Principal Engineer Electronics / Teamlead FPGA

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November 13th 2024

Letter of Recommendation about Alireza Zakeri

Dear Mr. Mrs,

I am delighted to recommend Alireza for any professional opportunity. In my role as team lead at Carux, in the driving electronics department. I have had the privilege of working closely with Alireza for a period about 16 months. I am confident in his exceptional abilities and dedication, fulfilling the required capabilities as our FPGA specialist hired from the Dekimo Company.

Alireza consistently showcased a remarkable aptitude for FPGA and IP implementation skills, contributing significantly to our Ghidorah project. Notably, his proficiency in HDL, IP's and general coding has been instrumental in achieving key milestones, exemplified by turning our IP implementations into a workable solution with our Ghidorah video platform project with an ARRIA 10 GX target device.

What sets Alireza apart is his exceptional ability to see complex structures, including effective communication, teamwork, and problem-solving. Alireza brings a proactive approach and resilience to challenging situations, making him an invaluable asset to our organization.

Beyond technical competencies, Alireza is known for his good overview in handling complex IP's and HDL structures including Nios cores. Alireza maintains a positive and group working attitude, but also able to work independently and find his way in the engineering environment or communicate across engineering teams outside the company.

I am confident that Alireza will bring the same dedication, knowledge and problem solving skills to any endeavor employer. Alireza has my recommendation, and if I was able to extend his hire period in our company I wouldn't doubt about extending his contract. But due to organizational headcount restrictions I must let him go.

Should you have any inquiries, please contact me at bart.peters@carux.com. I am more than willing to provide additional insights into Alireza's qualifications and capabilities.

Regards, Bart