Alireza Zakeri

Embedded System Developer Engineer · Hardware Designer on FPGAs

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Summary

Qualified FPGA developer engineer with 5+ years of experience in HDL circuit design based on Xilinx FPGAs and SoCs, also experienced in customizing in Linux-based and real-time processor-based systems. Familiar with the wide range of low-rate and high-rate protocols, processors, and microcontroller programming. Eager to collaborate and work in a team, interested in devising a better problem-solving method for challenging tasks, and learning new technologies and tools if the need arises.

Skills

Hardware Development	Expert on hardware development by VHDL on Xilinx FPGAs (7 series and Ultra Scale). Familiar with HDL design challenges such as timing faults and resolve.. Had experiences in debugging and test challenges in HDL designs. Familiar with Analog Devices ADCs, STM32, and Atmel microcontrollers and their peripherals configuration (UART, I2C, SPI, and etc).
System Development	Development and customization of Linux kernel, U-Boot, RTOS and firmware on Xilinx and TI SoCs (Zynq, ZynqMP, Keystone I&II and Sitara). Familiar with Linux devicetree structure and development driver in kernel. Familiar with Yocto Project build system, rootfs customization and Jenkins pipeline. Had a study on network concepts and protocols such as TCP/IP.
Softwares	C, Git, MATLAB, OpenCl
Personal Skills	Punctuality, Teamwork, Flexibility and Adaptability
Languages	Persian (native), English (fluent)

Experience

Sina Innovative Communication Systems

Tehran, Iran

Expert Embedded Firmware Developer (full-time) — *May 2021 – Present*

- Restored interfaces based on Command Line Interface (CLI) and SNMP protocols for optical network systems (as a team member refactor most of cisco 4120 commands on the company's new product).
- Developed, maintained, and debugged framing, mapping, and multiplexing codes of optical framer chips and modules (as a team member in charge of development and maintenance in the new kernel version).
- Implemented and modified FPGA codes on optical telecommunication cards.
- Developed Linux drivers and apps for boards with the Yocto project and Jenkins pipeline.
- Handled project management with Scrum methodology, Jira, and Redmine platforms.

Simorgh Intelligent Sky

Tehran, Iran

Project Consultant and Expert Embedded System Developer (part-time) — *September 2020 – March 2023*

- Designed GPS and GLONASS acquisition and tracking algorithms on Zynq7020 based on freeRTOS and Max2769. All codes were done both in PL and PS parts (25s sweep 32 satellites with 82 frequency bins).
- Implemented and tested anti-jamming technique for GPS on Zynq7020 based on embedded Linux, AD9361, LTC2174, and NT1065 in PL and PS parts (with four antennas, each lane 800Mbps rate).
- Optimized mentioned algorithms in MATLAB by cooperation with the system designer to achieve the optimal solution, to implement on PL and PS parts of Zynq.

Yasin Engineering developers Co

Tehran, Iran

Midlevel Embedded Firmware and Hardware Developer (full-time) — *September 2017 – May 2021*

- Upgraded SATA2 to SATA3 HDL code based on 7 series Xilinx FPGAs with 470MB/s write rate.
- Developed SRIO (4x6Gb/s) and EMIF (16x200Mb/s) link between K2H and XCKU115 based on RTOS.
- Developed a 10G link on ZynqMP based on VPX protocols with almost 8Gb/s data rate.
- Customized and configured embedded Linux for designed boards based on ZynqMP and K2H.
- Customized and Enabled Linux drivers based on the device tree: KSZ9893 and Si5341.
- Enabled si5341 configuration code on ZynqMP FSBL to solve Highspeed IPs' clock demands in PL.
- Optimized and tested algorithms (MUSIC) on K2H by OpenCL (CBLAS and LAPACK libs).
- Configured ADC ICs by STM32 and Atmel microcontrollers (AD9680).

Projects

Other projects:

- Implemented HDL codes of configuration and transferred data from ADC to PC by TCP protocol based on FPGA.
- Designed a target detector radar simulator on MATLAB GUI based on Adaptive Pulse Compression Algorithms.
- Optimized and implemented some Adaptive Pulse Compression (APC) algorithms on MATLAB and FPGAs (using Vivado HLS).
- Tutored a workshop on "Hands-on TI keystone II processors" in Iran Electronics Industries (Introduction of ProcessorSDKs, config, modify and compile of the kernel, U-boot, drivers and kernel modules, examples about OpenCL, OpenMP, Cblas and LAPACK, Some topics about TI-RTOS).
- Created a TCP network between 13 client boards and two server boards with STM32H750 microcontrollers (With STM32CubeIDE and Keil IDE). A computer program was designed as a client with LabVIEW that sent configuration board data to the config server. Alarms were sent to the other server.

Education

Iran University of Science and Technology

Iran, Tehran

Master of Science in Electronic Engineering

September 2012 — March 2015

- Master's thesis: An integrated ultra-wideband low-phase noise oscillator circuit design – GPA: 18.30/20.00

Shahid Beheshti University

Iran, Tehran

Bachelor of Science in Telecommunication Engineering

September 2007 — September 2012

- Bachelor's thesis: Power management module design based on GSM network – GPA: 15.39/20.00