Alireza Zakeri

Embedded System Developer Engineer · Hardware Designer on FPGAs

Antwerpen, Belgium

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Summary

Experienced FPGA and Embedded Systems Developer with over 8 years of hands-on expertise in HDL design targeting both Intel and Xilinx FPGAs and SoCs. Skilled in customizing and optimizing Linux-based and real-time embedded systems, with a strong background in microcontroller programming and a broad familiarity with both low- and high-speed communication protocols. A collaborative team player with a passion for solving complex engineering challenges, continuously seeking to improve solutions and adapt to new technologies and tools as needed.

Skills

Hardware Development

- Proficient in RTL design with VHDL and SystemVerilog targeting Xilinx and Intel FPGA platforms.
- Skilled at identifying and resolving common HDL design issues such as timing violations and lint errors.
- Proficient in addressing debugging, testing, simulation, and board bring-up challenges throughout the HDL design and deployment process.
- Familiar with Analog Devices ADCs, STM32, and Atmel microcontrollers and their peripherals configuration (UART, I2C, SPI, and etc).

System Development

- Development and customization of Linux kernel, U-Boot, RTOS and firmware on Xilinx and TI SoCs (Zynq, ZynqMP, Keystone I&II and Sitara).
- Familiar with Linux devicetree structure and development driver in kernel.
- Experienced with the Yocto Project build system, rootfs customization, and Jenkins CI/CD pipeline.
- Had a study on network concepts and protocols such as TCP/IP.

Softwares

- C, VHDL, SystemVerilog, MATLAB, Yocto Project, OpenCl, Git, crosstool-NG
- Familiar with C++, OOP, Python, SQLite, CMake, UVM, Xen hypervisor

Personal Skills

- Punctuality, Teamwork, Flexibility, and Adaptability
- Skilled in Agile methodologies with hands-on use of JIRA, Confluence, Bitbucket, and GitLab for project management and version control

Languages

- Persian (native), English (fluent)

Education

Iran University of Science and Technology

Iran, Tehran

Master of Science in Electronic Engineering — *September 2012 — March 2015*

- Master's thesis: An integrated ultra-wideband low-phase noise oscillator circuit design – GPA: 18.30/20.00

Shahid Beheshti University

Iran, Tehran

Bachelor of Science in Telecommunication Engineering — *September 2007 — September 2012*

- Bachelor's thesis: Power management module design based on GSM network – GPA: 15.39/20.00

Experience

Dekimo Experts Gent
Gent, Belgium

Consultant (full-time) *July 2023 – Present*

Sony Depthsensing Solutions (SDS)
Brussels, Belgium

Expert RTL Designer (full-time) *January 2025 – July 2025*

- Designed and optimized a real-time CSI-2 packet to ASEP packet converter system with fragmentation for transmission, achieving minimal latency and without data buffering with SystemVerilog and Cadence Xcelium (SystemVerilog)
- Collaborated in a team environment utilizing Bitbucket for source control, Confluence for documentation, and Jira for task and sprint planning.
- Working with the verification team to design tests for system debugging using Universal Verification Methodology (UVM with SystemVerilog)
- **Improved skills**: SystemVerilog, Digital design, UVM libraries

CarUX
Heerlen, Netherlands

Expert RTL Designer (full-time) *July 2023 – November 2024*

- Developed and optimized a complete controller system based on the Nios II processor on Intel FPGAs with a wide variety of prepherals (SD card reader, DDR4, I2C, UART, etc)
- Developed a video stream generator system based on DisplayPort on Intel FPGAs using Multi-Stream Transport (MST) for transmission of high-resolution video streams in VHDL.
- Implemented a video stream transmitter based on DisplayPort with Display Stream Compression (DSC), live compressor, and playback pre-compressed image loader for high-resolution images in VHDL.
- Merge the system controller with MST (3 streams plus DSC compression) and enable HDCP v2.3 in one project (partially implemented in C and partially in VHDL).
- **Improved skills**: VHDL for RTL design, C for drivers on NIOS II.

Sina Innovative Communication Systems
Tehran, Iran

Expert Embedded Firmware Developer (full-time) *May 2021 – June 2023*

- Interfaces Development Based on Command Line Interface (CLI) and SNMP protocol for Optical Network Systems (as a team member refactor most of Cisco 4120 commands on the company's new product) with C language.
- Developed, maintained, and debugged framing, mapping, and multiplexing codes of optical framer chips and modules (as a team member in charge of development and maintenance in the new kernel version).
- Implemented and modified FPGA codes on optical telecommunication cards.
- Developed Linux drivers and apps for boards with the Yocto project and Jenkins pipeline.
- Collaborated in a team environment utilizing GitLab for source control, Confluence for documentation, and Jira for task and sprint planning.
- **Improved skills**: C for development of libraries and applications, Yocto project, Linux.

Simorgh Intelligent Sky
Tehran, Iran

Project Consultant and Expert Embedded System Developer (part-time) *September 2020 – March 2023*

- Implementation of GPS and GLONASS acquisition and tracking algorithms on Zynq7020 based on FreeRTOS and Max2769 (partially implemented in C and partially in VHDL) sweep 32 satellites with 82 frequencies).
- GPS anti-jamming implementation on Zynq7020 based on embedded Linux, AD9361, LTC2174, and NT1065 (partially implemented in C and partially in VHDL).
- Optimization of mentioned algorithms in MATLAB by cooperation with the system designer to achieve the optimal solution, to implement on PL and PS parts of Zynq.
- **Improved skills**: C for development of drivers, libraries, and applications. VHDL for RTL design, Petalinux and Linux kernel and drivers configuration.

Yasin Engineering developers Co
Tehran, Iran

Midlevel Embedded Firmware and Hardware Developer (full-time) *September 2017 – May 2021*

- Customization and configuration of embedded Linux for designed boards based on ZynqMP and K2H with C.
- Linux driver customization and development based on device tree: KSZ9893 and Si5341 with C.
- Developed a PCIe IP speed testing project on Xilinx FPGA with VHDL.
- Upgrade SATA2 to SATA3 HDL code based on 7 series Xilinx FPGAs with 470MB/s write rate with VHDL.
- SRIO (4x6Gb/s) and EMIF (16x200Mb/s) link Development between K2H and XCKU115 based on RTOS (partially implemented in C and partially in VHDL)
- 10G link development on ZynqMP based on VPX protocols with almost 8Gb/s data rate (partially implemented in C and partially in VHDL)
- Development si5341 configuration code on ZynqMP FSBL to solve Highspeed IPs' clock demands in PL in C.
- Optimization and development of algorithms (MUSIC) on K2H by OpenCL (CBLAS and LAPACK libs).
- Configuration ADC ICs by STM32 and Atmel microcontrollers (AD9680) with C.
- Performed board bring-up for FPGA/SoC-based hardware integrating high-speed ADCs.
- **Improved skills**: C for development of drivers, libraries, and applications. VHDL for RTL design.

Projects

Other projects:

- Design a Xen hypervisor system on ZynqMP based on a Dom0 Linux kernel and one DomU guest kernel with an NFS filesystem (Self-study).
- Implementation of configuration and transfer data from ADC to PC by TCP protocol based on FPGA (Personal project).
- Design a target detector radar simulator on MATLAB GUI based on Adaptive Pulse Compression Algorithms (Personal project).
- Design and implementation of adaptive pulse compression algorithms on Matlab and FPGAs using Vivado HLS (Personal project).
- Tutored a workshop on ”Hands-on TI keystone II processors” in Iran Electronics Industries (Introduction of ProcessorSDKs, config, modify and compile of the kernel, U-boot, drivers and kernel modules, examples about OpenCL, OpenMP, Cblas and LAPACK, Some topics about TI-RTOS) (Contract project).
- Created a TCP network between 13 client boards and two server boards with STM32H750 microcontrollers (With STM32CubeIDE and LwIP library). A computer program was designed as a client with LabVIEW that sent configuration board data to the config server. Alarms were sent to the other server with C (Contract project).