ECSE 330 SPICE Project

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***Abstract*—Amplification of a $50\,\mathrm{mV}$ sinusoidal wave from a transducer can be accomplished using an NMOS transistor by establishing appropriate DC operating points. We wish to produce a signal between 2 to $6\mathrm{V}$. To accomplish this a regulated $18\,\mathrm{V}$ power supply was created using a zener diode. The result of this design was a single stage amplifier with an effective gain of approximately $-37\,\mathrm{V/V}$ and a bandwidth of $9900\,\mathrm{Hz}$. The final output signal stretched from 2.1 to $5.8\mathrm{V}$**

CONTENTS

I. REQUIREMENTS

We are given a transducer that produces a $50\,\mathrm{mV}$ sinusoidal output with an unknown DC bias. The AC component of this signal needs to be amplified and biased into the range $2\,\mathrm{V}$ to $6\,\mathrm{V}$. Additionally, the amplifier should have a constant amplification and bias for frequencies from $0.1\,\mathrm{kHz}$ to $10\,\mathrm{kHz}$.

The components of the system are as follows:

1) Power Supply
   a) Step Down Transformer
   b) Rectifier
   c) Filter
   d) Regulator
2) Amplification
   a) Coupling
   b) DC Bias
   c) Amplifier

We will begin our design with a top down approach. This will allow us to define our dependencies better.

The transistor we are provided is a CD4007 NMOSFET. The transistor's manufacturing parameters are as follows:

1) $k_n^{'} = 111\,\mu\mathrm{A\,V^{-2}}$
2) $W = 30\,\mu\mathrm{m}$
3) $L = 10\,\mu\mathrm{m}$
4) $V_t = 2\,\mathrm{V}$
5) $k_n = k_n^{'}\frac{W}{L} = 333\,\mu\mathrm{A\,V^{-2}}$

II. AMPLIFIER

In order to amplify a $50\,\mathrm{mV}$ signal to $2\,\mathrm{V}$ signal we need the amplifier's gain to be close to $40\,\mathrm{V/V}$. We can model the load, an ADC, as a $10\,\mathrm{M\Omega}$ resistor and $10\,\mathrm{pF}$ capacitor in parallel.

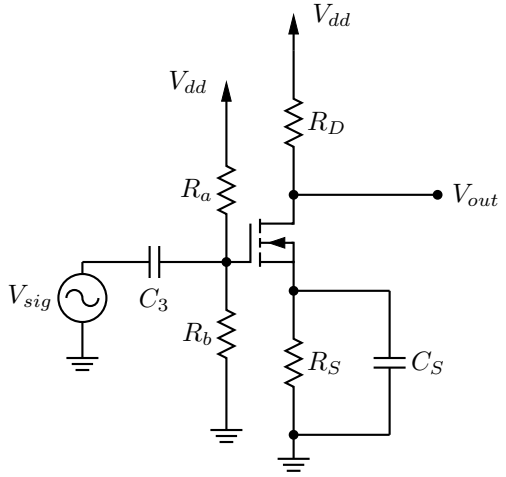


Fig. 1: CS Amplifier with Source Impedance[1]

We have to select the resistors to achieve the gain we need. The three design parameters are V_D, V_G, and V_S.

Using some intuition we can select V_S to be small so as to approximate a regular common source amplifier. However, we cannot set it to zero otherwise we would have a degenerate amplifer. This makes the gain of the circuit highly susceptible to changes in temperature. Additionally, R_S and C_S improve the bandwidth of the amplifier. Without these components, signals at low frequencies would experience greater attentuation that those at higher frequencies.

The capacitor C_3 is a coupling capacitor and we select a standard value of $1\,\mu\text{F}$. This is a good trade-off between the RC constant of the coupling capacitor and the attentuation at lower frequencies.

The resistors R_a and R_b are used to setup the DC bias point of the MOSFET's gate. I will show how I selected the values for these resistors as well as R_D and R_S using DC operating point analysis.

A. DC Operating Point

The first step is to establish V_D. Since the signal must be present between $2\,\text{V}$ and $6\,\text{V}$ we need to select a value within those boundaries. Selecting $4\,\text{V}$ is normally ideal as that allows to use a gain of $40\,\text{V}/\text{V}$ to fill the entire range. However, due to the load of the ADC, we will need a higher DC operating point. I will select $V_D = 5.2\,\text{V}$.

Since I want to approximate a typical common source amplifier I will select $V_S = 0.1\,\text{V}$ This will provided sufficient compromise between degeneration and our approximation.

The final step is to select V_G, our quiescient point. In order to facilitate this I have written a MATLAB script to calculate all possible arrangements of the component values for multiple value of V_G. Then we can select all solutions that produce a gain between $40\,\text{V}/\text{V}$ and $30\,\text{V}/\text{V}$. The results of the compution are presented in the appendix. For the complete script and its original output, please see the appendix.

We select $V_G = 2.5758\,\text{V}$. Now that we have our DC operating point established we can calculate the values of our resistors.

$$I_D = \frac{1}{2}k_n(V_G - V_S - V_t)^2(1 + \lambda V_{DS}) \approx 39.62\,\mu\text{A}$$

$$R_D = \frac{V_{dd} - V_D}{I_D} \approx 323.07\,\text{k}\Omega$$

$$R_S = \frac{V_S}{I_D} \approx 2.524\,\text{k}\Omega$$

For our bias resistors we have additional requirements. The input resistance of the amplifier must be greate than $20\,\text{k}\Omega$. Thus we must select R_a and R_b to satisfy these conditions.

$$\left(18\,\text{V}\left(\frac{R_b}{R_b + R_a}\right) = 2.5758\,\text{V}\right) \wedge \left(\frac{R_b R_a}{R_b + R_a} > 20\,\text{k}\Omega\right)$$

We will select $R_b = 25\,\text{k}\Omega$ and $R_a = 149.71\,\text{k}\Omega$ to satisfy these conditions.

The value of C_S has been chosen as $100\,\mu\text{F}$.

We can now calculate the transconductance, g_m, and the output resistance, r_o, for the small signal model calculations.

$$g_m = \frac{2I_D}{V_G - V_S - V_t} \approx 166.54\,\mu\text{A}\,\text{V}^{-1}$$

$$r_o = \frac{V_A + V_{DS}}{I_D} \approx 2.6527\,\text{M}\Omega$$

This completes the DC operating point analysis of the transistor.

B. Small Signal Model

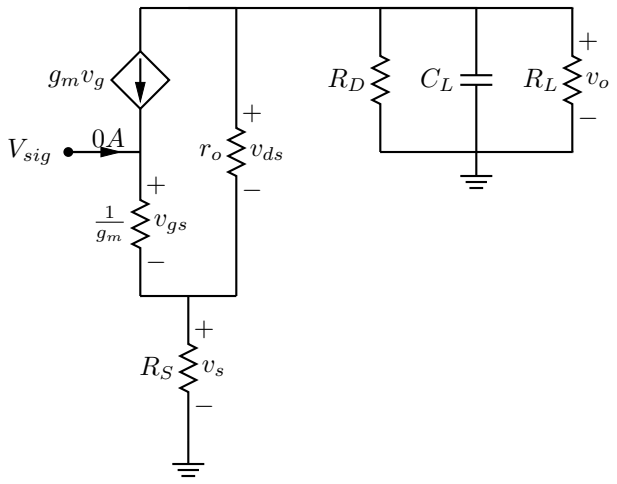


Fig. 2: Small Signal Model.

The small signal model for the amplifier can be seen above. From figure we can see that the open circuit gain of this amplifier is.

$$|G_o| = \frac{g_m R_D r_o}{R_D + R_S + r_o + g_m r_o R_S} \approx 34.8702\,\text{V}\,\text{V}^{-1}$$

The effective gain with a $10\,\text{M}\Omega$ load is

$$|G_l| = \frac{g_m r_o\,(R_D \parallel R_L)}{(R_D \parallel R_L) + R_S + r_o + g_m r_o R_S} \approx 33.7486\,\text{V}\,\text{V}^{-1}$$

This is only valid at low frequencies where the capacitor acts an open circuit. For extremely high frequencies the signal is attentuated. However, due to the addition of C_S the attenuation will be negligible and we will observe this in the simulation section.

Additionally, in the simulations, the signal fills the range $2.1\,\text{V}$ to $5.8\,\text{V}$ using this gain.

III. Power Supply

The power supply would need to power both the transducer and the amplifier. The client's requirements are as follows:

- Line regulation $> 10\,\text{mV}/\text{V}$
- Load regulation $> -5\,\text{mA}/\text{mV}$

A. Step Down Transformer

Mains power supply is provided at $120\,\text{V}$ $60\,\text{Hz}$ rms. This corresponds to $169.7\,\text{V}$ peak-to-peak $60\,\text{Hz}$. For our requirements we need to step down the voltage to approximately $30\,\text{V}$ $60\,\text{Hz}$.

$$\sqrt{\frac{L_p}{L_s}} = \frac{V_p}{V_s} = \frac{169.7}{30} \approx 5.6597$$

To satisfy this we select inductances $L_p = 100\,\text{H}$ and $L_s = 3.125\,\text{H}$. This will ensure that the AC load from the mains supply mostly drops accross the primary coil. We also select a coupling coefficient $K = 1$.

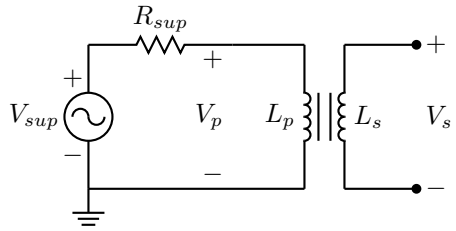


Fig. 3: Step Down Transformer Configuration.

From the above figure, we can see that $V_p \approx V_{sup}$ due to the large inductance of the primary coil. Thus $V_s \approx 30\,\text{V}\sin(2\pi 60t)$. Assuming that $R_{sup} = 300\,\Omega$.

B. Rectifier and Filter

Now that we have a sufficient AC sinusoidal we now need to convert the AC components into DC components. The first step in this proces is rectification. We will use a full bridge rectifier.

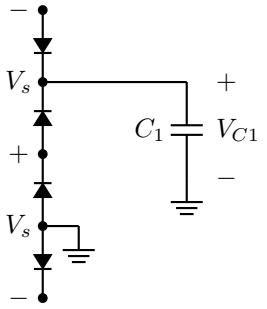


Fig. 4: Rectifier and Filter Configuration

The capacitor C_1 will be assigned a value of $100\,\mu\text{F}$. This should proved sufficient stabilisation of the voltage for the next stage, regulation. The output of this circuit is V_{C1} and the input is V_S.

We can calculate the average value of V_{C1} using the following method. The input sine wave is $60\,\text{Hz}$, hence if we take one quarter of the period, the capacitor will be discharging in this period.

$$T_0 = \frac{1}{4 \cdot 60} \approx 4.17\,\text{ms}$$

$$V_{C1} = 30 - \exp\left(\frac{-0.00417}{100 \cdot 10_{-6} \cdot 395}\right) \approx 26.994\,35\,\text{V}$$

However, the capacitor will also be discharging on the upswing of the sinusoidal input, at least until it reahces $26.994\,35\,\text{V}$. So we can calculate the time taken for this as

$$30\sin(2\pi 60t) = 26.99435 \implies t \approx 5.364\,\text{ms}$$

Thus the actual minimum value of V_{C1} is

$$V_{C1,min} = 30\exp\left(\frac{-0.00417 - 0.00536}{100 \cdot 10^{-6} \cdot 395}\right) \approx 23.566\,\text{V}$$

Thus taking the average we obtain $\langle V_{C1}\rangle = \frac{23.566+30}{2} \approx 26.75\,\text{V}$. Which I will approximate it as $26.5\,\text{V}$ because the actual peak value of the sinusoidal is actually less than $30\,\text{V}$.

C. Regulator

We have to calculate our requried regulated voltage V_{dd}. My student ID is 260681986 so $\alpha = 8.6$.

$$V_{dd} = \lfloor 10 + 8.6 \rfloor = 18$$

This will also be the output of the circuit as well as the final regulated supply for the amplifier. We will model our zener as operating in the break down region.

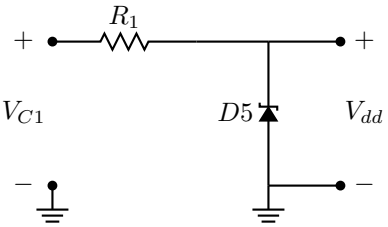


Fig. 5: Regulator Configuration

The load regulation is required to be greater than $-5\,\text{mV}\,\text{mA}^{-1}$. We select $4\,\Omega$ to satisfy this. Then we can establish our line regulation using R_1

$$-r_z > -5\,\text{mV}\,\text{mA}^{-1} \implies r_z < 5\,\Omega$$

$$\frac{4\,\Omega}{4\,\Omega + R_1} > 10\,\text{mV/V} \implies R_1 < 396\,\Omega$$

Select $R_1 = 395\,\Omega$ to satisfy this. If I had chosen a lower value for r_z, we would have a lower value for R_1 and too much current would have entered the diode and potentially caused it to burn. Thus we choose the highest possible value, to limit the current, while also meeting the load regulation specification.

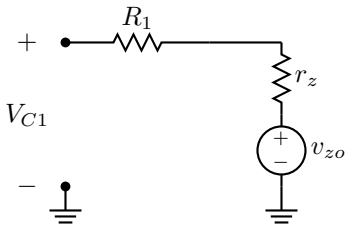


Fig. 6: Regulator Model[2]

The last value that needs to be selected is v_{zo}. Assuming a load current draw of $I_L \approx I_D$. We can solve for $v_{zo} = 17.914\,\mathrm{V}$ using $V_{C1} \approx 26.5\,\mathrm{V}$ on average, according to the simulations.

$$v_{zo} \approx 18\,\mathrm{V} - 4\,\Omega\left(\frac{26.5\,\mathrm{V} - 18\,\mathrm{V}}{395\,\Omega} - 40\,\mu\mathrm{A}\right) \approx 17.914\,\mathrm{V}$$

Simulations will show that this value is sufficient. Thus we can replace the zener diode D5 with this model. However, for the purposes of illustration, we shall keep the zener diode symbol in our schematics.

D. Completed Power Supply

Combining all the above components to create our power supply.

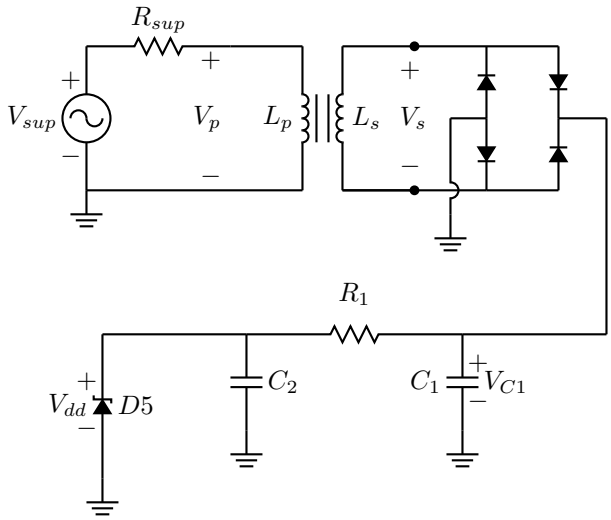


Fig. 7: Power Supply [2]

The capacitor C_2 is a decoupling capacitor for the power supply. It will be used to smoothen out the ripples caused by $D5$.

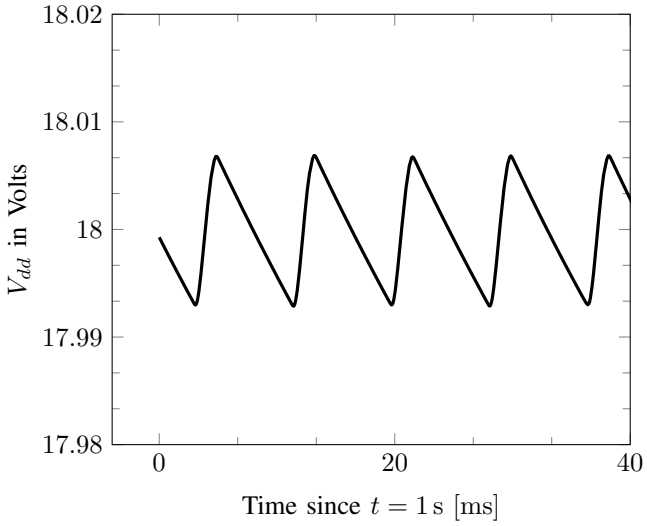
The final values for all the components are as follows

1) $R_{sup} = 0.3\,\mathrm{k}\Omega$
2) $L_p = 100\,\mathrm{H}$
3) $L_s = 3.125\,\mathrm{H}$
4) $C_1 = 100\,\mu\mathrm{F}$
5) $C_2 = 10\,\mathrm{pF}$
6) $R_1 = 395\,\Omega$
7) $r_z = 4\,\Omega$
8) $v_{zo} = 17.914\,\mathrm{V}$

IV. Power Supply Simulations

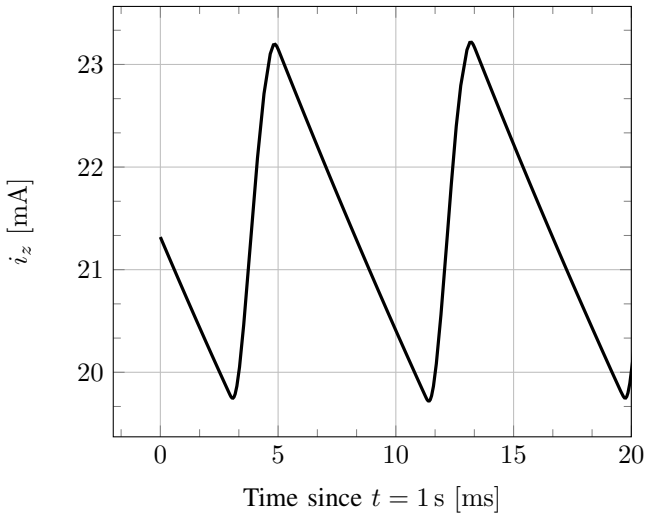
Constructing the power supply in LTSPICE and connecting it the amplifer circuit we can observe the behaviour of the supply.

Fig. 8: Plot of V_{dd} against time



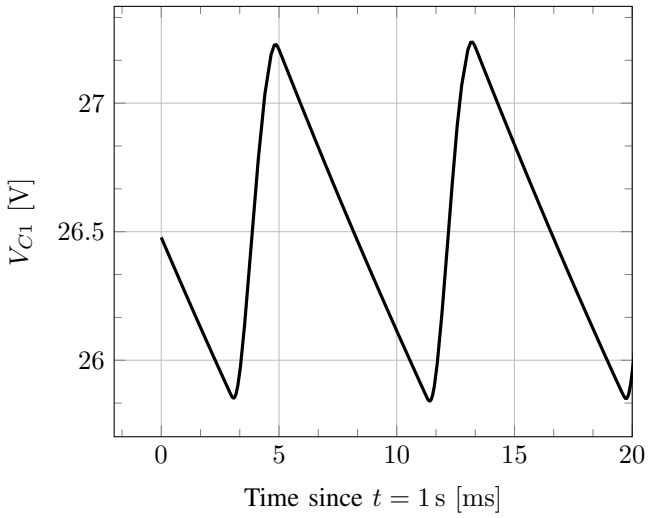
The ripples in the voltage are caused by the zener diode rapidly opening and closing. This is why the smoothing capacitor is needed, however SPICE does not show the smoothing. In an actual circuit we will see a constant voltage. Next we will plot the current though the zener diode D5, as i_z.

Fig. 9: Plot of i_z against time



As can be seen from the above plots. V_{dd} is approximately $18\,\mathrm{V}$ and the current draw matches the expected value when v_{zo} was calculated.

Fig. 10: Plot of V_{C1} against time



As you can see in the above plot, the average value of V_{C1} is $26.5\,\mathrm{V}$. Thus justifying our value for v_{zo}.

Our predictions and calculations for the power supply performance are correct. The supply behaves extremely close to ideal and can handle a large range of loads.

V. Amplifier Simulations

The amplifier was tested using a $100\,\mathrm{Hz}$ signal. Higher frequencies will not suffer from attenuation and so will be at their most ideal value. Thus the greatest problems with gain should arise at lower frequencies. For all tests the amplifier was connected to the power supply I designed.

Fig. 11: Plot of V_{sig} against time, $100\,\mathrm{Hz}$

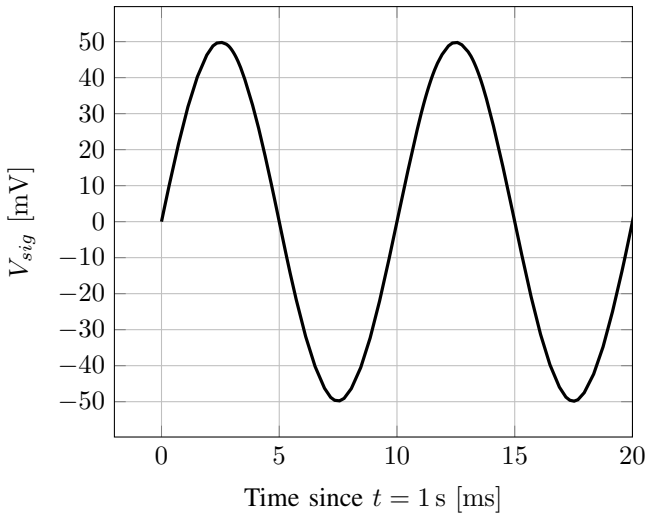
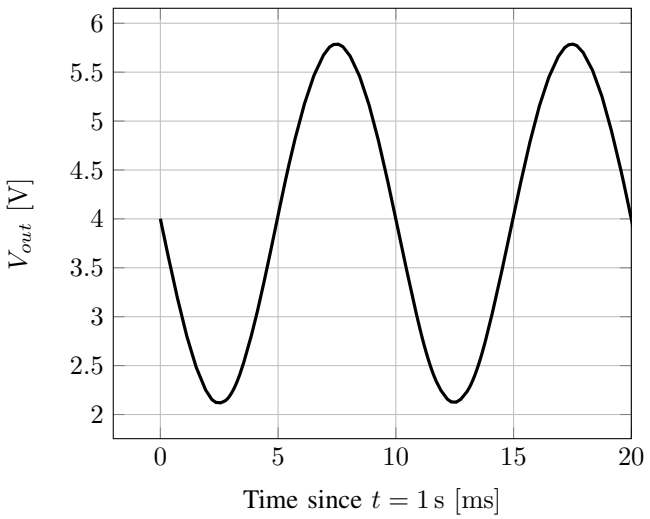


Fig. 12: Plot of V_{out} against time, $100\,\mathrm{Hz}$



From the above plot it can be see that the signal is inverted and has an effective gain of $-37\,\mathrm{V/V}$. The value is higher than we predicted. This is due the $10\,\mathrm{pF}$ capacitive load. C_L acts like a short for AC signals thus reducing the effect of R_L.

The low frequency signal's lack of attentuation is due to C_S and R_S. These components extend the bandwidth by stabilising the voltage at V_S.Now I will analyse the circuit's performace for a high frequency signal.

Fig. 13: Plot of V_{sig} against time, $10\,\mathrm{kHz}$

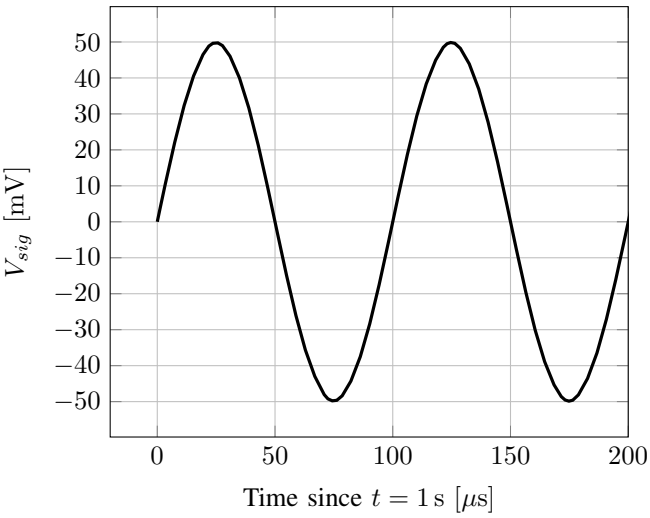
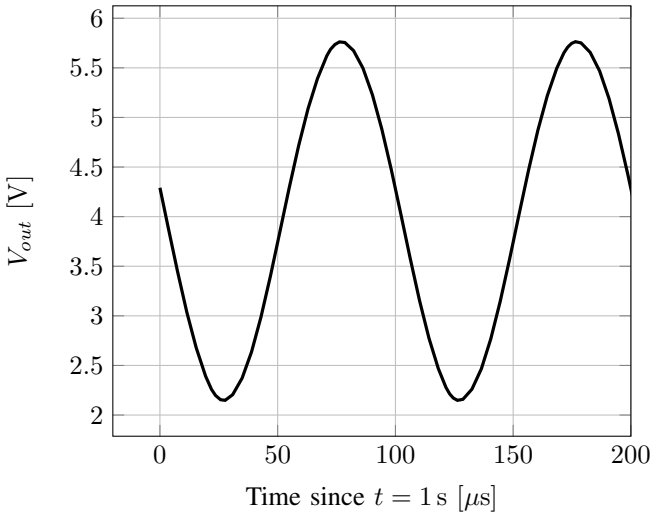
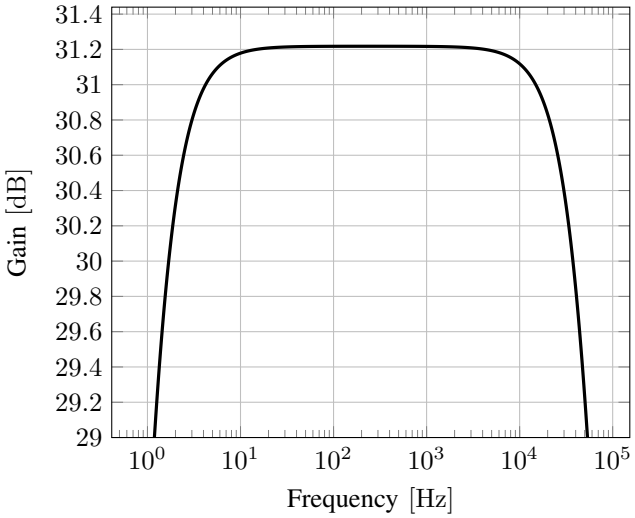


Fig. 14: Plot of V_{out} against time, 10 kHz



The waveforms are nearly identical except for their frequencies. You can see thus that the amplifier has an effective bandwidth of 9900 Hz.

Fig. 15: Frequency Response, $\frac{V_{out}}{V_{sig}}$



VI. Conclusion

While an amplifier is quite easy to model and build with no load, the difficulty becomes quite apparent when applying a load. Due to changes in the current draw and additional attenuation from capacitive loads, constructing a reliable amplifier can become extremely complicated. Nonetheless, what has been created in this paper is an amplifier for a 100 mV peak-to-peak sinusoidal signal. The amplifier's gain is consistent over the frequency range 0.1 kHz to 10 kHz. While at the very beginning the output the amplifier is saturated to 18 V, within a second the output is within acceptable ranges. Hence if you were going to use this amplifier in a real circuit, I would allow for short warm up period. One second should be enough time for the capacitors to charge up and allow AC signals through.

However, while this amplifier does work well, it also inverts the signal. This isn't an issue for the ADC however, as signal can be interpreted as inveretede by the microprocessor. However, for other analog operations this inversion is undesirable. Thus a multistage common source amplifier setup would be required to create a positive gain.

List of Figures

Appendix A
Initial Conditions Omission

The initial conditions of the circuit do not matter as we are only interested in the long term behaviour of our circuit, but we can see that there is a warm up time for the circuit. This is the time taken for the capacitors to charge and reach their DC operating point. However, this information has been omitted because it was not deemed relevant and hence all graphs start at $t = 1$.

Appendix B
Inverted Signal Output

After speaking to the TA, I was told that an inverted signal is not a problem and could be handled by the microcontroller. This is why no attempt has been made to remove the inversion.

Appendix C
MATLAB Code

```
% Common Source Amplifier
% with Source Resistance
clear all;
clc;
% Constants
V_t = 2;
k_n = 333e-6;
V_DD = 18;
lambda = 0.01;

% Parameters
V_D = 5.2;
Q = linspace(2, 5, 100);
```

```
V_S = 0.1;
R_b = 25e3;

V_ov = Q - V_S - V_t;
V_DS = V_D - V_S;
I_D = 0.5 * k_n * V_ov.^2 ...
    * (1 + lambda * V_DS);
R_D = (V_DD - V_D)./I_D;
R_S = V_S./I_D;
gm = 2 * I_D ./ V_ov;
r_o = ((1/lambda) + V_DS)./I_D;
gain = (-gm .* R_D .* r_o) ...
    ./(R_D + R_S + r_o + gm.*R_S.*r_o);
R_a = V_DD*R_b./(Q) - R_b;

solutions = find(gain < -32 ...
    & gain > -38);
Gains = gain(solutions)
output_resistances = r_o(solutions)
bias_points = Q(solutions)
drain_resistances = R_D(solutions)
source_resistances = R_S(solutions)
biasing_resistors = R_a(solutions)
```

APPENDIX D
MATLAB OUTPUT

I selected the middle column of values.

```
Gains =
  -36.5647   -34.8702   -33.3258
output_resistances =
   1.0e+06 *
    3.0268     2.6535     2.3452
bias_points =
    2.5455     2.5758     2.6061
drain_resistances =
   1.0e+05 *
    3.6863     3.2316     2.8562
source_resistances =
   1.0e+03 *
    2.8799     2.5247     2.2314
biasing_resistors =
   1.0e+05 *
    1.5179     1.4971     1.4767
```

APPENDIX E
SPICE NETLIST

V_{out} is node 10.

```
********************************
********************************
** ECSE330_SPICE_PROJECT
**
** ECSE 330 SPICE PROJECT
** Desgined by Ali Sharif, 260681986
**
** Tested in LTspice XVII
********************************
********************************

********************************
* POWER SUPPLY AND REGULATOR
********************************
* Description: Produces regulated
*  output of 18 Volts
Vsup 1 0 SINE(0 169.7 60)
Rsup 1 2 300
Lp 2 0 100
K Lp Ls 1
Ls 3 4 3.125
D1 0 3 1N4148
D2 0 4 1N4148
D3 3 6 1N4148
D4 4 6 1N4148
C1 6 0 100u
R1 6 Vdd 395
Rz Vdd 13 4
Vz 13 0 17.914
C2 Vdd 0 10p
********************************
* END POWER SUPPLY AND REGULATOR
********************************

********************************
* AMPLIFIER
********************************
M1 10 8 9 9 CD4007
RD Vdd 10 3.2316e5
RS 9 0 2.5247e3
CS 9 0 100u
Ra Vdd 8 1.4971e5
Rb 8 0 25k
C3 11 8 10u
Vsig 11 0 AC 0.05 0
********************************
* END AMPLIFIER
********************************

********************************
* ADC LOAD EQUIVALENT
********************************
RL 10 0 1meg
CL 10 0 10p
********************************
* END ADC EQUIVALENT
********************************

* Analysis Requests
*.tran 20us 1.0001 1
.ac dec 100 1 100k

********************************
* MODELS FOR COMPONENTS
********************************
* 1N4148 Signal Diode
.model 1N4148  D (
+ Is=5.84n N=1.94 Rs=.7017
+ Ikf=44.17m Xti=3 Eg=1.11
+ Cjo=.95p M=.55 Vj=.75
+ Fc=.5 Isr=11.07n Nr=2.088
+ Bv=100 Ibv=100u Tt=11.07n )
*****
* CD4007 NMOS transistor SPICE model
.model CD4007 NMOS (
+ Level=1    Gamma= 0    W=30u   L=10u
+ Tox=1200n  Phi=.6      Rs=0    Kp=111u
+ Vto=2.0  Lambda=0.01
+ Rd=0 Cbd=2.0p   Cbs=2.0p   Pb=.8
+ Cgso=0.1p Cgdo=0.1p  Is=16.64p  N=1 )
********************************
* END MODELS FOR COMPONENTS
********************************
.end
```

REFERENCES

[1] Gordon W. Roberts. *Transistor Amplifiers Chapter 7*. 2017.

[2] Gordon W. Roberts. *Diode Chapter 4*. 2017.