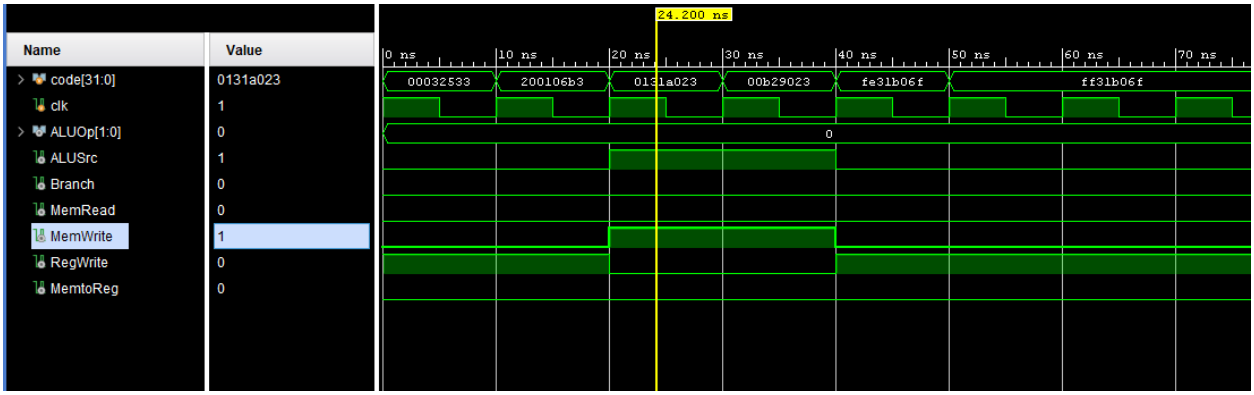
Computer Organization and Architecture

Complex Engineering Problem

Control Unit:

The Control Unit is responsible for generating control signals required to control the various stages of the pipeline. It ensures that instructions are executed correctly according to the RISC-V ISA specifications and supports all required instructions and pipeline stages.



Explanation:

The instruction is taken as input which generates the control signal, it identifies which operation have to be take place memory read, memory write, branch etc. Each instruction has a specified control signal.

R:

Func7	rs2	rs1	Func3	rd	opcode
0000000	01001	00010	000	01001	0110011

I:

imm[11]	rs1	Func3	rd	opcode
0010000000	00001	000	00001	0000011

L:

Func7	rs2	rs1	Func3	rd	opcode

00011	10000	01100	010	00001	0000011

S:

Imm[11:5]	rs2	rs1	Func3	Imm[4:0]	opcode
0000000	01001	00010	010	01011	0100011

Jal:

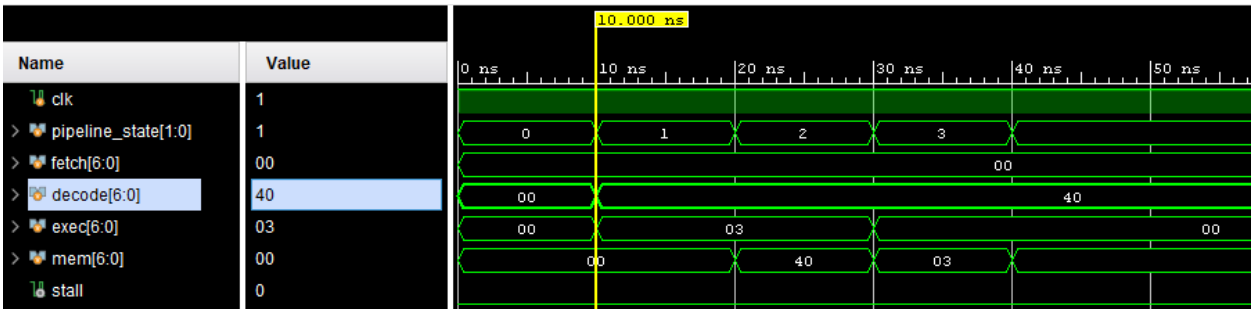
Imm[11:5]	rs2	rs1	Func3	Imm[4:0]	opcode
1111111	0011011	0011001	000	11111	1100111

BEQ:

Imm[11:5]	rs2	rs1	Func3	Imm[4:0]	opcode
0000010	0000110	0000010	000	00000	1100011

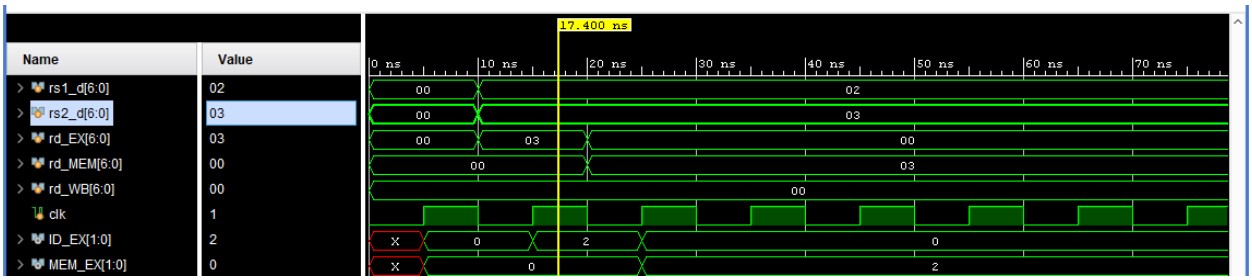
Hazard Detection Unit:

The Hazard Detection Unit is responsible for identifying potential hazards within the pipeline, such as data hazards, control hazards, and structural hazards. Its primary objective is to detect dependencies between instructions and determine whether any action needs to be taken to ensure correct execution and maintain pipeline throughput.



Forwarding Unit:

The Forwarding Unit, also known as the Data Forwarding Unit, is designed to resolve data hazards by forwarding data directly from one pipeline stage to another. Its goal is to minimize stalls in the pipeline caused by data dependencies between instructions.



It checks that if the source register from the decode stage match with the destination register from the execution and memory stage matches then they are stores in ID_EX,MEM_EX as a forwarding unit.