dtc_2 Project Status (03/18/2016 - 16:08:59)			
Project File:	bramTry_1.xise	**Parser Errors:**	No Errors
Module Name:	dtc_2	**Implementation State:**	Programming File Generated
Target Device:	xc6vlx240t-1ff1156	• **Errors:**	No Errors
Product Version:	ISE 14.5	• **Warnings:**	71 Warnings (6 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	9,060	301,440	3%	
Number used as Flip Flops	9,059			
Number used as Latches	1			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	4,982	150,720	3%	
Number used as logic	1,800	150,720	1%	
Number using O6 output only	453			
Number using O5 output only	142			
Number using O5 and O6	1,205			
Number used as ROM	0			
Number used as Memory	1,397	58,400	2%	
Number used as Dual Port RAM	0			
Number used as Single Port RAM	0			
Number used as Shift Register	1,397			
Number using O6 output only	827			
Number using O5 output only	1			
Number using O5 and O6	569			
Number used exclusively as route-thrus	1,785			
Number with same-slice register load	1,770			
Number with same-slice carry load	15			
Number with other load	0			
Number of occupied Slices	1,777	37,680	4%	
Number of LUT Flip Flop pairs used	6,346			
Number with an unused Flip Flop	904	6,346	14%	
Number with an unused LUT	1,364	6,346	21%	
Number of fully used LUT-FF pairs	4,078	6,346	64%	
Number of unique control sets	85			
Number of slice register sites lost to control set restrictions	342	301,440	1%	
Number of bonded IOBs	1	600	1%	
Number of LOCed IOBs	1	1	100%	
Number of RAMB36E1/FIFO36E1s	40	416	9%	
Number using RAMB36E1 only	40			

Number using FIFO36E1 only	0			
Number of RAMB18E1/FIFO18E1s	10	832	1%	
Number using RAMB18E1 only	10			
Number using FIFO18E1 only	0			
Number of BUFG/BUFGCTRLs	3	32	9%	
Number used as BUFGs	3			
Number used as BUFGCTRLs	0			
Number of ILOGICE1/ISERDESE1s	0	720	0%	
Number of OLOGICE1/OSERDESE1s	0	720	0%	
Number of BSCANs	1	4	25%	
Number of BUFHCEs	0	144	0%	
Number of BUFIODQSs	0	72	0%	
Number of BUFRs	0	36	0%	
Number of CAPTUREs	0	1	0%	
Number of DSP48E1s	0	768	0%	
Number of EFUSE_USRs	0	1	0%	
Number of FRAME_ECCs	0	1	0%	
Number of GTXE1s	0	20	0%	
Number of IBUFDS_GTXE1s	0	12	0%	
Number of ICAPs	0	2	0%	
Number of IDELAYCTRLs	0	18	0%	
Number of IODELAYE1s	0	720	0%	
Number of MMCM_ADVs	0	12	0%	
Number of PCIE_2_0s	0	2	0%	
Number of STARTUPs	1	1	100%	
Number of SYSMONs	0	1	0%	
Number of TEMAC_SINGLEs	0	4	0%	
Number of RPM macros	8			
Average Fanout of Non-Clock Nets	2.08			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0, Component Switching Limit: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Fri Mar 18 16:02:59 2016	0	37 Warnings (6 new)	558 Infos (0 new)
Translation Report	Current	Fri Mar 18 16:04:13 2016	0	0	0
Map Report	Current	Fri Mar 18 16:05:54 2016	0	11 Warnings (0 new)	7 Infos (0 new)
Place and Route Report	Current	Fri Mar 18 16:07:11 2016	0	12 Warnings (0 new)	0
Power Report					
Post-PAR Static Timing Report	Current	Fri Mar 18 16:07:32 2016	0	0	3 Infos (0 new)
Bitgen Report	Current	Fri Mar 18 16:08:48 2016	0	11 Warnings (0 new)	1 Info (0 new)

Secondary Reports		[-]
Report Name	**Status**	**Generated**
WebTalk Report	Current	Fri Mar 18 16:08:49 2016
WebTalk Log File	Current	Fri Mar 18 16:08:59 2016

Date Generated: 03/18/2016 - 16:08:59