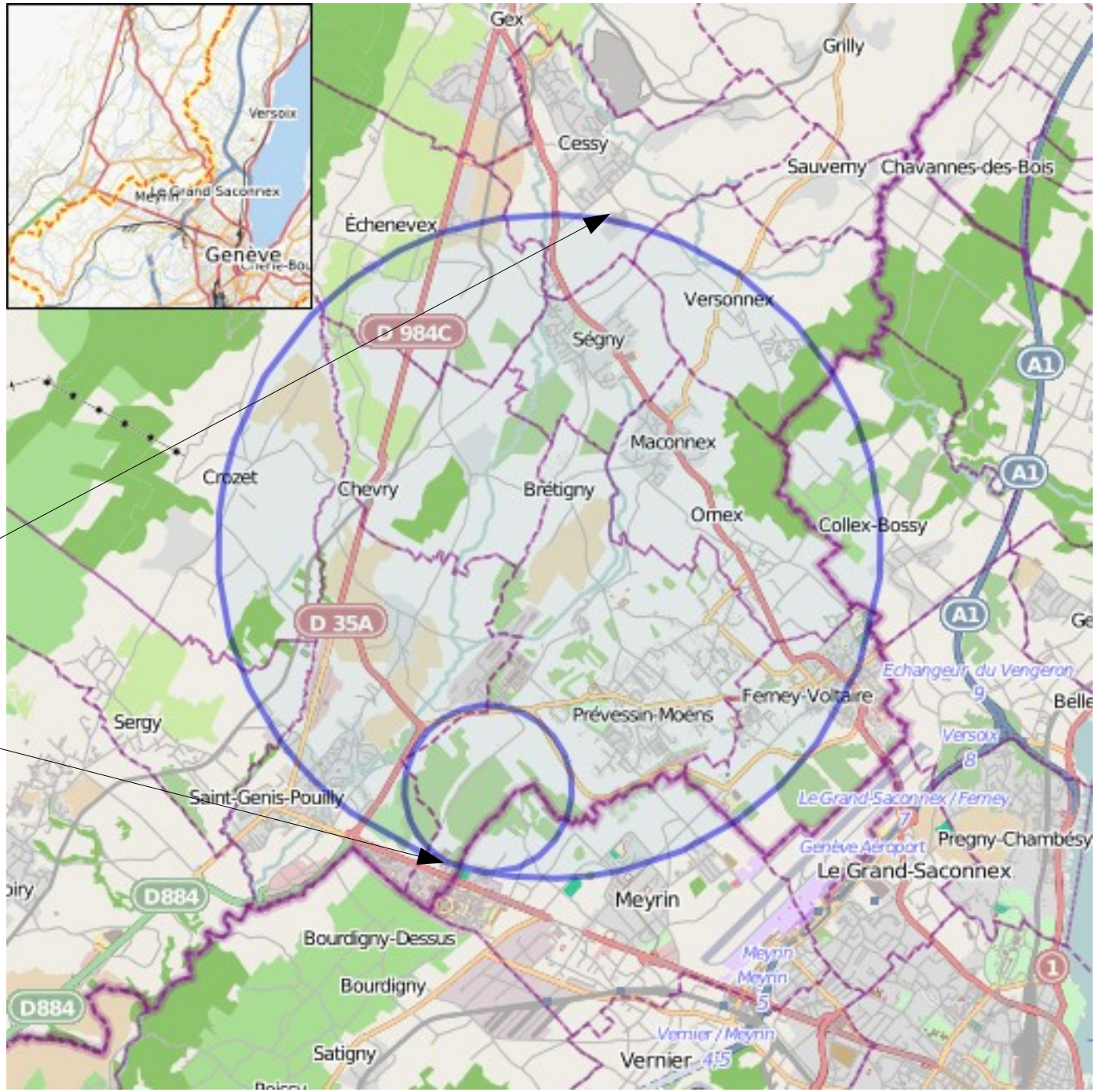
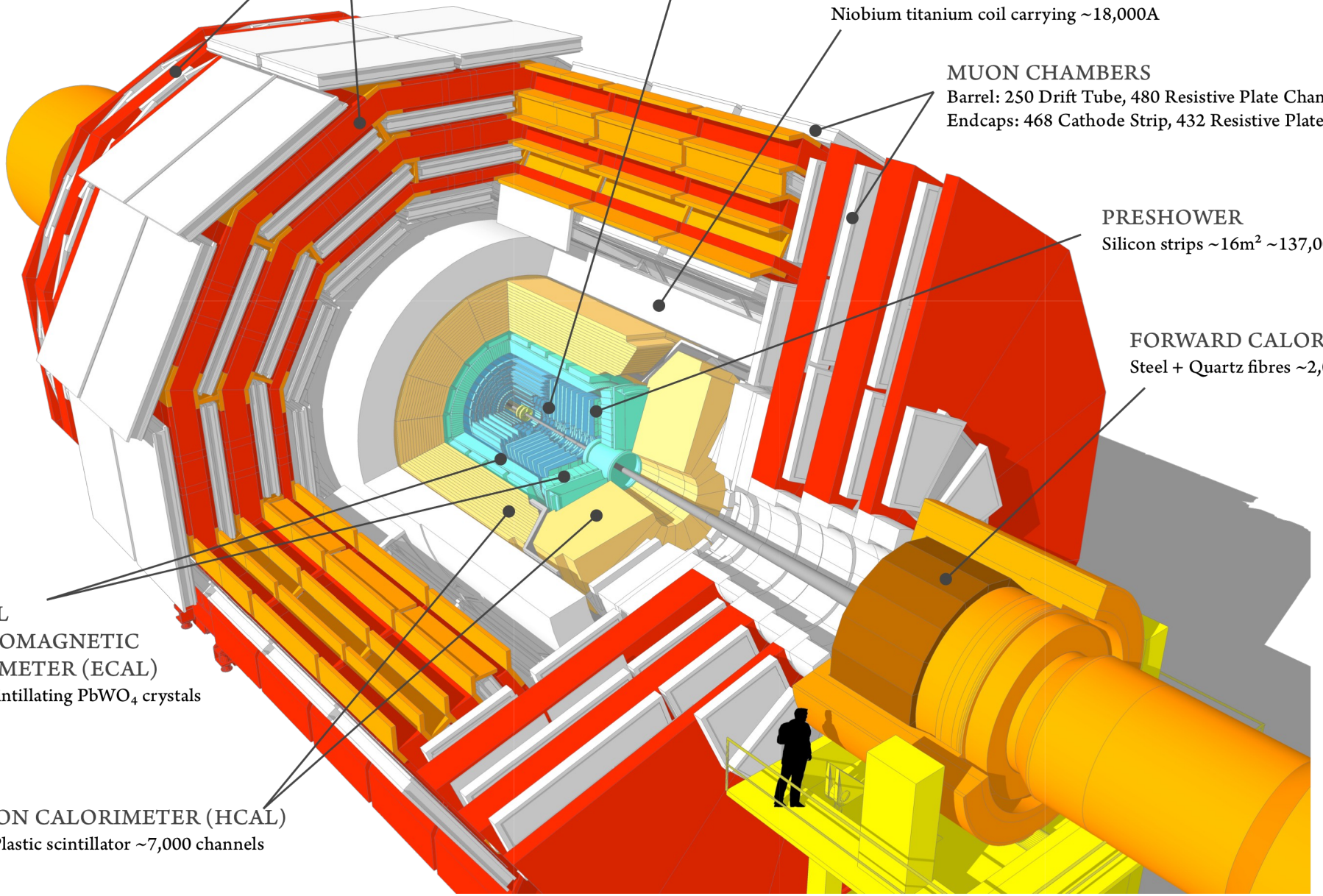
CMS Tracker Upgrade for High-Luminosity LHC

LHC


CMS
ATLAS
Gex
Grilly
Cessy
Sauverny
Chavannes-des-Bois
Échenevex
Versonnex
Ségny
D 984C
A1
Maconnex
Crozet
Chevry
Bretigny
Omex
Collex-Bossy
D 35A
Ferney-Voltaire
Prévessin-Moëns
Sergy
Saint-Genis-Pouilly
Le Grand-Saconnex / Ferney
Genève Aéroport
Pregny-Chambésy
Le Grand-Saconnex
Meyrin
D884
Bourdigny-Dessus
Bourdigny
Satigny
Vernier / Meyrin
Vernier
Versoix
Genève

CMS DETECTOR

Total weight : 14,000 tonnes
Overall diameter : 15.0 m
Overall length : 28.7 m
Magnetic field : 3.8 T



STEEL RETURN YOKE
12,500 tonnes

SILICON TRACKERS
Pixel (100x150 μm) ~16m² ~66M channels
Microstrips (80x180 μm) ~200m² ~9.6M channels

SUPERCONDUCTING SOLENOID
Niobium titanium coil carrying ~18,000A

MUON CHAMBERS
Barrel: 250 Drift Tube, 480 Resistive Plate Chambers
Endcaps: 468 Cathode Strip, 432 Resistive Plate Chambers

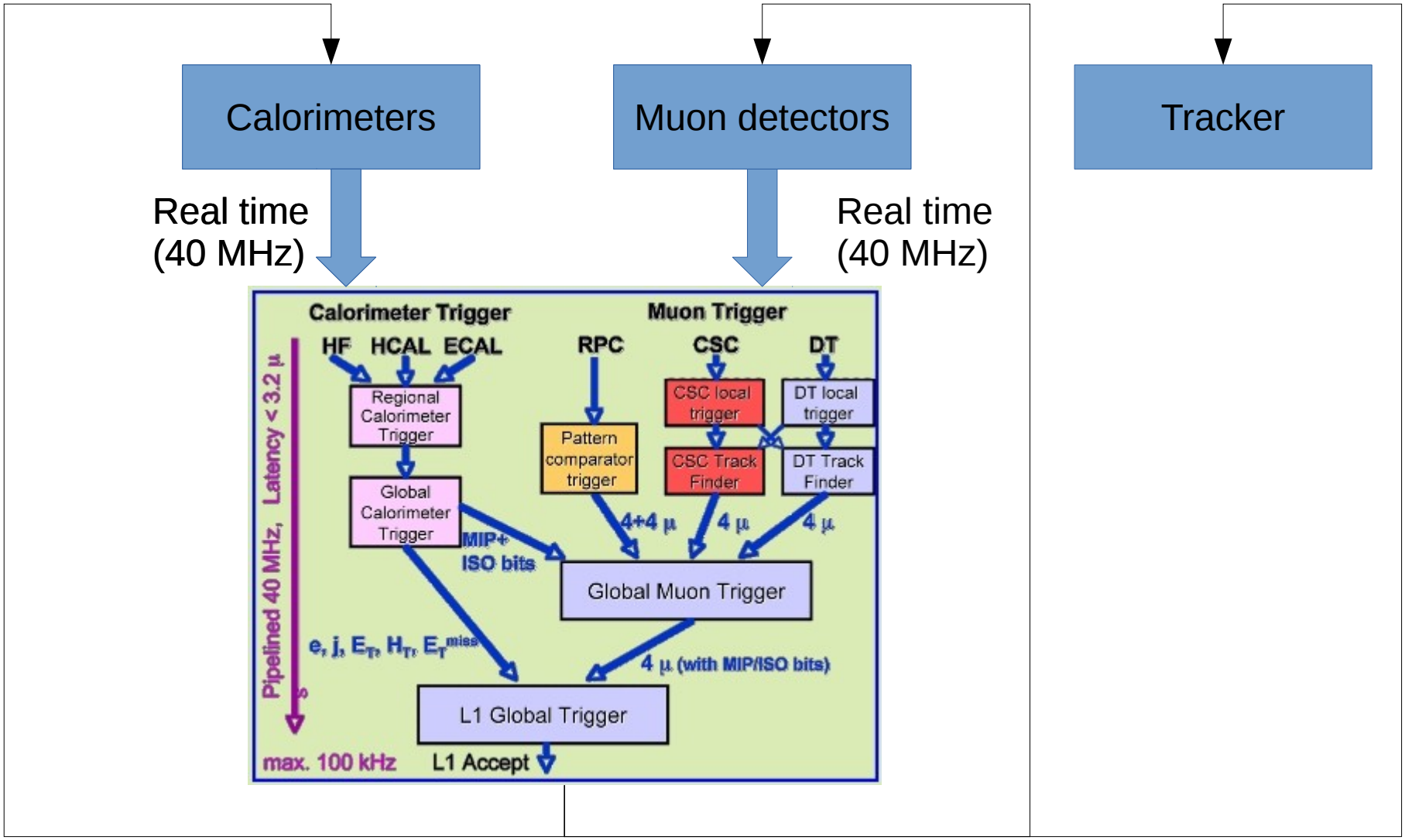
PRESHOWER
Silicon strips ~16m² ~137,000 channels

FORWARD CALORIMETER
Steel + Quartz fibres ~2,000 Channels

CRYSTAL ELECTROMAGNETIC CALORIMETER (ECAL)
~76,000 scintillating $PbWO_4$ crystals

HADRON CALORIMETER (HCAL)
Brass + Plastic scintillator ~7,000 channels

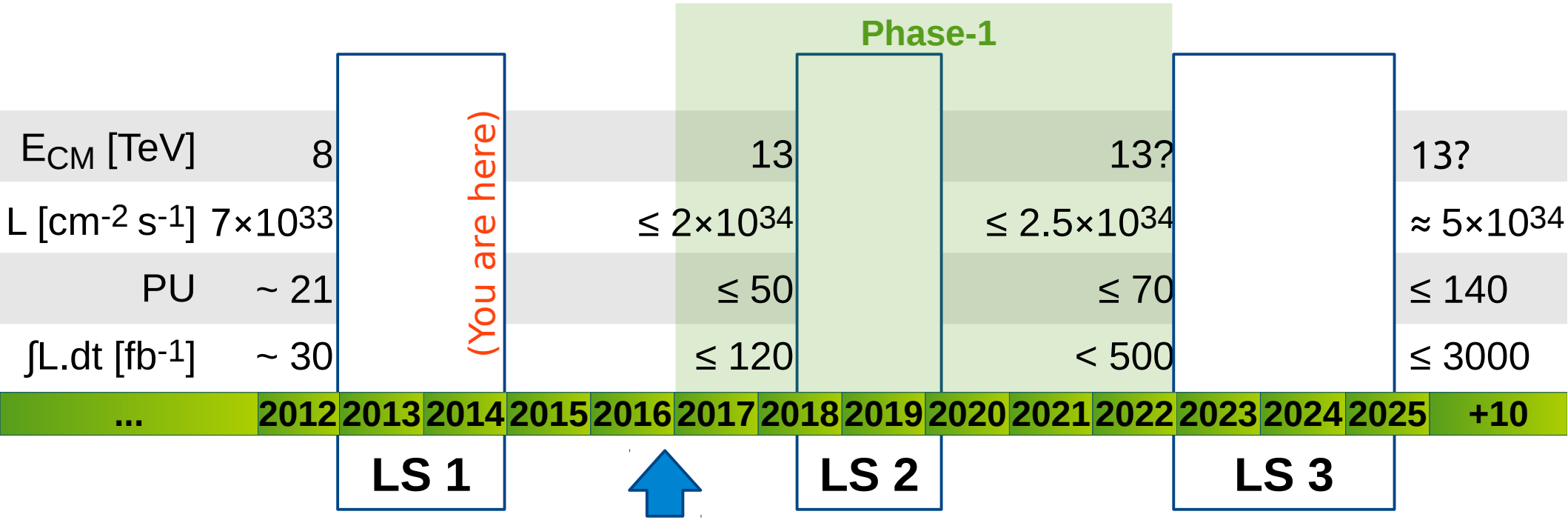
Current Readout Architecture



Current L1A rate ~ 100 kHz

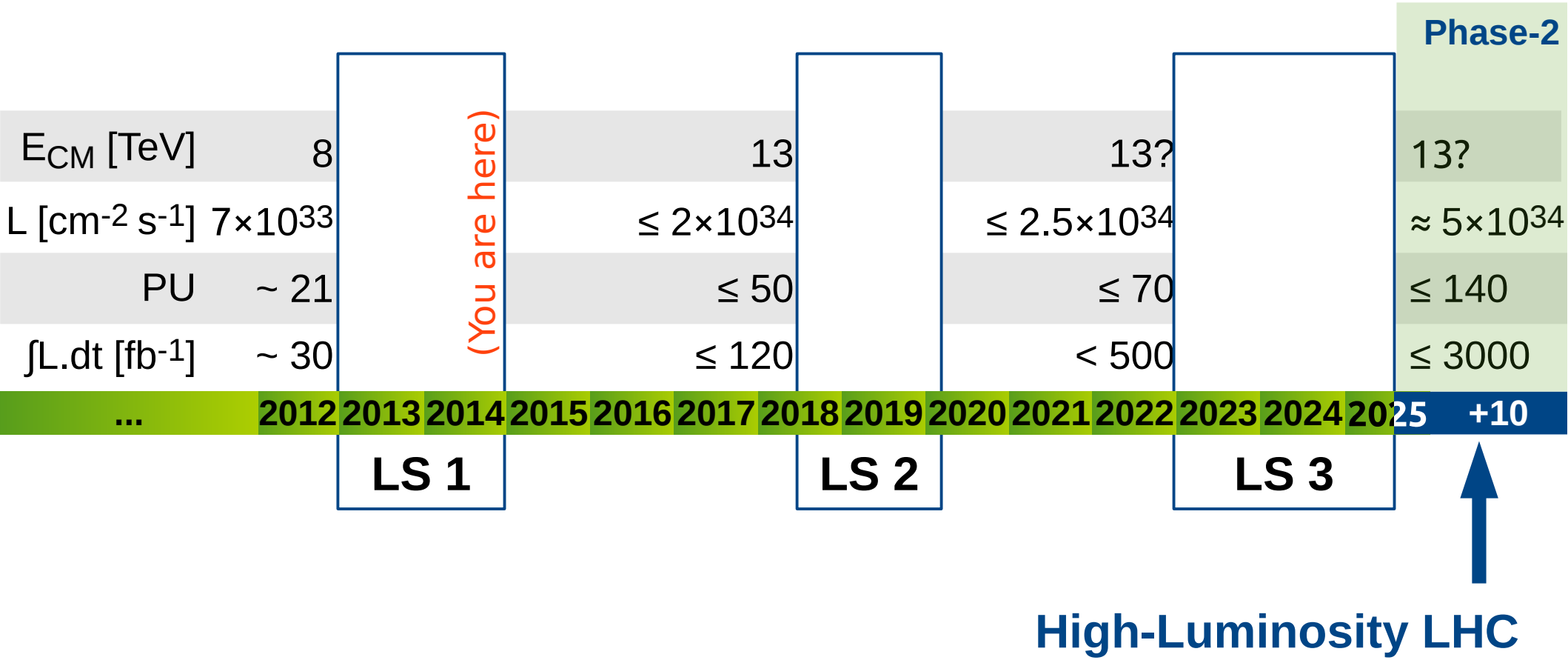
Trigger (a.k.a. Level-1 Trigger, a.k.a. Level-1 Accept, a.k.a. L1A)

LHC broad schedule

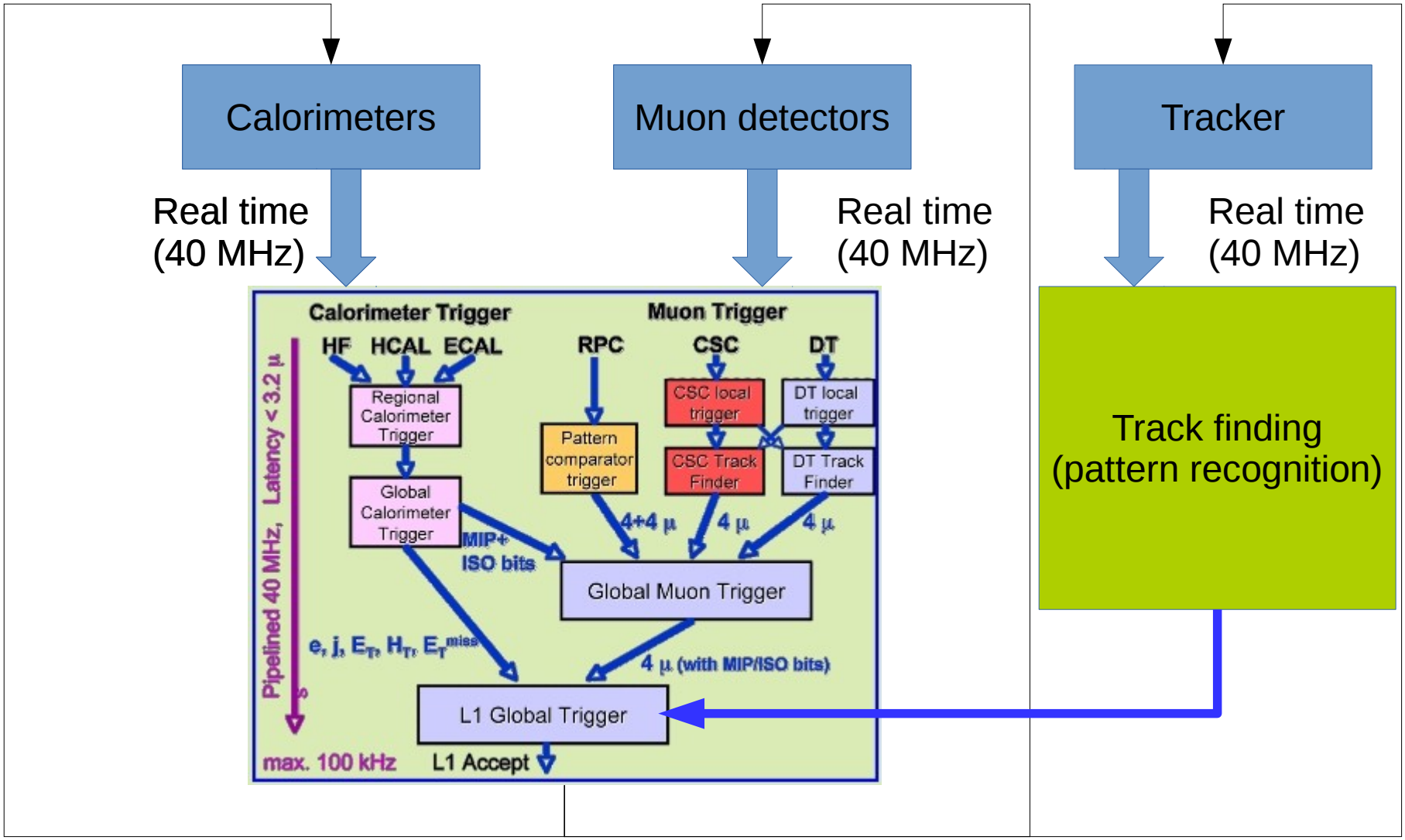


New CMS phase-1 pixel detector
installed during extended
winter shut-down

LHC broad schedule

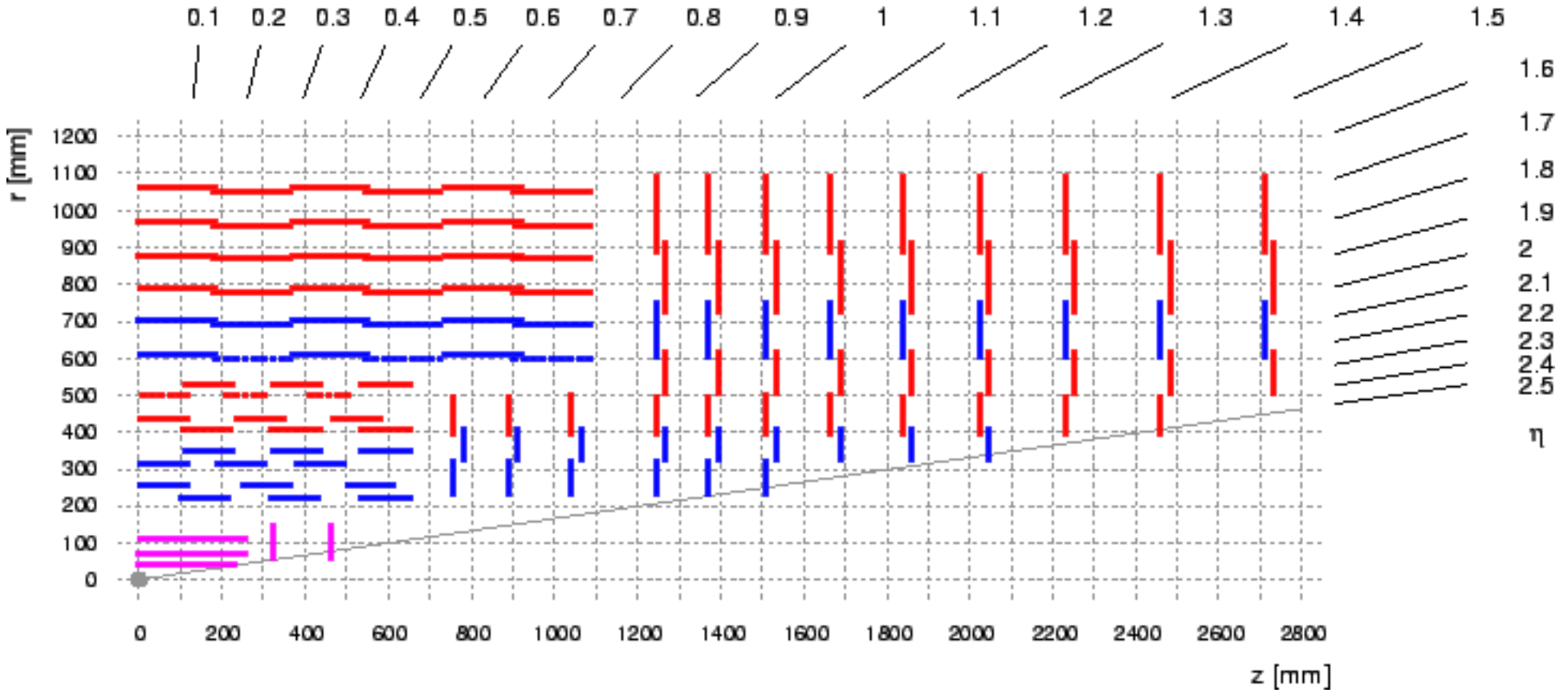


Upgrade Readout Architecture



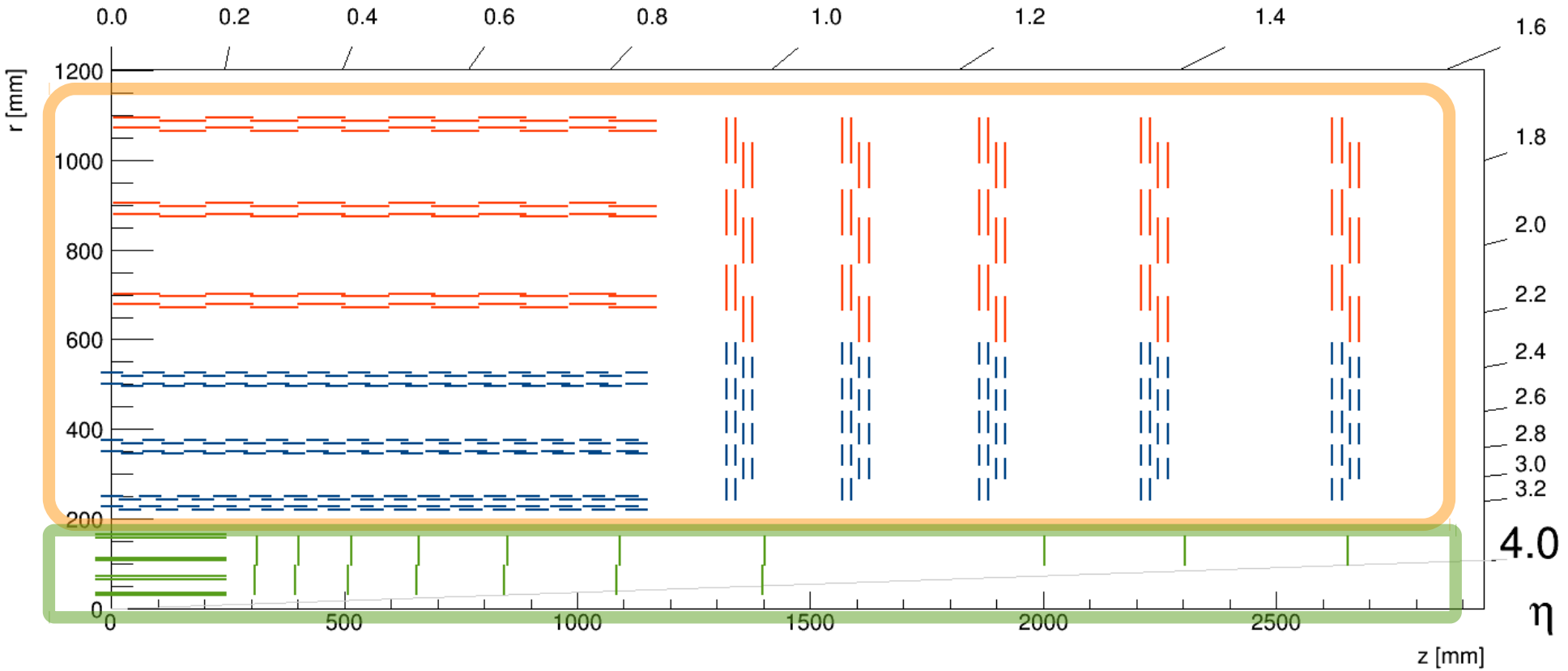
Upgrade L1A rate ~ 750 kHz

Current CMS Tracker



Upgraded Tracker Layout

Outer Tracker



Pixel detector

Outer tracker front-ends

Need to ship hits off detector

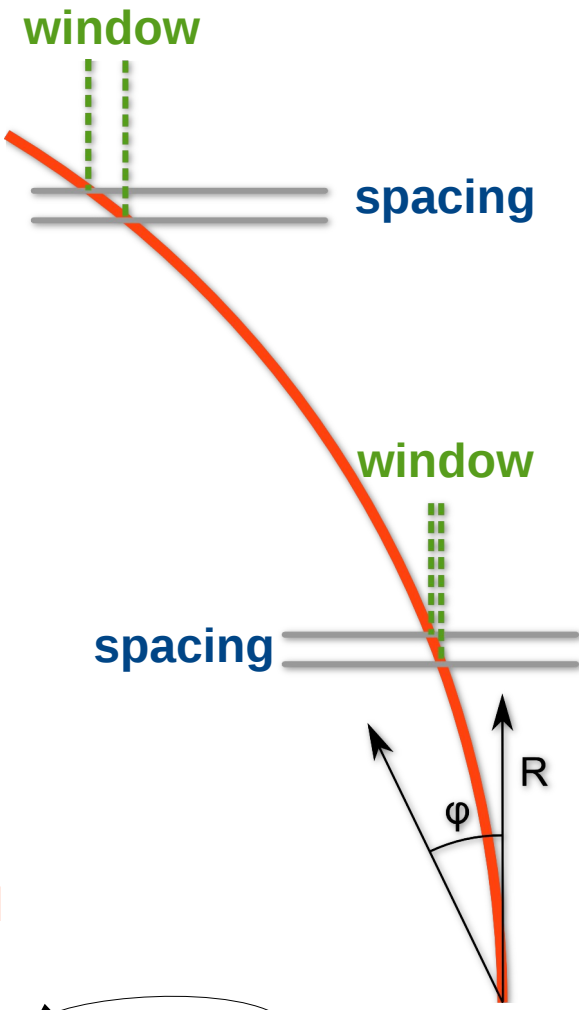
Ship all hits @ 40 MHz? No

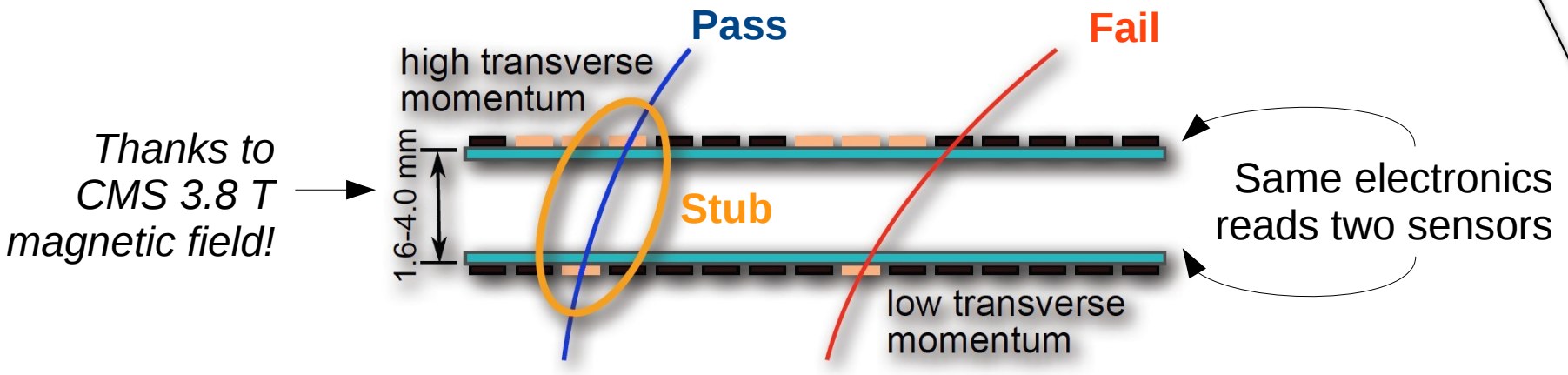
- Bandwidth needed: off by 1 order of magnitude (order of 10 Gbps per module)
- Track reconstruction ~ impossible

Solution: ship only high-pT hits (stubs)

- Threshold of ~ 2 GeV
- Data reduction of one order of magnitude or more

Modules with pT discrimination (“pT modules”)



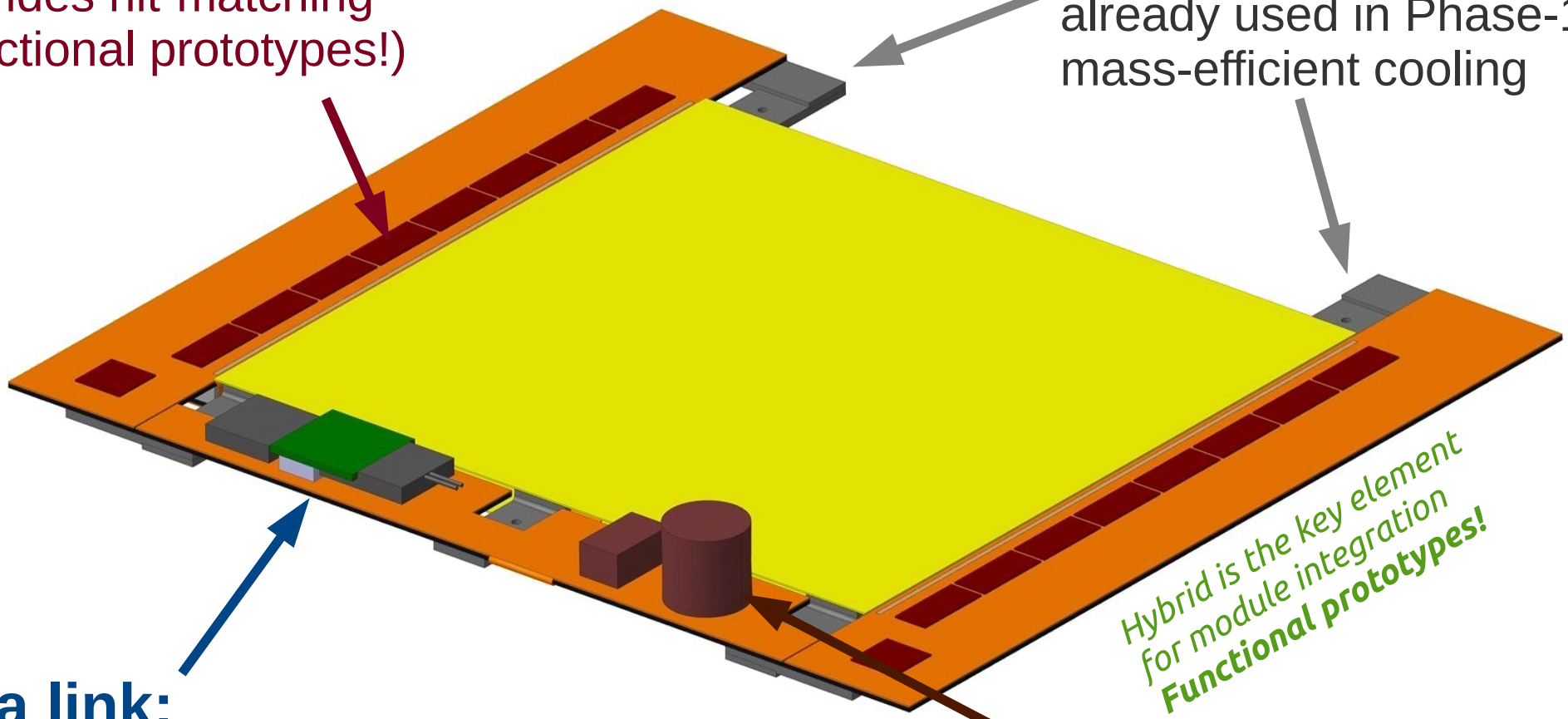


Module design

Integration at the module level

Binary readout: CBC
provides hit-matching
(functional prototypes!)

CO_2 cooling
already used in Phase-1
mass-efficient cooling



Hybrid is the key element for module integration ***Functional prototypes!***

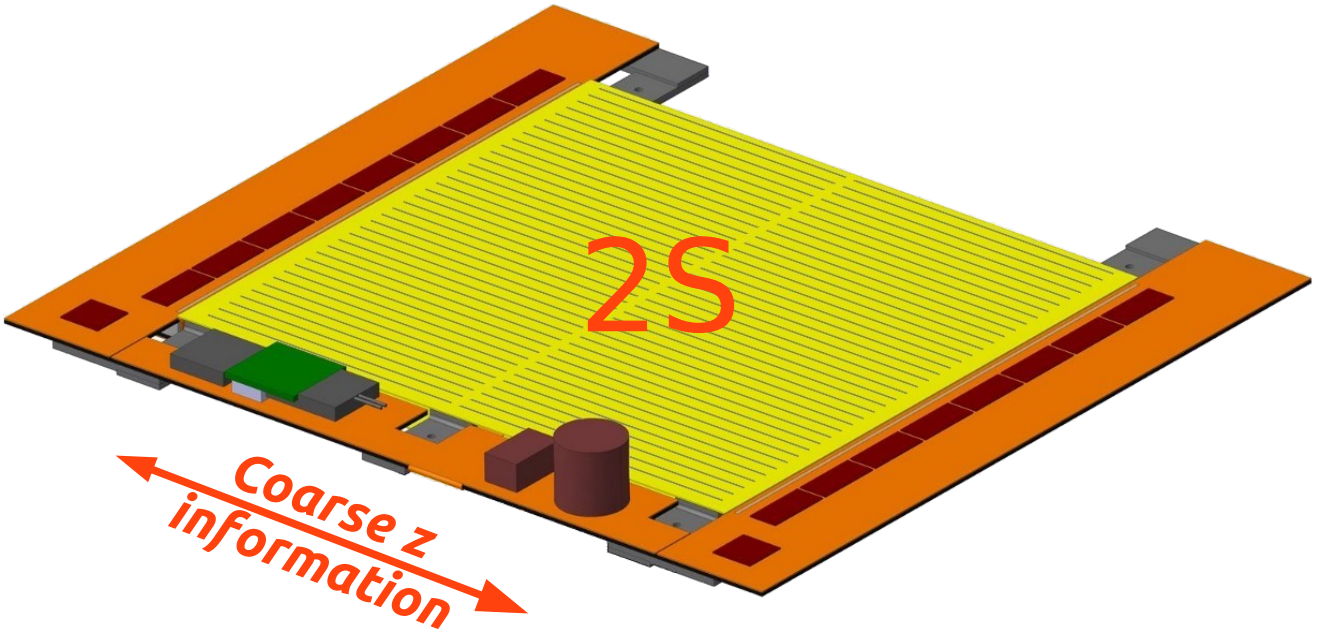
Data link:
Low-power GigaBit Transceiver
lpGBT currently under development
integrated at module level

DC/DC converter
already used in Phase-1
10 V lines: lower current, lower material

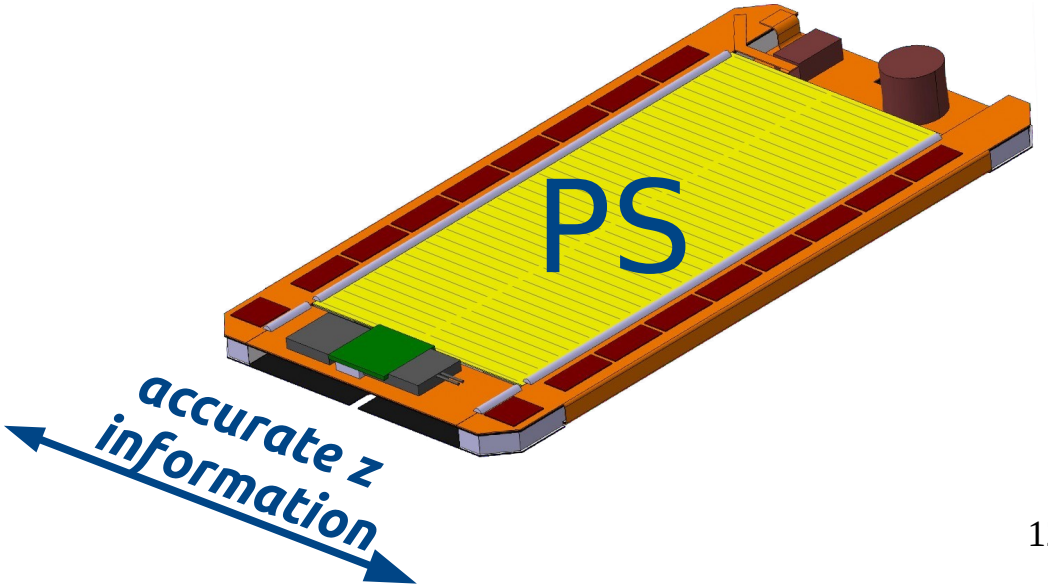
Module design

Only two module types

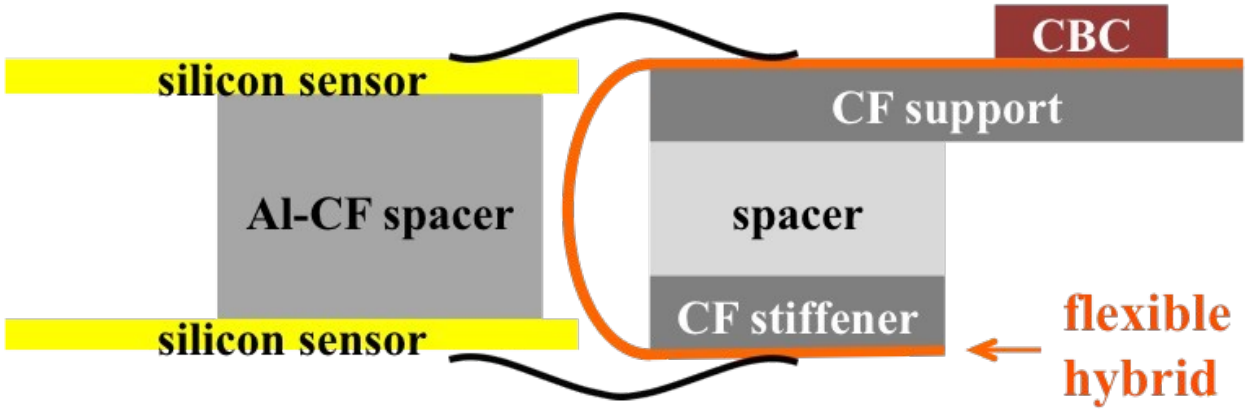
2 Strip sensors
Strips: 5 cm × 90 µm
Strips: 5 cm × 90 µm
P = 2.7 W
~ 92 cm^2 active area
For r > 40 cm

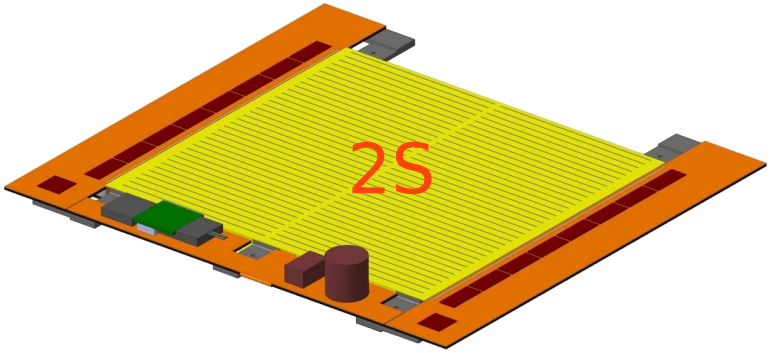


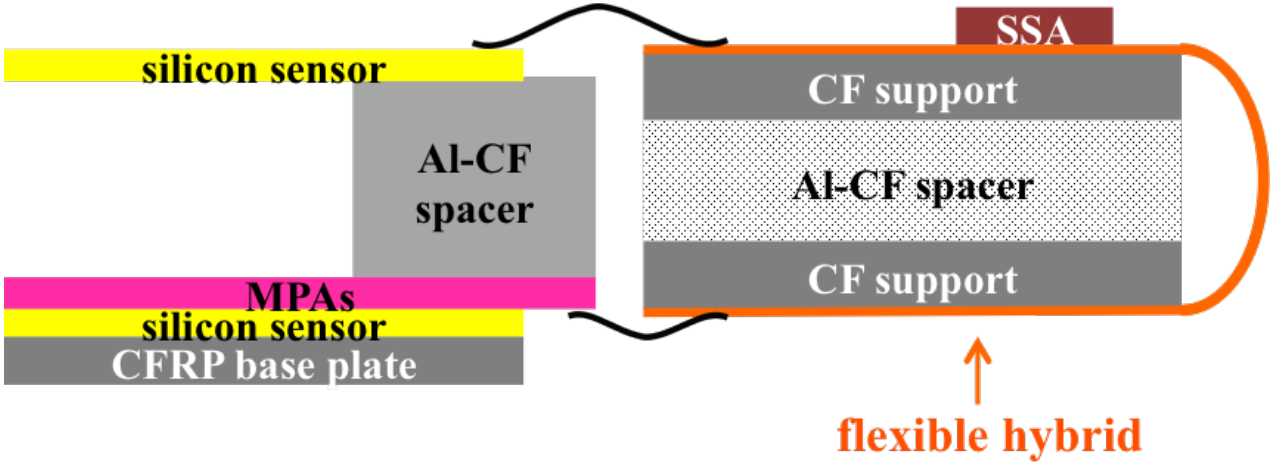
Pixel + **S**trip sensors
Strips: 2.5 cm × 100 µm
MacroPixels: 1.5 mm × 100 µm
P = 5.0 W
~ 44 cm^2 active area
For r > 20 cm

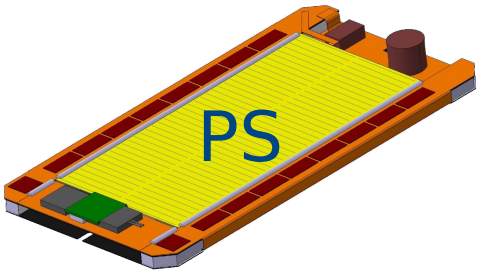


Front-end interconnection





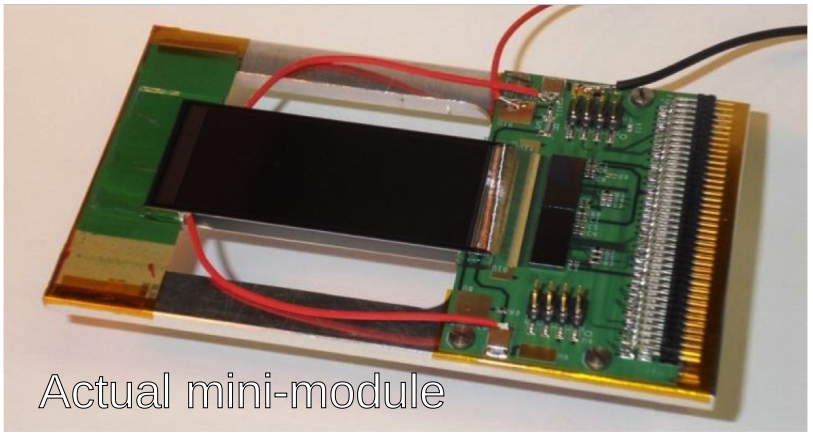




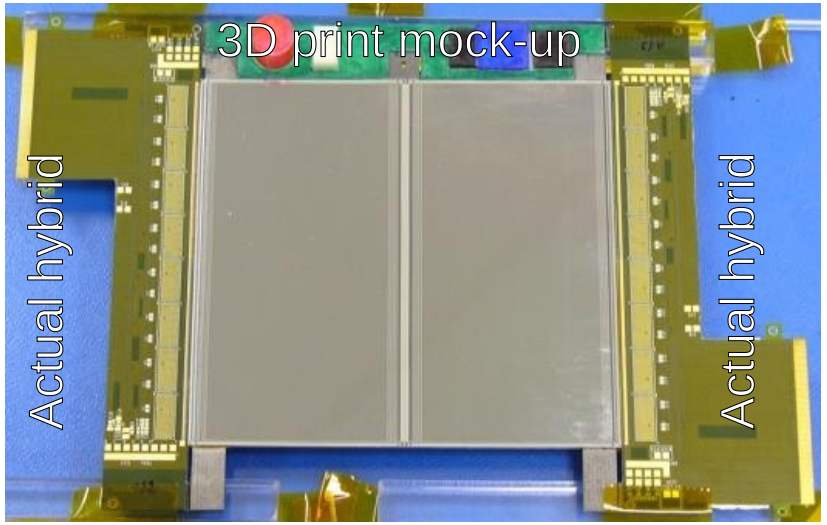
Flex hybrid:

- Technology leap
- Key element for 2-sensor design

Module prototypes



2xCBC functional module:
- 2 chips (instead of 8)
- Electrical readout (instead of optical)
- No data concentration
- Rigid hybrid
+ Stub-finding logic
+ Nominal noise and thresholds



8xCBC prototype:
+ 2x8 chips
- Electrical readout (instead of optical)
- No data concentration
+ Flex-hybrid
+ Stub-finding logic
  Just produced

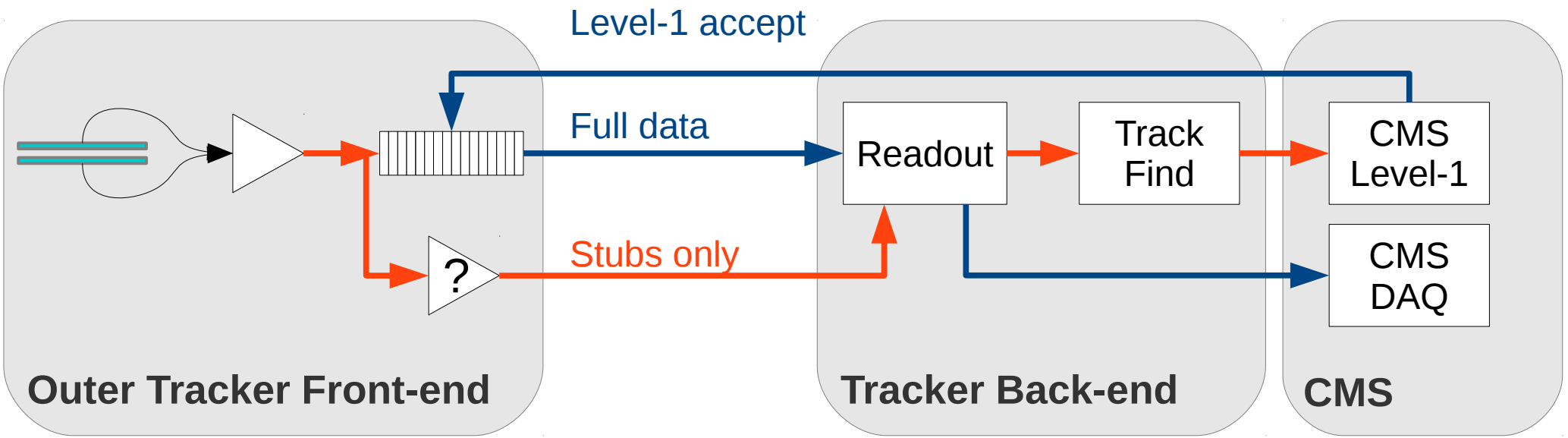
Prototype readout format **defined**

Data concentrator will be produced later fitting both PS and 2S modules

Providing tracks for trigger

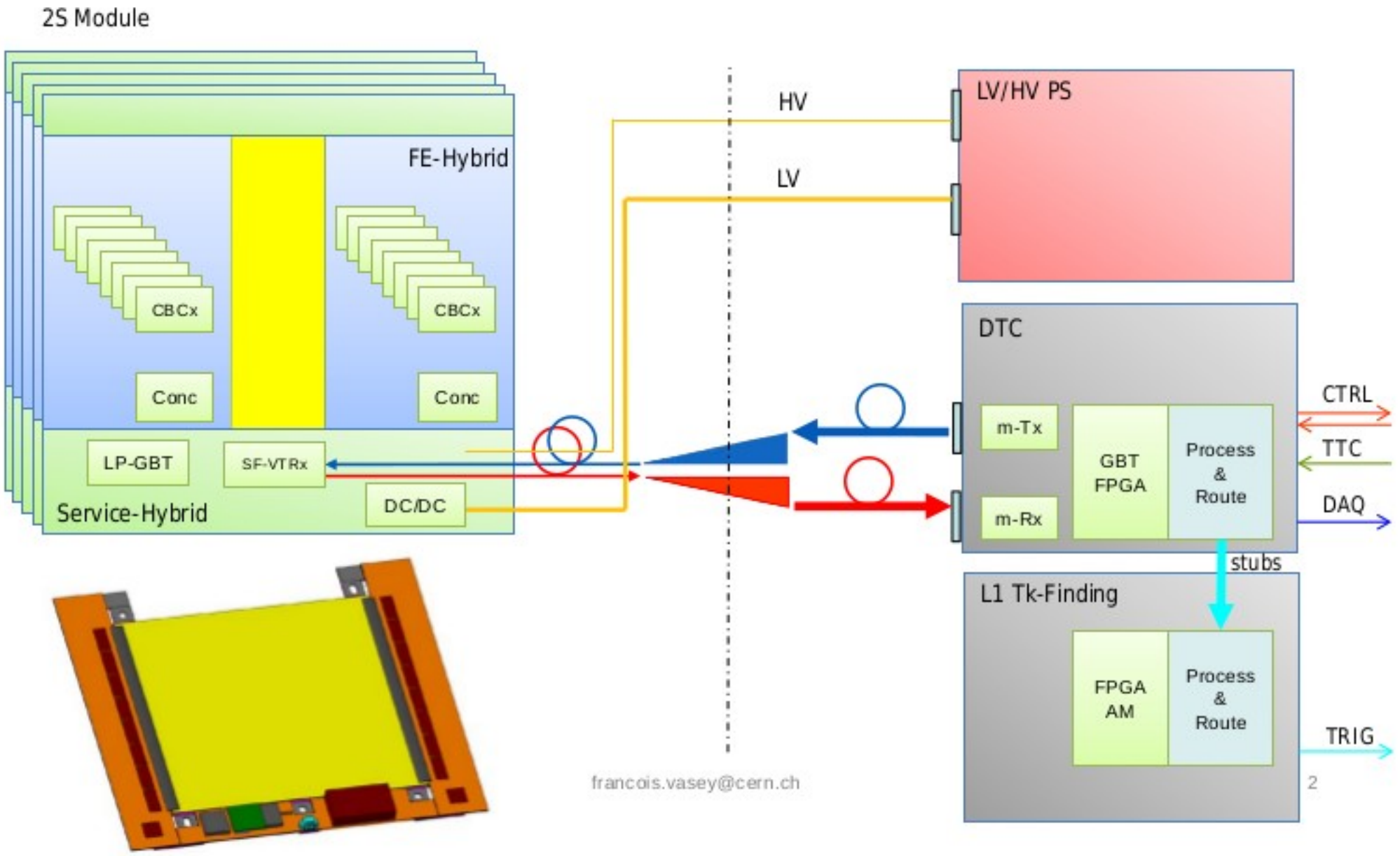
Level-1 “stubs” are processed in the back-end

Form Level-1 tracks, pT above ~ 2 GeV,
contributing to CMS Level-1 trigger



@ **40 MHz** – Bunch crossing
@ **750 kHz** – CMS Level-1 trigger

Electrical System Block Diagram, 2S



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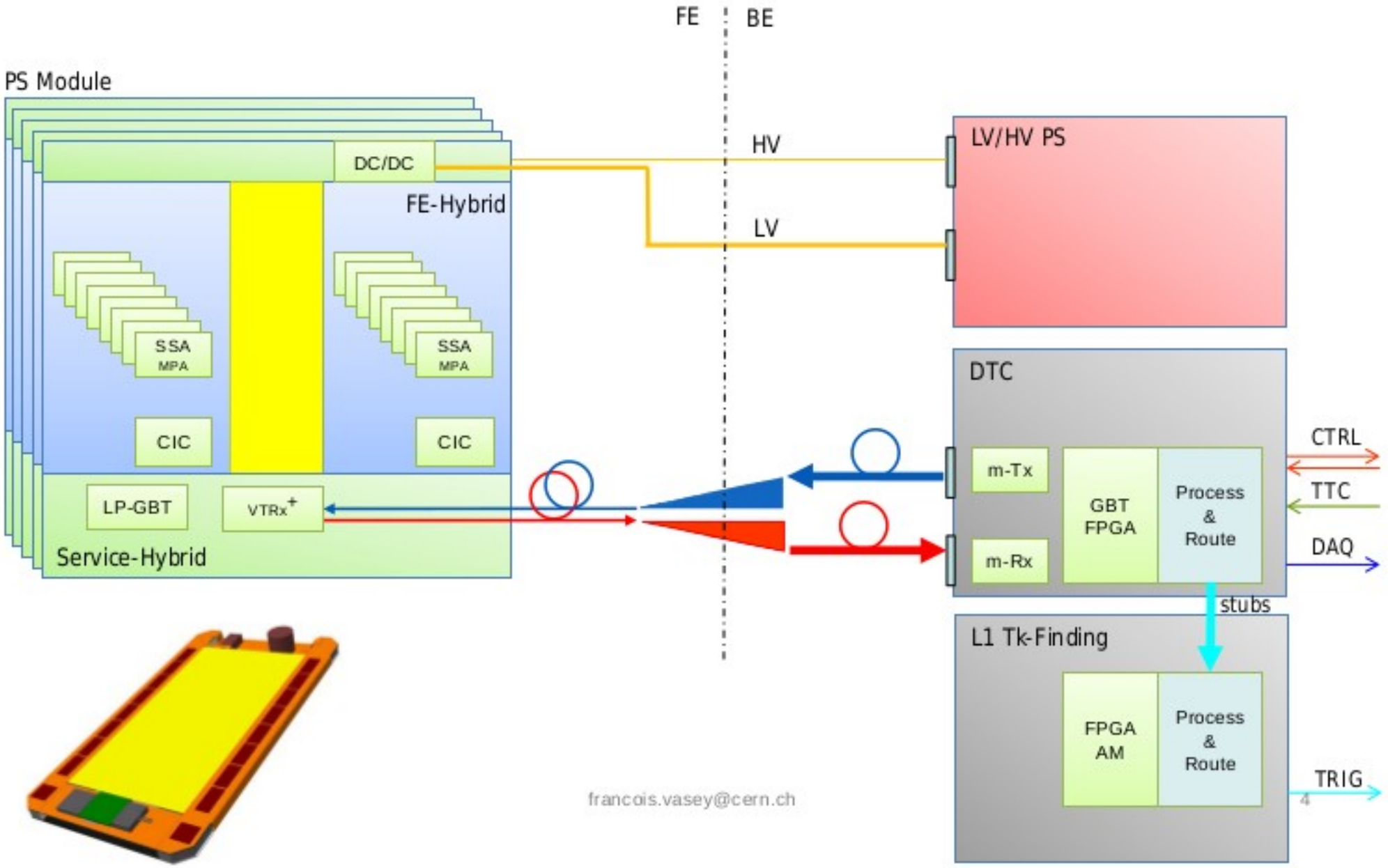
Electrical System Block Diagram, PS



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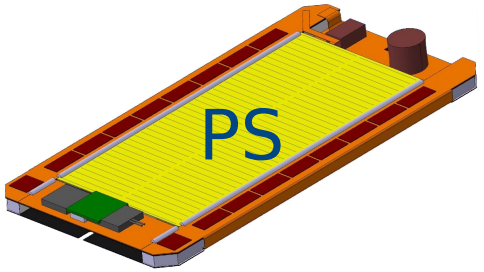
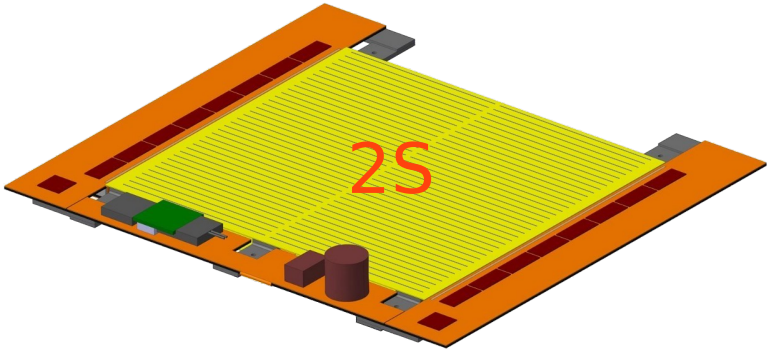
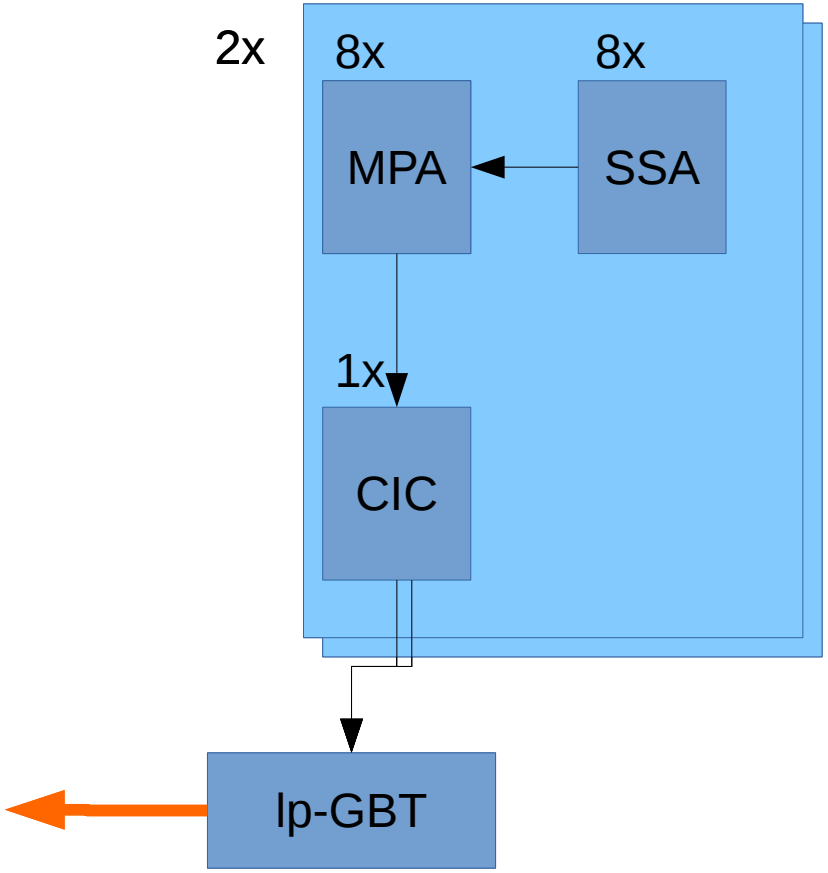
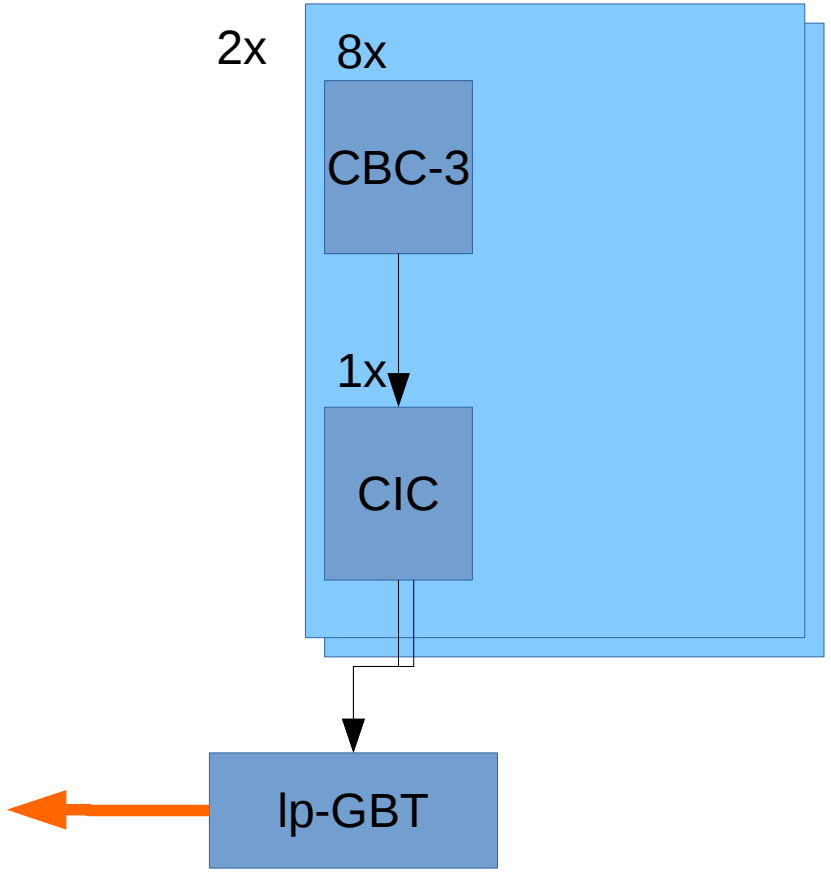
Module readout architecture









Parts for emulation

- Gather information on band-widths, based on specs of CBC-3, MPA, SSA, CIC
- Evaluate possibility to implement in one GLIB or in more GLIBS in the same shelf, using back-plane communication
  - Not necessary to implement full-speed simulation @40MHz
- MPA: existing VERILOG code (by CERN PH-ESE)
- SSA VERILOG will follow (by CERN PH-ESE)
- CBC-3 will not be implemented in VERILOG (a Verilog *simulation* will suffice). Chip from Imperial College, London
- CIC detailed model will arrive breifly (by group in Lyon)