

Virtex-6 FPGA Packaging and Pinout Specifications

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/24/2009	1.0	Initial Xilinx release.
10/08/2009	2.0	Added the Virtex-6 HXT devices throughout document. Updated description of VF_0S in Table 1-5 . Updated Figure 1-1 through Figure 1-5 with unbonded GTX banks. Updated from N/A to bank number all the transceiver banks in the Chapter 2 pinout tables. Updated all the I/O bank diagrams in Chapter 3 to include transceiver banks. Revised the FF1156, FF1759, and FF1760 mechanical drawings in Chapter 4 , including adding Note 5 to Figure 4-6, page 441 . Added thermal resistance data to Table 5-1, page 450 .
02/02/2010	2.1	Revised format of Table 1-3 and Table 1-4 for readability. Updated MRCC and SRCC in Table 1-6 . Clarified information in the Bank Numbering section. Added thermal resistance data to Table 5-1, page 450 .
02/23/2010	2.2	Added note 2 to bank 22 in Figure 1-2 . Added note 1 to banks 17, 21, 27, 28, 37, and 38 and note 2 to banks 10, 11, 18, 20, 30, and 31 to Figure 1-5 .
08/25/2010	2.3	Changed the A maximum dimension to 2.86 in Figure 4-1 : FF(G)484 package drawing and Figure 4-2 : FF(G)784 package drawing.

Date	Version	Revision
11/23/2011	2.4	<p>Updated the entire document to add the Defense-grade Virtex-6Q (XQ) FPGAs. Revised the pinout diagrams to correctly call out the MGTHAVTT: Figure 3-9, Figure 3-21, Figure 3-23, and Figure 3-25. The actual package files are unchanged. Added thermal resistance data to Table 5-1, page 450.</p>
12/04/2014	2.5	<p>Added a discussion on ULA materials on page 11. Revised description of VBATT_0 in Table 1-6. Updated Notice of Disclaimer.</p> <p>In Chapter 5: Thermal Specifications, added a note on page 450 above Table 5-1 and also added the Heat Sink Removal Procedure, Package Pressure Handling Capacity, and Soldering Guidelines sections. Updated the links in References.</p> <p>In Chapter 6: Package Marking, added note on informational product change customer notice XCN11022: Product Marking Change.</p> <p>Added Chapter 7, Packing and Shipping.</p>

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About This Guide

This guide describes Virtex®-6 device pinouts and package specifications; it also includes pinout diagrams and thermal data.

Organization of This Guide

This document is comprised of the following chapters:

- [Chapter 1, Packaging Overview](#)
Provides an introduction to the Virtex-6 family with a summary of maximum I/Os available in each device/package combination. Also includes table of pin definitions.
- [Chapter 2, Pinout Tables](#)
Provides pinout information for all Virtex-6 devices and packages.
- [Chapter 3, Pinout and I/O Bank Diagrams](#)
Provides pinout diagrams for all Virtex-6 FPGA package/device combinations.
- [Chapter 4, Mechanical Drawings](#)
Provides mechanical drawings of Virtex-6 FPGA packages.
- [Chapter 5, Thermal Specifications](#)
Provides thermal data associated with Virtex-6 FPGA packages. Discusses Virtex-6 FPGA power management strategy and thermal management options.
- [Chapter 6, Package Marking](#)
Provides example and description of the marking on top of the package (topmark).
- [Appendix A, Recommended PCB Design Rules for BGA Packages](#)
Provides PCB design rules for BGA packages.

Additional Documentation

A complete suite of documentation is available for the commercial (XC) [Virtex-6 FPGAs](#) as well as specific documentation for the Defense-grade [Virtex-6Q FPGAs](#) (XQ).

Additional Support Resources

To search the database of silicon and software questions and answers, or to create a technical support case in WebCase, visit the following Xilinx website:

<http://www.xilinx.com/support>

Packaging Overview

Summary

This chapter covers the following topics:

- [Introduction](#)
- [Device/Package Combinations and Maximum I/Os](#)
- [Pin Definitions](#)
- [Die Level Bank Numbering and Clock Pins Overview](#)

Introduction

This section describes the pinouts for Virtex®-6 devices in the 1.00 mm pitch flip-chip fine-pitch BGA packages.

Virtex-6 devices are offered exclusively in high performance flip-chip BGA packages that are optimally designed for improved signal integrity and jitter. Package inductance is minimized as a result of optimal placement and even distribution as well as an increased number of Power and GND pins.

All of the devices supported in a particular package are pinout compatible and are listed in the same table (one table per package). Pins that are not available for the smaller devices are listed in the “No Connects” column of each table.

Each device is split into nine or more I/O banks to allow for flexibility in the choice of I/O standards. Global pins, including JTAG, configuration, and power/ground pins, are listed at the end of each table. [Table 1-6](#) provides definitions for all pin types.

For the latest Virtex-6 FPGA pinout information, check the Xilinx website for any updates to this document.

Virtex-6 device’s flip-chip assembly materials are manufactured using ultra-low alpha (ULA) materials defined as <0.002 cph/cm² or materials that emit less than 0.002 alpha-particles per square centimeter per hour.

Device/Package Combinations and Maximum I/Os

Table 1-1 shows the package specifications and the maximum number of user I/Os possible in Virtex-6 FPGA flip-chip packages. FF denotes flip-chip fine-pitch BGA (1.00 mm pitch). Specific information on device/package combinations by family is available at:

- [DS150: Virtex-6 Family Overview](#)
- [DS155: Defense-grade Virtex-6Q Family Overview](#)

Table 1-1: Flip-Chip Packages

Package Specifications	Packages								
	FF484	FF784 RF784	FF1154	FF1155	FF1156 RF1156	FF1759 RF1759	FF1760	FF1923	FF1924
Pitch (mm)	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
Size (mm)	23 x 23	29 x 29	35 x 35	35 x 35	35 x 35	42.5 x 42.5	42.5 x 42.5	45 x 45	45 x 45
Maximum I/Os	240	400	320	440	600	840	1200	720	640

The number of I/Os per package includes all user I/Os *except* the 26 pins listed in [Table 1-2](#).

Table 1-2: Virtex-6 FPGA I/O Pins in the Dedicated Configuration Bank (Bank0)

DXP_0	HSWAPEN_0	INIT_B_0	M0_0	VN_0	TDO_0	VREFN_0
DXN_0	DIN_0	CSI_B_0	M1_0	VP_0	TCK_0	VREFP_0
VBATT_0	DONE_0	RDWR_B_0	M2_0	DOUT_BUSY_0	TMS_0	AVSS_0
PROGRAM_B_0	CCLK_0			VFS_0	TDI_0	AVDD_0

Table 1-3 lists the quantity of GTX serial transceiver channels for the Virtex-6 LXT and SXT devices. **Table 1-4** lists the quantity of GTX/GTH serial transceiver channels for the Virtex-6 HXT devices. In all devices, a serial transceiver channel is one set of MGTRXP, MGTRXN, MGTTXP, and MGTTXN pins.

Table 1-3: Number of Serial Transceiver Channels (GTX) by Device/Package for the LXT and SXT Devices

Package	I/O Channels By Device ⁽¹⁾								
	LX75T	LX130T	LX195T	LX240T	LX365T	LX550T	LX760	SX315T	SX475T
FF484/FFG484	8	8							
FF784/FFG784	12	12	12	12					
FF1156/FFG1156		20	20	20	20			20	20
FF1759/FFG1759				24	24	36		24	36
FF1760/FFG1760						0	0		

Notes:

1. In all devices, a serial transceiver channel is one set of MGTRXP, MGTRXN, MGTTXP, and MGTTXN pins.

Table 1-4: Number of Serial Transceiver Channels (GTX/GTH) by Device/Package for the HXT Devices

Package	I/O Channels By Device ⁽¹⁾							
	HX250T		HX255T		HX380T		HX565T	
	GTX	GTH	GTX	GTH	GTX	GTH	GTX	GTH
FF1154/FFG1154	48	0			48	0		
FF1155/FFG1155			24	12	24	12		
FF1923/FFG1923			24	24	40	24	40	24
FF1924/FFG1924					48	24	48	24

Notes:

1. In all devices, a serial transceiver channel is one set of MGTRXP, MGTRXN, MGTTXP, and MGTTXN pins.

Table 1-5 shows the number of available I/Os and the number of differential I/O pairs for each Virtex-6 device/package combination. The RF packages are only used for the Virtex-6Q devices (XQ) at the end of the table.

Table 1-5: Available I/O Pin/Device/Package Combinations

Virtex-6 Device	User I/O Pins	Virtex-6 FPGA Package								
		FF484	FF784 RF784	FF1154	FF1155	FF1156 RF1156	FF1759 RF1759	FF1760	FF1923	FF1924
XC6VLX75T	Available User I/Os	240	360	—	—	—	—	—	—	—
	Differential I/O Pairs	120	180	—	—	—	—	—	—	—
XC6VLX130T	Available User I/Os	240	400	—	—	600	—	—	—	—
	Differential I/O Pairs	120	200	—	—	300	—	—	—	—
XC6VLX195T	Available User I/Os	—	400	—	—	600	—	—	—	—
	Differential I/O Pairs	—	200	—	—	300	—	—	—	—
XC6VLX240T	Available User I/Os	—	400	—	—	600	720	—	—	—
	Differential I/O Pairs	—	200	—	—	300	360	—	—	—
XC6VLX365T	Available User I/Os	—	—	—	—	600	720	—	—	—
	Differential I/O Pairs	—	—	—	—	300	360	—	—	—
XC6VLX550T	Available User I/Os	—	—	—	—	—	840	1200	—	—
	Differential I/O Pairs	—	—	—	—	—	420	600	—	—
XC6VLX760	Available User I/Os	—	—	—	—	—	—	1200	—	—
	Differential I/O Pairs	—	—	—	—	—	—	600	—	—
XC6VSX315T	Available User I/Os	—	—	—	—	600	720	—	—	—
	Differential I/O Pairs	—	—	—	—	300	360	—	—	—
XC6VSX475T	Available User I/Os	—	—	—	—	600	840	—	—	—
	Differential I/O Pairs	—	—	—	—	300	420	—	—	—
XC6VHX250T	Available User I/Os	—	—	320	—	—	—	—	—	—
	Differential I/O Pairs	—	—	160	—	—	—	—	—	—
XC6VHX255T	Available User I/Os	—	—	—	440	—	—	—	480	—
	Differential I/O Pairs	—	—	—	220	—	—	—	240	—
XC6VHX380T	Available User I/Os	—	—	320	440	—	—	—	720	640
	Differential I/O Pairs	—	—	160	220	—	—	—	360	320
XC6VHX565T	Available User I/Os	—	—	—	—	—	—	—	720	640
	Differential I/O Pairs	—	—	—	—	—	—	—	360	320

Table 1-5: Available I/O Pin/Device/Package Combinations (Cont'd)

Virtex-6 Device	User I/O Pins	Virtex-6 FPGA Package								
		FF484	FF784 RF784	FF1154	FF1155	FF1156 RF1156	FF1759 RF1759	FF1760	FF1923	FF1924
XQ6VLX130T	Available User I/Os	-	400	-	-	600	-	-	-	-
	Differential I/O Pairs	-	200	-	-	300	-	-	-	-
XQ6VLX240T	Available User I/Os	-	400	-	-	600	720	-	-	-
	Differential I/O Pairs	-	200	-	-	300	360	-	-	-
XQ6VLX550T	Available User I/Os	-	-	-	-	-	840	-	-	-
	Differential I/O Pairs	-	-	-	-	-	420	-	-	-
XQ6VSX315T	Available User I/Os	-	-	-	-	600	720	-	-	-
	Differential I/O Pairs	-	-	-	-	300	360	-	-	-
XQ6VSX475T	Available User I/Os	-	-	-	-	600	840	-	-	-
	Differential I/O Pairs	-	-	-	-	300	420	-	-	-

Pin Definitions

Table 1-6 lists the pin definitions used in Virtex-6 FPGA packages.

Table 1-6: Virtex-6 FPGA Pin Definitions

Pin Name	Direction	Description
User I/O Pins		
IO_LXXY_#	Input/ Output	<p>All user I/O pins are capable of differential signaling and can implement pairs. Each user I/O is labeled IO_LXXY_#, where:</p> <ul style="list-style-type: none"> • IO indicates a user I/O pin. • LXXY indicates a differential pair, with XX a unique pair in the bank and Y = [P N] for the positive/negative sides of the differential pair.
Multi-Function Pins		
IO_LXXY_ZZZ_#		Multi-function pins are labelled IO_LXXY_ZZZ_#, where ZZZ represents one or more of the following functions in addition to being general purpose user I/O. If not used for their special function, these pins can be user I/O.
Dn	Input	In SelectMAP mode, D0 through D31 are configuration data pins. These pins become user I/Os after configuration, unless the SelectMAP port is retained. In BPI mode, D0 through D15 are configuration data-input pins.
An	Output	Address A0–A25 BPI address output. These pins become user I/O after configuration.
RSn	Output	RS0 and RS1 revision select output.
FCS_B	Output	BPI and SPI flash chip select.
FOE_B_MOSI	Output	BPI flash output enable or SPI data-master output, slave input.
FWE_B	Output	BPI flash write enable.
CSO_B	Output	Parallel daisy chain chip select.
FSn	Input	FS0–FS2 SPI flash vendor selection.
SRCC	Input	These are the clock capable I/Os driving BUFRs, BUFIOs, and MMCMs. These pins become regular user I/Os when not needed for clocks. If a single-ended clock is connected to the differential CC pair of pins, it must be connected to the positive (P) side of the pair. The SRCC (single region) pins can drive two BUFIOs in a single bank. Only CC pins in the inner I/O columns can connect to the MMCMs and BUFGs.
MRCC	Input	These are the clock capable I/Os driving BUFRs, BUFIOs, and MMCMs. These pins become regular user I/Os when not needed for clocks. If a single-ended clock is connected to the differential CC pair of pins, it must be connected to the positive (P) side of the pair. The MRCC (multi-region) pins can drive two BUFIOs spanning the banks above and below. Only CC pins in the inner I/O columns can connect to the MMCMs and BUFGs.
GC	Input	These clock pins connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks. If a single-ended clock is connected to the differential GC pair of pins, it must be connected to the positive (P) side of the pair.
SMnP/SMnN	Input	System Monitor auxiliary analog inputs 0–15.

Table 1-6: Virtex-6 FPGA Pin Definitions (Cont'd)

Pin Name	Direction	Description
VREF	N/A	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
VRN	N/A	This pin is for the DCI voltage reference resistor of N transistor (per bank, to be pulled High with reference resistor).
VRP	N/A	This pin is for the DCI voltage reference resistor of P transistor (per bank, to be pulled Low with reference resistor).
Dedicated Configuration Pins ⁽¹⁾		
CCLK_0	Input/Output	Configuration clock. Output and input in Master mode or Input in Slave mode.
CSI_B_0	Input	In SelectMAP mode, this is the active-low Chip Select signal.
DIN_0	Input	In bit-serial modes, DIN is the single-data input.
DONE_0	Input/Output	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence.
DOUT_BUSY_0	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. In bit-serial modes, DOUT gives preamble and configuration data to downstream devices in a daisy chain.
HSWAPEN_0	Input	Enable I/O pullups during configuration
INIT_B_0	Bidirectional (open-drain)	When Low, this pin indicates that the configuration memory is being cleared. When held Low, the start of configuration is delayed. During configuration, a Low on this output indicates that a configuration data error has occurred.
M0_0, M1_0, M2_0	Input	Configuration mode selection
PROGRAM_B_0	Input	Active Low asynchronous reset to configuration logic. This pin has a permanent weak pull-up resistor.
RDWR_B_0	Input	In SelectMAP mode, this is the active-low Write Enable signal.
TCK_0	Input	Boundary-Scan Clock.
TDI_0	Input	Boundary-Scan Data Input.
TDO_0	Output	Boundary-Scan Data Output.
TMS_0	Input	Boundary-Scan Mode Select.
DXP_0, DXN_0	N/A	Temperature-sensing diode pins (Anode: DXP; Cathode: DXN).
Other Pins		
GND	N/A	Ground.
VBATT_0	N/A	Decryptor key memory backup supply; this pin should be tied to VCCAUX or GND when not used.
VCCAUX	N/A	Power-supply pins for auxiliary circuits.
VCCINT	N/A	Power-supply pins for the internal core logic.
VCCO_# ⁽²⁾	N/A	Power-supply pins for the output drivers (per bank).

Table 1-6: Virtex-6 FPGA Pin Definitions (*Cont'd*)

Pin Name	Direction	Description
VFS_0	Input	e power supply pin for programming. When not used, connect to GND.
Dedicated System Monitor Pins		
AVDD_0 ⁽³⁾	N/A	System Monitor's ADC analog positive supply voltage. Default connection is to V _{CCAUX} .
AVSS_0 ⁽³⁾	N/A	System Monitor's ADC analog ground reference. Default connection is to system GND via a ferrite bead.
VP_0 ⁽³⁾	Input	System Monitor dedicated differential analog input (positive side).
VN_0 ⁽³⁾	Input	System Monitor dedicated differential analog input (negative side).
VREFP_0 ⁽³⁾	N/A	1.25V reference input. Default connection is AVSS to enable the on-chip reference.
VREFN_0 ⁽³⁾	N/A	1.25V reference GND reference. Default connection is AVSS to enable the on-chip reference.
RocketIO Serial Transceiver Pins (GTXE1 and GTHE1_QUAD)		
MGTRXP[0:3]	Input	Positive differential receive port.
MGTRXN[0:3]	Input	Negative differential receive port.
MGTTXP[0:3]	Output	Positive differential transmit port.
MGTTXN[0:3]	Output	Negative differential transmit port.
MGTAVCC MGTAVCC_N MGTAVCC_S	N/A	Power-supply pin for GTXE1 transceiver's mixed-signal circuitry and PLLs ⁽⁴⁾ . Only available in Virtex-6 LXT and SXT devices.
MGTAVTT MGTAVTT_N MGTAVTT_S	N/A	Power-supply pin for GTXE1 transceiver's TX and RX circuitry. ⁽⁴⁾ . Only available in Virtex-6 LXT and SXT devices.
MGTAVCC_LN	N/A	Power-supply pin for transceiver mixed-signal circuitry left/north. Virtex-6 HXT devices only.
MGTAVCC_LS	N/A	Power-supply pin for transceiver mixed-signal circuitry left/south. Virtex-6 HXT devices only.
MGTAVCC_RN	N/A	Power-supply pin for transceiver mixed-signal circuitry right/north. Virtex-6 HXT devices only.
MGTAVCC_RS	N/A	Power-supply pin for transceiver mixed-signal circuitry right/south. Virtex-6 HXT devices only.
MGTAVTT_LN	N/A	Power-supply pin for TX and RX circuitry left/north. Virtex-6 HXT devices only.
MGTAVTT_LS	N/A	Power-supply pin for TX and RX circuitry left/south. Virtex-6 HXT devices only.
MGTAVTT_RN	N/A	Power-supply pin for TX and RX circuitry right/north. Virtex-6 HXT devices only.
MGTAVTT_RS	N/A	Power-supply pin for TX and RX circuitry right/south. Virtex-6 HXT devices only.

Table 1-6: Virtex-6 FPGA Pin Definitions (Cont'd)

Pin Name	Direction	Description
MGTHAVCC	Input	Analog supply for the receiver and transmitter internal circuits. In Virtex-6 HXT devices containing GTH transceivers.
MGTHAVCCRX	Input	Analog supply for the PLL and the receiver equalizers. In Virtex-6 HXT devices containing GTH transceivers.
MGTHAVTT	Input	Analog supply for the transmit driver. In Virtex-6 HXT devices containing GTH transceivers.
MGTHAVCCPLL	Input	Analog supply for the reference clock buffer and the PLL. In Virtex-6 HXT devices containing GTH transceivers.
MGTHAGND	Input	GND reference for the GTH transceiver internal circuitry. These pins should be connected to the PCB power supply GND reference plane. In Virtex-6 HXT devices containing GTH transceivers.
MGTREFCLKP	Input	GTH Quad positive differential reference clock. In Virtex-6 HXT devices containing GTH transceivers.
MGTREFCLKN	Input	GTH Quad negative differential reference clock. In Virtex-6 HXT devices containing GTH transceivers.
MGTREFCLK0/1P	Input	GTXE1 positive differential reference clock.
MGTREFCLK0/1N	Input	GTXE1 negative differential reference clock.
MGTAVTTRCAL	N/A	Precision reference resistor pin for internal calibration termination. Always located in Bank 115. ⁽⁴⁾
MGTRREF	Input	Precision reference resistor pin for internal calibration termination. Always located in Bank 115. ⁽⁴⁾
MGTRBIAS	Input	Internal precision current, voltage, and resistor references for the GTH Quad. Connect this pin to a 1KΩ resistor with the other terminal of the resistor connected to GND. In Virtex-6 HXT devices containing GTH transceivers.
RSVD	N/A	Reserved. No Connection; leave floating. In Virtex-6 HXT devices containing GTH transceivers.

Notes:

1. All dedicated pins (JTAG and configuration) are powered by V_{CC_CONFIG} (V_{CC_0}).
2. V_{CCO} pins in unbonded banks must be connected to the V_{CCO} for that bank for package migration. Do NOT connect unbonded V_{CCO} pins to different supplies. Without a package migration requirement, V_{CCO} pins in unbonded banks can be left unconnected or tied to a common supply (V_{CC} or ground).
3. For more information on connecting the System Monitor pins, see *Virtex-6 FPGA System Monitor User Guide*.
4. The FF484 and FF784 contain MGTAVCC and MGTAVTT pins. All other packages contain MGTAVCC_N/_S pins. All the respective MGTAV* supply pins are connected via planes in the package to the GTXs. The MGTAVCC and MGTAVTT supply all GTXs in a device. The MGTAVCC_N and MGTAVTT_N supply all GTXs in the upper half (North) and MGTAVCC_S and MGTAVTT_S supply all GTXs in the lower half (South). If no GTXs are used in the lower half, then the *_S supply pins can be connected to GND. All *_N pins must always be connected to a supply because the calibration resistor resides in the upper half of the part (bank_115). For more information consult the *Virtex-6 FPGA RocketIO GTX Transceiver User Guide*.

Die Level Bank Numbering and Clock Pins Overview

Figure 1-1 through Figure 1-11 visually describe a die view of the FPGA bank numbering. Table 1-7 shows the I/O bank names and locations. Not all banks are bonded out in every part/package combination.

Table 1-7: Virtex-6 FPGA Bank Numbering

Bank Name	Location	Description
IOCL	I/O center, left bank column	Available in every device.
IOCR	I/O center, right bank column	Available in every device.
IOOL	I/O outer, left bank column	Only available in all LX, LXT, and SXT devices.
IOOR	I/O outer, right bank column	Device dependent, for LX, LXT, and SXT devices only.

Bank 0

- The center column contains Bank 0.
- Bank 0 contains dedicated configuration pins.
- Bank 0 is filled with CLB_LLs on the top and bottom.
- The CMT (MMCM) column is adjacent to the right.

Horizontal Clock Row—HROW

- HROW contains all clock tracks.
- HROW is located in the center of a region/bank.

GTX/GTH Transceiver Bank Columns

- One bank contains quad GTX or GTH transceiver banks which equals four GTXE1 primitives or one GTHE1_QUAD primitive.
- In the LXT and SXT devices there is a single GTX column and the physical XY locations for the GTXE1 transceivers always start at location X0Y0 with the lowest bank number and then increment by one in the vertical Y direction for each GTXE1 transceiver (four Y locations for each quad).
- Some HXT devices have two transceiver columns that can contain GTX and/or GTH transceivers. The physical XY locations for the GTXE1 transceivers always start at location X0Y0 and X1Y0 with the lowest bank number and then increment by one in the vertical Y direction for each GTXE1 transceiver (four Y locations for each quad). When present, GTHE1 transceivers are organized (instantiated) as quads under the GTHE1_QUAD primitive and start at X0Y0 or X1Y0 (one location for four GTH transceivers).
- The physical XY locations for each IDELAYCNTRL start at X0Y0 in the bottom left-most bank and then increment by one starting with the lowest bank number in each column in the vertical Y direction and by one for each column in the horizontal X direction. IDELAYCNTRLs are located in each of the HROWS.

Clocks

- Every bank has four clock-capable (CC) pin pairs driving four BUFIos and/or four BUFRs (including inner columns).
- Inner-column CCs can also drive MMCMs in the same region. This is the highest performance connection.
- The eight global clock (GC) pin pairs are marked as with a •.
- There are two GC pairs each in banks 24, 25, 34, 35.
- GCs can connect to all MMCMs and BUFGs

Configuration and System Monitor

- Banks 24 and 34 always contain the dual purpose configuration pins (CFG).
- Bank 35 contains the System Monitor auxiliary inputs.
- Bank 0 contains the dedicated configuration pins.

Bank Numbering

[Figure 1-1](#) shows the I/O and transceiver banks for the XC6VLX75T. The black dots denote the global clock banks.

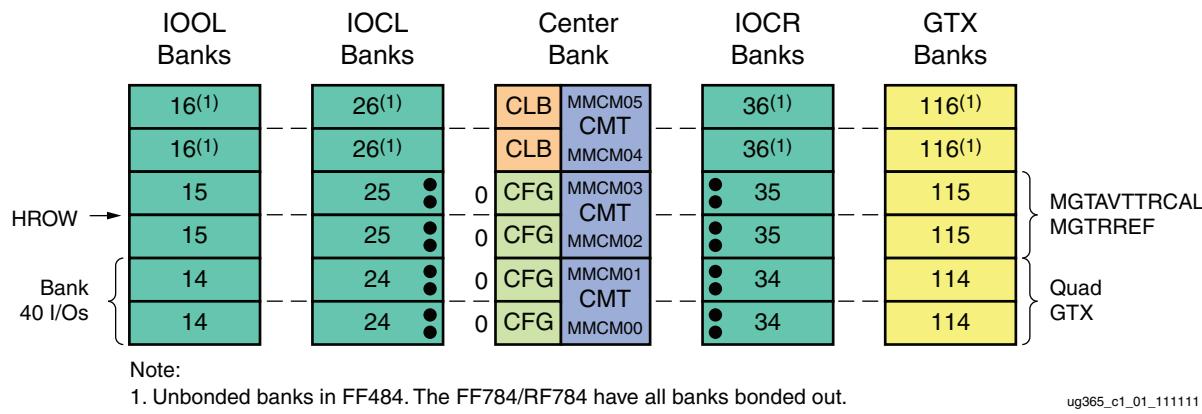
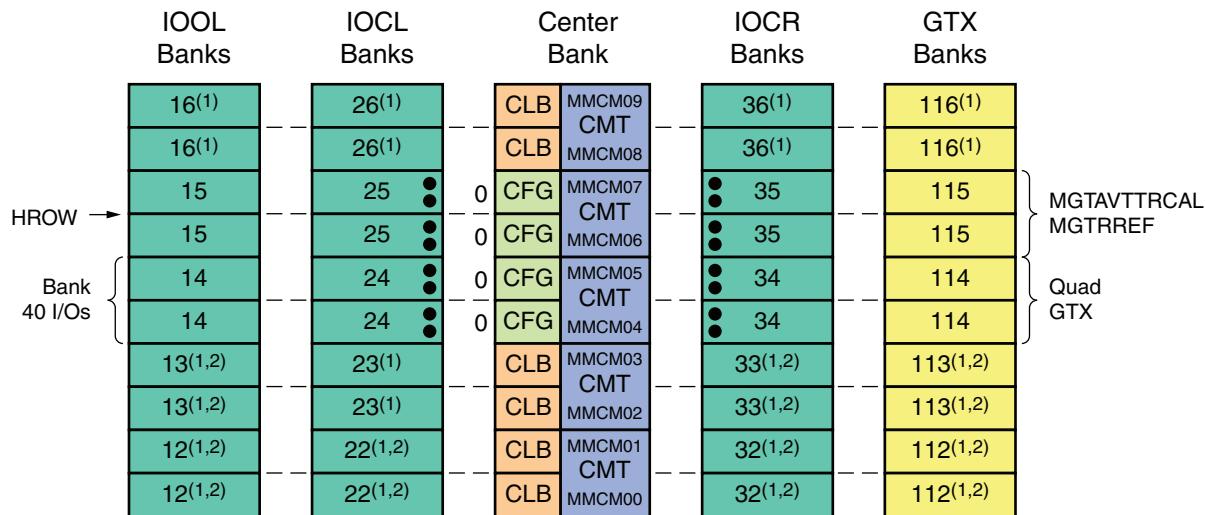


Figure 1-1: XC6VLX75T Banks

[Figure 1-2](#) shows the I/O and transceiver banks for the XC6VLX130T, XQ6VLX130T, and XC6VLX195T. The black dots denote the global clock banks.



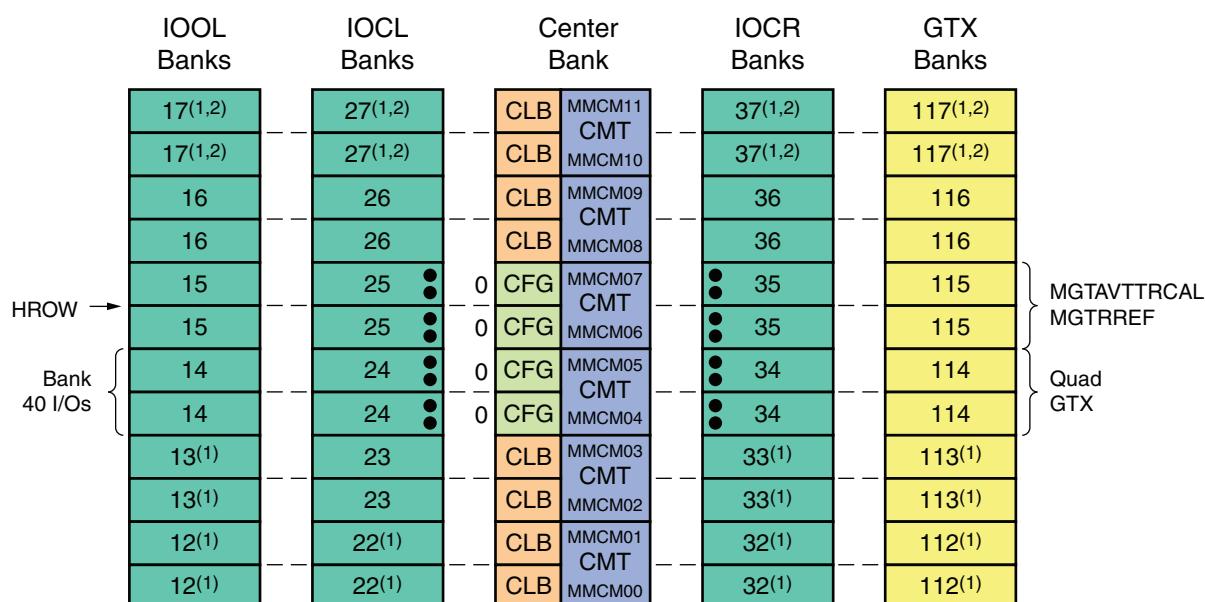
Notes:

1. Unbonded banks in FF484
2. Unbonded banks in FF784/RF784. The FF1156/RF1156 have all banks bonded out.

UG365_c1_02_111111

[Figure 1-2: XC6VLX130T, XQ6VLX130T, and XC6VLX195T Banks](#)

[Figure 1-3](#) shows the I/O and transceiver banks for the XC6VLX240T, XQ6VLX240T, XC6VSX315T, and XQ6VSX315T. The black dots denote the global clock banks.



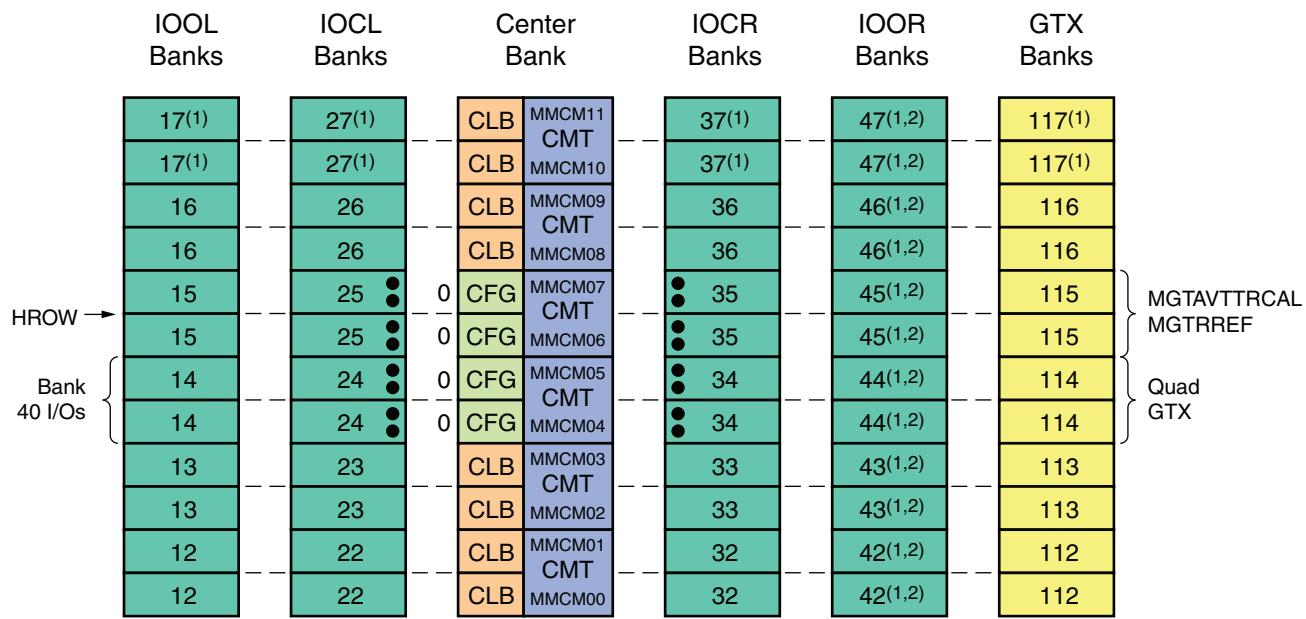
Notes:

1. Unbonded banks in FF784/RF784
2. Unbonded banks in FF1156/RF1156. The FF1759/RF1759 have all banks bonded out.

ug365_c1_03_111111

[Figure 1-3: XC6VLX240T, XQ6VLX240T, XC6VSX315T, and XQ6VSX315T Banks](#)

Figure 1-4 shows the I/O and transceiver banks for the XC6VLX365T. The black dots denote the global clock banks.



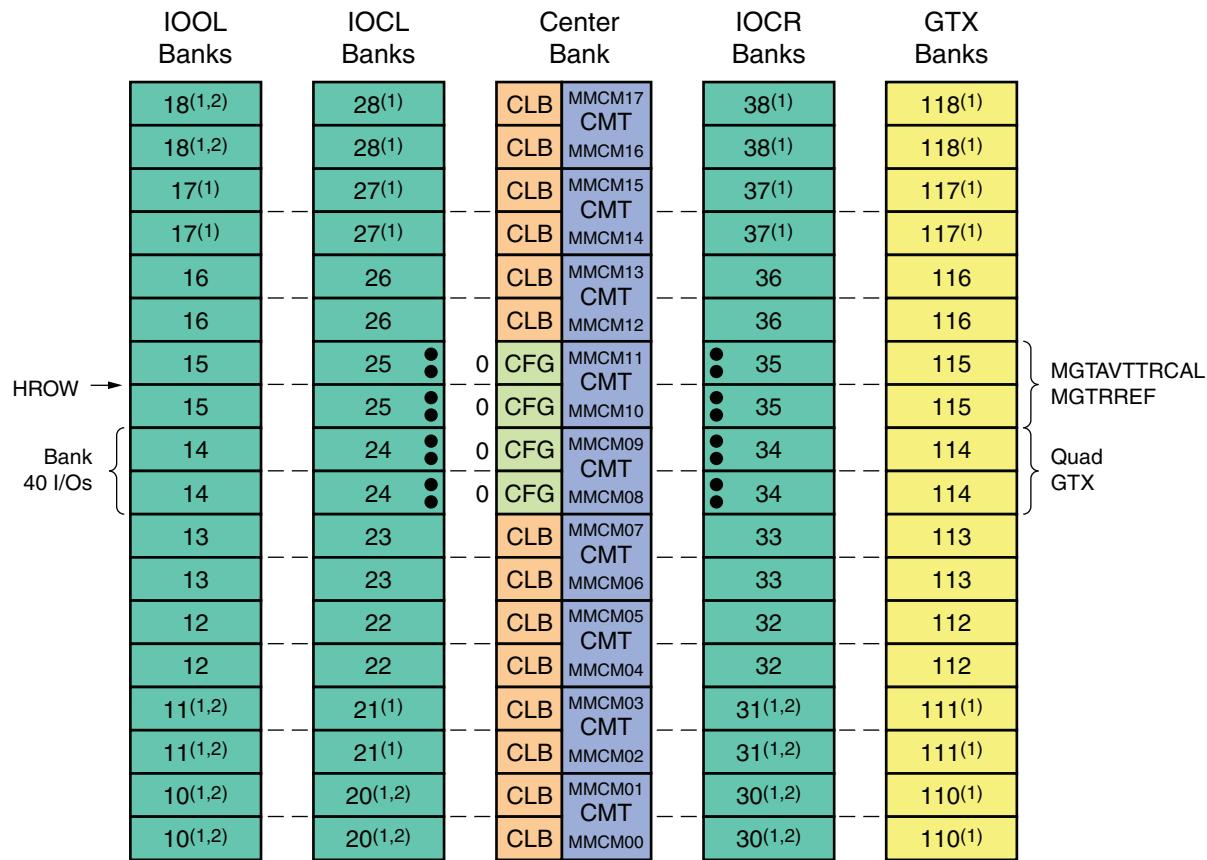
Notes:

1. Unbonded banks in FF1156.
2. Unbonded banks in FF1759.

ug365_c1_04_111111

Figure 1-4: XC6VLX365T Banks

Figure 1-5 shows the I/O and transceiver banks for the XC6VSX475T and XQ6VSX475T. The black dots denote the global clock banks.



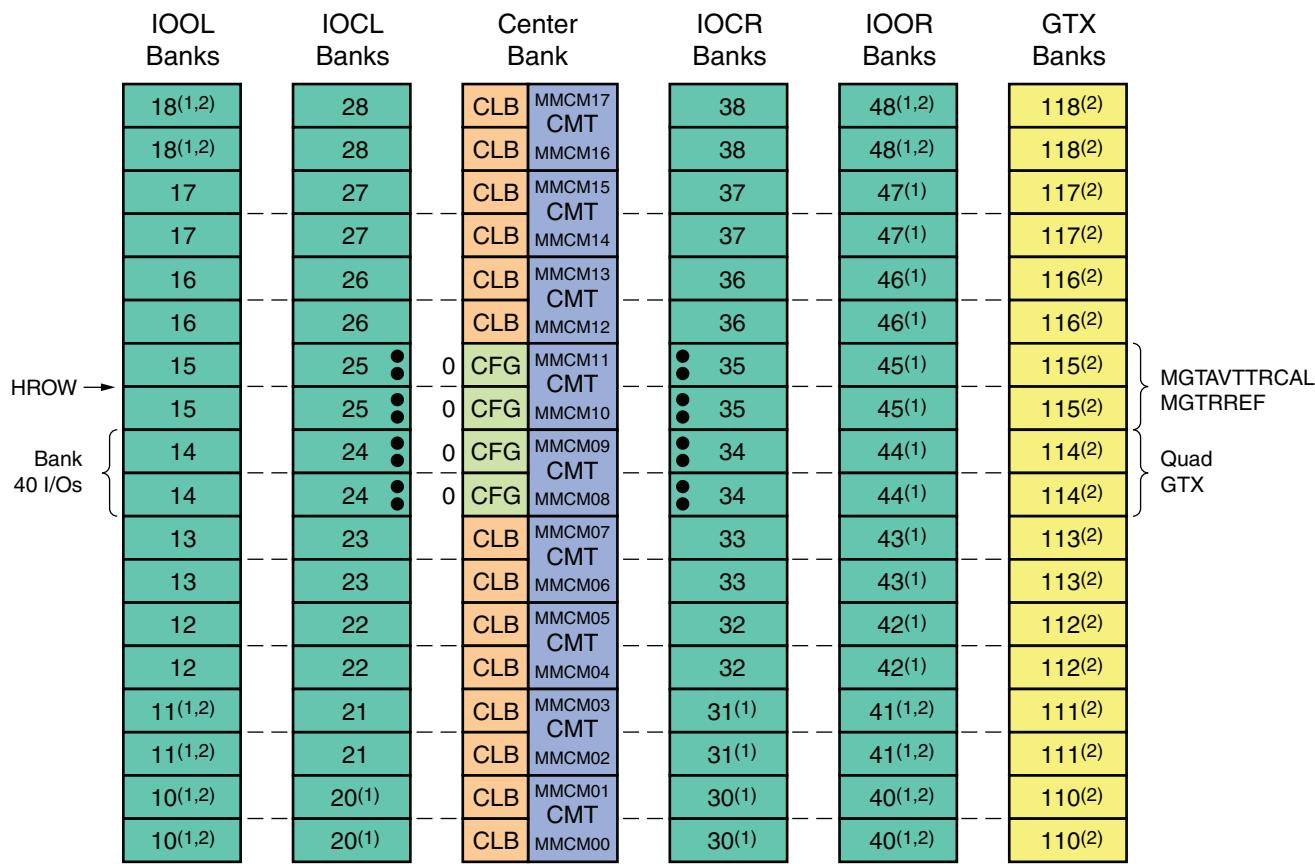
Note:

1. Unbonded banks in FF1156/RF1156.
2. Unbonded banks in FF1759/RF1759.

UG365_c1_05_111111

Figure 1-5: XC6VSX475T and XQ6VSX475T Banks

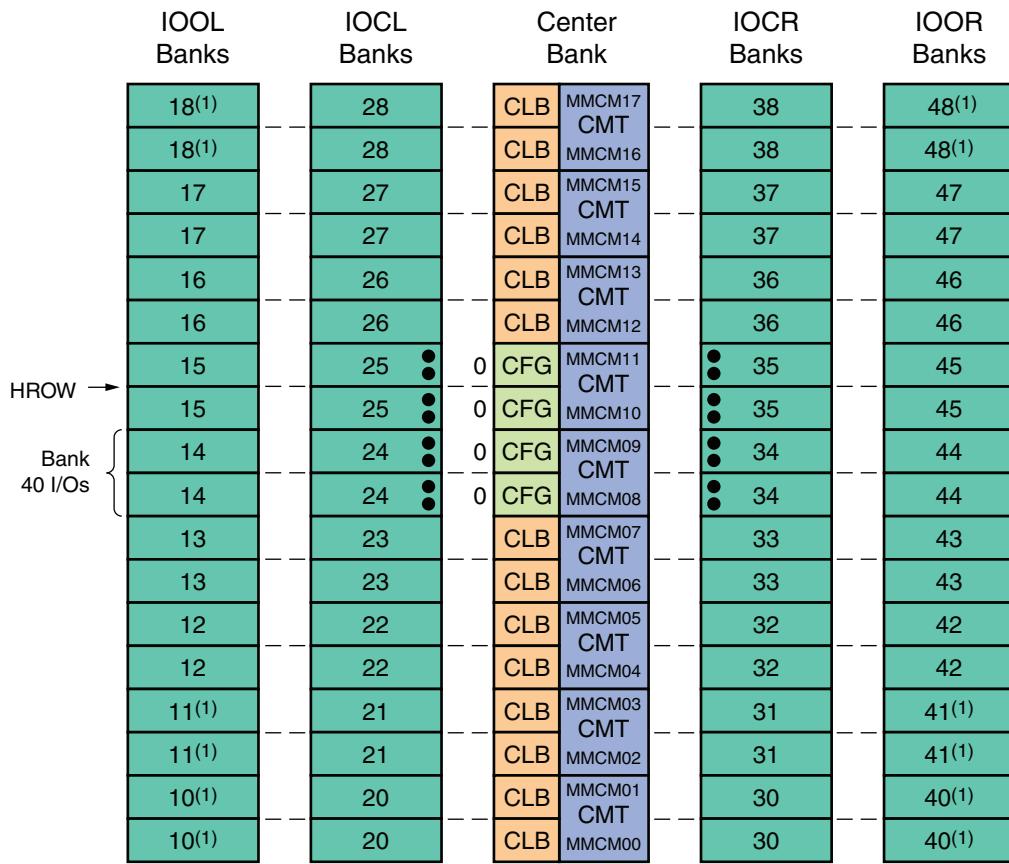
Figure 1-6 shows the I/O and transceiver banks for the XC6VLX550T and XQ6VLX550T. The black dots denote the global clock banks.



ug365_c1_06_111111

Figure 1-6: XC6VLX550T and XQ6VLX550TBanks

Figure 1-7 shows the I/O and transceiver banks for the XC6VLX760. The black dots denote the global clock banks.



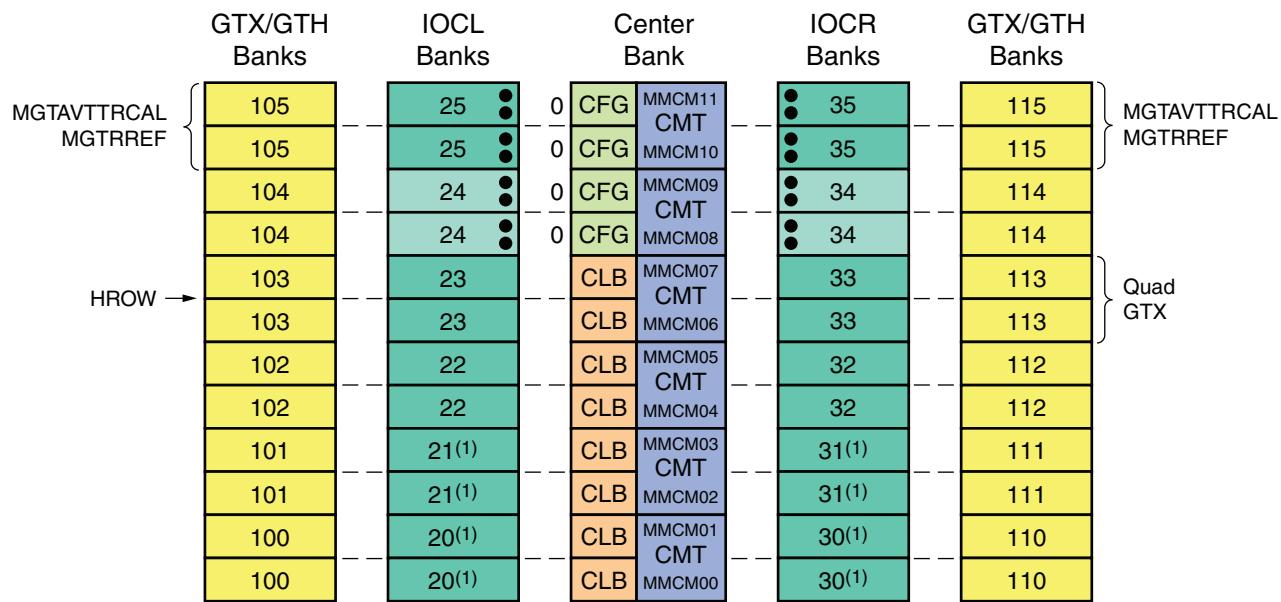
Note:

1. Unbonded banks in FF1760.

ug365_c1_07_111111

Figure 1-7: XC6VLX760 Banks

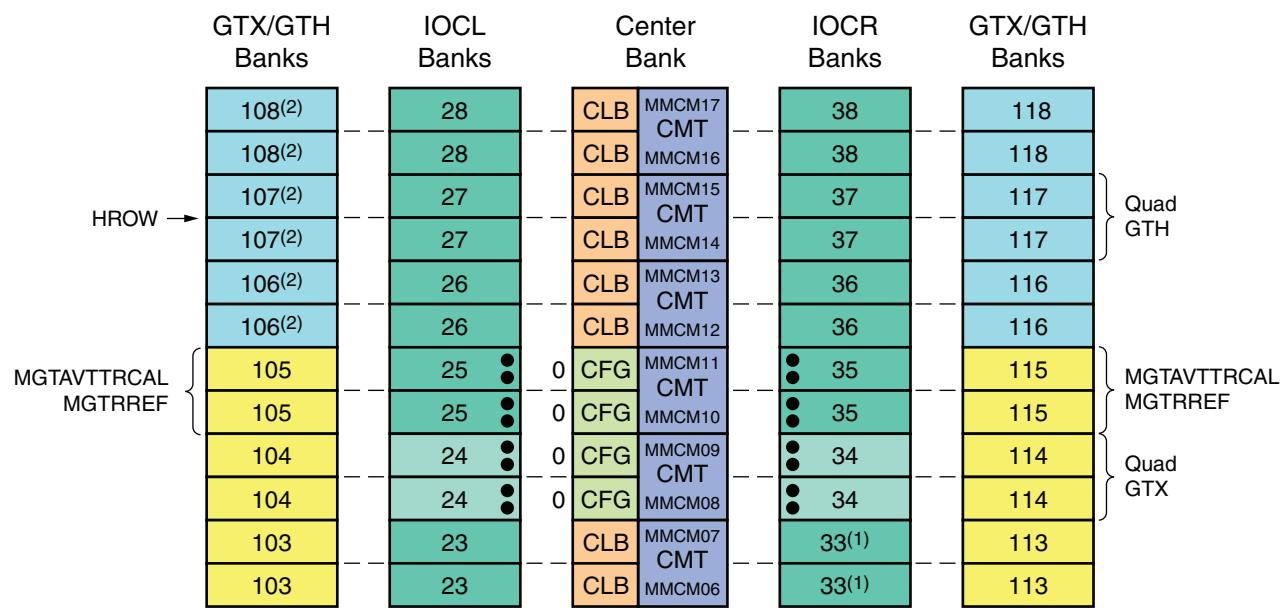
Figure 1-8 shows the I/O and transceiver banks for the XC6VHX250T. The black dots denote the global clock banks.



UG365_c1_08_111111

Figure 1-8: XC6VHX250T Banks

Figure 1-9 shows the I/O and transceiver banks for the XC6VHX255T. The black dots denote the global clock banks.



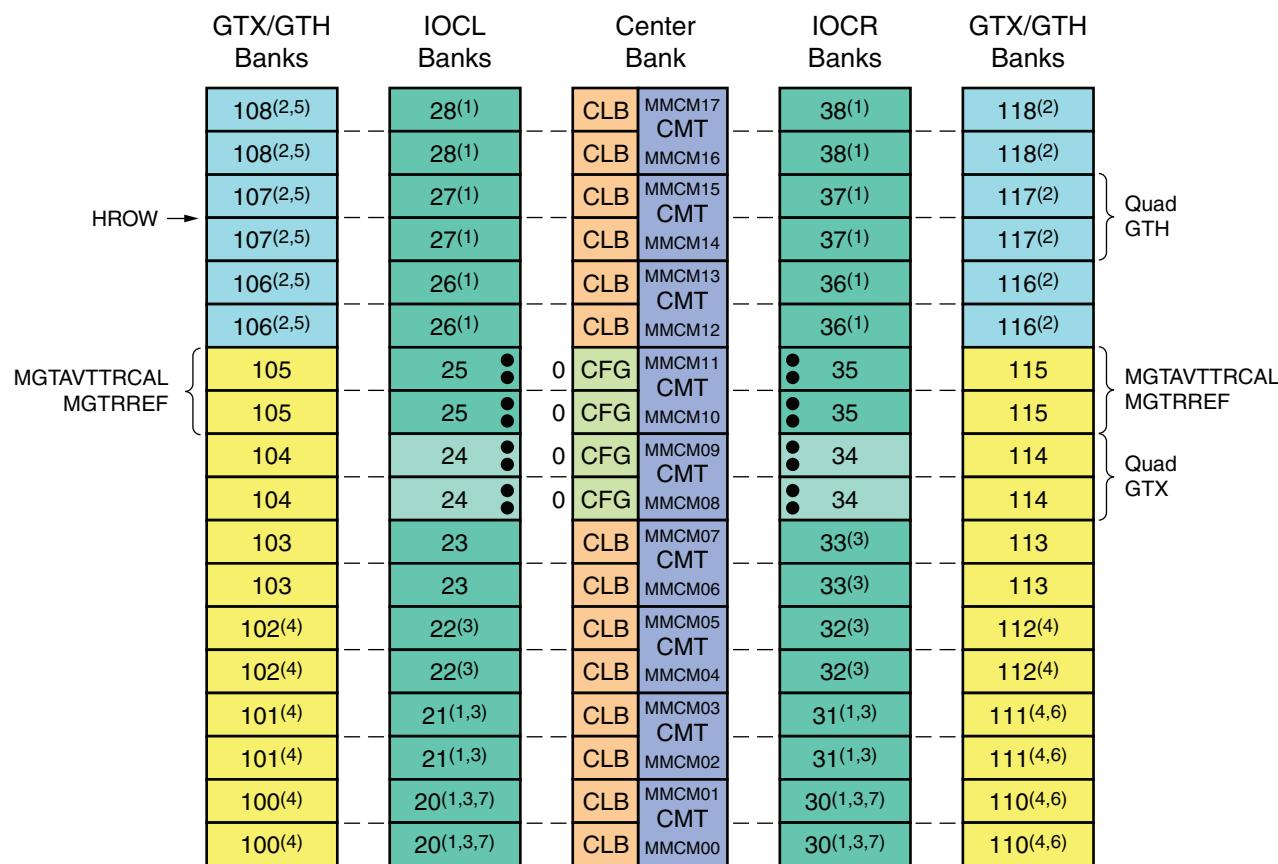
Note:

1. Unbonded banks in FF1155.
2. Unbonded GTH Quads in FF1155.
3. No unbonded banks in FF1923.

UG365_c1_09_111111

Figure 1-9: XC6VHX255T Banks

Figure 1-10 shows the I/O and transceiver banks for the XC6VH380T. The black dots denote the global clock banks.



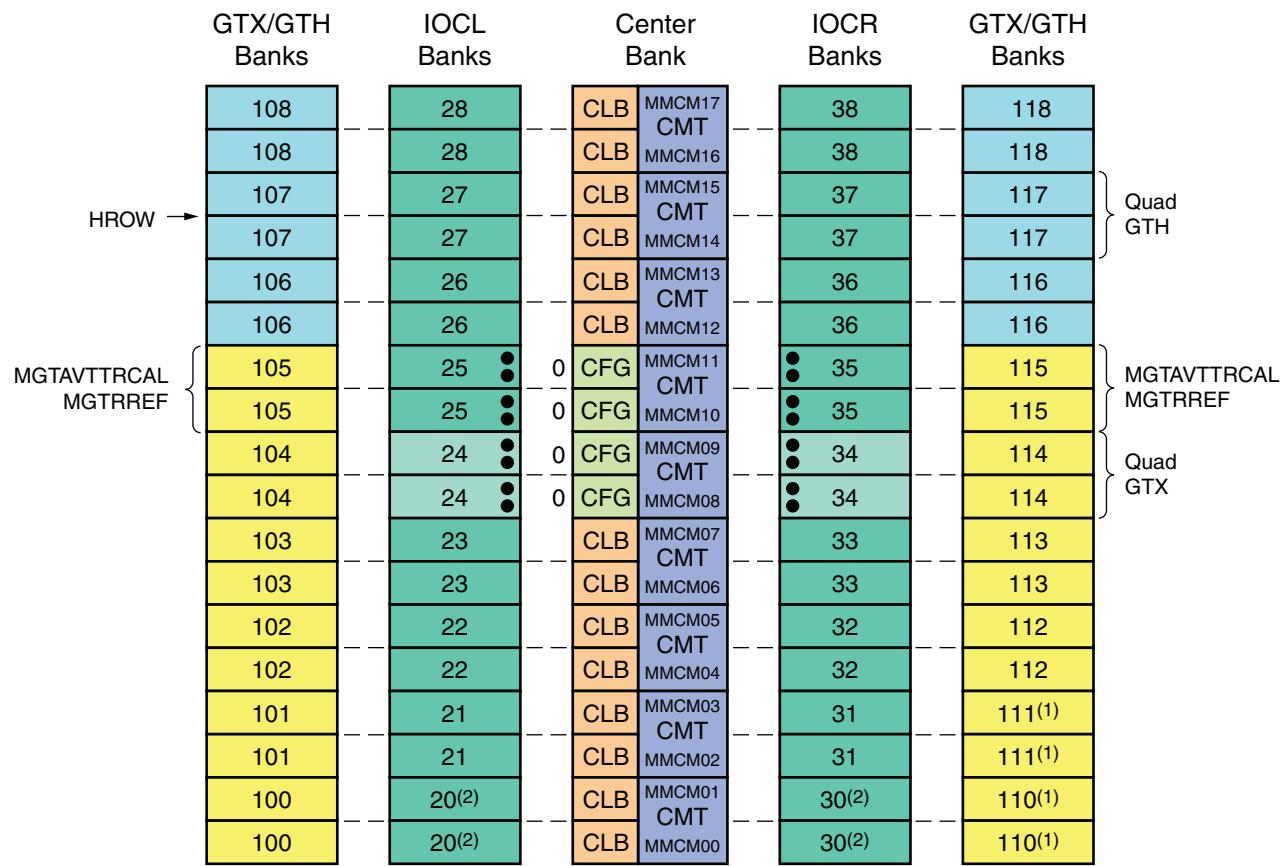
Note:

1. Unbonded banks in FF1154.
 2. Unbonded GTX Quads in FF1154.
 3. Unbonded banks in FF1155.
 4. Unbonded GTX Quads in FF1155.
 5. Unbonded GTH Quads in FF1155.
 6. Unbonded GTX Quads in FF1923.
 7. Unbonded banks in FF1924.

UG365_c1_10_111111

Figure 1-10: XC6VHX380T Banks

Figure 1-11 shows the I/O and transceiver banks for the XC6VHX565T. The black dots denote the global clock banks.



UG365_c1_11_111111

Figure 1-11: XC6VHX565T Banks

Pinout Tables

Summary

This chapter includes the pinout information tables for the following packages:

- Table 2-1, “FF484 Package—LX75T and LX130T,” on page 31
- Table 2-2, “FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T,” on page 47
- Table 2-3, “FF1154 Package—HX250T and HX380T,” on page 71
- Table 2-4, “FF1155 Package—HX255T and HX380T,” on page 107
- Table 2-5, “FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T,” on page 143
- Table 2-6, “FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T,” on page 180
- Table 2-7, “FF1760 Package—LX550T and LX760,” on page 234
- Table 2-8, “FF1923 Package—HX255T, HX380T, and HX565T,” on page 288
- Table 2-9, “FF1924 Package—HX380T and HX565T,” on page 347

FF484 Package—LX75T and LX130T

Table 2-1: FF484 Package—LX75T and LX130T

Bank	Pin Description	Pin Number	No Connect (NC)
0	INIT_B_0	H5	
0	DONE_0	K6	
0	M1_0	J7	
0	M2_0	H6	
0	HSWAPEN_0	L6	
0	PROGRAM_B_0	F5	
0	M0_0	H7	
0	AVSS_0	K11	
0	AVDD_0	K12	
0	VP_0	L12	
0	VREFP_0	M12	
0	VN_0	M11	

Table 2-1: FF484 Package—LX75T and LX130T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
0	VREFN_0	L11	
0	DXP_0	N12	
0	DXN_0	N11	
0	VBATT_0	T5	
0	DIN_0	Y5	
0	RDWR_B_0	V5	
0	CSI_B_0	M7	
0	DOUT_BUSY_0	N6	
0	CCLK_0	M6	
0	TDO_0	R7	
0	TCK_0	R6	
0	TMS_0	N7	
0	TDI_0	P7	
0	VFS_0	L7	
14	IO_L0P_14	M18	
14	IO_L0N_14	N18	
14	IO_L1P_14	M20	
14	IO_L1N_14	M19	
14	IO_L2P_14	N22	
14	IO_L2N_14	N21	
14	IO_L3P_14	L22	
14	IO_L3N_14	L21	
14	IO_L4P_14	P22	
14	IO_L4N_VREF_14	R22	
14	IO_L5P_14	R21	
14	IO_L5N_14	T22	
14	IO_L6P_14	N17	
14	IO_L6N_14	P17	
14	IO_L7P_14	M21	
14	IO_L7N_14	N20	
14	IO_L8P_SRCC_14	U21	
14	IO_L8N_SRCC_14	T21	
14	IO_L9P_MRCC_14	P19	

Table 2-1: FF484 Package—LX75T and LX130T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
14	IO_L9N_MRCC_14	P20	
14	IO_L10P_MRCC_14	W22	
14	IO_L10N_MRCC_14	V22	
14	IO_L11P_SRCC_14	R19	
14	IO_L11N_SRCC_14	R20	
14	IO_L12P_VRN_14	P18	
14	IO_L12N_VRP_14	R17	
14	IO_L13P_14	U19	
14	IO_L13N_14	U20	
14	IO_L14P_14	Y22	
14	IO_L14N_VREF_14	AA22	
14	IO_L15P_14	AA21	
14	IO_L15N_14	Y21	
14	IO_L16P_14	AB20	
14	IO_L16N_14	AB21	
14	IO_L17P_14	T18	
14	IO_L17N_14	T19	
14	IO_L18P_14	Y20	
14	IO_L18N_14	W20	
14	IO_L19P_14	V20	
14	IO_L19N_14	V21	
15	IO_L0P_15	B20	
15	IO_L0N_15	C20	
15	IO_L1P_15	G18	
15	IO_L1N_15	F18	
15	IO_L2P_SM8P_15	A21	
15	IO_L2N_SM8N_15	B21	
15	IO_L3P_SM9P_15	G19	
15	IO_L3N_SM9N_15	F19	
15	IO_L4P_15	J18	
15	IO_L4N_VREF_15	J17	
15	IO_L5P_SM10P_15	B22	
15	IO_L5N_SM10N_15	C21	

Table 2-1: FF484 Package—LX75T and LX130T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
15	IO_L6P_SM11P_15	K17	
15	IO_L6N_SM11N_15	L17	
15	IO_L7P_SM12P_15	E19	
15	IO_L7N_SM12N_15	D19	
15	IO_L8P_SRCC_15	K19	
15	IO_L8N_SRCC_15	J19	
15	IO_L9P_MRCC_15	D20	
15	IO_L9N_MRCC_15	E20	
15	IO_L10P_MRCC_15	C22	
15	IO_L10N_MRCC_15	D22	
15	IO_L11P_SRCC_15	E21	
15	IO_L11N_SRCC_15	E22	
15	IO_L12P_SM13P_15	F21	
15	IO_L12N_SM13N_15	F22	
15	IO_L13P_SM14P_15	J20	
15	IO_L13N_SM14N_15	K20	
15	IO_L14P_15	H17	
15	IO_L14N_VREF_15	H18	
15	IO_L15P_SM15P_15	G21	
15	IO_L15N_SM15N_15	H21	
15	IO_L16P_VRN_15	L18	
15	IO_L16N_VRP_15	L19	
15	IO_L17P_15	H20	
15	IO_L17N_15	G20	
15	IO_L18P_15	J22	
15	IO_L18N_15	H22	
15	IO_L19P_15	K21	
15	IO_L19N_15	K22	
24	IO_L0P_GC_24	T13	
24	IO_L0N_GC_24	U13	
24	IO_L1P_GC_24	T17	
24	IO_L1N_GC_24	U18	
24	IO_L2P_D15_24	T16	

Table 2-1: FF484 Package—LX75T and LX130T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
24	IO_L2N_D14_24	R16	
24	IO_L3P_D13_24	V17	
24	IO_L3N_D12_24	V18	
24	IO_L4P_D11_24	V13	
24	IO_L4N_VREF_D10_24	W13	
24	IO_L5P_D9_24	W18	
24	IO_L5N_D8_24	W17	
24	IO_L6P_D7_24	V16	
24	IO_L6N_D6_24	U16	
24	IO_L7P_D5_24	W19	
24	IO_L7N_D4_24	Y19	
24	IO_L8P_SRCC_24	AB18	
24	IO_L8N_SRCC_24	AA18	
24	IO_L9P_MRCC_24	AA19	
24	IO_L9N_MRCC_24	AB19	
24	IO_L10P_MRCC_24	Y17	
24	IO_L10N_MRCC_24	AA17	
24	IO_L11P_SRCC_24	AA16	
24	IO_L11N_SRCC_24	Y16	
24	IO_L12P_D3_24	R14	
24	IO_L12N_D2_FS2_24	R15	
24	IO_L13P_D1_FS1_24	U15	
24	IO_L13N_D0_FS0_24	V15	
24	IO_L14P_FCS_B_24	W15	
24	IO_L14N_VREF_FOE_B_MOSTI_24	Y15	
24	IO_L15P_FWE_B_24	T14	
24	IO_L15N_RS1_24	U14	
24	IO_L16P_RS0_24	AB13	
24	IO_L16N_CS0_B_24	AA13	
24	IO_L17P_VRN_24	Y14	
24	IO_L17N_VRP_24	W14	
24	IO_L18P_24	AB14	
24	IO_L18N_24	AA14	

Table 2-1: FF484 Package—LX75T and LX130T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
24	IO_L19P_24	AB15	
24	IO_L19N_24	AB16	
25	IO_L0P_25	D14	
25	IO_L0N_25	E14	
25	IO_L1P_25	B15	
25	IO_L1N_25	C15	
25	IO_L2P_25	A14	
25	IO_L2N_25	B14	
25	IO_L3P_25	D15	
25	IO_L3N_25	E15	
25	IO_L4P_25	F13	
25	IO_L4N_VREF_25	G13	
25	IO_L5P_25	A16	
25	IO_L5N_25	B16	
25	IO_L6P_25	F12	
25	IO_L6N_25	E12	
25	IO_L7P_25	A17	
25	IO_L7N_25	A18	
25	IO_L8P_SRCC_25	C13	
25	IO_L8N_SRCC_25	D13	
25	IO_L9P_MRCC_25	E16	
25	IO_L9N_MRCC_25	F16	
25	IO_L10P_MRCC_25	A19	
25	IO_L10N_MRCC_25	B19	
25	IO_L11P_SRCC_25	C16	
25	IO_L11N_SRCC_25	C17	
25	IO_L12P_25	A13	
25	IO_L12N_25	B13	
25	IO_L13P_25	B18	
25	IO_L13N_25	C18	
25	IO_L14P_25	G14	
25	IO_L14N_VREF_25	F14	
25	IO_L15P_25	G16	

Table 2-1: FF484 Package—LX75T and LX130T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
25	IO_L15N_25	H16	
25	IO_L16P_VRN_25	H12	
25	IO_L16N_VRP_25	H13	
25	IO_L17P_25	D17	
25	IO_L17N_25	D18	
25	IO_L18P_GC_25	G15	
25	IO_L18N_GC_25	H15	
25	IO_L19P_GC_25	E17	
25	IO_L19N_GC_25	F17	
34	IO_L0P_GC_34	V12	
34	IO_L0N_GC_34	W12	
34	IO_L1P_GC_34	T6	
34	IO_L1N_GC_34	T7	
34	IO_L2P_A15_D31_34	R9	
34	IO_L2N_A14_D30_34	T8	
34	IO_L3P_A13_D29_34	U6	
34	IO_L3N_A12_D28_34	V6	
34	IO_L4P_A11_D27_34	T12	
34	IO_L4N_VREF_A10_D26_34	T11	
34	IO_L5P_A09_D25_34	V7	
34	IO_L5N_A08_D24_34	W7	
34	IO_L6P_A07_D23_34	V8	
34	IO_L6N_A06_D22_34	U8	
34	IO_L7P_A05_D21_34	Y6	
34	IO_L7N_A04_D20_34	Y7	
34	IO_L8P_SRCC_34	AB6	
34	IO_L8N_SRCC_34	AA6	
34	IO_L9P_MRCC_34	AA7	
34	IO_L9N_MRCC_34	AA8	
34	IO_L10P_MRCC_34	AA9	
34	IO_L10N_MRCC_34	Y9	
34	IO_L11P_SRCC_34	V10	
34	IO_L11N_SRCC_34	U9	

Table 2-1: FF484 Package—LX75T and LX130T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
34	IO_L12P_A03_D19_34	W9	
34	IO_L12N_A02_D18_34	W8	
34	IO_L13P_A01_D17_34	T9	
34	IO_L13N_A00_D16_34	U10	
34	IO_L14P_A25_34	W10	
34	IO_L14N_VREF_A24_34	Y10	
34	IO_L15P_A23_34	AB9	
34	IO_L15N_A22_34	AB8	
34	IO_L16P_A21_34	Y12	
34	IO_L16N_A20_34	AA12	
34	IO_L17P_A19_34	U11	
34	IO_L17N_A18_34	V11	
34	IO_L18P_A17_34	AA11	
34	IO_L18N_A16_34	Y11	
34	IO_L19P_VRN_34	AB11	
34	IO_L19N_VRP_34	AB10	
35	IO_L0P_35	A12	
35	IO_L0N_35	A11	
35	IO_L1P_35	B10	
35	IO_L1N_35	C10	
35	IO_L2P_SM0P_35	C11	
35	IO_L2N_SM0N_35	B11	
35	IO_L3P_SM1P_35	A9	
35	IO_L3N_SM1N_35	B9	
35	IO_L4P_35	D10	
35	IO_L4N_VREF_35	E10	
35	IO_L5P_SM2P_35	A8	
35	IO_L5N_SM2N_35	B8	
35	IO_L6P_SM3P_35	A7	
35	IO_L6N_SM3N_35	A6	
35	IO_L7P_SM4P_35	C6	
35	IO_L7N_SM4N_35	B6	
35	IO_L8P_SRCC_35	G10	

Table 2-1: FF484 Package—LX75T and LX130T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
35	IO_L8N_SRCC_35	H10	
35	IO_L9P_MRCC_35	E9	
35	IO_L9N_MRCC_35	D9	
35	IO_L10P_MRCC_35	C8	
35	IO_L10N_MRCC_35	C7	
35	IO_L11P_SRCC_35	D8	
35	IO_L11N_SRCC_35	D7	
35	IO_L12P_SM5P_35	F9	
35	IO_L12N_SM5N_35	G9	
35	IO_L13P_SM6P_35	E7	
35	IO_L13N_SM6N_35	E6	
35	IO_L14P_35	E11	
35	IO_L14N_VREF_35	F11	
35	IO_L15P_SM7P_35	F8	
35	IO_L15N_SM7N_35	F7	
35	IO_L16P_VRN_35	G11	
35	IO_L16N_VRP_35	H11	
35	IO_L17P_35	G8	
35	IO_L17N_35	H8	
35	IO_L18P_GC_35	D12	
35	IO_L18N_GC_35	C12	
35	IO_L19P_GC_35	F6	
35	IO_L19N_GC_35	G6	
114	MGTTXN3_114	M2	
114	MGTRXN3_114	W4	
114	MGTTXP3_114	M1	
114	MGTRXP3_114	W3	
114	MGTTXN2_114	P2	
114	MGTRXN2_114	Y2	
114	MGTTXP2_114	P1	
114	MGTREFCLK1P_114	R4	
114	MGTREFCLK1N_114	R3	
114	MGTRXP2_114	Y1	

Table 2-1: FF484 Package—LX75T and LX130T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
114	MGTREFCLK0P_114	U4	
114	MGTREFCLK0N_114	U3	
114	MGTTXN1_114	T2	
114	MGTRXN1_114	AA4	
114	MGTTXP1_114	T1	
114	MGTRXP1_114	AA3	
114	MGTTXN0_114	V2	
114	MGTRXN0_114	AB2	
114	MGTTXP0_114	V1	
114	MGTRXP0_114	AB1	
115	MGTTXN3_115	D2	
115	MGTRXN3_115	B2	
115	MGTTXP3_115	D1	
115	MGTRXP3_115	B1	
115	MGTTXN2_115	F2	
115	MGTRXN2_115	C4	
115	MGTTXP2_115	F1	
115	MGTREFCLK1P_115	J4	
115	MGTREFCLK1N_115	J3	
115	MGTRXP2_115	C3	
115	MGTAVTTRCAL_115	A4	
115	MGTRREF_115	A3	
115	MGTREFCLK0P_115	L4	
115	MGTREFCLK0N_115	L3	
115	MGTTXN1_115	H2	
115	MGTRXN1_115	E4	
115	MGTTXP1_115	H1	
115	MGTRXP1_115	E3	
115	MGTTXN0_115	K2	
115	MGTRXN0_115	G4	
115	MGTTXP0_115	K1	
115	MGTRXP0_115	G3	
NA	GND	A1	

Table 2-1: FF484 Package—LX75T and LX130T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	A15	
NA	GND	A2	
NA	GND	A22	
NA	GND	A5	
NA	GND	AA1	
NA	GND	AA15	
NA	GND	AA5	
NA	GND	AB12	
NA	GND	AB22	
NA	GND	AB4	
NA	GND	AB5	
NA	GND	B12	
NA	GND	B4	
NA	GND	B5	
NA	GND	C1	
NA	GND	C19	
NA	GND	C5	
NA	GND	C9	
NA	GND	D16	
NA	GND	D3	
NA	GND	D5	
NA	GND	D6	
NA	GND	E1	
NA	GND	E13	
NA	GND	E5	
NA	GND	F10	
NA	GND	F20	
NA	GND	F3	
NA	GND	G1	
NA	GND	G17	
NA	GND	G5	
NA	GND	G7	
NA	GND	H14	

Table 2-1: FF484 Package—LX75T and LX130T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	H3	
NA	GND	J1	
NA	GND	J11	
NA	GND	J13	
NA	GND	J15	
NA	GND	J2	
NA	GND	J21	
NA	GND	J5	
NA	GND	J6	
NA	GND	J9	
NA	GND	K10	
NA	GND	K14	
NA	GND	K16	
NA	GND	K18	
NA	GND	K3	
NA	GND	K5	
NA	GND	K8	
NA	GND	L1	
NA	GND	L13	
NA	GND	L15	
NA	GND	L2	
NA	GND	L5	
NA	GND	L9	
NA	GND	M10	
NA	GND	M14	
NA	GND	M16	
NA	GND	M22	
NA	GND	M3	
NA	GND	M5	
NA	GND	M8	
NA	GND	N1	
NA	GND	N13	
NA	GND	N15	

Table 2-1: FF484 Package—LX75T and LX130T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	N19	
NA	GND	N4	
NA	GND	N5	
NA	GND	N9	
NA	GND	P10	
NA	GND	P12	
NA	GND	P14	
NA	GND	P16	
NA	GND	P3	
NA	GND	P5	
NA	GND	P8	
NA	GND	R1	
NA	GND	R11	
NA	GND	R13	
NA	GND	R2	
NA	GND	R5	
NA	GND	T10	
NA	GND	T20	
NA	GND	T3	
NA	GND	U1	
NA	GND	U17	
NA	GND	U2	
NA	GND	U5	
NA	GND	U7	
NA	GND	V14	
NA	GND	V3	
NA	GND	W1	
NA	GND	W11	
NA	GND	W21	
NA	GND	W5	
NA	GND	Y18	
NA	GND	Y4	
NA	GND	Y8	

Table 2-1: FF484 Package—LX75T and LX130T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCAUX	J8	
NA	VCCAUX	J16	
NA	VCCAUX	L8	
NA	VCCAUX	L16	
NA	VCCAUX	N8	
NA	VCCAUX	N16	
NA	VCCAUX	P15	
NA	VCCAUX	R8	
NA	VCCINT	J10	
NA	VCCINT	J12	
NA	VCCINT	J14	
NA	VCCINT	K9	
NA	VCCINT	K13	
NA	VCCINT	K15	
NA	VCCINT	L10	
NA	VCCINT	L14	
NA	VCCINT	M9	
NA	VCCINT	M13	
NA	VCCINT	M15	
NA	VCCINT	N10	
NA	VCCINT	N14	
NA	VCCINT	P9	
NA	VCCINT	P11	
NA	VCCINT	P13	
NA	VCCINT	R10	
NA	VCCINT	R12	
0	VCCO_0	K7	
0	VCCO_0	P6	
14	VCCO_14	AA20	
14	VCCO_14	M17	
14	VCCO_14	P21	
14	VCCO_14	R18	
14	VCCO_14	U22	

Table 2-1: FF484 Package—LX75T and LX130T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
15	VCCO_15	A20	
15	VCCO_15	D21	
15	VCCO_15	G22	
15	VCCO_15	H19	
15	VCCO_15	L20	
24	VCCO_24	AB17	
24	VCCO_24	T15	
24	VCCO_24	V19	
24	VCCO_24	W16	
24	VCCO_24	Y13	
25	VCCO_25	B17	
25	VCCO_25	C14	
25	VCCO_25	E18	
25	VCCO_25	F15	
25	VCCO_25	G12	
34	VCCO_34	AA10	
34	VCCO_34	AB7	
34	VCCO_34	U12	
34	VCCO_34	V9	
34	VCCO_34	W6	
35	VCCO_35	A10	
35	VCCO_35	B7	
35	VCCO_35	D11	
35	VCCO_35	E8	
35	VCCO_35	H9	
NA	MGTAVCC	D4	
NA	MGTAVCC	F4	
NA	MGTAVCC	H4	
NA	MGTAVCC	K4	
NA	MGTAVCC	M4	
NA	MGTAVCC	P4	
NA	MGTAVCC	T4	
NA	MGTAVCC	V4	

Table 2-1: FF484 Package—LX75T and LX130T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTAVTT	AA2	
NA	MGTAVTT	AB3	
NA	MGTAVTT	B3	
NA	MGTAVTT	C2	
NA	MGTAVTT	E2	
NA	MGTAVTT	G2	
NA	MGTAVTT	N2	
NA	MGTAVTT	N3	
NA	MGTAVTT	W2	
NA	MGTAVTT	Y3	

FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T

Bank	Pin Description	Pin Number	NoConnect (NC)
0	INIT_B_0	M6	
0	DONE_0	L6	
0	M1_0	D6	
0	M2_0	C6	
0	HSWAPEN_0	N7	
0	PROGRAM_B_0	M7	
0	M0_0	F6	
0	AVSS_0	N13	
0	AVDD_0	N14	
0	VP_0	P14	
0	VREFP_0	R14	
0	VN_0	R13	
0	VREFN_0	P13	
0	DXP_0	T14	
0	DXN_0	T13	
0	VBATT_0	J6	
0	DIN_0	H6	
0	RDWR_B_0	G6	
0	CSI_B_0	AG6	
0	DOUT_BUSY_0	AF6	
0	CCLK_0	AH6	
0	TDO_0	Y7	
0	TCK_0	AB6	
0	TMS_0	Y6	
0	TDI_0	AA6	
0	VFS_0	AD6	
14	IO_L0P_14	R27	
14	IO_L0N_14	R28	
14	IO_L1P_14	T27	
14	IO_L1N_14	U27	
14	IO_L2P_14	V28	

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T (Cont'd)

Bank	Pin Description	Pin Number	NoConnect (NC)
14	IO_L2N_14	U28	
14	IO_L3P_14	W25	
14	IO_L3N_14	V25	
14	IO_L4P_14	W26	
14	IO_L4N_VREF_14	V26	
14	IO_L5P_14	Y28	
14	IO_L5N_14	W28	
14	IO_L6P_14	W27	
14	IO_L6N_14	Y27	
14	IO_L7P_14	Y25	
14	IO_L7N_14	Y24	
14	IO_L8P_SRCC_14	P21	
14	IO_L8N_SRCC_14	P22	
14	IO_L9P_MRCC_14	Y23	
14	IO_L9N_MRCC_14	W23	
14	IO_L10P_MRCC_14	U26	
14	IO_L10N_MRCC_14	T26	
14	IO_L11P_SRCC_14	V23	
14	IO_L11N_SRCC_14	U23	
14	IO_L12P_VRN_14	R24	
14	IO_L12N_VRP_14	R25	
14	IO_L13P_14	Y22	
14	IO_L13N_14	W22	
14	IO_L14P_14	R20	
14	IO_L14N_VREF_14	P20	
14	IO_L15P_14	T24	
14	IO_L15N_14	T25	
14	IO_L16P_14	V24	
14	IO_L16N_14	U24	
14	IO_L17P_14	U22	
14	IO_L17N_14	U21	
14	IO_L18P_14	R22	
14	IO_L18N_14	R23	

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T (Cont'd)

Bank	Pin Description	Pin Number	NoConnect (NC)
14	IO_L19P_14	T21	
14	IO_L19N_14	T22	
15	IO_L0P_15	K22	
15	IO_L0N_15	K23	
15	IO_L1P_15	H25	
15	IO_L1N_15	H26	
15	IO_L2P_SM8P_15	K24	
15	IO_L2N_SM8N_15	J23	
15	IO_L3P_SM9P_15	J26	
15	IO_L3N_SM9N_15	J27	
15	IO_L4P_15	L20	
15	IO_L4N_VREF_15	M19	
15	IO_L5P_SM10P_15	K25	
15	IO_L5N_SM10N_15	J25	
15	IO_L6P_SM11P_15	M23	
15	IO_L6N_SM11N_15	M24	
15	IO_L7P_SM12P_15	J28	
15	IO_L7N_SM12N_15	K28	
15	IO_L8P_SRCC_15	L21	
15	IO_L8N_SRCC_15	L22	
15	IO_L9P_MRCC_15	K27	
15	IO_L9N_MRCC_15	L26	
15	IO_L10P_MRCC_15	M22	
15	IO_L10N_MRCC_15	M21	
15	IO_L11P_SRCC_15	M26	
15	IO_L11N_SRCC_15	N26	
15	IO_L12P_SM13P_15	M27	
15	IO_L12N_SM13N_15	L27	
15	IO_L13P_SM14P_15	P28	
15	IO_L13N_SM14N_15	P27	
15	IO_L14P_15	L24	
15	IO_L14N_VREF_15	L25	
15	IO_L15P_SM15P_15	N28	

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T (Cont'd)

Bank	Pin Description	Pin Number	NoConnect (NC)
15	IO_L15N_SM15N_15	M28	
15	IO_L16P_VRN_15	N24	
15	IO_L16N_VRP_15	N25	
15	IO_L17P_15	P26	
15	IO_L17N_15	P25	
15	IO_L18P_15	N20	
15	IO_L18N_15	N21	
15	IO_L19P_15	N23	
15	IO_L19N_15	P23	
16	IO_L0P_16	G22	
16	IO_L0N_16	H21	
16	IO_L1P_16	B24	
16	IO_L1N_16	C24	
16	IO_L2P_16	H23	
16	IO_L2N_16	G23	
16	IO_L3P_16	B26	
16	IO_L3N_16	C25	
16	IO_L4P_16	D22	
16	IO_L4N_VREF_16	C23	
16	IO_L5P_16	E22	
16	IO_L5N_16	F22	
16	IO_L6P_16	E24	
16	IO_L6N_16	D25	
16	IO_L7P_16	A26	
16	IO_L7N_16	A27	
16	IO_L8P_SRCC_16	J21	
16	IO_L8N_SRCC_16	J22	
16	IO_L9P_MRCC_16	B27	
16	IO_L9N_MRCC_16	B28	
16	IO_L10P_MRCC_16	E25	
16	IO_L10N_MRCC_16	F24	
16	IO_L11P_SRCC_16	D27	
16	IO_L11N_SRCC_16	C28	

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T (Cont'd)

Bank	Pin Description	Pin Number	NoConnect (NC)
16	IO_L12P_VRN_16	H24	
16	IO_L12N_VRP_16	G24	
16	IO_L13P_16	D28	
16	IO_L13N_16	E28	
16	IO_L14P_16	E23	
16	IO_L14N_VREF_16	D23	
16	IO_L15P_16	F26	
16	IO_L15N_16	F25	
16	IO_L16P_16	F27	
16	IO_L16N_16	E27	
16	IO_L17P_16	G27	
16	IO_L17N_16	G26	
16	IO_L18P_16	D26	
16	IO_L18N_16	C26	
16	IO_L19P_16	G28	
16	IO_L19N_16	H28	
23	IO_L0P_23	W21	LX75T
23	IO_L0N_23	V21	LX75T
23	IO_L1P_23	AD22	LX75T
23	IO_L1N_23	AC21	LX75T
23	IO_L2P_23	V20	LX75T
23	IO_L2N_23	V19	LX75T
23	IO_L3P_23	AG22	LX75T
23	IO_L3N_23	AF21	LX75T
23	IO_L4P_23	AF22	LX75T
23	IO_L4N_VREF_23	AE22	LX75T
23	IO_L5P_23	AA21	LX75T
23	IO_L5N_23	AB21	LX75T
23	IO_L6P_23	Y18	LX75T
23	IO_L6N_23	W18	LX75T
23	IO_L7P_23	AG21	LX75T
23	IO_L7N_23	AF20	LX75T
23	IO_L8P_SRCC_23	AD20	LX75T

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T (Cont'd)

Bank	Pin Description	Pin Number	NoConnect (NC)
23	IO_L8N_SRCC_23	AE20	LX75T
23	IO_L9P_MRCC_23	AD21	LX75T
23	IO_L9N_MRCC_23	AC20	LX75T
23	IO_L10P_MRCC_23	AF19	LX75T
23	IO_L10N_MRCC_23	AE19	LX75T
23	IO_L11P_SRCC_23	Y20	LX75T
23	IO_L11N_SRCC_23	AA20	LX75T
23	IO_L12P_VRN_23	AA19	LX75T
23	IO_L12N_VRP_23	Y19	LX75T
23	IO_L13P_23	AG17	LX75T
23	IO_L13N_23	AF17	LX75T
23	IO_L14P_23	AD18	LX75T
23	IO_L14N_VREF_23	AE18	LX75T
23	IO_L15P_23	AC19	LX75T
23	IO_L15N_23	AB19	LX75T
23	IO_L16P_23	AB18	LX75T
23	IO_L16N_23	AC18	LX75T
23	IO_L17P_23	AH20	LX75T
23	IO_L17N_23	AH21	LX75T
23	IO_L18P_23	AG18	LX75T
23	IO_L18N_23	AH18	LX75T
23	IO_L19P_23	AH19	LX75T
23	IO_L19N_23	AG19	LX75T
24	IO_L0P_GC_24	AA26	
24	IO_L0N_GC_24	AA27	
24	IO_L1P_GC_24	AD28	
24	IO_L1N_GC_24	AD27	
24	IO_L2P_D15_24	AC28	
24	IO_L2N_D14_24	AB28	
24	IO_L3P_D13_24	AG28	
24	IO_L3N_D12_24	AF27	
24	IO_L4P_D11_24	AG27	
24	IO_L4N_VREF_D10_24	AH28	

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T (Cont'd)

Bank	Pin Description	Pin Number	NoConnect (NC)
24	IO_L5P_D9_24	AE28	
24	IO_L5N_D8_24	AE27	
24	IO_L6P_D7_24	AA24	
24	IO_L6N_D6_24	AA25	
24	IO_L7P_D5_24	AC25	
24	IO_L7N_D4_24	AD25	
24	IO_L8P_SRCC_24	AB27	
24	IO_L8N_SRCC_24	AB26	
24	IO_L9P_MRCC_24	AF26	
24	IO_L9N_MRCC_24	AG26	
24	IO_L10P_MRCC_24	AE25	
24	IO_L10N_MRCC_24	AF25	
24	IO_L11P_SRCC_24	AB23	
24	IO_L11N_SRCC_24	AC23	
24	IO_L12P_D3_24	AC26	
24	IO_L12N_D2_FS2_24	AD26	
24	IO_L13P_D1_FS1_24	AH26	
24	IO_L13N_D0_FS0_24	AH25	
24	IO_L14P_FCS_B_24	AE24	
24	IO_L14N_VREF_FOE_B_MOSI_24	AF24	
24	IO_L15P_FWE_B_24	AG24	
24	IO_L15N_RS1_24	AH24	
24	IO_L16P_RS0_24	AC24	
24	IO_L16N_CSO_B_24	AB24	
24	IO_L17P_VRN_24	AH23	
24	IO_L17N_VRP_24	AG23	
24	IO_L18P_24	AE23	
24	IO_L18N_24	AD23	
24	IO_L19P_24	AB22	
24	IO_L19N_24	AA22	
25	IO_L0P_25	K17	
25	IO_L0N_25	K18	
25	IO_L1P_25	G17	

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T (Cont'd)

Bank	Pin Description	Pin Number	NoConnect (NC)
25	IO_L1N_25	F17	
25	IO_L2P_25	J17	
25	IO_L2N_25	J18	
25	IO_L3P_25	C18	
25	IO_L3N_25	D18	
25	IO_L4P_25	G18	
25	IO_L4N_VREF_25	H18	
25	IO_L5P_25	B18	
25	IO_L5N_25	B19	
25	IO_L6P_25	D17	
25	IO_L6N_25	E17	
25	IO_L7P_25	E18	
25	IO_L7N_25	F19	
25	IO_L8P_SRCC_25	A20	
25	IO_L8N_SRCC_25	A19	
25	IO_L9P_MRCC_25	H19	
25	IO_L9N_MRCC_25	G19	
25	IO_L10P_MRCC_25	D20	
25	IO_L10N_MRCC_25	E19	
25	IO_L11P_SRCC_25	A21	
25	IO_L11N_SRCC_25	A22	
25	IO_L12P_25	C19	
25	IO_L12N_25	C20	
25	IO_L13P_25	B21	
25	IO_L13N_25	C21	
25	IO_L14P_25	K19	
25	IO_L14N_VREF_25	J20	
25	IO_L15P_25	A24	
25	IO_L15N_25	A25	
25	IO_L16P_VRN_25	E20	
25	IO_L16N_VRP_25	D21	
25	IO_L17P_25	B22	
25	IO_L17N_25	B23	

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T (Cont'd)

Bank	Pin Description	Pin Number	NoConnect (NC)
25	IO_L18P_GC_25	H20	
25	IO_L18N_GC_25	G21	
25	IO_L19P_GC_25	F20	
25	IO_L19N_GC_25	F21	
26	IO_L0P_26	E12	
26	IO_L0N_26	D11	
26	IO_L1P_26	E13	
26	IO_L1N_26	E14	
26	IO_L2P_26	H16	
26	IO_L2N_26	G16	
26	IO_L3P_26	G14	
26	IO_L3N_26	F14	
26	IO_L4P_26	J16	
26	IO_L4N_VREF_26	H15	
26	IO_L5P_26	B11	
26	IO_L5N_26	C11	
26	IO_L6P_26	D13	
26	IO_L6N_26	D12	
26	IO_L7P_26	C14	
26	IO_L7N_26	B13	
26	IO_L8P_SRCC_26	J15	
26	IO_L8N_SRCC_26	K15	
26	IO_L9P_MRCC_26	B14	
26	IO_L9N_MRCC_26	A14	
26	IO_L10P_MRCC_26	F16	
26	IO_L10N_MRCC_26	F15	
26	IO_L11P_SRCC_26	G12	
26	IO_L11N_SRCC_26	F12	
26	IO_L12P_VRN_26	E15	
26	IO_L12N_VRP_26	D15	
26	IO_L13P_26	A15	
26	IO_L13N_26	A16	
26	IO_L14P_26	A11	

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T (Cont'd)

Bank	Pin Description	Pin Number	NoConnect (NC)
26	IO_L14N_VREF_26	A12	
26	IO_L15P_26	C15	
26	IO_L15N_26	B16	
26	IO_L16P_26	D16	
26	IO_L16N_26	C16	
26	IO_L17P_26	A17	
26	IO_L17N_26	B17	
26	IO_L18P_26	B12	
26	IO_L18N_26	C13	
26	IO_L19P_26	H14	
26	IO_L19N_26	G13	
34	IO_L0P_GC_34	AE13	
34	IO_L0N_GC_34	AD12	
34	IO_L1P_GC_34	AB12	
34	IO_L1N_GC_34	AC13	
34	IO_L2P_A15_D31_34	W12	
34	IO_L2N_A14_D30_34	Y12	
34	IO_L3P_A13_D29_34	AB13	
34	IO_L3N_A12_D28_34	AA14	
34	IO_L4P_A11_D27_34	AF14	
34	IO_L4N_VREF_A10_D26_34	AG13	
34	IO_L5P_A09_D25_34	AB14	
34	IO_L5N_A08_D24_34	AC14	
34	IO_L6P_A07_D23_34	AD13	
34	IO_L6N_A06_D22_34	AE14	
34	IO_L7P_A05_D21_34	AH13	
34	IO_L7N_A04_D20_34	AH14	
34	IO_L8P_SRCC_34	Y13	
34	IO_L8N_SRCC_34	AA12	
34	IO_L9P_MRCC_34	AH15	
34	IO_L9N_MRCC_34	AH16	
34	IO_L10P_MRCC_34	AG14	
34	IO_L10N_MRCC_34	AF15	

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T (Cont'd)

Bank	Pin Description	Pin Number	NoConnect (NC)
34	IO_L11P_SRCC_34	AD15	
34	IO_L11N_SRCC_34	AC15	
34	IO_L12P_A03_D19_34	AE17	
34	IO_L12N_A02_D18_34	AD17	
34	IO_L13P_A01_D17_34	AF16	
34	IO_L13N_A00_D16_34	AG16	
34	IO_L14P_A25_34	AB16	
34	IO_L14N_VREF_A24_34	AC16	
34	IO_L15P_A23_34	AD16	
34	IO_L15N_A22_34	AE15	
34	IO_L16P_A21_34	AA15	
34	IO_L16N_A20_34	Y14	
34	IO_L17P_A19_34	AA16	
34	IO_L17N_A18_34	AB17	
34	IO_L18P_A17_34	W16	
34	IO_L18N_A16_34	Y15	
34	IO_L19P_VRN_34	Y17	
34	IO_L19N_VRP_34	AA17	
35	IO_L0P_35	W8	
35	IO_L0N_35	Y9	
35	IO_L1P_35	Y10	
35	IO_L1N_35	AA10	
35	IO_L2P_SM0P_35	AA7	
35	IO_L2N_SM0N_35	AB7	
35	IO_L3P_SM1P_35	AC9	
35	IO_L3N_SM1N_35	AD8	
35	IO_L4P_35	AA9	
35	IO_L4N_VREF_35	AB9	
35	IO_L5P_SM2P_35	AC10	
35	IO_L5N_SM2N_35	AD10	
35	IO_L6P_SM3P_35	AC8	
35	IO_L6N_SM3N_35	AB8	
35	IO_L7P_SM4P_35	AD11	

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T (Cont'd)

Bank	Pin Description	Pin Number	NoConnect (NC)
35	IO_L7N_SM4N_35	AC11	
35	IO_L8P_SRCC_35	W11	
35	IO_L8N_SRCC_35	W10	
35	IO_L9P_MRCC_35	AB11	
35	IO_L9N_MRCC_35	AA11	
35	IO_L10P_MRCC_35	AD7	
35	IO_L10N_MRCC_35	AE7	
35	IO_L11P_SRCC_35	AF11	
35	IO_L11N_SRCC_35	AG11	
35	IO_L12P_SM5P_35	AF7	
35	IO_L12N_SM5N_35	AE8	
35	IO_L13P_SM6P_35	AG9	
35	IO_L13N_SM6N_35	AH8	
35	IO_L14P_35	AE9	
35	IO_L14N_VREF_35	AF9	
35	IO_L15P_SM7P_35	AF12	
35	IO_L15N_SM7N_35	AE12	
35	IO_L16P_VRN_35	AG7	
35	IO_L16N_VRP_35	AG8	
35	IO_L17P_35	AH9	
35	IO_L17N_35	AH10	
35	IO_L18P_GC_35	AF10	
35	IO_L18N_GC_35	AE10	
35	IO_L19P_GC_35	AH11	
35	IO_L19N_GC_35	AG12	
36	IO_L0P_36	F11	
36	IO_L0N_36	E10	
36	IO_L1P_36	B8	
36	IO_L1N_36	C8	
36	IO_L2P_36	A10	
36	IO_L2N_36	A9	
36	IO_L3P_36	A7	
36	IO_L3N_36	B7	

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T (Cont'd)

Bank	Pin Description	Pin Number	NoConnect (NC)
36	IO_L4P_36	H13	
36	IO_L4N_VREF_36	J13	
36	IO_L5P_36	D8	
36	IO_L5N_36	E9	
36	IO_L6P_36	G11	
36	IO_L6N_36	F10	
36	IO_L7P_36	E8	
36	IO_L7N_36	F9	
36	IO_L8P_SRCC_36	D10	
36	IO_L8N_SRCC_36	C10	
36	IO_L9P_MRCC_36	F7	
36	IO_L9N_MRCC_36	G7	
36	IO_L10P_MRCC_36	H11	
36	IO_L10N_MRCC_36	H10	
36	IO_L11P_SRCC_36	J12	
36	IO_L11N_SRCC_36	K13	
36	IO_L12P_VRN_36	B9	
36	IO_L12N_VRP_36	C9	
36	IO_L13P_36	G8	
36	IO_L13N_36	G9	
36	IO_L14P_36	D7	
36	IO_L14N_VREF_36	E7	
36	IO_L15P_36	H8	
36	IO_L15N_36	H9	
36	IO_L16P_36	J11	
36	IO_L16N_36	J10	
36	IO_L17P_36	J7	
36	IO_L17N_36	J8	
36	IO_L18P_36	K9	
36	IO_L18N_36	K10	
36	IO_L19P_36	K7	
36	IO_L19N_36	L7	
114	MGTTXN3_114	Y2	

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T (Cont'd)

Bank	Pin Description	Pin Number	NoConnect (NC)
114	MGTRXN3_114	AC4	
114	MGTTXP3_114	Y1	
114	MGTRXP3_114	AC3	
114	MGTTXN2_114	AB2	
114	MGTRXN2_114	AE4	
114	MGTTXP2_114	AB1	
114	MGTREFCLK1P_114	W4	
114	MGTREFCLK1N_114	W3	
114	MGTRXP2_114	AE3	
114	MGTREFCLK0P_114	AA4	
114	MGTREFCLK0N_114	AA3	
114	MGTTXN1_114	AD2	
114	MGTRXN1_114	AG4	
114	MGTTXP1_114	AD1	
114	MGTRXP1_114	AG3	
114	MGTTXN0_114	AF2	
114	MGTRXN0_114	AH2	
114	MGTTXP0_114	AF1	
114	MGTRXP0_114	AH1	
115	MGTTXN3_115	M2	
115	MGTRXN3_115	L4	
115	MGTTXP3_115	M1	
115	MGTRXP3_115	L3	
115	MGTTXN2_115	P2	
115	MGTRXN2_115	N4	
115	MGTTXP2_115	P1	
115	MGTREFCLK1P_115	P6	
115	MGTREFCLK1N_115	P5	
115	MGTRXP2_115	N3	
115	MGTAVTTRCAL_115	A5	
115	MGTRREF_115	B5	
115	MGTREFCLK0P_115	T6	
115	MGTREFCLK0N_115	T5	

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T (Cont'd)

Bank	Pin Description	Pin Number	NoConnect (NC)
115	MGTTXN1_115	T2	
115	MGTRXN1_115	R4	
115	MGTTXP1_115	T1	
115	MGTRXP1_115	R3	
115	MGTTXN0_115	V2	
115	MGTRXN0_115	U4	
115	MGTTXP0_115	V1	
115	MGTRXP0_115	U3	
116	MGTTXN3_116	D2	
116	MGTRXN3_116	A4	
116	MGTTXP3_116	D1	
116	MGTRXP3_116	A3	
116	MGTTXN2_116	F2	
116	MGTRXN2_116	B2	
116	MGTTXP2_116	F1	
116	MGTREFCLK1P_116	G4	
116	MGTREFCLK1N_116	G3	
116	MGTRXP2_116	B1	
116	MGTREFCLK0P_116	J4	
116	MGTREFCLK0N_116	J3	
116	MGTTXN1_116	H2	
116	MGTRXN1_116	C4	
116	MGTTXP1_116	H1	
116	MGTRXP1_116	C3	
116	MGTTXN0_116	K2	
116	MGTRXN0_116	E4	
116	MGTTXP0_116	K1	
116	MGTRXP0_116	E3	
NA	GND	A1	
NA	GND	A2	
NA	GND	A6	
NA	GND	A8	
NA	GND	A18	

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T (Cont'd)

Bank	Pin Description	Pin Number	NoConnect (NC)
NA	GND	A28	
NA	GND	AA1	
NA	GND	AA2	
NA	GND	AA5	
NA	GND	AA8	
NA	GND	AA18	
NA	GND	AA28	
NA	GND	AB3	
NA	GND	AB5	
NA	GND	AB15	
NA	GND	AB25	
NA	GND	AC1	
NA	GND	AC5	
NA	GND	AC6	
NA	GND	AC12	
NA	GND	AC22	
NA	GND	AD3	
NA	GND	AD5	
NA	GND	AD9	
NA	GND	AD19	
NA	GND	AE1	
NA	GND	AE5	
NA	GND	AE6	
NA	GND	AE16	
NA	GND	AE26	
NA	GND	AF3	
NA	GND	AF5	
NA	GND	AF13	
NA	GND	AF23	
NA	GND	AG1	
NA	GND	AG5	
NA	GND	AG10	
NA	GND	AG20	

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T (Cont'd)

Bank	Pin Description	Pin Number	NoConnect (NC)
NA	GND	AH3	
NA	GND	AH5	
NA	GND	AH7	
NA	GND	AH17	
NA	GND	AH27	
NA	GND	B3	
NA	GND	B6	
NA	GND	B15	
NA	GND	B25	
NA	GND	C1	
NA	GND	C5	
NA	GND	C12	
NA	GND	C22	
NA	GND	D3	
NA	GND	D5	
NA	GND	D9	
NA	GND	D19	
NA	GND	E1	
NA	GND	E5	
NA	GND	E6	
NA	GND	E16	
NA	GND	E26	
NA	GND	F3	
NA	GND	F5	
NA	GND	F13	
NA	GND	F23	
NA	GND	G1	
NA	GND	G5	
NA	GND	G10	
NA	GND	G20	
NA	GND	H3	
NA	GND	H4	
NA	GND	H5	

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T (Cont'd)

Bank	Pin Description	Pin Number	NoConnect (NC)
NA	GND	H7	
NA	GND	H17	
NA	GND	H27	
NA	GND	J1	
NA	GND	J2	
NA	GND	J5	
NA	GND	J14	
NA	GND	J24	
NA	GND	K3	
NA	GND	K5	
NA	GND	K6	
NA	GND	K11	
NA	GND	K21	
NA	GND	L1	
NA	GND	L5	
NA	GND	L8	
NA	GND	L10	
NA	GND	L12	
NA	GND	L14	
NA	GND	L16	
NA	GND	L18	
NA	GND	L28	
NA	GND	M3	
NA	GND	M5	
NA	GND	M9	
NA	GND	M11	
NA	GND	M13	
NA	GND	M15	
NA	GND	M17	
NA	GND	M25	
NA	GND	N1	
NA	GND	N5	
NA	GND	N6	

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T (Cont'd)

Bank	Pin Description	Pin Number	NoConnect (NC)
NA	GND	N8	
NA	GND	N10	
NA	GND	N12	
NA	GND	N16	
NA	GND	N18	
NA	GND	N22	
NA	GND	P3	
NA	GND	P7	
NA	GND	P9	
NA	GND	P11	
NA	GND	P15	
NA	GND	P17	
NA	GND	P19	
NA	GND	R1	
NA	GND	R5	
NA	GND	R6	
NA	GND	R7	
NA	GND	R8	
NA	GND	R10	
NA	GND	R12	
NA	GND	R16	
NA	GND	R18	
NA	GND	R26	
NA	GND	T3	
NA	GND	T4	
NA	GND	T7	
NA	GND	T9	
NA	GND	T11	
NA	GND	T15	
NA	GND	T17	
NA	GND	T19	
NA	GND	T23	
NA	GND	U1	

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T (Cont'd)

Bank	Pin Description	Pin Number	NoConnect (NC)
NA	GND	U5	
NA	GND	U6	
NA	GND	U7	
NA	GND	U8	
NA	GND	U10	
NA	GND	U12	
NA	GND	U14	
NA	GND	U16	
NA	GND	U18	
NA	GND	U20	
NA	GND	V3	
NA	GND	V5	
NA	GND	V7	
NA	GND	V9	
NA	GND	V11	
NA	GND	V13	
NA	GND	V15	
NA	GND	V17	
NA	GND	V27	
NA	GND	W1	
NA	GND	W5	
NA	GND	W6	
NA	GND	W14	
NA	GND	W24	
NA	GND	Y3	
NA	GND	Y5	
NA	GND	Y11	
NA	GND	Y21	
NA	GND	G2	
NA	GND	W2	
NA	GND	B4	
NA	GND	AD4	
NA	GND	V6	

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T (Cont'd)

Bank	Pin Description	Pin Number	NoConnect (NC)
0	VCCO_0	W7	
0	VCCO_0	Y8	
14	VCCO_14	R21	
14	VCCO_14	T28	
14	VCCO_14	U25	
14	VCCO_14	V22	
14	VCCO_14	Y26	
15	VCCO_15	K26	
15	VCCO_15	L23	
15	VCCO_15	M20	
15	VCCO_15	N27	
15	VCCO_15	P24	
16	VCCO_16	C27	
16	VCCO_16	D24	
16	VCCO_16	F28	
16	VCCO_16	G25	
16	VCCO_16	H22	
23	VCCO_23	AB20	
23	VCCO_23	AE21	
23	VCCO_23	AF18	
23	VCCO_23	AH22	
23	VCCO_23	W19	
24	VCCO_24	AA23	
24	VCCO_24	AC27	
24	VCCO_24	AD24	
24	VCCO_24	AF28	
24	VCCO_24	AG25	
25	VCCO_25	A23	
25	VCCO_25	B20	
25	VCCO_25	E21	
25	VCCO_25	F18	
25	VCCO_25	J19	
26	VCCO_26	A13	

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T (Cont'd)

Bank	Pin Description	Pin Number	NoConnect (NC)
26	VCCO_26	C17	
26	VCCO_26	D14	
26	VCCO_26	E11	
26	VCCO_26	G15	
34	VCCO_34	AA13	
34	VCCO_34	AC17	
34	VCCO_34	AD14	
34	VCCO_34	AG15	
34	VCCO_34	Y16	
35	VCCO_35	AB10	
35	VCCO_35	AC7	
35	VCCO_35	AE11	
35	VCCO_35	AF8	
35	VCCO_35	AH12	
35	VCCO_35	W9	
36	VCCO_36	B10	
36	VCCO_36	C7	
36	VCCO_36	F8	
36	VCCO_36	H12	
36	VCCO_36	J9	
NA	VCCAUX	K8	
NA	VCCAUX	K20	
NA	VCCAUX	L19	
NA	VCCAUX	M8	
NA	VCCAUX	N19	
NA	VCCAUX	P8	
NA	VCCAUX	R19	
NA	VCCAUX	T8	
NA	VCCAUX	T20	
NA	VCCAUX	U19	
NA	VCCAUX	U9	
NA	VCCAUX	V8	
NA	VCCAUX	W20	

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T (Cont'd)

Bank	Pin Description	Pin Number	NoConnect (NC)
NA	VCCINT	K12	
NA	VCCINT	K14	
NA	VCCINT	K16	
NA	VCCINT	L9	
NA	VCCINT	L11	
NA	VCCINT	L13	
NA	VCCINT	L15	
NA	VCCINT	L17	
NA	VCCINT	M10	
NA	VCCINT	M12	
NA	VCCINT	M14	
NA	VCCINT	M16	
NA	VCCINT	M18	
NA	VCCINT	N9	
NA	VCCINT	N11	
NA	VCCINT	N15	
NA	VCCINT	N17	
NA	VCCINT	P10	
NA	VCCINT	P12	
NA	VCCINT	P16	
NA	VCCINT	P18	
NA	VCCINT	R9	
NA	VCCINT	R11	
NA	VCCINT	R15	
NA	VCCINT	R17	
NA	VCCINT	T10	
NA	VCCINT	T12	
NA	VCCINT	T16	
NA	VCCINT	T18	
NA	VCCINT	U11	
NA	VCCINT	U13	
NA	VCCINT	U15	
NA	VCCINT	U17	

Table 2-2: FF784/RF784 Package—LX75T, LX130T, LX195T, and LX240T (Cont'd)

Bank	Pin Description	Pin Number	NoConnect (NC)
NA	VCCINT	V10	
NA	VCCINT	V12	
NA	VCCINT	V14	
NA	VCCINT	V16	
NA	VCCINT	V18	
NA	VCCINT	W13	
NA	VCCINT	W15	
NA	VCCINT	W17	
NA	MGTAVCC	D4	
NA	MGTAVCC	F4	
NA	MGTAVCC	K4	
NA	MGTAVCC	M4	
NA	MGTAVCC	P4	
NA	MGTAVCC	V4	
NA	MGTAVCC	Y4	
NA	MGTAVCC	AB4	
NA	MGTAVCC	AF4	
NA	MGTAVCC	AH4	
NA	MGTAVTT	C2	
NA	MGTAVTT	E2	
NA	MGTAVTT	L2	
NA	MGTAVTT	N2	
NA	MGTAVTT	R2	
NA	MGTAVTT	U2	
NA	MGTAVTT	AC2	
NA	MGTAVTT	AE2	
NA	MGTAVTT	AG2	

FF1154 Package—HX250T and HX380T

Table 2-3: FF1154 Package—HX250T and HX380T

Bank	Pin Description	Pin Number	No Connect (NC)
0	INIT_B_0	L10	
0	DONE_0	M11	
0	M1_0	M24	
0	M2_0	L25	
0	HSWAPEN_0	M10	
0	PROGRAM_B_0	P25	
0	M0_0	M25	
0	AVSS_0	T17	
0	AVDD_0	T18	
0	VP_0	U18	
0	VREFP_0	V18	
0	VN_0	V17	
0	VREFN_0	U17	
0	DXP_0	W18	
0	DXN_0	W17	
0	VBATT_0	P10	
0	DIN_0	R10	
0	RDWR_B_0	AA25	
0	CSI_B_0	AB25	
0	DOUT_BUSY_0	AD25	
0	CCLK_0	AC24	
0	TDO_0	AA10	
0	TCK_0	AB10	
0	TMS_0	AD10	
0	TDI_0	AE10	
0	VFS_0	AE25	
22	IO_L0P_22	AK22	
22	IO_L0N_22	AL22	
22	IO_L1P_22	AN18	
22	IO_L1N_22	AP18	
22	IO_L2P_22	AM22	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
22	IO_L2N_22	AN22	
22	IO_L3P_22	AL19	
22	IO_L3N_22	AM19	
22	IO_L4P_22	AC18	
22	IO_L4N_VREF_22	AC19	
22	IO_L5P_22	AH19	
22	IO_L5N_22	AJ19	
22	IO_L6P_22	AJ21	
22	IO_L6N_22	AK21	
22	IO_L7P_22	AF19	
22	IO_L7N_22	AG19	
22	IO_L8P_SRCC_22	AG21	
22	IO_L8N_SRCC_22	AH21	
22	IO_L9P_MRCC_22	AD20	
22	IO_L9N_MRCC_22	AE20	
22	IO_L10P_MRCC_22	AL20	
22	IO_L10N_MRCC_22	AM20	
22	IO_L11P_SRCC_22	AK18	
22	IO_L11N_SRCC_22	AL18	
22	IO_L12P_VRN_22	AJ20	
22	IO_L12N_VRP_22	AK20	
22	IO_L13P_22	AH18	
22	IO_L13N_22	AJ18	
22	IO_L14P_22	AF20	
22	IO_L14N_VREF_22	AG20	
22	IO_L15P_22	AE18	
22	IO_L15N_22	AF18	
22	IO_L16P_22	AP20	
22	IO_L16N_22	AP21	
22	IO_L17P_22	AD18	
22	IO_L17N_22	AD19	
22	IO_L18P_22	AN19	
22	IO_L18N_22	AP19	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
22	IO_L19P_22	AM21	
22	IO_L19N_22	AN21	
23	IO_L0P_23	AN28	
23	IO_L0N_23	AP28	
23	IO_L1P_23	AC23	
23	IO_L1N_23	AD24	
23	IO_L2P_23	AN26	
23	IO_L2N_23	AP26	
23	IO_L3P_23	AD23	
23	IO_L3N_23	AE23	
23	IO_L4P_23	AM26	
23	IO_L4N_VREF_23	AN27	
23	IO_L5P_23	AH23	
23	IO_L5N_23	AJ23	
23	IO_L6P_23	AF25	
23	IO_L6N_23	AG25	
23	IO_L7P_23	AK23	
23	IO_L7N_23	AL23	
23	IO_L8P_SRCC_23	AK25	
23	IO_L8N_SRCC_23	AL25	
23	IO_L9P_MRCC_23	AE22	
23	IO_L9N_MRCC_23	AF22	
23	IO_L10P_MRCC_23	AL24	
23	IO_L10N_MRCC_23	AM25	
23	IO_L11P_SRCC_23	AG22	
23	IO_L11N_SRCC_23	AH22	
23	IO_L12P_VRN_23	AJ24	
23	IO_L12N_VRP_23	AJ25	
23	IO_L13P_23	AP24	
23	IO_L13N_23	AP25	
23	IO_L14P_23	AG24	
23	IO_L14N_VREF_23	AH24	
23	IO_L15P_23	AN23	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
23	IO_L15N_23	AP23	
23	IO_L16P_23	AF23	
23	IO_L16N_23	AF24	
23	IO_L17P_23	AD21	
23	IO_L17N_23	AE21	
23	IO_L18P_23	AC21	
23	IO_L18N_23	AC22	
23	IO_L19P_23	AM24	
23	IO_L19N_23	AN24	
24	IO_L0P_GC_24	M21	
24	IO_L0N_GC_24	M22	
24	IO_L1P_GC_24	K21	
24	IO_L1N_GC_24	J21	
24	IO_L2P_D15_24	B25	
24	IO_L2N_D14_24	B26	
24	IO_L3P_D13_24	H22	
24	IO_L3N_D12_24	G22	
24	IO_L4P_D11_24	B24	
24	IO_L4N_VREF_D10_24	A25	
24	IO_L5P_D9_24	D23	
24	IO_L5N_D8_24	C23	
24	IO_L6P_D7_24	C26	
24	IO_L6N_D6_24	C27	
24	IO_L7P_D5_24	F23	
24	IO_L7N_D4_24	E23	
24	IO_L8P_SRCC_24	D25	
24	IO_L8N_SRCC_24	D26	
24	IO_L9P_MRCC_24	L22	
24	IO_L9N_MRCC_24	K22	
24	IO_L10P_MRCC_24	F24	
24	IO_L10N_MRCC_24	E25	
24	IO_L11P_SRCC_24	J23	
24	IO_L11N_SRCC_24	H23	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
24	IO_L12P_D3_24	G25	
24	IO_L12N_D2_FS2_24	F25	
24	IO_L13P_D1_FS1_24	L23	
24	IO_L13N_D0_FS0_24	K23	
24	IO_L14P_FCS_B_24	H24	
24	IO_L14N_VREF_FOE_B_MOSI_24	G24	
24	IO_L15P_FWE_B_24	D24	
24	IO_L15N_RS1_24	C24	
24	IO_L16P_RS0_24	J24	
24	IO_L16N_CS0_B_24	J25	
24	IO_L17P_VRN_24	A23	
24	IO_L17N_VRP_24	A24	
24	IO_L18P_24	L24	
24	IO_L18N_24	K25	
24	IO_L19P_24	B27	
24	IO_L19N_24	A27	
25	IO_L0P_25	G20	
25	IO_L0N_25	F20	
25	IO_L1P_25	L18	
25	IO_L1N_25	K18	
25	IO_L2P_SM8P_25	E20	
25	IO_L2N_SM8N_25	D20	
25	IO_L3P_SM9P_25	J18	
25	IO_L3N_SM9N_25	H18	
25	IO_L4P_25	M19	
25	IO_L4N_VREF_25	L19	
25	IO_L5P_SM10P_25	F18	
25	IO_L5N_SM10N_25	E18	
25	IO_L6P_SM11P_25	M20	
25	IO_L6N_SM11N_25	L20	
25	IO_L7P_SM12P_25	D18	
25	IO_L7N_SM12N_25	C18	
25	IO_L8P_SRCC_25	K20	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
25	IO_L8N_SRCC_25	J20	
25	IO_L9P_MRCC_25	A18	
25	IO_L9N_MRCC_25	A19	
25	IO_L10P_MRCC_25	H21	
25	IO_L10N_MRCC_25	G21	
25	IO_L11P_SRCC_25	J19	
25	IO_L11N_SRCC_25	H19	
25	IO_L12P_SM13P_25	E21	
25	IO_L12N_SM13N_25	D21	
25	IO_L13P_SM14P_25	G19	
25	IO_L13N_SM14N_25	F19	
25	IO_L14P_25	C21	
25	IO_L14N_VREF_25	C22	
25	IO_L15P_SM15P_25	D19	
25	IO_L15N_SM15N_25	C19	
25	IO_L16P_VRN_25	F22	
25	IO_L16N_VRP_25	E22	
25	IO_L17P_25	B19	
25	IO_L17N_25	A20	
25	IO_L18P_GC_25	B22	
25	IO_L18N_GC_25	A22	
25	IO_L19P_GC_25	B20	
25	IO_L19N_GC_25	B21	
32	IO_L0P_32	AF14	
32	IO_L0N_32	AG14	
32	IO_L1P_32	AP16	
32	IO_L1N_32	AP15	
32	IO_L2P_32	AH14	
32	IO_L2N_32	AJ14	
32	IO_L3P_32	AM16	
32	IO_L3N_32	AN16	
32	IO_L4P_32	AM15	
32	IO_L4N_VREF_32	AN14	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
32	IO_L5P_32	AJ16	
32	IO_L5N_32	AK16	
32	IO_L6P_32	AK13	
32	IO_L6N_32	AL13	
32	IO_L7P_32	AG16	
32	IO_L7N_32	AH16	
32	IO_L8P_SRCC_32	AL15	
32	IO_L8N_SRCC_32	AL14	
32	IO_L9P_MRCC_32	AC17	
32	IO_L9N_MRCC_32	AC16	
32	IO_L10P_MRCC_32	AD15	
32	IO_L10N_MRCC_32	AE15	
32	IO_L11P_SRCC_32	AK17	
32	IO_L11N_SRCC_32	AL17	
32	IO_L12P_VRN_32	AF15	
32	IO_L12N_VRP_32	AG15	
32	IO_L13P_32	AD16	
32	IO_L13N_32	AE16	
32	IO_L14P_32	AJ15	
32	IO_L14N_VREF_32	AK15	
32	IO_L15P_32	AG17	
32	IO_L15N_32	AH17	
32	IO_L16P_32	AM14	
32	IO_L16N_32	AN13	
32	IO_L17P_32	AE17	
32	IO_L17N_32	AF17	
32	IO_L18P_32	AP14	
32	IO_L18N_32	AP13	
32	IO_L19P_32	AM17	
32	IO_L19N_32	AN17	
33	IO_L0P_33	AD11	
33	IO_L0N_33	AE11	
33	IO_L1P_33	AC12	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
33	IO_L1N_33	AC11	
33	IO_L2P_33	AE12	
33	IO_L2N_33	AF12	
33	IO_L3P_33	AG12	
33	IO_L3N_33	AH12	
33	IO_L4P_33	AN8	
33	IO_L4N_VREF_33	AN7	
33	IO_L5P_33	AK12	
33	IO_L5N_33	AL12	
33	IO_L6P_33	AF10	
33	IO_L6N_33	AG10	
33	IO_L7P_33	AM12	
33	IO_L7N_33	AN12	
33	IO_L8P_SRCC_33	AG11	
33	IO_L8N_SRCC_33	AH11	
33	IO_L9P_MRCC_33	AP11	
33	IO_L9N_MRCC_33	AP10	
33	IO_L10P_MRCC_33	AJ11	
33	IO_L10N_MRCC_33	AJ10	
33	IO_L11P_SRCC_33	AC13	
33	IO_L11N_SRCC_33	AD13	
33	IO_L12P_VRN_33	AK11	
33	IO_L12N_VRP_33	AK10	
33	IO_L13P_33	AE13	
33	IO_L13N_33	AF13	
33	IO_L14P_33	AL10	
33	IO_L14N_VREF_33	AM10	
33	IO_L15P_33	AH13	
33	IO_L15N_33	AJ13	
33	IO_L16P_33	AM9	
33	IO_L16N_33	AN9	
33	IO_L17P_33	AC14	
33	IO_L17N_33	AD14	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
33	IO_L18P_33	AP9	
33	IO_L18N_33	AP8	
33	IO_L19P_33	AM11	
33	IO_L19N_33	AN11	
34	IO_L0P_GC_34	E11	
34	IO_L0N_GC_34	D10	
34	IO_L1P_GC_34	M14	
34	IO_L1N_GC_34	L14	
34	IO_L2P_A15_D31_34	A9	
34	IO_L2N_A14_D30_34	A8	
34	IO_L3P_A13_D29_34	J14	
34	IO_L3N_A12_D28_34	H14	
34	IO_L4P_A11_D27_34	C12	
34	IO_L4N_VREF_A10_D26_34	B11	
34	IO_L5P_A09_D25_34	B12	
34	IO_L5N_A08_D24_34	A12	
34	IO_L6P_A07_D23_34	C9	
34	IO_L6N_A06_D22_34	B9	
34	IO_L7P_A05_D21_34	L13	
34	IO_L7N_A04_D20_34	K13	
34	IO_L8P_SRCC_34	F10	
34	IO_L8N_SRCC_34	E10	
34	IO_L9P_MRCC_34	J13	
34	IO_L9N_MRCC_34	H13	
34	IO_L10P_MRCC_34	G11	
34	IO_L10N_MRCC_34	G10	
34	IO_L11P_SRCC_34	B10	
34	IO_L11N_SRCC_34	A10	
34	IO_L12P_A03_D19_34	J11	
34	IO_L12N_A02_D18_34	H11	
34	IO_L13P_A01_D17_34	D11	
34	IO_L13N_A00_D16_34	C11	
34	IO_L14P_A25_34	K12	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
34	IO_L14N_VREF_A24_34	K11	
34	IO_L15P_A23_34	F12	
34	IO_L15N_A22_34	E12	
34	IO_L16P_A21_34	M12	
34	IO_L16N_A20_34	L12	
34	IO_L17P_A19_34	H12	
34	IO_L17N_A18_34	G12	
34	IO_L18P_A17_34	K10	
34	IO_L18N_A16_34	J10	
34	IO_L19P_VRN_34	D9	
34	IO_L19N_VRP_34	C8	
35	IO_L0P_35	M17	
35	IO_L0N_35	M16	
35	IO_L1P_35	L17	
35	IO_L1N_35	K17	
35	IO_L2P_SM0P_35	B15	
35	IO_L2N_SM0N_35	A15	
35	IO_L3P_SM1P_35	H17	
35	IO_L3N_SM1N_35	G17	
35	IO_L4P_35	B17	
35	IO_L4N_VREF_35	A17	
35	IO_L5P_SM2P_35	F17	
35	IO_L5N_SM2N_35	E17	
35	IO_L6P_SM3P_35	G15	
35	IO_L6N_SM3N_35	F15	
35	IO_L7P_SM4P_35	C17	
35	IO_L7N_SM4N_35	B16	
35	IO_L8P_SRCC_35	E15	
35	IO_L8N_SRCC_35	D14	
35	IO_L9P_MRCC_35	D16	
35	IO_L9N_MRCC_35	C16	
35	IO_L10P_MRCC_35	K15	
35	IO_L10N_MRCC_35	J15	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
35	IO_L11P_SRCC_35	K16	
35	IO_L11N_SRCC_35	J16	
35	IO_L12P_SM5P_35	G14	
35	IO_L12N_SM5N_35	F14	
35	IO_L13P_SM6P_35	M15	
35	IO_L13N_SM6N_35	L15	
35	IO_L14P_35	D13	
35	IO_L14N_VREF_35	C13	
35	IO_L15P_SM7P_35	H16	
35	IO_L15N_SM7N_35	G16	
35	IO_L16P_VRN_35	F13	
35	IO_L16N_VRP_35	E13	
35	IO_L17P_35	E16	
35	IO_L17N_35	D15	
35	IO_L18P_GC_35	A14	
35	IO_L18N_GC_35	A13	
35	IO_L19P_GC_35	C14	
35	IO_L19N_GC_35	B14	
100	MGTTXN3_100	AL31	
100	MGTRXN3_100	AF29	
100	MGTTXP3_100	AL32	
100	MGTRXP3_100	AF30	
100	MGTTXN2_100	AM33	
100	MGTRXN2_100	AG31	
100	MGTTXP2_100	AM34	
100	MGTREFCLK1P_100	AG27	
100	MGTREFCLK1N_100	AG28	
100	MGTRXP2_100	AG32	
100	MGTREFCLK0P_100	AJ27	
100	MGTREFCLK0N_100	AJ28	
100	MGTTXN1_100	AN31	
100	MGTRXN1_100	AH29	
100	MGTTXP1_100	AN32	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
100	MGTRXP1_100	AH30	
100	MGTTXN0_100	AP33	
100	MGTRXN0_100	AK29	
100	MGTTXP0_100	AP34	
100	MGTRXP0_100	AK30	
101	MGTTXN3_101	AF33	
101	MGTRXN3_101	AB29	
101	MGTTXP3_101	AF34	
101	MGTRXP3_101	AB30	
101	MGTTXN2_101	AH33	
101	MGTRXN2_101	AC31	
101	MGTTXP2_101	AH34	
101	MGTREFCLK1P_101	AC27	
101	MGTREFCLK1N_101	AC28	
101	MGTRXP2_101	AC32	
101	MGTREFCLK0P_101	AE27	
101	MGTREFCLK0N_101	AE28	
101	MGTTXN1_101	AJ31	
101	MGTRXN1_101	AD29	
101	MGTTXP1_101	AJ32	
101	MGTRXP1_101	AD30	
101	MGTTXN0_101	AK33	
101	MGTRXN0_101	AE31	
101	MGTTXP0_101	AK34	
101	MGTRXP0_101	AE32	
102	MGTTXN3_102	V33	
102	MGTRXN3_102	V29	
102	MGTTXP3_102	V34	
102	MGTRXP3_102	V30	
102	MGTTXN2_102	Y33	
102	MGTRXN2_102	W31	
102	MGTTXP2_102	Y34	
102	MGTREFCLK1P_102	W27	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
102	MGTREFCLK1N_102	W28	
102	MGTRXP2_102	W32	
102	MGTREFCLK0P_102	AA27	
102	MGTREFCLK0N_102	AA28	
102	MGTTXN1_102	AB33	
102	MGTRXN1_102	Y29	
102	MGTTXP1_102	AB34	
102	MGTRXP1_102	Y30	
102	MGTTXN0_102	AD33	
102	MGTRXN0_102	AA31	
102	MGTTXP0_102	AD34	
102	MGTRXP0_102	AA32	
103	MGTTXN3_103	K33	
103	MGTRXN3_103	P29	
103	MGTTXP3_103	K34	
103	MGTRXP3_103	P30	
103	MGTTXN2_103	M33	
103	MGTRXN2_103	T29	
103	MGTTXP2_103	M34	
103	MGTREFCLK1P_103	R27	
103	MGTREFCLK1N_103	R28	
103	MGTRXP2_103	T30	
103	MGTREFCLK0P_103	U27	
103	MGTREFCLK0N_103	U28	
103	MGTTXN1_103	P33	
103	MGTRXN1_103	R31	
103	MGTTXP1_103	P34	
103	MGTRXP1_103	R32	
103	MGTTXN0_103	T33	
103	MGTRXN0_103	U31	
103	MGTTXP0_103	T34	
103	MGTRXP0_103	U32	
104	MGTTXN3_104	E31	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
104	MGTRXN3_104	K29	
104	MGTTXP3_104	E32	
104	MGTRXP3_104	K30	
104	MGTTXN2_104	F33	
104	MGTRXN2_104	L31	
104	MGTTXP2_104	F34	
104	MGTREFCLK1P_104	L27	
104	MGTREFCLK1N_104	L28	
104	MGTRXP2_104	L32	
104	MGTREFCLK0P_104	N27	
104	MGTREFCLK0N_104	N28	
104	MGTTXN1_104	G31	
104	MGTRXN1_104	M29	
104	MGTTXP1_104	G32	
104	MGTRXP1_104	M30	
104	MGTTXN0_104	H33	
104	MGTRXN0_104	N31	
104	MGTTXP0_104	H34	
104	MGTRXP0_104	N32	
105	MGTTXN3_105	A31	
105	MGTRXN3_105	D29	
105	MGTTXP3_105	A32	
105	MGTRXP3_105	D30	
105	MGTTXN2_105	B33	
105	MGTRXN2_105	F29	
105	MGTTXP2_105	B34	
105	MGTREFCLK1P_105	G27	
105	MGTREFCLK1N_105	G28	
105	MGTRXP2_105	F30	
105	MGTAVTTRCAL_105	AP30	
105	MGTRREF_105	AM30	
105	MGTREFCLK0P_105	J27	
105	MGTREFCLK0N_105	J28	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
105	MGTTXN1_105	C31	
105	MGTRXN1_105	H29	
105	MGTTXP1_105	C32	
105	MGTRXP1_105	H30	
105	MGTTXN0_105	D33	
105	MGTRXN0_105	J31	
105	MGTTXP0_105	D34	
105	MGTRXP0_105	J32	
110	MGTTXN3_110	AL4	
110	MGTRXN3_110	AF6	
110	MGTTXP3_110	AL3	
110	MGTRXP3_110	AF5	
110	MGTTXN2_110	AM2	
110	MGTRXN2_110	AG4	
110	MGTTXP2_110	AM1	
110	MGTREFCLK1P_110	AG8	
110	MGTREFCLK1N_110	AG7	
110	MGTRXP2_110	AG3	
110	MGTREFCLK0P_110	AJ8	
110	MGTREFCLK0N_110	AJ7	
110	MGTTXN1_110	AN4	
110	MGTRXN1_110	AH6	
110	MGTTXP1_110	AN3	
110	MGTRXP1_110	AH5	
110	MGTTXN0_110	AP2	
110	MGTRXN0_110	AK6	
110	MGTTXP0_110	AP1	
110	MGTRXP0_110	AK5	
111	MGTTXN3_111	AF2	
111	MGTRXN3_111	AB6	
111	MGTTXP3_111	AF1	
111	MGTRXP3_111	AB5	
111	MGTTXN2_111	AH2	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
111	MGTRXN2_111	AC4	
111	MGTTXP2_111	AH1	
111	MGTREFCLK1P_111	AC8	
111	MGTREFCLK1N_111	AC7	
111	MGTRXP2_111	AC3	
111	MGTREFCLK0P_111	AE8	
111	MGTREFCLK0N_111	AE7	
111	MGTTXN1_111	AJ4	
111	MGTRXN1_111	AD6	
111	MGTTXP1_111	AJ3	
111	MGTRXP1_111	AD5	
111	MGTTXN0_111	AK2	
111	MGTRXN0_111	AE4	
111	MGTTXP0_111	AK1	
111	MGTRXP0_111	AE3	
112	MGTTXN3_112	V2	
112	MGTRXN3_112	V6	
112	MGTTXP3_112	V1	
112	MGTRXP3_112	V5	
112	MGTTXN2_112	Y2	
112	MGTRXN2_112	W4	
112	MGTTXP2_112	Y1	
112	MGTREFCLK1P_112	W8	
112	MGTREFCLK1N_112	W7	
112	MGTRXP2_112	W3	
112	MGTREFCLK0P_112	AA8	
112	MGTREFCLK0N_112	AA7	
112	MGTTXN1_112	AB2	
112	MGTRXN1_112	Y6	
112	MGTTXP1_112	AB1	
112	MGTRXP1_112	Y5	
112	MGTTXN0_112	AD2	
112	MGTRXN0_112	AA4	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
112	MGTTXP0_112	AD1	
112	MGTRXP0_112	AA3	
113	MGTTXN3_113	K2	
113	MGTRXN3_113	P6	
113	MGTTXP3_113	K1	
113	MGTRXP3_113	P5	
113	MGTTXN2_113	M2	
113	MGTRXN2_113	T6	
113	MGTTXP2_113	M1	
113	MGTREFCLK1P_113	R8	
113	MGTREFCLK1N_113	R7	
113	MGTRXP2_113	T5	
113	MGTREFCLK0P_113	U8	
113	MGTREFCLK0N_113	U7	
113	MGTTXN1_113	P2	
113	MGTRXN1_113	R4	
113	MGTTXP1_113	P1	
113	MGTRXP1_113	R3	
113	MGTTXN0_113	T2	
113	MGTRXN0_113	U4	
113	MGTTXP0_113	T1	
113	MGTRXP0_113	U3	
114	MGTTXN3_114	E4	
114	MGTRXN3_114	K6	
114	MGTTXP3_114	E3	
114	MGTRXP3_114	K5	
114	MGTTXN2_114	F2	
114	MGTRXN2_114	L4	
114	MGTTXP2_114	F1	
114	MGTREFCLK1P_114	L8	
114	MGTREFCLK1N_114	L7	
114	MGTRXP2_114	L3	
114	MGTREFCLK0P_114	N8	

Table 2-3: FF1154 Package—HX250T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
114	MGTREFCLK0N_114	N7	
114	MGTTXN1_114	G4	
114	MGTRXN1_114	M6	
114	MGTTXP1_114	G3	
114	MGTRXP1_114	M5	
114	MGTTXN0_114	H2	
114	MGTRXN0_114	N4	
114	MGTTXP0_114	H1	
114	MGTRXP0_114	N3	
115	MGTTXN3_115	A4	
115	MGTRXN3_115	D6	
115	MGTTXP3_115	A3	
115	MGTRXP3_115	D5	
115	MGTTXN2_115	B2	
115	MGTRXN2_115	F6	
115	MGTTXP2_115	B1	
115	MGTREFCLK1P_115	G8	
115	MGTREFCLK1N_115	G7	
115	MGTRXP2_115	F5	
115	MGTAVTTRCAL_115	AP5	
115	MGTRREF_115	AM5	
115	MGTREFCLK0P_115	J8	
115	MGTREFCLK0N_115	J7	
115	MGTTXN1_115	C4	
115	MGTRXN1_115	H6	
115	MGTTXP1_115	C3	
115	MGTRXP1_115	H5	
115	MGTTXN0_115	D2	
115	MGTRXN0_115	J4	
115	MGTTXP0_115	D1	
115	MGTRXP0_115	J3	
NA	MGTAVCC_RN	E7	
NA	MGTAVCC_RN	F8	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTAVCC_RN	H8	
NA	MGTAVCC_RN	K8	
NA	MGTAVCC_RN	M8	
NA	MGTAVCC_RN	P8	
NA	MGTAVCC_RN	T8	
NA	MGTAVCC_RN	V8	
NA	MGTAVTT_RN	C2	
NA	MGTAVTT_RN	D3	
NA	MGTAVTT_RN	G2	
NA	MGTAVTT_RN	H3	
NA	MGTAVTT_RN	L2	
NA	MGTAVTT_RN	M3	
NA	MGTAVTT_RN	R2	
NA	MGTAVTT_RN	T3	
NA	MGTAVCC_RS	AB8	
NA	MGTAVCC_RS	AD8	
NA	MGTAVCC_RS	AF8	
NA	MGTAVCC_RS	AH8	
NA	MGTAVCC_RS	AK8	
NA	MGTAVCC_RS	AL7	
NA	MGTAVCC_RS	Y8	
NA	MGTAVTT_RS	AC2	
NA	MGTAVTT_RS	AD3	
NA	MGTAVTT_RS	AG2	
NA	MGTAVTT_RS	AH3	
NA	MGTAVTT_RS	AL2	
NA	MGTAVTT_RS	AM3	
NA	MGTAVTT_RS	W2	
NA	MGTAVTT_RS	Y3	
NA	MGTAVCC_LN	E28	
NA	MGTAVCC_LN	F27	
NA	MGTAVCC_LN	H27	
NA	MGTAVCC_LN	K27	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTAVCC_LN	M27	
NA	MGTAVCC_LN	P27	
NA	MGTAVCC_LN	T27	
NA	MGTAVCC_LN	V27	
NA	MGTAVTT_LN	C33	
NA	MGTAVTT_LN	D32	
NA	MGTAVTT_LN	G33	
NA	MGTAVTT_LN	H32	
NA	MGTAVTT_LN	L33	
NA	MGTAVTT_LN	M32	
NA	MGTAVTT_LN	R33	
NA	MGTAVTT_LN	T32	
NA	MGTAVCC_LS	AB27	
NA	MGTAVCC_LS	AD27	
NA	MGTAVCC_LS	AF27	
NA	MGTAVCC_LS	AH27	
NA	MGTAVCC_LS	AK27	
NA	MGTAVCC_LS	AL28	
NA	MGTAVCC_LS	Y27	
NA	MGTAVTT_LS	AC33	
NA	MGTAVTT_LS	AD32	
NA	MGTAVTT_LS	AG33	
NA	MGTAVTT_LS	AH32	
NA	MGTAVTT_LS	AL33	
NA	MGTAVTT_LS	AM32	
NA	MGTAVTT_LS	W33	
NA	MGTAVTT_LS	Y32	
NA	GND	A1	
NA	GND	A2	
NA	GND	A5	
NA	GND	A6	
NA	GND	A7	
NA	GND	A11	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	A21	
NA	GND	A28	
NA	GND	A29	
NA	GND	A30	
NA	GND	A33	
NA	GND	A34	
NA	GND	AA1	
NA	GND	AA2	
NA	GND	AA5	
NA	GND	AA6	
NA	GND	AA9	
NA	GND	AA11	
NA	GND	AA13	
NA	GND	AA15	
NA	GND	AA17	
NA	GND	AA19	
NA	GND	AA21	
NA	GND	AA23	
NA	GND	AA26	
NA	GND	AA29	
NA	GND	AA30	
NA	GND	AA33	
NA	GND	AA34	
NA	GND	AB3	
NA	GND	AB4	
NA	GND	AB7	
NA	GND	AB9	
NA	GND	AB12	
NA	GND	AB14	
NA	GND	AB16	
NA	GND	AB18	
NA	GND	AB20	
NA	GND	AB22	

Table 2-3: FF1154 Package—HX250T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AB24	
NA	GND	AB26	
NA	GND	AB28	
NA	GND	AB31	
NA	GND	AB32	
NA	GND	AC1	
NA	GND	AC5	
NA	GND	AC6	
NA	GND	AC9	
NA	GND	AC15	
NA	GND	AC25	
NA	GND	AC26	
NA	GND	AC29	
NA	GND	AC30	
NA	GND	AC34	
NA	GND	AD4	
NA	GND	AD7	
NA	GND	AD9	
NA	GND	AD12	
NA	GND	AD22	
NA	GND	AD26	
NA	GND	AD28	
NA	GND	AD31	
NA	GND	AE1	
NA	GND	AE2	
NA	GND	AE5	
NA	GND	AE6	
NA	GND	AE9	
NA	GND	AE19	
NA	GND	AE26	
NA	GND	AE29	
NA	GND	AE30	
NA	GND	AE33	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AE34	
NA	GND	AF3	
NA	GND	AF4	
NA	GND	AF7	
NA	GND	AF9	
NA	GND	AF16	
NA	GND	AF26	
NA	GND	AF28	
NA	GND	AF31	
NA	GND	AF32	
NA	GND	AG1	
NA	GND	AG5	
NA	GND	AG6	
NA	GND	AG9	
NA	GND	AG13	
NA	GND	AG23	
NA	GND	AG26	
NA	GND	AG29	
NA	GND	AG30	
NA	GND	AG34	
NA	GND	AH4	
NA	GND	AH7	
NA	GND	AH9	
NA	GND	AH10	
NA	GND	AH20	
NA	GND	AH26	
NA	GND	AH28	
NA	GND	AH31	
NA	GND	AJ1	
NA	GND	AJ2	
NA	GND	AJ5	
NA	GND	AJ6	
NA	GND	AJ9	

Table 2-3: FF1154 Package—HX250T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AJ17	
NA	GND	AJ26	
NA	GND	AJ29	
NA	GND	AJ30	
NA	GND	AJ33	
NA	GND	AJ34	
NA	GND	AK3	
NA	GND	AK4	
NA	GND	AK7	
NA	GND	AK9	
NA	GND	AK14	
NA	GND	AK24	
NA	GND	AK26	
NA	GND	AK28	
NA	GND	AK31	
NA	GND	AK32	
NA	GND	AL1	
NA	GND	AL5	
NA	GND	AL6	
NA	GND	AL8	
NA	GND	AL9	
NA	GND	AL11	
NA	GND	AL21	
NA	GND	AL26	
NA	GND	AL27	
NA	GND	AL29	
NA	GND	AL30	
NA	GND	AL34	
NA	GND	AM4	
NA	GND	AM6	
NA	GND	AM7	
NA	GND	AM8	
NA	GND	AM18	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AM27	
NA	GND	AM28	
NA	GND	AM29	
NA	GND	AM31	
NA	GND	AN1	
NA	GND	AN2	
NA	GND	AN5	
NA	GND	AN6	
NA	GND	AN15	
NA	GND	AN25	
NA	GND	AN29	
NA	GND	AN30	
NA	GND	AN33	
NA	GND	AN34	
NA	GND	AP3	
NA	GND	AP4	
NA	GND	AP6	
NA	GND	AP12	
NA	GND	AP22	
NA	GND	AP29	
NA	GND	AP31	
NA	GND	AP32	
NA	GND	B3	
NA	GND	B4	
NA	GND	B5	
NA	GND	B6	
NA	GND	B7	
NA	GND	B8	
NA	GND	B18	
NA	GND	B28	
NA	GND	B29	
NA	GND	B30	
NA	GND	B31	

Table 2-3: FF1154 Package—HX250T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	B32	
NA	GND	C1	
NA	GND	C5	
NA	GND	C6	
NA	GND	C7	
NA	GND	C15	
NA	GND	C25	
NA	GND	C28	
NA	GND	C29	
NA	GND	C30	
NA	GND	C34	
NA	GND	D4	
NA	GND	D7	
NA	GND	D8	
NA	GND	D12	
NA	GND	D22	
NA	GND	D27	
NA	GND	D28	
NA	GND	D31	
NA	GND	E1	
NA	GND	E2	
NA	GND	E5	
NA	GND	E6	
NA	GND	E8	
NA	GND	E9	
NA	GND	E19	
NA	GND	E26	
NA	GND	E27	
NA	GND	E29	
NA	GND	E30	
NA	GND	E33	
NA	GND	E34	
NA	GND	F3	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	F4	
NA	GND	F7	
NA	GND	F9	
NA	GND	F16	
NA	GND	F26	
NA	GND	F28	
NA	GND	F31	
NA	GND	F32	
NA	GND	G1	
NA	GND	G5	
NA	GND	G6	
NA	GND	G9	
NA	GND	G13	
NA	GND	G23	
NA	GND	G26	
NA	GND	G29	
NA	GND	G30	
NA	GND	G34	
NA	GND	H4	
NA	GND	H7	
NA	GND	H9	
NA	GND	H10	
NA	GND	H20	
NA	GND	H26	
NA	GND	H28	
NA	GND	H31	
NA	GND	J1	
NA	GND	J2	
NA	GND	J5	
NA	GND	J6	
NA	GND	J9	
NA	GND	J17	
NA	GND	J26	

Table 2-3: FF1154 Package—HX250T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	J29	
NA	GND	J30	
NA	GND	J33	
NA	GND	J34	
NA	GND	K3	
NA	GND	K4	
NA	GND	K7	
NA	GND	K9	
NA	GND	K14	
NA	GND	K24	
NA	GND	K26	
NA	GND	K28	
NA	GND	K31	
NA	GND	K32	
NA	GND	L1	
NA	GND	L5	
NA	GND	L6	
NA	GND	L9	
NA	GND	L11	
NA	GND	L21	
NA	GND	L26	
NA	GND	L29	
NA	GND	L30	
NA	GND	L34	
NA	GND	M4	
NA	GND	M7	
NA	GND	M9	
NA	GND	M18	
NA	GND	M26	
NA	GND	M28	
NA	GND	M31	
NA	GND	N1	
NA	GND	N2	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	N5	
NA	GND	N6	
NA	GND	N9	
NA	GND	N11	
NA	GND	N13	
NA	GND	N15	
NA	GND	N17	
NA	GND	N19	
NA	GND	N21	
NA	GND	N23	
NA	GND	N25	
NA	GND	N26	
NA	GND	N29	
NA	GND	N30	
NA	GND	N33	
NA	GND	N34	
NA	GND	P3	
NA	GND	P4	
NA	GND	P7	
NA	GND	P9	
NA	GND	P12	
NA	GND	P14	
NA	GND	P16	
NA	GND	P18	
NA	GND	P20	
NA	GND	P22	
NA	GND	P24	
NA	GND	P26	
NA	GND	P28	
NA	GND	P31	
NA	GND	P32	
NA	GND	R1	
NA	GND	R5	

Table 2-3: FF1154 Package—HX250T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	R6	
NA	GND	R9	
NA	GND	R11	
NA	GND	R13	
NA	GND	R15	
NA	GND	R17	
NA	GND	R19	
NA	GND	R21	
NA	GND	R23	
NA	GND	R25	
NA	GND	R26	
NA	GND	R29	
NA	GND	R30	
NA	GND	R34	
NA	GND	T4	
NA	GND	T7	
NA	GND	T9	
NA	GND	T10	
NA	GND	T12	
NA	GND	T14	
NA	GND	T16	
NA	GND	T20	
NA	GND	T22	
NA	GND	T24	
NA	GND	T25	
NA	GND	T26	
NA	GND	T28	
NA	GND	T31	
NA	GND	U1	
NA	GND	U2	
NA	GND	U5	
NA	GND	U6	
NA	GND	U9	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	U10	
NA	GND	U11	
NA	GND	U13	
NA	GND	U15	
NA	GND	U19	
NA	GND	U21	
NA	GND	U23	
NA	GND	U25	
NA	GND	U26	
NA	GND	U29	
NA	GND	U30	
NA	GND	U33	
NA	GND	U34	
NA	GND	V3	
NA	GND	V4	
NA	GND	V7	
NA	GND	V9	
NA	GND	V10	
NA	GND	V12	
NA	GND	V14	
NA	GND	V16	
NA	GND	V20	
NA	GND	V22	
NA	GND	V24	
NA	GND	V25	
NA	GND	V26	
NA	GND	V28	
NA	GND	V31	
NA	GND	V32	
NA	GND	W1	
NA	GND	W5	
NA	GND	W6	
NA	GND	W9	

Table 2-3: FF1154 Package—HX250T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	W10	
NA	GND	W11	
NA	GND	W13	
NA	GND	W15	
NA	GND	W19	
NA	GND	W21	
NA	GND	W23	
NA	GND	W25	
NA	GND	W26	
NA	GND	W29	
NA	GND	W30	
NA	GND	W34	
NA	GND	Y4	
NA	GND	Y7	
NA	GND	Y9	
NA	GND	Y10	
NA	GND	Y12	
NA	GND	Y14	
NA	GND	Y16	
NA	GND	Y18	
NA	GND	Y20	
NA	GND	Y22	
NA	GND	Y24	
NA	GND	Y25	
NA	GND	Y26	
NA	GND	Y28	
NA	GND	Y31	
NA	VCCAUX	AA24	
NA	VCCAUX	AB11	
NA	VCCAUX	AB23	
NA	VCCAUX	N12	
NA	VCCAUX	N24	
NA	VCCAUX	P11	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCAUX	R24	
NA	VCCAUX	T11	
NA	VCCAUX	U24	
NA	VCCAUX	V11	
NA	VCCAUX	W24	
NA	VCCAUX	Y11	
NA	VCCINT	AA12	
NA	VCCINT	AA14	
NA	VCCINT	AA16	
NA	VCCINT	AA18	
NA	VCCINT	AA20	
NA	VCCINT	AA22	
NA	VCCINT	AB13	
NA	VCCINT	AB15	
NA	VCCINT	AB17	
NA	VCCINT	AB19	
NA	VCCINT	AB21	
NA	VCCINT	N14	
NA	VCCINT	N16	
NA	VCCINT	N18	
NA	VCCINT	N20	
NA	VCCINT	N22	
NA	VCCINT	P13	
NA	VCCINT	P15	
NA	VCCINT	P17	
NA	VCCINT	P19	
NA	VCCINT	P21	
NA	VCCINT	P23	
NA	VCCINT	R12	
NA	VCCINT	R14	
NA	VCCINT	R16	
NA	VCCINT	R18	
NA	VCCINT	R20	

Table 2-3: FF1154 Package—HX250T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	R22	
NA	VCCINT	T13	
NA	VCCINT	T15	
NA	VCCINT	T19	
NA	VCCINT	T21	
NA	VCCINT	T23	
NA	VCCINT	U12	
NA	VCCINT	U14	
NA	VCCINT	U16	
NA	VCCINT	U20	
NA	VCCINT	U22	
NA	VCCINT	V13	
NA	VCCINT	V15	
NA	VCCINT	V19	
NA	VCCINT	V21	
NA	VCCINT	V23	
NA	VCCINT	W12	
NA	VCCINT	W14	
NA	VCCINT	W16	
NA	VCCINT	W20	
NA	VCCINT	W22	
NA	VCCINT	Y13	
NA	VCCINT	Y15	
NA	VCCINT	Y17	
NA	VCCINT	Y19	
NA	VCCINT	Y21	
NA	VCCINT	Y23	
0	VCCO_0	AC10	
0	VCCO_0	N10	
22	VCCO_22	AC20	
22	VCCO_22	AG18	
22	VCCO_22	AJ22	
22	VCCO_22	AK19	

Table 2-3: FF1154 Package—HX250T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
22	VCCO_22	AN20	
23	VCCO_23	AE24	
23	VCCO_23	AF21	
23	VCCO_23	AH25	
23	VCCO_23	AM23	
23	VCCO_23	AP27	
24	VCCO_24	A26	
24	VCCO_24	E24	
24	VCCO_24	H25	
24	VCCO_24	J22	
24	VCCO_24	M23	
25	VCCO_25	B23	
25	VCCO_25	C20	
25	VCCO_25	F21	
25	VCCO_25	G18	
25	VCCO_25	K19	
32	VCCO_32	AD17	
32	VCCO_32	AH15	
32	VCCO_32	AL16	
32	VCCO_32	AM13	
32	VCCO_32	AP17	
33	VCCO_33	AE14	
33	VCCO_33	AF11	
33	VCCO_33	AJ12	
33	VCCO_33	AN10	
33	VCCO_33	AP7	
34	VCCO_34	B13	
34	VCCO_34	C10	
34	VCCO_34	F11	
34	VCCO_34	J12	
34	VCCO_34	M13	
35	VCCO_35	A16	
35	VCCO_35	D17	

Table 2-3: FF1154 Package—HX250T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
35	VCCO_35	E14	
35	VCCO_35	H15	
35	VCCO_35	L16	

FF1155 Package—HX255T and HX380T

Table 2-4: FF1155 Package—HX255T and HX380T

Bank	Pin Description	Pin Number	No Connect (NC)
0	INIT_B_0	T9	
0	DONE_0	U8	
0	M1_0	P25	
0	M2_0	R25	
0	HSWAPEN_0	U10	
0	PROGRAM_B_0	U25	
0	M0_0	T25	
0	AVSS_0	T17	
0	AVDD_0	T18	
0	VP_0	U18	
0	VREFP_0	V18	
0	VN_0	V17	
0	VREFN_0	U17	
0	DXP_0	W18	
0	DXN_0	W17	
0	VBATT_0	R9	
0	DIN_0	T8	
0	RDWR_B_0	Y25	
0	CSI_B_0	W25	
0	DOUT_BUSY_0	W26	
0	CCLK_0	Y10	
0	TDO_0	W9	
0	TCK_0	W8	
0	TMS_0	W10	
0	TDI_0	V9	
0	VFS_0	AA25	
23	IO_L0P_23	AJ21	
23	IO_L0N_23	AK21	
23	IO_L1P_23	AG21	
23	IO_L1N_23	AH21	
23	IO_L2P_23	AM21	

Table 2-4: FF1155 Package—HX255T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
23	IO_L2N_23	AN22	
23	IO_L3P_23	AN19	
23	IO_L3N_23	AP19	
23	IO_L4P_23	AC21	
23	IO_L4N_VREF_23	AD21	
23	IO_L5P_23	AE20	
23	IO_L5N_23	AE21	
23	IO_L6P_23	AM20	
23	IO_L6N_23	AN21	
23	IO_L7P_23	AL19	
23	IO_L7N_23	AM19	
23	IO_L8P_SRCC_23	AK20	
23	IO_L8N_SRCC_23	AL20	
23	IO_L9P_MRCC_23	AG19	
23	IO_L9N_MRCC_23	AH19	
23	IO_L10P_MRCC_23	AF20	
23	IO_L10N_MRCC_23	AG20	
23	IO_L11P_SRCC_23	AK18	
23	IO_L11N_SRCC_23	AL18	
23	IO_L12P_VRN_23	AD19	
23	IO_L12N_VRP_23	AD20	
23	IO_L13P_23	AF18	
23	IO_L13N_23	AF19	
23	IO_L14P_23	AJ19	
23	IO_L14N_VREF_23	AJ20	
23	IO_L15P_23	AH18	
23	IO_L15N_23	AJ18	
23	IO_L16P_23	AP20	
23	IO_L16N_23	AP21	
23	IO_L17P_23	AD18	
23	IO_L17N_23	AE18	
23	IO_L18P_23	AN18	
23	IO_L18N_23	AP18	

Table 2-4: FF1155 Package—HX255T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
23	IO_L19P_23	AC18	
23	IO_L19N_23	AC19	
24	IO_L0P_GC_24	AE25	
24	IO_L0N_GC_24	AF25	
24	IO_L1P_GC_24	AL25	
24	IO_L1N_GC_24	AM25	
24	IO_L2P_D15_24	AF24	
24	IO_L2N_D14_24	AG25	
24	IO_L3P_D13_24	AL23	
24	IO_L3N_D12_24	AL24	
24	IO_L4P_D11_24	AB24	
24	IO_L4N_VREF_D10_24	AC24	
24	IO_L5P_D9_24	AD23	
24	IO_L5N_D8_24	AE23	
24	IO_L6P_D7_24	AJ25	
24	IO_L6N_D6_24	AK25	
24	IO_L7P_D5_24	AC22	
24	IO_L7N_D4_24	AC23	
24	IO_L8P_SRCC_24	AN26	
24	IO_L8N_SRCC_24	AP26	
24	IO_L9P_MRCC_24	AE22	
24	IO_L9N_MRCC_24	AF23	
24	IO_L10P_MRCC_24	AP24	
24	IO_L10N_MRCC_24	AP25	
24	IO_L11P_SRCC_24	AH22	
24	IO_L11N_SRCC_24	AH23	
24	IO_L12P_D3_24	AG24	
24	IO_L12N_D2_FS2_24	AH24	
24	IO_L13P_D1_FS1_24	AK22	
24	IO_L13N_D0_FS0_24	AK23	
24	IO_L14P_FCS_B_24	AJ23	
24	IO_L14N_VREF_FOE_B_MOSI_24	AJ24	
24	IO_L15P_FWE_B_24	AL22	

Table 2-4: FF1155 Package—HX255T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
24	IO_L15N_RS1_24	AM22	
24	IO_L16P_RS0_24	AM24	
24	IO_L16N_CS0_B_24	AN24	
24	IO_L17P_VRN_24	AF22	
24	IO_L17N_VRP_24	AG22	
24	IO_L18P_24	AN23	
24	IO_L18N_24	AP23	
24	IO_L19P_24	AD24	
24	IO_L19N_24	AD25	
25	IO_L0P_25	N32	
25	IO_L0N_25	M32	
25	IO_L1P_25	P33	
25	IO_L1N_25	N33	
25	IO_L2P_SM8P_25	R28	
25	IO_L2N_SM8N_25	P28	
25	IO_L3P_SM9P_25	R30	
25	IO_L3N_SM9N_25	P30	
25	IO_L4P_25	N27	
25	IO_L4N_VREF_25	N28	
25	IO_L5P_SM10P_25	N34	
25	IO_L5N_SM10N_25	M34	
25	IO_L6P_SM11P_25	R26	
25	IO_L6N_SM11N_25	R27	
25	IO_L7P_SM12P_25	T29	
25	IO_L7N_SM12N_25	T30	
25	IO_L8P_SRCC_25	P29	
25	IO_L8N_SRCC_25	N29	
25	IO_L9P_MRCC_25	R33	
25	IO_L9N_MRCC_25	P34	
25	IO_L10P_MRCC_25	U31	
25	IO_L10N_MRCC_25	T32	
25	IO_L11P_SRCC_25	T27	
25	IO_L11N_SRCC_25	T28	

Table 2-4: FF1155 Package—HX255T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
25	IO_L12P_SM13P_25	P31	
25	IO_L12N_SM13N_25	N31	
25	IO_L13P_SM14P_25	T33	
25	IO_L13N_SM14N_25	T34	
25	IO_L14P_25	U26	
25	IO_L14N_VREF_25	U27	
25	IO_L15P_SM15P_25	U29	
25	IO_L15N_SM15N_25	U30	
25	IO_L16P_VRN_25	R31	
25	IO_L16N_VRP_25	R32	
25	IO_L17P_25	P26	
25	IO_L17N_25	N26	
25	IO_L18P_GC_25	V26	
25	IO_L18N_GC_25	V27	
25	IO_L19P_GC_25	V28	
25	IO_L19N_GC_25	V29	
26	IO_L0P_26	D33	
26	IO_L0N_26	C34	
26	IO_L1P_26	D31	
26	IO_L1N_26	C32	
26	IO_L2P_26	H32	
26	IO_L2N_26	H33	
26	IO_L3P_26	E31	
26	IO_L3N_26	E32	
26	IO_L4P_26	L27	
26	IO_L4N_VREF_26	K28	
26	IO_L5P_26	G31	
26	IO_L5N_26	F32	
26	IO_L6P_26	K33	
26	IO_L6N_26	J33	
26	IO_L7P_26	G32	
26	IO_L7N_26	F33	
26	IO_L8P_SRCC_26	E33	

Table 2-4: FF1155 Package—HX255T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
26	IO_L8N_SRCC_26	D34	
26	IO_L9P_MRCC_26	C33	
26	IO_L9N_MRCC_26	B34	
26	IO_L10P_MRCC_26	G34	
26	IO_L10N_MRCC_26	F34	
26	IO_L11P_SRCC_26	J31	
26	IO_L11N_SRCC_26	H31	
26	IO_L12P_VRN_26	J34	
26	IO_L12N_VRP_26	H34	
26	IO_L13P_26	K31	
26	IO_L13N_26	K32	
26	IO_L14P_26	L33	
26	IO_L14N_VREF_26	L34	
26	IO_L15P_26	L28	
26	IO_L15N_26	L29	
26	IO_L16P_26	M31	
26	IO_L16N_26	L32	
26	IO_L17P_26	L30	
26	IO_L17N_26	K30	
26	IO_L18P_26	M29	
26	IO_L18N_26	M30	
26	IO_L19P_26	M26	
26	IO_L19N_26	M27	
27	IO_L0P_27	J24	
27	IO_L0N_27	H24	
27	IO_L1P_27	H26	
27	IO_L1N_27	G27	
27	IO_L2P_27	J25	
27	IO_L2N_27	J26	
27	IO_L3P_27	F28	
27	IO_L3N_27	E28	
27	IO_L4P_27	L24	
27	IO_L4N_VREF_27	L25	

Table 2-4: FF1155 Package—HX255T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
27	IO_L5P_27	D28	
27	IO_L5N_27	C29	
27	IO_L6P_27	G30	
27	IO_L6N_27	F30	
27	IO_L7P_27	B29	
27	IO_L7N_27	A29	
27	IO_L8P_SRCC_27	K25	
27	IO_L8N_SRCC_27	K26	
27	IO_L9P_MRCC_27	B30	
27	IO_L9N_MRCC_27	A30	
27	IO_L10P_MRCC_27	K27	
27	IO_L10N_MRCC_27	J28	
27	IO_L11P_SRCC_27	D29	
27	IO_L11N_SRCC_27	D30	
27	IO_L12P_VRN_27	J29	
27	IO_L12N_VRP_27	J30	
27	IO_L13P_27	F29	
27	IO_L13N_27	E30	
27	IO_L14P_27	C31	
27	IO_L14N_VREF_27	B31	
27	IO_L15P_27	H27	
27	IO_L15N_27	H28	
27	IO_L16P_27	B32	
27	IO_L16N_27	A32	
27	IO_L17P_27	H29	
27	IO_L17N_27	G29	
27	IO_L18P_27	A33	
27	IO_L18N_27	A34	
27	IO_L19P_27	M24	
27	IO_L19N_27	M25	
28	IO_L0P_28	B26	
28	IO_L0N_28	A27	
28	IO_L1P_28	C27	

Table 2-4: FF1155 Package—HX255T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
28	IO_L1N_28	C28	
28	IO_L2P_28	B27	
28	IO_L2N_28	A28	
28	IO_L3P_28	G20	
28	IO_L3N_28	G21	
28	IO_L4P_28	M21	
28	IO_L4N_VREF_28	M22	
28	IO_L5P_28	D24	
28	IO_L5N_28	D25	
28	IO_L6P_28	H21	
28	IO_L6N_28	G22	
28	IO_L7P_28	F22	
28	IO_L7N_28	F23	
28	IO_L8P_SRCC_28	H23	
28	IO_L8N_SRCC_28	G24	
28	IO_L9P_MRCC_28	D26	
28	IO_L9N_MRCC_28	C26	
28	IO_L10P_MRCC_28	J21	
28	IO_L10N_MRCC_28	H22	
28	IO_L11P_SRCC_28	F27	
28	IO_L11N_SRCC_28	E27	
28	IO_L12P_VRN_28	K23	
28	IO_L12N_VRP_28	J23	
28	IO_L13P_28	F24	
28	IO_L13N_28	E25	
28	IO_L14P_28	L22	
28	IO_L14N_VREF_28	L23	
28	IO_L15P_28	F25	
28	IO_L15N_28	E26	
28	IO_L16P_28	K21	
28	IO_L16N_28	K22	
28	IO_L17P_28	G25	
28	IO_L17N_28	G26	

Table 2-4: FF1155 Package—HX255T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
28	IO_L18P_28	K20	
28	IO_L18N_28	J20	
28	IO_L19P_28	M20	
28	IO_L19N_28	L20	
34	IO_L0P_GC_34	AJ13	
34	IO_L0N_GC_34	AK13	
34	IO_L1P_GC_34	AF14	
34	IO_L1N_GC_34	AG14	
34	IO_L2P_A15_D31_34	AH14	
34	IO_L2N_A14_D30_34	AJ14	
34	IO_L3P_A13_D29_34	AL14	
34	IO_L3N_A12_D28_34	AM14	
34	IO_L4P_A11_D27_34	AC14	
34	IO_L4N_VREF_A10_D26_34	AD14	
34	IO_L5P_A09_D25_34	AE15	
34	IO_L5N_A08_D24_34	AF15	
34	IO_L6P_A07_D23_34	AN14	
34	IO_L6N_A06_D22_34	AP14	
34	IO_L7P_A05_D21_34	AL15	
34	IO_L7N_A04_D20_34	AM15	
34	IO_L8P_SRCC_34	AP16	
34	IO_L8N_SRCC_34	AP15	
34	IO_L9P_MRCC_34	AG16	
34	IO_L9N_MRCC_34	AG15	
34	IO_L10P_MRCC_34	AJ15	
34	IO_L10N_MRCC_34	AK15	
34	IO_L11P_SRCC_34	AJ16	
34	IO_L11N_SRCC_34	AK16	
34	IO_L12P_A03_D19_34	AH17	
34	IO_L12N_A02_D18_34	AH16	
34	IO_L13P_A01_D17_34	AM16	
34	IO_L13N_A00_D16_34	AN16	
34	IO_L14P_A25_34	AF17	

Table 2-4: FF1155 Package—HX255T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
34	IO_L14N_VREF_A24_34	AG17	
34	IO_L15P_A23_34	AM17	
34	IO_L15N_A22_34	AN17	
34	IO_L16P_A21_34	AE17	
34	IO_L16N_A20_34	AE16	
34	IO_L17P_A19_34	AK17	
34	IO_L17N_A18_34	AL17	
34	IO_L18P_A17_34	AD16	
34	IO_L18N_A16_34	AD15	
34	IO_L19P_VRN_34	AC17	
34	IO_L19N_VRP_34	AC16	
35	IO_L0P_35	AD10	
35	IO_L0N_35	AE10	
35	IO_L1P_35	AG12	
35	IO_L1N_35	AG11	
35	IO_L2P_SM0P_35	AF10	
35	IO_L2N_SM0N_35	AG10	
35	IO_L3P_SM1P_35	AE12	
35	IO_L3N_SM1N_35	AE11	
35	IO_L4P_35	AB11	
35	IO_L4N_VREF_35	AB10	
35	IO_L5P_SM2P_35	AH11	
35	IO_L5N_SM2N_35	AJ11	
35	IO_L6P_SM3P_35	AJ10	
35	IO_L6N_SM3N_35	AK10	
35	IO_L7P_SM4P_35	AK12	
35	IO_L7N_SM4N_35	AK11	
35	IO_L8P_SRCC_35	AL10	
35	IO_L8N_SRCC_35	AM10	
35	IO_L9P_MRCC_35	AM12	
35	IO_L9N_MRCC_35	AM11	
35	IO_L10P_MRCC_35	AN9	
35	IO_L10N_MRCC_35	AP9	

Table 2-4: FF1155 Package—HX255T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
35	IO_L11P_SRCC_35	AH13	
35	IO_L11N_SRCC_35	AH12	
35	IO_L12P_SM5P_35	AN11	
35	IO_L12N_SM5N_35	AP10	
35	IO_L13P_SM6P_35	AF13	
35	IO_L13N_SM6N_35	AF12	
35	IO_L14P_35	AN12	
35	IO_L14N_VREF_35	AP11	
35	IO_L15P_SM7P_35	AL13	
35	IO_L15N_SM7N_35	AL12	
35	IO_L16P_VRN_35	AD13	
35	IO_L16N_VRP_35	AE13	
35	IO_L17P_35	AN13	
35	IO_L17N_35	AP13	
35	IO_L18P_GC_35	AC13	
35	IO_L18N_GC_35	AC12	
35	IO_L19P_GC_35	AC11	
35	IO_L19N_GC_35	AD11	
36	IO_L0P_36	M12	
36	IO_L0N_36	L12	
36	IO_L1P_36	J13	
36	IO_L1N_36	H13	
36	IO_L2P_36	H12	
36	IO_L2N_36	G11	
36	IO_L3P_36	F13	
36	IO_L3N_36	E13	
36	IO_L4P_36	L13	
36	IO_L4N_VREF_36	K13	
36	IO_L5P_36	D13	
36	IO_L5N_36	C13	
36	IO_L6P_36	C12	
36	IO_L6N_36	B11	
36	IO_L7P_36	A14	

Table 2-4: FF1155 Package—HX255T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
36	IO_L7N_36	A13	
36	IO_L8P_SRCC_36	D11	
36	IO_L8N_SRCC_36	C11	
36	IO_L9P_MRCC_36	B12	
36	IO_L9N_MRCC_36	A12	
36	IO_L10P_MRCC_36	B10	
36	IO_L10N_MRCC_36	A10	
36	IO_L11P_SRCC_36	E12	
36	IO_L11N_SRCC_36	E11	
36	IO_L12P_VRN_36	E10	
36	IO_L12N_VRP_36	D10	
36	IO_L13P_36	G12	
36	IO_L13N_36	F12	
36	IO_L14P_36	G10	
36	IO_L14N_VREF_36	F10	
36	IO_L15P_36	J11	
36	IO_L15N_36	H11	
36	IO_L16P_36	K10	
36	IO_L16N_36	J10	
36	IO_L17P_36	K12	
36	IO_L17N_36	K11	
36	IO_L18P_36	M10	
36	IO_L18N_36	L10	
36	IO_L19P_36	N11	
36	IO_L19N_36	M11	
37	IO_L0P_37	D15	
37	IO_L0N_37	D14	
37	IO_L1P_37	H16	
37	IO_L1N_37	G16	
37	IO_L2P_37	F15	
37	IO_L2N_37	E15	
37	IO_L3P_37	B21	
37	IO_L3N_37	A20	

Table 2-4: FF1155 Package—HX255T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
37	IO_L4P_37	K16	
37	IO_L4N_VREF_37	J16	
37	IO_L5P_37	B20	
37	IO_L5N_37	A19	
37	IO_L6P_37	G15	
37	IO_L6N_37	F14	
37	IO_L7P_37	B22	
37	IO_L7N_37	A22	
37	IO_L8P_SRCC_37	H14	
37	IO_L8N_SRCC_37	G14	
37	IO_L9P_MRCC_37	E16	
37	IO_L9N_MRCC_37	D16	
37	IO_L10P_MRCC_37	J15	
37	IO_L10N_MRCC_37	J14	
37	IO_L11P_SRCC_37	B19	
37	IO_L11N_SRCC_37	A18	
37	IO_L12P_VRN_37	B15	
37	IO_L12N_VRP_37	A15	
37	IO_L13P_37	C18	
37	IO_L13N_37	C17	
37	IO_L14P_37	C14	
37	IO_L14N_VREF_37	B14	
37	IO_L15P_37	C16	
37	IO_L15N_37	B16	
37	IO_L16P_37	L15	
37	IO_L16N_37	K15	
37	IO_L17P_37	B17	
37	IO_L17N_37	A17	
37	IO_L18P_37	M14	
37	IO_L18N_37	L14	
37	IO_L19P_37	M16	
37	IO_L19N_37	M15	
38	IO_L0P_38	E17	

Table 2-4: FF1155 Package—HX255T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
38	IO_L0N_38	E18	
38	IO_L1P_38	C24	
38	IO_L1N_38	B24	
38	IO_L2P_38	D18	
38	IO_L2N_38	C19	
38	IO_L3P_38	B25	
38	IO_L3N_38	A25	
38	IO_L4P_38	G17	
38	IO_L4N_VREF_38	F17	
38	IO_L5P_38	A23	
38	IO_L5N_38	A24	
38	IO_L6P_38	F18	
38	IO_L6N_38	F19	
38	IO_L7P_38	D19	
38	IO_L7N_38	D20	
38	IO_L8P_SRCC_38	H19	
38	IO_L8N_SRCC_38	G19	
38	IO_L9P_MRCC_38	C21	
38	IO_L9N_MRCC_38	C22	
38	IO_L10P_MRCC_38	H17	
38	IO_L10N_MRCC_38	H18	
38	IO_L11P_SRCC_38	D23	
38	IO_L11N_SRCC_38	C23	
38	IO_L12P_VRN_38	J18	
38	IO_L12N_VRP_38	J19	
38	IO_L13P_38	E20	
38	IO_L13N_38	D21	
38	IO_L14P_38	M19	
38	IO_L14N_VREF_38	L19	
38	IO_L15P_38	E22	
38	IO_L15N_38	E23	
38	IO_L16P_38	L17	
38	IO_L16N_38	K17	

Table 2-4: FF1155 Package—HX255T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
38	IO_L17P_38	F20	
38	IO_L17N_38	E21	
38	IO_L18P_38	N17	
38	IO_L18N_38	M17	
38	IO_L19P_38	L18	
38	IO_L19N_38	K18	
103	MGTTXN3_103	AL31	
103	MGTRXN3_103	AH29	
103	MGTTXP3_103	AL32	
103	MGTRXP3_103	AH30	
103	MGTTXN2_103	AM33	
103	MGTRXN2_103	AJ31	
103	MGTTXP2_103	AM34	
103	MGTREFCLK1P_103	AJ27	
103	MGTREFCLK1N_103	AJ28	
103	MGTRXP2_103	AJ32	
103	MGTREFCLK0P_103	AL27	
103	MGTREFCLK0N_103	AL28	
103	MGTTXN1_103	AN31	
103	MGTRXN1_103	AK29	
103	MGTTXP1_103	AN32	
103	MGTRXP1_103	AK30	
103	MGTTXN0_103	AP33	
103	MGTRXN0_103	AM29	
103	MGTTXP0_103	AP34	
103	MGTRXP0_103	AM30	
104	MGTTXN3_104	AD33	
104	MGTRXN3_104	AD29	
104	MGTTXP3_104	AD34	
104	MGTRXP3_104	AD30	
104	MGTTXN2_104	AF33	
104	MGTRXN2_104	AE31	
104	MGTTXP2_104	AF34	

Table 2-4: FF1155 Package—HX255T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
104	MGTREFCLK1P_104	AE27	
104	MGTREFCLK1N_104	AE28	
104	MGTRXP2_104	AE32	
104	MGTREFCLK0P_104	AG27	
104	MGTREFCLK0N_104	AG28	
104	MGTTXN1_104	AH33	
104	MGTRXN1_104	AF29	
104	MGTTXP1_104	AH34	
104	MGTRXP1_104	AF30	
104	MGTTXN0_104	AK33	
104	MGTRXN0_104	AG31	
104	MGTTXP0_104	AK34	
104	MGTRXP0_104	AG32	
105	MGTTXN3_105	V33	
105	MGTRXN3_105	AA31	
105	MGTTXP3_105	V34	
105	MGTRXP3_105	AA32	
105	MGTTXN2_105	Y33	
105	MGTRXN2_105	AB29	
105	MGTTXP2_105	Y34	
105	MGTREFCLK1P_105	AA27	
105	MGTREFCLK1N_105	AA28	
105	MGTRXP2_105	AB30	
105	MGTAVTTRCAL_105	AP29	
105	MGTRREF_105	AP30	
105	MGTREFCLK0P_105	AC27	
105	MGTREFCLK0N_105	AC28	
105	MGTTXN1_105	W31	
105	MGTRXN1_105	Y29	
105	MGTTXP1_105	W32	
105	MGTRXP1_105	Y30	
105	MGTTXN0_105	AB33	
105	MGTRXN0_105	AC31	

Table 2-4: FF1155 Package—HX255T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
105	MGTTXP0_105	AB34	
105	MGTRXP0_105	AC32	
113	MGTTXN3_113	AL4	
113	MGTRXN3_113	AH6	
113	MGTTXP3_113	AL3	
113	MGTRXP3_113	AH5	
113	MGTTXN2_113	AM2	
113	MGTRXN2_113	AJ4	
113	MGTTXP2_113	AM1	
113	MGTREFCLK1P_113	AJ8	
113	MGTREFCLK1N_113	AJ7	
113	MGTRXP2_113	AJ3	
113	MGTREFCLK0P_113	AL8	
113	MGTREFCLK0N_113	AL7	
113	MGTTXN1_113	AN4	
113	MGTRXN1_113	AK6	
113	MGTTXP1_113	AN3	
113	MGTRXP1_113	AK5	
113	MGTTXN0_113	AP2	
113	MGTRXN0_113	AM6	
113	MGTTXP0_113	AP1	
113	MGTRXP0_113	AM5	
114	MGTTXN3_114	AD2	
114	MGTRXN3_114	AD6	
114	MGTTXP3_114	AD1	
114	MGTRXP3_114	AD5	
114	MGTTXN2_114	AF2	
114	MGTRXN2_114	AE4	
114	MGTTXP2_114	AF1	
114	MGTREFCLK1P_114	AE8	
114	MGTREFCLK1N_114	AE7	
114	MGTRXP2_114	AE3	
114	MGTREFCLK0P_114	AG8	

Table 2-4: FF1155 Package—HX255T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
114	MGTREFCLK0N_114	AG7	
114	MGTTXN1_114	AH2	
114	MGTRXN1_114	AF6	
114	MGTTXP1_114	AH1	
114	MGTRXP1_114	AF5	
114	MGTTXN0_114	AK2	
114	MGTRXN0_114	AG4	
114	MGTTXP0_114	AK1	
114	MGTRXP0_114	AG3	
115	MGTTXN3_115	V2	
115	MGTRXN3_115	AA4	
115	MGTTXP3_115	V1	
115	MGTRXP3_115	AA3	
115	MGTTXN2_115	Y2	
115	MGTRXN2_115	AB6	
115	MGTTXP2_115	Y1	
115	MGTREFCLK1P_115	AA8	
115	MGTREFCLK1N_115	AA7	
115	MGTRXP2_115	AB5	
115	MGTAVTTRCAL_115	AP6	
115	MGTRREF_115	AP5	
115	MGTREFCLK0P_115	AC8	
115	MGTREFCLK0N_115	AC7	
115	MGTTXN1_115	W4	
115	MGTRXN1_115	Y6	
115	MGTTXP1_115	W3	
115	MGTRXP1_115	Y5	
115	MGTTXN0_115	AB2	
115	MGTRXN0_115	AC4	
115	MGTTXP0_115	AB1	
115	MGTRXP0_115	AC3	
116	MGTRXP2_116	N4	
116	MGTRXN2_116	N3	

Table 2-4: FF1155 Package—HX255T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
116	MGTTXP2_116	L4	
116	MGTTXN2_116	L3	
116	MGTRXP3_116	M6	
116	MGTRXN3_116	M5	
116	MGTTXP3_116	M2	
116	MGTTXN3_116	M1	
116	MGTRBIAS_116	L8	
116	MGTREFCLKP_116	P6	
116	MGTREFCLKN_116	P5	
116	MGTRXP1_116	R4	
116	MGTRXN1_116	R3	
116	MGTTXP1_116	P2	
116	MGTTXN1_116	P1	
116	MGTRXP0_116	U4	
116	MGTRXN0_116	U3	
116	MGTTXP0_116	T2	
116	MGTTXN0_116	T1	
117	MGTRXP2_117	D6	
117	MGTRXN2_117	D5	
117	MGTTXP2_117	F2	
117	MGTTXN2_117	F1	
117	MGTRXP3_117	F6	
117	MGTRXN3_117	F5	
117	MGTTXP3_117	G4	
117	MGTTXN3_117	G3	
117	MGTRBIAS_117	J8	
117	MGTREFCLKP_117	H2	
117	MGTREFCLKN_117	H1	
117	MGTRXP1_117	H6	
117	MGTRXN1_117	H5	
117	MGTTXP1_117	J4	
117	MGTTXN1_117	J3	
117	MGTRXP0_117	K6	

Table 2-4: FF1155 Package—HX255T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
117	MGTRXN0_117	K5	
117	MGTTXP0_117	K2	
117	MGTTXN0_117	K1	
118	MGTRXP2_118	A8	
118	MGTRXN2_118	A7	
118	MGTTXP2_118	A4	
118	MGTTXN2_118	A3	
118	MGTRXP3_118	B6	
118	MGTRXN3_118	B5	
118	MGTTXP3_118	B2	
118	MGTTXN3_118	B1	
118	MGTRBIAS_118	G8	
118	MGTREFCLKP_118	C4	
118	MGTREFCLKN_118	C3	
118	MGTRXP1_118	C8	
118	MGTRXN1_118	C7	
118	MGTTXP1_118	D2	
118	MGTTXN1_118	D1	
118	MGTRXP0_118	E8	
118	MGTRXN0_118	E7	
118	MGTTXP0_118	E4	
118	MGTTXN0_118	E3	
NA	GND	A9	
NA	GND	A16	
NA	GND	A26	
NA	GND	AA1	
NA	GND	AA2	
NA	GND	AA5	
NA	GND	AA9	
NA	GND	AA11	
NA	GND	AA13	
NA	GND	AA15	
NA	GND	AA17	

Table 2-4: FF1155 Package—HX255T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AA19	
NA	GND	AA21	
NA	GND	AA23	
NA	GND	AA26	
NA	GND	AA30	
NA	GND	AA33	
NA	GND	AA34	
NA	GND	AB3	
NA	GND	AB4	
NA	GND	AB8	
NA	GND	AB9	
NA	GND	AB12	
NA	GND	AB14	
NA	GND	AB16	
NA	GND	AB18	
NA	GND	AB20	
NA	GND	AB22	
NA	GND	AB25	
NA	GND	AB26	
NA	GND	AB27	
NA	GND	AB31	
NA	GND	AB32	
NA	GND	AC1	
NA	GND	AC5	
NA	GND	AC6	
NA	GND	AC9	
NA	GND	AC10	
NA	GND	AC20	
NA	GND	AC26	
NA	GND	AC29	
NA	GND	AC30	
NA	GND	AC34	
NA	GND	AD4	

Table 2-4: FF1155 Package—HX255T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AD8	
NA	GND	AD9	
NA	GND	AD17	
NA	GND	AD26	
NA	GND	AD27	
NA	GND	AD31	
NA	GND	AE1	
NA	GND	AE2	
NA	GND	AE5	
NA	GND	AE6	
NA	GND	AE9	
NA	GND	AE14	
NA	GND	AE24	
NA	GND	AE26	
NA	GND	AE29	
NA	GND	AE30	
NA	GND	AE33	
NA	GND	AE34	
NA	GND	AF3	
NA	GND	AF4	
NA	GND	AF8	
NA	GND	AF9	
NA	GND	AF11	
NA	GND	AF21	
NA	GND	AF26	
NA	GND	AF27	
NA	GND	AF31	
NA	GND	AF32	
NA	GND	AG1	
NA	GND	AG5	
NA	GND	AG6	
NA	GND	AG9	
NA	GND	AG18	

Table 2-4: FF1155 Package—HX255T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AG26	
NA	GND	AG29	
NA	GND	AG30	
NA	GND	AG34	
NA	GND	AH4	
NA	GND	AH8	
NA	GND	AH9	
NA	GND	AH15	
NA	GND	AH25	
NA	GND	AH26	
NA	GND	AH27	
NA	GND	AH31	
NA	GND	AJ1	
NA	GND	AJ2	
NA	GND	AJ5	
NA	GND	AJ6	
NA	GND	AJ9	
NA	GND	AJ12	
NA	GND	AJ22	
NA	GND	AJ26	
NA	GND	AJ29	
NA	GND	AJ30	
NA	GND	AJ33	
NA	GND	AJ34	
NA	GND	AK3	
NA	GND	AK4	
NA	GND	AK8	
NA	GND	AK9	
NA	GND	AK19	
NA	GND	AK26	
NA	GND	AK27	
NA	GND	AK31	
NA	GND	AK32	

Table 2-4: FF1155 Package—HX255T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AL1	
NA	GND	AL5	
NA	GND	AL9	
NA	GND	AL16	
NA	GND	AL26	
NA	GND	AL30	
NA	GND	AL34	
NA	GND	AM4	
NA	GND	AM8	
NA	GND	AM9	
NA	GND	AM13	
NA	GND	AM23	
NA	GND	AM26	
NA	GND	AM27	
NA	GND	AM31	
NA	GND	AN1	
NA	GND	AN2	
NA	GND	AN5	
NA	GND	AN6	
NA	GND	AN7	
NA	GND	AN8	
NA	GND	AN10	
NA	GND	AN20	
NA	GND	AN27	
NA	GND	AN28	
NA	GND	AN29	
NA	GND	AN30	
NA	GND	AN33	
NA	GND	AN34	
NA	GND	AP3	
NA	GND	AP4	
NA	GND	AP7	
NA	GND	AP8	

Table 2-4: FF1155 Package—HX255T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AP17	
NA	GND	AP27	
NA	GND	AP28	
NA	GND	AP31	
NA	GND	AP32	
NA	GND	B9	
NA	GND	B13	
NA	GND	B23	
NA	GND	B33	
NA	GND	C9	
NA	GND	C10	
NA	GND	C20	
NA	GND	C30	
NA	GND	D9	
NA	GND	D17	
NA	GND	D27	
NA	GND	E9	
NA	GND	E14	
NA	GND	E24	
NA	GND	E34	
NA	GND	F9	
NA	GND	F11	
NA	GND	F21	
NA	GND	F31	
NA	GND	G9	
NA	GND	G18	
NA	GND	G28	
NA	GND	H9	
NA	GND	H15	
NA	GND	H25	
NA	GND	J9	
NA	GND	J12	
NA	GND	J22	

Table 2-4: FF1155 Package—HX255T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	J32	
NA	GND	K9	
NA	GND	K19	
NA	GND	K29	
NA	GND	L9	
NA	GND	L16	
NA	GND	L26	
NA	GND	M9	
NA	GND	M13	
NA	GND	M23	
NA	GND	M33	
NA	GND	N9	
NA	GND	N10	
NA	GND	N13	
NA	GND	N15	
NA	GND	N19	
NA	GND	N21	
NA	GND	N23	
NA	GND	N30	
NA	GND	P8	
NA	GND	P9	
NA	GND	P12	
NA	GND	P14	
NA	GND	P16	
NA	GND	P18	
NA	GND	P20	
NA	GND	P22	
NA	GND	P24	
NA	GND	P27	
NA	GND	R7	
NA	GND	R8	
NA	GND	R11	
NA	GND	R13	

Table 2-4: FF1155 Package—HX255T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	R15	
NA	GND	R17	
NA	GND	R19	
NA	GND	R21	
NA	GND	R23	
NA	GND	R34	
NA	GND	T7	
NA	GND	T10	
NA	GND	T12	
NA	GND	T14	
NA	GND	T16	
NA	GND	T20	
NA	GND	T22	
NA	GND	T24	
NA	GND	T31	
NA	GND	U6	
NA	GND	U7	
NA	GND	U11	
NA	GND	U13	
NA	GND	U15	
NA	GND	U19	
NA	GND	U21	
NA	GND	U23	
NA	GND	U28	
NA	GND	U32	
NA	GND	U33	
NA	GND	U34	
NA	GND	V3	
NA	GND	V4	
NA	GND	V5	
NA	GND	V6	
NA	GND	V7	
NA	GND	V8	

Table 2-4: FF1155 Package—HX255T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	V10	
NA	GND	V12	
NA	GND	V14	
NA	GND	V16	
NA	GND	V20	
NA	GND	V22	
NA	GND	V24	
NA	GND	V25	
NA	GND	V30	
NA	GND	V31	
NA	GND	V32	
NA	GND	W1	
NA	GND	W5	
NA	GND	W6	
NA	GND	W7	
NA	GND	W11	
NA	GND	W13	
NA	GND	W15	
NA	GND	W19	
NA	GND	W21	
NA	GND	W23	
NA	GND	W28	
NA	GND	W29	
NA	GND	W30	
NA	GND	W34	
NA	GND	Y4	
NA	GND	Y7	
NA	GND	Y8	
NA	GND	Y9	
NA	GND	Y12	
NA	GND	Y14	
NA	GND	Y16	
NA	GND	Y18	

Table 2-4: FF1155 Package—HX255T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	Y20	
NA	GND	Y22	
NA	GND	Y24	
NA	GND	Y26	
NA	GND	Y27	
NA	GND	Y28	
NA	GND	Y31	
NA	VCCAUX	AA10	
NA	VCCAUX	AA24	
NA	VCCAUX	AB23	
NA	VCCAUX	N24	
NA	VCCAUX	P11	
NA	VCCAUX	R10	
NA	VCCAUX	R24	
NA	VCCAUX	T11	
NA	VCCAUX	U24	
NA	VCCAUX	V11	
NA	VCCAUX	W24	
NA	VCCAUX	Y11	
NA	VCCINT	AA12	
NA	VCCINT	AA14	
NA	VCCINT	AA16	
NA	VCCINT	AA18	
NA	VCCINT	AA20	
NA	VCCINT	AA22	
NA	VCCINT	AB13	
NA	VCCINT	AB15	
NA	VCCINT	AB17	
NA	VCCINT	AB19	
NA	VCCINT	AB21	
NA	VCCINT	N12	
NA	VCCINT	N14	
NA	VCCINT	N16	

Table 2-4: FF1155 Package—HX255T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	N18	
NA	VCCINT	N20	
NA	VCCINT	N22	
NA	VCCINT	P13	
NA	VCCINT	P15	
NA	VCCINT	P17	
NA	VCCINT	P19	
NA	VCCINT	P21	
NA	VCCINT	P23	
NA	VCCINT	R12	
NA	VCCINT	R14	
NA	VCCINT	R16	
NA	VCCINT	R18	
NA	VCCINT	R20	
NA	VCCINT	R22	
NA	VCCINT	T13	
NA	VCCINT	T15	
NA	VCCINT	T19	
NA	VCCINT	T21	
NA	VCCINT	T23	
NA	VCCINT	U12	
NA	VCCINT	U14	
NA	VCCINT	U16	
NA	VCCINT	U20	
NA	VCCINT	U22	
NA	VCCINT	V13	
NA	VCCINT	V15	
NA	VCCINT	V19	
NA	VCCINT	V21	
NA	VCCINT	V23	
NA	VCCINT	W12	
NA	VCCINT	W14	
NA	VCCINT	W16	

Table 2-4: FF1155 Package—HX255T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	W20	
NA	VCCINT	W22	
NA	VCCINT	Y13	
NA	VCCINT	Y15	
NA	VCCINT	Y17	
NA	VCCINT	Y19	
NA	VCCINT	Y21	
NA	VCCINT	Y23	
0	VCCO_0	P10	
0	VCCO_0	U9	
23	VCCO_23	AE19	
23	VCCO_23	AH20	
23	VCCO_23	AL21	
23	VCCO_23	AM18	
23	VCCO_23	AP22	
24	VCCO_24	AC25	
24	VCCO_24	AD22	
24	VCCO_24	AG23	
24	VCCO_24	AK24	
24	VCCO_24	AN25	
25	VCCO_25	N25	
25	VCCO_25	P32	
25	VCCO_25	R29	
25	VCCO_25	T26	
25	VCCO_25	W27	
26	VCCO_26	D32	
26	VCCO_26	G33	
26	VCCO_26	K34	
26	VCCO_26	L31	
26	VCCO_26	M28	
27	VCCO_27	A31	
27	VCCO_27	E29	
27	VCCO_27	H30	

Table 2-4: FF1155 Package—HX255T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
27	VCCO_27	J27	
27	VCCO_27	K24	
28	VCCO_28	B28	
28	VCCO_28	F26	
28	VCCO_28	G23	
28	VCCO_28	H20	
28	VCCO_28	L21	
34	VCCO_34	AC15	
34	VCCO_34	AF16	
34	VCCO_34	AJ17	
34	VCCO_34	AK14	
34	VCCO_34	AN15	
35	VCCO_35	AD12	
35	VCCO_35	AG13	
35	VCCO_35	AH10	
35	VCCO_35	AL11	
35	VCCO_35	AP12	
36	VCCO_36	A11	
36	VCCO_36	D12	
36	VCCO_36	G13	
36	VCCO_36	H10	
36	VCCO_36	L11	
37	VCCO_37	A21	
37	VCCO_37	B18	
37	VCCO_37	C15	
37	VCCO_37	F16	
37	VCCO_37	K14	
38	VCCO_38	C25	
38	VCCO_38	D22	
38	VCCO_38	E19	
38	VCCO_38	J17	
38	VCCO_38	M18	
NA	MGTHAGND	A1	

Table 2-4: FF1155 Package—HX255T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTHAGND	A2	
NA	MGTHAGND	A5	
NA	MGTHAGND	B3	
NA	MGTHAGND	B7	
NA	MGTHAGND	C1	
NA	MGTHAGND	C5	
NA	MGTHAGND	D3	
NA	MGTHAGND	D7	
NA	MGTHAGND	E1	
NA	MGTHAGND	E2	
NA	MGTHAGND	E5	
NA	MGTHAGND	F3	
NA	MGTHAGND	F7	
NA	MGTHAGND	G1	
NA	MGTHAGND	G5	
NA	MGTHAGND	G7	
NA	MGTHAGND	H3	
NA	MGTHAGND	H7	
NA	MGTHAGND	J1	
NA	MGTHAGND	J2	
NA	MGTHAGND	J5	
NA	MGTHAGND	J7	
NA	MGTHAGND	K3	
NA	MGTHAGND	K7	
NA	MGTHAGND	L1	
NA	MGTHAGND	L5	
NA	MGTHAGND	M3	
NA	MGTHAGND	M7	
NA	MGTHAGND	M8	
NA	MGTHAGND	N1	
NA	MGTHAGND	N2	
NA	MGTHAGND	N5	
NA	MGTHAGND	P3	

Table 2-4: FF1155 Package—HX255T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTHAGND	P7	
NA	MGTHAGND	R1	
NA	MGTHAGND	R5	
NA	MGTHAGND	T3	
NA	MGTHAGND	T5	
NA	MGTHAGND	T6	
NA	MGTHAGND	U1	
NA	MGTHAGND	U2	
NA	MGTHAGND	U5	
NA	MGTAVCC_R	AA6	
NA	MGTAVCC_R	AB7	
NA	MGTAVCC_R	AD7	
NA	MGTAVCC_R	AF7	
NA	MGTAVCC_R	AH7	
NA	MGTAVCC_R	AK7	
NA	MGTAVCC_R	AL6	
NA	MGTAVCC_R	AM7	
NA	MGTAVCC_L	AA29	
NA	MGTAVCC_L	AB28	
NA	MGTAVCC_L	AD28	
NA	MGTAVCC_L	AF28	
NA	MGTAVCC_L	AH28	
NA	MGTAVCC_L	AK28	
NA	MGTAVCC_L	AL29	
NA	MGTAVCC_L	AM28	
NA	MGTAVTT_R	AC2	
NA	MGTAVTT_R	AD3	
NA	MGTAVTT_R	AG2	
NA	MGTAVTT_R	AH3	
NA	MGTAVTT_R	AL2	
NA	MGTAVTT_R	AM3	
NA	MGTAVTT_R	W2	
NA	MGTAVTT_R	Y3	

Table 2-4: FF1155 Package—HX255T and HX380T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTAVTT_L	AC33	
NA	MGTAVTT_L	AD32	
NA	MGTAVTT_L	AG33	
NA	MGTAVTT_L	AH32	
NA	MGTAVTT_L	AL33	
NA	MGTAVTT_L	AM32	
NA	MGTAVTT_L	W33	
NA	MGTAVTT_L	Y32	
NA	MGTHAVCC	B4	
NA	MGTHAVCC	D4	
NA	MGTHAVCC	F4	
NA	MGTHAVCC	G6	
NA	MGTHAVCC	H4	
NA	MGTHAVCC	K4	
NA	MGTHAVCC	M4	
NA	MGTHAVCC	P4	
NA	MGTHAVCC	R6	
NA	MGTHAVCC	T4	
NA	MGTHAVCCPLL	F8	
NA	MGTHAVCCPLL	H8	
NA	MGTHAVCCPLL	K8	
NA	MGTHAVCCRX	A6	
NA	MGTHAVCCRX	B8	
NA	MGTHAVCCRX	C6	
NA	MGTHAVCCRX	D8	
NA	MGTHAVCCRX	E6	
NA	MGTHAVCCRX	J6	
NA	MGTHAVCCRX	L6	
NA	MGTHAVCCRX	N6	
NA	MGTHAVTT	C2	
NA	MGTHAVTT	G2	
NA	MGTHAVTT	L2	
NA	MGTHAVTT	R2	

Table 2-4: FF1155 Package—HX255T and HX380T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	RSVD	L7	
NA	RSVD	N8	
NA	RSVD	N7	

FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
0	INIT_B_0	P8	
0	DONE_0	R8	
0	M1_0	W8	
0	M2_0	V8	
0	HSWAPEN_0	M8	
0	PROGRAM_B_0	L8	
0	M0_0	U8	
0	AVSS_0	T17	
0	AVDD_0	T18	
0	VP_0	U18	
0	VREFP_0	V18	
0	VN_0	V17	
0	VREFN_0	U17	
0	DXP_0	W18	
0	DXN_0	W17	
0	VBATT_0	N8	
0	DIN_0	H8	
0	RDWR_B_0	G8	
0	CSI_B_0	F8	
0	DOUT_BUSY_0	AA8	
0	CCLK_0	K8	
0	TDO_0	AC8	
0	TCK_0	AE8	
0	TMS_0	AF8	
0	TDI_0	AD8	
0	VFS_0	Y8	
12	IO_L0P_12	AD25	
12	IO_L0N_12	AD26	
12	IO_L1P_12	AE27	
12	IO_L1N_12	AD27	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
12	IO_L2P_12	AH33	
12	IO_L2N_12	AH32	
12	IO_L3P_12	AE28	
12	IO_L3N_12	AE29	
12	IO_L4P_12	AJ34	
12	IO_L4N_VREF_12	AH34	
12	IO_L5P_12	AF28	
12	IO_L5N_12	AF29	
12	IO_L6P_12	AL34	
12	IO_L6N_12	AK34	
12	IO_L7P_12	AH29	
12	IO_L7N_12	AH30	
12	IO_L8P_SRCC_12	AN33	
12	IO_L8N_SRCC_12	AN34	
12	IO_L9P_MRCC_12	AG27	
12	IO_L9N_MRCC_12	AG28	
12	IO_L10P_MRCC_12	AF30	
12	IO_L10N_MRCC_12	AG30	
12	IO_L11P_SRCC_12	AF26	
12	IO_L11N_SRCC_12	AE26	
12	IO_L12P_VRN_12	AJ31	
12	IO_L12N_VRP_12	AJ32	
12	IO_L13P_12	AJ29	
12	IO_L13N_12	AJ30	
12	IO_L14P_12	AK33	
12	IO_L14N_VREF_12	AK32	
12	IO_L15P_12	AL31	
12	IO_L15N_12	AK31	
12	IO_L16P_12	AM33	
12	IO_L16N_12	AL33	
12	IO_L17P_12	AN32	
12	IO_L17N_12	AM32	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
12	IO_L18P_12	AP32	
12	IO_L18N_12	AP33	
12	IO_L19P_12	AL30	
12	IO_L19N_12	AM31	
13	IO_L0P_13	AA34	
13	IO_L0N_13	AA33	
13	IO_L1P_13	AA30	
13	IO_L1N_13	AA31	
13	IO_L2P_13	AD34	
13	IO_L2N_13	AC34	
13	IO_L3P_13	AB30	
13	IO_L3N_13	AB31	
13	IO_L4P_13	AC33	
13	IO_L4N_VREF_13	AB33	
13	IO_L5P_13	AE31	
13	IO_L5N_13	AD31	
13	IO_L6P_13	AA25	
13	IO_L6N_13	Y26	
13	IO_L7P_13	AA28	
13	IO_L7N_13	AA29	
13	IO_L8P_SRCC_13	AE34	
13	IO_L8N_SRCC_13	AF34	
13	IO_L9P_MRCC_13	AD30	
13	IO_L9N_MRCC_13	AC30	
13	IO_L10P_MRCC_13	AE33	
13	IO_L10N_MRCC_13	AF33	
13	IO_L11P_SRCC_13	AD29	
13	IO_L11N_SRCC_13	AC29	
13	IO_L12P_VRN_13	AB32	
13	IO_L12N_VRP_13	AC32	
13	IO_L13P_13	AB28	
13	IO_L13N_13	AC28	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
13	IO_L14P_13	AD32	
13	IO_L14N_VREF_13	AE32	
13	IO_L15P_13	AB27	
13	IO_L15N_13	AC27	
13	IO_L16P_13	AG33	
13	IO_L16N_13	AG32	
13	IO_L17P_13	AA26	
13	IO_L17N_13	AB26	
13	IO_L18P_13	AG31	
13	IO_L18N_13	AF31	
13	IO_L19P_13	AB25	
13	IO_L19N_13	AC25	
14	IO_L0P_14	U25	
14	IO_L0N_14	T25	
14	IO_L1P_14	T28	
14	IO_L1N_14	T29	
14	IO_L2P_14	R33	
14	IO_L2N_14	R34	
14	IO_L3P_14	T30	
14	IO_L3N_14	T31	
14	IO_L4P_14	T33	
14	IO_L4N_VREF_14	T34	
14	IO_L5P_14	U26	
14	IO_L5N_14	U27	
14	IO_L6P_14	U33	
14	IO_L6N_14	U32	
14	IO_L7P_14	U28	
14	IO_L7N_14	V29	
14	IO_L8P_SRCC_14	U31	
14	IO_L8N_SRCC_14	U30	
14	IO_L9P_MRCC_14	V30	
14	IO_L9N_MRCC_14	W30	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
14	IO_L10P_MRCC_14	V34	
14	IO_L10N_MRCC_14	W34	
14	IO_L11P_SRCC_14	V28	
14	IO_L11N_SRCC_14	V27	
14	IO_L12P_VRN_14	V32	
14	IO_L12N_VRP_14	V33	
14	IO_L13P_14	Y32	
14	IO_L13N_14	Y31	
14	IO_L14P_14	Y33	
14	IO_L14N_VREF_14	Y34	
14	IO_L15P_14	W29	
14	IO_L15N_14	Y29	
14	IO_L16P_14	W31	
14	IO_L16N_14	W32	
14	IO_L17P_14	Y28	
14	IO_L17N_14	Y27	
14	IO_L18P_14	W25	
14	IO_L18N_14	V25	
14	IO_L19P_14	W27	
14	IO_L19N_14	W26	
15	IO_L0P_15	M31	
15	IO_L0N_15	L31	
15	IO_L1P_15	N25	
15	IO_L1N_15	M25	
15	IO_L2P_SM8P_15	K32	
15	IO_L2N_SM8N_15	K31	
15	IO_L3P_SM9P_15	M26	
15	IO_L3N_SM9N_15	M27	
15	IO_L4P_15	P31	
15	IO_L4N_VREF_15	P30	
15	IO_L5P_SM10P_15	N27	
15	IO_L5N_SM10N_15	P27	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
15	IO_L6P_SM11P_15	L33	
15	IO_L6N_SM11N_15	M32	
15	IO_L7P_SM12P_15	L28	
15	IO_L7N_SM12N_15	M28	
15	IO_L8P_SRCC_15	N32	
15	IO_L8N_SRCC_15	P32	
15	IO_L9P_MRCC_15	N28	
15	IO_L9N_MRCC_15	N29	
15	IO_L10P_MRCC_15	N33	
15	IO_L10N_MRCC_15	M33	
15	IO_L11P_SRCC_15	L29	
15	IO_L11N_SRCC_15	L30	
15	IO_L12P_SM13P_15	P25	
15	IO_L12N_SM13N_15	P26	
15	IO_L13P_SM14P_15	R28	
15	IO_L13N_SM14N_15	R27	
15	IO_L14P_15	R31	
15	IO_L14N_VREF_15	R32	
15	IO_L15P_SM15P_15	R26	
15	IO_L15N_SM15N_15	T26	
15	IO_L16P_VRN_15	K34	
15	IO_L16N_VRP_15	L34	
15	IO_L17P_15	M30	
15	IO_L17N_15	N30	
15	IO_L18P_15	N34	
15	IO_L18N_15	P34	
15	IO_L19P_15	P29	
15	IO_L19N_15	R29	
16	IO_L0P_16	C32	
16	IO_L0N_16	B32	
16	IO_L1P_16	J26	
16	IO_L1N_16	J27	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
16	IO_L2P_16	E32	
16	IO_L2N_16	E33	
16	IO_L3P_16	F30	
16	IO_L3N_16	G30	
16	IO_L4P_16	A33	
16	IO_L4N_VREF_16	B33	
16	IO_L5P_16	G31	
16	IO_L5N_16	H30	
16	IO_L6P_16	C33	
16	IO_L6N_16	B34	
16	IO_L7P_16	K28	
16	IO_L7N_16	J29	
16	IO_L8P_SRCC_16	D34	
16	IO_L8N_SRCC_16	C34	
16	IO_L9P_MRCC_16	K26	
16	IO_L9N_MRCC_16	K27	
16	IO_L10P_MRCC_16	F33	
16	IO_L10N_MRCC_16	G33	
16	IO_L11P_SRCC_16	F31	
16	IO_L11N_SRCC_16	E31	
16	IO_L12P_VRN_16	E34	
16	IO_L12N_VRP_16	F34	
16	IO_L13P_16	J30	
16	IO_L13N_16	K29	
16	IO_L14P_16	H34	
16	IO_L14N_VREF_16	H33	
16	IO_L15P_16	D31	
16	IO_L15N_16	D32	
16	IO_L16P_16	K33	
16	IO_L16N_16	J34	
16	IO_L17P_16	G32	
16	IO_L17N_16	H32	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
16	IO_L18P_16	L25	
16	IO_L18N_16	L26	
16	IO_L19P_16	J31	
16	IO_L19N_16	J32	
22	IO_L0P_22	AE21	
22	IO_L0N_22	AD21	
22	IO_L1P_22	AM18	
22	IO_L1N_22	AL18	
22	IO_L2P_22	AG22	
22	IO_L2N_22	AH22	
22	IO_L3P_22	AP19	
22	IO_L3N_22	AN18	
22	IO_L4P_22	AK22	
22	IO_L4N_VREF_22	AJ22	
22	IO_L5P_22	AN19	
22	IO_L5N_22	AN20	
22	IO_L6P_22	AC20	
22	IO_L6N_22	AD20	
22	IO_L7P_22	AM20	
22	IO_L7N_22	AL20	
22	IO_L8P_SRCC_22	AF19	
22	IO_L8N_SRCC_22	AE19	
22	IO_L9P_MRCC_22	AP20	
22	IO_L9N_MRCC_22	AP21	
22	IO_L10P_MRCC_22	AK19	
22	IO_L10N_MRCC_22	AL19	
22	IO_L11P_SRCC_22	AF20	
22	IO_L11N_SRCC_22	AF21	
22	IO_L12P_VRN_22	AJ20	
22	IO_L12N_VRP_22	AH20	
22	IO_L13P_22	AM21	
22	IO_L13N_22	AL21	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
22	IO_L14P_22	AC19	
22	IO_L14N_VREF_22	AD19	
22	IO_L15P_22	AM23	
22	IO_L15N_22	AL23	
22	IO_L16P_22	AK21	
22	IO_L16N_22	AJ21	
22	IO_L17P_22	AM22	
22	IO_L17N_22	AN22	
22	IO_L18P_22	AG20	
22	IO_L18N_22	AG21	
22	IO_L19P_22	AP22	
22	IO_L19N_22	AN23	
23	IO_L0P_23	AH27	
23	IO_L0N_23	AH28	
23	IO_L1P_23	AN30	
23	IO_L1N_23	AM30	
23	IO_L2P_23	AG25	
23	IO_L2N_23	AG26	
23	IO_L3P_23	AP30	
23	IO_L3N_23	AP31	
23	IO_L4P_23	AL29	
23	IO_L4N_VREF_23	AK29	
23	IO_L5P_23	AN29	
23	IO_L5N_23	AP29	
23	IO_L6P_23	AL28	
23	IO_L6N_23	AK28	
23	IO_L7P_23	AN28	
23	IO_L7N_23	AM28	
23	IO_L8P_SRCC_23	AH25	
23	IO_L8N_SRCC_23	AJ25	
23	IO_L9P_MRCC_23	AN27	
23	IO_L9N_MRCC_23	AM27	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
23	IO_L10P_MRCC_23	AK27	
23	IO_L10N_MRCC_23	AJ27	
23	IO_L11P_SRCC_23	AH23	
23	IO_L11N_SRCC_23	AH24	
23	IO_L12P_VRN_23	AK26	
23	IO_L12N_VRP_23	AJ26	
23	IO_L13P_23	AL26	
23	IO_L13N_23	AM26	
23	IO_L14P_23	AJ24	
23	IO_L14N_VREF_23	AK24	
23	IO_L15P_23	AP27	
23	IO_L15N_23	AP26	
23	IO_L16P_23	AM25	
23	IO_L16N_23	AL25	
23	IO_L17P_23	AN25	
23	IO_L17N_23	AN24	
23	IO_L18P_23	AK23	
23	IO_L18N_23	AL24	
23	IO_L19P_23	AP25	
23	IO_L19N_23	AP24	
24	IO_L0P_GC_24	L23	
24	IO_L0N_GC_24	M22	
24	IO_L1P_GC_24	K24	
24	IO_L1N_GC_24	K23	
24	IO_L2P_D15_24	M23	
24	IO_L2N_D14_24	L24	
24	IO_L3P_D13_24	F24	
24	IO_L3N_D12_24	F23	
24	IO_L4P_D11_24	N23	
24	IO_L4N_VREF_D10_24	N24	
24	IO_L5P_D9_24	H23	
24	IO_L5N_D8_24	G23	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
24	IO_L6P_D7_24	R24	
24	IO_L6N_D6_24	P24	
24	IO_L7P_D5_24	H25	
24	IO_L7N_D4_24	H24	
24	IO_L8P_SRCC_24	T24	
24	IO_L8N_SRCC_24	T23	
24	IO_L9P_MRCC_24	J25	
24	IO_L9N_MRCC_24	J24	
24	IO_L10P_MRCC_24	U23	
24	IO_L10N_MRCC_24	V23	
24	IO_L11P_SRCC_24	AD24	
24	IO_L11N_SRCC_24	AE24	
24	IO_L12P_D3_24	V24	
24	IO_L12N_D2_FS2_24	W24	
24	IO_L13P_D1_FS1_24	AF25	
24	IO_L13N_D0_FS0_24	AF24	
24	IO_L14P_FCS_B_24	Y24	
24	IO_L14N_VREF_FOE_B_MOSTI_24	AA24	
24	IO_L15P_FWE_B_24	AF23	
24	IO_L15N_RS1_24	AG23	
24	IO_L16P_RS0_24	AA23	
24	IO_L16N_CS0_B_24	AB23	
24	IO_L17P_VRN_24	AE23	
24	IO_L17N_VRP_24	AE22	
24	IO_L18P_24	AC23	
24	IO_L18N_24	AC24	
24	IO_L19P_24	AC22	
24	IO_L19N_24	AD22	
25	IO_L0P_25	D25	
25	IO_L0N_25	D26	
25	IO_L1P_25	C24	
25	IO_L1N_25	C25	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
25	IO_L2P_25	E26	
25	IO_L2N_25	F26	
25	IO_L3P_25	B25	
25	IO_L3N_25	A25	
25	IO_L4P_25	D27	
25	IO_L4N_VREF_25	E27	
25	IO_L5P_25	B26	
25	IO_L5N_25	A26	
25	IO_L6P_25	G26	
25	IO_L6N_25	G27	
25	IO_L7P_25	B27	
25	IO_L7N_25	C27	
25	IO_L8P_SRCC_25	D24	
25	IO_L8N_SRCC_25	E24	
25	IO_L9P_MRCC_25	C28	
25	IO_L9N_MRCC_25	B28	
25	IO_L10P_MRCC_25	C29	
25	IO_L10N_MRCC_25	D29	
25	IO_L11P_SRCC_25	F25	
25	IO_L11N_SRCC_25	G25	
25	IO_L12P_25	H27	
25	IO_L12N_25	G28	
25	IO_L13P_25	A28	
25	IO_L13N_25	A29	
25	IO_L14P_25	F28	
25	IO_L14N_VREF_25	E28	
25	IO_L15P_25	A30	
25	IO_L15N_25	B30	
25	IO_L16P_VRN_25	E29	
25	IO_L16N_VRP_25	F29	
25	IO_L17P_25	C30	
25	IO_L17N_25	D30	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
25	IO_L18P_GC_25	H28	
25	IO_L18N_GC_25	H29	
25	IO_L19P_GC_25	B31	
25	IO_L19N_GC_25	A31	
26	IO_L0P_26	C20	
26	IO_L0N_26	D20	
26	IO_L1P_26	A23	
26	IO_L1N_26	A24	
26	IO_L2P_26	G21	
26	IO_L2N_26	G22	
26	IO_L3P_26	B23	
26	IO_L3N_26	C23	
26	IO_L4P_26	J20	
26	IO_L4N_VREF_26	J21	
26	IO_L5P_26	B21	
26	IO_L5N_26	B22	
26	IO_L6P_26	E22	
26	IO_L6N_26	E23	
26	IO_L7P_26	A20	
26	IO_L7N_26	A21	
26	IO_L8P_SRCC_26	F19	
26	IO_L8N_SRCC_26	F20	
26	IO_L9P_MRCC_26	B20	
26	IO_L9N_MRCC_26	C19	
26	IO_L10P_MRCC_26	F21	
26	IO_L10N_MRCC_26	G20	
26	IO_L11P_SRCC_26	H19	
26	IO_L11N_SRCC_26	H20	
26	IO_L12P_VRN_26	D21	
26	IO_L12N_VRP_26	E21	
26	IO_L13P_26	E19	
26	IO_L13N_26	D19	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
26	IO_L14P_26	H22	
26	IO_L14N_VREF_26	J22	
26	IO_L15P_26	A18	
26	IO_L15N_26	A19	
26	IO_L16P_26	K21	
26	IO_L16N_26	K22	
26	IO_L17P_26	B18	
26	IO_L17N_26	C18	
26	IO_L18P_26	L20	
26	IO_L18N_26	L21	
26	IO_L19P_26	C22	
26	IO_L19N_26	D22	
32	IO_L0P_32	AG15	
32	IO_L0N_32	AF15	
32	IO_L1P_32	AK14	
32	IO_L1N_32	AJ14	
32	IO_L2P_32	AJ15	
32	IO_L2N_32	AH15	
32	IO_L3P_32	AL15	
32	IO_L3N_32	AL14	
32	IO_L4P_32	AG16	
32	IO_L4N_VREF_32	AF16	
32	IO_L5P_32	AN15	
32	IO_L5N_32	AM15	
32	IO_L6P_32	AJ17	
32	IO_L6N_32	AJ16	
32	IO_L7P_32	AP16	
32	IO_L7N_32	AP15	
32	IO_L8P_SRCC_32	AH17	
32	IO_L8N_SRCC_32	AG17	
32	IO_L9P_MRCC_32	AC15	
32	IO_L9N_MRCC_32	AD15	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
32	IO_L10P_MRCC_32	AE16	
32	IO_L10N_MRCC_32	AD16	
32	IO_L11P_SRCC_32	AC18	
32	IO_L11N_SRCC_32	AC17	
32	IO_L12P_VRN_32	AH18	
32	IO_L12N_VRP_32	AG18	
32	IO_L13P_32	AN17	
32	IO_L13N_32	AP17	
32	IO_L14P_32	AJ19	
32	IO_L14N_VREF_32	AH19	
32	IO_L15P_32	AM17	
32	IO_L15N_32	AM16	
32	IO_L16P_32	AD17	
32	IO_L16N_32	AE17	
32	IO_L17P_32	AK18	
32	IO_L17N_32	AK17	
32	IO_L18P_32	AE18	
32	IO_L18N_32	AF18	
32	IO_L19P_32	AL16	
32	IO_L19N_32	AK16	
33	IO_L0P_33	AE13	
33	IO_L0N_33	AE12	
33	IO_L1P_33	AJ11	
33	IO_L1N_33	AK11	
33	IO_L2P_33	AD14	
33	IO_L2N_33	AC14	
33	IO_L3P_33	AK12	
33	IO_L3N_33	AJ12	
33	IO_L4P_33	AF11	
33	IO_L4N_VREF_33	AE11	
33	IO_L5P_33	AM10	
33	IO_L5N_33	AL10	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
33	IO_L6P_33	AG11	
33	IO_L6N_33	AG10	
33	IO_L7P_33	AL11	
33	IO_L7N_33	AM11	
33	IO_L8P_SRCC_33	AJ10	
33	IO_L8N_SRCC_33	AH10	
33	IO_L9P_MRCC_33	AC13	
33	IO_L9N_MRCC_33	AC12	
33	IO_L10P_MRCC_33	AD12	
33	IO_L10N_MRCC_33	AD11	
33	IO_L11P_SRCC_33	AP11	
33	IO_L11N_SRCC_33	AP12	
33	IO_L12P_VRN_33	AF13	
33	IO_L12N_VRP_33	AG13	
33	IO_L13P_33	AM12	
33	IO_L13N_33	AN12	
33	IO_L14P_33	AE14	
33	IO_L14N_VREF_33	AF14	
33	IO_L15P_33	AN13	
33	IO_L15N_33	AM13	
33	IO_L16P_33	AG12	
33	IO_L16N_33	AH12	
33	IO_L17P_33	AK13	
33	IO_L17N_33	AL13	
33	IO_L18P_33	AH13	
33	IO_L18N_33	AH14	
33	IO_L19P_33	AP14	
33	IO_L19N_33	AN14	
34	IO_L0P_GC_34	J9	
34	IO_L0N_GC_34	H9	
34	IO_L1P_GC_34	A10	
34	IO_L1N_GC_34	B10	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
34	IO_L2P_A15_D31_34	F9	
34	IO_L2N_A14_D30_34	F10	
34	IO_L3P_A13_D29_34	C10	
34	IO_L3N_A12_D28_34	D10	
34	IO_L4P_A11_D27_34	C9	
34	IO_L4N_VREF_A10_D26_34	D9	
34	IO_L5P_A09_D25_34	A9	
34	IO_L5N_A08_D24_34	A8	
34	IO_L6P_A07_D23_34	E8	
34	IO_L6N_A06_D22_34	E9	
34	IO_L7P_A05_D21_34	B8	
34	IO_L7N_A04_D20_34	C8	
34	IO_L8P_SRCC_34	L9	
34	IO_L8N_SRCC_34	K9	
34	IO_L9P_MRCC_34	L10	
34	IO_L9N_MRCC_34	M10	
34	IO_L10P_MRCC_34	AC10	
34	IO_L10N_MRCC_34	AB10	
34	IO_L11P_SRCC_34	AH9	
34	IO_L11N_SRCC_34	AJ9	
34	IO_L12P_A03_D19_34	AD10	
34	IO_L12N_A02_D18_34	AC9	
34	IO_L13P_A01_D17_34	AK8	
34	IO_L13N_A00_D16_34	AL8	
34	IO_L14P_A25_34	AD9	
34	IO_L14N_VREF_A24_34	AE9	
34	IO_L15P_A23_34	AK9	
34	IO_L15N_A22_34	AL9	
34	IO_L16P_A21_34	AF9	
34	IO_L16N_A20_34	AF10	
34	IO_L17P_A19_34	AN9	
34	IO_L17N_A18_34	AP9	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
34	IO_L18P_A17_34	AG8	
34	IO_L18N_A16_34	AH8	
34	IO_L19P_VRN_34	AN10	
34	IO_L19N_VRP_34	AP10	
35	IO_L0P_35	G13	
35	IO_L0N_35	H14	
35	IO_L1P_35	D14	
35	IO_L1N_35	C14	
35	IO_L2P_SM0P_35	G11	
35	IO_L2N_SM0N_35	F11	
35	IO_L3P_SM1P_35	A13	
35	IO_L3N_SM1N_35	A14	
35	IO_L4P_35	G12	
35	IO_L4N_VREF_35	H13	
35	IO_L5P_SM2P_35	F14	
35	IO_L5N_SM2N_35	E14	
35	IO_L6P_SM3P_35	H10	
35	IO_L6N_SM3N_35	G10	
35	IO_L7P_SM4P_35	B12	
35	IO_L7N_SM4N_35	B13	
35	IO_L8P_SRCC_35	K14	
35	IO_L8N_SRCC_35	J14	
35	IO_L9P_MRCC_35	L13	
35	IO_L9N_MRCC_35	M13	
35	IO_L10P_MRCC_35	M12	
35	IO_L10N_MRCC_35	M11	
35	IO_L11P_SRCC_35	C13	
35	IO_L11N_SRCC_35	C12	
35	IO_L12P_SM5P_35	H12	
35	IO_L12N_SM5N_35	J12	
35	IO_L13P_SM6P_35	A11	
35	IO_L13N_SM6N_35	B11	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
35	IO_L14P_35	J11	
35	IO_L14N_VREF_35	J10	
35	IO_L15P_SM7P_35	E13	
35	IO_L15N_SM7N_35	F13	
35	IO_L16P_VRN_35	K11	
35	IO_L16N_VRP_35	L11	
35	IO_L17P_35	D12	
35	IO_L17N_35	E12	
35	IO_L18P_GC_35	K13	
35	IO_L18N_GC_35	K12	
35	IO_L19P_GC_35	D11	
35	IO_L19N_GC_35	E11	
36	IO_L0P_36	F18	
36	IO_L0N_36	E17	
36	IO_L1P_36	E18	
36	IO_L1N_36	D17	
36	IO_L2P_36	K18	
36	IO_L2N_36	K17	
36	IO_L3P_36	H17	
36	IO_L3N_36	G17	
36	IO_L4P_36	L19	
36	IO_L4N_VREF_36	L18	
36	IO_L5P_36	C17	
36	IO_L5N_36	B17	
36	IO_L6P_36	K19	
36	IO_L6N_36	J19	
36	IO_L7P_36	M18	
36	IO_L7N_36	M17	
36	IO_L8P_SRCC_36	G18	
36	IO_L8N_SRCC_36	H18	
36	IO_L9P_MRCC_36	K16	
36	IO_L9N_MRCC_36	L16	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
36	IO_L10P_MRCC_36	L15	
36	IO_L10N_MRCC_36	L14	
36	IO_L11P_SRCC_36	A16	
36	IO_L11N_SRCC_36	B16	
36	IO_L12P_VRN_36	F16	
36	IO_L12N_VRP_36	G16	
36	IO_L13P_36	E16	
36	IO_L13N_36	D16	
36	IO_L14P_36	J17	
36	IO_L14N_VREF_36	J16	
36	IO_L15P_36	A15	
36	IO_L15N_36	B15	
36	IO_L16P_36	G15	
36	IO_L16N_36	F15	
36	IO_L17P_36	M16	
36	IO_L17N_36	M15	
36	IO_L18P_36	H15	
36	IO_L18N_36	J15	
36	IO_L19P_36	D15	
36	IO_L19N_36	C15	
112	MGTTXN3_112	AK2	
112	MGTRXN3_112	AJ4	
112	MGTTXP3_112	AK1	
112	MGTRXP3_112	AJ3	
112	MGTTXN2_112	AM2	
112	MGTRXN2_112	AL4	
112	MGTTXP2_112	AM1	
112	MGTRFCLK1P_112	AH6	
112	MGTRFCLK1N_112	AH5	
112	MGTRXP2_112	AL3	
112	MGTRFCLK0P_112	AK6	
112	MGTRFCLK0N_112	AK5	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
112	MGTTXN1_112	AN4	
112	MGTRXN1_112	AM6	
112	MGTTXP1_112	AN3	
112	MGTRXP1_112	AM5	
112	MGTTXN0_112	AP2	
112	MGTRXN0_112	AP6	
112	MGTTXP0_112	AP1	
112	MGTRXP0_112	AP5	
113	MGTTXN3_113	AB2	
113	MGTRXN3_113	AC4	
113	MGTTXP3_113	AB1	
113	MGTRXP3_113	AC3	
113	MGTTXN2_113	AD2	
113	MGTRXN2_113	AE4	
113	MGTTXP2_113	AD1	
113	MGTREFCLK1P_113	AB6	
113	MGTREFCLK1N_113	AB5	
113	MGTRXP2_113	AE3	
113	MGTREFCLK0P_113	AD6	
113	MGTREFCLK0N_113	AD5	
113	MGTTXN1_113	AF2	
113	MGTRXN1_113	AF6	
113	MGTTXP1_113	AF1	
113	MGTRXP1_113	AF5	
113	MGTTXN0_113	AH2	
113	MGTRXN0_113	AG4	
113	MGTTXP0_113	AH1	
113	MGTRXP0_113	AG3	
114	MGTTXN3_114	P2	
114	MGTRXN3_114	R4	
114	MGTTXP3_114	P1	
114	MGTRXP3_114	R3	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
114	MGTTXN2_114	T2	
114	MGTRXN2_114	U4	
114	MGTTXP2_114	T1	
114	MGTREFCLK1P_114	T6	
114	MGTREFCLK1N_114	T5	
114	MGTRXP2_114	U3	
114	MGTREFCLK0P_114	V6	
114	MGTREFCLK0N_114	V5	
114	MGTTXN1_114	V2	
114	MGTRXN1_114	W4	
114	MGTTXP1_114	V1	
114	MGTRXP1_114	W3	
114	MGTTXN0_114	Y2	
114	MGTRXN0_114	AA4	
114	MGTTXP0_114	Y1	
114	MGTRXP0_114	AA3	
115	MGTTXN3_115	F2	
115	MGTRXN3_115	J4	
115	MGTTXP3_115	F1	
115	MGTRXP3_115	J3	
115	MGTTXN2_115	H2	
115	MGTRXN2_115	K6	
115	MGTTXP2_115	H1	
115	MGTREFCLK1P_115	M6	
115	MGTREFCLK1N_115	M5	
115	MGTRXP2_115	K5	
115	MGTAVTTRCAL_115	AP7	
115	MGTRREF_115	AN7	
115	MGTREFCLK0P_115	P6	
115	MGTREFCLK0N_115	P5	
115	MGTTXN1_115	K2	
115	MGTRXN1_115	L4	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
115	MGTTXP1_115	K1	
115	MGTRXP1_115	L3	
115	MGTTXN0_115	M2	
115	MGTRXN0_115	N4	
115	MGTTXP0_115	M1	
115	MGTRXP0_115	N3	
116	MGTTXN3_116	A4	
116	MGTRXN3_116	B6	
116	MGTTXP3_116	A3	
116	MGTRXP3_116	B5	
116	MGTTXN2_116	B2	
116	MGTRXN2_116	D6	
116	MGTTXP2_116	B1	
116	MGTREFCLK1P_116	F6	
116	MGTREFCLK1N_116	F5	
116	MGTRXP2_116	D5	
116	MGTREFCLK0P_116	H6	
116	MGTREFCLK0N_116	H5	
116	MGTTXN1_116	C4	
116	MGTRXN1_116	E4	
116	MGTTXP1_116	C3	
116	MGTRXP1_116	E3	
116	MGTTXN0_116	D2	
116	MGTRXN0_116	G4	
116	MGTTXP0_116	D1	
116	MGTRXP0_116	G3	
NA	MGTAVCC_N	C6	
NA	MGTAVCC_N	E6	
NA	MGTAVCC_N	G6	
NA	MGTAVCC_N	J6	
NA	MGTAVCC_N	L6	
NA	MGTAVCC_N	N6	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTAVCC_S	AA6	
NA	MGTAVCC_S	AC6	
NA	MGTAVCC_S	AE6	
NA	MGTAVCC_S	AG6	
NA	MGTAVCC_S	AJ6	
NA	MGTAVCC_S	AL6	
NA	MGTAVCC_S	AN6	
NA	MGTAVCC_S	R6	
NA	MGTAVCC_S	U6	
NA	MGTAVCC_S	W6	
NA	MGTAVTT_N	C2	
NA	MGTAVTT_N	D3	
NA	MGTAVTT_N	G2	
NA	MGTAVTT_N	H3	
NA	MGTAVTT_N	L2	
NA	MGTAVTT_N	M3	
NA	MGTAVTT_S	AC2	
NA	MGTAVTT_S	AD3	
NA	MGTAVTT_S	AG2	
NA	MGTAVTT_S	AH3	
NA	MGTAVTT_S	AL2	
NA	MGTAVTT_S	AM3	
NA	MGTAVTT_S	R2	
NA	MGTAVTT_S	T3	
NA	MGTAVTT_S	W2	
NA	MGTAVTT_S	Y3	
NA	GND	A1	
NA	GND	A2	
NA	GND	A5	
NA	GND	A6	
NA	GND	A7	
NA	GND	A17	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	A27	
NA	GND	A34	
NA	GND	AA1	
NA	GND	AA2	
NA	GND	AA5	
NA	GND	AA7	
NA	GND	AA9	
NA	GND	AA11	
NA	GND	AA13	
NA	GND	AA15	
NA	GND	AA17	
NA	GND	AA19	
NA	GND	AA21	
NA	GND	AA27	
NA	GND	AB3	
NA	GND	AB4	
NA	GND	AB7	
NA	GND	AB8	
NA	GND	AB12	
NA	GND	AB14	
NA	GND	AB16	
NA	GND	AB18	
NA	GND	AB20	
NA	GND	AB22	
NA	GND	AB24	
NA	GND	AB34	
NA	GND	AC1	
NA	GND	AC5	
NA	GND	AC7	
NA	GND	AC11	
NA	GND	AC21	
NA	GND	AC31	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AD4	
NA	GND	AD7	
NA	GND	AD18	
NA	GND	AD28	
NA	GND	AE1	
NA	GND	AE2	
NA	GND	AE5	
NA	GND	AE7	
NA	GND	AE15	
NA	GND	AE25	
NA	GND	AF3	
NA	GND	AF4	
NA	GND	AF7	
NA	GND	AF12	
NA	GND	AF22	
NA	GND	AF32	
NA	GND	AG1	
NA	GND	AG5	
NA	GND	AG7	
NA	GND	AG9	
NA	GND	AG19	
NA	GND	AG29	
NA	GND	AH4	
NA	GND	AH7	
NA	GND	AH16	
NA	GND	AH26	
NA	GND	AJ1	
NA	GND	AJ2	
NA	GND	AJ5	
NA	GND	AJ7	
NA	GND	AJ13	
NA	GND	AJ23	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AJ33	
NA	GND	AK3	
NA	GND	AK4	
NA	GND	AK7	
NA	GND	AK10	
NA	GND	AK20	
NA	GND	AK30	
NA	GND	AL1	
NA	GND	AL5	
NA	GND	AL7	
NA	GND	AL17	
NA	GND	AL27	
NA	GND	AM4	
NA	GND	AM7	
NA	GND	AM8	
NA	GND	AM14	
NA	GND	AM24	
NA	GND	AM34	
NA	GND	AN1	
NA	GND	AN2	
NA	GND	AN5	
NA	GND	AN8	
NA	GND	AN11	
NA	GND	AN21	
NA	GND	AN31	
NA	GND	AP3	
NA	GND	AP4	
NA	GND	AP8	
NA	GND	AP18	
NA	GND	AP28	
NA	GND	AP34	
NA	GND	B3	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	B4	
NA	GND	B7	
NA	GND	B14	
NA	GND	B24	
NA	GND	C1	
NA	GND	C5	
NA	GND	C7	
NA	GND	C11	
NA	GND	C21	
NA	GND	C31	
NA	GND	D4	
NA	GND	D7	
NA	GND	D8	
NA	GND	D18	
NA	GND	D28	
NA	GND	E1	
NA	GND	E2	
NA	GND	E5	
NA	GND	E7	
NA	GND	E15	
NA	GND	E25	
NA	GND	F3	
NA	GND	F4	
NA	GND	F7	
NA	GND	F12	
NA	GND	F22	
NA	GND	F32	
NA	GND	G1	
NA	GND	G5	
NA	GND	G7	
NA	GND	G9	
NA	GND	G19	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	G29	
NA	GND	H4	
NA	GND	H7	
NA	GND	H16	
NA	GND	H26	
NA	GND	J1	
NA	GND	J2	
NA	GND	J5	
NA	GND	J7	
NA	GND	J8	
NA	GND	J13	
NA	GND	J23	
NA	GND	J33	
NA	GND	K3	
NA	GND	K4	
NA	GND	K7	
NA	GND	K10	
NA	GND	K20	
NA	GND	K30	
NA	GND	L1	
NA	GND	L5	
NA	GND	L7	
NA	GND	L17	
NA	GND	L27	
NA	GND	M4	
NA	GND	M7	
NA	GND	M14	
NA	GND	M20	
NA	GND	M24	
NA	GND	M34	
NA	GND	N1	
NA	GND	N2	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	N5	
NA	GND	N7	
NA	GND	N9	
NA	GND	N11	
NA	GND	N13	
NA	GND	N15	
NA	GND	N17	
NA	GND	N19	
NA	GND	N21	
NA	GND	N31	
NA	GND	P3	
NA	GND	P4	
NA	GND	P7	
NA	GND	P10	
NA	GND	P12	
NA	GND	P14	
NA	GND	P16	
NA	GND	P18	
NA	GND	P20	
NA	GND	P22	
NA	GND	P28	
NA	GND	R1	
NA	GND	R5	
NA	GND	R7	
NA	GND	R9	
NA	GND	R11	
NA	GND	R13	
NA	GND	R15	
NA	GND	R17	
NA	GND	R19	
NA	GND	R21	
NA	GND	R23	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	R25	
NA	GND	T4	
NA	GND	T7	
NA	GND	T10	
NA	GND	T12	
NA	GND	T14	
NA	GND	T16	
NA	GND	T20	
NA	GND	T22	
NA	GND	T32	
NA	GND	U1	
NA	GND	U2	
NA	GND	U5	
NA	GND	U7	
NA	GND	U9	
NA	GND	U11	
NA	GND	U13	
NA	GND	U15	
NA	GND	U19	
NA	GND	U21	
NA	GND	U29	
NA	GND	V3	
NA	GND	V4	
NA	GND	V7	
NA	GND	V10	
NA	GND	V12	
NA	GND	V14	
NA	GND	V16	
NA	GND	V20	
NA	GND	V22	
NA	GND	V26	
NA	GND	W1	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	W5	
NA	GND	W7	
NA	GND	W9	
NA	GND	W11	
NA	GND	W13	
NA	GND	W15	
NA	GND	W19	
NA	GND	W21	
NA	GND	W23	
NA	GND	W33	
NA	GND	Y4	
NA	GND	Y5	
NA	GND	Y6	
NA	GND	Y7	
NA	GND	Y10	
NA	GND	Y12	
NA	GND	Y14	
NA	GND	Y16	
NA	GND	Y18	
NA	GND	Y20	
NA	GND	Y22	
NA	GND	Y30	
NA	GND	T8	
0	VCCO_0	AB9	
0	VCCO_0	Y9	
12	VCCO_12	AF27	
12	VCCO_12	AG34	
12	VCCO_12	AH31	
12	VCCO_12	AL32	
13	VCCO_13	AA32	
13	VCCO_13	AB29	
13	VCCO_13	AC26	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
13	VCCO_13	AD33	
13	VCCO_13	AE30	
14	VCCO_14	T27	
14	VCCO_14	U34	
14	VCCO_14	V31	
14	VCCO_14	W28	
15	VCCO_15	L32	
15	VCCO_15	M29	
15	VCCO_15	N26	
15	VCCO_15	P33	
15	VCCO_15	R30	
16	VCCO_16	A32	
16	VCCO_16	D33	
16	VCCO_16	G34	
16	VCCO_16	H31	
16	VCCO_16	J28	
16	VCCO_16	K25	
22	VCCO_22	AE20	
22	VCCO_22	AH21	
22	VCCO_22	AL22	
22	VCCO_22	AM19	
22	VCCO_22	AP23	
23	VCCO_23	AJ28	
23	VCCO_23	AK25	
23	VCCO_23	AM29	
23	VCCO_23	AN26	
24	VCCO_24	AD23	
24	VCCO_24	AG24	
24	VCCO_24	G24	
24	VCCO_24	L22	
24	VCCO_24	U24	
24	VCCO_24	Y25	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
25	VCCO_25	B29	
25	VCCO_25	C26	
25	VCCO_25	E30	
25	VCCO_25	F27	
26	VCCO_26	A22	
26	VCCO_26	B19	
26	VCCO_26	D23	
26	VCCO_26	E20	
26	VCCO_26	H21	
32	VCCO_32	AC16	
32	VCCO_32	AF17	
32	VCCO_32	AJ18	
32	VCCO_32	AK15	
32	VCCO_32	AN16	
33	VCCO_33	AD13	
33	VCCO_33	AG14	
33	VCCO_33	AH11	
33	VCCO_33	AL12	
33	VCCO_33	AP13	
34	VCCO_34	AE10	
34	VCCO_34	AJ8	
34	VCCO_34	AM9	
34	VCCO_34	B9	
34	VCCO_34	E10	
34	VCCO_34	M9	
35	VCCO_35	A12	
35	VCCO_35	D13	
35	VCCO_35	G14	
35	VCCO_35	H11	
35	VCCO_35	L12	
36	VCCO_36	C16	
36	VCCO_36	F17	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
36	VCCO_36	J18	
36	VCCO_36	K15	
NA	VCCAUX	AA10	
NA	VCCAUX	AA22	
NA	VCCAUX	N10	
NA	VCCAUX	N22	
NA	VCCAUX	P9	
NA	VCCAUX	P23	
NA	VCCAUX	R22	
NA	VCCAUX	T9	
NA	VCCAUX	U22	
NA	VCCAUX	V9	
NA	VCCAUX	W10	
NA	VCCAUX	W22	
NA	VCCAUX	Y23	
NA	VCCINT	AA12	
NA	VCCINT	AA14	
NA	VCCINT	AA16	
NA	VCCINT	AA18	
NA	VCCINT	AA20	
NA	VCCINT	AB11	
NA	VCCINT	AB13	
NA	VCCINT	AB15	
NA	VCCINT	AB17	
NA	VCCINT	AB19	
NA	VCCINT	AB21	
NA	VCCINT	M19	
NA	VCCINT	M21	
NA	VCCINT	N12	
NA	VCCINT	N14	
NA	VCCINT	N16	
NA	VCCINT	N18	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	N20	
NA	VCCINT	P11	
NA	VCCINT	P13	
NA	VCCINT	P15	
NA	VCCINT	P17	
NA	VCCINT	P19	
NA	VCCINT	P21	
NA	VCCINT	R10	
NA	VCCINT	R12	
NA	VCCINT	R14	
NA	VCCINT	R16	
NA	VCCINT	R18	
NA	VCCINT	R20	
NA	VCCINT	T11	
NA	VCCINT	T13	
NA	VCCINT	T15	
NA	VCCINT	T19	
NA	VCCINT	T21	
NA	VCCINT	U10	
NA	VCCINT	U12	
NA	VCCINT	U14	
NA	VCCINT	U16	
NA	VCCINT	U20	
NA	VCCINT	V11	
NA	VCCINT	V13	
NA	VCCINT	V15	
NA	VCCINT	V19	
NA	VCCINT	V21	
NA	VCCINT	W12	
NA	VCCINT	W14	
NA	VCCINT	W16	
NA	VCCINT	W20	

Table 2-5: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	Y11	
NA	VCCINT	Y13	
NA	VCCINT	Y15	
NA	VCCINT	Y17	
NA	VCCINT	Y19	
NA	VCCINT	Y21	

FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, and SX475T

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
0	INIT_B_0	N11	
0	DONE_0	N10	
0	M1_0	AM11	
0	M2_0	AL10	
0	HswapEN_0	P10	
0	PROGRAM_B_0	M11	
0	M0_0	AL11	
0	AVSS_0	Y21	
0	AVDD_0	Y22	
0	VP_0	AA22	
0	VREFP_0	AB22	
0	VN_0	AB21	
0	VREFN_0	AA21	
0	DXP_0	AC22	
0	DXN_0	AC21	
0	VBATT_0	R10	
0	DIN_0	L10	
0	RDWR_B_0	J10	
0	CSI_B_0	T10	
0	DOUT_BUSY_0	AK10	
0	CCLK_0	K10	
0	TDO_0	AR10	
0	TCK_0	AN10	
0	TMS_0	AN11	
0	TDI_0	AP10	
0	VFS_0	AH10	
12	IO_L0P_12	AT37	
12	IO_L0N_12	AR38	
12	IO_L1P_12	AV39	
12	IO_L1N_12	AV38	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
12	IO_L2P_12	AP37	
12	IO_L2N_12	AR37	
12	IO_L3P_12	AY39	
12	IO_L3N_12	BA39	
12	IO_L4P_12	AU37	
12	IO_L4N_VREF_12	AU38	
12	IO_L5P_12	AY38	
12	IO_L5N_12	AY37	
12	IO_L6P_12	AU36	
12	IO_L6N_12	AT36	
12	IO_L7P_12	BB39	
12	IO_L7N_12	BB38	
12	IO_L8P_SRCC_12	AW37	
12	IO_L8N_SRCC_12	AW38	
12	IO_L9P_MRCC_12	AN35	
12	IO_L9N_MRCC_12	AN36	
12	IO_L10P_MRCC_12	AP36	
12	IO_L10N_MRCC_12	AP35	
12	IO_L11P_SRCC_12	BA37	
12	IO_L11N_SRCC_12	BB37	
12	IO_L12P_VRN_12	AR35	
12	IO_L12N_VRP_12	AT35	
12	IO_L13P_12	BB36	
12	IO_L13N_12	BA36	
12	IO_L14P_12	AW36	
12	IO_L14N_VREF_12	AV36	
12	IO_L15P_12	BB34	
12	IO_L15N_12	BA34	
12	IO_L16P_12	AU34	
12	IO_L16N_12	AT34	
12	IO_L17P_12	BA35	
12	IO_L17N_12	AY35	
12	IO_L18P_12	AV34	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
12	IO_L18N_12	AV35	
12	IO_L19P_12	AY34	
12	IO_L19N_12	AW35	
13	IO_L0P_13	AN40	
13	IO_L0N_13	AP40	
13	IO_L1P_13	AN41	
13	IO_L1N_13	AP41	
13	IO_L2P_13	AN39	
13	IO_L2N_13	AM39	
13	IO_L3P_13	AP42	
13	IO_L3N_13	AR42	
13	IO_L4P_13	AL37	
13	IO_L4N_VREF_13	AM38	
13	IO_L5P_13	AT42	
13	IO_L5N_13	AU42	
13	IO_L6P_13	AM34	
13	IO_L6N_13	AL35	
13	IO_L7P_13	AW42	
13	IO_L7N_13	AW41	
13	IO_L8P_SRCC_13	AR40	
13	IO_L8N_SRCC_13	AT41	
13	IO_L9P_MRCC_13	AL34	
13	IO_L9N_MRCC_13	AK34	
13	IO_L10P_MRCC_13	AT40	
13	IO_L10N_MRCC_13	AU39	
13	IO_L11P_SRCC_13	AV41	
13	IO_L11N_SRCC_13	AU41	
13	IO_L12P_VRN_13	AN38	
13	IO_L12N_VRP_13	AP38	
13	IO_L13P_13	AY42	
13	IO_L13N_13	BA42	
13	IO_L14P_13	AR39	
13	IO_L14N_VREF_13	AT39	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
13	IO_L15P_13	BA41	
13	IO_L15N_13	BB41	
13	IO_L16P_13	AM37	
13	IO_L16N_13	AM36	
13	IO_L17P_13	BA40	
13	IO_L17N_13	AY40	
13	IO_L18P_13	AK35	
13	IO_L18N_13	AL36	
13	IO_L19P_13	AV40	
13	IO_L19N_13	AW40	
14	IO_L0P_14	AG34	
14	IO_L0N_14	AF34	
14	IO_L1P_14	AF40	
14	IO_L1N_14	AG41	
14	IO_L2P_14	AF39	
14	IO_L2N_14	AG39	
14	IO_L3P_14	AG42	
14	IO_L3N_14	AH41	
14	IO_L4P_14	AG38	
14	IO_L4N_VREF_14	AH38	
14	IO_L5P_14	AH40	
14	IO_L5N_14	AJ41	
14	IO_L6P_14	AF37	
14	IO_L6N_14	AG37	
14	IO_L7P_14	AJ42	
14	IO_L7N_14	AK42	
14	IO_L8P_SRCC_14	AK38	
14	IO_L8N_SRCC_14	AJ38	
14	IO_L9P_MRCC_14	AH34	
14	IO_L9N_MRCC_14	AJ35	
14	IO_L10P_MRCC_14	AJ37	
14	IO_L10N_MRCC_14	AK37	
14	IO_L11P_SRCC_14	AH39	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
14	IO_L11N_SRCC_14	AJ40	
14	IO_L12P_VRN_14	AJ36	
14	IO_L12N_VRP_14	AH35	
14	IO_L13P_14	AL42	
14	IO_L13N_14	AM42	
14	IO_L14P_14	AG36	
14	IO_L14N_VREF_14	AH36	
14	IO_L15P_14	AL41	
14	IO_L15N_14	AM41	
14	IO_L16P_14	AF35	
14	IO_L16N_14	AF36	
14	IO_L17P_14	AK40	
14	IO_L17N_14	AL40	
14	IO_L18P_14	AF32	
14	IO_L18N_14	AG33	
14	IO_L19P_14	AK39	
14	IO_L19N_14	AL39	
15	IO_L0P_15	AE34	
15	IO_L0N_15	AE35	
15	IO_L1P_15	AB37	
15	IO_L1N_15	AB38	
15	IO_L2P_SM8P_15	AE33	
15	IO_L2N_SM8N_15	AD33	
15	IO_L3P_SM9P_15	AB39	
15	IO_L3N_SM9N_15	AA40	
15	IO_L4P_15	AC38	
15	IO_L4N_VREF_15	AC39	
15	IO_L5P_SM10P_15	AA41	
15	IO_L5N_SM10N_15	AB41	
15	IO_L6P_SM11P_15	AE38	
15	IO_L6N_SM11N_15	AD38	
15	IO_L7P_SM12P_15	AA42	
15	IO_L7N_SM12N_15	AB42	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
15	IO_L8P_SRCC_15	AC36	
15	IO_L8N_SRCC_15	AB36	
15	IO_L9P_MRCC_15	AD32	
15	IO_L9N_MRCC_15	AE32	
15	IO_L10P_MRCC_15	AE37	
15	IO_L10N_MRCC_15	AD37	
15	IO_L11P_SRCC_15	AC41	
15	IO_L11N_SRCC_15	AD41	
15	IO_L12P_SM13P_15	AB32	
15	IO_L12N_SM13N_15	AB33	
15	IO_L13P_SM14P_15	AC40	
15	IO_L13N_SM14N_15	AD40	
15	IO_L14P_15	AD36	
15	IO_L14N_VREF_15	AD35	
15	IO_L15P_SM15P_15	AD42	
15	IO_L15N_SM15N_15	AE42	
15	IO_L16P_VRN_15	AC35	
15	IO_L16N_VRP_15	AB34	
15	IO_L17P_15	AF42	
15	IO_L17N_15	AF41	
15	IO_L18P_15	AC34	
15	IO_L18N_15	AC33	
15	IO_L19P_15	AE40	
15	IO_L19N_15	AE39	
16	IO_L0P_16	W37	
16	IO_L0N_16	Y37	
16	IO_L1P_16	U37	
16	IO_L1N_16	U38	
16	IO_L2P_16	W36	
16	IO_L2N_16	V36	
16	IO_L3P_16	U42	
16	IO_L3N_16	U41	
16	IO_L4P_16	AA36	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
16	IO_L4N_VREF_16	AA37	
16	IO_L5P_16	U39	
16	IO_L5N_16	V39	
16	IO_L6P_16	W35	
16	IO_L6N_16	V35	
16	IO_L7P_16	V38	
16	IO_L7N_16	W38	
16	IO_L8P_SRCC_16	AA35	
16	IO_L8N_SRCC_16	Y35	
16	IO_L9P_MRCC_16	W32	
16	IO_L9N_MRCC_16	Y33	
16	IO_L10P_MRCC_16	V34	
16	IO_L10N_MRCC_16	U34	
16	IO_L11P_SRCC_16	V40	
16	IO_L11N_SRCC_16	W40	
16	IO_L12P_VRN_16	AA32	
16	IO_L12N_VRP_16	Y32	
16	IO_L13P_16	V41	
16	IO_L13N_16	W41	
16	IO_L14P_16	AA34	
16	IO_L14N_VREF_16	Y34	
16	IO_L15P_16	W42	
16	IO_L15N_16	Y42	
16	IO_L16P_16	U32	
16	IO_L16N_16	U33	
16	IO_L17P_16	Y40	
16	IO_L17N_16	Y39	
16	IO_L18P_16	V33	
16	IO_L18N_16	W33	
16	IO_L19P_16	Y38	
16	IO_L19N_16	AA39	
17	IO_L0P_17	M36	
17	IO_L0N_17	M37	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
17	IO_L1P_17	L39	
17	IO_L1N_17	L40	
17	IO_L2P_17	M38	
17	IO_L2N_17	M39	
17	IO_L3P_17	L41	
17	IO_L3N_17	L42	
17	IO_L4P_17	N35	
17	IO_L4N_VREF_17	N34	
17	IO_L5P_17	N38	
17	IO_L5N_17	N39	
17	IO_L6P_17	N36	
17	IO_L6N_17	P37	
17	IO_L7P_17	M41	
17	IO_L7N_17	M42	
17	IO_L8P_SRCC_17	R39	
17	IO_L8N_SRCC_17	P38	
17	IO_L9P_MRCC_17	P36	
17	IO_L9N_MRCC_17	P35	
17	IO_L10P_MRCC_17	T39	
17	IO_L10N_MRCC_17	R38	
17	IO_L11P_SRCC_17	N40	
17	IO_L11N_SRCC_17	N41	
17	IO_L12P_VRN_17	R37	
17	IO_L12N_VRP_17	T37	
17	IO_L13P_17	P40	
17	IO_L13N_17	P41	
17	IO_L14P_17	R35	
17	IO_L14N_VREF_17	R34	
17	IO_L15P_17	P42	
17	IO_L15N_17	R42	
17	IO_L16P_17	U36	
17	IO_L16N_17	T36	
17	IO_L17P_17	R40	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
17	IO_L17N_17	T40	
17	IO_L18P_17	T34	
17	IO_L18N_17	T35	
17	IO_L19P_17	T41	
17	IO_L19N_17	T42	
21	IO_L0P_21	AT26	LX240T,LX365T,SX315T
21	IO_L0N_21	AU27	LX240T,LX365T,SX315T
21	IO_L1P_21	AK22	LX240T,LX365T,SX315T
21	IO_L1N_21	AJ22	LX240T,LX365T,SX315T
21	IO_L2P_21	AY27	LX240T,LX365T,SX315T
21	IO_L2N_21	AW27	LX240T,LX365T,SX315T
21	IO_L3P_21	AM22	LX240T,LX365T,SX315T
21	IO_L3N_21	AL22	LX240T,LX365T,SX315T
21	IO_L4P_21	BA26	LX240T,LX365T,SX315T
21	IO_L4N_VREF_21	BA27	LX240T,LX365T,SX315T
21	IO_L5P_21	AJ23	LX240T,LX365T,SX315T
21	IO_L5N_21	AK23	LX240T,LX365T,SX315T
21	IO_L6P_21	BB26	LX240T,LX365T,SX315T
21	IO_L6N_21	BB27	LX240T,LX365T,SX315T
21	IO_L7P_21	AM23	LX240T,LX365T,SX315T
21	IO_L7N_21	AN23	LX240T,LX365T,SX315T
21	IO_L8P_SRCC_21	AU23	LX240T,LX365T,SX315T
21	IO_L8N_SRCC_21	AU24	LX240T,LX365T,SX315T
21	IO_L9P_MRCC_21	AP25	LX240T,LX365T,SX315T
21	IO_L9N_MRCC_21	AP26	LX240T,LX365T,SX315T
21	IO_L10P_MRCC_21	AK24	LX240T,LX365T,SX315T
21	IO_L10N_MRCC_21	AL25	LX240T,LX365T,SX315T
21	IO_L11P_SRCC_21	AP23	LX240T,LX365T,SX315T
21	IO_L11N_SRCC_21	AR23	LX240T,LX365T,SX315T
21	IO_L12P_VRN_21	AV24	LX240T,LX365T,SX315T
21	IO_L12N_VRP_21	AV25	LX240T,LX365T,SX315T
21	IO_L13P_21	AM24	LX240T,LX365T,SX315T
21	IO_L13N_21	AL24	LX240T,LX365T,SX315T

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
21	IO_L14P_21	BA25	LX240T,LX365T,SX315T
21	IO_L14N_VREF_21	AY25	LX240T,LX365T,SX315T
21	IO_L15P_21	AN24	LX240T,LX365T,SX315T
21	IO_L15N_21	AN25	LX240T,LX365T,SX315T
21	IO_L16P_21	AV26	LX240T,LX365T,SX315T
21	IO_L16N_21	AU26	LX240T,LX365T,SX315T
21	IO_L17P_21	AR24	LX240T,LX365T,SX315T
21	IO_L17N_21	AT24	LX240T,LX365T,SX315T
21	IO_L18P_21	AW25	LX240T,LX365T,SX315T
21	IO_L18N_21	AW26	LX240T,LX365T,SX315T
21	IO_L19P_21	AT25	LX240T,LX365T,SX315T
21	IO_L19N_21	AR25	LX240T,LX365T,SX315T
22	IO_L0P_22	AW30	
22	IO_L0N_22	AV30	
22	IO_L1P_22	AN26	
22	IO_L1N_22	AP27	
22	IO_L2P_22	AW31	
22	IO_L2N_22	AV31	
22	IO_L3P_22	AR28	
22	IO_L3N_22	AP28	
22	IO_L4P_22	AY32	
22	IO_L4N_VREF_22	AW32	
22	IO_L5P_22	AT29	
22	IO_L5N_22	AR29	
22	IO_L6P_22	BA32	
22	IO_L6N_22	AY33	
22	IO_L7P_22	AT30	
22	IO_L7N_22	AR30	
22	IO_L8P_SRCC_22	BA30	
22	IO_L8N_SRCC_22	AY30	
22	IO_L9P_MRCC_22	AM26	
22	IO_L9N_MRCC_22	AL26	
22	IO_L10P_MRCC_22	AN28	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
22	IO_L10N_MRCC_22	AM27	
22	IO_L11P_SRCC_22	AR27	
22	IO_L11N_SRCC_22	AT27	
22	IO_L12P_VRN_22	AY29	
22	IO_L12N_VRP_22	BA29	
22	IO_L13P_22	AT31	
22	IO_L13N_22	AU31	
22	IO_L14P_22	BB33	
22	IO_L14N_VREF_22	BB32	
22	IO_L15P_22	AU29	
22	IO_L15N_22	AV29	
22	IO_L16P_22	BA31	
22	IO_L16N_22	BB31	
22	IO_L17P_22	AU28	
22	IO_L17N_22	AV28	
22	IO_L18P_22	BB29	
22	IO_L18N_22	BB28	
22	IO_L19P_22	AW28	
22	IO_L19N_22	AY28	
23	IO_L0P_23	AP30	
23	IO_L0N_23	AN30	
23	IO_L1P_23	AM31	
23	IO_L1N_23	AL31	
23	IO_L2P_23	AL29	
23	IO_L2N_23	AL30	
23	IO_L3P_23	AM33	
23	IO_L3N_23	AM32	
23	IO_L4P_23	AN29	
23	IO_L4N_VREF_23	AM29	
23	IO_L5P_23	AN33	
23	IO_L5N_23	AN34	
23	IO_L6P_23	AL27	
23	IO_L6N_23	AM28	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
23	IO_L7P_23	AP31	
23	IO_L7N_23	AN31	
23	IO_L8P_SRCC_23	AK28	
23	IO_L8N_SRCC_23	AK29	
23	IO_L9P_MRCC_23	AJ25	
23	IO_L9N_MRCC_23	AK25	
23	IO_L10P_MRCC_23	AH24	
23	IO_L10N_MRCC_23	AH25	
23	IO_L11P_SRCC_23	AR34	
23	IO_L11N_SRCC_23	AP33	
23	IO_L12P_VRN_23	AH28	
23	IO_L12N_VRP_23	AJ28	
23	IO_L13P_23	AP32	
23	IO_L13N_23	AR32	
23	IO_L14P_23	AG28	
23	IO_L14N_VREF_23	AG27	
23	IO_L15P_23	AR33	
23	IO_L15N_23	AT32	
23	IO_L16P_23	AK27	
23	IO_L16N_23	AJ27	
23	IO_L17P_23	AU33	
23	IO_L17N_23	AU32	
23	IO_L18P_23	AJ26	
23	IO_L18N_23	AH26	
23	IO_L19P_23	AV33	
23	IO_L19N_23	AW33	
24	IO_L0P_GC_24	AE30	
24	IO_L0N_GC_24	AF30	
24	IO_L1P_GC_24	W30	
24	IO_L1N_GC_24	V30	
24	IO_L2P_D15_24	AG32	
24	IO_L2N_D14_24	AF31	
24	IO_L3P_D13_24	T30	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
24	IO_L3N_D12_24	R30	
24	IO_L4P_D11_24	AH31	
24	IO_L4N_VREF_D10_24	AG31	
24	IO_L5P_D9_24	N33	
24	IO_L5N_D8_24	P33	
24	IO_L6P_D7_24	AJ33	
24	IO_L6N_D6_24	AH33	
24	IO_L7P_D5_24	P32	
24	IO_L7N_D4_24	R33	
24	IO_L8P_SRCC_24	AK33	
24	IO_L8N_SRCC_24	AJ32	
24	IO_L9P_MRCC_24	Y30	
24	IO_L9N_MRCC_24	AA30	
24	IO_L10P_MRCC_24	AA31	
24	IO_L10N_MRCC_24	AB31	
24	IO_L11P_SRCC_24	R32	
24	IO_L11N_SRCC_24	T32	
24	IO_L12P_D3_24	AK32	
24	IO_L12N_D2_FS2_24	AL32	
24	IO_L13P_D1_FS1_24	T31	
24	IO_L13N_D0_FS0_24	U31	
24	IO_L14P_FCS_B_24	AH30	
24	IO_L14N_VREF_FOE_B_MOSTI_24	AJ30	
24	IO_L15P_FWE_B_24	V31	
24	IO_L15N_RS1_24	W31	
24	IO_L16P_RS0_24	AJ31	
24	IO_L16N_CS0_B_24	AK30	
24	IO_L17P_VRN_24	AC31	
24	IO_L17N_VRP_24	AC30	
24	IO_L18P_24	AH29	
24	IO_L18N_24	AG29	
24	IO_L19P_24	AD31	
24	IO_L19N_24	AD30	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
25	IO_L0P_25	K33	
25	IO_L0N_25	K32	
25	IO_L1P_25	N28	
25	IO_L1N_25	P28	
25	IO_L2P_25	K35	
25	IO_L2N_25	K34	
25	IO_L3P_25	L31	
25	IO_L3N_25	L32	
25	IO_L4P_25	J37	
25	IO_L4N_VREF_25	J36	
25	IO_L5P_25	N29	
25	IO_L5N_25	N30	
25	IO_L6P_25	H39	
25	IO_L6N_25	H38	
25	IO_L7P_25	L35	
25	IO_L7N_25	L36	
25	IO_L8P_SRCC_25	K38	
25	IO_L8N_SRCC_25	J38	
25	IO_L9P_MRCC_25	P27	
25	IO_L9N_MRCC_25	R27	
25	IO_L10P_MRCC_25	R28	
25	IO_L10N_MRCC_25	R29	
25	IO_L11P_SRCC_25	K37	
25	IO_L11N_SRCC_25	L37	
25	IO_L12P_25	H40	
25	IO_L12N_25	H41	
25	IO_L13P_25	L34	
25	IO_L13N_25	M34	
25	IO_L14P_25	J40	
25	IO_L14N_VREF_25	J41	
25	IO_L15P_25	M33	
25	IO_L15N_25	M32	
25	IO_L16P_VRN_25	K39	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
25	IO_L16N_VRP_25	K40	
25	IO_L17P_25	M31	
25	IO_L17N_25	N31	
25	IO_L18P_GC_25	J42	
25	IO_L18N_GC_25	K42	
25	IO_L19P_GC_25	P30	
25	IO_L19N_GC_25	P31	
26	IO_L0P_26	H36	
26	IO_L0N_26	G36	
26	IO_L1P_26	B37	
26	IO_L1N_26	A37	
26	IO_L2P_26	J35	
26	IO_L2N_26	H35	
26	IO_L3P_26	B38	
26	IO_L3N_26	A39	
26	IO_L4P_26	F37	
26	IO_L4N_VREF_26	E37	
26	IO_L5P_26	B39	
26	IO_L5N_26	C39	
26	IO_L6P_26	D38	
26	IO_L6N_26	C38	
26	IO_L7P_26	A40	
26	IO_L7N_26	A41	
26	IO_L8P_SRCC_26	E39	
26	IO_L8N_SRCC_26	E38	
26	IO_L9P_MRCC_26	G34	
26	IO_L9N_MRCC_26	H34	
26	IO_L10P_MRCC_26	F35	
26	IO_L10N_MRCC_26	F36	
26	IO_L11P_SRCC_26	B41	
26	IO_L11N_SRCC_26	B42	
26	IO_L12P_VRN_26	F39	
26	IO_L12N_VRP_26	G39	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
26	IO_L13P_26	C40	
26	IO_L13N_26	C41	
26	IO_L14P_26	G37	
26	IO_L14N_VREF_26	G38	
26	IO_L15P_26	D42	
26	IO_L15N_26	D41	
26	IO_L16P_26	F40	
26	IO_L16N_26	F41	
26	IO_L17P_26	D40	
26	IO_L17N_26	E40	
26	IO_L18P_26	G41	
26	IO_L18N_26	G42	
26	IO_L19P_26	E42	
26	IO_L19N_26	F42	
27	IO_L0P_27	E32	
27	IO_L0N_27	D32	
27	IO_L1P_27	A32	
27	IO_L1N_27	B32	
27	IO_L2P_27	F32	
27	IO_L2N_27	F31	
27	IO_L3P_27	B33	
27	IO_L3N_27	C33	
27	IO_L4P_27	E35	
27	IO_L4N_VREF_27	D35	
27	IO_L5P_27	A34	
27	IO_L5N_27	A35	
27	IO_L6P_27	H31	
27	IO_L6N_27	G31	
27	IO_L7P_27	B34	
27	IO_L7N_27	C34	
27	IO_L8P_SRCC_27	G33	
27	IO_L8N_SRCC_27	G32	
27	IO_L9P_MRCC_27	L29	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
27	IO_L9N_MRCC_27	L30	
27	IO_L10P_MRCC_27	M28	
27	IO_L10N_MRCC_27	M29	
27	IO_L11P_SRCC_27	D33	
27	IO_L11N_SRCC_27	E33	
27	IO_L12P_VRN_27	H33	
27	IO_L12N_VRP_27	J33	
27	IO_L13P_27	A36	
27	IO_L13N_27	B36	
27	IO_L14P_27	J32	
27	IO_L14N_VREF_27	J31	
27	IO_L15P_27	C35	
27	IO_L15N_27	C36	
27	IO_L16P_27	H30	
27	IO_L16N_27	J30	
27	IO_L17P_27	E34	
27	IO_L17N_27	F34	
27	IO_L18P_27	K29	
27	IO_L18N_27	K30	
27	IO_L19P_27	D36	
27	IO_L19N_27	D37	
28	IO_L0P_28	J27	LX240T,LX365T,SX315T
28	IO_L0N_28	J26	LX240T,LX365T,SX315T
28	IO_L1P_28	D28	LX240T,LX365T,SX315T
28	IO_L1N_28	E29	LX240T,LX365T,SX315T
28	IO_L2P_28	G28	LX240T,LX365T,SX315T
28	IO_L2N_28	G27	LX240T,LX365T,SX315T
28	IO_L3P_28	E30	LX240T,LX365T,SX315T
28	IO_L3N_28	F30	LX240T,LX365T,SX315T
28	IO_L4P_28	G29	LX240T,LX365T,SX315T
28	IO_L4N_VREF_28	F29	LX240T,LX365T,SX315T
28	IO_L5P_28	C31	LX240T,LX365T,SX315T
28	IO_L5N_28	D31	LX240T,LX365T,SX315T

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
28	IO_L6P_28	R23	LX240T,LX365T,SX315T
28	IO_L6N_28	P23	LX240T,LX365T,SX315T
28	IO_L7P_28	C30	LX240T,LX365T,SX315T
28	IO_L7N_28	D30	LX240T,LX365T,SX315T
28	IO_L8P_SRCC_28	R25	LX240T,LX365T,SX315T
28	IO_L8N_SRCC_28	P25	LX240T,LX365T,SX315T
28	IO_L9P_MRCC_28	L26	LX240T,LX365T,SX315T
28	IO_L9N_MRCC_28	L25	LX240T,LX365T,SX315T
28	IO_L10P_MRCC_28	N24	LX240T,LX365T,SX315T
28	IO_L10N_MRCC_28	N25	LX240T,LX365T,SX315T
28	IO_L11P_SRCC_28	F27	LX240T,LX365T,SX315T
28	IO_L11N_SRCC_28	E28	LX240T,LX365T,SX315T
28	IO_L12P_VRN_28	P26	LX240T,LX365T,SX315T
28	IO_L12N_VRP_28	N26	LX240T,LX365T,SX315T
28	IO_L13P_28	A31	LX240T,LX365T,SX315T
28	IO_L13N_28	B31	LX240T,LX365T,SX315T
28	IO_L14P_28	H28	LX240T,LX365T,SX315T
28	IO_L14N_VREF_28	H29	LX240T,LX365T,SX315T
28	IO_L15P_28	B29	LX240T,LX365T,SX315T
28	IO_L15N_28	C29	LX240T,LX365T,SX315T
28	IO_L16P_28	J28	LX240T,LX365T,SX315T
28	IO_L16N_28	K28	LX240T,LX365T,SX315T
28	IO_L17P_28	A29	LX240T,LX365T,SX315T
28	IO_L17N_28	A30	LX240T,LX365T,SX315T
28	IO_L18P_28	L27	LX240T,LX365T,SX315T
28	IO_L18N_28	K27	LX240T,LX365T,SX315T
28	IO_L19P_28	M26	LX240T,LX365T,SX315T
28	IO_L19N_28	M27	LX240T,LX365T,SX315T
32	IO_L0P_32	AY24	
32	IO_L0N_32	BA24	
32	IO_L1P_32	AL19	
32	IO_L1N_32	AM19	
32	IO_L2P_32	AV23	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
32	IO_L2N_32	AU22	
32	IO_L3P_32	AT20	
32	IO_L3N_32	AR20	
32	IO_L4P_32	AW23	
32	IO_L4N_VREF_32	AY23	
32	IO_L5P_32	AL20	
32	IO_L5N_32	AL21	
32	IO_L6P_32	BB24	
32	IO_L6N_32	BB23	
32	IO_L7P_32	AN20	
32	IO_L7N_32	AP20	
32	IO_L8P_SRCC_32	AY20	
32	IO_L8N_SRCC_32	BA20	
32	IO_L9P_MRCC_32	AJ21	
32	IO_L9N_MRCC_32	AJ20	
32	IO_L10P_MRCC_32	AK20	
32	IO_L10N_MRCC_32	AK19	
32	IO_L11P_SRCC_32	AM21	
32	IO_L11N_SRCC_32	AN21	
32	IO_L12P_VRN_32	AV21	
32	IO_L12N_VRP_32	AW21	
32	IO_L13P_32	AV20	
32	IO_L13N_32	AW20	
32	IO_L14P_32	BA22	
32	IO_L14N_VREF_32	BA21	
32	IO_L15P_32	AU21	
32	IO_L15N_32	AT21	
32	IO_L16P_32	AW22	
32	IO_L16N_32	AY22	
32	IO_L17P_32	AT22	
32	IO_L17N_32	AR22	
32	IO_L18P_32	BB22	
32	IO_L18N_32	BB21	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
32	IO_L19P_32	AP21	
32	IO_L19N_32	AP22	
33	IO_L0P_33	AL15	
33	IO_L0N_33	AL14	
33	IO_L1P_33	AR17	
33	IO_L1N_33	AR18	
33	IO_L2P_33	AN15	
33	IO_L2N_33	AM14	
33	IO_L3P_33	AT16	
33	IO_L3N_33	AU17	
33	IO_L4P_33	AL17	
33	IO_L4N_VREF_33	AL16	
33	IO_L5P_33	AT17	
33	IO_L5N_33	AU18	
33	IO_L6P_33	AJ17	
33	IO_L6N_33	AK17	
33	IO_L7P_33	AY18	
33	IO_L7N_33	AW18	
33	IO_L8P_SRCC_33	AN16	
33	IO_L8N_SRCC_33	AM16	
33	IO_L9P_MRCC_33	AK15	
33	IO_L9N_MRCC_33	AK14	
33	IO_L10P_MRCC_33	AJ16	
33	IO_L10N_MRCC_33	AJ15	
33	IO_L11P_SRCC_33	AP18	
33	IO_L11N_SRCC_33	AR19	
33	IO_L12P_VRN_33	AP16	
33	IO_L12N_VRP_33	AP17	
33	IO_L13P_33	AV18	
33	IO_L13N_33	AV19	
33	IO_L14P_33	AM17	
33	IO_L14N_VREF_33	AM18	
33	IO_L15P_33	BB18	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
33	IO_L15N_33	BB19	
33	IO_L16P_33	AN18	
33	IO_L16N_33	AN19	
33	IO_L17P_33	BA19	
33	IO_L17N_33	AY19	
33	IO_L18P_33	AK18	
33	IO_L18N_33	AJ18	
33	IO_L19P_33	AU19	
33	IO_L19N_33	AT19	
34	IO_L0P_GC_34	AY14	
34	IO_L0N_GC_34	AY13	
34	IO_L1P_GC_34	AP11	
34	IO_L1N_GC_34	AP12	
34	IO_L2P_A15_D31_34	BA15	
34	IO_L2N_A14_D30_34	BA14	
34	IO_L3P_A13_D29_34	AR12	
34	IO_L3N_A12_D28_34	AT12	
34	IO_L4P_A11_D27_34	AV15	
34	IO_L4N_VREF_A10_D26_34	AU14	
34	IO_L5P_A09_D25_34	AP13	
34	IO_L5N_A08_D24_34	AR13	
34	IO_L6P_A07_D23_34	AY15	
34	IO_L6N_A06_D22_34	AW15	
34	IO_L7P_A05_D21_34	AU12	
34	IO_L7N_A04_D20_34	AU13	
34	IO_L8P_SRCC_34	AV16	
34	IO_L8N_SRCC_34	AW16	
34	IO_L9P_MRCC_34	AM13	
34	IO_L9N_MRCC_34	AM12	
34	IO_L10P_MRCC_34	AN14	
34	IO_L10N_MRCC_34	AN13	
34	IO_L11P_SRCC_34	AV13	
34	IO_L11N_SRCC_34	AV14	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
34	IO_L12P_A03_D19_34	BB13	
34	IO_L12N_A02_D18_34	BB14	
34	IO_L13P_A01_D17_34	AW12	
34	IO_L13N_A00_D16_34	AW13	
34	IO_L14P_A25_34	BA16	
34	IO_L14N_VREF_A24_34	BA17	
34	IO_L15P_A23_34	AR14	
34	IO_L15N_A22_34	AT14	
34	IO_L16P_A21_34	BB16	
34	IO_L16N_A20_34	BB17	
34	IO_L17P_A19_34	AP15	
34	IO_L17N_A18_34	AR15	
34	IO_L18P_A17_34	AY17	
34	IO_L18N_A16_34	AW17	
34	IO_L19P_VRN_34	AT15	
34	IO_L19N_VRP_34	AU16	
35	IO_L0P_35	F12	
35	IO_L0N_35	E12	
35	IO_L1P_35	A16	
35	IO_L1N_35	B16	
35	IO_L2P_SM0P_35	H15	
35	IO_L2N_SM0N_35	G14	
35	IO_L3P_SM1P_35	D16	
35	IO_L3N_SM1N_35	C16	
35	IO_L4P_35	H14	
35	IO_L4N_VREF_35	G13	
35	IO_L5P_SM2P_35	A15	
35	IO_L5N_SM2N_35	A14	
35	IO_L6P_SM3P_35	H13	
35	IO_L6N_SM3N_35	G12	
35	IO_L7P_SM4P_35	C15	
35	IO_L7N_SM4N_35	D15	
35	IO_L8P_SRCC_35	J12	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
35	IO_L8N_SRCC_35	J11	
35	IO_L9P_MRCC_35	M14	
35	IO_L9N_MRCC_35	N14	
35	IO_L10P_MRCC_35	M13	
35	IO_L10N_MRCC_35	N13	
35	IO_L11P_SRCC_35	E15	
35	IO_L11N_SRCC_35	F15	
35	IO_L12P_SM5P_35	J13	
35	IO_L12N_SM5N_35	K13	
35	IO_L13P_SM6P_35	B14	
35	IO_L13N_SM6N_35	C14	
35	IO_L14P_35	K14	
35	IO_L14N_VREF_35	L14	
35	IO_L15P_SM7P_35	C13	
35	IO_L15N_SM7N_35	D12	
35	IO_L16P_VRN_35	K12	
35	IO_L16N_VRP_35	L11	
35	IO_L17P_35	D13	
35	IO_L17N_35	E13	
35	IO_L18P_GC_35	L12	
35	IO_L18N_GC_35	M12	
35	IO_L19P_GC_35	E14	
35	IO_L19N_GC_35	F14	
36	IO_L0P_36	K18	
36	IO_L0N_36	J18	
36	IO_L1P_36	H18	
36	IO_L1N_36	G18	
36	IO_L2P_36	G16	
36	IO_L2N_36	F16	
36	IO_L3P_36	G19	
36	IO_L3N_36	F19	
36	IO_L4P_36	J16	
36	IO_L4N_VREF_36	H16	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
36	IO_L5P_36	E19	
36	IO_L5N_36	E18	
36	IO_L6P_36	K17	
36	IO_L6N_36	J17	
36	IO_L7P_36	C19	
36	IO_L7N_36	B19	
36	IO_L8P_SRCC_36	M18	
36	IO_L8N_SRCC_36	N18	
36	IO_L9P_MRCC_36	P18	
36	IO_L9N_MRCC_36	P17	
36	IO_L10P_MRCC_36	N16	
36	IO_L10N_MRCC_36	P16	
36	IO_L11P_SRCC_36	F17	
36	IO_L11N_SRCC_36	G17	
36	IO_L12P_VRN_36	L17	
36	IO_L12N_VRP_36	M17	
36	IO_L13P_36	D18	
36	IO_L13N_36	C18	
36	IO_L14P_36	J15	
36	IO_L14N_VREF_36	K15	
36	IO_L15P_36	B18	
36	IO_L15N_36	A19	
36	IO_L16P_36	L16	
36	IO_L16N_36	L15	
36	IO_L17P_36	A17	
36	IO_L17N_36	B17	
36	IO_L18P_36	M16	
36	IO_L18N_36	N15	
36	IO_L19P_36	D17	
36	IO_L19N_36	E17	
37	IO_L0P_37	G23	
37	IO_L0N_37	H23	
37	IO_L1P_37	B24	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
37	IO_L1N_37	A24	
37	IO_L2P_37	G22	
37	IO_L2N_37	F22	
37	IO_L3P_37	C24	
37	IO_L3N_37	C23	
37	IO_L4P_37	F21	
37	IO_L4N_VREF_37	E22	
37	IO_L5P_37	B23	
37	IO_L5N_37	B22	
37	IO_L6P_37	H21	
37	IO_L6N_37	J21	
37	IO_L7P_37	E24	
37	IO_L7N_37	E23	
37	IO_L8P_SRCC_37	H20	
37	IO_L8N_SRCC_37	G21	
37	IO_L9P_MRCC_37	L22	
37	IO_L9N_MRCC_37	L21	
37	IO_L10P_MRCC_37	J22	
37	IO_L10N_MRCC_37	K22	
37	IO_L11P_SRCC_37	D23	
37	IO_L11N_SRCC_37	D22	
37	IO_L12P_VRN_37	E20	
37	IO_L12N_VRP_37	F20	
37	IO_L13P_37	A22	
37	IO_L13N_37	A21	
37	IO_L14P_37	J20	
37	IO_L14N_VREF_37	H19	
37	IO_L15P_37	B21	
37	IO_L15N_37	A20	
37	IO_L16P_37	K20	
37	IO_L16N_37	L20	
37	IO_L17P_37	C21	
37	IO_L17N_37	D21	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
37	IO_L18P_37	K19	
37	IO_L18N_37	L19	
37	IO_L19P_37	C20	
37	IO_L19N_37	D20	
38	IO_L0P_38	H24	LX240T,LX365T,SX315T
38	IO_L0N_38	G24	LX240T,LX365T,SX315T
38	IO_L1P_38	E27	LX240T,LX365T,SX315T
38	IO_L1N_38	D27	LX240T,LX365T,SX315T
38	IO_L2P_38	F25	LX240T,LX365T,SX315T
38	IO_L2N_38	F24	LX240T,LX365T,SX315T
38	IO_L3P_38	C28	LX240T,LX365T,SX315T
38	IO_L3N_38	B28	LX240T,LX365T,SX315T
38	IO_L4P_38	H26	LX240T,LX365T,SX315T
38	IO_L4N_VREF_38	H25	LX240T,LX365T,SX315T
38	IO_L5P_38	G26	LX240T,LX365T,SX315T
38	IO_L5N_38	F26	LX240T,LX365T,SX315T
38	IO_L6P_38	K25	LX240T,LX365T,SX315T
38	IO_L6N_38	J25	LX240T,LX365T,SX315T
38	IO_L7P_38	B27	LX240T,LX365T,SX315T
38	IO_L7N_38	A27	LX240T,LX365T,SX315T
38	IO_L8P_SRCC_38	J23	LX240T,LX365T,SX315T
38	IO_L8N_SRCC_38	K23	LX240T,LX365T,SX315T
38	IO_L9P_MRCC_38	M19	LX240T,LX365T,SX315T
38	IO_L9N_MRCC_38	N19	LX240T,LX365T,SX315T
38	IO_L10P_MRCC_38	N21	LX240T,LX365T,SX315T
38	IO_L10N_MRCC_38	M21	LX240T,LX365T,SX315T
38	IO_L11P_SRCC_38	A26	LX240T,LX365T,SX315T
38	IO_L11N_SRCC_38	A25	LX240T,LX365T,SX315T
38	IO_L12P_VRN_38	L24	LX240T,LX365T,SX315T
38	IO_L12N_VRP_38	K24	LX240T,LX365T,SX315T
38	IO_L13P_38	C26	LX240T,LX365T,SX315T
38	IO_L13N_38	D26	LX240T,LX365T,SX315T
38	IO_L14P_38	M22	LX240T,LX365T,SX315T

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
38	IO_L14N_VREF_38	M23	LX240T,LX365T,SX315T
38	IO_L15P_38	B26	LX240T,LX365T,SX315T
38	IO_L15N_38	C25	LX240T,LX365T,SX315T
38	IO_L16P_38	N23	LX240T,LX365T,SX315T
38	IO_L16N_38	M24	LX240T,LX365T,SX315T
38	IO_L17P_38	D25	LX240T,LX365T,SX315T
38	IO_L17N_38	E25	LX240T,LX365T,SX315T
38	IO_L18P_38	P21	LX240T,LX365T,SX315T
38	IO_L18N_38	P22	LX240T,LX365T,SX315T
38	IO_L19P_38	P20	LX240T,LX365T,SX315T
38	IO_L19N_38	N20	LX240T,LX365T,SX315T
110	MGTTXN3_110	AW2	LX240T,LX365T,SX315T
110	MGTRXN3_110	AW6	LX240T,LX365T,SX315T
110	MGTTXP3_110	AW1	LX240T,LX365T,SX315T
110	MGTRXP3_110	AW5	LX240T,LX365T,SX315T
110	MGTTXN2_110	AY4	LX240T,LX365T,SX315T
110	MGTRXN2_110	AY8	LX240T,LX365T,SX315T
110	MGTTXP2_110	AY3	LX240T,LX365T,SX315T
110	MGTREFCLK1P_110	AW10	LX240T,LX365T,SX315T
110	MGTREFCLK1N_110	AW9	LX240T,LX365T,SX315T
110	MGTRXP2_110	AY7	LX240T,LX365T,SX315T
110	MGTREFCLK0P_110	BA10	LX240T,LX365T,SX315T
110	MGTREFCLK0N_110	BA9	LX240T,LX365T,SX315T
110	MGTTXN1_110	BA2	LX240T,LX365T,SX315T
110	MGTRXN1_110	BA6	LX240T,LX365T,SX315T
110	MGTTXP1_110	BA1	LX240T,LX365T,SX315T
110	MGTRXP1_110	BA5	LX240T,LX365T,SX315T
110	MGTTXN0_110	BB4	LX240T,LX365T,SX315T
110	MGTRXN0_110	BB8	LX240T,LX365T,SX315T
110	MGTTXP0_110	BB3	LX240T,LX365T,SX315T
110	MGTRXP0_110	BB7	LX240T,LX365T,SX315T
111	MGTTXN3_111	AR2	LX240T,LX365T,SX315T
111	MGTRXN3_111	AP8	LX240T,LX365T,SX315T

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
111	MGTTXP3_111	AR1	LX240T,LX365T,SX315T
111	MGTRXP3_111	AP7	LX240T,LX365T,SX315T
111	MGTTXN2_111	AT4	LX240T,LX365T,SX315T
111	MGTRXN2_111	AR6	LX240T,LX365T,SX315T
111	MGTTXP2_111	AT3	LX240T,LX365T,SX315T
111	MGTREFCLK1P_111	AT8	LX240T,LX365T,SX315T
111	MGTREFCLK1N_111	AT7	LX240T,LX365T,SX315T
111	MGTRXP2_111	AR5	LX240T,LX365T,SX315T
111	MGTREFCLK0P_111	AU10	LX240T,LX365T,SX315T
111	MGTREFCLK0N_111	AU9	LX240T,LX365T,SX315T
111	MGTTXN1_111	AU2	LX240T,LX365T,SX315T
111	MGTRXN1_111	AU6	LX240T,LX365T,SX315T
111	MGTTXP1_111	AU1	LX240T,LX365T,SX315T
111	MGTRXP1_111	AU5	LX240T,LX365T,SX315T
111	MGTTXN0_111	AV4	LX240T,LX365T,SX315T
111	MGTRXN0_111	AV8	LX240T,LX365T,SX315T
111	MGTTXP0_111	AV3	LX240T,LX365T,SX315T
111	MGTRXP0_111	AV7	LX240T,LX365T,SX315T
112	MGTTXN3_112	AL2	
112	MGTRXN3_112	AJ6	
112	MGTTXP3_112	AL1	
112	MGTRXP3_112	AJ5	
112	MGTTXN2_112	AM4	
112	MGTRXN2_112	AL6	
112	MGTTXP2_112	AM3	
112	MGTREFCLK1P_112	AH8	
112	MGTREFCLK1N_112	AH7	
112	MGTRXP2_112	AL5	
112	MGTREFCLK0P_112	AK8	
112	MGTREFCLK0N_112	AK7	
112	MGTTXN1_112	AN2	
112	MGTRXN1_112	AM8	
112	MGTTXP1_112	AN1	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
112	MGTRXP1_112	AM7	
112	MGTTXN0_112	AP4	
112	MGTRXN0_112	AN6	
112	MGTTXP0_112	AP3	
112	MGTRXP0_112	AN5	
113	MGTTXN3_113	AG2	
113	MGTRXN3_113	AD4	
113	MGTTXP3_113	AG1	
113	MGTRXP3_113	AD3	
113	MGTTXN2_113	AH4	
113	MGTRXN2_113	AE6	
113	MGTTXP2_113	AH3	
113	MGTREFCLK1P_113	AD8	
113	MGTREFCLK1N_113	AD7	
113	MGTRXP2_113	AE5	
113	MGTREFCLK0P_113	AF8	
113	MGTREFCLK0N_113	AF7	
113	MGTTXN1_113	AJ2	
113	MGTRXN1_113	AF4	
113	MGTTXP1_113	AJ1	
113	MGTRXP1_113	AF3	
113	MGTTXN0_113	AK4	
113	MGTRXN0_113	AG6	
113	MGTTXP0_113	AK3	
113	MGTRXP0_113	AG5	
114	MGTTXN3_114	W2	
114	MGTRXN3_114	Y4	
114	MGTTXP3_114	W1	
114	MGTRXP3_114	Y3	
114	MGTTXN2_114	AA2	
114	MGTRXN2_114	AA6	
114	MGTTXP2_114	AA1	
114	MGTREFCLK1P_114	Y8	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
114	MGTREFCLK1N_114	Y7	
114	MGTRXP2_114	AA5	
114	MGTREFCLK0P_114	AB8	
114	MGTREFCLK0N_114	AB7	
114	MGTTXN1_114	AC2	
114	MGTRXN1_114	AB4	
114	MGTTXP1_114	AC1	
114	MGTRXP1_114	AB3	
114	MGTTXN0_114	AE2	
114	MGTRXN0_114	AC6	
114	MGTTXP0_114	AE1	
114	MGTRXP0_114	AC5	
115	MGTTXN3_115	P4	
115	MGTRXN3_115	R6	
115	MGTTXP3_115	P3	
115	MGTRXP3_115	R5	
115	MGTTXN2_115	R2	
115	MGTRXN2_115	U6	
115	MGTTXP2_115	R1	
115	MGTREFCLK1P_115	T8	
115	MGTREFCLK1N_115	T7	
115	MGTRXP2_115	U5	
115	MGTAVTTRCAL_115	A12	
115	MGTRREF_115	B11	
115	MGTREFCLK0P_115	V8	
115	MGTREFCLK0N_115	V7	
115	MGTTXN1_115	T4	
115	MGTRXN1_115	V4	
115	MGTTXP1_115	T3	
115	MGTRXP1_115	V3	
115	MGTTXN0_115	U2	
115	MGTRXN0_115	W6	
115	MGTTXP0_115	U1	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
115	MGTRXP0_115	W5	
116	MGTTXN3_116	K4	
116	MGTRXN3_116	J6	
116	MGTTXP3_116	K3	
116	MGTRXP3_116	J5	
116	MGTTXN2_116	L2	
116	MGTRXN2_116	L6	
116	MGTTXP2_116	L1	
116	MGTREFCLK1P_116	K8	
116	MGTREFCLK1N_116	K7	
116	MGTRXP2_116	L5	
116	MGTREFCLK0P_116	M8	
116	MGTREFCLK0N_116	M7	
116	MGTTXN1_116	M4	
116	MGTRXN1_116	N6	
116	MGTTXP1_116	M3	
116	MGTRXP1_116	N5	
116	MGTTXN0_116	N2	
116	MGTRXN0_116	P8	
116	MGTTXP0_116	N1	
116	MGTRXP0_116	P7	
117	MGTTXN3_117	F4	
117	MGTRXN3_117	E6	
117	MGTTXP3_117	F3	
117	MGTRXP3_117	E5	
117	MGTTXN2_117	G2	
117	MGTRXN2_117	F8	
117	MGTTXP2_117	G1	
117	MGTREFCLK1P_117	E10	
117	MGTREFCLK1N_117	E9	
117	MGTRXP2_117	F7	
117	MGTREFCLK0P_117	G10	
117	MGTREFCLK0N_117	G9	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
117	MGTTXN1_117	H4	
117	MGTRXN1_117	G6	
117	MGTTXP1_117	H3	
117	MGTRXP1_117	G5	
117	MGTTXN0_117	J2	
117	MGTRXN0_117	H8	
117	MGTTXP0_117	J1	
117	MGTRXP0_117	H7	
118	MGTTXN3_118	B4	LX240T,LX365T,SX315T
118	MGTRXN3_118	A6	LX240T,LX365T,SX315T
118	MGTTXP3_118	B3	LX240T,LX365T,SX315T
118	MGTRXP3_118	A5	LX240T,LX365T,SX315T
118	MGTTXN2_118	C2	LX240T,LX365T,SX315T
118	MGTRXN2_118	B8	LX240T,LX365T,SX315T
118	MGTTXP2_118	C1	LX240T,LX365T,SX315T
118	MGTREFCLK1P_118	A10	LX240T,LX365T,SX315T
118	MGTREFCLK1N_118	A9	LX240T,LX365T,SX315T
118	MGTRXP2_118	B7	LX240T,LX365T,SX315T
118	MGTREFCLK0P_118	C10	LX240T,LX365T,SX315T
118	MGTREFCLK0N_118	C9	LX240T,LX365T,SX315T
118	MGTTXN1_118	D4	LX240T,LX365T,SX315T
118	MGTRXN1_118	C6	LX240T,LX365T,SX315T
118	MGTTXP1_118	D3	LX240T,LX365T,SX315T
118	MGTRXP1_118	C5	LX240T,LX365T,SX315T
118	MGTTXN0_118	E2	LX240T,LX365T,SX315T
118	MGTRXN0_118	D8	LX240T,LX365T,SX315T
118	MGTTXP0_118	E1	LX240T,LX365T,SX315T
118	MGTRXP0_118	D7	LX240T,LX365T,SX315T
NA	GND	A2	
NA	GND	A3	
NA	GND	A4	
NA	GND	A7	
NA	GND	A8	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	A11	
NA	GND	A13	
NA	GND	A18	
NA	GND	A28	
NA	GND	A38	
NA	GND	AA3	
NA	GND	AA7	
NA	GND	AA9	
NA	GND	AA11	
NA	GND	AA13	
NA	GND	AA15	
NA	GND	AA17	
NA	GND	AA19	
NA	GND	AA23	
NA	GND	AA25	
NA	GND	AA27	
NA	GND	AA29	
NA	GND	AA38	
NA	GND	AB1	
NA	GND	AB2	
NA	GND	AB5	
NA	GND	AB6	
NA	GND	AB9	
NA	GND	AB10	
NA	GND	AB12	
NA	GND	AB14	
NA	GND	AB16	
NA	GND	AB18	
NA	GND	AB20	
NA	GND	AB24	
NA	GND	AB26	
NA	GND	AB28	
NA	GND	AB35	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AC3	
NA	GND	AC7	
NA	GND	AC9	
NA	GND	AC11	
NA	GND	AC13	
NA	GND	AC15	
NA	GND	AC17	
NA	GND	AC19	
NA	GND	AC23	
NA	GND	AC25	
NA	GND	AC27	
NA	GND	AC29	
NA	GND	AC32	
NA	GND	AC42	
NA	GND	AD1	
NA	GND	AD2	
NA	GND	AD5	
NA	GND	AD6	
NA	GND	AD9	
NA	GND	AD10	
NA	GND	AD12	
NA	GND	AD14	
NA	GND	AD16	
NA	GND	AD18	
NA	GND	AD20	
NA	GND	AD22	
NA	GND	AD24	
NA	GND	AD26	
NA	GND	AD28	
NA	GND	AD39	
NA	GND	AE3	
NA	GND	AE7	
NA	GND	AE9	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AE11	
NA	GND	AE13	
NA	GND	AE15	
NA	GND	AE17	
NA	GND	AE19	
NA	GND	AE21	
NA	GND	AE23	
NA	GND	AE25	
NA	GND	AE27	
NA	GND	AE29	
NA	GND	AE36	
NA	GND	AF1	
NA	GND	AF2	
NA	GND	AF5	
NA	GND	AF6	
NA	GND	AF9	
NA	GND	AF10	
NA	GND	AF11	
NA	GND	AF12	
NA	GND	AF14	
NA	GND	AF16	
NA	GND	AF18	
NA	GND	AF20	
NA	GND	AF22	
NA	GND	AF24	
NA	GND	AF26	
NA	GND	AF28	
NA	GND	AF33	
NA	GND	AG3	
NA	GND	AG4	
NA	GND	AG7	
NA	GND	AG8	
NA	GND	AG9	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AG10	
NA	GND	AG11	
NA	GND	AG13	
NA	GND	AG15	
NA	GND	AG17	
NA	GND	AG19	
NA	GND	AG21	
NA	GND	AG23	
NA	GND	AG30	
NA	GND	AG40	
NA	GND	AH1	
NA	GND	AH2	
NA	GND	AH5	
NA	GND	AH6	
NA	GND	AH9	
NA	GND	AH11	
NA	GND	AH12	
NA	GND	AH14	
NA	GND	AH16	
NA	GND	AH17	
NA	GND	AH18	
NA	GND	AH20	
NA	GND	AH27	
NA	GND	AH37	
NA	GND	AJ3	
NA	GND	AJ7	
NA	GND	AJ9	
NA	GND	AJ11	
NA	GND	AJ12	
NA	GND	AJ13	
NA	GND	AJ14	
NA	GND	AJ24	
NA	GND	AJ34	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AK1	
NA	GND	AK2	
NA	GND	AK5	
NA	GND	AK6	
NA	GND	AK9	
NA	GND	AK11	
NA	GND	AK12	
NA	GND	AK13	
NA	GND	AK21	
NA	GND	AK31	
NA	GND	AK41	
NA	GND	AL3	
NA	GND	AL7	
NA	GND	AL9	
NA	GND	AL12	
NA	GND	AL18	
NA	GND	AL28	
NA	GND	AL38	
NA	GND	AM1	
NA	GND	AM2	
NA	GND	AM5	
NA	GND	AM9	
NA	GND	AM10	
NA	GND	AM15	
NA	GND	AM25	
NA	GND	AM35	
NA	GND	AN3	
NA	GND	AN7	
NA	GND	AN9	
NA	GND	AN12	
NA	GND	AN22	
NA	GND	AN32	
NA	GND	AN42	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AP1	
NA	GND	AP2	
NA	GND	AP5	
NA	GND	AP9	
NA	GND	AP19	
NA	GND	AP29	
NA	GND	AP39	
NA	GND	AR3	
NA	GND	AR7	
NA	GND	AR9	
NA	GND	AR16	
NA	GND	AR26	
NA	GND	AR36	
NA	GND	AT1	
NA	GND	AT2	
NA	GND	AT5	
NA	GND	AT6	
NA	GND	AT9	
NA	GND	AT10	
NA	GND	AT11	
NA	GND	AT13	
NA	GND	AT23	
NA	GND	AT33	
NA	GND	AU3	
NA	GND	AU7	
NA	GND	AU11	
NA	GND	AU20	
NA	GND	AU30	
NA	GND	AU40	
NA	GND	AV1	
NA	GND	AV2	
NA	GND	AV5	
NA	GND	AV9	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AV10	
NA	GND	AV11	
NA	GND	AV17	
NA	GND	AV27	
NA	GND	AV37	
NA	GND	AW3	
NA	GND	AW7	
NA	GND	AW11	
NA	GND	AW14	
NA	GND	AW24	
NA	GND	AW34	
NA	GND	AY1	
NA	GND	AY2	
NA	GND	AY5	
NA	GND	AY9	
NA	GND	AY10	
NA	GND	AY11	
NA	GND	AY12	
NA	GND	AY21	
NA	GND	AY31	
NA	GND	AY41	
NA	GND	B1	
NA	GND	B2	
NA	GND	B5	
NA	GND	B9	
NA	GND	B10	
NA	GND	B12	
NA	GND	B13	
NA	GND	B15	
NA	GND	B25	
NA	GND	B35	
NA	GND	BA3	
NA	GND	BA7	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	BA11	
NA	GND	BA12	
NA	GND	BA18	
NA	GND	BA28	
NA	GND	BA38	
NA	GND	BB2	
NA	GND	BB5	
NA	GND	BB6	
NA	GND	BB9	
NA	GND	BB10	
NA	GND	BB11	
NA	GND	BB12	
NA	GND	BB15	
NA	GND	BB25	
NA	GND	BB35	
NA	GND	C3	
NA	GND	C7	
NA	GND	C11	
NA	GND	C12	
NA	GND	C22	
NA	GND	C32	
NA	GND	C42	
NA	GND	D1	
NA	GND	D2	
NA	GND	D5	
NA	GND	D9	
NA	GND	D10	
NA	GND	D11	
NA	GND	D19	
NA	GND	D29	
NA	GND	D39	
NA	GND	E3	
NA	GND	E7	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	E11	
NA	GND	E16	
NA	GND	E26	
NA	GND	E36	
NA	GND	F1	
NA	GND	F2	
NA	GND	F5	
NA	GND	F9	
NA	GND	F10	
NA	GND	F11	
NA	GND	F13	
NA	GND	F23	
NA	GND	F33	
NA	GND	G3	
NA	GND	G7	
NA	GND	G11	
NA	GND	G20	
NA	GND	G30	
NA	GND	G40	
NA	GND	H1	
NA	GND	H2	
NA	GND	H5	
NA	GND	H9	
NA	GND	H10	
NA	GND	H11	
NA	GND	H17	
NA	GND	H27	
NA	GND	H37	
NA	GND	J3	
NA	GND	J7	
NA	GND	J9	
NA	GND	J14	
NA	GND	J24	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	J34	
NA	GND	K1	
NA	GND	K2	
NA	GND	K5	
NA	GND	K6	
NA	GND	K9	
NA	GND	K11	
NA	GND	K21	
NA	GND	K31	
NA	GND	K41	
NA	GND	L3	
NA	GND	L7	
NA	GND	L9	
NA	GND	L18	
NA	GND	L28	
NA	GND	L38	
NA	GND	M1	
NA	GND	M2	
NA	GND	M5	
NA	GND	M6	
NA	GND	M9	
NA	GND	M15	
NA	GND	M25	
NA	GND	M35	
NA	GND	N3	
NA	GND	N7	
NA	GND	N9	
NA	GND	N12	
NA	GND	N22	
NA	GND	N32	
NA	GND	N42	
NA	GND	P1	
NA	GND	P2	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	P5	
NA	GND	P9	
NA	GND	P11	
NA	GND	P12	
NA	GND	P19	
NA	GND	P29	
NA	GND	P39	
NA	GND	R3	
NA	GND	R7	
NA	GND	R9	
NA	GND	R13	
NA	GND	R15	
NA	GND	R16	
NA	GND	R17	
NA	GND	R19	
NA	GND	R26	
NA	GND	R36	
NA	GND	T1	
NA	GND	T2	
NA	GND	T5	
NA	GND	T6	
NA	GND	T9	
NA	GND	T11	
NA	GND	T12	
NA	GND	T14	
NA	GND	T16	
NA	GND	T18	
NA	GND	T20	
NA	GND	T22	
NA	GND	T24	
NA	GND	T26	
NA	GND	T33	
NA	GND	U3	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	U4	
NA	GND	U7	
NA	GND	U8	
NA	GND	U9	
NA	GND	U10	
NA	GND	U11	
NA	GND	U13	
NA	GND	U15	
NA	GND	U17	
NA	GND	U19	
NA	GND	U21	
NA	GND	U23	
NA	GND	U25	
NA	GND	U27	
NA	GND	U29	
NA	GND	U30	
NA	GND	U40	
NA	GND	V1	
NA	GND	V2	
NA	GND	V5	
NA	GND	V6	
NA	GND	V9	
NA	GND	V10	
NA	GND	V12	
NA	GND	V14	
NA	GND	V16	
NA	GND	V18	
NA	GND	V20	
NA	GND	V22	
NA	GND	V24	
NA	GND	V26	
NA	GND	V28	
NA	GND	V37	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	W3	
NA	GND	W7	
NA	GND	W9	
NA	GND	W11	
NA	GND	W13	
NA	GND	W15	
NA	GND	W17	
NA	GND	W19	
NA	GND	W21	
NA	GND	W23	
NA	GND	W25	
NA	GND	W27	
NA	GND	W34	
NA	GND	Y1	
NA	GND	Y2	
NA	GND	Y5	
NA	GND	Y6	
NA	GND	Y9	
NA	GND	Y10	
NA	GND	Y12	
NA	GND	Y14	
NA	GND	Y16	
NA	GND	Y18	
NA	GND	Y20	
NA	GND	Y24	
NA	GND	Y26	
NA	GND	Y28	
NA	GND	Y31	
NA	GND	Y41	
NA	GND	AJ10	
NA	VCCAUX	AA10	
NA	VCCAUX	AA28	
NA	VCCAUX	AB11	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCAUX	AB29	
NA	VCCAUX	AC10	
NA	VCCAUX	AC28	
NA	VCCAUX	AD11	
NA	VCCAUX	AD29	
NA	VCCAUX	AE10	
NA	VCCAUX	AE28	
NA	VCCAUX	AF27	
NA	VCCAUX	AF29	
NA	VCCAUX	T29	
NA	VCCAUX	U28	
NA	VCCAUX	V11	
NA	VCCAUX	V29	
NA	VCCAUX	W10	
NA	VCCAUX	W28	
NA	VCCAUX	Y11	
NA	VCCAUX	Y29	
NA	VCCINT	AA12	
NA	VCCINT	AA14	
NA	VCCINT	AA16	
NA	VCCINT	AA18	
NA	VCCINT	AA20	
NA	VCCINT	AA24	
NA	VCCINT	AA26	
NA	VCCINT	AB13	
NA	VCCINT	AB15	
NA	VCCINT	AB17	
NA	VCCINT	AB19	
NA	VCCINT	AB23	
NA	VCCINT	AB25	
NA	VCCINT	AB27	
NA	VCCINT	AC12	
NA	VCCINT	AC14	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	AC16	
NA	VCCINT	AC18	
NA	VCCINT	AC20	
NA	VCCINT	AC24	
NA	VCCINT	AC26	
NA	VCCINT	AD13	
NA	VCCINT	AD15	
NA	VCCINT	AD17	
NA	VCCINT	AD19	
NA	VCCINT	AD21	
NA	VCCINT	AD23	
NA	VCCINT	AD25	
NA	VCCINT	AD27	
NA	VCCINT	AE12	
NA	VCCINT	AE14	
NA	VCCINT	AE16	
NA	VCCINT	AE18	
NA	VCCINT	AE20	
NA	VCCINT	AE22	
NA	VCCINT	AE24	
NA	VCCINT	AE26	
NA	VCCINT	AF13	
NA	VCCINT	AF15	
NA	VCCINT	AF17	
NA	VCCINT	AF19	
NA	VCCINT	AF21	
NA	VCCINT	AF23	
NA	VCCINT	AF25	
NA	VCCINT	AG12	
NA	VCCINT	AG14	
NA	VCCINT	AG16	
NA	VCCINT	AG18	
NA	VCCINT	AG20	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	AG22	
NA	VCCINT	AG24	
NA	VCCINT	AG26	
NA	VCCINT	AH13	
NA	VCCINT	AH15	
NA	VCCINT	AH19	
NA	VCCINT	AH21	
NA	VCCINT	AH23	
NA	VCCINT	P13	
NA	VCCINT	P15	
NA	VCCINT	R12	
NA	VCCINT	R14	
NA	VCCINT	R18	
NA	VCCINT	R20	
NA	VCCINT	R22	
NA	VCCINT	R24	
NA	VCCINT	T13	
NA	VCCINT	T15	
NA	VCCINT	T17	
NA	VCCINT	T19	
NA	VCCINT	T21	
NA	VCCINT	T23	
NA	VCCINT	T25	
NA	VCCINT	T27	
NA	VCCINT	U12	
NA	VCCINT	U14	
NA	VCCINT	U16	
NA	VCCINT	U18	
NA	VCCINT	U20	
NA	VCCINT	U22	
NA	VCCINT	U24	
NA	VCCINT	U26	
NA	VCCINT	V13	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	V15	
NA	VCCINT	V17	
NA	VCCINT	V19	
NA	VCCINT	V21	
NA	VCCINT	V23	
NA	VCCINT	V25	
NA	VCCINT	V27	
NA	VCCINT	W12	
NA	VCCINT	W14	
NA	VCCINT	W16	
NA	VCCINT	W18	
NA	VCCINT	W20	
NA	VCCINT	W22	
NA	VCCINT	W24	
NA	VCCINT	W26	
NA	VCCINT	Y13	
NA	VCCINT	Y15	
NA	VCCINT	Y17	
NA	VCCINT	Y19	
NA	VCCINT	Y23	
NA	VCCINT	Y25	
NA	VCCINT	Y27	
0	VCCO_0	M10	
0	VCCO_0	R11	
12	VCCO_12	AP34	
12	VCCO_12	AT38	
12	VCCO_12	AU35	
12	VCCO_12	AW39	
12	VCCO_12	AY36	
13	VCCO_13	AK36	
13	VCCO_13	AN37	
13	VCCO_13	AR41	
13	VCCO_13	AV42	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
13	VCCO_13	BB40	
14	VCCO_14	AF38	
14	VCCO_14	AG35	
14	VCCO_14	AH42	
14	VCCO_14	AJ39	
14	VCCO_14	AM40	
15	VCCO_15	AA33	
15	VCCO_15	AB40	
15	VCCO_15	AC37	
15	VCCO_15	AD34	
15	VCCO_15	AE41	
16	VCCO_16	U35	
16	VCCO_16	V32	
16	VCCO_16	V42	
16	VCCO_16	W39	
16	VCCO_16	Y36	
17	VCCO_17	M40	
17	VCCO_17	N37	
17	VCCO_17	P34	
17	VCCO_17	R41	
17	VCCO_17	T38	
21	VCCO_21	AH22	
21	VCCO_21	AL23	
21	VCCO_21	AP24	
21	VCCO_21	AU25	
21	VCCO_21	AY26	
22	VCCO_22	AN27	
22	VCCO_22	AT28	
22	VCCO_22	AW29	
22	VCCO_22	BA33	
22	VCCO_22	BB30	
23	VCCO_23	AG25	
23	VCCO_23	AK26	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
23	VCCO_23	AL33	
23	VCCO_23	AM30	
23	VCCO_23	AR31	
23	VCCO_23	AV32	
24	VCCO_24	AB30	
24	VCCO_24	AE31	
24	VCCO_24	AH32	
24	VCCO_24	AJ29	
24	VCCO_24	R31	
24	VCCO_24	W29	
25	VCCO_25	H42	
25	VCCO_25	J39	
25	VCCO_25	K36	
25	VCCO_25	L33	
25	VCCO_25	M30	
25	VCCO_25	T28	
26	VCCO_26	B40	
26	VCCO_26	C37	
26	VCCO_26	E41	
26	VCCO_26	F38	
26	VCCO_26	G35	
27	VCCO_27	A33	
27	VCCO_27	D34	
27	VCCO_27	E31	
27	VCCO_27	H32	
27	VCCO_27	J29	
28	VCCO_28	B30	
28	VCCO_28	F28	
28	VCCO_28	K26	
28	VCCO_28	N27	
28	VCCO_28	P24	
32	VCCO_32	AJ19	
32	VCCO_32	AM20	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
32	VCCO_32	AR21	
32	VCCO_32	AV22	
32	VCCO_32	BA23	
33	VCCO_33	AK16	
33	VCCO_33	AL13	
33	VCCO_33	AN17	
33	VCCO_33	AT18	
33	VCCO_33	AW19	
33	VCCO_33	BB20	
34	VCCO_34	AP14	
34	VCCO_34	AR11	
34	VCCO_34	AU15	
34	VCCO_34	AV12	
34	VCCO_34	AY16	
34	VCCO_34	BA13	
35	VCCO_35	C17	
35	VCCO_35	D14	
35	VCCO_35	G15	
35	VCCO_35	H12	
35	VCCO_35	L13	
36	VCCO_36	B20	
36	VCCO_36	F18	
36	VCCO_36	K16	
36	VCCO_36	N17	
36	VCCO_36	P14	
37	VCCO_37	A23	
37	VCCO_37	D24	
37	VCCO_37	E21	
37	VCCO_37	H22	
37	VCCO_37	J19	
38	VCCO_38	C27	
38	VCCO_38	G25	
38	VCCO_38	L23	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
38	VCCO_38	M20	
38	VCCO_38	R21	
NA	MGTAVCC_N	AA8	
NA	MGTAVCC_N	C8	
NA	MGTAVCC_N	E8	
NA	MGTAVCC_N	G8	
NA	MGTAVCC_N	J8	
NA	MGTAVCC_N	L8	
NA	MGTAVCC_N	N8	
NA	MGTAVCC_N	R8	
NA	MGTAVCC_N	W8	
NA	MGTAVCC_S	AC8	
NA	MGTAVCC_S	AE8	
NA	MGTAVCC_S	AJ8	
NA	MGTAVCC_S	AL8	
NA	MGTAVCC_S	AN8	
NA	MGTAVCC_S	AR8	
NA	MGTAVCC_S	AU8	
NA	MGTAVCC_S	AW8	
NA	MGTAVCC_S	BA8	
NA	MGTAVTT_N	B6	
NA	MGTAVTT_N	C4	
NA	MGTAVTT_N	D6	
NA	MGTAVTT_N	E4	
NA	MGTAVTT_N	F6	
NA	MGTAVTT_N	G4	
NA	MGTAVTT_N	H6	
NA	MGTAVTT_N	J4	
NA	MGTAVTT_N	L4	
NA	MGTAVTT_N	N4	
NA	MGTAVTT_N	P6	
NA	MGTAVTT_N	R4	
NA	MGTAVTT_N	W4	

Table 2-6: FF1759/RF1759 Package—LX240T, LX365T, LX550T, SX315T, SX475T

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTAVTT_S	AA4	
NA	MGTAVTT_S	AC4	
NA	MGTAVTT_S	AE4	
NA	MGTAVTT_S	AJ4	
NA	MGTAVTT_S	AL4	
NA	MGTAVTT_S	AM6	
NA	MGTAVTT_S	AN4	
NA	MGTAVTT_S	AP6	
NA	MGTAVTT_S	AR4	
NA	MGTAVTT_S	AU4	
NA	MGTAVTT_S	AV6	
NA	MGTAVTT_S	AW4	
NA	MGTAVTT_S	AY6	
NA	MGTAVTT_S	BA4	

FF1760 Package—LX550T and LX760

Table 2-7: FF1760 Package—LX550T and LX760

Bank	Pin Description	Pin Number	No Connect (NC)
0	INIT_B_0	R14	
0	DONE_0	T14	
0	M1_0	R29	
0	M2_0	T29	
0	HSWAPEN_0	T15	
0	PROGRAM_B_0	T30	
0	M0_0	R30	
0	AVSS_0	Y21	
0	AVDD_0	Y22	
0	VP_0	AA22	
0	VREFP_0	AB22	
0	VN_0	AB21	
0	VREFN_0	AA21	
0	DXP_0	AC22	
0	DXN_0	AC21	
0	VBATT_0	U14	
0	DIN_0	AF29	
0	RDWR_B_0	AD31	
0	CSI_B_0	AF30	
0	DOUT_BUSY_0	AH28	
0	CCLK_0	AF13	
0	TDO_0	AH13	
0	TCK_0	AH14	
0	TMS_0	AE12	
0	TDI_0	AF14	
0	VFS_0	AG29	
12	IO_L0P_12	AM39	
12	IO_L0N_12	AL39	
12	IO_L1P_12	AE33	
12	IO_L1N_12	AE32	
12	IO_L2P_12	AT40	

Table 2-7: FF1760 Package—LX550T and LX760 (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
12	IO_L2N_12	AR40	
12	IO_L3P_12	AR42	
12	IO_L3N_12	AP42	
12	IO_L4P_12	AF31	
12	IO_L4N_VREF_12	AF32	
12	IO_L5P_12	AK38	
12	IO_L5N_12	AJ37	
12	IO_L6P_12	AH33	
12	IO_L6N_12	AH34	
12	IO_L7P_12	AT42	
12	IO_L7N_12	AU42	
12	IO_L8P_SRCC_12	AK35	
12	IO_L8N_SRCC_12	AJ35	
12	IO_L9P_MRCC_12	AN41	
12	IO_L9N_MRCC_12	AM41	
12	IO_L10P_MRCC_12	AK37	
12	IO_L10N_MRCC_12	AJ36	
12	IO_L11P_SRCC_12	AP41	
12	IO_L11N_SRCC_12	AN40	
12	IO_L12P_VRN_12	AG32	
12	IO_L12N_VRP_12	AG31	
12	IO_L13P_12	AG34	
12	IO_L13N_12	AG33	
12	IO_L14P_12	AU41	
12	IO_L14N_VREF_12	AT41	
12	IO_L15P_12	AN39	
12	IO_L15N_12	AP40	
12	IO_L16P_12	AW42	
12	IO_L16N_12	AV41	
12	IO_L17P_12	AK39	
12	IO_L17N_12	AJ38	
12	IO_L18P_12	AV40	
12	IO_L18N_12	AW41	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
12	IO_L19P_12	AH36	
12	IO_L19N_12	AH35	
13	IO_L0P_13	AF39	
13	IO_L0N_13	AE39	
13	IO_L1P_13	AF42	
13	IO_L1N_13	AE42	
13	IO_L2P_13	AG38	
13	IO_L2N_13	AG39	
13	IO_L3P_13	AD40	
13	IO_L3N_13	AD41	
13	IO_L4P_13	AE34	
13	IO_L4N_VREF_13	AE35	
13	IO_L5P_13	AE37	
13	IO_L5N_13	AE38	
13	IO_L6P_13	AJ40	
13	IO_L6N_13	AH40	
13	IO_L7P_13	AG42	
13	IO_L7N_13	AF41	
13	IO_L8P_SRCC_13	AJ41	
13	IO_L8N_SRCC_13	AJ42	
13	IO_L9P_MRCC_13	AD36	
13	IO_L9N_MRCC_13	AD35	
13	IO_L10P_MRCC_13	AF36	
13	IO_L10N_MRCC_13	AF37	
13	IO_L11P_SRCC_13	AD37	
13	IO_L11N_SRCC_13	AD38	
13	IO_L12P_VRN_13	AL42	
13	IO_L12N_VRP_13	AK42	
13	IO_L13P_13	AH41	
13	IO_L13N_13	AG41	
13	IO_L14P_13	AL40	
13	IO_L14N_VREF_13	AK40	
13	IO_L15P_13	AH38	

Table 2-7: FF1760 Package—LX550T and LX760 (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
13	IO_L15N_13	AH39	
13	IO_L16P_13	AF34	
13	IO_L16N_13	AF35	
13	IO_L17P_13	AE40	
13	IO_L17N_13	AF40	
13	IO_L18P_13	AM42	
13	IO_L18N_13	AL41	
13	IO_L19P_13	AG36	
13	IO_L19N_13	AG37	
14	IO_L0P_14	Y38	
14	IO_L0N_14	Y37	
14	IO_L1P_14	Y35	
14	IO_L1N_14	Y34	
14	IO_L2P_14	AB34	
14	IO_L2N_14	AA34	
14	IO_L3P_14	V41	
14	IO_L3N_14	W40	
14	IO_L4P_14	AC36	
14	IO_L4N_VREF_14	AB36	
14	IO_L5P_14	AA39	
14	IO_L5N_14	Y39	
14	IO_L6P_14	AC38	
14	IO_L6N_14	AC39	
14	IO_L7P_14	W41	
14	IO_L7N_14	W42	
14	IO_L8P_SRCC_14	AC34	
14	IO_L8N_SRCC_14	AC35	
14	IO_L9P_MRCC_14	AA40	
14	IO_L9N_MRCC_14	Y40	
14	IO_L10P_MRCC_14	AB37	
14	IO_L10N_MRCC_14	AA37	
14	IO_L11P_SRCC_14	AA32	
14	IO_L11N_SRCC_14	AB33	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
14	IO_L12P_VRN_14	AB41	
14	IO_L12N_VRP_14	AC40	
14	IO_L13P_14	AA36	
14	IO_L13N_14	AA35	
14	IO_L14P_14	AB42	
14	IO_L14N_VREF_14	AA42	
14	IO_L15P_14	AB39	
14	IO_L15N_14	AB38	
14	IO_L16P_14	AC33	
14	IO_L16N_14	AB32	
14	IO_L17P_14	AA41	
14	IO_L17N_14	Y42	
14	IO_L18P_14	AD42	
14	IO_L18N_14	AC41	
14	IO_L19P_14	AD33	
14	IO_L19N_14	AD32	
15	IO_L0P_15	R39	
15	IO_L0N_15	R38	
15	IO_L1P_15	M42	
15	IO_L1N_15	M41	
15	IO_L2P_SM8P_15	V36	
15	IO_L2N_SM8N_15	U36	
15	IO_L3P_SM9P_15	U34	
15	IO_L3N_SM9N_15	V33	
15	IO_L4P_15	U39	
15	IO_L4N_VREF_15	V39	
15	IO_L5P_SM10P_15	U37	
15	IO_L5N_SM10N_15	T37	
15	IO_L6P_SM11P_15	W35	
15	IO_L6N_SM11N_15	W36	
15	IO_L7P_SM12P_15	R37	
15	IO_L7N_SM12N_15	T36	
15	IO_L8P_SRCC_15	T40	

Table 2-7: FF1760 Package—LX550T and LX760 (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
15	IO_L8N_SRCC_15	T39	
15	IO_L9P_MRCC_15	N41	
15	IO_L9N_MRCC_15	N40	
15	IO_L10P_MRCC_15	V38	
15	IO_L10N_MRCC_15	U38	
15	IO_L11P_SRCC_15	W32	
15	IO_L11N_SRCC_15	W33	
15	IO_L12P_SM13P_15	U41	
15	IO_L12N_SM13N_15	V40	
15	IO_L13P_SM14P_15	R40	
15	IO_L13N_SM14N_15	P40	
15	IO_L14P_15	R42	
15	IO_L14N_VREF_15	T41	
15	IO_L15P_SM15P_15	W38	
15	IO_L15N_SM15N_15	W37	
15	IO_L16P_VRN_15	U42	
15	IO_L16N_VRP_15	T42	
15	IO_L17P_15	P41	
15	IO_L17N_15	P42	
15	IO_L18P_15	Y32	
15	IO_L18N_15	Y33	
15	IO_L19P_15	V35	
15	IO_L19N_15	V34	
16	IO_L0P_16	K38	
16	IO_L0N_16	L37	
16	IO_L1P_16	R33	
16	IO_L1N_16	R32	
16	IO_L2P_16	T35	
16	IO_L2N_16	R35	
16	IO_L3P_16	M36	
16	IO_L3N_16	N35	
16	IO_L4P_16	M39	
16	IO_L4N_VREF_16	L39	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
16	IO_L5P_16	P36	
16	IO_L5N_16	N36	
16	IO_L6P_16	L40	
16	IO_L6N_16	K40	
16	IO_L7P_16	T31	
16	IO_L7N_16	T32	
16	IO_L8P_SRCC_16	U33	
16	IO_L8N_SRCC_16	T34	
16	IO_L9P_MRCC_16	J40	
16	IO_L9N_MRCC_16	K39	
16	IO_L10P_MRCC_16	M38	
16	IO_L10N_MRCC_16	M37	
16	IO_L11P_SRCC_16	H40	
16	IO_L11N_SRCC_16	G41	
16	IO_L12P_VRN_16	N39	
16	IO_L12N_VRP_16	N38	
16	IO_L13P_16	G42	
16	IO_L13N_16	F42	
16	IO_L14P_16	U31	
16	IO_L14N_VREF_16	U32	
16	IO_L15P_16	P38	
16	IO_L15N_16	P37	
16	IO_L16P_16	K42	
16	IO_L16N_16	J41	
16	IO_L17P_16	R34	
16	IO_L17N_16	P35	
16	IO_L18P_16	L42	
16	IO_L18N_16	L41	
16	IO_L19P_16	J42	
16	IO_L19N_16	H41	
17	IO_L0P_17	G37	
17	IO_L0N_17	H36	
17	IO_L1P_17	B39	

Table 2-7: FF1760 Package—LX550T and LX760 (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
17	IO_L1N_17	C39	
17	IO_L2P_17	F40	
17	IO_L2N_17	F39	
17	IO_L3P_17	A41	
17	IO_L3N_17	A40	
17	IO_L4P_17	H38	
17	IO_L4N_VREF_17	G38	
17	IO_L5P_17	E39	
17	IO_L5N_17	E38	
17	IO_L6P_17	L35	
17	IO_L6N_17	M34	
17	IO_L7P_17	B41	
17	IO_L7N_17	B42	
17	IO_L8P_SRCC_17	P33	
17	IO_L8N_SRCC_17	N34	
17	IO_L9P_MRCC_17	C41	
17	IO_L9N_MRCC_17	C40	
17	IO_L10P_MRCC_17	J38	
17	IO_L10N_MRCC_17	J37	
17	IO_L11P_SRCC_17	M33	
17	IO_L11N_SRCC_17	L34	
17	IO_L12P_VRN_17	H39	
17	IO_L12N_VRP_17	G39	
17	IO_L13P_17	N33	
17	IO_L13N_17	P32	
17	IO_L14P_17	D40	
17	IO_L14N_VREF_17	E40	
17	IO_L15P_17	K37	
17	IO_L15N_17	L36	
17	IO_L16P_17	D42	
17	IO_L16N_17	D41	
17	IO_L17P_17	K34	
17	IO_L17N_17	J35	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
17	IO_L18P_17	F41	
17	IO_L18N_17	E42	
17	IO_L19P_17	J36	
17	IO_L19N_17	K35	
20	IO_L0P_20	AV26	
20	IO_L0N_20	AV25	
20	IO_L1P_20	AY27	
20	IO_L1N_20	AW26	
20	IO_L2P_20	AR24	
20	IO_L2N_20	AT25	
20	IO_L3P_20	BA29	
20	IO_L3N_20	AY28	
20	IO_L4P_20	BA25	
20	IO_L4N_VREF_20	AY25	
20	IO_L5P_20	AV24	
20	IO_L5N_20	AW25	
20	IO_L6P_20	AW22	
20	IO_L6N_20	AW23	
20	IO_L7P_20	BB29	
20	IO_L7N_20	BB28	
20	IO_L8P_SRCC_20	BA24	
20	IO_L8N_SRCC_20	AY24	
20	IO_L9P_MRCC_20	AP25	
20	IO_L9N_MRCC_20	AR25	
20	IO_L10P_MRCC_20	AT22	
20	IO_L10N_MRCC_20	AU22	
20	IO_L11P_SRCC_20	AP23	
20	IO_L11N_SRCC_20	AR23	
20	IO_L12P_VRN_20	BA21	
20	IO_L12N_VRP_20	BB21	
20	IO_L13P_20	BB26	
20	IO_L13N_20	BA26	
20	IO_L14P_20	BB23	

Table 2-7: FF1760 Package—LX550T and LX760 (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
20	IO_L14N_VREF_20	BB24	
20	IO_L15P_20	AT24	
20	IO_L15N_20	AU24	
20	IO_L16P_20	AY22	
20	IO_L16N_20	AY23	
20	IO_L17P_20	BB27	
20	IO_L17N_20	BA27	
20	IO_L18P_20	BA22	
20	IO_L18N_20	BB22	
20	IO_L19P_20	AU23	
20	IO_L19N_20	AV23	
21	IO_L0P_21	AU29	
21	IO_L0N_21	AV29	
21	IO_L1P_21	BA32	
21	IO_L1N_21	AY32	
21	IO_L2P_21	AY30	
21	IO_L2N_21	AW30	
21	IO_L3P_21	BA31	
21	IO_L3N_21	BB32	
21	IO_L4P_21	AJ26	
21	IO_L4N_VREF_21	AH26	
21	IO_L5P_21	AU27	
21	IO_L5N_21	AU28	
21	IO_L6P_21	AW27	
21	IO_L6N_21	AV28	
21	IO_L7P_21	BB31	
21	IO_L7N_21	BA30	
21	IO_L8P_SRCC_21	AJ23	
21	IO_L8N_SRCC_21	AJ22	
21	IO_L9P_MRCC_21	AW28	
21	IO_L9N_MRCC_21	AY29	
21	IO_L10P_MRCC_21	AU26	
21	IO_L10N_MRCC_21	AT26	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
21	IO_L11P_SRCC_21	AT27	
21	IO_L11N_SRCC_21	AR27	
21	IO_L12P_VRN_21	AK25	
21	IO_L12N_VRP_21	AJ25	
21	IO_L13P_21	AP26	
21	IO_L13N_21	AP27	
21	IO_L14P_21	AN24	
21	IO_L14N_VREF_21	AN25	
21	IO_L15P_21	AL24	
21	IO_L15N_21	AM24	
21	IO_L16P_21	AK23	
21	IO_L16N_21	AK22	
21	IO_L17P_21	AN26	
21	IO_L17N_21	AM26	
21	IO_L18P_21	AM23	
21	IO_L18N_21	AN23	
21	IO_L19P_21	AK24	
21	IO_L19N_21	AL25	
22	IO_L0P_22	AJ28	
22	IO_L0N_22	AK28	
22	IO_L1P_22	BA34	
22	IO_L1N_22	BA35	
22	IO_L2P_22	AY35	
22	IO_L2N_22	AW35	
22	IO_L3P_22	BB33	
22	IO_L3N_22	BB34	
22	IO_L4P_22	AT32	
22	IO_L4N_VREF_22	AU33	
22	IO_L5P_22	AV34	
22	IO_L5N_22	AU34	
22	IO_L6P_22	AV33	
22	IO_L6N_22	AU32	
22	IO_L7P_22	AP31	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
22	IO_L7N_22	AP30	
22	IO_L8P_SRCC_22	AY33	
22	IO_L8N_SRCC_22	AY34	
22	IO_L9P_MRCC_22	AR30	
22	IO_L9N_MRCC_22	AT31	
22	IO_L10P_MRCC_22	AW32	
22	IO_L10N_MRCC_22	AW33	
22	IO_L11P_SRCC_22	AT30	
22	IO_L11N_SRCC_22	AR29	
22	IO_L12P_VRN_22	AV30	
22	IO_L12N_VRP_22	AW31	
22	IO_L13P_22	AR28	
22	IO_L13N_22	AT29	
22	IO_L14P_22	AN28	
22	IO_L14N_VREF_22	AP28	
22	IO_L15P_22	AV31	
22	IO_L15N_22	AU31	
22	IO_L16P_22	AL27	
22	IO_L16N_22	AM28	
22	IO_L17P_22	AM29	
22	IO_L17N_22	AN29	
22	IO_L18P_22	AL26	
22	IO_L18N_22	AM27	
22	IO_L19P_22	AK27	
22	IO_L19N_22	AJ27	
23	IO_L0P_23	AU39	
23	IO_L0N_23	AV39	
23	IO_L1P_23	AY40	
23	IO_L1N_23	AW40	
23	IO_L2P_23	AY38	
23	IO_L2N_23	AW38	
23	IO_L3P_23	BA42	
23	IO_L3N_23	AY42	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
23	IO_L4P_23	BA37	
23	IO_L4N_VREF_23	AY37	
23	IO_L5P_23	AV38	
23	IO_L5N_23	AU38	
23	IO_L6P_23	AM31	
23	IO_L6N_23	AM32	
23	IO_L7P_23	BA41	
23	IO_L7N_23	BB41	
23	IO_L8P_SRCC_23	BB37	
23	IO_L8N_SRCC_23	BB38	
23	IO_L9P_MRCC_23	BA39	
23	IO_L9N_MRCC_23	AY39	
23	IO_L10P_MRCC_23	AU36	
23	IO_L10N_MRCC_23	AU37	
23	IO_L11P_SRCC_23	BA40	
23	IO_L11N_SRCC_23	BB39	
23	IO_L12P_VRN_23	BB36	
23	IO_L12N_VRP_23	BA36	
23	IO_L13P_23	AP33	
23	IO_L13N_23	AN33	
23	IO_L14P_23	AR33	
23	IO_L14N_VREF_23	AT34	
23	IO_L15P_23	AV36	
23	IO_L15N_23	AW37	
23	IO_L16P_23	AP32	
23	IO_L16N_23	AR32	
23	IO_L17P_23	AT35	
23	IO_L17N_23	AR34	
23	IO_L18P_23	AN30	
23	IO_L18N_23	AN31	
23	IO_L19P_23	AW36	
23	IO_L19N_23	AV35	
24	IO_L0P_GC_24	AL36	

Table 2-7: FF1760 Package—LX550T and LX760 (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
24	IO_L0N_GC_24	AL37	
24	IO_L1P_GC_24	AR38	
24	IO_L1N_GC_24	AP38	
24	IO_L2P_D15_24	AJ32	
24	IO_L2N_D14_24	AH31	
24	IO_L3P_D13_24	AT39	
24	IO_L3N_D12_24	AR39	
24	IO_L4P_D11_24	AK34	
24	IO_L4N_VREF_D10_24	AJ33	
24	IO_L5P_D9_24	AM36	
24	IO_L5N_D8_24	AM37	
24	IO_L6P_D7_24	AN38	
24	IO_L6N_D6_24	AM38	
24	IO_L7P_D5_24	AL35	
24	IO_L7N_D4_24	AL34	
24	IO_L8P_SRCC_24	AR35	
24	IO_L8N_SRCC_24	AT36	
24	IO_L9P_MRCC_24	AT37	
24	IO_L9N_MRCC_24	AR37	
24	IO_L10P_MRCC_24	AP37	
24	IO_L10N_MRCC_24	AN36	
24	IO_L11P_SRCC_24	AJ31	
24	IO_L11N_SRCC_24	AH30	
24	IO_L12P_D3_24	AN34	
24	IO_L12N_D2_FS2_24	AN35	
24	IO_L13P_D1_FS1_24	AM33	
24	IO_L13N_D0_FS0_24	AM34	
24	IO_L14P_FCS_B_24	AL31	
24	IO_L14N_VREF_FOE_B_MOSI_24	AL32	
24	IO_L15P_FWE_B_24	AP35	
24	IO_L15N_RS1_24	AP36	
24	IO_L16P_RS0_24	AK30	
24	IO_L16N_CS0_B_24	AL30	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
24	IO_L17P_VRN_24	AK33	
24	IO_L17N_VRP_24	AK32	
24	IO_L18P_24	AH29	
24	IO_L18N_24	AJ30	
24	IO_L19P_24	AL29	
24	IO_L19N_24	AK29	
25	IO_L0P_25	F34	
25	IO_L0N_25	F35	
25	IO_L1P_25	R28	
25	IO_L1N_25	P28	
25	IO_L2P_25	P30	
25	IO_L2N_25	N29	
25	IO_L3P_25	M29	
25	IO_L3N_25	N28	
25	IO_L4P_25	L31	
25	IO_L4N_VREF_25	L30	
25	IO_L5P_25	D38	
25	IO_L5N_25	C38	
25	IO_L6P_25	H35	
25	IO_L6N_25	H34	
25	IO_L7P_25	A36	
25	IO_L7N_25	B36	
25	IO_L8P_SRCC_25	K32	
25	IO_L8N_SRCC_25	J32	
25	IO_L9P_MRCC_25	B37	
25	IO_L9N_MRCC_25	A37	
25	IO_L10P_MRCC_25	G36	
25	IO_L10N_MRCC_25	F36	
25	IO_L11P_SRCC_25	C36	
25	IO_L11N_SRCC_25	D37	
25	IO_L12P_25	G34	
25	IO_L12N_25	H33	
25	IO_L13P_25	M31	

Table 2-7: FF1760 Package—LX550T and LX760 (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
25	IO_L13N_25	L32	
25	IO_L14P_25	K33	
25	IO_L14N_VREF_25	J33	
25	IO_L15P_25	F37	
25	IO_L15N_25	E37	
25	IO_L16P_VRN_25	D36	
25	IO_L16N_VRP_25	E35	
25	IO_L17P_25	N30	
25	IO_L17N_25	P31	
25	IO_L18P_GC_25	A39	
25	IO_L18N_GC_25	B38	
25	IO_L19P_GC_25	N31	
25	IO_L19N_GC_25	M32	
26	IO_L0P_26	P27	
26	IO_L0N_26	R27	
26	IO_L1P_26	P26	
26	IO_L1N_26	N26	
26	IO_L2P_26	P25	
26	IO_L2N_26	R25	
26	IO_L3P_26	L27	
26	IO_L3N_26	M27	
26	IO_L4P_26	J30	
26	IO_L4N_VREF_26	K29	
26	IO_L5P_26	F31	
26	IO_L5N_26	F30	
26	IO_L6P_26	E32	
26	IO_L6N_26	F32	
26	IO_L7P_26	A32	
26	IO_L7N_26	B32	
26	IO_L8P_SRCC_26	K30	
26	IO_L8N_SRCC_26	J31	
26	IO_L9P_MRCC_26	A35	
26	IO_L9N_MRCC_26	A34	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
26	IO_L10P_MRCC_26	D33	
26	IO_L10N_MRCC_26	E33	
26	IO_L11P_SRCC_26	B33	
26	IO_L11N_SRCC_26	C34	
26	IO_L12P_VRN_26	M28	
26	IO_L12N_VRP_26	L29	
26	IO_L13P_26	K28	
26	IO_L13N_26	J28	
26	IO_L14P_26	G31	
26	IO_L14N_VREF_26	H31	
26	IO_L15P_26	C33	
26	IO_L15N_26	D32	
26	IO_L16P_26	G33	
26	IO_L16N_26	G32	
26	IO_L17P_26	H29	
26	IO_L17N_26	H30	
26	IO_L18P_26	C35	
26	IO_L18N_26	B34	
26	IO_L19P_26	D35	
26	IO_L19N_26	E34	
27	IO_L0P_27	L25	
27	IO_L0N_27	M24	
27	IO_L1P_27	N25	
27	IO_L1N_27	M26	
27	IO_L2P_27	M22	
27	IO_L2N_27	M21	
27	IO_L3P_27	G27	
27	IO_L3N_27	G26	
27	IO_L4P_27	N23	
27	IO_L4N_VREF_27	M23	
27	IO_L5P_27	G28	
27	IO_L5N_27	F27	
27	IO_L6P_27	G29	

Table 2-7: FF1760 Package—LX550T and LX760 (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
27	IO_L6N_27	F29	
27	IO_L7P_27	H26	
27	IO_L7N_27	J26	
27	IO_L8P_SRCC_27	N21	
27	IO_L8N_SRCC_27	P22	
27	IO_L9P_MRCC_27	P23	
27	IO_L9N_MRCC_27	N24	
27	IO_L10P_MRCC_27	D28	
27	IO_L10N_MRCC_27	E28	
27	IO_L11P_SRCC_27	B28	
27	IO_L11N_SRCC_27	B29	
27	IO_L12P_VRN_27	H28	
27	IO_L12N_VRP_27	J27	
27	IO_L13P_27	C29	
27	IO_L13N_27	C28	
27	IO_L14P_27	C31	
27	IO_L14N_VREF_27	C30	
27	IO_L15P_27	D30	
27	IO_L15N_27	E29	
27	IO_L16P_27	A30	
27	IO_L16N_27	A29	
27	IO_L17P_27	L26	
27	IO_L17N_27	K27	
27	IO_L18P_27	A31	
27	IO_L18N_27	B31	
27	IO_L19P_27	D31	
27	IO_L19N_27	E30	
28	IO_L0P_28	E22	
28	IO_L0N_28	D22	
28	IO_L1P_28	B24	
28	IO_L1N_28	C24	
28	IO_L2P_28	K24	
28	IO_L2N_28	J25	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
28	IO_L3P_28	G24	
28	IO_L3N_28	F24	
28	IO_L4P_28	L24	
28	IO_L4N_VREF_28	K25	
28	IO_L5P_28	E23	
28	IO_L5N_28	D23	
28	IO_L6P_28	E24	
28	IO_L6N_28	E25	
28	IO_L7P_28	H24	
28	IO_L7N_28	H25	
28	IO_L8P_SRCC_28	K23	
28	IO_L8N_SRCC_28	J23	
28	IO_L9P_MRCC_28	B22	
28	IO_L9N_MRCC_28	A22	
28	IO_L10P_MRCC_28	F26	
28	IO_L10N_MRCC_28	F25	
28	IO_L11P_SRCC_28	C23	
28	IO_L11N_SRCC_28	B23	
28	IO_L12P_VRN_28	B26	
28	IO_L12N_VRP_28	C25	
28	IO_L13P_28	F22	
28	IO_L13N_28	G22	
28	IO_L14P_28	B27	
28	IO_L14N_VREF_28	C26	
28	IO_L15P_28	D26	
28	IO_L15N_28	D25	
28	IO_L16P_28	A25	
28	IO_L16N_28	A24	
28	IO_L17P_28	G23	
28	IO_L17N_28	H23	
28	IO_L18P_28	A27	
28	IO_L18N_28	A26	
28	IO_L19P_28	E27	

Table 2-7: FF1760 Package—LX550T and LX760 (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
28	IO_L19N_28	D27	
30	IO_L0P_30	AU18	
30	IO_L0N_30	AV18	
30	IO_L1P_30	AT19	
30	IO_L1N_30	AR19	
30	IO_L2P_30	BB14	
30	IO_L2N_30	BA14	
30	IO_L3P_30	BA17	
30	IO_L3N_30	BA16	
30	IO_L4P_30	BB16	
30	IO_L4N_VREF_30	BA15	
30	IO_L5P_30	AU19	
30	IO_L5N_30	AV19	
30	IO_L6P_30	AV20	
30	IO_L6N_30	AW20	
30	IO_L7P_30	BB17	
30	IO_L7N_30	BB18	
30	IO_L8P_SRCC_30	AY17	
30	IO_L8N_SRCC_30	AW17	
30	IO_L9P_MRCC_30	BA20	
30	IO_L9N_MRCC_30	BB19	
30	IO_L10P_MRCC_30	AM22	
30	IO_L10N_MRCC_30	AL22	
30	IO_L11P_SRCC_30	AW21	
30	IO_L11N_SRCC_30	AY20	
30	IO_L12P_VRN_30	AY18	
30	IO_L12N_VRP_30	AW18	
30	IO_L13P_30	AR22	
30	IO_L13N_30	AP22	
30	IO_L14P_30	AY19	
30	IO_L14N_VREF_30	BA19	
30	IO_L15P_30	AN21	
30	IO_L15N_30	AM21	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
30	IO_L16P_30	AN20	
30	IO_L16N_30	AP20	
30	IO_L17P_30	AT21	
30	IO_L17N_30	AT20	
30	IO_L18P_30	AP21	
30	IO_L18N_30	AR20	
30	IO_L19P_30	AU21	
30	IO_L19N_30	AV21	
31	IO_L0P_31	AV13	
31	IO_L0N_31	AV14	
31	IO_L1P_31	AP18	
31	IO_L1N_31	AN18	
31	IO_L2P_31	AW11	
31	IO_L2N_31	AY10	
31	IO_L3P_31	AN19	
31	IO_L3N_31	AM19	
31	IO_L4P_31	BA11	
31	IO_L4N_VREF_31	BA10	
31	IO_L5P_31	AU16	
31	IO_L5N_31	AV15	
31	IO_L6P_31	AJ20	
31	IO_L6N_31	AK19	
31	IO_L7P_31	AP17	
31	IO_L7N_31	AR17	
31	IO_L8P_SRCC_31	BA12	
31	IO_L8N_SRCC_31	BB11	
31	IO_L9P_MRCC_31	AT17	
31	IO_L9N_MRCC_31	AR18	
31	IO_L10P_MRCC_31	AK20	
31	IO_L10N_MRCC_31	AJ21	
31	IO_L11P_SRCC_31	AY12	
31	IO_L11N_SRCC_31	AY13	
31	IO_L12P_VRN_31	AW13	

Table 2-7: FF1760 Package—LX550T and LX760 (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
31	IO_L12N_VRP_31	AW12	
31	IO_L13P_31	AY15	
31	IO_L13N_31	AY14	
31	IO_L14P_31	AT16	
31	IO_L14N_VREF_31	AT15	
31	IO_L15P_31	AW16	
31	IO_L15N_31	AW15	
31	IO_L16P_31	AL19	
31	IO_L16N_31	AM18	
31	IO_L17P_31	BB12	
31	IO_L17N_31	BB13	
31	IO_L18P_31	AL21	
31	IO_L18N_31	AL20	
31	IO_L19P_31	AU17	
31	IO_L19N_31	AV16	
32	IO_L0P_32	AU9	
32	IO_L0N_32	AV9	
32	IO_L1P_32	AP16	
32	IO_L1N_32	AN16	
32	IO_L2P_32	AL15	
32	IO_L2N_32	AK15	
32	IO_L3P_32	AR14	
32	IO_L3N_32	AR13	
32	IO_L4P_32	AT10	
32	IO_L4N_VREF_32	AT11	
32	IO_L5P_32	AU11	
32	IO_L5N_32	AV10	
32	IO_L6P_32	AU12	
32	IO_L6N_32	AV11	
32	IO_L7P_32	AK18	
32	IO_L7N_32	AJ18	
32	IO_L8P_SRCC_32	AW8	
32	IO_L8N_SRCC_32	AV8	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
32	IO_L9P_MRCC_32	AT14	
32	IO_L9N_MRCC_32	AR15	
32	IO_L10P_MRCC_32	AU14	
32	IO_L10N_MRCC_32	AU13	
32	IO_L11P_SRCC_32	AW10	
32	IO_L11N_SRCC_32	AY9	
32	IO_L12P_VRN_32	AY8	
32	IO_L12N_VRP_32	BA7	
32	IO_L13P_32	BB9	
32	IO_L13N_32	BA9	
32	IO_L14P_32	AM16	
32	IO_L14N_VREF_32	AL16	
32	IO_L15P_32	AK17	
32	IO_L15N_32	AJ17	
32	IO_L16P_32	AT12	
32	IO_L16N_32	AR12	
32	IO_L17P_32	BB7	
32	IO_L17N_32	BB8	
32	IO_L18P_32	AP15	
32	IO_L18N_32	AN15	
32	IO_L19P_32	AM17	
32	IO_L19N_32	AL17	
33	IO_L0P_33	AT7	
33	IO_L0N_33	AR8	
33	IO_L1P_33	AN10	
33	IO_L1N_33	AM11	
33	IO_L2P_33	AK13	
33	IO_L2N_33	AJ13	
33	IO_L3P_33	AR10	
33	IO_L3N_33	AP10	
33	IO_L4P_33	AP8	
33	IO_L4N_VREF_33	AN9	
33	IO_L5P_33	AK14	

Table 2-7: FF1760 Package—LX550T and LX760 (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
33	IO_L5N_33	AJ15	
33	IO_L6P_33	AJ16	
33	IO_L6N_33	AH16	
33	IO_L7P_33	AP11	
33	IO_L7N_33	AP12	
33	IO_L8P_SRCC_33	AT6	
33	IO_L8N_SRCC_33	AR7	
33	IO_L9P_MRCC_33	AT9	
33	IO_L9N_MRCC_33	AR9	
33	IO_L10P_MRCC_33	AV6	
33	IO_L10N_MRCC_33	AU6	
33	IO_L11P_SRCC_33	AW7	
33	IO_L11N_SRCC_33	AY7	
33	IO_L12P_VRN_33	BA5	
33	IO_L12N_VRP_33	AY5	
33	IO_L13P_33	BB6	
33	IO_L13N_33	BA6	
33	IO_L14P_33	AM12	
33	IO_L14N_VREF_33	AN11	
33	IO_L15P_33	AW6	
33	IO_L15N_33	AW5	
33	IO_L16P_33	AM13	
33	IO_L16N_33	AN13	
33	IO_L17P_33	AN14	
33	IO_L17N_33	AP13	
33	IO_L18P_33	AM14	
33	IO_L18N_33	AL14	
33	IO_L19P_33	AU8	
33	IO_L19N_33	AU7	
34	IO_L0P_GC_34	AH11	
34	IO_L0N_GC_34	AJ10	
34	IO_L1P_GC_34	AW2	
34	IO_L1N_GC_34	AW1	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
34	IO_L2P_A15_D31_34	AL7	
34	IO_L2N_A14_D30_34	AK8	
34	IO_L3P_A13_D29_34	AY2	
34	IO_L3N_A12_D28_34	BA1	
34	IO_L4P_A11_D27_34	AU4	
34	IO_L4N_VREF_A10_D26_34	AV3	
34	IO_L5P_A09_D25_34	AN6	
34	IO_L5N_A08_D24_34	AM7	
34	IO_L6P_A07_D23_34	AR5	
34	IO_L6N_A06_D22_34	AP5	
34	IO_L7P_A05_D21_34	BA2	
34	IO_L7N_A04_D20_34	BB2	
34	IO_L8P_SRCC_34	BB4	
34	IO_L8N_SRCC_34	BB3	
34	IO_L9P_MRCC_34	AY3	
34	IO_L9N_MRCC_34	AW3	
34	IO_L10P_MRCC_34	AV5	
34	IO_L10N_MRCC_34	AV4	
34	IO_L11P_SRCC_34	AK9	
34	IO_L11N_SRCC_34	AL9	
34	IO_L12P_A03_D19_34	AY4	
34	IO_L12N_A02_D18_34	BA4	
34	IO_L13P_A01_D17_34	AK10	
34	IO_L13N_A00_D16_34	AJ11	
34	IO_L14P_A25_34	AT5	
34	IO_L14N_VREF_A24_34	AT4	
34	IO_L15P_A23_34	AP7	
34	IO_L15N_A22_34	AP6	
34	IO_L16P_A21_34	AK12	
34	IO_L16N_A20_34	AJ12	
34	IO_L17P_A19_34	AM9	
34	IO_L17N_A18_34	AL10	
34	IO_L18P_A17_34	AL12	

Table 2-7: FF1760 Package—LX550T and LX760 (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
34	IO_L18N_A16_34	AL11	
34	IO_L19P_VRN_34	AN8	
34	IO_L19N_VRP_34	AM8	
35	IO_L0P_35	F10	
35	IO_L0N_35	F9	
35	IO_L1P_35	D6	
35	IO_L1N_35	D7	
35	IO_L2P_SM0P_35	H9	
35	IO_L2N_SM0N_35	G9	
35	IO_L3P_SM1P_35	H11	
35	IO_L3N_SM1N_35	H10	
35	IO_L4P_35	M14	
35	IO_L4N_VREF_35	L14	
35	IO_L5P_SM2P_35	F7	
35	IO_L5N_SM2N_35	E7	
35	IO_L6P_SM3P_35	G6	
35	IO_L6N_SM3N_35	F6	
35	IO_L7P_SM4P_35	J10	
35	IO_L7N_SM4N_35	J11	
35	IO_L8P_SRCC_35	K10	
35	IO_L8N_SRCC_35	L11	
35	IO_L9P_MRCC_35	K13	
35	IO_L9N_MRCC_35	J12	
35	IO_L10P_MRCC_35	G7	
35	IO_L10N_MRCC_35	G8	
35	IO_L11P_SRCC_35	K12	
35	IO_L11N_SRCC_35	L12	
35	IO_L12P_SM5P_35	L10	
35	IO_L12N_SM5N_35	K9	
35	IO_L13P_SM6P_35	M16	
35	IO_L13N_SM6N_35	L15	
35	IO_L14P_35	M13	
35	IO_L14N_VREF_35	M12	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
35	IO_L15P_SM7P_35	J8	
35	IO_L15N_SM7N_35	H8	
35	IO_L16P_VRN_35	N14	
35	IO_L16N_VRP_35	N15	
35	IO_L17P_35	N16	
35	IO_L17N_35	P16	
35	IO_L18P_GC_35	R15	
35	IO_L18N_GC_35	P15	
35	IO_L19P_GC_35	K8	
35	IO_L19N_GC_35	J7	
36	IO_L0P_36	D10	
36	IO_L0N_36	D11	
36	IO_L1P_36	A11	
36	IO_L1N_36	A12	
36	IO_L2P_36	G11	
36	IO_L2N_36	G12	
36	IO_L3P_36	A9	
36	IO_L3N_36	A10	
36	IO_L4P_36	C8	
36	IO_L4N_VREF_36	C9	
36	IO_L5P_36	E12	
36	IO_L5N_36	D12	
36	IO_L6P_36	E8	
36	IO_L6N_36	D8	
36	IO_L7P_36	B12	
36	IO_L7N_36	B11	
36	IO_L8P_SRCC_36	B7	
36	IO_L8N_SRCC_36	A7	
36	IO_L9P_MRCC_36	B8	
36	IO_L9N_MRCC_36	B9	
36	IO_L10P_MRCC_36	J15	
36	IO_L10N_MRCC_36	J16	
36	IO_L11P_SRCC_36	C11	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
36	IO_L11N_SRCC_36	C10	
36	IO_L12P_VRN_36	J13	
36	IO_L12N_VRP_36	K14	
36	IO_L13P_36	H14	
36	IO_L13N_36	G14	
36	IO_L14P_36	A5	
36	IO_L14N_VREF_36	A6	
36	IO_L15P_36	E9	
36	IO_L15N_36	E10	
36	IO_L16P_36	L16	
36	IO_L16N_36	K15	
36	IO_L17P_36	G13	
36	IO_L17N_36	H13	
36	IO_L18P_36	C6	
36	IO_L18N_36	B6	
36	IO_L19P_36	F11	
36	IO_L19N_36	F12	
37	IO_L0P_37	D13	
37	IO_L0N_37	E13	
37	IO_L1P_37	A14	
37	IO_L1N_37	A15	
37	IO_L2P_37	K17	
37	IO_L2N_37	J17	
37	IO_L3P_37	B13	
37	IO_L3N_37	B14	
37	IO_L4P_37	P20	
37	IO_L4N_VREF_37	N19	
37	IO_L5P_37	E14	
37	IO_L5N_37	E15	
37	IO_L6P_37	F15	
37	IO_L6N_37	F14	
37	IO_L7P_37	C16	
37	IO_L7N_37	D16	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
37	IO_L8P_SRCC_37	H15	
37	IO_L8N_SRCC_37	H16	
37	IO_L9P_MRCC_37	P21	
37	IO_L9N_MRCC_37	N20	
37	IO_L10P_MRCC_37	G16	
37	IO_L10N_MRCC_37	F16	
37	IO_L11P_SRCC_37	C15	
37	IO_L11N_SRCC_37	D15	
37	IO_L12P_VRN_37	C13	
37	IO_L12N_VRP_37	C14	
37	IO_L13P_37	H18	
37	IO_L13N_37	G17	
37	IO_L14P_37	M17	
37	IO_L14N_VREF_37	L17	
37	IO_L15P_37	K18	
37	IO_L15N_37	J18	
37	IO_L16P_37	P17	
37	IO_L16N_37	N18	
37	IO_L17P_37	K19	
37	IO_L17N_37	L19	
37	IO_L18P_37	R17	
37	IO_L18N_37	P18	
37	IO_L19P_37	M18	
37	IO_L19N_37	M19	
38	IO_L0P_38	F21	
38	IO_L0N_38	E20	
38	IO_L1P_38	J22	
38	IO_L1N_38	J21	
38	IO_L2P_38	K20	
38	IO_L2N_38	J20	
38	IO_L3P_38	G21	
38	IO_L3N_38	H21	
38	IO_L4P_38	G18	

Table 2-7: FF1760 Package—LX550T and LX760 (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
38	IO_L4N_VREF_38	H19	
38	IO_L5P_38	F20	
38	IO_L5N_38	E19	
38	IO_L6P_38	E17	
38	IO_L6N_38	F17	
38	IO_L7P_38	K22	
38	IO_L7N_38	L22	
38	IO_L8P_SRCC_38	L21	
38	IO_L8N_SRCC_38	L20	
38	IO_L9P_MRCC_38	D21	
38	IO_L9N_MRCC_38	C21	
38	IO_L10P_MRCC_38	D17	
38	IO_L10N_MRCC_38	D18	
38	IO_L11P_SRCC_38	B21	
38	IO_L11N_SRCC_38	A21	
38	IO_L12P_VRN_38	C18	
38	IO_L12N_VRP_38	C19	
38	IO_L13P_38	A19	
38	IO_L13N_38	A20	
38	IO_L14P_38	B18	
38	IO_L14N_VREF_38	B19	
38	IO_L15P_38	F19	
38	IO_L15N_38	E18	
38	IO_L16P_38	B16	
38	IO_L16N_38	B17	
38	IO_L17P_38	C20	
38	IO_L17N_38	D20	
38	IO_L18P_38	A16	
38	IO_L18N_38	A17	
38	IO_L19P_38	G19	
38	IO_L19N_38	H20	
42	IO_L0P_42	AH6	
42	IO_L0N_42	AH5	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
42	IO_L1P_42	AL1	
42	IO_L1N_42	AK2	
42	IO_L2P_42	AR2	
42	IO_L2N_42	AP2	
42	IO_L3P_42	AL2	
42	IO_L3N_42	AK3	
42	IO_L4P_42	AT2	
42	IO_L4N_VREF_42	AT1	
42	IO_L5P_42	AJ6	
42	IO_L5N_42	AJ5	
42	IO_L6P_42	AL4	
42	IO_L6N_42	AK4	
42	IO_L7P_42	AM1	
42	IO_L7N_42	AM2	
42	IO_L8P_SRCC_42	AV1	
42	IO_L8N_SRCC_42	AU1	
42	IO_L9P_MRCC_42	AP1	
42	IO_L9N_MRCC_42	AN1	
42	IO_L10P_MRCC_42	AL5	
42	IO_L10N_MRCC_42	AK5	
42	IO_L11P_SRCC_42	AP3	
42	IO_L11N_SRCC_42	AN3	
42	IO_L12P_VRN_42	AU3	
42	IO_L12N_VRP_42	AU2	
42	IO_L13P_42	AM4	
42	IO_L13N_42	AM3	
42	IO_L14P_42	AH10	
42	IO_L14N_VREF_42	AH9	
42	IO_L15P_42	AJ8	
42	IO_L15N_42	AK7	
42	IO_L16P_42	AR4	
42	IO_L16N_42	AR3	
42	IO_L17P_42	AN4	

Table 2-7: FF1760 Package—LX550T and LX760 (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
42	IO_L17N_42	AN5	
42	IO_L18P_42	AM6	
42	IO_L18N_42	AL6	
42	IO_L19P_42	AH8	
42	IO_L19N_42	AJ7	
43	IO_L0P_43	AD6	
43	IO_L0N_43	AD5	
43	IO_L1P_43	AG1	
43	IO_L1N_43	AF1	
43	IO_L2P_43	AC10	
43	IO_L2N_43	AC11	
43	IO_L3P_43	AG2	
43	IO_L3N_43	AF2	
43	IO_L4P_43	AF4	
43	IO_L4N_VREF_43	AE4	
43	IO_L5P_43	AF5	
43	IO_L5N_43	AE5	
43	IO_L6P_43	AG7	
43	IO_L6N_43	AG6	
43	IO_L7P_43	AH1	
43	IO_L7N_43	AJ1	
43	IO_L8P_SRCC_43	AF10	
43	IO_L8N_SRCC_43	AF9	
43	IO_L9P_MRCC_43	AE7	
43	IO_L9N_MRCC_43	AD7	
43	IO_L10P_MRCC_43	AH4	
43	IO_L10N_MRCC_43	AG4	
43	IO_L11P_SRCC_43	AD8	
43	IO_L11N_SRCC_43	AE8	
43	IO_L12P_VRN_43	AG9	
43	IO_L12N_VRP_43	AG8	
43	IO_L13P_43	AD10	
43	IO_L13N_43	AD11	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
43	IO_L14P_43	AH3	
43	IO_L14N_VREF_43	AG3	
43	IO_L15P_43	AF7	
43	IO_L15N_43	AF6	
43	IO_L16P_43	AJ3	
43	IO_L16N_43	AJ2	
43	IO_L17P_43	AE10	
43	IO_L17N_43	AE9	
43	IO_L18P_43	AG12	
43	IO_L18N_43	AG11	
43	IO_L19P_43	AF12	
43	IO_L19N_43	AF11	
44	IO_L0P_44	AA6	
44	IO_L0N_44	AA7	
44	IO_L1P_44	W1	
44	IO_L1N_44	W2	
44	IO_L2P_44	AB9	
44	IO_L2N_44	AB8	
44	IO_L3P_44	Y3	
44	IO_L3N_44	Y2	
44	IO_L4P_44	AC6	
44	IO_L4N_VREF_44	AC5	
44	IO_L5P_44	AA4	
44	IO_L5N_44	AA5	
44	IO_L6P_44	AC3	
44	IO_L6N_44	AB3	
44	IO_L7P_44	AA1	
44	IO_L7N_44	AA2	
44	IO_L8P_SRCC_44	AB1	
44	IO_L8N_SRCC_44	AB2	
44	IO_L9P_MRCC_44	Y7	
44	IO_L9N_MRCC_44	Y8	
44	IO_L10P_MRCC_44	AC4	

Table 2-7: FF1760 Package—LX550T and LX760 (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
44	IO_L10N_MRCC_44	AB4	
44	IO_L11P_SRCC_44	Y10	
44	IO_L11N_SRCC_44	AA11	
44	IO_L12P_VRN_44	AC9	
44	IO_L12N_VRP_44	AC8	
44	IO_L13P_44	Y5	
44	IO_L13N_44	Y4	
44	IO_L14P_44	AD3	
44	IO_L14N_VREF_44	AD2	
44	IO_L15P_44	AB7	
44	IO_L15N_44	AB6	
44	IO_L16P_44	AD1	
44	IO_L16N_44	AC1	
44	IO_L17P_44	AA10	
44	IO_L17N_44	AB11	
44	IO_L18P_44	AE3	
44	IO_L18N_44	AE2	
44	IO_L19P_44	AA9	
44	IO_L19N_44	Y9	
45	IO_L0P_45	R4	
45	IO_L0N_45	R5	
45	IO_L1P_45	N1	
45	IO_L1N_45	M1	
45	IO_L2P_45	V9	
45	IO_L2N_45	V10	
45	IO_L3P_45	P2	
45	IO_L3N_45	P3	
45	IO_L4P_45	V4	
45	IO_L4N_VREF_45	U4	
45	IO_L5P_45	U6	
45	IO_L5N_45	T5	
45	IO_L6P_45	W3	
45	IO_L6N_45	V3	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
45	IO_L7P_45	U11	
45	IO_L7N_45	V11	
45	IO_L8P_SRCC_45	W8	
45	IO_L8N_SRCC_45	W7	
45	IO_L9P_MRCC_45	T6	
45	IO_L9N_MRCC_45	T7	
45	IO_L10P_MRCC_45	V5	
45	IO_L10N_MRCC_45	V6	
45	IO_L11P_SRCC_45	R3	
45	IO_L11N_SRCC_45	T4	
45	IO_L12P_VRN_45	W11	
45	IO_L12N_VRP_45	W10	
45	IO_L13P_45	U8	
45	IO_L13N_45	U9	
45	IO_L14P_45	U2	
45	IO_L14N_VREF_45	U3	
45	IO_L15P_45	W6	
45	IO_L15N_45	W5	
45	IO_L16P_45	T1	
45	IO_L16N_45	T2	
45	IO_L17P_45	P1	
45	IO_L17N_45	R2	
45	IO_L18P_45	V1	
45	IO_L18N_45	U1	
45	IO_L19P_45	V8	
45	IO_L19N_45	U7	
46	IO_L0P_46	L5	
46	IO_L0N_46	M6	
46	IO_L1P_46	D1	
46	IO_L1N_46	E2	
46	IO_L2P_46	T9	
46	IO_L2N_46	R10	
46	IO_L3P_46	F1	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
46	IO_L3N_46	F2	
46	IO_L4P_46	L4	
46	IO_L4N_VREF_46	M4	
46	IO_L5P_46	N5	
46	IO_L5N_46	N6	
46	IO_L6P_46	L2	
46	IO_L6N_46	K2	
46	IO_L7P_46	G3	
46	IO_L7N_46	H3	
46	IO_L8P_SRCC_46	G1	
46	IO_L8N_SRCC_46	G2	
46	IO_L9P_MRCC_46	K3	
46	IO_L9N_MRCC_46	K4	
46	IO_L10P_MRCC_46	P5	
46	IO_L10N_MRCC_46	N4	
46	IO_L11P_SRCC_46	N8	
46	IO_L11N_SRCC_46	P7	
46	IO_L12P_VRN_46	T11	
46	IO_L12N_VRP_46	T10	
46	IO_L13P_46	R9	
46	IO_L13N_46	P10	
46	IO_L14P_46	N3	
46	IO_L14N_VREF_46	M3	
46	IO_L15P_46	R7	
46	IO_L15N_46	P6	
46	IO_L16P_46	J1	
46	IO_L16N_46	H1	
46	IO_L17P_46	P8	
46	IO_L17N_46	R8	
46	IO_L18P_46	L1	
46	IO_L18N_46	M2	
46	IO_L19P_46	J2	
46	IO_L19N_46	J3	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
47	IO_L0P_47	J6	
47	IO_L0N_47	K7	
47	IO_L1P_47	B4	
47	IO_L1N_47	A4	
47	IO_L2P_47	H5	
47	IO_L2N_47	H6	
47	IO_L3P_47	B3	
47	IO_L3N_47	A2	
47	IO_L4P_47	N9	
47	IO_L4N_VREF_47	N10	
47	IO_L5P_47	F5	
47	IO_L5N_47	E5	
47	IO_L6P_47	H4	
47	IO_L6N_47	G4	
47	IO_L7P_47	C5	
47	IO_L7N_47	D5	
47	IO_L8P_SRCC_47	M8	
47	IO_L8N_SRCC_47	L7	
47	IO_L9P_MRCC_47	C3	
47	IO_L9N_MRCC_47	C4	
47	IO_L10P_MRCC_47	F4	
47	IO_L10N_MRCC_47	E4	
47	IO_L11P_SRCC_47	N13	
47	IO_L11N_SRCC_47	P13	
47	IO_L12P_VRN_47	L6	
47	IO_L12N_VRP_47	M7	
47	IO_L13P_47	M9	
47	IO_L13N_47	L9	
47	IO_L14P_47	E3	
47	IO_L14N_VREF_47	D3	
47	IO_L15P_47	K5	
47	IO_L15N_47	J5	
47	IO_L16P_47	B1	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
47	IO_L16N_47	B2	
47	IO_L17P_47	M11	
47	IO_L17N_47	N11	
47	IO_L18P_47	C1	
47	IO_L18N_47	D2	
47	IO_L19P_47	P11	
47	IO_L19N_47	P12	
NA	GND	A13	
NA	GND	A23	
NA	GND	A3	
NA	GND	A33	
NA	GND	AA13	
NA	GND	AA15	
NA	GND	AA17	
NA	GND	AA19	
NA	GND	AA23	
NA	GND	AA25	
NA	GND	AA27	
NA	GND	AA29	
NA	GND	AA3	
NA	GND	AA31	
NA	GND	AA33	
NA	GND	AB10	
NA	GND	AB12	
NA	GND	AB14	
NA	GND	AB16	
NA	GND	AB18	
NA	GND	AB20	
NA	GND	AB24	
NA	GND	AB26	
NA	GND	AB28	
NA	GND	AB30	
NA	GND	AB40	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AC13	
NA	GND	AC15	
NA	GND	AC17	
NA	GND	AC19	
NA	GND	AC23	
NA	GND	AC25	
NA	GND	AC27	
NA	GND	AC29	
NA	GND	AC31	
NA	GND	AC37	
NA	GND	AC7	
NA	GND	AD12	
NA	GND	AD14	
NA	GND	AD16	
NA	GND	AD18	
NA	GND	AD20	
NA	GND	AD22	
NA	GND	AD24	
NA	GND	AD26	
NA	GND	AD28	
NA	GND	AD30	
NA	GND	AD34	
NA	GND	AD4	
NA	GND	AE1	
NA	GND	AE11	
NA	GND	AE13	
NA	GND	AE15	
NA	GND	AE17	
NA	GND	AE19	
NA	GND	AE21	
NA	GND	AE23	
NA	GND	AE25	
NA	GND	AE27	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AE29	
NA	GND	AE31	
NA	GND	AE41	
NA	GND	AF16	
NA	GND	AF18	
NA	GND	AF20	
NA	GND	AF22	
NA	GND	AF24	
NA	GND	AF26	
NA	GND	AF28	
NA	GND	AF38	
NA	GND	AF8	
NA	GND	AG13	
NA	GND	AG15	
NA	GND	AG17	
NA	GND	AG19	
NA	GND	AG21	
NA	GND	AG23	
NA	GND	AG25	
NA	GND	AG27	
NA	GND	AG35	
NA	GND	AG5	
NA	GND	AH12	
NA	GND	AH18	
NA	GND	AH2	
NA	GND	AH20	
NA	GND	AH22	
NA	GND	AH24	
NA	GND	AH32	
NA	GND	AH42	
NA	GND	AJ19	
NA	GND	AJ29	
NA	GND	AJ39	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AJ9	
NA	GND	AK16	
NA	GND	AK26	
NA	GND	AK36	
NA	GND	AK6	
NA	GND	AL13	
NA	GND	AL23	
NA	GND	AL3	
NA	GND	AL33	
NA	GND	AM10	
NA	GND	AM20	
NA	GND	AM30	
NA	GND	AM40	
NA	GND	AN17	
NA	GND	AN27	
NA	GND	AN37	
NA	GND	AN7	
NA	GND	AP14	
NA	GND	AP24	
NA	GND	AP34	
NA	GND	AP4	
NA	GND	AR1	
NA	GND	AR11	
NA	GND	AR21	
NA	GND	AR31	
NA	GND	AR41	
NA	GND	AT18	
NA	GND	AT28	
NA	GND	AT38	
NA	GND	AT8	
NA	GND	AU15	
NA	GND	AU25	
NA	GND	AU35	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AU5	
NA	GND	AV12	
NA	GND	AV2	
NA	GND	AV22	
NA	GND	AV32	
NA	GND	AV42	
NA	GND	AW19	
NA	GND	AW29	
NA	GND	AW39	
NA	GND	AW9	
NA	GND	AY16	
NA	GND	AY26	
NA	GND	AY36	
NA	GND	AY6	
NA	GND	B10	
NA	GND	B20	
NA	GND	B30	
NA	GND	B40	
NA	GND	BA13	
NA	GND	BA23	
NA	GND	BA3	
NA	GND	BA33	
NA	GND	BB10	
NA	GND	BB20	
NA	GND	BB30	
NA	GND	BB40	
NA	GND	C17	
NA	GND	C27	
NA	GND	C37	
NA	GND	C7	
NA	GND	D14	
NA	GND	D24	
NA	GND	D34	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	D4	
NA	GND	E1	
NA	GND	E11	
NA	GND	E21	
NA	GND	E31	
NA	GND	E41	
NA	GND	F18	
NA	GND	F28	
NA	GND	F38	
NA	GND	F8	
NA	GND	G15	
NA	GND	G25	
NA	GND	G35	
NA	GND	G5	
NA	GND	H12	
NA	GND	H2	
NA	GND	H22	
NA	GND	H32	
NA	GND	H42	
NA	GND	J19	
NA	GND	J29	
NA	GND	J39	
NA	GND	J9	
NA	GND	K16	
NA	GND	K26	
NA	GND	K36	
NA	GND	K6	
NA	GND	L13	
NA	GND	L23	
NA	GND	L3	
NA	GND	L33	
NA	GND	M10	
NA	GND	M20	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	M30	
NA	GND	M40	
NA	GND	N17	
NA	GND	N27	
NA	GND	N37	
NA	GND	N7	
NA	GND	P14	
NA	GND	P24	
NA	GND	P34	
NA	GND	P4	
NA	GND	R1	
NA	GND	R11	
NA	GND	R13	
NA	GND	R19	
NA	GND	R21	
NA	GND	R23	
NA	GND	R31	
NA	GND	R41	
NA	GND	T12	
NA	GND	T16	
NA	GND	T18	
NA	GND	T20	
NA	GND	T22	
NA	GND	T24	
NA	GND	T26	
NA	GND	T28	
NA	GND	T38	
NA	GND	T8	
NA	GND	U13	
NA	GND	U17	
NA	GND	U19	
NA	GND	U21	
NA	GND	U23	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	U25	
NA	GND	U27	
NA	GND	U29	
NA	GND	U35	
NA	GND	U5	
NA	GND	V12	
NA	GND	V14	
NA	GND	V16	
NA	GND	V18	
NA	GND	V2	
NA	GND	V20	
NA	GND	V22	
NA	GND	V24	
NA	GND	V26	
NA	GND	V28	
NA	GND	V30	
NA	GND	V32	
NA	GND	V42	
NA	GND	W13	
NA	GND	W15	
NA	GND	W17	
NA	GND	W19	
NA	GND	W21	
NA	GND	W23	
NA	GND	W25	
NA	GND	W27	
NA	GND	W29	
NA	GND	W31	
NA	GND	W39	
NA	GND	W9	
NA	GND	Y12	
NA	GND	Y14	
NA	GND	Y16	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	Y18	
NA	GND	Y20	
NA	GND	Y24	
NA	GND	Y26	
NA	GND	Y28	
NA	GND	Y30	
NA	GND	Y36	
NA	GND	Y6	
NA	VCCAUX	AA12	
NA	VCCAUX	AA30	
NA	VCCAUX	AB13	
NA	VCCAUX	AB29	
NA	VCCAUX	AB31	
NA	VCCAUX	AC12	
NA	VCCAUX	AC30	
NA	VCCAUX	AD13	
NA	VCCAUX	AD29	
NA	VCCAUX	AE30	
NA	VCCAUX	R12	
NA	VCCAUX	T13	
NA	VCCAUX	U12	
NA	VCCAUX	U30	
NA	VCCAUX	V13	
NA	VCCAUX	V29	
NA	VCCAUX	V31	
NA	VCCAUX	W12	
NA	VCCAUX	W30	
NA	VCCAUX	Y13	
NA	VCCAUX	Y31	
NA	VCCINT	AA14	
NA	VCCINT	AA16	
NA	VCCINT	AA18	
NA	VCCINT	AA20	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	AA24	
NA	VCCINT	AA26	
NA	VCCINT	AA28	
NA	VCCINT	AB15	
NA	VCCINT	AB17	
NA	VCCINT	AB19	
NA	VCCINT	AB23	
NA	VCCINT	AB25	
NA	VCCINT	AB27	
NA	VCCINT	AC14	
NA	VCCINT	AC16	
NA	VCCINT	AC18	
NA	VCCINT	AC20	
NA	VCCINT	AC24	
NA	VCCINT	AC26	
NA	VCCINT	AC28	
NA	VCCINT	AD15	
NA	VCCINT	AD17	
NA	VCCINT	AD19	
NA	VCCINT	AD21	
NA	VCCINT	AD23	
NA	VCCINT	AD25	
NA	VCCINT	AD27	
NA	VCCINT	AE14	
NA	VCCINT	AE16	
NA	VCCINT	AE18	
NA	VCCINT	AE20	
NA	VCCINT	AE22	
NA	VCCINT	AE24	
NA	VCCINT	AE26	
NA	VCCINT	AE28	
NA	VCCINT	AF15	
NA	VCCINT	AF17	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	AF19	
NA	VCCINT	AF21	
NA	VCCINT	AF23	
NA	VCCINT	AF25	
NA	VCCINT	AF27	
NA	VCCINT	AG14	
NA	VCCINT	AG16	
NA	VCCINT	AG18	
NA	VCCINT	AG20	
NA	VCCINT	AG22	
NA	VCCINT	AG24	
NA	VCCINT	AG26	
NA	VCCINT	AG28	
NA	VCCINT	AH15	
NA	VCCINT	AH17	
NA	VCCINT	AH19	
NA	VCCINT	AH21	
NA	VCCINT	AH23	
NA	VCCINT	AH25	
NA	VCCINT	AH27	
NA	VCCINT	R18	
NA	VCCINT	R20	
NA	VCCINT	R22	
NA	VCCINT	R24	
NA	VCCINT	T17	
NA	VCCINT	T19	
NA	VCCINT	T21	
NA	VCCINT	T23	
NA	VCCINT	T25	
NA	VCCINT	T27	
NA	VCCINT	U16	
NA	VCCINT	U18	
NA	VCCINT	U20	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	U22	
NA	VCCINT	U24	
NA	VCCINT	U26	
NA	VCCINT	U28	
NA	VCCINT	V15	
NA	VCCINT	V17	
NA	VCCINT	V19	
NA	VCCINT	V21	
NA	VCCINT	V23	
NA	VCCINT	V25	
NA	VCCINT	V27	
NA	VCCINT	W14	
NA	VCCINT	W16	
NA	VCCINT	W18	
NA	VCCINT	W20	
NA	VCCINT	W22	
NA	VCCINT	W24	
NA	VCCINT	W26	
NA	VCCINT	W28	
NA	VCCINT	Y15	
NA	VCCINT	Y17	
NA	VCCINT	Y19	
NA	VCCINT	Y23	
NA	VCCINT	Y25	
NA	VCCINT	Y27	
NA	VCCINT	Y29	
0	VCCO_0	R16	
0	VCCO_0	U15	
12	VCCO_12	AF33	
12	VCCO_12	AJ34	
12	VCCO_12	AL38	
12	VCCO_12	AN42	
12	VCCO_12	AU40	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
13	VCCO_13	AD39	
13	VCCO_13	AE36	
13	VCCO_13	AG40	
13	VCCO_13	AH37	
13	VCCO_13	AK41	
14	VCCO_14	AA38	
14	VCCO_14	AB35	
14	VCCO_14	AC32	
14	VCCO_14	AC42	
14	VCCO_14	Y41	
15	VCCO_15	N42	
15	VCCO_15	P39	
15	VCCO_15	U40	
15	VCCO_15	V37	
15	VCCO_15	W34	
16	VCCO_16	G40	
16	VCCO_16	K41	
16	VCCO_16	L38	
16	VCCO_16	R36	
16	VCCO_16	T33	
17	VCCO_17	C42	
17	VCCO_17	D39	
17	VCCO_17	H37	
17	VCCO_17	J34	
17	VCCO_17	M35	
17	VCCO_17	N32	
20	VCCO_20	AT23	
20	VCCO_20	AW24	
20	VCCO_20	AY21	
20	VCCO_20	BA28	
20	VCCO_20	BB25	
21	VCCO_21	AJ24	
21	VCCO_21	AM25	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
21	VCCO_21	AR26	
21	VCCO_21	AV27	
21	VCCO_21	AY31	
22	VCCO_22	AL28	
22	VCCO_22	AP29	
22	VCCO_22	AU30	
22	VCCO_22	AW34	
22	VCCO_22	BB35	
23	VCCO_23	AN32	
23	VCCO_23	AT33	
23	VCCO_23	AV37	
23	VCCO_23	AY41	
23	VCCO_23	BA38	
24	VCCO_24	AG30	
24	VCCO_24	AK31	
24	VCCO_24	AM35	
24	VCCO_24	AP39	
24	VCCO_24	AR36	
25	VCCO_25	A38	
25	VCCO_25	E36	
25	VCCO_25	F33	
25	VCCO_25	K31	
25	VCCO_25	P29	
26	VCCO_26	B35	
26	VCCO_26	C32	
26	VCCO_26	G30	
26	VCCO_26	L28	
26	VCCO_26	R26	
27	VCCO_27	A28	
27	VCCO_27	D29	
27	VCCO_27	H27	
27	VCCO_27	M25	
27	VCCO_27	N22	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
28	VCCO_28	B25	
28	VCCO_28	C22	
28	VCCO_28	E26	
28	VCCO_28	F23	
28	VCCO_28	J24	
30	VCCO_30	AN22	
30	VCCO_30	AU20	
30	VCCO_30	AV17	
30	VCCO_30	BA18	
30	VCCO_30	BB15	
31	VCCO_31	AK21	
31	VCCO_31	AP19	
31	VCCO_31	AR16	
31	VCCO_31	AW14	
31	VCCO_31	AY11	
32	VCCO_32	AL18	
32	VCCO_32	AM15	
32	VCCO_32	AT13	
32	VCCO_32	AU10	
32	VCCO_32	BA8	
33	VCCO_33	AJ14	
33	VCCO_33	AN12	
33	VCCO_33	AP9	
33	VCCO_33	AV7	
33	VCCO_33	BB5	
34	VCCO_34	AK11	
34	VCCO_34	AL8	
34	VCCO_34	AR6	
34	VCCO_34	AW4	
34	VCCO_34	AY1	
35	VCCO_35	E6	
35	VCCO_35	G10	
35	VCCO_35	H7	

Table 2-7: FF1760 Package—LX550T and LX760 (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
35	VCCO_35	K11	
35	VCCO_35	M15	
36	VCCO_36	A8	
36	VCCO_36	C12	
36	VCCO_36	D9	
36	VCCO_36	F13	
36	VCCO_36	J14	
37	VCCO_37	B15	
37	VCCO_37	E16	
37	VCCO_37	H17	
37	VCCO_37	L18	
37	VCCO_37	P19	
38	VCCO_38	A18	
38	VCCO_38	D19	
38	VCCO_38	G20	
38	VCCO_38	K21	
42	VCCO_42	AH7	
42	VCCO_42	AJ4	
42	VCCO_42	AM5	
42	VCCO_42	AN2	
42	VCCO_42	AT3	
43	VCCO_43	AD9	
43	VCCO_43	AE6	
43	VCCO_43	AF3	
43	VCCO_43	AG10	
43	VCCO_43	AK1	
44	VCCO_44	AA8	
44	VCCO_44	AB5	
44	VCCO_44	AC2	
44	VCCO_44	Y1	
44	VCCO_44	Y11	
45	VCCO_45	N2	
45	VCCO_45	T3	

Table 2-7: FF1760 Package—LX550T and LX760 (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
45	VCCO_45	U10	
45	VCCO_45	V7	
45	VCCO_45	W4	
46	VCCO_46	F3	
46	VCCO_46	K1	
46	VCCO_46	M5	
46	VCCO_46	P9	
46	VCCO_46	R6	
47	VCCO_47	B5	
47	VCCO_47	C2	
47	VCCO_47	J4	
47	VCCO_47	L8	
47	VCCO_47	N12	

FF1923 Package—HX255T, HX380T, and HX565T

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T

Bank	Pin Description	Pin Number	No Connect (NC)
0	INIT_B_0	T14	
0	DONE_0	T13	
0	M1_0	T32	
0	M2_0	T33	
0	HSWAPEN_0	U13	
0	PROGRAM_B_0	U33	
0	M0_0	V32	
0	AVSS_0	AA22	
0	AVDD_0	AA23	
0	VP_0	AB23	
0	VREFP_0	AC23	
0	VN_0	AC22	
0	VREFN_0	AB22	
0	DXP_0	AD23	
0	DXN_0	AD22	
0	VBATT_0	AA13	
0	DIN_0	W13	
0	RDWR_B_0	W33	
0	CSI_B_0	AA33	
0	DOUT_BUSY_0	AE33	
0	CCLK_0	AC33	
0	TDO_0	Y12	
0	TCK_0	AB12	
0	TMS_0	AD12	
0	TDI_0	AF12	
0	VFS_0	AG33	
20	IO_L0P_20	BD21	HX255T
20	IO_L0N_20	BD20	HX255T
20	IO_L1P_20	BC19	HX255T
20	IO_L1N_20	BD19	HX255T
20	IO_L2P_20	BB21	HX255T

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
20	IO_L2N_20	BC21	HX255T
20	IO_L3P_20	AT23	HX255T
20	IO_L3N_20	AT22	HX255T
20	IO_L4P_20	BC23	HX255T
20	IO_L4N_VREF_20	BD23	HX255T
20	IO_L5P_20	BA19	HX255T
20	IO_L5N_20	BB19	HX255T
20	IO_L6P_20	AU22	HX255T
20	IO_L6N_20	AV22	HX255T
20	IO_L7P_20	AV19	HX255T
20	IO_L7N_20	AW19	HX255T
20	IO_L8P_SRCC_20	BB22	HX255T
20	IO_L8N_SRCC_20	BC22	HX255T
20	IO_L9P_MRCC_20	AR22	HX255T
20	IO_L9N_MRCC_20	AR21	HX255T
20	IO_L10P_MRCC_20	AY22	HX255T
20	IO_L10N_MRCC_20	BA22	HX255T
20	IO_L11P_SRCC_20	BA20	HX255T
20	IO_L11N_SRCC_20	BB20	HX255T
20	IO_L12P_VRN_20	AT20	HX255T
20	IO_L12N_VRP_20	AU20	HX255T
20	IO_L13P_20	AW20	HX255T
20	IO_L13N_20	AY20	HX255T
20	IO_L14P_20	AY23	HX255T
20	IO_L14N_VREF_20	BA23	HX255T
20	IO_L15P_20	AP23	HX255T
20	IO_L15N_20	AR23	HX255T
20	IO_L16P_20	AV23	HX255T
20	IO_L16N_20	AW23	HX255T
20	IO_L17P_20	AW21	HX255T
20	IO_L17N_20	AY21	HX255T
20	IO_L18P_20	AN23	HX255T
20	IO_L18N_20	AN22	HX255T

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
20	IO_L19P_20	AU21	HX255T
20	IO_L19N_20	AV21	HX255T
21	IO_L0P_21	AT25	HX255T
21	IO_L0N_21	AU25	HX255T
21	IO_L1P_21	AM26	HX255T
21	IO_L1N_21	AN26	HX255T
21	IO_L2P_21	AW26	HX255T
21	IO_L2N_21	AY26	HX255T
21	IO_L3P_21	AJ23	HX255T
21	IO_L3N_21	AK23	HX255T
21	IO_L4P_21	BA25	HX255T
21	IO_L4N_VREF_21	BB25	HX255T
21	IO_L5P_21	AU26	HX255T
21	IO_L5N_21	AV26	HX255T
21	IO_L6P_21	AK22	HX255T
21	IO_L6N_21	AL23	HX255T
21	IO_L7P_21	AW25	HX255T
21	IO_L7N_21	AY25	HX255T
21	IO_L8P_SRCC_21	AP26	HX255T
21	IO_L8N_SRCC_21	AR26	HX255T
21	IO_L9P_MRCC_21	AL22	HX255T
21	IO_L9N_MRCC_21	AM22	HX255T
21	IO_L10P_MRCC_21	AV24	HX255T
21	IO_L10N_MRCC_21	AW24	HX255T
21	IO_L11P_SRCC_21	BB26	HX255T
21	IO_L11N_SRCC_21	BC26	HX255T
21	IO_L12P_VRN_21	AP25	HX255T
21	IO_L12N_VRP_21	AR25	HX255T
21	IO_L13P_21	AL25	HX255T
21	IO_L13N_21	AM25	HX255T
21	IO_L14P_21	BD25	HX255T
21	IO_L14N_VREF_21	BD26	HX255T
21	IO_L15P_21	AL24	HX255T

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
21	IO_L15N_21	AM24	HX255T
21	IO_L16P_21	BC24	HX255T
21	IO_L16N_21	BD24	HX255T
21	IO_L17P_21	AT24	HX255T
21	IO_L17N_21	AU24	HX255T
21	IO_L18P_21	AN24	HX255T
21	IO_L18N_21	AP24	HX255T
21	IO_L19P_21	BA24	HX255T
21	IO_L19N_21	BB24	HX255T
22	IO_L0P_22	AN29	HX255T
22	IO_L0N_22	AP29	HX255T
22	IO_L1P_22	AN28	HX255T
22	IO_L1N_22	AP28	HX255T
22	IO_L2P_22	AV29	HX255T
22	IO_L2N_22	AW29	HX255T
22	IO_L3P_22	AJ28	HX255T
22	IO_L3N_22	AK28	HX255T
22	IO_L4P_22	AR28	HX255T
22	IO_L4N_VREF_22	AT28	HX255T
22	IO_L5P_22	AT29	HX255T
22	IO_L5N_22	AU29	HX255T
22	IO_L6P_22	AL27	HX255T
22	IO_L6N_22	AL28	HX255T
22	IO_L7P_22	AR27	HX255T
22	IO_L7N_22	AT27	HX255T
22	IO_L8P_SRCC_22	AY28	HX255T
22	IO_L8N_SRCC_22	BA28	HX255T
22	IO_L9P_MRCC_22	AJ26	HX255T
22	IO_L9N_MRCC_22	AK27	HX255T
22	IO_L10P_MRCC_22	AU27	HX255T
22	IO_L10N_MRCC_22	AV27	HX255T
22	IO_L11P_SRCC_22	AV28	HX255T
22	IO_L11N_SRCC_22	AW28	HX255T

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
22	IO_L12P_VRN_22	AJ25	HX255T
22	IO_L12N_VRP_22	AK26	HX255T
22	IO_L13P_22	BA29	HX255T
22	IO_L13N_22	BB29	HX255T
22	IO_L14P_22	BC29	HX255T
22	IO_L14N_VREF_22	BD29	HX255T
22	IO_L15P_22	AM27	HX255T
22	IO_L15N_22	AN27	HX255T
22	IO_L16P_22	BB27	HX255T
22	IO_L16N_22	BC27	HX255T
22	IO_L17P_22	AY27	HX255T
22	IO_L17N_22	BA27	HX255T
22	IO_L18P_22	AJ24	HX255T
22	IO_L18N_22	AK25	HX255T
22	IO_L19P_22	BC28	HX255T
22	IO_L19N_22	BD28	HX255T
23	IO_L0P_23	AN31	
23	IO_L0N_23	AN32	
23	IO_L1P_23	AP31	
23	IO_L1N_23	AR32	
23	IO_L2P_23	AU32	
23	IO_L2N_23	AV32	
23	IO_L3P_23	AJ30	
23	IO_L3N_23	AJ31	
23	IO_L4P_23	AT30	
23	IO_L4N_VREF_23	AU30	
23	IO_L5P_23	AP30	
23	IO_L5N_23	AR30	
23	IO_L6P_23	AK31	
23	IO_L6N_23	AL32	
23	IO_L7P_23	AR31	
23	IO_L7N_23	AT32	
23	IO_L8P_SRCC_23	AW31	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
23	IO_L8N_SRCC_23	AY31	
23	IO_L9P_MRCC_23	AJ29	
23	IO_L9N_MRCC_23	AK30	
23	IO_L10P_MRCC_23	BA30	
23	IO_L10N_MRCC_23	BB30	
23	IO_L11P_SRCC_23	AU31	
23	IO_L11N_SRCC_23	AV31	
23	IO_L12P_VRN_23	AM31	
23	IO_L12N_VRP_23	AM32	
23	IO_L13P_23	AY32	
23	IO_L13N_23	BA32	
23	IO_L14P_23	BB32	
23	IO_L14N_VREF_23	BC32	
23	IO_L15P_23	AL30	
23	IO_L15N_23	AM30	
23	IO_L16P_23	BD30	
23	IO_L16N_23	BD31	
23	IO_L17P_23	AW30	
23	IO_L17N_23	AY30	
23	IO_L18P_23	AL29	
23	IO_L18N_23	AM29	
23	IO_L19P_23	BB31	
23	IO_L19N_23	BC31	
24	IO_L0P_GC_24	AN33	
24	IO_L0N_GC_24	AP34	
24	IO_L1P_GC_24	AP33	
24	IO_L1N_GC_24	AR33	
24	IO_L2P_D15_24	AP35	
24	IO_L2N_D14_24	AR35	
24	IO_L3P_D13_24	AH32	
24	IO_L3N_D12_24	AH33	
24	IO_L4P_D11_24	AT35	
24	IO_L4N_VREF_D10_24	AU35	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
24	IO_L5P_D9_24	AT33	
24	IO_L5N_D8_24	AT34	
24	IO_L6P_D7_24	AJ33	
24	IO_L6N_D6_24	AK33	
24	IO_L7P_D5_24	AU34	
24	IO_L7N_D4_24	AV34	
24	IO_L8P_SRCC_24	AV33	
24	IO_L8N_SRCC_24	AW34	
24	IO_L9P_MRCC_24	AK35	
24	IO_L9N_MRCC_24	AL35	
24	IO_L10P_MRCC_24	AW33	
24	IO_L10N_MRCC_24	AY33	
24	IO_L11P_SRCC_24	AW35	
24	IO_L11N_SRCC_24	AY35	
24	IO_L12P_D3_24	AL34	
24	IO_L12N_D2_FS2_24	AM35	
24	IO_L13P_D1_FS1_24	BA35	
24	IO_L13N_D0_FS0_24	BB35	
24	IO_L14P_FCS_B_24	BB34	
24	IO_L14N_VREF_FOE_B_MOSI_24	BC34	
24	IO_L15P_FWE_B_24	AM34	
24	IO_L15N_RS1_24	AN34	
24	IO_L16P_RS0_24	BD34	
24	IO_L16N_CSO_B_24	BD35	
24	IO_L17P_VRN_24	BA33	
24	IO_L17N_VRP_24	BA34	
24	IO_L18P_24	AK32	
24	IO_L18N_24	AL33	
24	IO_L19P_24	BC33	
24	IO_L19N_24	BD33	
25	IO_L0P_25	A34	
25	IO_L0N_25	A35	
25	IO_L1P_25	B35	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
25	IO_L1N_25	B36	
25	IO_L2P_SM8P_25	B37	
25	IO_L2N_SM8N_25	A37	
25	IO_L3P_SM9P_25	L33	
25	IO_L3N_SM9N_25	K33	
25	IO_L4P_25	P34	
25	IO_L4N_VREF_25	P35	
25	IO_L5P_SM10P_25	E35	
25	IO_L5N_SM10N_25	D35	
25	IO_L6P_SM11P_25	K35	
25	IO_L6N_SM11N_25	J35	
25	IO_L7P_SM12P_25	C34	
25	IO_L7N_SM12N_25	B34	
25	IO_L8P_SRCC_25	D33	
25	IO_L8N_SRCC_25	D34	
25	IO_L9P_MRCC_25	N33	
25	IO_L9N_MRCC_25	N34	
25	IO_L10P_MRCC_25	M35	
25	IO_L10N_MRCC_25	L35	
25	IO_L11P_SRCC_25	G35	
25	IO_L11N_SRCC_25	F35	
25	IO_L12P_SM13P_25	P31	
25	IO_L12N_SM13N_25	N32	
25	IO_L13P_SM14P_25	F33	
25	IO_L13N_SM14N_25	E33	
25	IO_L14P_25	G34	
25	IO_L14N_VREF_25	F34	
25	IO_L15P_SM15P_25	R33	
25	IO_L15N_SM15N_25	P33	
25	IO_L16P_VRN_25	M34	
25	IO_L16N_VRP_25	L34	
25	IO_L17P_25	J34	
25	IO_L17N_25	H34	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
25	IO_L18P_GC_25	R31	
25	IO_L18N_GC_25	R32	
25	IO_L19P_GC_25	J33	
25	IO_L19N_GC_25	H33	
26	IO_L0P_26	B31	
26	IO_L0N_26	A32	
26	IO_L1P_26	B30	
26	IO_L1N_26	A30	
26	IO_L2P_26	C32	
26	IO_L2N_26	C33	
26	IO_L3P_26	M30	
26	IO_L3N_26	M31	
26	IO_L4P_26	E30	
26	IO_L4N_VREF_26	D30	
26	IO_L5P_26	B32	
26	IO_L5N_26	A33	
26	IO_L6P_26	N29	
26	IO_L6N_26	M29	
26	IO_L7P_26	D31	
26	IO_L7N_26	C31	
26	IO_L8P_SRCC_26	G31	
26	IO_L8N_SRCC_26	F32	
26	IO_L9P_MRCC_26	R28	
26	IO_L9N_MRCC_26	P29	
26	IO_L10P_MRCC_26	J31	
26	IO_L10N_MRCC_26	H32	
26	IO_L11P_SRCC_26	E31	
26	IO_L11N_SRCC_26	E32	
26	IO_L12P_VRN_26	N31	
26	IO_L12N_VRP_26	M32	
26	IO_L13P_26	G30	
26	IO_L13N_26	F30	
26	IO_L14P_26	L30	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
26	IO_L14N_VREF_26	K31	
26	IO_L15P_26	R30	
26	IO_L15N_26	P30	
26	IO_L16P_26	L32	
26	IO_L16N_26	K32	
26	IO_L17P_26	H31	
26	IO_L17N_26	G32	
26	IO_L18P_26	T29	
26	IO_L18N_26	T30	
26	IO_L19P_26	K30	
26	IO_L19N_26	J30	
27	IO_L0P_27	B27	
27	IO_L0N_27	A27	
27	IO_L1P_27	A28	
27	IO_L1N_27	A29	
27	IO_L2P_27	C27	
27	IO_L2N_27	C28	
27	IO_L3P_27	N26	
27	IO_L3N_27	M26	
27	IO_L4P_27	F27	
27	IO_L4N_VREF_27	E27	
27	IO_L5P_27	C29	
27	IO_L5N_27	B29	
27	IO_L6P_27	N27	
27	IO_L6N_27	M27	
27	IO_L7P_27	F28	
27	IO_L7N_27	E28	
27	IO_L8P_SRCC_27	D28	
27	IO_L8N_SRCC_27	D29	
27	IO_L9P_MRCC_27	R25	
27	IO_L9N_MRCC_27	P25	
27	IO_L10P_MRCC_27	G29	
27	IO_L10N_MRCC_27	F29	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
27	IO_L11P_SRCC_27	H27	
27	IO_L11N_SRCC_27	G27	
27	IO_L12P_VRN_27	R26	
27	IO_L12N_VRP_27	P26	
27	IO_L13P_27	K26	
27	IO_L13N_27	K27	
27	IO_L14P_27	L27	
27	IO_L14N_VREF_27	K28	
27	IO_L15P_27	P28	
27	IO_L15N_27	N28	
27	IO_L16P_27	L28	
27	IO_L16N_27	L29	
27	IO_L17P_27	H28	
27	IO_L17N_27	H29	
27	IO_L18P_27	T27	
27	IO_L18N_27	R27	
27	IO_L19P_27	J28	
27	IO_L19N_27	J29	
28	IO_L0P_28	F23	
28	IO_L0N_28	F24	
28	IO_L1P_28	E23	
28	IO_L1N_28	D24	
28	IO_L2P_28	C26	
28	IO_L2N_28	B26	
28	IO_L3P_28	L23	
28	IO_L3N_28	K23	
28	IO_L4P_28	D23	
28	IO_L4N_VREF_28	C24	
28	IO_L5P_28	C23	
28	IO_L5N_28	B24	
28	IO_L6P_28	L24	
28	IO_L6N_28	L25	
28	IO_L7P_28	B25	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
28	IO_L7N_28	A25	
28	IO_L8P_SRCC_28	A23	
28	IO_L8N_SRCC_28	A24	
28	IO_L9P_MRCC_28	M24	
28	IO_L9N_MRCC_28	M25	
28	IO_L10P_MRCC_28	E25	
28	IO_L10N_MRCC_28	D25	
28	IO_L11P_SRCC_28	E26	
28	IO_L11N_SRCC_28	D26	
28	IO_L12P_VRN_28	K25	
28	IO_L12N_VRP_28	J25	
28	IO_L13P_28	J23	
28	IO_L13N_28	H23	
28	IO_L14P_28	G25	
28	IO_L14N_VREF_28	G26	
28	IO_L15P_28	P23	
28	IO_L15N_28	P24	
28	IO_L16P_28	J24	
28	IO_L16N_28	H24	
28	IO_L17P_28	G24	
28	IO_L17N_28	F25	
28	IO_L18P_28	N23	
28	IO_L18N_28	N24	
28	IO_L19P_28	J26	
28	IO_L19N_28	H26	
30	IO_L0P_30	AR18	HX255T
30	IO_L0N_30	AT18	HX255T
30	IO_L1P_30	AT19	HX255T
30	IO_L1N_30	AU19	HX255T
30	IO_L2P_30	AU17	HX255T
30	IO_L2N_30	AV17	HX255T
30	IO_L3P_30	AP20	HX255T
30	IO_L3N_30	AP19	HX255T

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
30	IO_L4P_30	BA17	HX255T
30	IO_L4N_VREF_30	BB17	HX255T
30	IO_L5P_30	AV18	HX255T
30	IO_L5N_30	AW18	HX255T
30	IO_L6P_30	AP21	HX255T
30	IO_L6N_30	AR20	HX255T
30	IO_L7P_30	AY18	HX255T
30	IO_L7N_30	BA18	HX255T
30	IO_L8P_SRCC_30	BB12	HX255T
30	IO_L8N_SRCC_30	BC11	HX255T
30	IO_L9P_MRCC_30	AT17	HX255T
30	IO_L9N_MRCC_30	AU16	HX255T
30	IO_L10P_MRCC_30	BC13	HX255T
30	IO_L10N_MRCC_30	BC12	HX255T
30	IO_L11P_SRCC_30	BB16	HX255T
30	IO_L11N_SRCC_30	BB15	HX255T
30	IO_L12P_VRN_30	AV16	HX255T
30	IO_L12N_VRP_30	AW16	HX255T
30	IO_L13P_30	BD11	HX255T
30	IO_L13N_30	BD10	HX255T
30	IO_L14P_30	BD14	HX255T
30	IO_L14N_VREF_30	BD13	HX255T
30	IO_L15P_30	AY17	HX255T
30	IO_L15N_30	AY16	HX255T
30	IO_L16P_30	BC17	HX255T
30	IO_L16N_30	BD16	HX255T
30	IO_L17P_30	BC16	HX255T
30	IO_L17N_30	BD15	HX255T
30	IO_L18P_30	BB14	HX255T
30	IO_L18N_30	BC14	HX255T
30	IO_L19P_30	BC18	HX255T
30	IO_L19N_30	BD18	HX255T
31	IO_L0P_31	AN16	HX255T

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
31	IO_L0N_31	AP15	HX255T
31	IO_L1P_31	AL18	HX255T
31	IO_L1N_31	AM17	HX255T
31	IO_L2P_31	AP16	HX255T
31	IO_L2N_31	AR16	HX255T
31	IO_L3P_31	AJ21	HX255T
31	IO_L3N_31	AK21	HX255T
31	IO_L4P_31	AN18	HX255T
31	IO_L4N_VREF_31	AN17	HX255T
31	IO_L5P_31	AM19	HX255T
31	IO_L5N_31	AN19	HX255T
31	IO_L6P_31	AJ18	HX255T
31	IO_L6N_31	AK18	HX255T
31	IO_L7P_31	AP18	HX255T
31	IO_L7N_31	AR17	HX255T
31	IO_L8P_SRCC_31	AR15	HX255T
31	IO_L8N_SRCC_31	AT15	HX255T
31	IO_L9P_MRCC_31	AJ20	HX255T
31	IO_L9N_MRCC_31	AJ19	HX255T
31	IO_L10P_MRCC_31	AT14	HX255T
31	IO_L10N_MRCC_31	AT13	HX255T
31	IO_L11P_SRCC_31	AU15	HX255T
31	IO_L11N_SRCC_31	AV14	HX255T
31	IO_L12P_VRN_31	AK20	HX255T
31	IO_L12N_VRP_31	AL19	HX255T
31	IO_L13P_31	AW15	HX255T
31	IO_L13N_31	AW14	HX255T
31	IO_L14P_31	AU14	HX255T
31	IO_L14N_VREF_31	AV13	HX255T
31	IO_L15P_31	AL20	HX255T
31	IO_L15N_31	AM20	HX255T
31	IO_L16P_31	AW13	HX255T
31	IO_L16N_31	AY13	HX255T

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
31	IO_L17P_31	BA14	HX255T
31	IO_L17N_31	BA13	HX255T
31	IO_L18P_31	AM21	HX255T
31	IO_L18N_31	AN21	HX255T
31	IO_L19P_31	AY15	HX255T
31	IO_L19N_31	BA15	HX255T
32	IO_L0P_32	BA10	HX255T
32	IO_L0N_32	BB9	HX255T
32	IO_L1P_32	AY10	HX255T
32	IO_L1N_32	BA9	HX255T
32	IO_L2P_32	BB7	HX255T
32	IO_L2N_32	BB6	HX255T
32	IO_L3P_32	BB10	HX255T
32	IO_L3N_32	BC9	HX255T
32	IO_L4P_32	AY12	HX255T
32	IO_L4N_VREF_32	AY11	HX255T
32	IO_L5P_32	BA8	HX255T
32	IO_L5N_32	BA7	HX255T
32	IO_L6P_32	BA12	HX255T
32	IO_L6N_32	BB11	HX255T
32	IO_L7P_32	AW5	HX255T
32	IO_L7N_32	AY5	HX255T
32	IO_L8P_SRCC_32	BB5	HX255T
32	IO_L8N_SRCC_32	BB4	HX255T
32	IO_L9P_MRCC_32	BC6	HX255T
32	IO_L9N_MRCC_32	BD6	HX255T
32	IO_L10P_MRCC_32	BC8	HX255T
32	IO_L10N_MRCC_32	BC7	HX255T
32	IO_L11P_SRCC_32	BA5	HX255T
32	IO_L11N_SRCC_32	BA4	HX255T
32	IO_L12P_VRN_32	BD9	HX255T
32	IO_L12N_VRP_32	BD8	HX255T
32	IO_L13P_32	AY3	HX255T

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
32	IO_L13N_32	BA3	HX255T
32	IO_L14P_32	BC3	HX255T
32	IO_L14N_VREF_32	BC2	HX255T
32	IO_L15P_32	BC4	HX255T
32	IO_L15N_32	BD3	HX255T
32	IO_L16P_32	BB2	HX255T
32	IO_L16N_32	BB1	HX255T
32	IO_L17P_32	AY2	HX255T
32	IO_L17N_32	BA2	HX255T
32	IO_L18P_32	BD5	HX255T
32	IO_L18N_32	BD4	HX255T
32	IO_L19P_32	AW1	HX255T
32	IO_L19N_32	AY1	HX255T
33	IO_L0P_33	AL14	
33	IO_L0N_33	AM14	
33	IO_L1P_33	AK15	
33	IO_L1N_33	AL15	
33	IO_L2P_33	AK17	
33	IO_L2N_33	AK16	
33	IO_L3P_33	AJ16	
33	IO_L3N_33	AJ15	
33	IO_L4P_33	AU9	
33	IO_L4N_VREF_33	AV8	
33	IO_L5P_33	AN13	
33	IO_L5N_33	AN12	
33	IO_L6P_33	AM15	
33	IO_L6N_33	AN14	
33	IO_L7P_33	AP11	
33	IO_L7N_33	AR11	
33	IO_L8P_SRCC_33	AV7	
33	IO_L8N_SRCC_33	AW6	
33	IO_L9P_MRCC_33	AP13	
33	IO_L9N_MRCC_33	AR12	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
33	IO_L10P_MRCC_33	AU11	
33	IO_L10N_MRCC_33	AU10	
33	IO_L11P_SRCC_33	AV9	
33	IO_L11N_SRCC_33	AW8	
33	IO_L12P_VRN_33	AP14	
33	IO_L12N_VRP_33	AR13	
33	IO_L13P_33	AW9	
33	IO_L13N_33	AY8	
33	IO_L14P_33	AV11	
33	IO_L14N_VREF_33	AW10	
33	IO_L15P_33	AU7	
33	IO_L15N_33	AV6	
33	IO_L16P_33	AL17	
33	IO_L16N_33	AM16	
33	IO_L17P_33	AY7	
33	IO_L17N_33	AY6	
33	IO_L18P_33	AV12	
33	IO_L18N_33	AW11	
33	IO_L19P_33	AT12	
33	IO_L19N_33	AU12	
34	IO_L0P_GC_34	AK13	
34	IO_L0N_GC_34	AK12	
34	IO_L1P_GC_34	AL13	
34	IO_L1N_GC_34	AL12	
34	IO_L2P_A15_D31_34	AK11	
34	IO_L2N_A14_D30_34	AK10	
34	IO_L3P_A13_D29_34	AH13	
34	IO_L3N_A12_D28_34	AH12	
34	IO_L4P_A11_D27_34	AL10	
34	IO_L4N_VREF_A10_D26_34	AM10	
34	IO_L5P_A09_D25_34	AM12	
34	IO_L5N_A08_D24_34	AM11	
34	IO_L6P_A07_D23_34	AJ14	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
34	IO_L6N_A06_D22_34	AJ13	
34	IO_L7P_A05_D21_34	AT9	
34	IO_L7N_A04_D20_34	AT8	
34	IO_L8P_SRCC_34	AN11	
34	IO_L8N_SRCC_34	AP10	
34	IO_L9P_MRCC_34	AR7	
34	IO_L9N_MRCC_34	AR6	
34	IO_L10P_MRCC_34	AR8	
34	IO_L10N_MRCC_34	AT7	
34	IO_L11P_SRCC_34	AU6	
34	IO_L11N_SRCC_34	AU5	
34	IO_L12P_A03_D19_34	AR5	
34	IO_L12N_A02_D18_34	AT4	
34	IO_L13P_A01_D17_34	AU2	
34	IO_L13N_A00_D16_34	AU1	
34	IO_L14P_A25_34	AT5	
34	IO_L14N_VREF_A24_34	AU4	
34	IO_L15P_A23_34	AT3	
34	IO_L15N_A22_34	AT2	
34	IO_L16P_A21_34	AV2	
34	IO_L16N_A20_34	AV1	
34	IO_L17P_A19_34	AW4	
34	IO_L17N_A18_34	AW3	
34	IO_L18P_A17_34	AV4	
34	IO_L18N_A16_34	AV3	
34	IO_L19P_VRN_34	AR10	
34	IO_L19N_VRP_34	AT10	
35	IO_L0P_35	C12	
35	IO_L0N_35	C11	
35	IO_L1P_35	A13	
35	IO_L1N_35	A12	
35	IO_L2P_SM0P_35	B11	
35	IO_L2N_SM0N_35	A10	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
35	IO_L3P_SM1P_35	R13	
35	IO_L3N_SM1N_35	R12	
35	IO_L4P_35	B9	
35	IO_L4N_VREF_35	A8	
35	IO_L5P_SM2P_35	C13	
35	IO_L5N_SM2N_35	B12	
35	IO_L6P_SM3P_35	H11	
35	IO_L6N_SM3N_35	G10	
35	IO_L7P_SM4P_35	B10	
35	IO_L7N_SM4N_35	A9	
35	IO_L8P_SRCC_35	E12	
35	IO_L8N_SRCC_35	D11	
35	IO_L9P_MRCC_35	K11	
35	IO_L9N_MRCC_35	J11	
35	IO_L10P_MRCC_35	G12	
35	IO_L10N_MRCC_35	F12	
35	IO_L11P_SRCC_35	K10	
35	IO_L11N_SRCC_35	J10	
35	IO_L12P_SM5P_35	P11	
35	IO_L12N_SM5N_35	P10	
35	IO_L13P_SM6P_35	F10	
35	IO_L13N_SM6N_35	E10	
35	IO_L14P_35	E11	
35	IO_L14N_VREF_35	D10	
35	IO_L15P_SM7P_35	M11	
35	IO_L15N_SM7N_35	L10	
35	IO_L16P_VRN_35	L12	
35	IO_L16N_VRP_35	K12	
35	IO_L17P_35	H12	
35	IO_L17N_35	G11	
35	IO_L18P_GC_35	N11	
35	IO_L18N_GC_35	M10	
35	IO_L19P_GC_35	N12	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
35	IO_L19N_GC_35	M12	
36	IO_L0P_36	B17	
36	IO_L0N_36	A17	
36	IO_L1P_36	B15	
36	IO_L1N_36	A15	
36	IO_L2P_36	C16	
36	IO_L2N_36	B16	
36	IO_L3P_36	G15	
36	IO_L3N_36	F15	
36	IO_L4P_36	D14	
36	IO_L4N_VREF_36	C14	
36	IO_L5P_36	B14	
36	IO_L5N_36	A14	
36	IO_L6P_36	F14	
36	IO_L6N_36	F13	
36	IO_L7P_36	E16	
36	IO_L7N_36	D16	
36	IO_L8P_SRCC_36	J14	
36	IO_L8N_SRCC_36	H13	
36	IO_L9P_MRCC_36	P15	
36	IO_L9N_MRCC_36	P14	
36	IO_L10P_MRCC_36	P13	
36	IO_L10N_MRCC_36	N13	
36	IO_L11P_SRCC_36	E15	
36	IO_L11N_SRCC_36	D15	
36	IO_L12P_VRN_36	N14	
36	IO_L12N_VRP_36	M14	
36	IO_L13P_36	H14	
36	IO_L13N_36	G14	
36	IO_L14P_36	K13	
36	IO_L14N_VREF_36	J13	
36	IO_L15P_36	T15	
36	IO_L15N_36	R15	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
36	IO_L16P_36	M15	
36	IO_L16N_36	L15	
36	IO_L17P_36	E13	
36	IO_L17N_36	D13	
36	IO_L18P_36	L14	
36	IO_L18N_36	L13	
36	IO_L19P_36	K15	
36	IO_L19N_36	J15	
37	IO_L0P_37	H19	
37	IO_L0N_37	G19	
37	IO_L1P_37	D19	
37	IO_L1N_37	C19	
37	IO_L2P_37	E18	
37	IO_L2N_37	D18	
37	IO_L3P_37	M19	
37	IO_L3N_37	L19	
37	IO_L4P_37	F17	
37	IO_L4N_VREF_37	E17	
37	IO_L5P_37	C18	
37	IO_L5N_37	C17	
37	IO_L6P_37	P19	
37	IO_L6N_37	N19	
37	IO_L7P_37	F19	
37	IO_L7N_37	F18	
37	IO_L8P_SRCC_37	H18	
37	IO_L8N_SRCC_37	G17	
37	IO_L9P_MRCC_37	R18	
37	IO_L9N_MRCC_37	P18	
37	IO_L10P_MRCC_37	L18	
37	IO_L10N_MRCC_37	K18	
37	IO_L11P_SRCC_37	J19	
37	IO_L11N_SRCC_37	J18	
37	IO_L12P_VRN_37	N18	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
37	IO_L12N_VRP_37	N17	
37	IO_L13P_37	H17	
37	IO_L13N_37	G16	
37	IO_L14P_37	J16	
37	IO_L14N_VREF_37	H16	
37	IO_L15P_37	T17	
37	IO_L15N_37	R17	
37	IO_L16P_37	N16	
37	IO_L16N_37	M16	
37	IO_L17P_37	K17	
37	IO_L17N_37	K16	
37	IO_L18P_37	M17	
37	IO_L18N_37	L17	
37	IO_L19P_37	R16	
37	IO_L19N_37	P16	
38	IO_L0P_38	K22	
38	IO_L0N_38	J21	
38	IO_L1P_38	C22	
38	IO_L1N_38	C21	
38	IO_L2P_38	E22	
38	IO_L2N_38	D21	
38	IO_L3P_38	M22	
38	IO_L3N_38	L22	
38	IO_L4P_38	B19	
38	IO_L4N_VREF_38	A18	
38	IO_L5P_38	B20	
38	IO_L5N_38	A19	
38	IO_L6P_38	M21	
38	IO_L6N_38	M20	
38	IO_L7P_38	B22	
38	IO_L7N_38	A22	
38	IO_L8P_SRCC_38	B21	
38	IO_L8N_SRCC_38	A20	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
38	IO_L9P_MRCC_38	N22	
38	IO_L9N_MRCC_38	N21	
38	IO_L10P_MRCC_38	H22	
38	IO_L10N_MRCC_38	G21	
38	IO_L11P_SRCC_38	E21	
38	IO_L11N_SRCC_38	D20	
38	IO_L12P_VRN_38	R20	
38	IO_L12N_VRP_38	P20	
38	IO_L13P_38	G22	
38	IO_L13N_38	F22	
38	IO_L14P_38	L20	
38	IO_L14N_VREF_38	K20	
38	IO_L15P_38	R23	
38	IO_L15N_38	R22	
38	IO_L16P_38	F20	
38	IO_L16N_38	E20	
38	IO_L17P_38	H21	
38	IO_L17N_38	G20	
38	IO_L18P_38	R21	
38	IO_L18N_38	P21	
38	IO_L19P_38	K21	
38	IO_L19N_38	J20	
100	MGTTXN3_100	AV43	HX255T
100	MGTRXN3_100	BA41	HX255T
100	MGTTXP3_100	AV44	HX255T
100	MGTRXP3_100	BA42	HX255T
100	MGTTXN2_100	AW41	HX255T
100	MGTRXN2_100	BB39	HX255T
100	MGTTXP2_100	AW42	HX255T
100	MGTRXP2_100	AW37	HX255T
100	MGTRXP2_100	AW38	HX255T
100	MGTRXP2_100	BB40	HX255T
100	MGTRXP2_100	BA37	HX255T

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
100	MGTREFCLK0N_100	BA38	HX255T
100	MGTTXN1_100	AY43	HX255T
100	MGTRXN1_100	BC41	HX255T
100	MGTTXP1_100	AY44	HX255T
100	MGTRXP1_100	BC42	HX255T
100	MGTTXN0_100	BB43	HX255T
100	MGTRXN0_100	BD39	HX255T
100	MGTTXP0_100	BB44	HX255T
100	MGTRXP0_100	BD40	HX255T
101	MGTTXN3_101	AP43	HX255T
101	MGTRXN3_101	AP39	HX255T
101	MGTTXP3_101	AP44	HX255T
101	MGTRXP3_101	AP40	HX255T
101	MGTTXN2_101	AR41	HX255T
101	MGTRXN2_101	AT39	HX255T
101	MGTTXP2_101	AR42	HX255T
101	MGTREFCLK1P_101	AR37	HX255T
101	MGTREFCLK1N_101	AR38	HX255T
101	MGTRXP2_101	AT40	HX255T
101	MGTREFCLK0P_101	AU37	HX255T
101	MGTREFCLK0N_101	AU38	HX255T
101	MGTTXN1_101	AT43	HX255T
101	MGTRXN1_101	AV39	HX255T
101	MGTTXP1_101	AT44	HX255T
101	MGTRXP1_101	AV40	HX255T
101	MGTTXN0_101	AU41	HX255T
101	MGTRXN0_101	AY39	HX255T
101	MGTTXP0_101	AU42	HX255T
101	MGTRXP0_101	AY40	HX255T
102	MGTTXN3_102	AK43	HX255T
102	MGTRXN3_102	AK39	HX255T
102	MGTTXP3_102	AK44	HX255T
102	MGTRXP3_102	AK40	HX255T

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
102	MGTTXN2_102	AL41	HX255T
102	MGTRXN2_102	AJ37	HX255T
102	MGTTXP2_102	AL42	HX255T
102	MGTREFCLK1P_102	AH35	HX255T
102	MGTREFCLK1N_102	AH36	HX255T
102	MGTRXP2_102	AJ38	HX255T
102	MGTREFCLK0P_102	AN37	HX255T
102	MGTREFCLK0N_102	AN38	HX255T
102	MGTTXN1_102	AM43	HX255T
102	MGTRXN1_102	AM39	HX255T
102	MGTTXP1_102	AM44	HX255T
102	MGTRXP1_102	AM40	HX255T
102	MGTTXN0_102	AN41	HX255T
102	MGTRXN0_102	AL37	HX255T
102	MGTTXP0_102	AN42	HX255T
102	MGTRXP0_102	AL38	HX255T
103	MGTTXN3_103	AF43	
103	MGTRXN3_103	AE37	
103	MGTTXP3_103	AF44	
103	MGTRXP3_103	AE38	
103	MGTTXN2_103	AG41	
103	MGTRXN2_103	AF39	
103	MGTTXP2_103	AG42	
103	MGTREFCLK1P_103	AD35	
103	MGTREFCLK1N_103	AD36	
103	MGTRXP2_103	AF40	
103	MGTREFCLK0P_103	AF35	
103	MGTREFCLK0N_103	AF36	
103	MGTTXN1_103	AH43	
103	MGTRXN1_103	AG37	
103	MGTTXP1_103	AH44	
103	MGTRXP1_103	AG38	
103	MGTTXN0_103	AJ41	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
103	MGTRXN0_103	AH39	
103	MGTTP0_103	AJ42	
103	MGTRXP0_103	AH40	
104	MGTTXN3_104	AB43	
104	MGTRXN3_104	AA37	
104	MGTTP3_104	AB44	
104	MGTRXP3_104	AA38	
104	MGTTXN2_104	AC41	
104	MGTRXN2_104	AB39	
104	MGTTP2_104	AC42	
104	MGTREFCLK1P_104	Y35	
104	MGTREFCLK1N_104	Y36	
104	MGTRXP2_104	AB40	
104	MGTREFCLK0P_104	AB35	
104	MGTREFCLK0N_104	AB36	
104	MGTTXN1_104	AD43	
104	MGTRXN1_104	AC37	
104	MGTTP1_104	AD44	
104	MGTRXP1_104	AC38	
104	MGTTXN0_104	AE41	
104	MGTRXN0_104	AD39	
104	MGTTP0_104	AE42	
104	MGTRXP0_104	AD40	
105	MGTTXN3_105	V43	
105	MGTRXN3_105	U37	
105	MGTTP3_105	V44	
105	MGTRXP3_105	U38	
105	MGTTXN2_105	W41	
105	MGTRXN2_105	V39	
105	MGTTP2_105	W42	
105	MGTREFCLK1P_105	T35	
105	MGTREFCLK1N_105	T36	
105	MGTRXP2_105	V40	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
105	MGTAVTTRCAL_105	BC37	
105	MGTRREF_105	BC38	
105	MGTREFCLK0P_105	V35	
105	MGTREFCLK0N_105	V36	
105	MGTTXN1_105	Y43	
105	MGTRXN1_105	W37	
105	MGTTXP1_105	Y44	
105	MGTRXP1_105	W38	
105	MGTTXN0_105	AA41	
105	MGTRXN0_105	Y39	
105	MGTTXP0_105	AA42	
105	MGTRXP0_105	Y40	
106	MGTRXP2_106	N37	
106	MGTRXN2_106	N38	
106	MGTTXP2_106	M43	
106	MGTTXN2_106	M44	
106	MGTRXP3_106	M39	
106	MGTRXN3_106	M40	
106	MGTTXP3_106	N41	
106	MGTTXN3_106	N42	
106	MGTRBIAS_106	R38	
106	MGTREFCLKP_106	R41	
106	MGTREFCLKN_106	R42	
106	MGTRXP1_106	T39	
106	MGTRXN1_106	T40	
106	MGTTXP1_106	P43	
106	MGTTXN1_106	P44	
106	MGTRXP0_106	U41	
106	MGTRXN0_106	U42	
106	MGTTXP0_106	T43	
106	MGTTXN0_106	T44	
107	MGTRXP2_107	H39	
107	MGTRXN2_107	H40	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
107	MGTTXP2_107	G41	
107	MGTTXN2_107	G42	
107	MGTRXP3_107	J37	
107	MGTRXN3_107	J38	
107	MGTTXP3_107	H43	
107	MGTTXN3_107	H44	
107	MGTRBIAS_107	E37	
107	MGTRREFCLKP_107	J41	
107	MGTRREFCLKN_107	J42	
107	MGTRXP1_107	L37	
107	MGTRXN1_107	L38	
107	MGTTXP1_107	K43	
107	MGTTXN1_107	K44	
107	MGTRXP0_107	K39	
107	MGTRXN0_107	K40	
107	MGTTXP0_107	L41	
107	MGTTXN0_107	L42	
108	MGTRXP2_108	B39	
108	MGTRXN2_108	B40	
108	MGTTXP2_108	A41	
108	MGTTXN2_108	A42	
108	MGTRXP3_108	D39	
108	MGTRXN3_108	D40	
108	MGTTXP3_108	C41	
108	MGTTXN3_108	C42	
108	MGTRBIAS_108	D37	
108	MGTRREFCLKP_108	E41	
108	MGTRREFCLKN_108	E42	
108	MGTRXP1_108	F39	
108	MGTRXN1_108	F40	
108	MGTTXP1_108	D43	
108	MGTTXN1_108	D44	
108	MGTRXP0_108	G37	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
108	MGTRXN0_108	G38	
108	MGTTXP0_108	F43	
108	MGTTXN0_108	F44	
112	MGTTXN3_112	AK2	HX255T
112	MGTRXN3_112	AK6	HX255T
112	MGTTXP3_112	AK1	HX255T
112	MGTRXP3_112	AK5	HX255T
112	MGTTXN2_112	AL4	HX255T
112	MGTRXN2_112	AJ8	HX255T
112	MGTTXP2_112	AL3	HX255T
112	MGTREFCLK1P_112	AH10	HX255T
112	MGTREFCLK1N_112	AH9	HX255T
112	MGTRXP2_112	AJ7	HX255T
112	MGTREFCLK0P_112	AN8	HX255T
112	MGTREFCLK0N_112	AN7	HX255T
112	MGTTXN1_112	AM2	HX255T
112	MGTRXN1_112	AM6	HX255T
112	MGTTXP1_112	AM1	HX255T
112	MGTRXP1_112	AM5	HX255T
112	MGTTXN0_112	AN4	HX255T
112	MGTRXN0_112	AL8	HX255T
112	MGTTXP0_112	AN3	HX255T
112	MGTRXP0_112	AL7	HX255T
113	MGTTXN3_113	AF2	
113	MGTRXN3_113	AE8	
113	MGTTXP3_113	AF1	
113	MGTRXP3_113	AE7	
113	MGTTXN2_113	AG4	
113	MGTRXN2_113	AF6	
113	MGTTXP2_113	AG3	
113	MGTREFCLK1P_113	AD10	
113	MGTREFCLK1N_113	AD9	
113	MGTRXP2_113	AF5	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
113	MGTREFCLK0P_113	AF10	
113	MGTREFCLK0N_113	AF9	
113	MGTTXN1_113	AH2	
113	MGTRXN1_113	AG8	
113	MGTTXP1_113	AH1	
113	MGTRXP1_113	AG7	
113	MGTTXN0_113	AJ4	
113	MGTRXN0_113	AH6	
113	MGTTXP0_113	AJ3	
113	MGTRXP0_113	AH5	
114	MGTTXN3_114	AB2	
114	MGTRXN3_114	AA8	
114	MGTTXP3_114	AB1	
114	MGTRXP3_114	AA7	
114	MGTTXN2_114	AC4	
114	MGTRXN2_114	AB6	
114	MGTTXP2_114	AC3	
114	MGTREFCLK1P_114	Y10	
114	MGTREFCLK1N_114	Y9	
114	MGTRXP2_114	AB5	
114	MGTREFCLK0P_114	AB10	
114	MGTREFCLK0N_114	AB9	
114	MGTTXN1_114	AD2	
114	MGTRXN1_114	AC8	
114	MGTTXP1_114	AD1	
114	MGTRXP1_114	AC7	
114	MGTTXN0_114	AE4	
114	MGTRXN0_114	AD6	
114	MGTTXP0_114	AE3	
114	MGTRXP0_114	AD5	
115	MGTTXN3_115	V2	
115	MGTRXN3_115	U8	
115	MGTTXP3_115	V1	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
115	MGTRXP3_115	U7	
115	MGT TXN2_115	W4	
115	MGT RXN2_115	V6	
115	MGT TXP2_115	W3	
115	MGT REFCLK1P_115	T10	
115	MGT REFCLK1N_115	T9	
115	MGTRXP2_115	V5	
115	MGT AVTTRCAL_115	AP2	
115	MGT RREF_115	AP1	
115	MGT REFCLK0P_115	V10	
115	MGT REFCLK0N_115	V9	
115	MGT TXN1_115	Y2	
115	MGT RXN1_115	W8	
115	MGT TXP1_115	Y1	
115	MGTRXP1_115	W7	
115	MGT TXN0_115	AA4	
115	MGT RXN0_115	Y6	
115	MGT TXP0_115	AA3	
115	MGTRXP0_115	Y5	
116	MGTRXP2_116	N8	
116	MGT RXN2_116	N7	
116	MGT TXP2_116	M2	
116	MGT TXN2_116	M1	
116	MGTRXP3_116	M6	
116	MGT RXN3_116	M5	
116	MGT TXP3_116	N4	
116	MGT TXN3_116	N3	
116	MGTRBIAS_116	R7	
116	MGT REFCLKP_116	R4	
116	MGT REFCLKN_116	R3	
116	MGTRXP1_116	T6	
116	MGT RXN1_116	T5	
116	MGT TXP1_116	P2	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
116	MGTTXN1_116	P1	
116	MGTRXP0_116	U4	
116	MGTRXN0_116	U3	
116	MGTTXP0_116	T2	
116	MGTTXN0_116	T1	
117	MGTRXP2_117	H6	
117	MGTRXN2_117	H5	
117	MGTTXP2_117	G4	
117	MGTTXN2_117	G3	
117	MGTRXP3_117	J8	
117	MGTRXN3_117	J7	
117	MGTTXP3_117	H2	
117	MGTTXN3_117	H1	
117	MGTRBIAS_117	E8	
117	MGTREFCLKP_117	J4	
117	MGTREFCLKN_117	J3	
117	MGTRXP1_117	L8	
117	MGTRXN1_117	L7	
117	MGTTXP1_117	K2	
117	MGTTXN1_117	K1	
117	MGTRXP0_117	K6	
117	MGTRXN0_117	K5	
117	MGTTXP0_117	L4	
117	MGTTXN0_117	L3	
118	MGTRXP2_118	B6	
118	MGTRXN2_118	B5	
118	MGTTXP2_118	A4	
118	MGTTXN2_118	A3	
118	MGTRXP3_118	D6	
118	MGTRXN3_118	D5	
118	MGTTXP3_118	C4	
118	MGTTXN3_118	C3	
118	MGTRBIAS_118	D8	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
118	MGTRREFCLKP_118	E4	
118	MGTRREFCLKN_118	E3	
118	MGTRXP1_118	F6	
118	MGTRXN1_118	F5	
118	MGTTXP1_118	D2	
118	MGTTXN1_118	D1	
118	MGTRXP0_118	G8	
118	MGTRXN0_118	G7	
118	MGTTXP0_118	F2	
118	MGTTXN0_118	F1	
NA	MGTHAVCCRX_L	A39	
NA	MGTHAVCCRX_L	C39	
NA	MGTHAVCCRX_L	F37	
NA	MGTHAVCCRX_L	G39	
NA	MGTHAVCCRX_L	J39	
NA	MGTHAVCCRX_L	L39	
NA	MGTHAVCCRX_L	P37	
NA	MGTHAVCCRX_L	R39	
NA	MGTHAVCCRX_R	A6	
NA	MGTHAVCCRX_R	C6	
NA	MGTHAVCCRX_R	F8	
NA	MGTHAVCCRX_R	G6	
NA	MGTHAVCCRX_R	J6	
NA	MGTHAVCCRX_R	L6	
NA	MGTHAVCCRX_R	P8	
NA	MGTHAVCCRX_R	R6	
NA	MGTHAVTT_L	E43	
NA	MGTHAVTT_L	J43	
NA	MGTHAVTT_L	L43	
NA	MGTHAVTT_L	R43	
NA	MGTHAVTT_R	E2	
NA	MGTHAVTT_R	J2	
NA	MGTHAVTT_R	L2	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTHAVTT_R	R2	
NA	MGTAVCC_LN	AA36	
NA	MGTAVCC_LN	AC36	
NA	MGTAVCC_LN	AE36	
NA	MGTAVCC_LN	AG36	
NA	MGTAVCC_LN	U36	
NA	MGTAVCC_LN	V37	
NA	MGTAVCC_LN	W36	
NA	MGTAVCC_LS	AK37	
NA	MGTAVCC_LS	AM37	
NA	MGTAVCC_LS	AP37	
NA	MGTAVCC_LS	AT37	
NA	MGTAVCC_LS	AV37	
NA	MGTAVCC_LS	AY37	
NA	MGTAVCC_LS	BB37	
NA	MGTAVCC_RN	AA9	
NA	MGTAVCC_RN	AC9	
NA	MGTAVCC_RN	AE9	
NA	MGTAVCC_RN	AG9	
NA	MGTAVCC_RN	U9	
NA	MGTAVCC_RN	V8	
NA	MGTAVCC_RN	W9	
NA	MGTAVTT_LN	AB41	
NA	MGTAVTT_LN	AC43	
NA	MGTAVTT_LN	AD42	
NA	MGTAVTT_LN	AF41	
NA	MGTAVTT_LN	AG43	
NA	MGTAVTT_LN	AH42	
NA	MGTAVTT_LN	W43	
NA	MGTAVTT_LN	Y42	
NA	MGTAVTT_LS	AN43	
NA	MGTAVTT_LS	AP42	
NA	MGTAVTT_LS	AT41	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTAVTT_LS	AU43	
NA	MGTAVTT_LS	AV42	
NA	MGTAVTT_LS	AY41	
NA	MGTAVTT_LS	BA43	
NA	MGTAVTT_LS	BB42	
NA	MGTAVTT_RN	AB4	
NA	MGTAVTT_RN	AC2	
NA	MGTAVTT_RN	AD3	
NA	MGTAVTT_RN	AF4	
NA	MGTAVTT_RN	AG2	
NA	MGTAVTT_RN	AH3	
NA	MGTAVTT_RN	W2	
NA	MGTAVTT_RN	Y3	
NA	MGTHAVCC_L	B41	
NA	MGTHAVCC_L	D41	
NA	MGTHAVCC_L	E39	
NA	MGTHAVCC_L	F41	
NA	MGTHAVCC_L	H41	
NA	MGTHAVCC_L	K41	
NA	MGTHAVCC_L	M41	
NA	MGTHAVCC_L	N39	
NA	MGTHAVCC_L	P41	
NA	MGTHAVCC_L	T41	
NA	MGTHAVCC_R	B4	
NA	MGTHAVCC_R	D4	
NA	MGTHAVCC_R	E6	
NA	MGTHAVCC_R	F4	
NA	MGTHAVCC_R	H4	
NA	MGTHAVCC_R	K4	
NA	MGTHAVCC_R	M4	
NA	MGTHAVCC_R	N6	
NA	MGTHAVCC_R	P4	
NA	MGTHAVCC_R	T4	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTHAVCCPLL_L	H37	
NA	MGTHAVCCPLL_L	K37	
NA	MGTHAVCCPLL_L	M37	
NA	MGTHAVCCPLL_R	H8	
NA	MGTHAVCCPLL_R	K8	
NA	MGTHAVCCPLL_R	M8	
NA	MGTHAGND_L	A40	
NA	MGTHAGND_L	B42	
NA	MGTHAGND_L	B43	
NA	MGTHAGND_L	C40	
NA	MGTHAGND_L	C43	
NA	MGTHAGND_L	C44	
NA	MGTHAGND_L	D38	
NA	MGTHAGND_L	D42	
NA	MGTHAGND_L	E38	
NA	MGTHAGND_L	E40	
NA	MGTHAGND_L	E44	
NA	MGTHAGND_L	F38	
NA	MGTHAGND_L	F42	
NA	MGTHAGND_L	G40	
NA	MGTHAGND_L	G43	
NA	MGTHAGND_L	G44	
NA	MGTHAGND_L	H38	
NA	MGTHAGND_L	H42	
NA	MGTHAGND_L	J40	
NA	MGTHAGND_L	J44	
NA	MGTHAGND_L	K38	
NA	MGTHAGND_L	K42	
NA	MGTHAGND_L	L40	
NA	MGTHAGND_L	L44	
NA	MGTHAGND_L	M38	
NA	MGTHAGND_L	M42	
NA	MGTHAGND_L	N40	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTHAGND_L	N43	
NA	MGTHAGND_L	N44	
NA	MGTHAGND_L	P38	
NA	MGTHAGND_L	P42	
NA	MGTHAGND_L	R40	
NA	MGTHAGND_L	R44	
NA	MGTHAGND_L	T38	
NA	MGTHAGND_L	T42	
NA	MGTHAGND_L	U39	
NA	MGTHAGND_L	U40	
NA	MGTHAGND_L	U43	
NA	MGTHAGND_L	U44	
NA	MGTHAGND_L	V41	
NA	MGTHAGND_R	A5	
NA	MGTHAGND_R	B2	
NA	MGTHAGND_R	B3	
NA	MGTHAGND_R	C1	
NA	MGTHAGND_R	C2	
NA	MGTHAGND_R	C5	
NA	MGTHAGND_R	D3	
NA	MGTHAGND_R	D7	
NA	MGTHAGND_R	E1	
NA	MGTHAGND_R	E5	
NA	MGTHAGND_R	E7	
NA	MGTHAGND_R	F3	
NA	MGTHAGND_R	F7	
NA	MGTHAGND_R	G1	
NA	MGTHAGND_R	G2	
NA	MGTHAGND_R	G5	
NA	MGTHAGND_R	H3	
NA	MGTHAGND_R	H7	
NA	MGTHAGND_R	J1	
NA	MGTHAGND_R	J5	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTHAGND_R	K3	
NA	MGTHAGND_R	K7	
NA	MGTHAGND_R	L1	
NA	MGTHAGND_R	L5	
NA	MGTHAGND_R	M3	
NA	MGTHAGND_R	M7	
NA	MGTHAGND_R	N1	
NA	MGTHAGND_R	N2	
NA	MGTHAGND_R	N5	
NA	MGTHAGND_R	P3	
NA	MGTHAGND_R	P7	
NA	MGTHAGND_R	R1	
NA	MGTHAGND_R	R5	
NA	MGTHAGND_R	T3	
NA	MGTHAGND_R	T7	
NA	MGTHAGND_R	U1	
NA	MGTHAGND_R	U2	
NA	MGTHAGND_R	U5	
NA	MGTHAGND_R	U6	
NA	MGTHAGND_R	V4	
NA	GND	A7	
NA	GND	A16	
NA	GND	A26	
NA	GND	A36	
NA	GND	A38	
NA	GND	AA1	
NA	GND	AA2	
NA	GND	AA5	
NA	GND	AA6	
NA	GND	AA10	
NA	GND	AA11	
NA	GND	AA15	
NA	GND	AA17	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AA19	
NA	GND	AA21	
NA	GND	AA25	
NA	GND	AA27	
NA	GND	AA29	
NA	GND	AA31	
NA	GND	AA34	
NA	GND	AA35	
NA	GND	AA39	
NA	GND	AA40	
NA	GND	AA43	
NA	GND	AA44	
NA	GND	AB3	
NA	GND	AB7	
NA	GND	AB8	
NA	GND	AB11	
NA	GND	AB14	
NA	GND	AB16	
NA	GND	AB18	
NA	GND	AB20	
NA	GND	AB24	
NA	GND	AB26	
NA	GND	AB28	
NA	GND	AB30	
NA	GND	AB32	
NA	GND	AB34	
NA	GND	AB37	
NA	GND	AB38	
NA	GND	AB42	
NA	GND	AC1	
NA	GND	AC5	
NA	GND	AC6	
NA	GND	AC10	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AC11	
NA	GND	AC13	
NA	GND	AC15	
NA	GND	AC17	
NA	GND	AC19	
NA	GND	AC21	
NA	GND	AC25	
NA	GND	AC27	
NA	GND	AC29	
NA	GND	AC31	
NA	GND	AC34	
NA	GND	AC35	
NA	GND	AC39	
NA	GND	AC40	
NA	GND	AC44	
NA	GND	AD4	
NA	GND	AD7	
NA	GND	AD8	
NA	GND	AD11	
NA	GND	AD14	
NA	GND	AD16	
NA	GND	AD18	
NA	GND	AD20	
NA	GND	AD24	
NA	GND	AD26	
NA	GND	AD28	
NA	GND	AD30	
NA	GND	AD32	
NA	GND	AD34	
NA	GND	AD37	
NA	GND	AD38	
NA	GND	AD41	
NA	GND	AE1	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AE2	
NA	GND	AE5	
NA	GND	AE6	
NA	GND	AE10	
NA	GND	AE11	
NA	GND	AE13	
NA	GND	AE15	
NA	GND	AE17	
NA	GND	AE19	
NA	GND	AE21	
NA	GND	AE23	
NA	GND	AE25	
NA	GND	AE27	
NA	GND	AE29	
NA	GND	AE31	
NA	GND	AE34	
NA	GND	AE35	
NA	GND	AE39	
NA	GND	AE40	
NA	GND	AE43	
NA	GND	AE44	
NA	GND	AF3	
NA	GND	AF7	
NA	GND	AF8	
NA	GND	AF11	
NA	GND	AF14	
NA	GND	AF16	
NA	GND	AF18	
NA	GND	AF20	
NA	GND	AF22	
NA	GND	AF24	
NA	GND	AF26	
NA	GND	AF28	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AF30	
NA	GND	AF32	
NA	GND	AF34	
NA	GND	AF37	
NA	GND	AF38	
NA	GND	AF42	
NA	GND	AG1	
NA	GND	AG5	
NA	GND	AG6	
NA	GND	AG10	
NA	GND	AG11	
NA	GND	AG13	
NA	GND	AG15	
NA	GND	AG17	
NA	GND	AG19	
NA	GND	AG21	
NA	GND	AG23	
NA	GND	AG25	
NA	GND	AG27	
NA	GND	AG29	
NA	GND	AG31	
NA	GND	AG34	
NA	GND	AG35	
NA	GND	AG39	
NA	GND	AG40	
NA	GND	AG44	
NA	GND	AH4	
NA	GND	AH7	
NA	GND	AH8	
NA	GND	AH11	
NA	GND	AH14	
NA	GND	AH16	
NA	GND	AH18	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AH20	
NA	GND	AH22	
NA	GND	AH24	
NA	GND	AH26	
NA	GND	AH28	
NA	GND	AH30	
NA	GND	AH34	
NA	GND	AH37	
NA	GND	AH38	
NA	GND	AH41	
NA	GND	AJ1	
NA	GND	AJ2	
NA	GND	AJ5	
NA	GND	AJ6	
NA	GND	AJ9	
NA	GND	AJ10	
NA	GND	AJ11	
NA	GND	AJ12	
NA	GND	AJ22	
NA	GND	AJ32	
NA	GND	AJ34	
NA	GND	AJ35	
NA	GND	AJ36	
NA	GND	AJ39	
NA	GND	AJ40	
NA	GND	AJ43	
NA	GND	AJ44	
NA	GND	AK3	
NA	GND	AK4	
NA	GND	AK7	
NA	GND	AK8	
NA	GND	AK9	
NA	GND	AK19	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AK29	
NA	GND	AK36	
NA	GND	AK38	
NA	GND	AK41	
NA	GND	AK42	
NA	GND	AL1	
NA	GND	AL2	
NA	GND	AL5	
NA	GND	AL6	
NA	GND	AL9	
NA	GND	AL16	
NA	GND	AL26	
NA	GND	AL36	
NA	GND	AL39	
NA	GND	AL40	
NA	GND	AL43	
NA	GND	AL44	
NA	GND	AM3	
NA	GND	AM4	
NA	GND	AM7	
NA	GND	AM8	
NA	GND	AM9	
NA	GND	AM13	
NA	GND	AM23	
NA	GND	AM33	
NA	GND	AM36	
NA	GND	AM38	
NA	GND	AM41	
NA	GND	AM42	
NA	GND	AN1	
NA	GND	AN2	
NA	GND	AN5	
NA	GND	AN6	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AN9	
NA	GND	AN10	
NA	GND	AN20	
NA	GND	AN30	
NA	GND	AN36	
NA	GND	AN39	
NA	GND	AN40	
NA	GND	AN44	
NA	GND	AP3	
NA	GND	AP4	
NA	GND	AP5	
NA	GND	AP6	
NA	GND	AP7	
NA	GND	AP8	
NA	GND	AP9	
NA	GND	AP17	
NA	GND	AP27	
NA	GND	AP36	
NA	GND	AP38	
NA	GND	AP41	
NA	GND	AR1	
NA	GND	AR2	
NA	GND	AR3	
NA	GND	AR4	
NA	GND	AR14	
NA	GND	AR24	
NA	GND	AR34	
NA	GND	AR36	
NA	GND	AR39	
NA	GND	AR40	
NA	GND	AR43	
NA	GND	AR44	
NA	GND	AT1	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AT11	
NA	GND	AT21	
NA	GND	AT31	
NA	GND	AT36	
NA	GND	AT38	
NA	GND	AT42	
NA	GND	AU8	
NA	GND	AU18	
NA	GND	AU28	
NA	GND	AU36	
NA	GND	AU39	
NA	GND	AU40	
NA	GND	AU44	
NA	GND	AV5	
NA	GND	AV15	
NA	GND	AV25	
NA	GND	AV35	
NA	GND	AV36	
NA	GND	AV38	
NA	GND	AV41	
NA	GND	AW2	
NA	GND	AW12	
NA	GND	AW22	
NA	GND	AW32	
NA	GND	AW36	
NA	GND	AW39	
NA	GND	AW40	
NA	GND	AW43	
NA	GND	AW44	
NA	GND	AY9	
NA	GND	AY19	
NA	GND	AY29	
NA	GND	AY36	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AY38	
NA	GND	AY42	
NA	GND	B7	
NA	GND	B13	
NA	GND	B23	
NA	GND	B33	
NA	GND	B38	
NA	GND	BA6	
NA	GND	BA16	
NA	GND	BA26	
NA	GND	BA36	
NA	GND	BA39	
NA	GND	BA40	
NA	GND	BA44	
NA	GND	BB3	
NA	GND	BB13	
NA	GND	BB23	
NA	GND	BB33	
NA	GND	BB36	
NA	GND	BB38	
NA	GND	BB41	
NA	GND	BC10	
NA	GND	BC20	
NA	GND	BC30	
NA	GND	BC36	
NA	GND	BC39	
NA	GND	BC40	
NA	GND	BC43	
NA	GND	BD7	
NA	GND	BD17	
NA	GND	BD27	
NA	GND	BD36	
NA	GND	BD37	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	BD38	
NA	GND	BD41	
NA	GND	BD42	
NA	GND	C7	
NA	GND	C8	
NA	GND	C9	
NA	GND	C10	
NA	GND	C20	
NA	GND	C30	
NA	GND	C36	
NA	GND	C37	
NA	GND	C38	
NA	GND	D9	
NA	GND	D17	
NA	GND	D27	
NA	GND	D36	
NA	GND	E9	
NA	GND	E14	
NA	GND	E24	
NA	GND	E34	
NA	GND	E36	
NA	GND	F9	
NA	GND	F11	
NA	GND	F21	
NA	GND	F31	
NA	GND	F36	
NA	GND	G9	
NA	GND	G18	
NA	GND	G28	
NA	GND	G36	
NA	GND	H9	
NA	GND	H15	
NA	GND	H25	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	H35	
NA	GND	H36	
NA	GND	J9	
NA	GND	J12	
NA	GND	J22	
NA	GND	J32	
NA	GND	J36	
NA	GND	K9	
NA	GND	K19	
NA	GND	K29	
NA	GND	K36	
NA	GND	L9	
NA	GND	L16	
NA	GND	L26	
NA	GND	L36	
NA	GND	M9	
NA	GND	M13	
NA	GND	M23	
NA	GND	M33	
NA	GND	M36	
NA	GND	N9	
NA	GND	N10	
NA	GND	N20	
NA	GND	N30	
NA	GND	N36	
NA	GND	P9	
NA	GND	P17	
NA	GND	P27	
NA	GND	P36	
NA	GND	R9	
NA	GND	R10	
NA	GND	R11	
NA	GND	R14	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	R24	
NA	GND	R34	
NA	GND	R35	
NA	GND	R36	
NA	GND	T8	
NA	GND	T11	
NA	GND	T18	
NA	GND	T20	
NA	GND	T22	
NA	GND	T24	
NA	GND	T28	
NA	GND	T31	
NA	GND	T34	
NA	GND	T37	
NA	GND	U10	
NA	GND	U11	
NA	GND	U15	
NA	GND	U17	
NA	GND	U19	
NA	GND	U21	
NA	GND	U23	
NA	GND	U25	
NA	GND	U27	
NA	GND	U29	
NA	GND	U31	
NA	GND	U34	
NA	GND	U35	
NA	GND	V3	
NA	GND	V7	
NA	GND	V11	
NA	GND	V14	
NA	GND	V16	
NA	GND	V18	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	V20	
NA	GND	V22	
NA	GND	V24	
NA	GND	V26	
NA	GND	V28	
NA	GND	V30	
NA	GND	V34	
NA	GND	V38	
NA	GND	V42	
NA	GND	W1	
NA	GND	W5	
NA	GND	W6	
NA	GND	W10	
NA	GND	W11	
NA	GND	W15	
NA	GND	W17	
NA	GND	W19	
NA	GND	W21	
NA	GND	W23	
NA	GND	W25	
NA	GND	W27	
NA	GND	W29	
NA	GND	W31	
NA	GND	W34	
NA	GND	W35	
NA	GND	W39	
NA	GND	W40	
NA	GND	W44	
NA	GND	Y4	
NA	GND	Y7	
NA	GND	Y8	
NA	GND	Y11	
NA	GND	Y14	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	Y16	
NA	GND	Y18	
NA	GND	Y20	
NA	GND	Y22	
NA	GND	Y24	
NA	GND	Y26	
NA	GND	Y28	
NA	GND	Y30	
NA	GND	Y32	
NA	GND	Y34	
NA	GND	Y37	
NA	GND	Y38	
NA	GND	Y41	
NA	VCCAUX	AA12	
NA	VCCAUX	AA32	
NA	VCCAUX	AB13	
NA	VCCAUX	AB33	
NA	VCCAUX	AC12	
NA	VCCAUX	AC32	
NA	VCCAUX	AD13	
NA	VCCAUX	AD33	
NA	VCCAUX	AE12	
NA	VCCAUX	AE32	
NA	VCCAUX	AF13	
NA	VCCAUX	AF33	
NA	VCCAUX	AG12	
NA	VCCAUX	AG32	
NA	VCCAUX	U12	
NA	VCCAUX	U32	
NA	VCCAUX	V13	
NA	VCCAUX	V33	
NA	VCCAUX	W12	
NA	VCCAUX	W32	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCAUX	Y13	
NA	VCCAUX	Y33	
NA	VCCINT	AA14	
NA	VCCINT	AA16	
NA	VCCINT	AA18	
NA	VCCINT	AA20	
NA	VCCINT	AA24	
NA	VCCINT	AA26	
NA	VCCINT	AA28	
NA	VCCINT	AA30	
NA	VCCINT	AB15	
NA	VCCINT	AB17	
NA	VCCINT	AB19	
NA	VCCINT	AB21	
NA	VCCINT	AB25	
NA	VCCINT	AB27	
NA	VCCINT	AB29	
NA	VCCINT	AB31	
NA	VCCINT	AC14	
NA	VCCINT	AC16	
NA	VCCINT	AC18	
NA	VCCINT	AC20	
NA	VCCINT	AC24	
NA	VCCINT	AC26	
NA	VCCINT	AC28	
NA	VCCINT	AC30	
NA	VCCINT	AD15	
NA	VCCINT	AD17	
NA	VCCINT	AD19	
NA	VCCINT	AD21	
NA	VCCINT	AD25	
NA	VCCINT	AD27	
NA	VCCINT	AD29	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	AD31	
NA	VCCINT	AE14	
NA	VCCINT	AE16	
NA	VCCINT	AE18	
NA	VCCINT	AE20	
NA	VCCINT	AE22	
NA	VCCINT	AE24	
NA	VCCINT	AE26	
NA	VCCINT	AE28	
NA	VCCINT	AE30	
NA	VCCINT	AF15	
NA	VCCINT	AF17	
NA	VCCINT	AF19	
NA	VCCINT	AF21	
NA	VCCINT	AF23	
NA	VCCINT	AF25	
NA	VCCINT	AF27	
NA	VCCINT	AF29	
NA	VCCINT	AF31	
NA	VCCINT	AG14	
NA	VCCINT	AG16	
NA	VCCINT	AG18	
NA	VCCINT	AG20	
NA	VCCINT	AG22	
NA	VCCINT	AG24	
NA	VCCINT	AG26	
NA	VCCINT	AG28	
NA	VCCINT	AG30	
NA	VCCINT	AH15	
NA	VCCINT	AH17	
NA	VCCINT	AH19	
NA	VCCINT	AH21	
NA	VCCINT	AH23	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	AH25	
NA	VCCINT	AH27	
NA	VCCINT	AH29	
NA	VCCINT	AH31	
NA	VCCINT	T19	
NA	VCCINT	T21	
NA	VCCINT	T23	
NA	VCCINT	T25	
NA	VCCINT	U14	
NA	VCCINT	U16	
NA	VCCINT	U18	
NA	VCCINT	U20	
NA	VCCINT	U22	
NA	VCCINT	U24	
NA	VCCINT	U26	
NA	VCCINT	U28	
NA	VCCINT	U30	
NA	VCCINT	V15	
NA	VCCINT	V17	
NA	VCCINT	V19	
NA	VCCINT	V21	
NA	VCCINT	V23	
NA	VCCINT	V25	
NA	VCCINT	V27	
NA	VCCINT	V29	
NA	VCCINT	V31	
NA	VCCINT	W14	
NA	VCCINT	W16	
NA	VCCINT	W18	
NA	VCCINT	W20	
NA	VCCINT	W22	
NA	VCCINT	W24	
NA	VCCINT	W26	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	W28	
NA	VCCINT	W30	
NA	VCCINT	Y15	
NA	VCCINT	Y17	
NA	VCCINT	Y19	
NA	VCCINT	Y21	
NA	VCCINT	Y23	
NA	VCCINT	Y25	
NA	VCCINT	Y27	
NA	VCCINT	Y29	
NA	VCCINT	Y31	
0	VCCO_0	T12	
0	VCCO_0	V12	
20	VCCO_20	AP22	
20	VCCO_20	AU23	
20	VCCO_20	AV20	
20	VCCO_20	BA21	
20	VCCO_20	BD22	
21	VCCO_21	AK24	
21	VCCO_21	AN25	
21	VCCO_21	AT26	
21	VCCO_21	AY24	
21	VCCO_21	BC25	
22	VCCO_22	AJ27	
22	VCCO_22	AM28	
22	VCCO_22	AR29	
22	VCCO_22	AW27	
22	VCCO_22	BB28	
23	VCCO_23	AL31	
23	VCCO_23	AP32	
23	VCCO_23	AV30	
23	VCCO_23	BA31	
23	VCCO_23	BD32	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
24	VCCO_24	AK34	
24	VCCO_24	AN35	
24	VCCO_24	AU33	
24	VCCO_24	AY34	
24	VCCO_24	BC35	
25	VCCO_25	C35	
25	VCCO_25	G33	
25	VCCO_25	K34	
25	VCCO_25	N35	
25	VCCO_25	P32	
26	VCCO_26	A31	
26	VCCO_26	D32	
26	VCCO_26	H30	
26	VCCO_26	L31	
26	VCCO_26	R29	
27	VCCO_27	B28	
27	VCCO_27	E29	
27	VCCO_27	J27	
27	VCCO_27	M28	
27	VCCO_27	T26	
28	VCCO_28	C25	
28	VCCO_28	F26	
28	VCCO_28	G23	
28	VCCO_28	K24	
28	VCCO_28	N25	
30	VCCO_30	AR19	
30	VCCO_30	AW17	
30	VCCO_30	BB18	
30	VCCO_30	BC15	
30	VCCO_30	BD12	
31	VCCO_31	AL21	
31	VCCO_31	AM18	
31	VCCO_31	AT16	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
31	VCCO_31	AU13	
31	VCCO_31	AY14	
32	VCCO_32	AY4	
32	VCCO_32	BA1	
32	VCCO_32	BA11	
32	VCCO_32	BB8	
32	VCCO_32	BC5	
33	VCCO_33	AJ17	
33	VCCO_33	AN15	
33	VCCO_33	AP12	
33	VCCO_33	AV10	
33	VCCO_33	AW7	
34	VCCO_34	AK14	
34	VCCO_34	AL11	
34	VCCO_34	AR9	
34	VCCO_34	AT6	
34	VCCO_34	AU3	
35	VCCO_35	A11	
35	VCCO_35	B8	
35	VCCO_35	D12	
35	VCCO_35	H10	
35	VCCO_35	L11	
35	VCCO_35	P12	
36	VCCO_36	C15	
36	VCCO_36	F16	
36	VCCO_36	G13	
36	VCCO_36	K14	
36	VCCO_36	N15	
37	VCCO_37	E19	
37	VCCO_37	J17	
37	VCCO_37	M18	
37	VCCO_37	R19	
37	VCCO_37	T16	

Table 2-8: FF1923 Package—HX255T, HX380T, and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
38	VCCO_38	A21	
38	VCCO_38	B18	
38	VCCO_38	D22	
38	VCCO_38	H20	
38	VCCO_38	L21	
38	VCCO_38	P22	
NA	RSVD	R37	
NA	RSVD	P39	
NA	RSVD	P40	
NA	RSVD	R8	
NA	RSVD	P6	
NA	RSVD	P5	

FF1924 Package—HX380T and HX565T

Table 2-9: FF1924 Package—HX380T and HX565T

Bank	Pin Description	Pin Number	No Connect (NC)
0	INIT_B_0	T14	
0	DONE_0	T13	
0	M1_0	T32	
0	M2_0	T33	
0	HSWAPEN_0	U13	
0	PROGRAM_B_0	U33	
0	M0_0	V32	
0	AVSS_0	AA22	
0	AVDD_0	AA23	
0	VP_0	AB23	
0	VREFP_0	AC23	
0	VN_0	AC22	
0	VREFN_0	AB22	
0	DXP_0	AD23	
0	DXN_0	AD22	
0	VBATT_0	AA13	
0	DIN_0	W13	
0	RDWR_B_0	W33	
0	CSI_B_0	AH32	
0	DOUT_BUSY_0	AK32	
0	CCLK_0	AJ33	
0	TDO_0	AH12	
0	TCK_0	AJ13	
0	TMS_0	AK12	
0	TDI_0	AK11	
0	VFS_0	AK33	
21	IO_L0P_21	AU26	
21	IO_L0N_21	AV26	
21	IO_L1P_21	AT25	
21	IO_L1N_21	AU25	
21	IO_L2P_21	AW25	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
21	IO_L2N_21	AY25	
21	IO_L3P_21	AK23	
21	IO_L3N_21	AL23	
21	IO_L4P_21	BD25	
21	IO_L4N_VREF_21	BD26	
21	IO_L5P_21	AW26	
21	IO_L5N_21	AY26	
21	IO_L6P_21	AN23	
21	IO_L6N_21	AP23	
21	IO_L7P_21	BB26	
21	IO_L7N_21	BC26	
21	IO_L8P_SRCC_21	BA24	
21	IO_L8N_SRCC_21	BB24	
21	IO_L9P_MRCC_21	AR23	
21	IO_L9N_MRCC_21	AT23	
21	IO_L10P_MRCC_21	AV23	
21	IO_L10N_MRCC_21	AW23	
21	IO_L11P_SRCC_21	AY23	
21	IO_L11N_SRCC_21	BA23	
21	IO_L12P_VRN_21	AP25	
21	IO_L12N_VRP_21	AR25	
21	IO_L13P_21	AV24	
21	IO_L13N_21	AW24	
21	IO_L14P_21	AT24	
21	IO_L14N_VREF_21	AU24	
21	IO_L15P_21	AL24	
21	IO_L15N_21	AM24	
21	IO_L16P_21	BC23	
21	IO_L16N_21	BD23	
21	IO_L17P_21	BC24	
21	IO_L17N_21	BD24	
21	IO_L18P_21	AN24	
21	IO_L18N_21	AP24	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
21	IO_L19P_21	BA25	
21	IO_L19N_21	BB25	
22	IO_L0P_22	AM27	
22	IO_L0N_22	AN28	
22	IO_L1P_22	AN27	
22	IO_L1N_22	AP28	
22	IO_L2P_22	AR28	
22	IO_L2N_22	AT28	
22	IO_L3P_22	AJ28	
22	IO_L3N_22	AK28	
22	IO_L4P_22	AV28	
22	IO_L4N_VREF_22	AW29	
22	IO_L5P_22	AR26	
22	IO_L5N_22	AR27	
22	IO_L6P_22	AL27	
22	IO_L6N_22	AL28	
22	IO_L7P_22	AT27	
22	IO_L7N_22	AU27	
22	IO_L8P_SRCC_22	AY28	
22	IO_L8N_SRCC_22	BA29	
22	IO_L9P_MRCC_22	AJ26	
22	IO_L9N_MRCC_22	AK27	
22	IO_L10P_MRCC_22	AN26	
22	IO_L10N_MRCC_22	AP26	
22	IO_L11P_SRCC_22	AV27	
22	IO_L11N_SRCC_22	AW28	
22	IO_L12P_VRN_22	AJ25	
22	IO_L12N_VRP_22	AK26	
22	IO_L13P_22	AY27	
22	IO_L13N_22	BA28	
22	IO_L14P_22	BC27	
22	IO_L14N_VREF_22	BD28	
22	IO_L15P_22	AM25	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
22	IO_L15N_22	AM26	
22	IO_L16P_22	BA27	
22	IO_L16N_22	BB27	
22	IO_L17P_22	BB29	
22	IO_L17N_22	BC29	
22	IO_L18P_22	AK25	
22	IO_L18N_22	AL25	
22	IO_L19P_22	BC28	
22	IO_L19N_22	BD29	
23	IO_L0P_23	AP31	
23	IO_L0N_23	AR31	
23	IO_L1P_23	AP29	
23	IO_L1N_23	AP30	
23	IO_L2P_23	AU31	
23	IO_L2N_23	AV31	
23	IO_L3P_23	AJ31	
23	IO_L3N_23	AK31	
23	IO_L4P_23	AR30	
23	IO_L4N_VREF_23	AT30	
23	IO_L5P_23	AU32	
23	IO_L5N_23	AV32	
23	IO_L6P_23	AK30	
23	IO_L6N_23	AL30	
23	IO_L7P_23	AT29	
23	IO_L7N_23	AU30	
23	IO_L8P_SRCC_23	AY32	
23	IO_L8N_SRCC_23	BA32	
23	IO_L9P_MRCC_23	AJ29	
23	IO_L9N_MRCC_23	AJ30	
23	IO_L10P_MRCC_23	BB31	
23	IO_L10N_MRCC_23	BC31	
23	IO_L11P_SRCC_23	AW31	
23	IO_L11N_SRCC_23	AY31	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
23	IO_L12P_VRN_23	AL29	
23	IO_L12N_VRP_23	AM30	
23	IO_L13P_23	BB32	
23	IO_L13N_23	BC32	
23	IO_L14P_23	AU29	
23	IO_L14N_VREF_23	AV29	
23	IO_L15P_23	AM31	
23	IO_L15N_23	AN31	
23	IO_L16P_23	AW30	
23	IO_L16N_23	AY30	
23	IO_L17P_23	BA30	
23	IO_L17N_23	BB30	
23	IO_L18P_23	AM29	
23	IO_L18N_23	AN29	
23	IO_L19P_23	BD30	
23	IO_L19N_23	BD31	
24	IO_L0P_GC_24	AP33	
24	IO_L0N_GC_24	AP34	
24	IO_L1P_GC_24	AR33	
24	IO_L1N_GC_24	AT33	
24	IO_L2P_D15_24	AR35	
24	IO_L2N_D14_24	AT35	
24	IO_L3P_D13_24	AK35	
24	IO_L3N_D12_24	AL35	
24	IO_L4P_D11_24	AU34	
24	IO_L4N_VREF_D10_24	AV34	
24	IO_L5P_D9_24	AT34	
24	IO_L5N_D8_24	AU35	
24	IO_L6P_D7_24	AL34	
24	IO_L6N_D6_24	AM35	
24	IO_L7P_D5_24	AV33	
24	IO_L7N_D4_24	AW34	
24	IO_L8P_SRCC_24	AR32	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
24	IO_L8N_SRCC_24	AT32	
24	IO_L9P_MRCC_24	AL33	
24	IO_L9N_MRCC_24	AM34	
24	IO_L10P_MRCC_24	AW35	
24	IO_L10N_MRCC_24	AY35	
24	IO_L11P_SRCC_24	BA35	
24	IO_L11N_SRCC_24	BB35	
24	IO_L12P_D3_24	AN34	
24	IO_L12N_D2_FS2_24	AP35	
24	IO_L13P_D1_FS1_24	BA33	
24	IO_L13N_D0_FS0_24	BA34	
24	IO_L14P_FCS_B_24	AW33	
24	IO_L14N_VREF_FOE_B_MOSI_24	AY33	
24	IO_L15P_FWE_B_24	AN32	
24	IO_L15N_RS1_24	AN33	
24	IO_L16P_RS0_24	BB34	
24	IO_L16N_CS0_B_24	BC34	
24	IO_L17P_VRN_24	BD34	
24	IO_L17N_VRP_24	BD35	
24	IO_L18P_24	AL32	
24	IO_L18N_24	AM32	
24	IO_L19P_24	BC33	
24	IO_L19N_24	BD33	
25	IO_L0P_25	A34	
25	IO_L0N_25	A35	
25	IO_L1P_25	B35	
25	IO_L1N_25	B36	
25	IO_L2P_SM8P_25	B37	
25	IO_L2N_SM8N_25	A37	
25	IO_L3P_SM9P_25	L33	
25	IO_L3N_SM9N_25	K33	
25	IO_L4P_25	P34	
25	IO_L4N_VREF_25	P35	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
25	IO_L5P_SM10P_25	E35	
25	IO_L5N_SM10N_25	D35	
25	IO_L6P_SM11P_25	K35	
25	IO_L6N_SM11N_25	J35	
25	IO_L7P_SM12P_25	C34	
25	IO_L7N_SM12N_25	B34	
25	IO_L8P_SRCC_25	D33	
25	IO_L8N_SRCC_25	D34	
25	IO_L9P_MRCC_25	N33	
25	IO_L9N_MRCC_25	N34	
25	IO_L10P_MRCC_25	M35	
25	IO_L10N_MRCC_25	L35	
25	IO_L11P_SRCC_25	G35	
25	IO_L11N_SRCC_25	F35	
25	IO_L12P_SM13P_25	P31	
25	IO_L12N_SM13N_25	N32	
25	IO_L13P_SM14P_25	F33	
25	IO_L13N_SM14N_25	E33	
25	IO_L14P_25	G34	
25	IO_L14N_VREF_25	F34	
25	IO_L15P_SM15P_25	R33	
25	IO_L15N_SM15N_25	P33	
25	IO_L16P_VRN_25	M34	
25	IO_L16N_VRP_25	L34	
25	IO_L17P_25	J34	
25	IO_L17N_25	H34	
25	IO_L18P_GC_25	R31	
25	IO_L18N_GC_25	R32	
25	IO_L19P_GC_25	J33	
25	IO_L19N_GC_25	H33	
26	IO_L0P_26	B31	
26	IO_L0N_26	A32	
26	IO_L1P_26	B30	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
26	IO_L1N_26	A30	
26	IO_L2P_26	C32	
26	IO_L2N_26	C33	
26	IO_L3P_26	M30	
26	IO_L3N_26	M31	
26	IO_L4P_26	E30	
26	IO_L4N_VREF_26	D30	
26	IO_L5P_26	B32	
26	IO_L5N_26	A33	
26	IO_L6P_26	N29	
26	IO_L6N_26	M29	
26	IO_L7P_26	D31	
26	IO_L7N_26	C31	
26	IO_L8P_SRCC_26	G31	
26	IO_L8N_SRCC_26	F32	
26	IO_L9P_MRCC_26	R28	
26	IO_L9N_MRCC_26	P29	
26	IO_L10P_MRCC_26	J31	
26	IO_L10N_MRCC_26	H32	
26	IO_L11P_SRCC_26	E31	
26	IO_L11N_SRCC_26	E32	
26	IO_L12P_VRN_26	N31	
26	IO_L12N_VRP_26	M32	
26	IO_L13P_26	G30	
26	IO_L13N_26	F30	
26	IO_L14P_26	L30	
26	IO_L14N_VREF_26	K31	
26	IO_L15P_26	R30	
26	IO_L15N_26	P30	
26	IO_L16P_26	L32	
26	IO_L16N_26	K32	
26	IO_L17P_26	H31	
26	IO_L17N_26	G32	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
26	IO_L18P_26	T29	
26	IO_L18N_26	T30	
26	IO_L19P_26	K30	
26	IO_L19N_26	J30	
27	IO_L0P_27	B27	
27	IO_L0N_27	A27	
27	IO_L1P_27	A28	
27	IO_L1N_27	A29	
27	IO_L2P_27	C27	
27	IO_L2N_27	C28	
27	IO_L3P_27	N26	
27	IO_L3N_27	M26	
27	IO_L4P_27	F27	
27	IO_L4N_VREF_27	E27	
27	IO_L5P_27	C29	
27	IO_L5N_27	B29	
27	IO_L6P_27	N27	
27	IO_L6N_27	M27	
27	IO_L7P_27	F28	
27	IO_L7N_27	E28	
27	IO_L8P_SRCC_27	D28	
27	IO_L8N_SRCC_27	D29	
27	IO_L9P_MRCC_27	R25	
27	IO_L9N_MRCC_27	P25	
27	IO_L10P_MRCC_27	G29	
27	IO_L10N_MRCC_27	F29	
27	IO_L11P_SRCC_27	H27	
27	IO_L11N_SRCC_27	G27	
27	IO_L12P_VRN_27	R26	
27	IO_L12N_VRP_27	P26	
27	IO_L13P_27	K26	
27	IO_L13N_27	K27	
27	IO_L14P_27	L27	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
27	IO_L14N_VREF_27	K28	
27	IO_L15P_27	P28	
27	IO_L15N_27	N28	
27	IO_L16P_27	L28	
27	IO_L16N_27	L29	
27	IO_L17P_27	H28	
27	IO_L17N_27	H29	
27	IO_L18P_27	T27	
27	IO_L18N_27	R27	
27	IO_L19P_27	J28	
27	IO_L19N_27	J29	
28	IO_L0P_28	F23	
28	IO_L0N_28	F24	
28	IO_L1P_28	E23	
28	IO_L1N_28	D24	
28	IO_L2P_28	C26	
28	IO_L2N_28	B26	
28	IO_L3P_28	L23	
28	IO_L3N_28	K23	
28	IO_L4P_28	D23	
28	IO_L4N_VREF_28	C24	
28	IO_L5P_28	C23	
28	IO_L5N_28	B24	
28	IO_L6P_28	L24	
28	IO_L6N_28	L25	
28	IO_L7P_28	B25	
28	IO_L7N_28	A25	
28	IO_L8P_SRCC_28	A23	
28	IO_L8N_SRCC_28	A24	
28	IO_L9P_MRCC_28	M24	
28	IO_L9N_MRCC_28	M25	
28	IO_L10P_MRCC_28	E25	
28	IO_L10N_MRCC_28	D25	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
28	IO_L11P_SRCC_28	E26	
28	IO_L11N_SRCC_28	D26	
28	IO_L12P_VRN_28	K25	
28	IO_L12N_VRP_28	J25	
28	IO_L13P_28	J23	
28	IO_L13N_28	H23	
28	IO_L14P_28	G25	
28	IO_L14N_VREF_28	G26	
28	IO_L15P_28	P23	
28	IO_L15N_28	P24	
28	IO_L16P_28	J24	
28	IO_L16N_28	H24	
28	IO_L17P_28	G24	
28	IO_L17N_28	F25	
28	IO_L18P_28	N23	
28	IO_L18N_28	N24	
28	IO_L19P_28	J26	
28	IO_L19N_28	H26	
31	IO_L0P_31	AU19	
31	IO_L0N_31	AV19	
31	IO_L1P_31	AT20	
31	IO_L1N_31	AU20	
31	IO_L2P_31	AW20	
31	IO_L2N_31	AW19	
31	IO_L3P_31	AK22	
31	IO_L3N_31	AK21	
31	IO_L4P_31	AY20	
31	IO_L4N_VREF_31	BA19	
31	IO_L5P_31	BA20	
31	IO_L5N_31	BB20	
31	IO_L6P_31	AN21	
31	IO_L6N_31	AP20	
31	IO_L7P_31	BB19	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
31	IO_L7N_31	BC19	
31	IO_L8P_SRCC_31	BD20	
31	IO_L8N_SRCC_31	BD19	
31	IO_L9P_MRCC_31	AP21	
31	IO_L9N_MRCC_31	AR20	
31	IO_L10P_MRCC_31	AV22	
31	IO_L10N_MRCC_31	AW21	
31	IO_L11P_SRCC_31	BA22	
31	IO_L11N_SRCC_31	BB21	
31	IO_L12P_VRN_31	AR22	
31	IO_L12N_VRP_31	AR21	
31	IO_L13P_31	AT22	
31	IO_L13N_31	AU22	
31	IO_L14P_31	AU21	
31	IO_L14N_VREF_31	AV21	
31	IO_L15P_31	AL22	
31	IO_L15N_31	AM21	
31	IO_L16P_31	BB22	
31	IO_L16N_31	BC22	
31	IO_L17P_31	BC21	
31	IO_L17N_31	BD21	
31	IO_L18P_31	AM22	
31	IO_L18N_31	AN22	
31	IO_L19P_31	AY22	
31	IO_L19N_31	AY21	
32	IO_L0P_32	AM17	
32	IO_L0N_32	AN17	
32	IO_L1P_32	AN18	
32	IO_L1N_32	AP18	
32	IO_L2P_32	AR18	
32	IO_L2N_32	AR17	
32	IO_L3P_32	AK17	
32	IO_L3N_32	AL17	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
32	IO_L4P_32	AV17	
32	IO_L4N_VREF_32	AW16	
32	IO_L5P_32	AT17	
32	IO_L5N_32	AU17	
32	IO_L6P_32	AJ18	
32	IO_L6N_32	AK18	
32	IO_L7P_32	AT19	
32	IO_L7N_32	AT18	
32	IO_L8P_SRCC_32	BB17	
32	IO_L8N_SRCC_32	BC16	
32	IO_L9P_MRCC_32	AL19	
32	IO_L9N_MRCC_32	AL18	
32	IO_L10P_MRCC_32	AN19	
32	IO_L10N_MRCC_32	AP19	
32	IO_L11P_SRCC_32	AV18	
32	IO_L11N_SRCC_32	AW18	
32	IO_L12P_VRN_32	AM20	
32	IO_L12N_VRP_32	AM19	
32	IO_L13P_32	AY17	
32	IO_L13N_32	AY16	
32	IO_L14P_32	BC18	
32	IO_L14N_VREF_32	BD18	
32	IO_L15P_32	AJ20	
32	IO_L15N_32	AJ19	
32	IO_L16P_32	AY18	
32	IO_L16N_32	BA18	
32	IO_L17P_32	BA17	
32	IO_L17N_32	BB16	
32	IO_L18P_32	AK20	
32	IO_L18N_32	AL20	
32	IO_L19P_32	BC17	
32	IO_L19N_32	BD16	
33	IO_L0P_33	AR15	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
33	IO_L0N_33	AT14	
33	IO_L1P_33	AP15	
33	IO_L1N_33	AP14	
33	IO_L2P_33	AV14	
33	IO_L2N_33	AW14	
33	IO_L3P_33	AJ15	
33	IO_L3N_33	AJ14	
33	IO_L4P_33	AP16	
33	IO_L4N_VREF_33	AR16	
33	IO_L5P_33	AU14	
33	IO_L5N_33	AV13	
33	IO_L6P_33	AJ16	
33	IO_L6N_33	AK16	
33	IO_L7P_33	AT15	
33	IO_L7N_33	AU15	
33	IO_L8P_SRCC_33	BA14	
33	IO_L8N_SRCC_33	BA13	
33	IO_L9P_MRCC_33	AK15	
33	IO_L9N_MRCC_33	AL14	
33	IO_L10P_MRCC_33	BC14	
33	IO_L10N_MRCC_33	BD13	
33	IO_L11P_SRCC_33	AW13	
33	IO_L11N_SRCC_33	AY13	
33	IO_L12P_VRN_33	AL15	
33	IO_L12N_VRP_33	AM15	
33	IO_L13P_33	BB14	
33	IO_L13N_33	BC13	
33	IO_L14P_33	AU16	
33	IO_L14N_VREF_33	AV16	
33	IO_L15P_33	AM14	
33	IO_L15N_33	AN14	
33	IO_L16P_33	BA15	
33	IO_L16N_33	BB15	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
33	IO_L17P_33	AW15	
33	IO_L17N_33	AY15	
33	IO_L18P_33	AM16	
33	IO_L18N_33	AN16	
33	IO_L19P_33	BD15	
33	IO_L19N_33	BD14	
34	IO_L0P_GC_34	AP11	
34	IO_L0N_GC_34	AR11	
34	IO_L1P_GC_34	AR12	
34	IO_L1N_GC_34	AT12	
34	IO_L2P_A15_D31_34	AR10	
34	IO_L2N_A14_D30_34	AT10	
34	IO_L3P_A13_D29_34	AK10	
34	IO_L3N_A12_D28_34	AL10	
34	IO_L4P_A11_D27_34	AU11	
34	IO_L4N_VREF_A10_D26_34	AU10	
34	IO_L5P_A09_D25_34	AV12	
34	IO_L5N_A08_D24_34	AV11	
34	IO_L6P_A07_D23_34	AM11	
34	IO_L6N_A06_D22_34	AM10	
34	IO_L7P_A05_D21_34	AW11	
34	IO_L7N_A04_D20_34	AY11	
34	IO_L8P_SRCC_34	AP13	
34	IO_L8N_SRCC_34	AR13	
34	IO_L9P_MRCC_34	AL12	
34	IO_L9N_MRCC_34	AM12	
34	IO_L10P_MRCC_34	AW10	
34	IO_L10N_MRCC_34	AY10	
34	IO_L11P_SRCC_34	BA10	
34	IO_L11N_SRCC_34	BB10	
34	IO_L12P_A03_D19_34	AN11	
34	IO_L12N_A02_D18_34	AP10	
34	IO_L13P_A01_D17_34	AT13	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
34	IO_L13N_A00_D16_34	AU12	
34	IO_L14P_A25_34	AY12	
34	IO_L14N_VREF_A24_34	BA12	
34	IO_L15P_A23_34	AK13	
34	IO_L15N_A22_34	AL13	
34	IO_L16P_A21_34	BB11	
34	IO_L16N_A20_34	BC11	
34	IO_L17P_A19_34	BD11	
34	IO_L17N_A18_34	BD10	
34	IO_L18P_A17_34	AN13	
34	IO_L18N_A16_34	AN12	
34	IO_L19P_VRN_34	BB12	
34	IO_L19N_VRP_34	BC12	
35	IO_L0P_35	C12	
35	IO_L0N_35	C11	
35	IO_L1P_35	A13	
35	IO_L1N_35	A12	
35	IO_L2P_SM0P_35	B11	
35	IO_L2N_SM0N_35	A10	
35	IO_L3P_SM1P_35	R13	
35	IO_L3N_SM1N_35	R12	
35	IO_L4P_35	B9	
35	IO_L4N_VREF_35	A8	
35	IO_L5P_SM2P_35	C13	
35	IO_L5N_SM2N_35	B12	
35	IO_L6P_SM3P_35	H11	
35	IO_L6N_SM3N_35	G10	
35	IO_L7P_SM4P_35	B10	
35	IO_L7N_SM4N_35	A9	
35	IO_L8P_SRCC_35	E12	
35	IO_L8N_SRCC_35	D11	
35	IO_L9P_MRCC_35	K11	
35	IO_L9N_MRCC_35	J11	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
35	IO_L10P_MRCC_35	G12	
35	IO_L10N_MRCC_35	F12	
35	IO_L11P_SRCC_35	K10	
35	IO_L11N_SRCC_35	J10	
35	IO_L12P_SM5P_35	P11	
35	IO_L12N_SM5N_35	P10	
35	IO_L13P_SM6P_35	F10	
35	IO_L13N_SM6N_35	E10	
35	IO_L14P_35	E11	
35	IO_L14N_VREF_35	D10	
35	IO_L15P_SM7P_35	M11	
35	IO_L15N_SM7N_35	L10	
35	IO_L16P_VRN_35	L12	
35	IO_L16N_VRP_35	K12	
35	IO_L17P_35	H12	
35	IO_L17N_35	G11	
35	IO_L18P_GC_35	N11	
35	IO_L18N_GC_35	M10	
35	IO_L19P_GC_35	N12	
35	IO_L19N_GC_35	M12	
36	IO_L0P_36	B17	
36	IO_L0N_36	A17	
36	IO_L1P_36	B15	
36	IO_L1N_36	A15	
36	IO_L2P_36	C16	
36	IO_L2N_36	B16	
36	IO_L3P_36	G15	
36	IO_L3N_36	F15	
36	IO_L4P_36	D14	
36	IO_L4N_VREF_36	C14	
36	IO_L5P_36	B14	
36	IO_L5N_36	A14	
36	IO_L6P_36	F14	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
36	IO_L6N_36	F13	
36	IO_L7P_36	E16	
36	IO_L7N_36	D16	
36	IO_L8P_SRCC_36	J14	
36	IO_L8N_SRCC_36	H13	
36	IO_L9P_MRCC_36	P15	
36	IO_L9N_MRCC_36	P14	
36	IO_L10P_MRCC_36	P13	
36	IO_L10N_MRCC_36	N13	
36	IO_L11P_SRCC_36	E15	
36	IO_L11N_SRCC_36	D15	
36	IO_L12P_VRN_36	N14	
36	IO_L12N_VRP_36	M14	
36	IO_L13P_36	H14	
36	IO_L13N_36	G14	
36	IO_L14P_36	K13	
36	IO_L14N_VREF_36	J13	
36	IO_L15P_36	T15	
36	IO_L15N_36	R15	
36	IO_L16P_36	M15	
36	IO_L16N_36	L15	
36	IO_L17P_36	E13	
36	IO_L17N_36	D13	
36	IO_L18P_36	L14	
36	IO_L18N_36	L13	
36	IO_L19P_36	K15	
36	IO_L19N_36	J15	
37	IO_L0P_37	H19	
37	IO_L0N_37	G19	
37	IO_L1P_37	D19	
37	IO_L1N_37	C19	
37	IO_L2P_37	E18	
37	IO_L2N_37	D18	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
37	IO_L3P_37	M19	
37	IO_L3N_37	L19	
37	IO_L4P_37	F17	
37	IO_L4N_VREF_37	E17	
37	IO_L5P_37	C18	
37	IO_L5N_37	C17	
37	IO_L6P_37	P19	
37	IO_L6N_37	N19	
37	IO_L7P_37	F19	
37	IO_L7N_37	F18	
37	IO_L8P_SRCC_37	H18	
37	IO_L8N_SRCC_37	G17	
37	IO_L9P_MRCC_37	R18	
37	IO_L9N_MRCC_37	P18	
37	IO_L10P_MRCC_37	L18	
37	IO_L10N_MRCC_37	K18	
37	IO_L11P_SRCC_37	J19	
37	IO_L11N_SRCC_37	J18	
37	IO_L12P_VRN_37	N18	
37	IO_L12N_VRP_37	N17	
37	IO_L13P_37	H17	
37	IO_L13N_37	G16	
37	IO_L14P_37	J16	
37	IO_L14N_VREF_37	H16	
37	IO_L15P_37	T17	
37	IO_L15N_37	R17	
37	IO_L16P_37	N16	
37	IO_L16N_37	M16	
37	IO_L17P_37	K17	
37	IO_L17N_37	K16	
37	IO_L18P_37	M17	
37	IO_L18N_37	L17	
37	IO_L19P_37	R16	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
37	IO_L19N_37	P16	
38	IO_L0P_38	K22	
38	IO_L0N_38	J21	
38	IO_L1P_38	C22	
38	IO_L1N_38	C21	
38	IO_L2P_38	E22	
38	IO_L2N_38	D21	
38	IO_L3P_38	M22	
38	IO_L3N_38	L22	
38	IO_L4P_38	B19	
38	IO_L4N_VREF_38	A18	
38	IO_L5P_38	B20	
38	IO_L5N_38	A19	
38	IO_L6P_38	M21	
38	IO_L6N_38	M20	
38	IO_L7P_38	B22	
38	IO_L7N_38	A22	
38	IO_L8P_SRCC_38	B21	
38	IO_L8N_SRCC_38	A20	
38	IO_L9P_MRCC_38	N22	
38	IO_L9N_MRCC_38	N21	
38	IO_L10P_MRCC_38	H22	
38	IO_L10N_MRCC_38	G21	
38	IO_L11P_SRCC_38	E21	
38	IO_L11N_SRCC_38	D20	
38	IO_L12P_VRN_38	R20	
38	IO_L12N_VRP_38	P20	
38	IO_L13P_38	G22	
38	IO_L13N_38	F22	
38	IO_L14P_38	L20	
38	IO_L14N_VREF_38	K20	
38	IO_L15P_38	R23	
38	IO_L15N_38	R22	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
38	IO_L16P_38	F20	
38	IO_L16N_38	E20	
38	IO_L17P_38	H21	
38	IO_L17N_38	G20	
38	IO_L18P_38	R21	
38	IO_L18N_38	P21	
38	IO_L19P_38	K21	
38	IO_L19N_38	J20	
100	MGTTXN3_100	AV43	
100	MGTRXN3_100	BA41	
100	MGTTXP3_100	AV44	
100	MGTRXP3_100	BA42	
100	MGTTXN2_100	AW41	
100	MGTRXN2_100	BB39	
100	MGTTXP2_100	AW42	
100	MGTREFCLK1P_100	AW37	
100	MGTREFCLK1N_100	AW38	
100	MGTRXP2_100	BB40	
100	MGTREFCLK0P_100	BA37	
100	MGTREFCLK0N_100	BA38	
100	MGTTXN1_100	AY43	
100	MGTRXN1_100	BC41	
100	MGTTXP1_100	AY44	
100	MGTRXP1_100	BC42	
100	MGTTXN0_100	BB43	
100	MGTRXN0_100	BD39	
100	MGTTXP0_100	BB44	
100	MGTRXP0_100	BD40	
101	MGTTXN3_101	AP43	
101	MGTRXN3_101	AP39	
101	MGTTXP3_101	AP44	
101	MGTRXP3_101	AP40	
101	MGTTXN2_101	AR41	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
101	MGTRXN2_101	AT39	
101	MGTTXP2_101	AR42	
101	MGTREFCLK1P_101	AR37	
101	MGTREFCLK1N_101	AR38	
101	MGTRXP2_101	AT40	
101	MGTREFCLK0P_101	AU37	
101	MGTREFCLK0N_101	AU38	
101	MGTTXN1_101	AT43	
101	MGTRXN1_101	AV39	
101	MGTTXP1_101	AT44	
101	MGTRXP1_101	AV40	
101	MGTTXN0_101	AU41	
101	MGTRXN0_101	AY39	
101	MGTTXP0_101	AU42	
101	MGTRXP0_101	AY40	
102	MGTTXN3_102	AK43	
102	MGTRXN3_102	AK39	
102	MGTTXP3_102	AK44	
102	MGTRXP3_102	AK40	
102	MGTTXN2_102	AL41	
102	MGTRXN2_102	AJ37	
102	MGTTXP2_102	AL42	
102	MGTREFCLK1P_102	AH35	
102	MGTREFCLK1N_102	AH36	
102	MGTRXP2_102	AJ38	
102	MGTREFCLK0P_102	AN37	
102	MGTREFCLK0N_102	AN38	
102	MGTTXN1_102	AM43	
102	MGTRXN1_102	AM39	
102	MGTTXP1_102	AM44	
102	MGTRXP1_102	AM40	
102	MGTTXN0_102	AN41	
102	MGTRXN0_102	AL37	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
102	MGTTXP0_102	AN42	
102	MGTRXP0_102	AL38	
103	MGTTXN3_103	AF43	
103	MGTRXN3_103	AE37	
103	MGTTXP3_103	AF44	
103	MGTRXP3_103	AE38	
103	MGTTXN2_103	AG41	
103	MGTRXN2_103	AF39	
103	MGTTXP2_103	AG42	
103	MGTREFCLK1P_103	AD35	
103	MGTREFCLK1N_103	AD36	
103	MGTRXP2_103	AF40	
103	MGTREFCLK0P_103	AF35	
103	MGTREFCLK0N_103	AF36	
103	MGTTXN1_103	AH43	
103	MGTRXN1_103	AG37	
103	MGTTXP1_103	AH44	
103	MGTRXP1_103	AG38	
103	MGTTXN0_103	AJ41	
103	MGTRXN0_103	AH39	
103	MGTTXP0_103	AJ42	
103	MGTRXP0_103	AH40	
104	MGTTXN3_104	AB43	
104	MGTRXN3_104	AA37	
104	MGTTXP3_104	AB44	
104	MGTRXP3_104	AA38	
104	MGTTXN2_104	AC41	
104	MGTRXN2_104	AB39	
104	MGTTXP2_104	AC42	
104	MGTREFCLK1P_104	Y35	
104	MGTREFCLK1N_104	Y36	
104	MGTRXP2_104	AB40	
104	MGTREFCLK0P_104	AB35	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
104	MGTREFCLK0N_104	AB36	
104	MGTTXN1_104	AD43	
104	MGTRXN1_104	AC37	
104	MGTTXP1_104	AD44	
104	MGTRXP1_104	AC38	
104	MGTTXN0_104	AE41	
104	MGTRXN0_104	AD39	
104	MGTTXP0_104	AE42	
104	MGTRXP0_104	AD40	
105	MGTTXN3_105	V43	
105	MGTRXN3_105	U37	
105	MGTTXP3_105	V44	
105	MGTRXP3_105	U38	
105	MGTTXN2_105	W41	
105	MGTRXN2_105	V39	
105	MGTTXP2_105	W42	
105	MGTREFCLK1P_105	T35	
105	MGTREFCLK1N_105	T36	
105	MGTRXP2_105	V40	
105	MGTAVTTRCAL_105	BC37	
105	MGTRREF_105	BC38	
105	MGTREFCLK0P_105	V35	
105	MGTREFCLK0N_105	V36	
105	MGTTXN1_105	Y43	
105	MGTRXN1_105	W37	
105	MGTTXP1_105	Y44	
105	MGTRXP1_105	W38	
105	MGTTXN0_105	AA41	
105	MGTRXN0_105	Y39	
105	MGTTXP0_105	AA42	
105	MGTRXP0_105	Y40	
106	MGTRXP2_106	N37	
106	MGTRXN2_106	N38	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
106	MGTTXP2_106	M43	
106	MGTTXN2_106	M44	
106	MGTRXP3_106	M39	
106	MGTRXN3_106	M40	
106	MGTTXP3_106	N41	
106	MGTTXN3_106	N42	
106	MGTRBIAS_106	R38	
106	MGTREFCLKP_106	R41	
106	MGTREFCLKN_106	R42	
106	MGTRXP1_106	T39	
106	MGTRXN1_106	T40	
106	MGTTXP1_106	P43	
106	MGTTXN1_106	P44	
106	MGTRXP0_106	U41	
106	MGTRXN0_106	U42	
106	MGTTXP0_106	T43	
106	MGTTXN0_106	T44	
107	MGTRXP2_107	H39	
107	MGTRXN2_107	H40	
107	MGTTXP2_107	G41	
107	MGTTXN2_107	G42	
107	MGTRXP3_107	J37	
107	MGTRXN3_107	J38	
107	MGTTXP3_107	H43	
107	MGTTXN3_107	H44	
107	MGTRBIAS_107	E37	
107	MGTREFCLKP_107	J41	
107	MGTREFCLKN_107	J42	
107	MGTRXP1_107	L37	
107	MGTRXN1_107	L38	
107	MGTTXP1_107	K43	
107	MGTTXN1_107	K44	
107	MGTRXP0_107	K39	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
107	MGTRXN0_107	K40	
107	MGTTXP0_107	L41	
107	MGTTXN0_107	L42	
108	MGTRXP2_108	B39	
108	MGTRXN2_108	B40	
108	MGTTXP2_108	A41	
108	MGTTXN2_108	A42	
108	MGTRXP3_108	D39	
108	MGTRXN3_108	D40	
108	MGTTXP3_108	C41	
108	MGTTXN3_108	C42	
108	MGTRBIAS_108	D37	
108	MGTREFCLKP_108	E41	
108	MGTREFCLKN_108	E42	
108	MGTRXP1_108	F39	
108	MGTRXN1_108	F40	
108	MGTTXP1_108	D43	
108	MGTTXN1_108	D44	
108	MGTRXP0_108	G37	
108	MGTRXN0_108	G38	
108	MGTTXP0_108	F43	
108	MGTTXN0_108	F44	
110	MGTTXN3_110	AV2	
110	MGTRXN3_110	BA4	
110	MGTTXP3_110	AV1	
110	MGTRXP3_110	BA3	
110	MGTTXN2_110	AW4	
110	MGTRXN2_110	BB6	
110	MGTTXP2_110	AW3	
110	MGTREFCLK1P_110	AW8	
110	MGTREFCLK1N_110	AW7	
110	MGTRXP2_110	BB5	
110	MGTREFCLK0P_110	BA8	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
110	MGTREFCLK0N_110	BA7	
110	MGTTXN1_110	AY2	
110	MGTRXN1_110	BC4	
110	MGTTXP1_110	AY1	
110	MGTRXP1_110	BC3	
110	MGTTXN0_110	BB2	
110	MGTRXN0_110	BD6	
110	MGTTXP0_110	BB1	
110	MGTRXP0_110	BD5	
111	MGTTXN3_111	AP2	
111	MGTRXN3_111	AP6	
111	MGTTXP3_111	AP1	
111	MGTRXP3_111	AP5	
111	MGTTXN2_111	AR4	
111	MGTRXN2_111	AT6	
111	MGTTXP2_111	AR3	
111	MGTREFCLK1P_111	AR8	
111	MGTREFCLK1N_111	AR7	
111	MGTRXP2_111	AT5	
111	MGTREFCLK0P_111	AU8	
111	MGTREFCLK0N_111	AU7	
111	MGTTXN1_111	AT2	
111	MGTRXN1_111	AV6	
111	MGTTXP1_111	AT1	
111	MGTRXP1_111	AV5	
111	MGTTXN0_111	AU4	
111	MGTRXN0_111	AY6	
111	MGTTXP0_111	AU3	
111	MGTRXP0_111	AY5	
112	MGTTXN3_112	AK2	
112	MGTRXN3_112	AK6	
112	MGTTXP3_112	AK1	
112	MGTRXP3_112	AK5	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
112	MGTTXN2_112	AL4	
112	MGTRXN2_112	AJ8	
112	MGTTXP2_112	AL3	
112	MGTREFCLK1P_112	AH10	
112	MGTREFCLK1N_112	AH9	
112	MGTRXP2_112	AJ7	
112	MGTREFCLK0P_112	AN8	
112	MGTREFCLK0N_112	AN7	
112	MGTTXN1_112	AM2	
112	MGTRXN1_112	AM6	
112	MGTTXP1_112	AM1	
112	MGTRXP1_112	AM5	
112	MGTTXN0_112	AN4	
112	MGTRXN0_112	AL8	
112	MGTTXP0_112	AN3	
112	MGTRXP0_112	AL7	
113	MGTTXN3_113	AF2	
113	MGTRXN3_113	AE8	
113	MGTTXP3_113	AF1	
113	MGTRXP3_113	AE7	
113	MGTTXN2_113	AG4	
113	MGTRXN2_113	AF6	
113	MGTTXP2_113	AG3	
113	MGTREFCLK1P_113	AD10	
113	MGTREFCLK1N_113	AD9	
113	MGTRXP2_113	AF5	
113	MGTREFCLK0P_113	AF10	
113	MGTREFCLK0N_113	AF9	
113	MGTTXN1_113	AH2	
113	MGTRXN1_113	AG8	
113	MGTTXP1_113	AH1	
113	MGTRXP1_113	AG7	
113	MGTTXN0_113	AJ4	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
113	MGTRXN0_113	AH6	
113	MGTTXP0_113	AJ3	
113	MGTRXP0_113	AH5	
114	MGTTXN3_114	AB2	
114	MGTRXN3_114	AA8	
114	MGTTXP3_114	AB1	
114	MGTRXP3_114	AA7	
114	MGTTXN2_114	AC4	
114	MGTRXN2_114	AB6	
114	MGTTXP2_114	AC3	
114	MGTREFCLK1P_114	Y10	
114	MGTREFCLK1N_114	Y9	
114	MGTRXP2_114	AB5	
114	MGTREFCLK0P_114	AB10	
114	MGTREFCLK0N_114	AB9	
114	MGTTXN1_114	AD2	
114	MGTRXN1_114	AC8	
114	MGTTXP1_114	AD1	
114	MGTRXP1_114	AC7	
114	MGTTXN0_114	AE4	
114	MGTRXN0_114	AD6	
114	MGTTXP0_114	AE3	
114	MGTRXP0_114	AD5	
115	MGTTXN3_115	V2	
115	MGTRXN3_115	U8	
115	MGTTXP3_115	V1	
115	MGTRXP3_115	U7	
115	MGTTXN2_115	W4	
115	MGTRXN2_115	V6	
115	MGTTXP2_115	W3	
115	MGTREFCLK1P_115	T10	
115	MGTREFCLK1N_115	T9	
115	MGTRXP2_115	V5	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
115	MGTAVTTRCAL_115	BC8	
115	MGTRREF_115	BC7	
115	MGTREFCLK0P_115	V10	
115	MGTREFCLK0N_115	V9	
115	MGTTXN1_115	Y2	
115	MGTRXN1_115	W8	
115	MGTTXP1_115	Y1	
115	MGTRXP1_115	W7	
115	MGTTXN0_115	AA4	
115	MGTRXN0_115	Y6	
115	MGTTXP0_115	AA3	
115	MGTRXP0_115	Y5	
116	MGTRXP2_116	N8	
116	MGTRXN2_116	N7	
116	MGTTXP2_116	M2	
116	MGTTXN2_116	M1	
116	MGTRXP3_116	M6	
116	MGTRXN3_116	M5	
116	MGTTXP3_116	N4	
116	MGTTXN3_116	N3	
116	MGTRBIAS_116	R7	
116	MGTREFCLKP_116	R4	
116	MGTREFCLKN_116	R3	
116	MGTRXP1_116	T6	
116	MGTRXN1_116	T5	
116	MGTTXP1_116	P2	
116	MGTTXN1_116	P1	
116	MGTRXP0_116	U4	
116	MGTRXN0_116	U3	
116	MGTTXP0_116	T2	
116	MGTTXN0_116	T1	
117	MGTRXP2_117	H6	
117	MGTRXN2_117	H5	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
117	MGTTXP2_117	G4	
117	MGTTXN2_117	G3	
117	MGTRXP3_117	J8	
117	MGTRXN3_117	J7	
117	MGTTXP3_117	H2	
117	MGTTXN3_117	H1	
117	MGTRBIAS_117	E8	
117	MGTREFCLKP_117	J4	
117	MGTREFCLKN_117	J3	
117	MGTRXP1_117	L8	
117	MGTRXN1_117	L7	
117	MGTTXP1_117	K2	
117	MGTTXN1_117	K1	
117	MGTRXP0_117	K6	
117	MGTRXN0_117	K5	
117	MGTTXP0_117	L4	
117	MGTTXN0_117	L3	
118	MGTRXP2_118	B6	
118	MGTRXN2_118	B5	
118	MGTTXP2_118	A4	
118	MGTTXN2_118	A3	
118	MGTRXP3_118	D6	
118	MGTRXN3_118	D5	
118	MGTTXP3_118	C4	
118	MGTTXN3_118	C3	
118	MGTRBIAS_118	D8	
118	MGTREFCLKP_118	E4	
118	MGTREFCLKN_118	E3	
118	MGTRXP1_118	F6	
118	MGTRXN1_118	F5	
118	MGTTXP1_118	D2	
118	MGTTXN1_118	D1	
118	MGTRXP0_118	G8	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
118	MGTRXN0_118	G7	
118	MGTTPXPO_118	F2	
118	MGTTXN0_118	F1	
NA	MGTHAVCCPLL_L	H37	
NA	MGTHAVCCPLL_L	K37	
NA	MGTHAVCCPLL_L	M37	
NA	MGTHAVCCPLL_R	H8	
NA	MGTHAVCCPLL_R	K8	
NA	MGTHAVCCPLL_R	M8	
NA	MGTAVCC_LN	AA36	
NA	MGTAVCC_LN	AC36	
NA	MGTAVCC_LN	AE36	
NA	MGTAVCC_LN	AG36	
NA	MGTAVCC_LN	U36	
NA	MGTAVCC_LN	V37	
NA	MGTAVCC_LN	W36	
NA	MGTAVCC_LS	AK37	
NA	MGTAVCC_LS	AM37	
NA	MGTAVCC_LS	AP37	
NA	MGTAVCC_LS	AT37	
NA	MGTAVCC_LS	AV37	
NA	MGTAVCC_LS	AY37	
NA	MGTAVCC_LS	BB37	
NA	MGTAVCC_RN	AA9	
NA	MGTAVCC_RN	AC9	
NA	MGTAVCC_RN	AE9	
NA	MGTAVCC_RN	AG9	
NA	MGTAVCC_RN	U9	
NA	MGTAVCC_RN	V8	
NA	MGTAVCC_RN	W9	
NA	MGTAVCC_RS	AK8	
NA	MGTAVCC_RS	AM8	
NA	MGTAVCC_RS	AP8	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTAVCC_RS	AT8	
NA	MGTAVCC_RS	AV8	
NA	MGTAVCC_RS	AY8	
NA	MGTAVCC_RS	BB8	
NA	MGTAVTT_LN	AB41	
NA	MGTAVTT_LN	AC43	
NA	MGTAVTT_LN	AD42	
NA	MGTAVTT_LN	AF41	
NA	MGTAVTT_LN	AG43	
NA	MGTAVTT_LN	AH42	
NA	MGTAVTT_LN	W43	
NA	MGTAVTT_LN	Y42	
NA	MGTAVTT_LS	AN43	
NA	MGTAVTT_LS	AP42	
NA	MGTAVTT_LS	AT41	
NA	MGTAVTT_LS	AU43	
NA	MGTAVTT_LS	AV42	
NA	MGTAVTT_LS	AY41	
NA	MGTAVTT_LS	BA43	
NA	MGTAVTT_LS	BB42	
NA	MGTAVTT_RN	AB4	
NA	MGTAVTT_RN	AC2	
NA	MGTAVTT_RN	AD3	
NA	MGTAVTT_RN	AF4	
NA	MGTAVTT_RN	AG2	
NA	MGTAVTT_RN	AH3	
NA	MGTAVTT_RN	W2	
NA	MGTAVTT_RN	Y3	
NA	MGTAVTT_RS	AN2	
NA	MGTAVTT_RS	AP3	
NA	MGTAVTT_RS	AT4	
NA	MGTAVTT_RS	AU2	
NA	MGTAVTT_RS	AV3	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTAVTT_RS	AY4	
NA	MGTAVTT_RS	BA2	
NA	MGTAVTT_RS	BB3	
NA	MGTHAVCCRX_L	A39	
NA	MGTHAVCCRX_L	C39	
NA	MGTHAVCCRX_L	F37	
NA	MGTHAVCCRX_L	G39	
NA	MGTHAVCCRX_L	J39	
NA	MGTHAVCCRX_L	L39	
NA	MGTHAVCCRX_L	P37	
NA	MGTHAVCCRX_L	R39	
NA	MGTHAVCCRX_R	A6	
NA	MGTHAVCCRX_R	C6	
NA	MGTHAVCCRX_R	F8	
NA	MGTHAVCCRX_R	G6	
NA	MGTHAVCCRX_R	J6	
NA	MGTHAVCCRX_R	L6	
NA	MGTHAVCCRX_R	P8	
NA	MGTHAVCCRX_R	R6	
NA	MGTHAVTT_L	E43	
NA	MGTHAVTT_L	J43	
NA	MGTHAVTT_L	L43	
NA	MGTHAVTT_L	R43	
NA	MGTHAVTT_R	E2	
NA	MGTHAVTT_R	J2	
NA	MGTHAVTT_R	L2	
NA	MGTHAVTT_R	R2	
NA	MGTHAVCC_L	B41	
NA	MGTHAVCC_L	D41	
NA	MGTHAVCC_L	E39	
NA	MGTHAVCC_L	F41	
NA	MGTHAVCC_L	H41	
NA	MGTHAVCC_L	K41	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTHAVCC_L	M41	
NA	MGTHAVCC_L	N39	
NA	MGTHAVCC_L	P41	
NA	MGTHAVCC_L	T41	
NA	MGTHAVCC_R	B4	
NA	MGTHAVCC_R	D4	
NA	MGTHAVCC_R	E6	
NA	MGTHAVCC_R	F4	
NA	MGTHAVCC_R	H4	
NA	MGTHAVCC_R	K4	
NA	MGTHAVCC_R	M4	
NA	MGTHAVCC_R	N6	
NA	MGTHAVCC_R	P4	
NA	MGTHAVCC_R	T4	
NA	MGTHAGND_L	A40	
NA	MGTHAGND_L	B42	
NA	MGTHAGND_L	B43	
NA	MGTHAGND_L	C40	
NA	MGTHAGND_L	C43	
NA	MGTHAGND_L	C44	
NA	MGTHAGND_L	D38	
NA	MGTHAGND_L	D42	
NA	MGTHAGND_L	E38	
NA	MGTHAGND_L	E40	
NA	MGTHAGND_L	E44	
NA	MGTHAGND_L	F38	
NA	MGTHAGND_L	F42	
NA	MGTHAGND_L	G40	
NA	MGTHAGND_L	G43	
NA	MGTHAGND_L	G44	
NA	MGTHAGND_L	H38	
NA	MGTHAGND_L	H42	
NA	MGTHAGND_L	J40	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTHAGND_L	J44	
NA	MGTHAGND_L	K38	
NA	MGTHAGND_L	K42	
NA	MGTHAGND_L	L40	
NA	MGTHAGND_L	L44	
NA	MGTHAGND_L	M38	
NA	MGTHAGND_L	M42	
NA	MGTHAGND_L	N40	
NA	MGTHAGND_L	N43	
NA	MGTHAGND_L	N44	
NA	MGTHAGND_L	P38	
NA	MGTHAGND_L	P42	
NA	MGTHAGND_L	R40	
NA	MGTHAGND_L	R44	
NA	MGTHAGND_L	T38	
NA	MGTHAGND_L	T42	
NA	MGTHAGND_L	U39	
NA	MGTHAGND_L	U40	
NA	MGTHAGND_L	U43	
NA	MGTHAGND_L	U44	
NA	MGTHAGND_L	V41	
NA	MGTHAGND_R	A5	
NA	MGTHAGND_R	B2	
NA	MGTHAGND_R	B3	
NA	MGTHAGND_R	C1	
NA	MGTHAGND_R	C2	
NA	MGTHAGND_R	C5	
NA	MGTHAGND_R	D3	
NA	MGTHAGND_R	D7	
NA	MGTHAGND_R	E1	
NA	MGTHAGND_R	E5	
NA	MGTHAGND_R	E7	
NA	MGTHAGND_R	F3	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	MGTHAGND_R	F7	
NA	MGTHAGND_R	G1	
NA	MGTHAGND_R	G2	
NA	MGTHAGND_R	G5	
NA	MGTHAGND_R	H3	
NA	MGTHAGND_R	H7	
NA	MGTHAGND_R	J1	
NA	MGTHAGND_R	J5	
NA	MGTHAGND_R	K3	
NA	MGTHAGND_R	K7	
NA	MGTHAGND_R	L1	
NA	MGTHAGND_R	L5	
NA	MGTHAGND_R	M3	
NA	MGTHAGND_R	M7	
NA	MGTHAGND_R	N1	
NA	MGTHAGND_R	N2	
NA	MGTHAGND_R	N5	
NA	MGTHAGND_R	P3	
NA	MGTHAGND_R	P7	
NA	MGTHAGND_R	R1	
NA	MGTHAGND_R	R5	
NA	MGTHAGND_R	T3	
NA	MGTHAGND_R	T7	
NA	MGTHAGND_R	U1	
NA	MGTHAGND_R	U2	
NA	MGTHAGND_R	U5	
NA	MGTHAGND_R	U6	
NA	MGTHAGND_R	V4	
NA	GND	A7	
NA	GND	A16	
NA	GND	A26	
NA	GND	A36	
NA	GND	A38	

Table 2-9: FF1924 Package—HX380T and HX565T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AA1	
NA	GND	AA2	
NA	GND	AA5	
NA	GND	AA6	
NA	GND	AA10	
NA	GND	AA11	
NA	GND	AA15	
NA	GND	AA17	
NA	GND	AA19	
NA	GND	AA21	
NA	GND	AA25	
NA	GND	AA27	
NA	GND	AA29	
NA	GND	AA31	
NA	GND	AA33	
NA	GND	AA34	
NA	GND	AA35	
NA	GND	AA39	
NA	GND	AA40	
NA	GND	AA43	
NA	GND	AA44	
NA	GND	AB3	
NA	GND	AB7	
NA	GND	AB8	
NA	GND	AB11	
NA	GND	AB12	
NA	GND	AB14	
NA	GND	AB16	
NA	GND	AB18	
NA	GND	AB20	
NA	GND	AB24	
NA	GND	AB26	
NA	GND	AB28	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AB30	
NA	GND	AB32	
NA	GND	AB34	
NA	GND	AB37	
NA	GND	AB38	
NA	GND	AB42	
NA	GND	AC1	
NA	GND	AC5	
NA	GND	AC6	
NA	GND	AC10	
NA	GND	AC11	
NA	GND	AC13	
NA	GND	AC15	
NA	GND	AC17	
NA	GND	AC19	
NA	GND	AC21	
NA	GND	AC25	
NA	GND	AC27	
NA	GND	AC29	
NA	GND	AC31	
NA	GND	AC33	
NA	GND	AC34	
NA	GND	AC35	
NA	GND	AC39	
NA	GND	AC40	
NA	GND	AC44	
NA	GND	AD4	
NA	GND	AD7	
NA	GND	AD8	
NA	GND	AD11	
NA	GND	AD12	
NA	GND	AD14	
NA	GND	AD16	

Table 2-9: FF1924 Package—HX380T and HX565T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AD18	
NA	GND	AD20	
NA	GND	AD24	
NA	GND	AD26	
NA	GND	AD28	
NA	GND	AD30	
NA	GND	AD32	
NA	GND	AD34	
NA	GND	AD37	
NA	GND	AD38	
NA	GND	AD41	
NA	GND	AE1	
NA	GND	AE2	
NA	GND	AE5	
NA	GND	AE6	
NA	GND	AE10	
NA	GND	AE11	
NA	GND	AE13	
NA	GND	AE15	
NA	GND	AE17	
NA	GND	AE19	
NA	GND	AE21	
NA	GND	AE23	
NA	GND	AE25	
NA	GND	AE27	
NA	GND	AE29	
NA	GND	AE31	
NA	GND	AE33	
NA	GND	AE34	
NA	GND	AE35	
NA	GND	AE39	
NA	GND	AE40	
NA	GND	AE43	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AE44	
NA	GND	AF3	
NA	GND	AF7	
NA	GND	AF8	
NA	GND	AF11	
NA	GND	AF12	
NA	GND	AF14	
NA	GND	AF16	
NA	GND	AF18	
NA	GND	AF20	
NA	GND	AF22	
NA	GND	AF24	
NA	GND	AF26	
NA	GND	AF28	
NA	GND	AF30	
NA	GND	AF32	
NA	GND	AF34	
NA	GND	AF37	
NA	GND	AF38	
NA	GND	AF42	
NA	GND	AG1	
NA	GND	AG5	
NA	GND	AG6	
NA	GND	AG10	
NA	GND	AG11	
NA	GND	AG13	
NA	GND	AG15	
NA	GND	AG17	
NA	GND	AG19	
NA	GND	AG21	
NA	GND	AG23	
NA	GND	AG25	
NA	GND	AG27	

Table 2-9: FF1924 Package—HX380T and HX565T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AG29	
NA	GND	AG31	
NA	GND	AG33	
NA	GND	AG34	
NA	GND	AG35	
NA	GND	AG39	
NA	GND	AG40	
NA	GND	AG44	
NA	GND	AH4	
NA	GND	AH7	
NA	GND	AH8	
NA	GND	AH11	
NA	GND	AH14	
NA	GND	AH16	
NA	GND	AH18	
NA	GND	AH20	
NA	GND	AH22	
NA	GND	AH24	
NA	GND	AH26	
NA	GND	AH28	
NA	GND	AH30	
NA	GND	AH34	
NA	GND	AH37	
NA	GND	AH38	
NA	GND	AH41	
NA	GND	AJ1	
NA	GND	AJ2	
NA	GND	AJ5	
NA	GND	AJ6	
NA	GND	AJ9	
NA	GND	AJ10	
NA	GND	AJ11	
NA	GND	AJ12	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AJ21	
NA	GND	AJ23	
NA	GND	AJ32	
NA	GND	AJ34	
NA	GND	AJ35	
NA	GND	AJ36	
NA	GND	AJ39	
NA	GND	AJ40	
NA	GND	AJ43	
NA	GND	AJ44	
NA	GND	AK3	
NA	GND	AK4	
NA	GND	AK7	
NA	GND	AK9	
NA	GND	AK19	
NA	GND	AK29	
NA	GND	AK36	
NA	GND	AK38	
NA	GND	AK41	
NA	GND	AK42	
NA	GND	AL1	
NA	GND	AL2	
NA	GND	AL5	
NA	GND	AL6	
NA	GND	AL9	
NA	GND	AL16	
NA	GND	AL26	
NA	GND	AL36	
NA	GND	AL39	
NA	GND	AL40	
NA	GND	AL43	
NA	GND	AL44	
NA	GND	AM3	

Table 2-9: FF1924 Package—HX380T and HX565T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AM4	
NA	GND	AM7	
NA	GND	AM9	
NA	GND	AM13	
NA	GND	AM23	
NA	GND	AM33	
NA	GND	AM36	
NA	GND	AM38	
NA	GND	AM41	
NA	GND	AM42	
NA	GND	AN1	
NA	GND	AN5	
NA	GND	AN6	
NA	GND	AN9	
NA	GND	AN10	
NA	GND	AN20	
NA	GND	AN30	
NA	GND	AN36	
NA	GND	AN39	
NA	GND	AN40	
NA	GND	AN44	
NA	GND	AP4	
NA	GND	AP7	
NA	GND	AP9	
NA	GND	AP17	
NA	GND	AP27	
NA	GND	AP36	
NA	GND	AP38	
NA	GND	AP41	
NA	GND	AR1	
NA	GND	AR2	
NA	GND	AR5	
NA	GND	AR6	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AR9	
NA	GND	AR14	
NA	GND	AR24	
NA	GND	AR34	
NA	GND	AR36	
NA	GND	AR39	
NA	GND	AR40	
NA	GND	AR43	
NA	GND	AR44	
NA	GND	AT3	
NA	GND	AT7	
NA	GND	AT9	
NA	GND	AT11	
NA	GND	AT21	
NA	GND	AT31	
NA	GND	AT36	
NA	GND	AT38	
NA	GND	AT42	
NA	GND	AU1	
NA	GND	AU5	
NA	GND	AU6	
NA	GND	AU9	
NA	GND	AU18	
NA	GND	AU28	
NA	GND	AU36	
NA	GND	AU39	
NA	GND	AU40	
NA	GND	AU44	
NA	GND	AV4	
NA	GND	AV7	
NA	GND	AV9	
NA	GND	AV15	
NA	GND	AV25	

Table 2-9: FF1924 Package—HX380T and HX565T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	AV35	
NA	GND	AV36	
NA	GND	AV38	
NA	GND	AV41	
NA	GND	AW1	
NA	GND	AW2	
NA	GND	AW5	
NA	GND	AW6	
NA	GND	AW9	
NA	GND	AW12	
NA	GND	AW22	
NA	GND	AW32	
NA	GND	AW36	
NA	GND	AW39	
NA	GND	AW40	
NA	GND	AW43	
NA	GND	AW44	
NA	GND	AY3	
NA	GND	AY7	
NA	GND	AY9	
NA	GND	AY19	
NA	GND	AY29	
NA	GND	AY36	
NA	GND	AY38	
NA	GND	AY42	
NA	GND	B7	
NA	GND	B13	
NA	GND	B23	
NA	GND	B33	
NA	GND	B38	
NA	GND	BA1	
NA	GND	BA5	
NA	GND	BA6	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	BA9	
NA	GND	BA16	
NA	GND	BA26	
NA	GND	BA36	
NA	GND	BA39	
NA	GND	BA40	
NA	GND	BA44	
NA	GND	BB4	
NA	GND	BB7	
NA	GND	BB9	
NA	GND	BB13	
NA	GND	BB23	
NA	GND	BB33	
NA	GND	BB36	
NA	GND	BB38	
NA	GND	BB41	
NA	GND	BC2	
NA	GND	BC5	
NA	GND	BC6	
NA	GND	BC9	
NA	GND	BC10	
NA	GND	BC20	
NA	GND	BC30	
NA	GND	BC36	
NA	GND	BC39	
NA	GND	BC40	
NA	GND	BC43	
NA	GND	BD3	
NA	GND	BD4	
NA	GND	BD7	
NA	GND	BD8	
NA	GND	BD9	
NA	GND	BD17	

Table 2-9: FF1924 Package—HX380T and HX565T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	BD27	
NA	GND	BD36	
NA	GND	BD37	
NA	GND	BD38	
NA	GND	BD41	
NA	GND	BD42	
NA	GND	C7	
NA	GND	C8	
NA	GND	C9	
NA	GND	C10	
NA	GND	C20	
NA	GND	C30	
NA	GND	C36	
NA	GND	C37	
NA	GND	C38	
NA	GND	D9	
NA	GND	D17	
NA	GND	D27	
NA	GND	D36	
NA	GND	E9	
NA	GND	E14	
NA	GND	E24	
NA	GND	E34	
NA	GND	E36	
NA	GND	F9	
NA	GND	F11	
NA	GND	F21	
NA	GND	F31	
NA	GND	F36	
NA	GND	G9	
NA	GND	G18	
NA	GND	G28	
NA	GND	G36	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	H9	
NA	GND	H15	
NA	GND	H25	
NA	GND	H35	
NA	GND	H36	
NA	GND	J9	
NA	GND	J12	
NA	GND	J22	
NA	GND	J32	
NA	GND	J36	
NA	GND	K9	
NA	GND	K19	
NA	GND	K29	
NA	GND	K36	
NA	GND	L9	
NA	GND	L16	
NA	GND	L26	
NA	GND	L36	
NA	GND	M9	
NA	GND	M13	
NA	GND	M23	
NA	GND	M33	
NA	GND	M36	
NA	GND	N9	
NA	GND	N10	
NA	GND	N20	
NA	GND	N30	
NA	GND	N36	
NA	GND	P9	
NA	GND	P17	
NA	GND	P27	
NA	GND	P36	
NA	GND	R9	

Table 2-9: FF1924 Package—HX380T and HX565T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	R10	
NA	GND	R11	
NA	GND	R14	
NA	GND	R24	
NA	GND	R34	
NA	GND	R35	
NA	GND	R36	
NA	GND	T8	
NA	GND	T11	
NA	GND	T18	
NA	GND	T20	
NA	GND	T22	
NA	GND	T24	
NA	GND	T28	
NA	GND	T31	
NA	GND	T34	
NA	GND	T37	
NA	GND	U10	
NA	GND	U11	
NA	GND	U15	
NA	GND	U17	
NA	GND	U19	
NA	GND	U21	
NA	GND	U23	
NA	GND	U25	
NA	GND	U27	
NA	GND	U29	
NA	GND	U31	
NA	GND	U34	
NA	GND	U35	
NA	GND	V3	
NA	GND	V7	
NA	GND	V11	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	V14	
NA	GND	V16	
NA	GND	V18	
NA	GND	V20	
NA	GND	V22	
NA	GND	V24	
NA	GND	V26	
NA	GND	V28	
NA	GND	V30	
NA	GND	V34	
NA	GND	V38	
NA	GND	V42	
NA	GND	W1	
NA	GND	W5	
NA	GND	W6	
NA	GND	W10	
NA	GND	W11	
NA	GND	W15	
NA	GND	W17	
NA	GND	W19	
NA	GND	W21	
NA	GND	W23	
NA	GND	W25	
NA	GND	W27	
NA	GND	W29	
NA	GND	W31	
NA	GND	W34	
NA	GND	W35	
NA	GND	W39	
NA	GND	W40	
NA	GND	W44	
NA	GND	Y4	
NA	GND	Y7	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	GND	Y8	
NA	GND	Y11	
NA	GND	Y12	
NA	GND	Y14	
NA	GND	Y16	
NA	GND	Y18	
NA	GND	Y20	
NA	GND	Y22	
NA	GND	Y24	
NA	GND	Y26	
NA	GND	Y28	
NA	GND	Y30	
NA	GND	Y32	
NA	GND	Y34	
NA	GND	Y37	
NA	GND	Y38	
NA	GND	Y41	
NA	VCCAUX	AA12	
NA	VCCAUX	AA32	
NA	VCCAUX	AB13	
NA	VCCAUX	AB33	
NA	VCCAUX	AC12	
NA	VCCAUX	AC32	
NA	VCCAUX	AD13	
NA	VCCAUX	AD33	
NA	VCCAUX	AE12	
NA	VCCAUX	AE32	
NA	VCCAUX	AF13	
NA	VCCAUX	AF33	
NA	VCCAUX	AG12	
NA	VCCAUX	AG32	
NA	VCCAUX	AH13	
NA	VCCAUX	AH33	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCAUX	U12	
NA	VCCAUX	U32	
NA	VCCAUX	V13	
NA	VCCAUX	V33	
NA	VCCAUX	W12	
NA	VCCAUX	W32	
NA	VCCAUX	Y13	
NA	VCCAUX	Y33	
NA	VCCINT	AA14	
NA	VCCINT	AA16	
NA	VCCINT	AA18	
NA	VCCINT	AA20	
NA	VCCINT	AA24	
NA	VCCINT	AA26	
NA	VCCINT	AA28	
NA	VCCINT	AA30	
NA	VCCINT	AB15	
NA	VCCINT	AB17	
NA	VCCINT	AB19	
NA	VCCINT	AB21	
NA	VCCINT	AB25	
NA	VCCINT	AB27	
NA	VCCINT	AB29	
NA	VCCINT	AB31	
NA	VCCINT	AC14	
NA	VCCINT	AC16	
NA	VCCINT	AC18	
NA	VCCINT	AC20	
NA	VCCINT	AC24	
NA	VCCINT	AC26	
NA	VCCINT	AC28	
NA	VCCINT	AC30	
NA	VCCINT	AD15	

Table 2-9: FF1924 Package—HX380T and HX565T (*Cont'd*)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	AD17	
NA	VCCINT	AD19	
NA	VCCINT	AD21	
NA	VCCINT	AD25	
NA	VCCINT	AD27	
NA	VCCINT	AD29	
NA	VCCINT	AD31	
NA	VCCINT	AE14	
NA	VCCINT	AE16	
NA	VCCINT	AE18	
NA	VCCINT	AE20	
NA	VCCINT	AE22	
NA	VCCINT	AE24	
NA	VCCINT	AE26	
NA	VCCINT	AE28	
NA	VCCINT	AE30	
NA	VCCINT	AF15	
NA	VCCINT	AF17	
NA	VCCINT	AF19	
NA	VCCINT	AF21	
NA	VCCINT	AF23	
NA	VCCINT	AF25	
NA	VCCINT	AF27	
NA	VCCINT	AF29	
NA	VCCINT	AF31	
NA	VCCINT	AG14	
NA	VCCINT	AG16	
NA	VCCINT	AG18	
NA	VCCINT	AG20	
NA	VCCINT	AG22	
NA	VCCINT	AG24	
NA	VCCINT	AG26	
NA	VCCINT	AG28	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	AG30	
NA	VCCINT	AH15	
NA	VCCINT	AH17	
NA	VCCINT	AH19	
NA	VCCINT	AH21	
NA	VCCINT	AH23	
NA	VCCINT	AH25	
NA	VCCINT	AH27	
NA	VCCINT	AH29	
NA	VCCINT	AH31	
NA	VCCINT	AJ22	
NA	VCCINT	AJ24	
NA	VCCINT	T19	
NA	VCCINT	T21	
NA	VCCINT	T23	
NA	VCCINT	T25	
NA	VCCINT	U14	
NA	VCCINT	U16	
NA	VCCINT	U18	
NA	VCCINT	U20	
NA	VCCINT	U22	
NA	VCCINT	U24	
NA	VCCINT	U26	
NA	VCCINT	U28	
NA	VCCINT	U30	
NA	VCCINT	V15	
NA	VCCINT	V17	
NA	VCCINT	V19	
NA	VCCINT	V21	
NA	VCCINT	V23	
NA	VCCINT	V25	
NA	VCCINT	V27	
NA	VCCINT	V29	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
NA	VCCINT	V31	
NA	VCCINT	W14	
NA	VCCINT	W16	
NA	VCCINT	W18	
NA	VCCINT	W20	
NA	VCCINT	W22	
NA	VCCINT	W24	
NA	VCCINT	W26	
NA	VCCINT	W28	
NA	VCCINT	W30	
NA	VCCINT	Y15	
NA	VCCINT	Y17	
NA	VCCINT	Y19	
NA	VCCINT	Y21	
NA	VCCINT	Y23	
NA	VCCINT	Y25	
NA	VCCINT	Y27	
NA	VCCINT	Y29	
NA	VCCINT	Y31	
0	VCCO_0	T12	
0	VCCO_0	V12	
21	VCCO_21	AK24	
21	VCCO_21	AN25	
21	VCCO_21	AU23	
21	VCCO_21	AY24	
21	VCCO_21	BC25	
22	VCCO_22	AJ27	
22	VCCO_22	AM28	
22	VCCO_22	AT26	
22	VCCO_22	AW27	
22	VCCO_22	BB28	
23	VCCO_23	AL31	
23	VCCO_23	AR29	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
23	VCCO_23	AV30	
23	VCCO_23	BA31	
23	VCCO_23	BD32	
24	VCCO_24	AK34	
24	VCCO_24	AN35	
24	VCCO_24	AP32	
24	VCCO_24	AU33	
24	VCCO_24	AY34	
24	VCCO_24	BC35	
25	VCCO_25	C35	
25	VCCO_25	G33	
25	VCCO_25	K34	
25	VCCO_25	N35	
25	VCCO_25	P32	
26	VCCO_26	A31	
26	VCCO_26	D32	
26	VCCO_26	H30	
26	VCCO_26	L31	
26	VCCO_26	R29	
27	VCCO_27	B28	
27	VCCO_27	E29	
27	VCCO_27	J27	
27	VCCO_27	M28	
27	VCCO_27	T26	
28	VCCO_28	C25	
28	VCCO_28	F26	
28	VCCO_28	G23	
28	VCCO_28	K24	
28	VCCO_28	N25	
31	VCCO_31	AL21	
31	VCCO_31	AP22	
31	VCCO_31	AV20	
31	VCCO_31	BA21	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
31	VCCO_31	BD22	
32	VCCO_32	AJ17	
32	VCCO_32	AM18	
32	VCCO_32	AR19	
32	VCCO_32	AW17	
32	VCCO_32	BB18	
33	VCCO_33	AK14	
33	VCCO_33	AN15	
33	VCCO_33	AT16	
33	VCCO_33	AU13	
33	VCCO_33	AY14	
33	VCCO_33	BC15	
34	VCCO_34	AL11	
34	VCCO_34	AP12	
34	VCCO_34	AV10	
34	VCCO_34	BA11	
34	VCCO_34	BD12	
35	VCCO_35	A11	
35	VCCO_35	B8	
35	VCCO_35	D12	
35	VCCO_35	H10	
35	VCCO_35	L11	
35	VCCO_35	P12	
36	VCCO_36	C15	
36	VCCO_36	F16	
36	VCCO_36	G13	
36	VCCO_36	K14	
36	VCCO_36	N15	
37	VCCO_37	E19	
37	VCCO_37	J17	
37	VCCO_37	M18	
37	VCCO_37	R19	
37	VCCO_37	T16	

Table 2-9: FF1924 Package—HX380T and HX565T (Cont'd)

Bank	Pin Description	Pin Number	No Connect (NC)
38	VCCO_38	A21	
38	VCCO_38	B18	
38	VCCO_38	D22	
38	VCCO_38	H20	
38	VCCO_38	L21	
38	VCCO_38	P22	
NA	RSVD	R37	
NA	RSVD	P39	
NA	RSVD	P40	
NA	RSVD	R8	
NA	RSVD	P6	
NA	RSVD	P5	

Pinout and I/O Bank Diagrams

Summary

This chapter provides pinout diagrams for each Virtex-6 FPGA package/device combination.

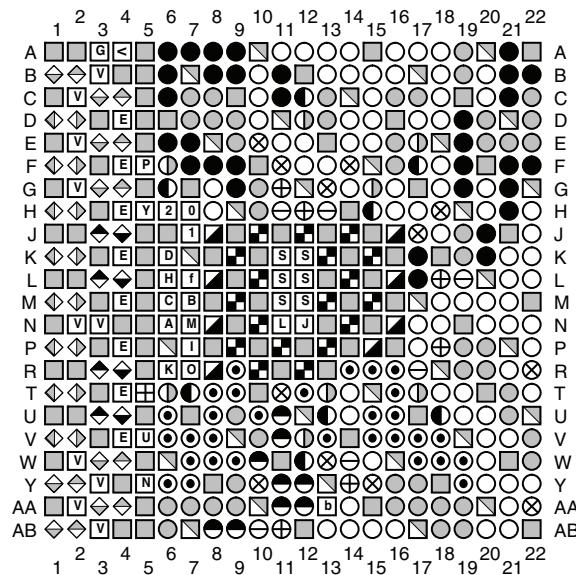
- FF484 Package—LX75T and LX130T, page 408
- FF784 Package—LX75T, page 410
- FF784/RF784 Package—LX130T, LX195T, and LX240T, page 412
- FF1154 Package—HX250T and HX380T, page 414
- FF1155 Package—HX255T and HX380T, page 416
- FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315, and SX475T, page 418
- FF1759/RF1759 Package—LX240T, LX365T, and SX315T, page 420
- FF1759/RF1759 Package—LX550T and SX475T, page 422
- FF1760 Package—LX550T, page 424
- FF1760 Package—LX760, page 426
- FF1923 Package—HX255T, page 428
- FF1923 Package—HX380T and HX565T, page 430
- FF1924 Package—HX380T and HX565T, page 432

Multi-function I/O pins are represented in these diagrams by symbols for only one of the pins available functions, with precedence given to functionality in the following order:

- VREF, VRP, or VRN
- GC
- CC
- D0–D31
- A0–A25

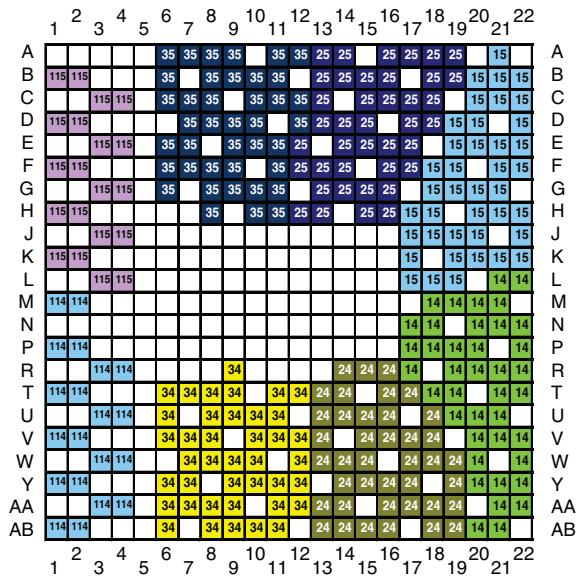
For example, a pin description such as IO_L8P_SRCC_12 is represented with a CC symbol, a pin description such as IO_L4N_VREF_12 is represented with a VREF symbol, and a pin description such as IO_L2P_A15_D31_34 is represented with a D0–D31 symbol.

FF484 Package—LX75T and LX130T



User I/O Pins	Multi-Function Pins	Transceiver Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#	<ul style="list-style-type: none"> ● SM ⊗ VREF ⊕ VRN ⊖ VRP ∅ P_GC ● N_GC ● CC ● D0 - D31 ● A0 - A25 ■ CSO_B 	<ul style="list-style-type: none"> ■ MGTAVCC ■ MGTAVTT ■ MGTAVTTRCAL ◆ MGTREFCLKP ◆ MGTREFCLKN ■ MGTRREF ◆ MGTRXP ◆ MGTRXN ◆ MGTTXN ◆ MGTTXP 	<ul style="list-style-type: none"> □ CCLK ■ CSI_B ■ DIN □ DONE ■ DOUT_BUSY ■ HSWAPEN ■ INIT ■ M2, M1, M0 ■ AVDD, AVSS, VP, VN, VREFP, VREFN □ DXN 	<ul style="list-style-type: none"> ■ GND ■ VFS ■ VBATT ■ VCCAUX ■ VCCINT ■ VCCO ■ NC ■ FLOAT

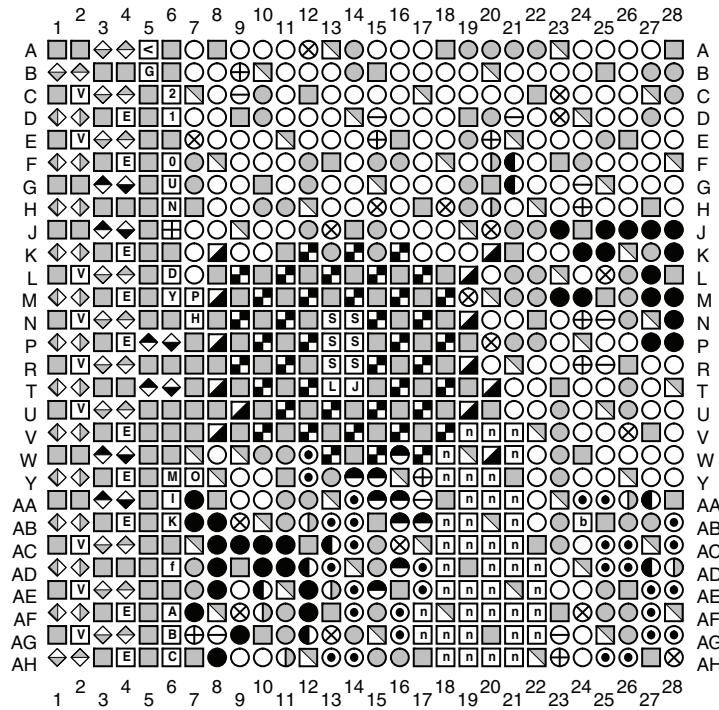
Figure 3.1: EE484 Package – LX7ET and LX130T Pinout Diagram



UG365_c3_02_091509

Figure 3-2: FF484 Package—LX75T and LX130T I/O Bank Diagram

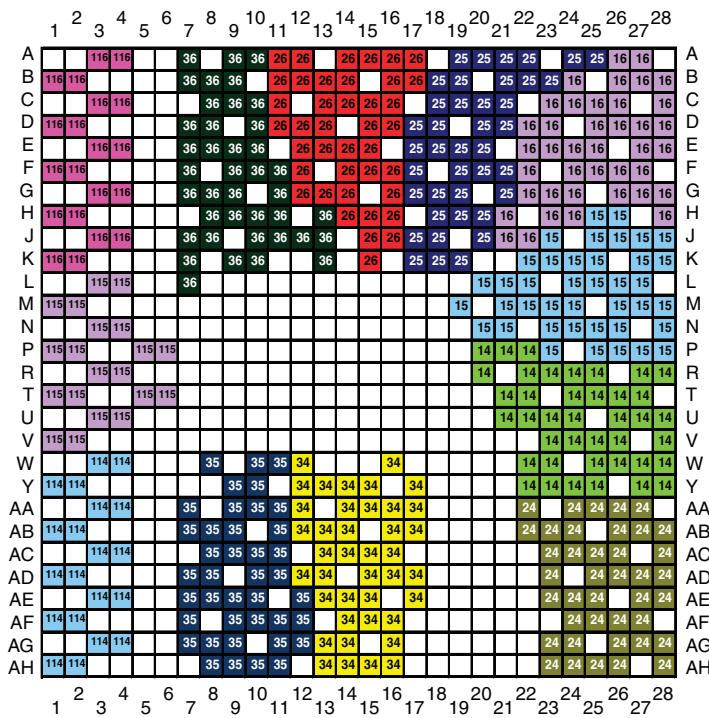
FF784 Package—LX75T



User I/O Pins	Multi-Function Pins	Transceiver Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#	<ul style="list-style-type: none"> ● SM ⊗ VREF ⊕ VRN ⊖ VRP ∅ P_GC ● N_GC ● CC ● D0 - D31 ● A0 - A25 ■ CSO_B 	<ul style="list-style-type: none"> ■ MGTAVCC ■ MGTAVTT ■ MGTAVTTRCAL ◆ MGTREFCLKP ◆ MGTREFCLKN ■ MGTRREF ◆ MGTRXP ◆ MGTRXN ◆ MGTTXN ◆ MGTTXP 	<ul style="list-style-type: none"> □ CCLK □ CSI_B □ DIN □ DONE □ HSWAPEN □ INIT □ M2, M1, M0 □ AVDD, AVSS, VP, VN, VREFP, VREFN □ PROGRAM_B □ RDWR □ TCK □ TDI □ TDO □ TMS □ DXP □ DXN 	<ul style="list-style-type: none"> □ GND □ VFS □ VBATT ■ VCCAUX ■ VCCINT □ VCO □ NC □ FLOAT

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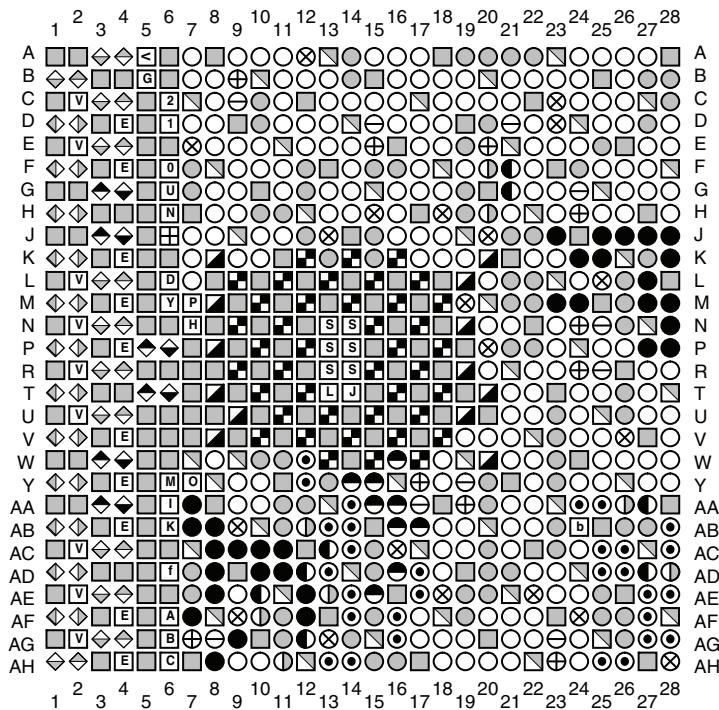
Figure 3-3: FF784 Package—LX75T Pinout Diagram



UG365_c3_04_091509

Figure 3-4: FF784 Package—LX75T I/O Bank Diagram

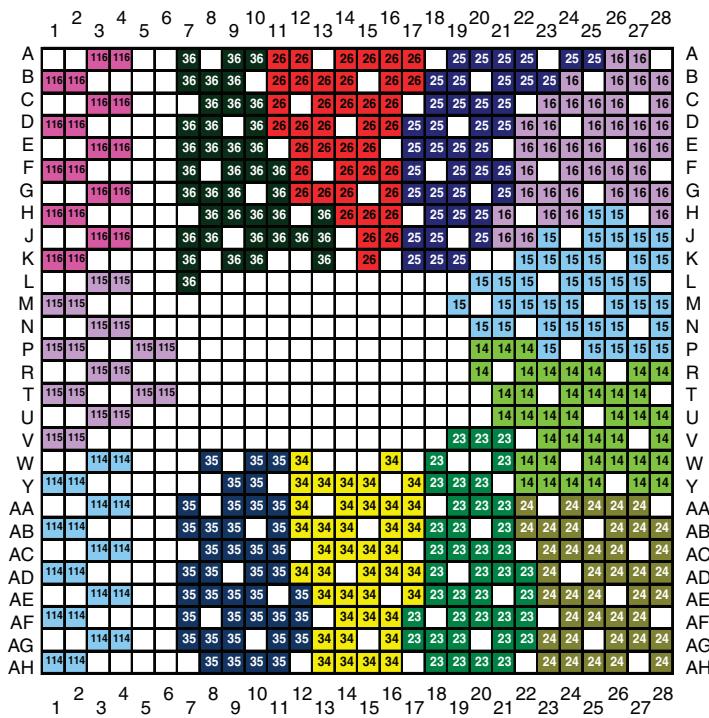
FF784/RF784 Package—LX130T, LX195T, and LX240T



User I/O Pins	Multi-Function Pins	Transceiver Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#	● SM ⊗ VREF ⊕ VRN ⊖ VRP ∅ P_GC ● N_GC ○ CC ◎ D0 - D31 ● A0 - A25 ■ CSO_B	■ MGTAVCC ■ MGTAVTT ■ MGTAVTRCAL ◆ MGTREFCLKP ◆ MGTREFCLKN ■ MGTRREF ◆ MGTRXP ◆ MGTRXN ◆ MGTTXN ◆ MGTTXP	□ CCLK ■ CSI_B ■ DIN □ DONE ■ HSWAPEN ■ INIT ■ 210 M2, M1, M0 ■ S AVDD, AVSS, VP, VN, VREFP, VREFN	□ PROGRAM_B □ RDWR □ TCK □ TDI □ TDO □ TMS □ DXP □ DXN ■ GND ■ VFS ■ VBATT ■ VCCAUX ■ VCCINT ■ VCCO □ NC ■ FLOAT

UG365_c3_05_061309

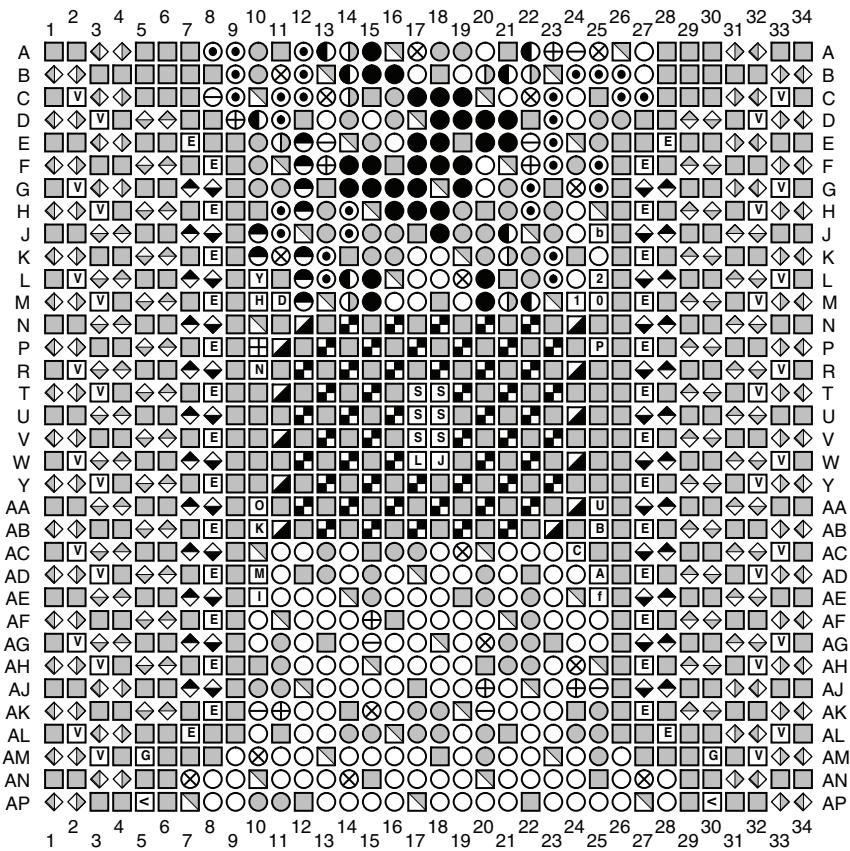
Figure 3-5: FF784/RF784 Package—LX130T, LX195T, and LX240T Pinout Diagram



UG365_c3_06_091509

Figure 3-6: FF784/RF784 Package—LX130T, LX195T, and LX240T I/O Bank Diagram

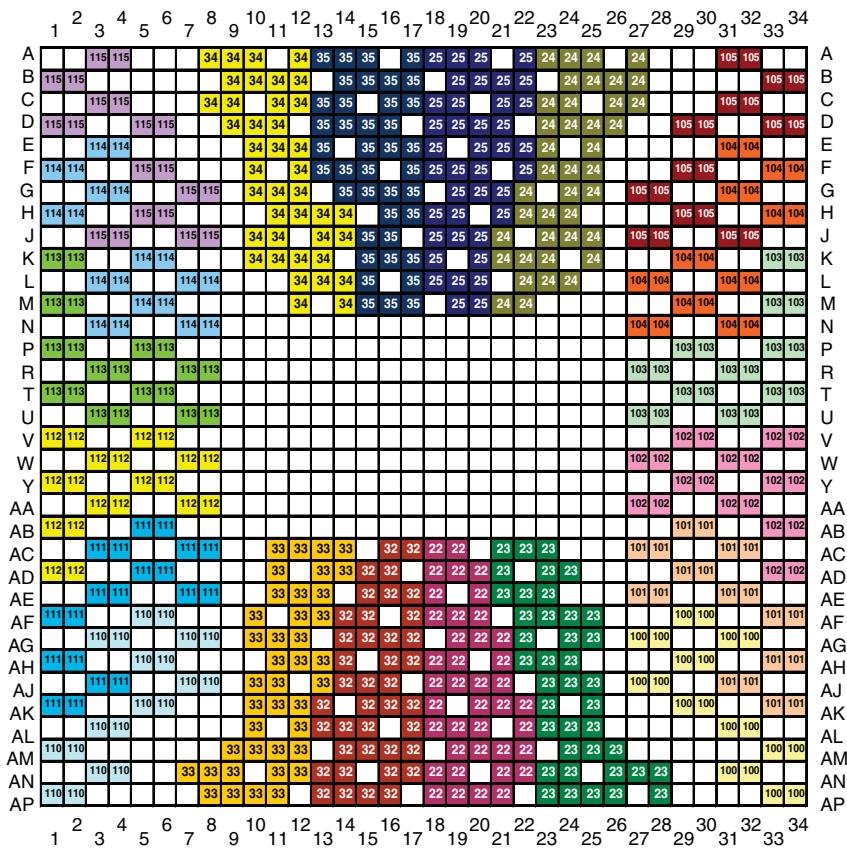
FF1154 Package—HX250T and HX380T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#			□ GND
Multi-Function Pins			□ RSVD
● SM	■ MGTAVCC	□ CCLK	□ VFS
⊗ VREF	■ MGTAVTT	□ CSI_B	□ VBATT
⊕ VRN	■ MGTAVTRCAL	□ DIN	■ VCCAUX
⊖ VRP	◆ MGTREFCLKP	□ TCK	■ VCCINT
○ P_GC	◆ MGTREFCLKN	□ DONE	□ VCO
● N_GC	■ MGTRREF	□ DOUT_BUSY	□ NC
○ CC	◆ MGTRXP	□ HSWAPEN	□ FLOAT
○ D0 - D31	◆ MGTRXN	□ INIT	
● A0 - A25	◆ MGTTXP	□ M2, M1, M0	
□ CSO_B	◆ MGTTXN	□ AVDD, AVSS, VP, VN, VREFP, VREFN	
		□ PROGRAM_B	
		□ RDWR	
		□ TDI	
		□ TDO	
		□ TMS	
		□ DXP	
		□ DXN	
		□ GND	
		□ RSVD	
		□ VFS	
		□ VBATT	
		■ VCCAUX	
		■ VCCINT	
		□ VCO	
		□ NC	
		□ FLOAT	

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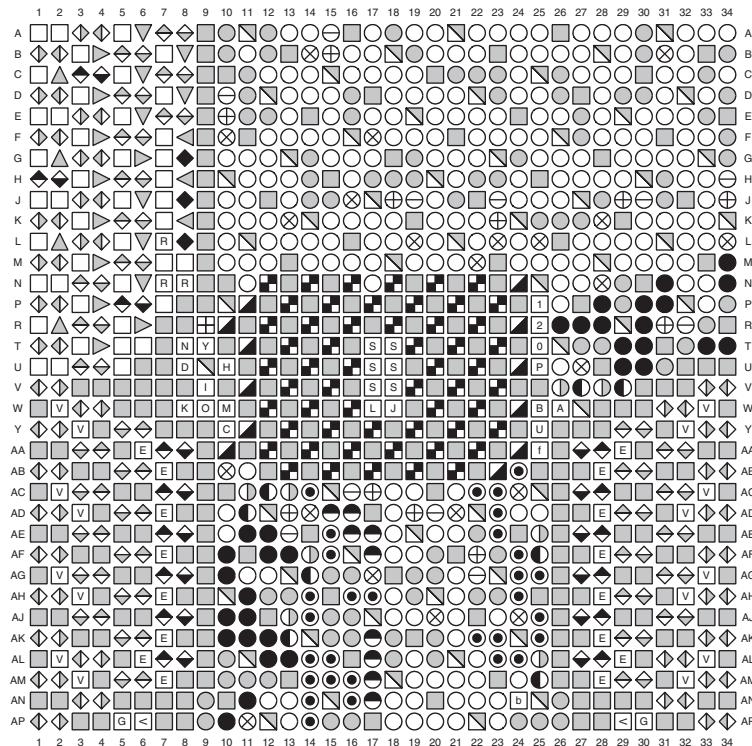
Figure 3-7: FF1154 Package—HX250T and HX380T Pinout Diagram



UG365_c3_08_092809

Figure 3-8: FF1154 Package—HX250T and HX380T I/O Bank Diagram

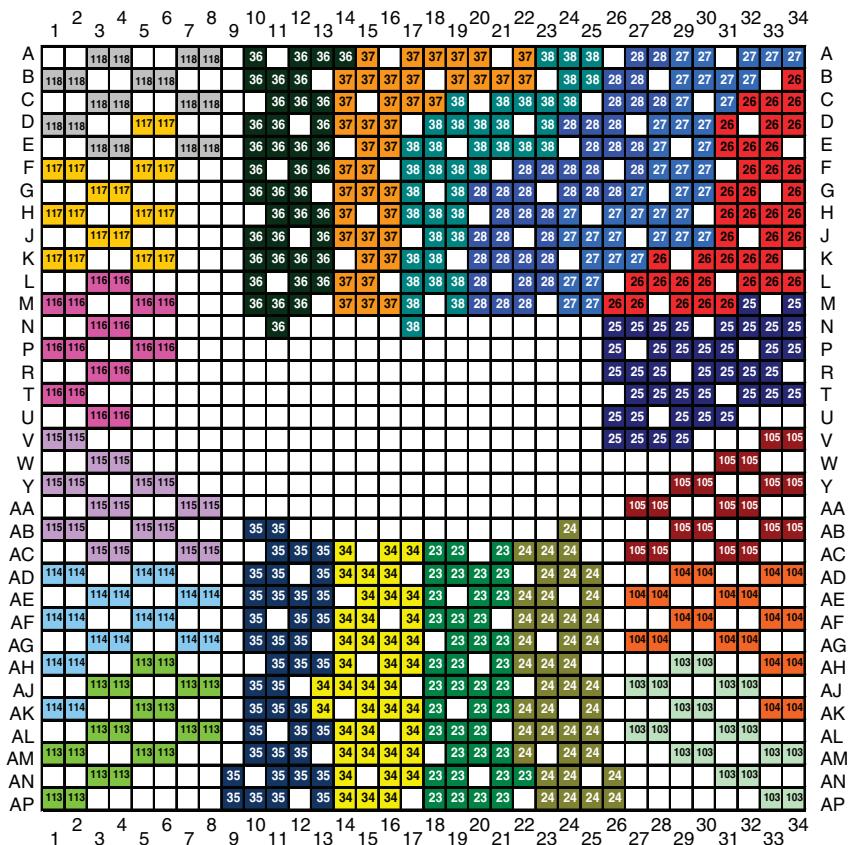
FF1155 Package—HX255T and HX380T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
○ IO_LXXY #			
Multi-Function Pins			
● SM	■ MGTAVCC	□ CCLK	■ GND
⊗ VREF	▼ MGTAVTT	■ CSI_B	■ RSVD
⊕ VRN	□ MGTAVTRCAL	□ DIN	□ VFS
⊖ VRP	◆ MGTREFCLKP	△ DONE	□ VBATT
① P_GC	◆ MGTREFCLKN	□ MGTHAGND	■ VCCAUX
● N_GC	■ MGTRREF	◆ MGTRBIAS	■ VCCINT
○ CC	◆ MGTRXP		■ VCCO
● D0 - D31	◆ MGTRXN		□ NC
● A0 - A25	◆ MGTTXP		■ FLOAT
■ CSO_B	◆ MGTTXN		
		□ HSWAPEN	
		□ INIT	
		□ M2, M1, M0	
		□ AVDD, AVSS, VP, VN, VREFP, VREFN	
		□ TDO	
		□ TMS	
		□ TDI	
		□ DOUT_BUSY	
		□ HSWAPEN	
		□ INIT	
		□ M2, M1, M0	
		□ AVDD, AVSS, VP, VN, VREFP, VREFN	
		□ TDO	
		□ TMS	
		□ TDI	
		□ DOUT_BUSY	
		□ HSWAPEN	
		□ INIT	
		□ M2, M1, M0	
		□ AVDD, AVSS, VP, VN, VREFP, VREFN	

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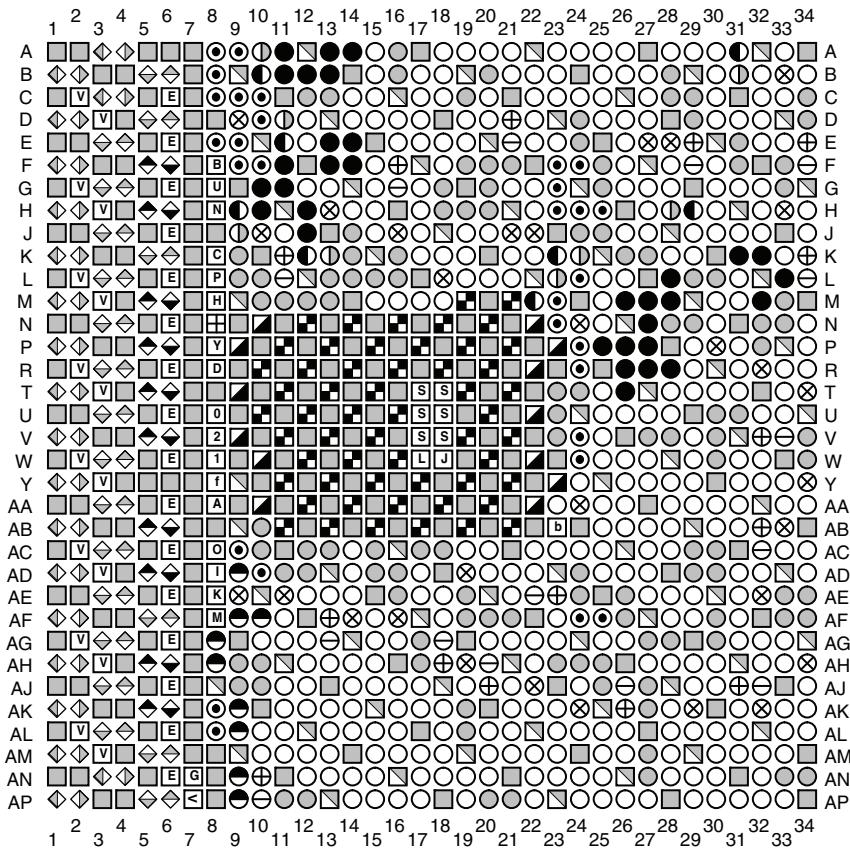
Figure 3-9: FF1155 Package—HX255T and HX380T Pinout Diagram



UG365_c3_10_092809

Figure 3-10: FF1155 Package—HX255T and HX380T I/O Bank Diagram

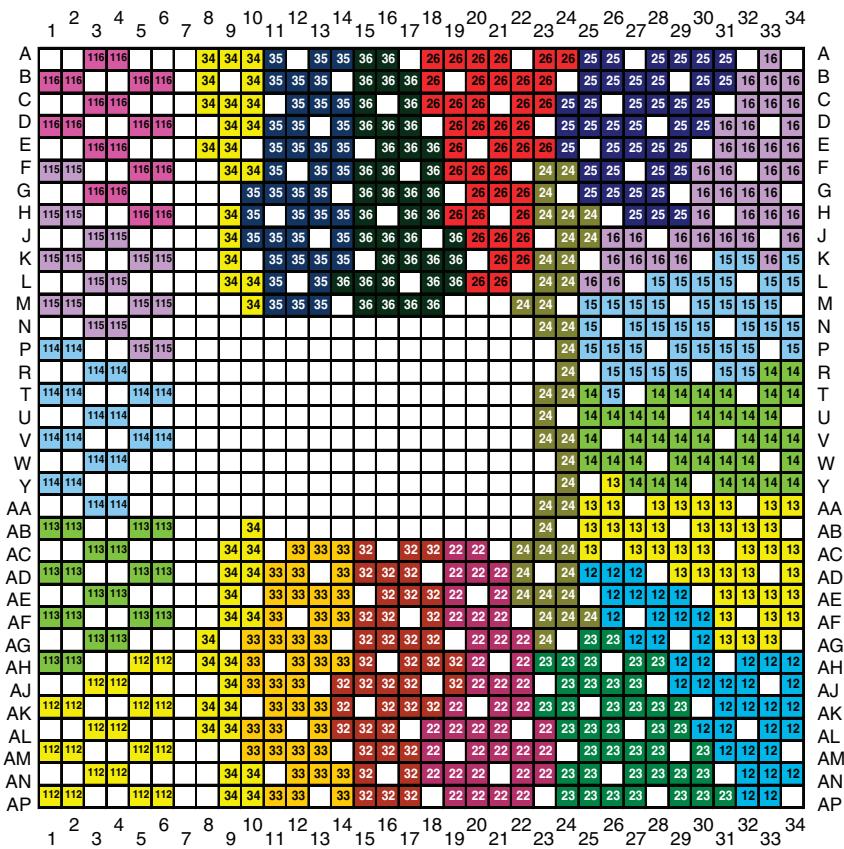
FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315, and SX475T



User I/O Pins	Multi-Function Pins	Transceiver Pins	Dedicated Pins	Other Pins
○	● SM ⊗ VREF ⊕ VRN ⊖ VRP ○ P_GC ● N_GC ○ CC ○ D0 - D31 ● A0 - A25 □ CSO_B	□ MGTAVCC ⊗ MGTAVTT ⊕ MGTAVTRCAL ⊖ MGTREFCLKP ○ MGTREFCLKN ● MGTRREF ○ MGTRXP ○ MGTRXN ● MGTTXN □ MGTTXP	□ C CCLK ⊗ B CSI_B ⊕ N DIN ⊖ D DONE ○ A DOUT_BUSY ● G MGTRREF ○ H HSWAPEN ○ Y INIT □ Z M2, M1, M0 ⊗ S AVDD, AVSS, VP, VN, VREFP, VREFN	□ PROGRAM_B ⊗ U RDWR ⊕ K TCK ⊖ L TDI ○ M TDO ● H TMS ○ J DXP □ L DXN □ GND ⊗ F VFS ⊕ E VBATT ⊖ F VCCAUX ○ D VCCINT ● C VCCO ○ H NC □ F FLOAT

UG365_c3_11_062709

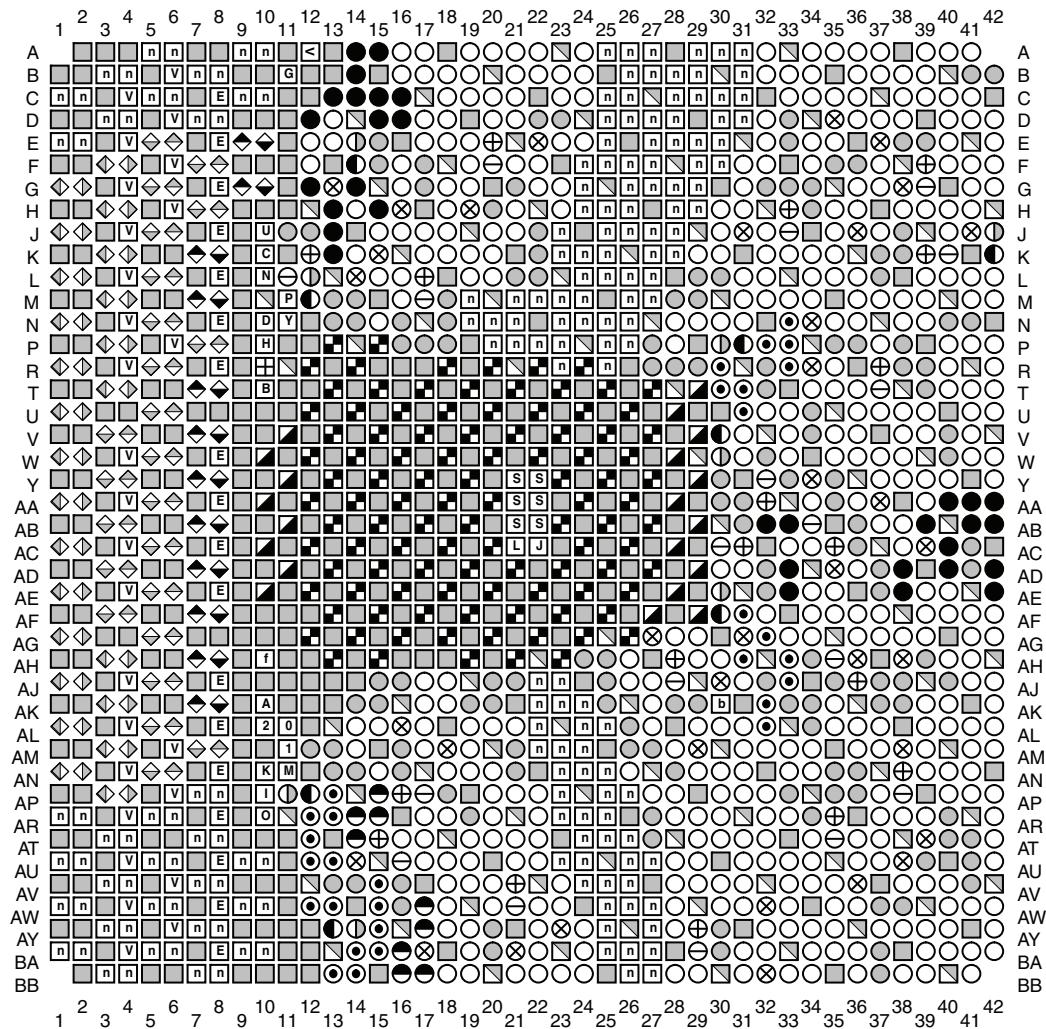
Figure 3-11: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T Pinout Diagram



UG365_c3_12_091509

Figure 3-12: FF1156/RF1156 Package—LX130T, LX195T, LX240T, LX365T, SX315T, and SX475T I/O Bank Diagram

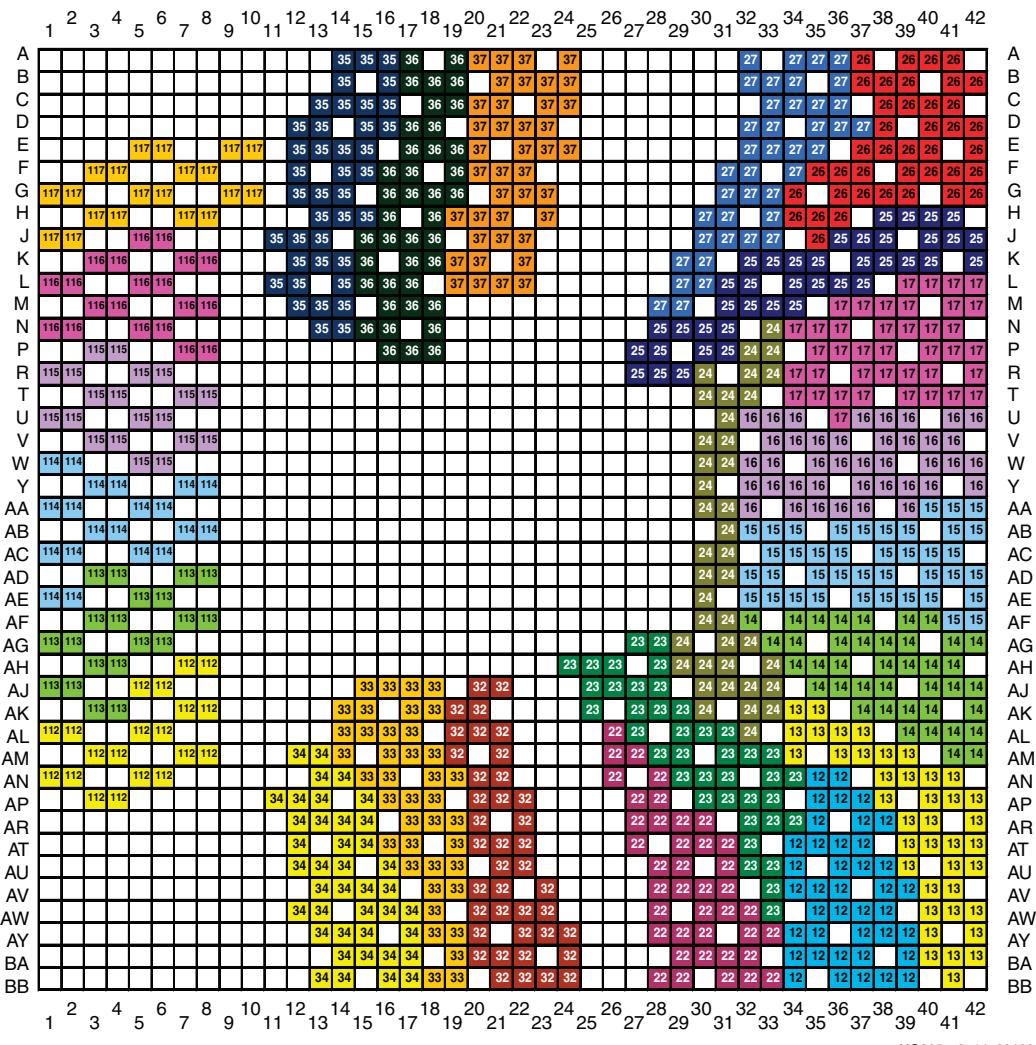
FF1759/RF1759 Package—LX240T, LX365T, and SX315T



User I/O Pins	Multi-Function Pins	Transceiver Pins	Dedicated Pins	Other Pins	
<input type="radio"/> IO_LXXY_# <input type="radio"/> SM <input type="radio"/> VREF <input type="radio"/> VRN <input type="radio"/> VRP <input type="radio"/> P_GC <input type="radio"/> N_GC <input type="radio"/> CC <input type="radio"/> D0 - D31 <input type="radio"/> A0 - A25 <input type="radio"/> CSO_B	<input type="radio"/> ● SM <input type="radio"/> ○ VREF <input type="radio"/> ⊕ VRN <input type="radio"/> ○ VRP <input type="radio"/> ○ P_GC <input type="radio"/> ● N_GC <input type="radio"/> ○ CC <input type="radio"/> ○ D0 - D31 <input type="radio"/> ● A0 - A25 <input type="radio"/> ■ CSO_B	<input type="radio"/> MGTAVCC <input type="radio"/> MGTAVTT <input type="radio"/> MGTAVTRCAL <input type="radio"/> MGTRCLKP <input type="radio"/> MGTRCLKN <input type="radio"/> MGTRREF <input type="radio"/> MGTRXP <input type="radio"/> MGTRXN <input type="radio"/> MGTTXN <input type="radio"/> MGTTXP	<input type="radio"/> C CCLK <input type="radio"/> B CSI_B <input type="radio"/> N DIN <input type="radio"/> D DONE <input type="radio"/> G DOUT_BUSY <input type="radio"/> H HSWAPEN <input type="radio"/> Y INIT <input type="radio"/> 2 1 0 M2, M1, M0 <input type="radio"/> S AVDD, AVSS, VP, VN, VREFP, VREFN	<input type="radio"/> PROGRAM_B <input type="radio"/> RDWR <input type="radio"/> TCK <input type="radio"/> TDI <input type="radio"/> TDO <input type="radio"/> TMS <input type="radio"/> J DXP <input type="radio"/> DXN	<input type="radio"/> GND <input type="radio"/> VFS <input type="radio"/> VBATT <input type="radio"/> VCCAUX <input type="radio"/> VCCINT <input type="radio"/> VCCO <input type="radio"/> NC <input type="radio"/> FLOAT

UG365_c3_13_082709

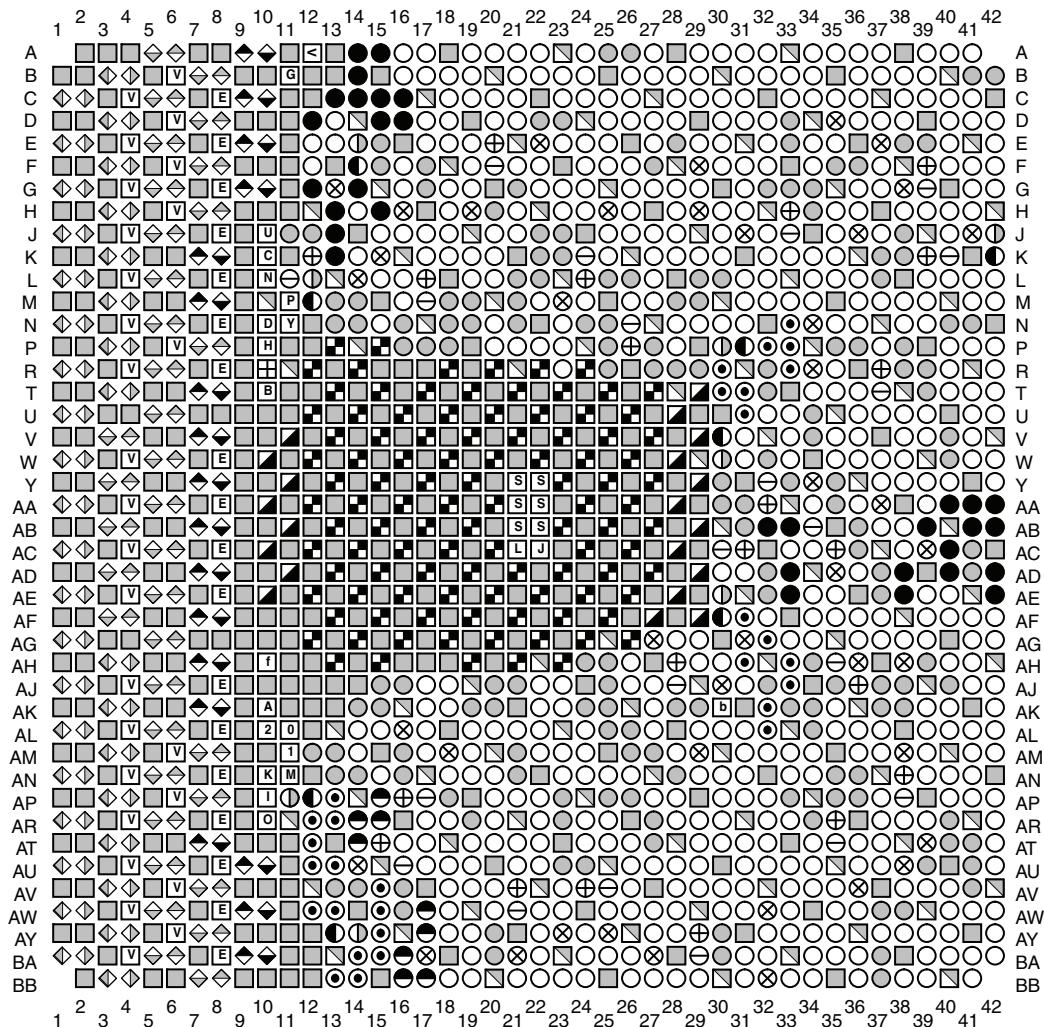
Figure 3-13: FF1759/RF1759 Package—LX240T, LX365T, and SX315T Pinout Diagram



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Figure 3-14: FF1759/RF1759 Package—LX240T, LX365T, and SX315T I/O Bank Diagram

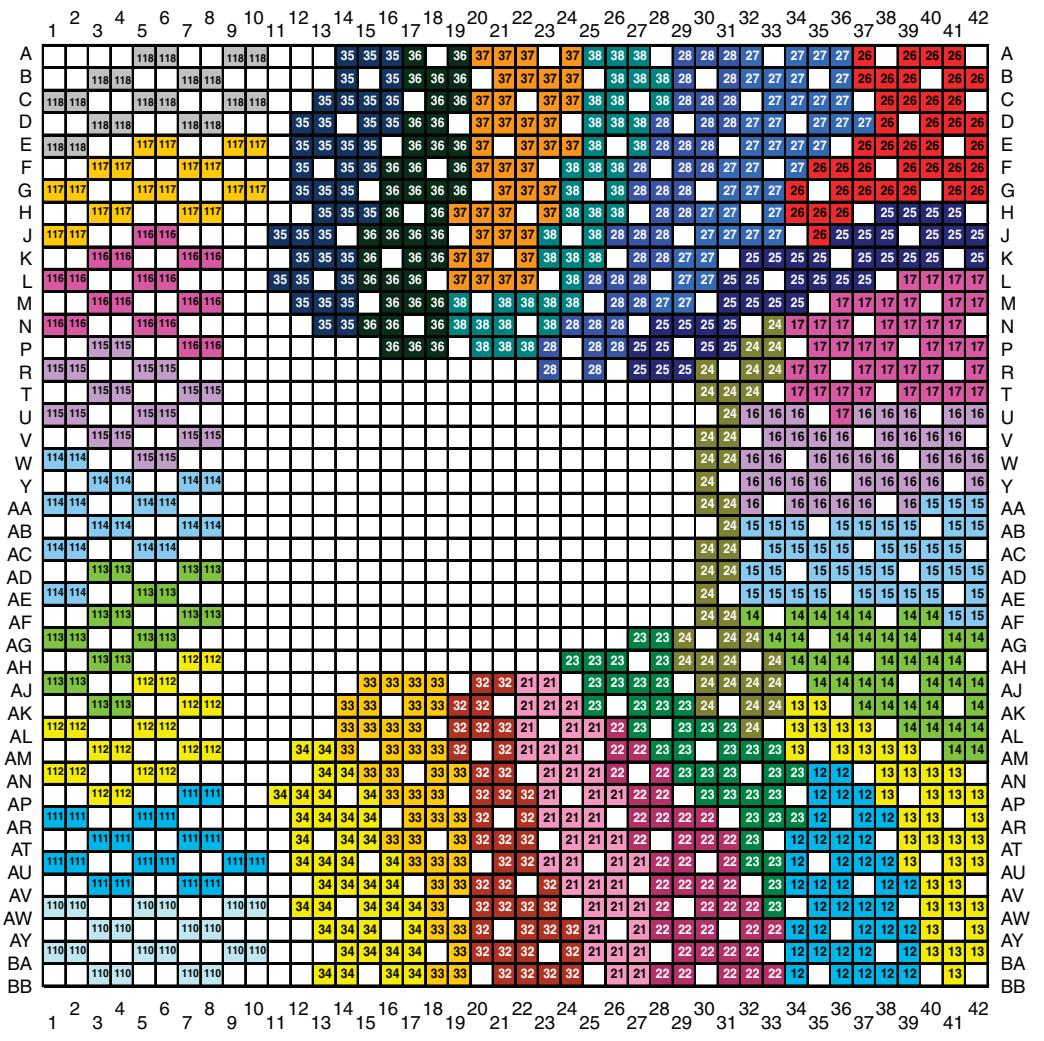
FF1759/RF1759 Package—LX550T and SX475T



User I/O Pins	Multi-Function Pins	Transceiver Pins	Dedicated Pins		Other Pins
<input type="radio"/> IO_LXXY_#	<input checked="" type="radio"/> SM <input checked="" type="radio"/> VREF <input checked="" type="radio"/> VRN <input checked="" type="radio"/> VRP <input checked="" type="radio"/> P_GC <input checked="" type="radio"/> N_GC <input checked="" type="radio"/> CC <input checked="" type="radio"/> D0 - D31 <input checked="" type="radio"/> A0 - A25 <input checked="" type="radio"/> CSO_B	<input checked="" type="radio"/> MGTAVCC <input checked="" type="radio"/> MGTAVTT <input checked="" type="radio"/> MGTAVTRCAL <input checked="" type="radio"/> MGTRREFCLKP <input checked="" type="radio"/> MGTRREFCLKN <input checked="" type="radio"/> MGTRREF <input checked="" type="radio"/> MGTRXP <input checked="" type="radio"/> MGTRXN <input checked="" type="radio"/> MGTTXN <input checked="" type="radio"/> MGTTXP	<input checked="" type="radio"/> CCLK <input checked="" type="radio"/> CSI_B <input checked="" type="radio"/> DIN <input checked="" type="radio"/> DONE <input checked="" type="radio"/> DOUT_BUSY <input checked="" type="radio"/> HSWAPEN <input checked="" type="radio"/> INIT <input checked="" type="radio"/> M2, M1, M0	<input checked="" type="radio"/> PROGRAM_B <input checked="" type="radio"/> RDWR <input checked="" type="radio"/> TCK <input checked="" type="radio"/> TDI <input checked="" type="radio"/> TDO <input checked="" type="radio"/> TMS <input checked="" type="radio"/> DXP <input checked="" type="radio"/> DXN	<input checked="" type="radio"/> GND <input checked="" type="radio"/> VFS <input checked="" type="radio"/> VBATT <input checked="" type="radio"/> VCCAUX <input checked="" type="radio"/> VCCINT <input checked="" type="radio"/> VCO <input checked="" type="radio"/> NC <input checked="" type="radio"/> FLOAT

UG365_c3_15_082709

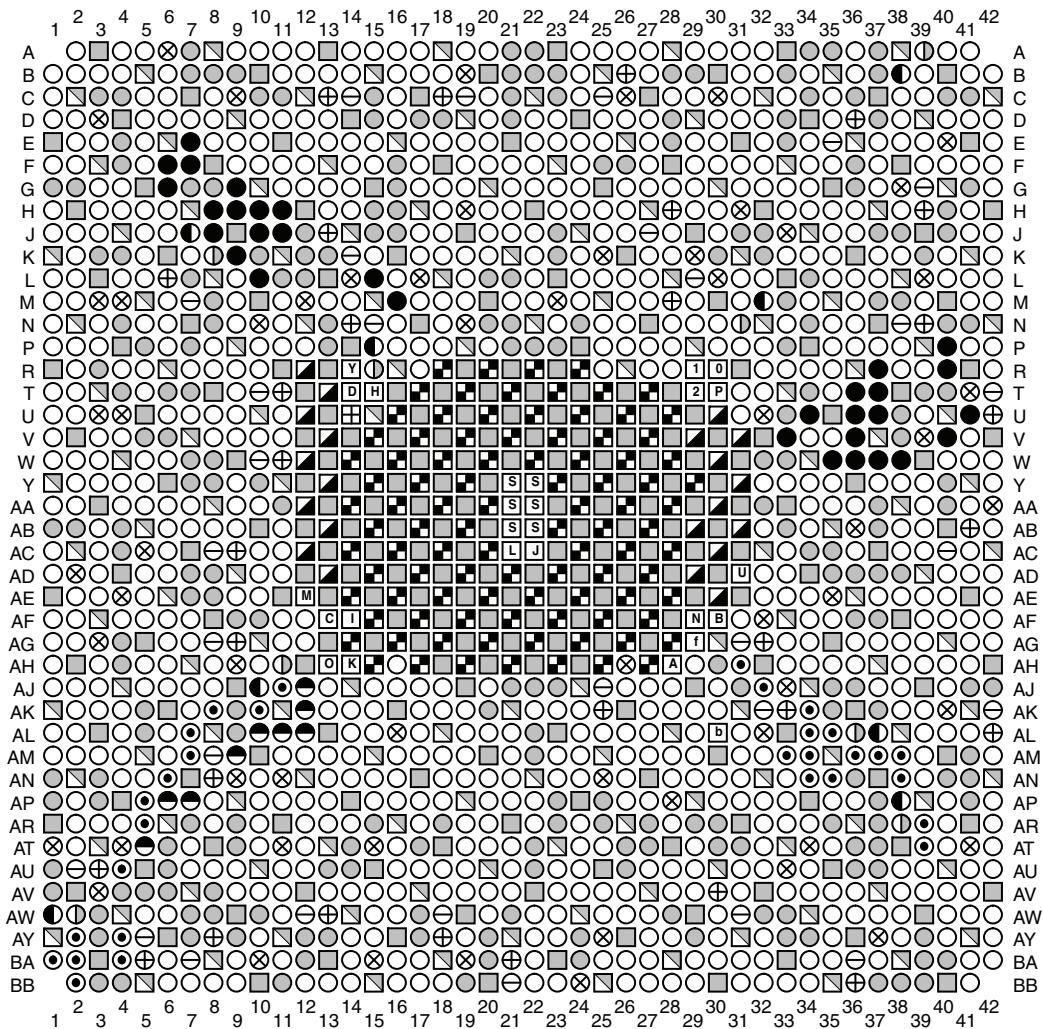
Figure 3-15: FF1759/RF1759 Package—LX550T and SX475T Pinout Diagram



UG365_c3_16_091609

Figure 3-16: FF1759/RF1759 Package—LX550T and SX475T I/O Bank Diagram

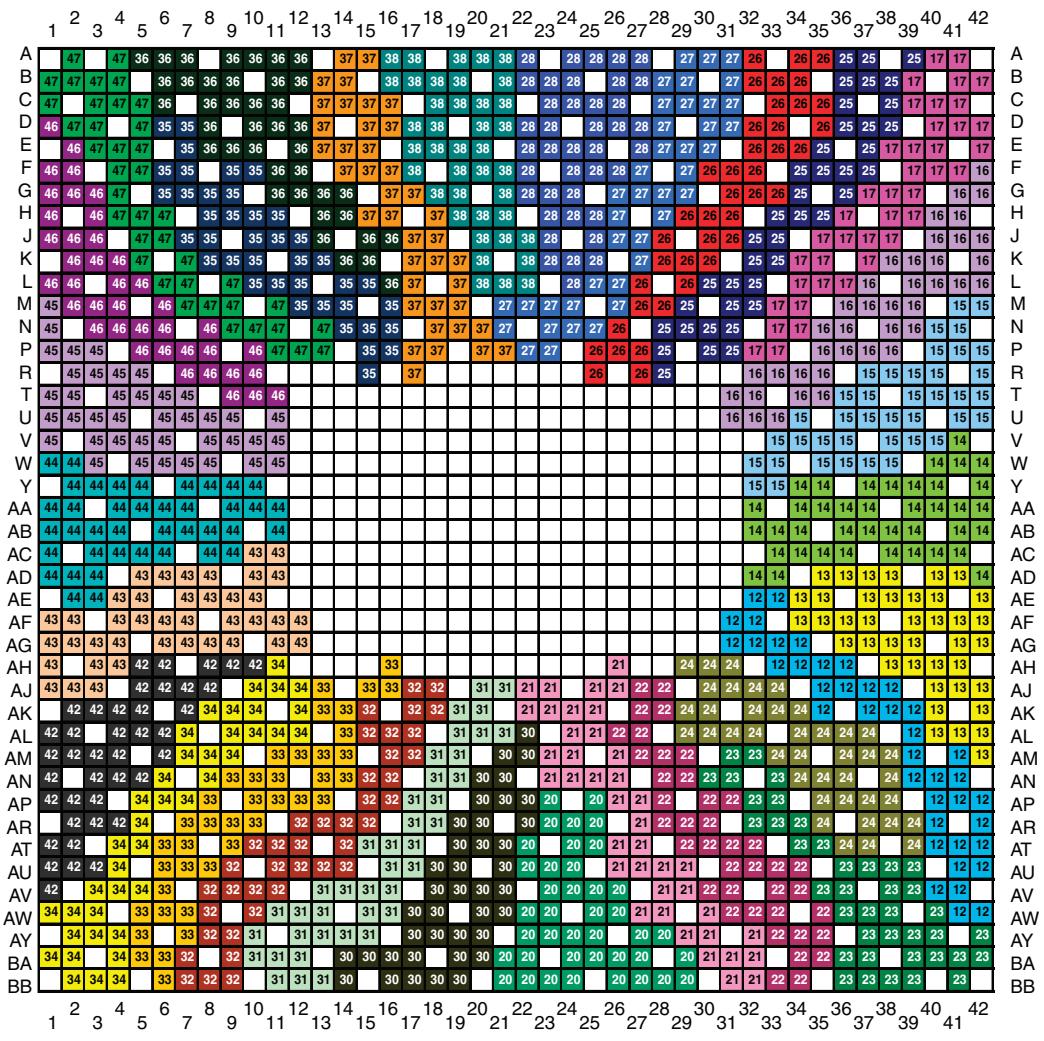
FF1760 Package—LX550T



User I/O Pins	Multi-Function Pins	Transceiver Pins	Dedicated Pins	Other Pins
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UG365_c3_17_082709

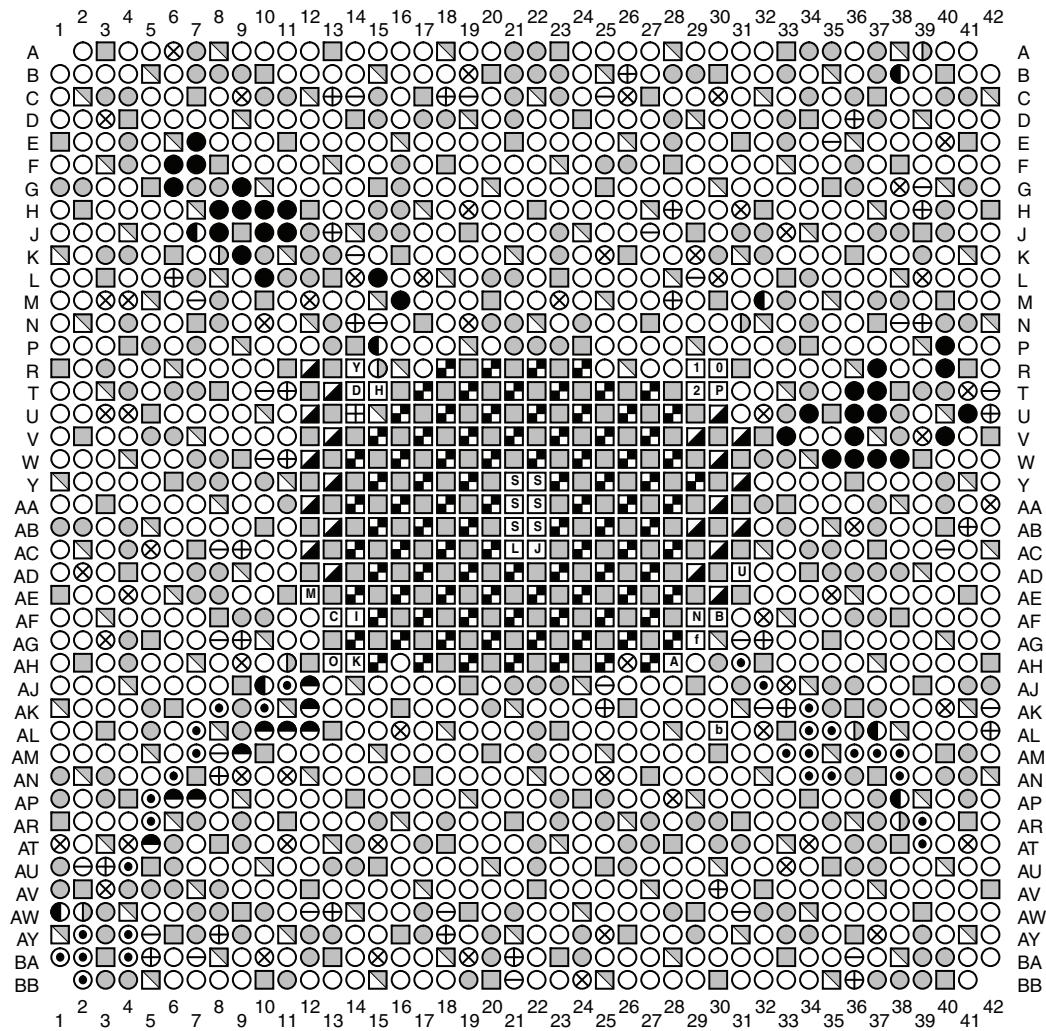
Figure 3-17: FF1760 Package—LX550T Pinout Diagram



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Figure 3-18: FF1760 Package—LX550T I/O Bank Diagram

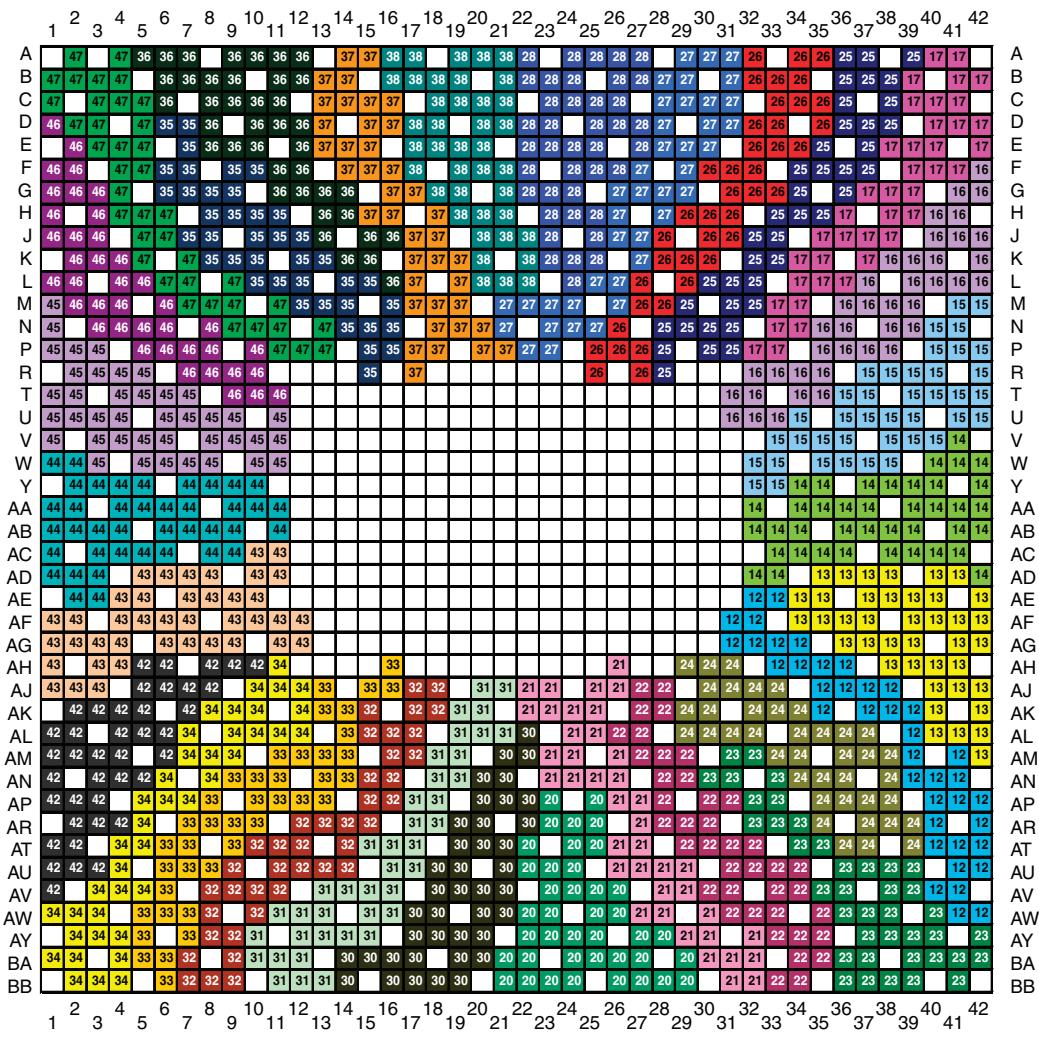
FF1760 Package—LX760



User I/O Pins	Multi-Function Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#	<ul style="list-style-type: none"> ● SM ⊗ VREF ⊕ VRN ⊖ VRP ○ P_GC ● N_GC ○ CC ○ D0 - D31 ● A0 - A25 □ CSO_B 	<ul style="list-style-type: none"> □ CCLK □ CSI_B □ DIN □ DONE □ DOUT_BUSY □ HSWAPEN □ INIT □ M2, M1, M0 □ AVDD, AVSS, VP, VN, VREFP, VREFN □ PROGRAM_B □ RDWR □ TCK □ TDI □ TDO □ TMS □ DXP □ DXN 	<ul style="list-style-type: none"> □ GND □ VFS □ VBATT □ VCCAUX □ VCCINT □ VCCO □ NC □ FLOAT

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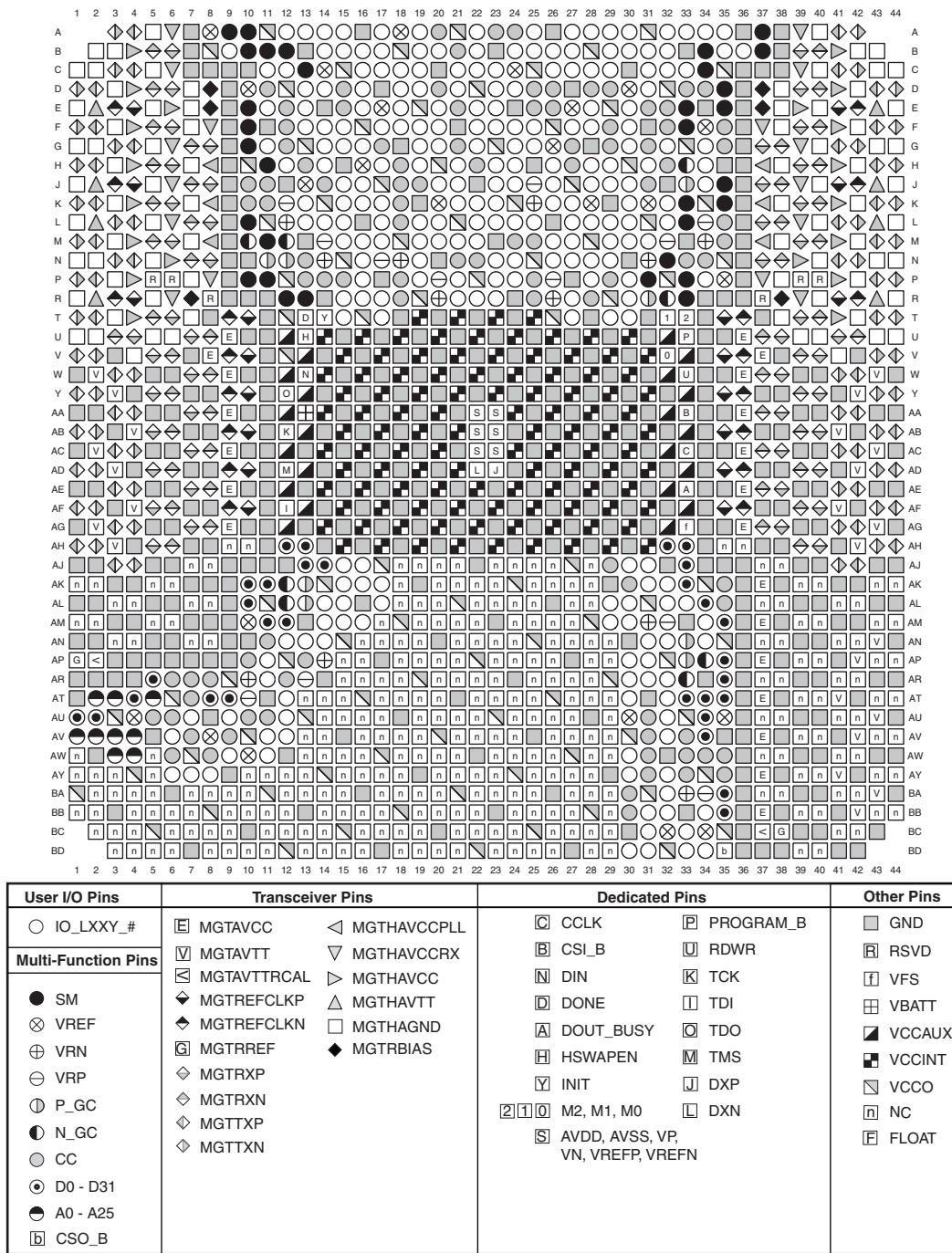
Figure 3-19: FF1760 Package—LX760 Pinout Diagram



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Figure 3-20: FF1760 Package—LX760 I/O Bank Diagram

FF1923 Package—HX255T



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Figure 3-21: FF1923 Package—HX255T Pinout Diagram

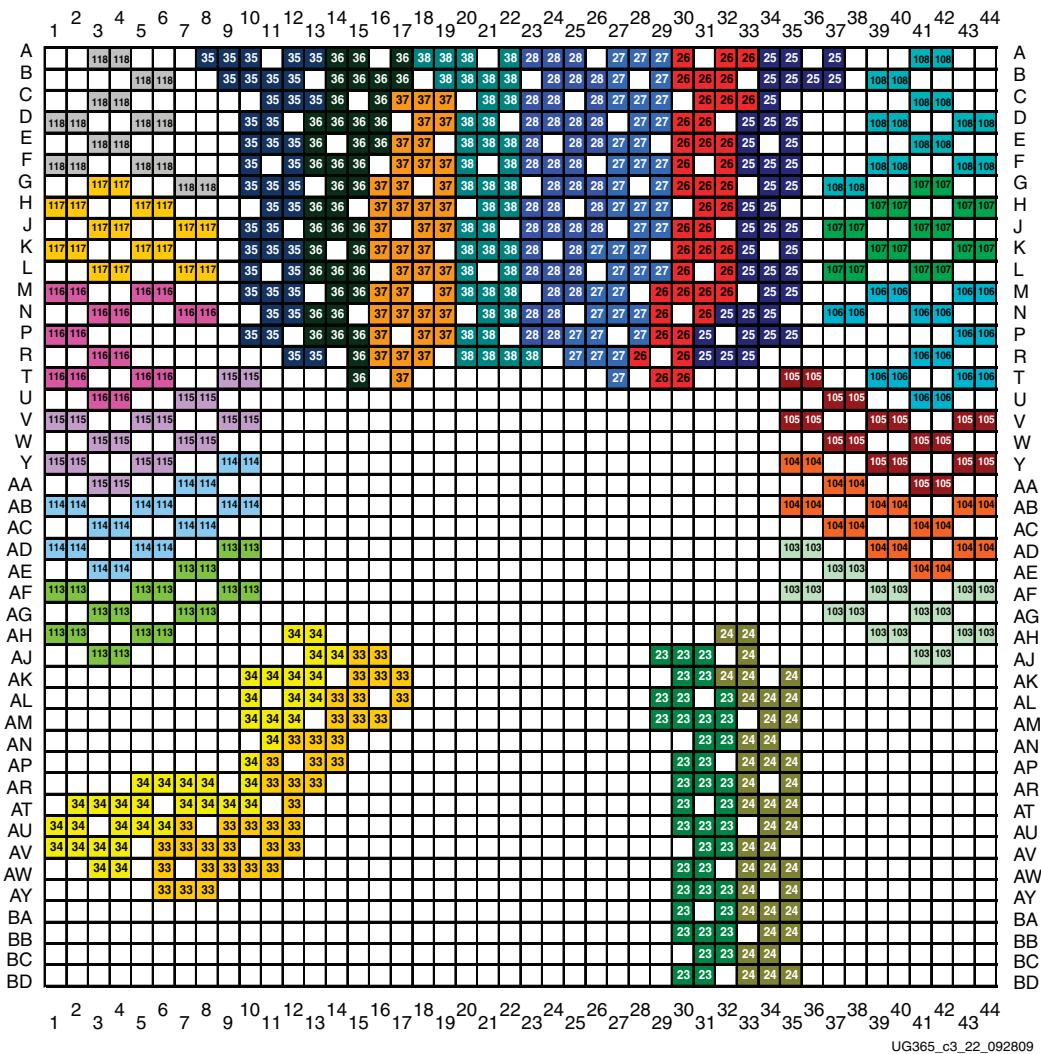
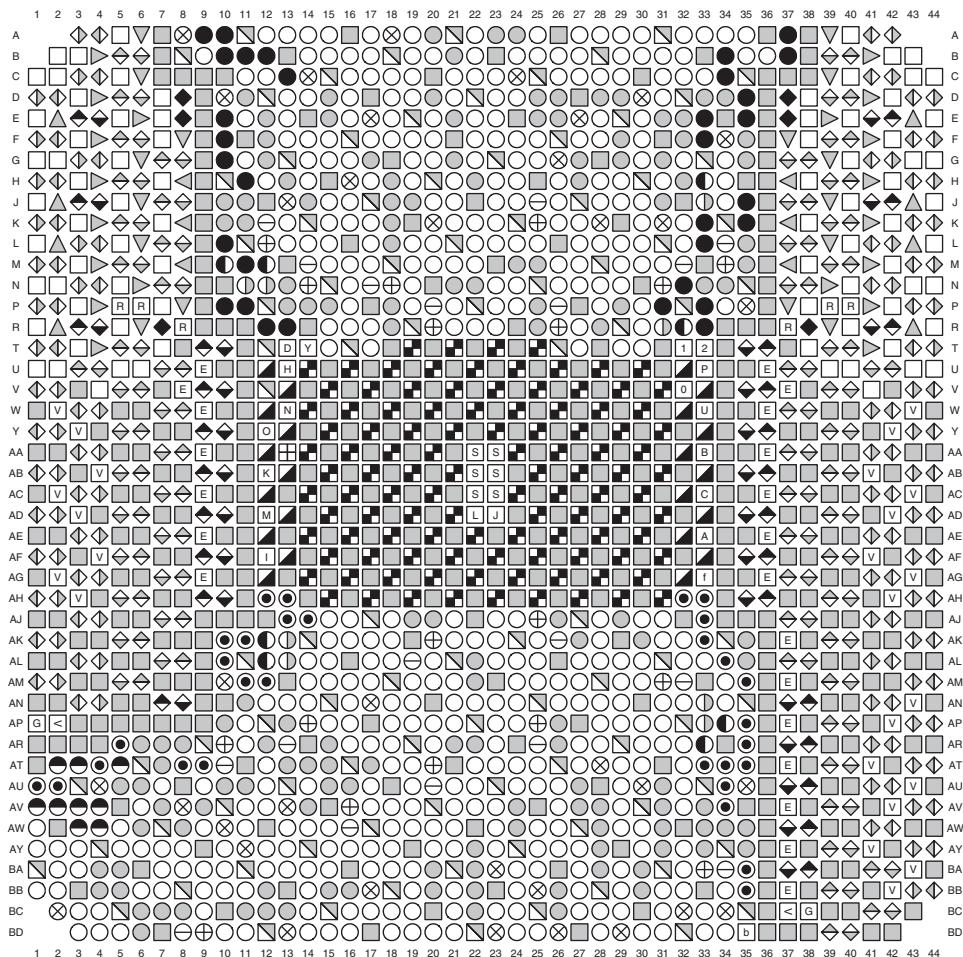


Figure 3-22: FF1923 Package—HX255T I/O Bank Diagram

FF1923 Package—HX380T and HX565T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#	E MGTAVCC □ MGTHAVCCPLL V MGTAVTT ▽ MGTHAVCCRX □ MGTAVTRCAL ▷ MGTHAVCC ◆ MGTREFCLKP △ MGTHAVTT ◆ MGTREFCLKN □ MGTHAGND ■ MGTRREF ◆ MGTRBIAS ◆ MGTRXP ◆ MGTRXN ◆ MGTTXP ◆ MGTTXN	C CCLK □ PROGRAM_B B CSI_B □ RDWR N DIN □ TCK D DONE □ TDI A DOUT_BUSY □ TDO H HSWAPEN □ TMS Y INIT □ DXP □ M2, M1, M0 □ DXN S AVDD, AVSS, VP, VN, VREFP, VREFN	□ GND □ RSVD □ VFS □ VBATT ■ VCCAUX □ VCCINT □ VCCO □ NC □ FLOAT
Multi-Function Pins			
● SM ⊗ VREF ⊕ VRN ⊖ VRP ○ P_GC ● N_GC ○ CC ○ D0 - D31 ● A0 - A25 □ CSO_B			

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Figure 3-23: FF1923 Package—HX380T and HX565T Pinout Diagram

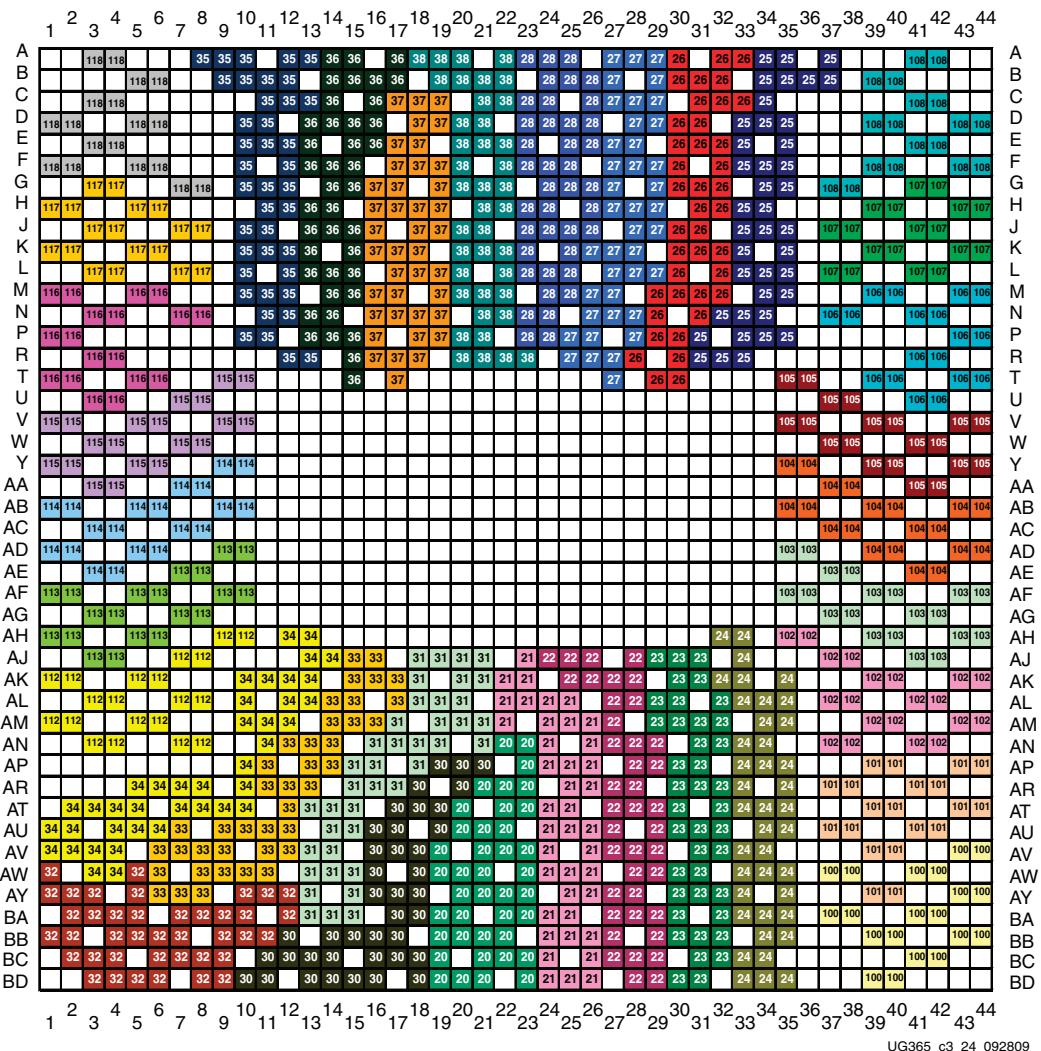
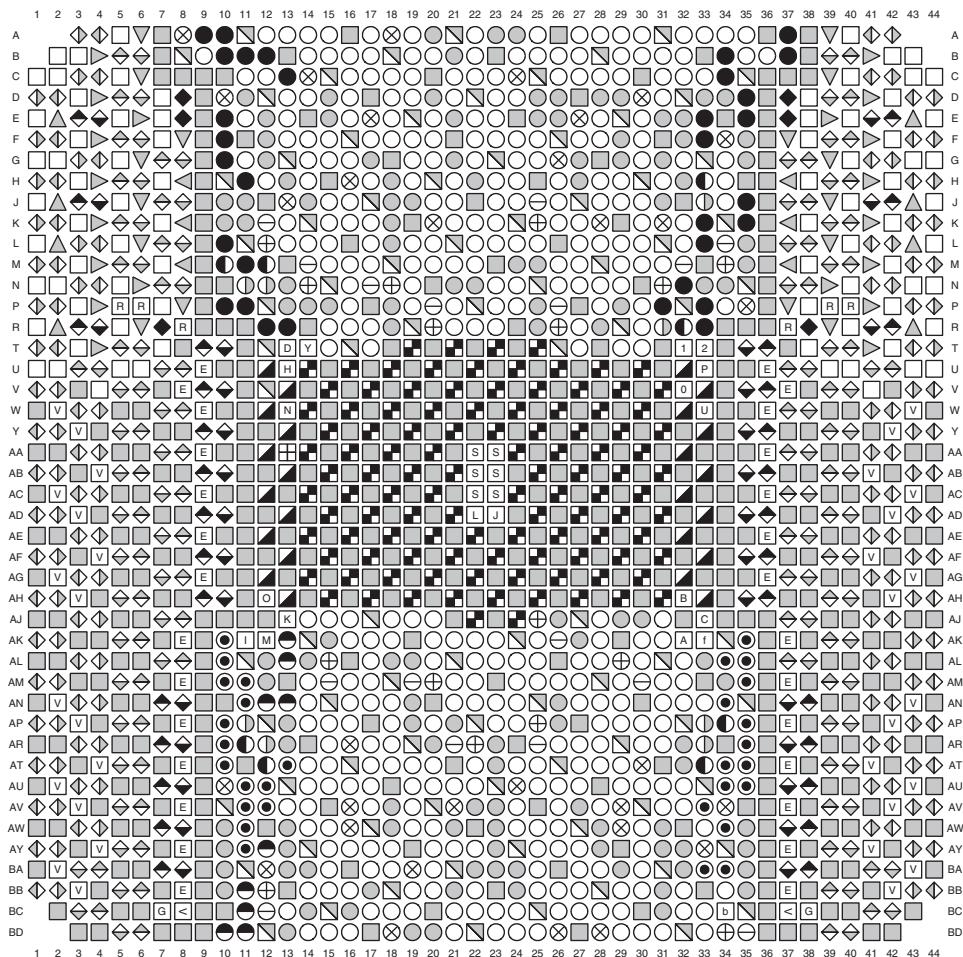


Figure 3-24: FF1923 Package—HX380T and HX565T I/O Bank Diagram

FF1924 Package—HX380T and HX565T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#	E MGTAVCC □ MGTHAVCCPLL V MGTAVTT ▽ MGTHAVCCRX L MGTVTTTRCAL ▷ MGTHAVCC ◆ MGTREFCLKP △ MGTHAVTT ◆ MGTREFCLKN □ MGTHAGND G MGTREFREF ◆ MGTRBIAS ◆ MGTRXP ◆ MGTRXN ◆ MGTTXP ◆ MGTTXN	C CCLK □ PROGRAM_B B CSI_B □ RDWR N DIN □ TCK D DONE □ TDI A DOUT_BUSY □ TDO H HSWAPEN □ TMS Y INIT □ DXP 2 1 0 M2, M1, M0 □ DXN S AVDD, AVSS, VP, VN, VREFP, VREFN	□ GND □ RSVD □ VFS □ VBATT □ VCCAUX □ VCCINT □ VCCO □ NC □ FLOAT
Multi-Function Pins			
● SM ⊗ VREF ⊕ VRN ⊖ VRP ① P_GC ● N_GC ◎ CC ◎ D0 - D31 ● A0 - A25 □ CSO_B			

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Figure 3-25: FF1924 Package—HX380T and HX565T Pinout Diagram

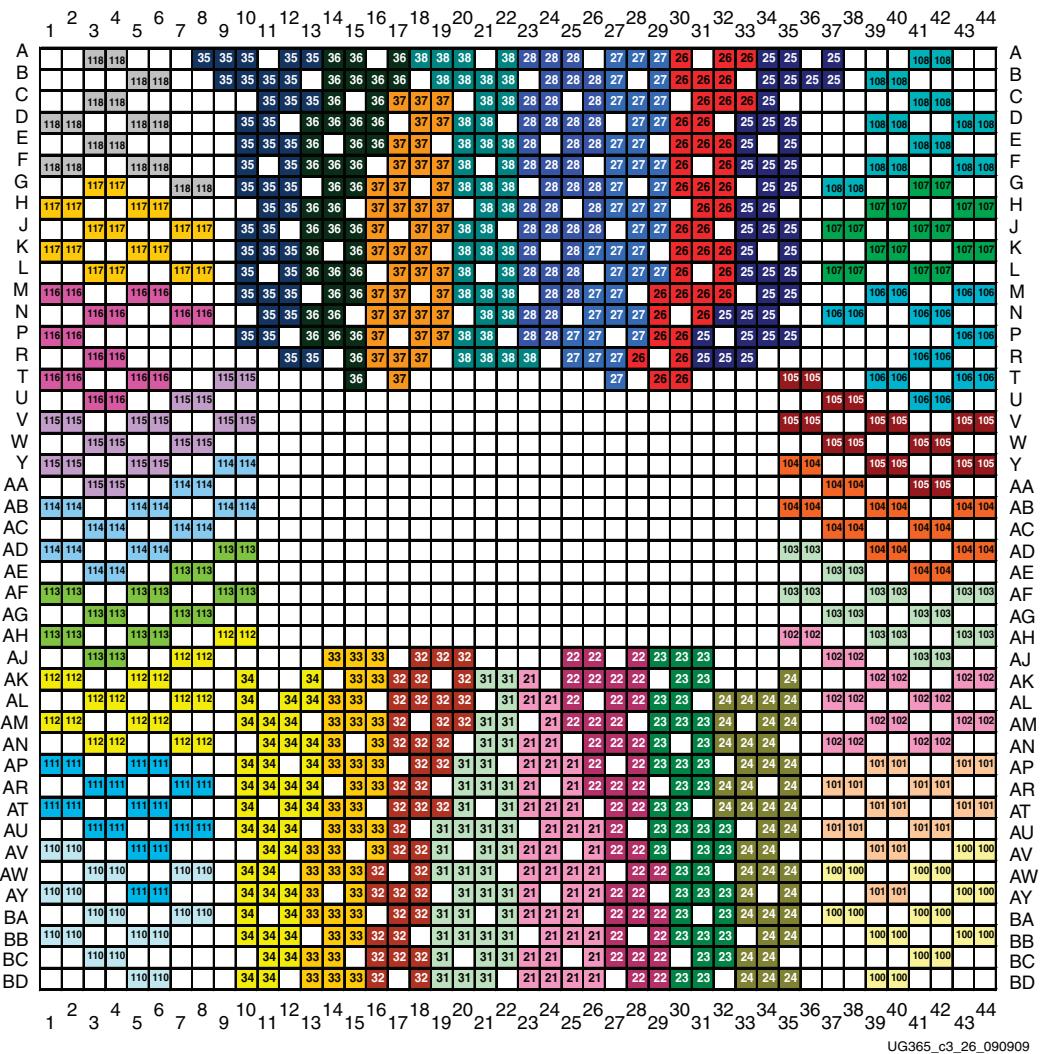


Figure 3-26: FF1924 Package—HX380T and HX565T I/O Bank Diagram

Mechanical Drawings

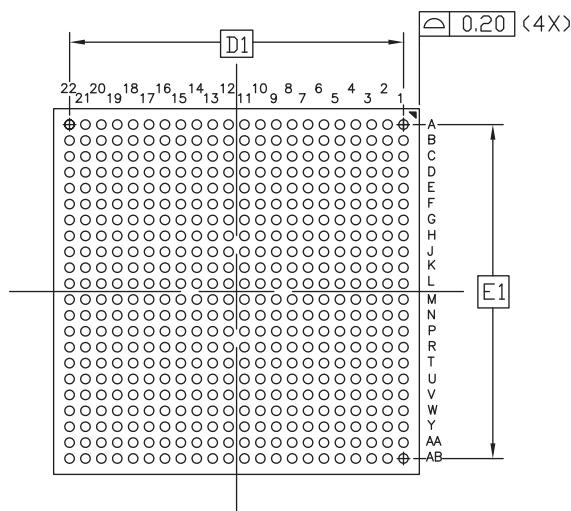
Summary

This chapter provides mechanical drawings of the following Virtex-6 FPGA packages:

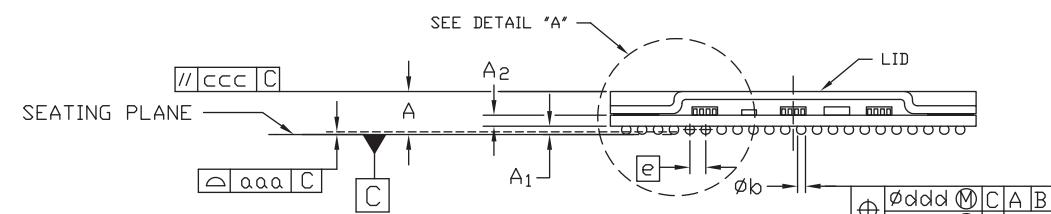
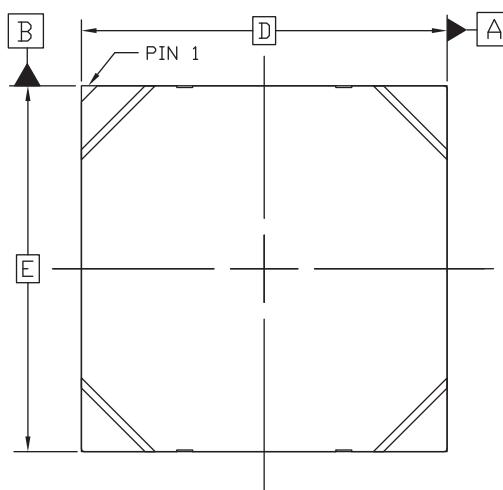
- FF484 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch), page 436
- FF784 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch), page 437
- RF784 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch), page 438
- FF1154 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch), page 439
- FF1155 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch), page 440
- FF1156 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch), page 441
- RF1156 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch), page 442
- FF1759 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch), page 443
- RF1759 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch), page 444
- FF1760 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch), page 445
- FF1923 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch), page 446
- FF1924 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch), page 447

FF484 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)

BOTTOM VIEW

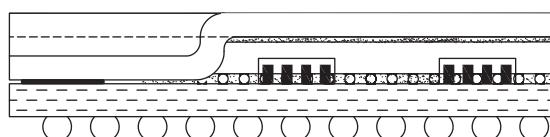


TOP VIEW



S Y M B O L	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.35	\cancel{x}	2.86	
A ₁	0.40	0.50	0.60	
A ₂	0.65	\cancel{x}	0.90	
D/E	23.00	BASIC		
D/E	21.00	REF		
e	1.00	BASIC		
Øb	0.50	0.60	0.70	
aaa	\cancel{x}	\cancel{x}	0.20	
ccc	\cancel{x}	\cancel{x}	0.25	
ddd	\cancel{x}	\cancel{x}	0.25	
eee	\cancel{x}	\cancel{x}	0.10	
M	22			2

FF484 - Sn/Pb SOLDER BALLS
FFG484 - Sn/Ag/Cu SOLDER BALLS



DETAIL "A"
(NOT TO SCALE)

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994.
 2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
 3. CONFORMS TO JEDEC MS-034-AAJ-1.

ug475 s4 01 083110

Figure 4-1: FF484 Flip-Chip Fine-Pitch BGA Package Specifications

FF784 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)

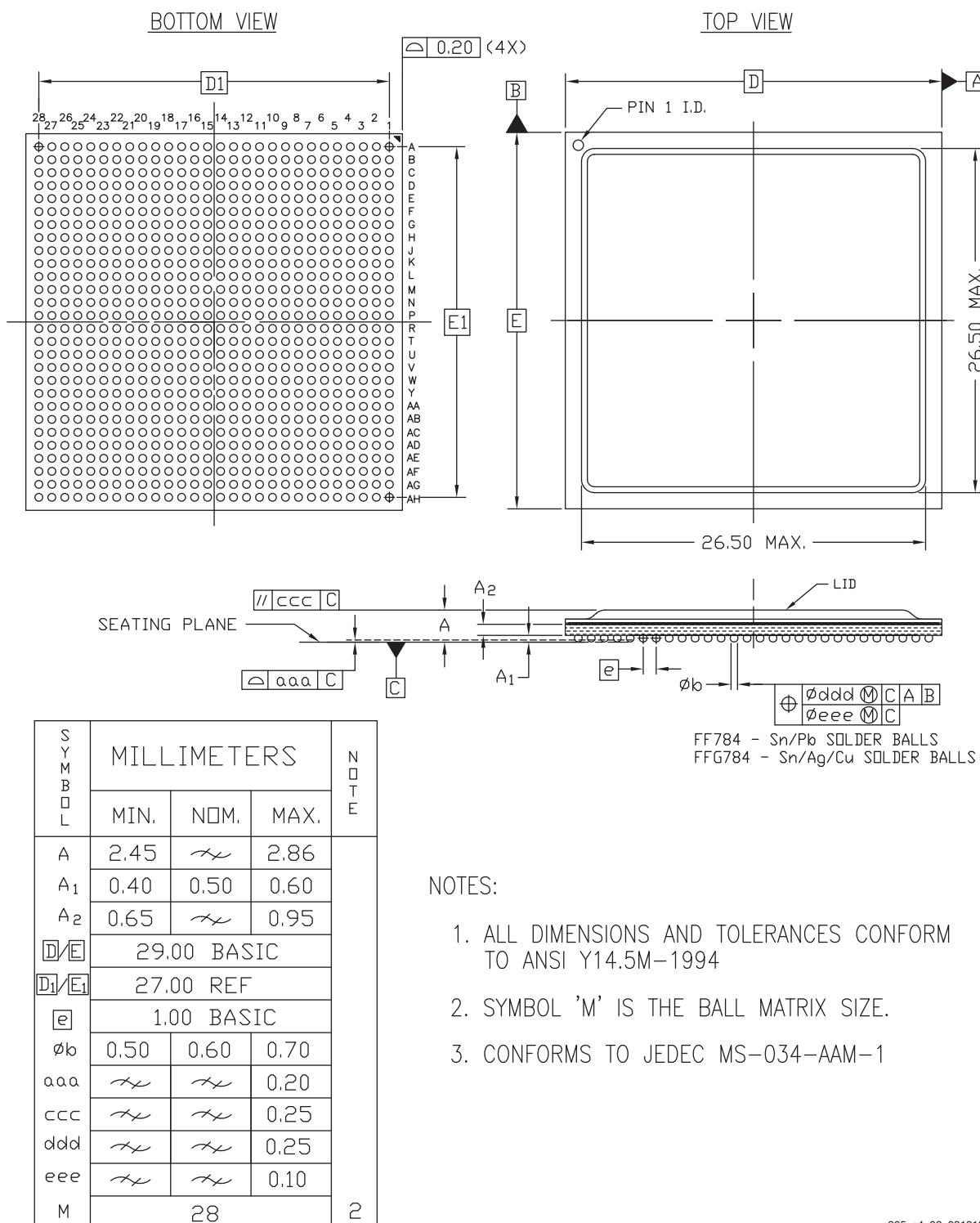


Figure 4-2: FF784 Flip-Chip Fine-Pitch BGA Package Specifications

RF784 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)

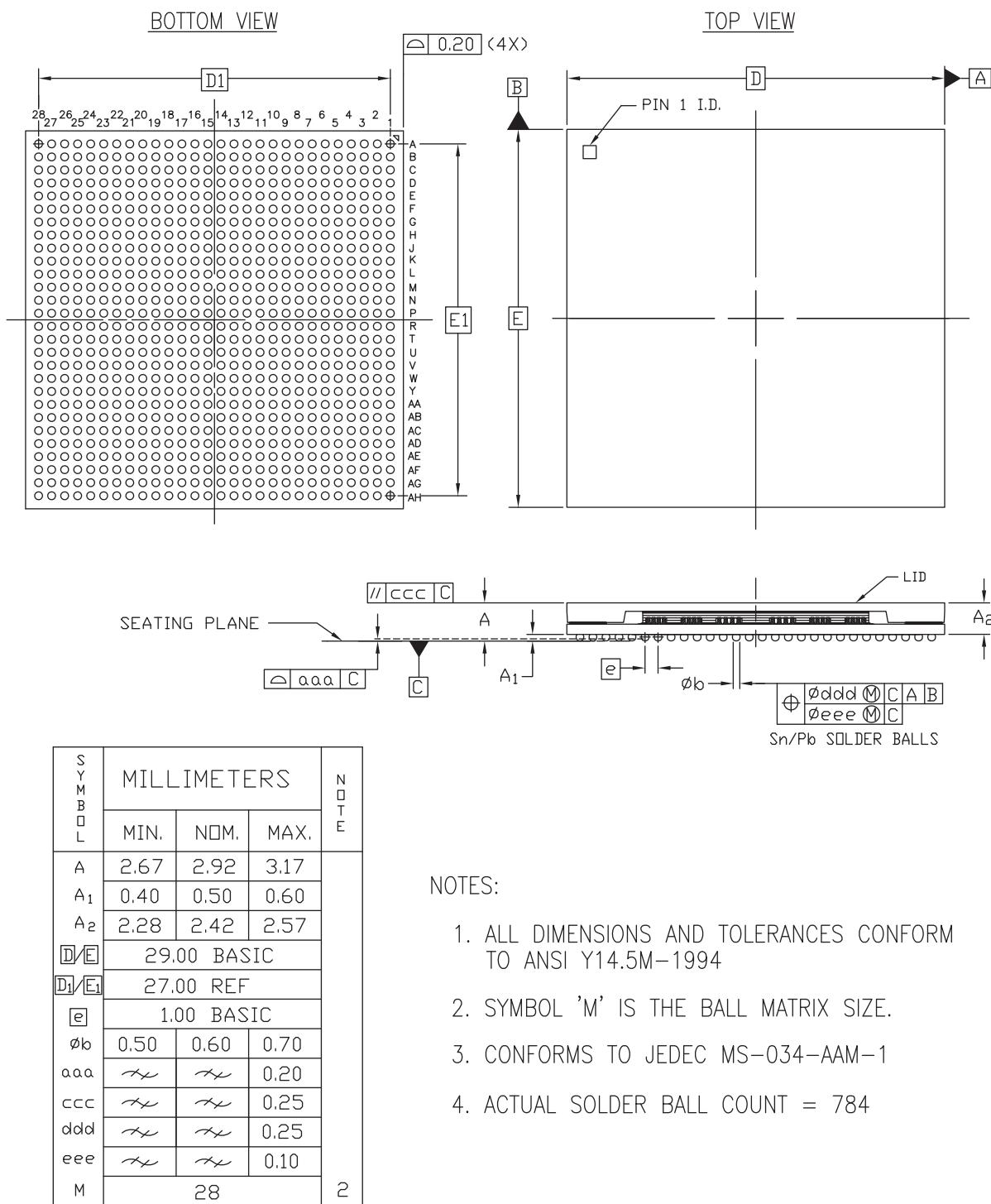
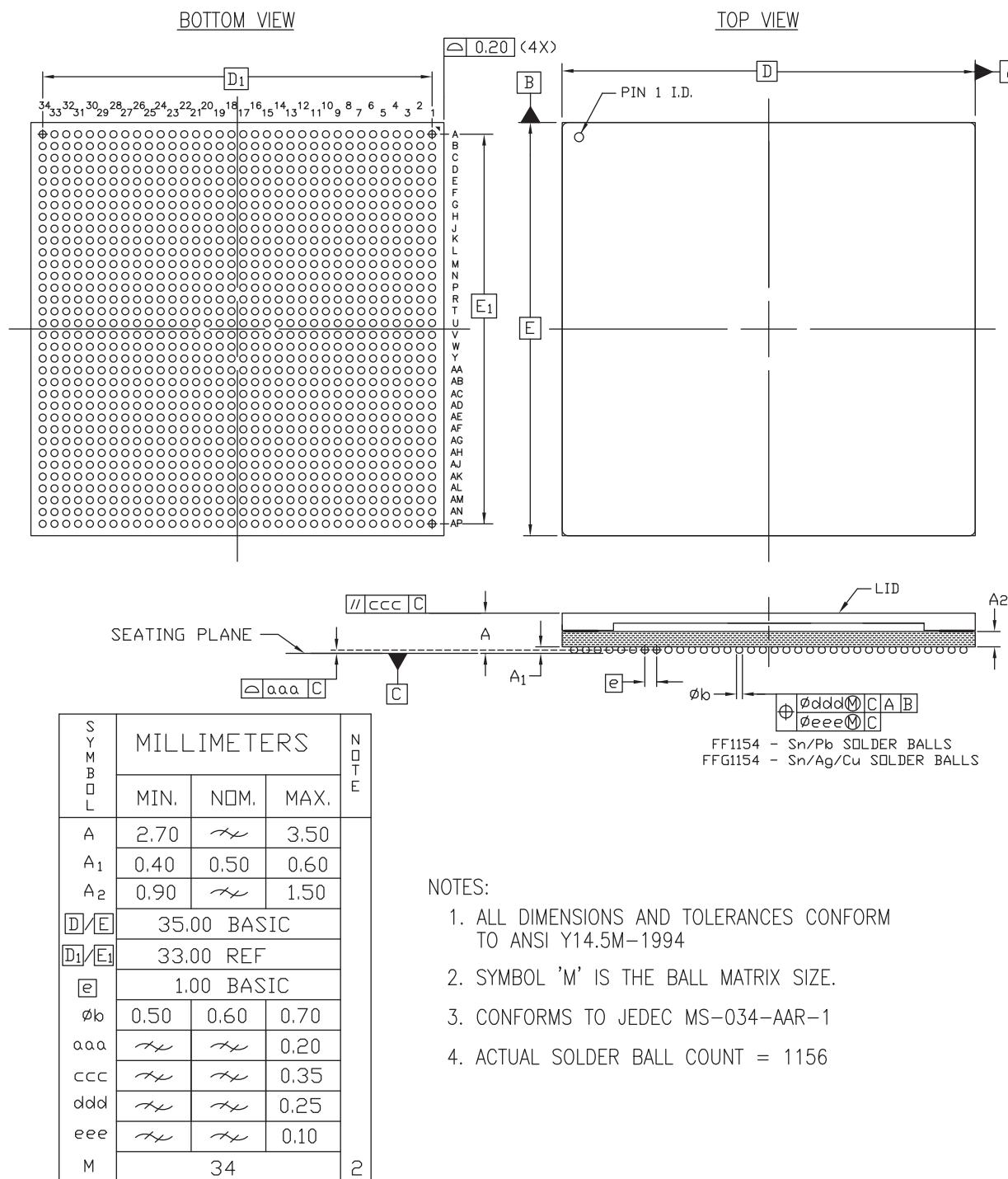


Figure 4-3: RF784 Flip-Chip Fine-Pitch BGA Package Specifications

ug365_c4_13_11111

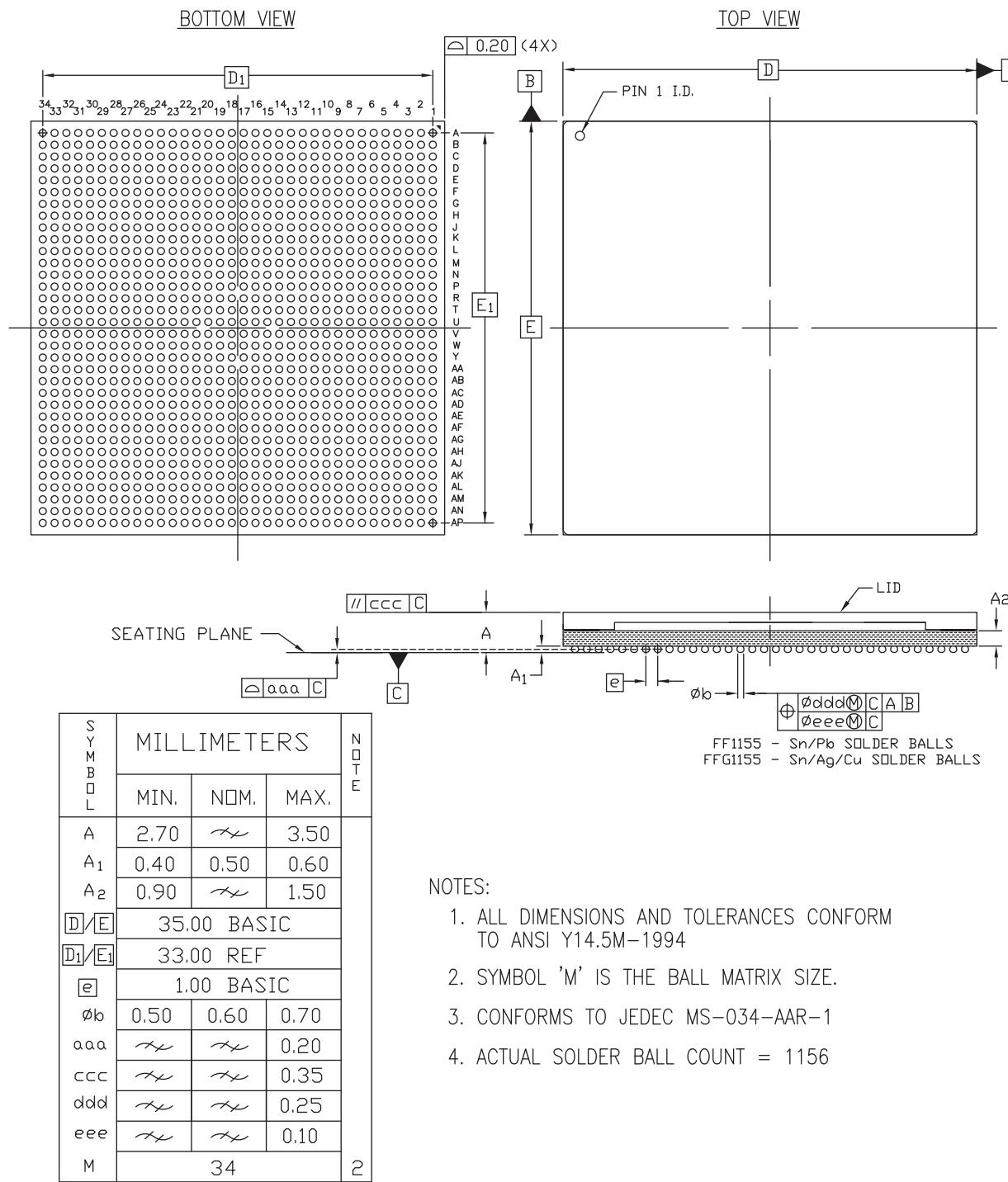
FF1154 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)



ug365_c4_03_100109

Figure 4-4: FF1154 Flip-Chip Fine-Pitch BGA Package Specifications

FF1155 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)



ug365_c4_04_100109

Figure 4-5: FF1155 Flip-Chip Fine-Pitch BGA Package Specifications

FF1156 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)

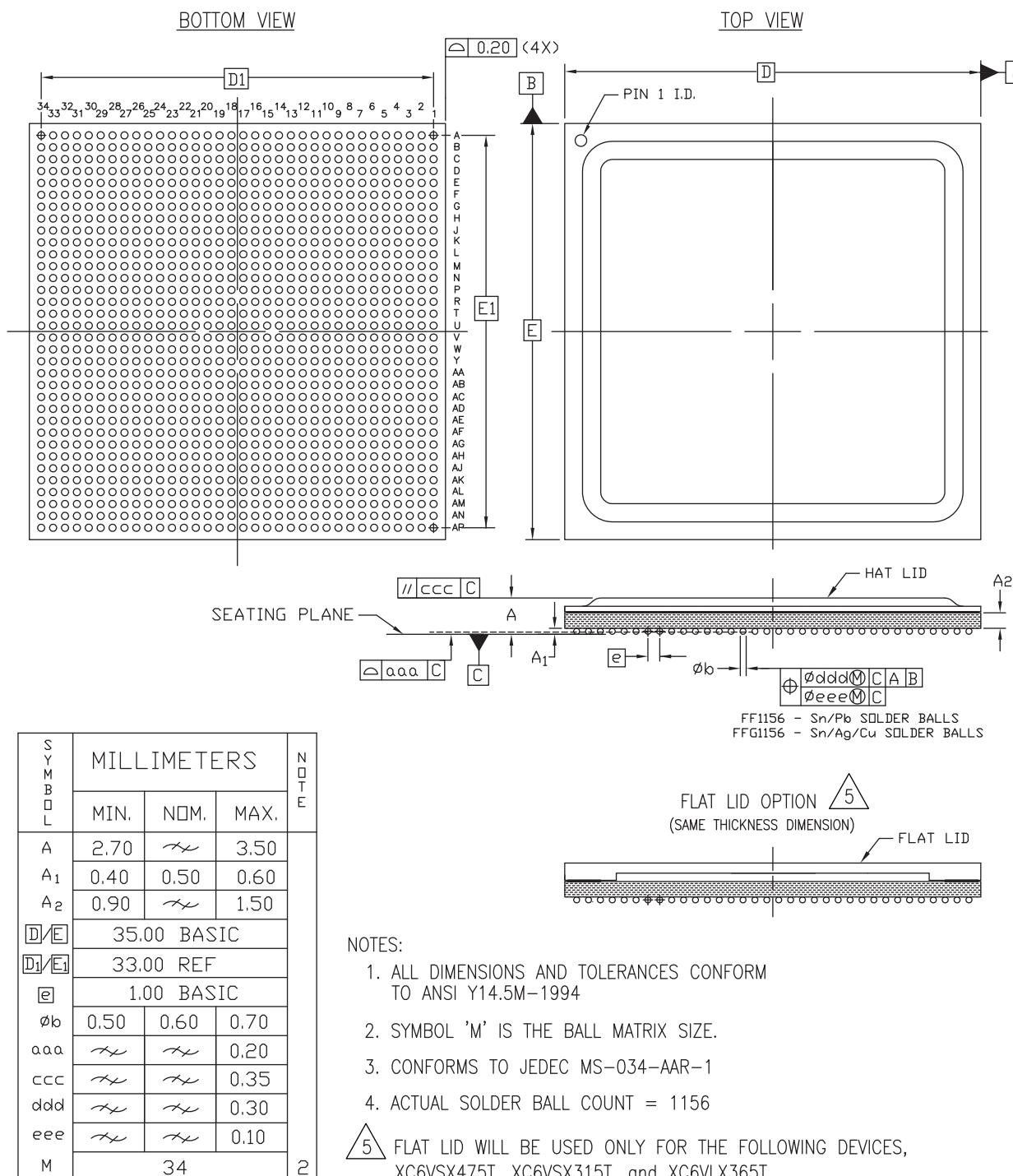
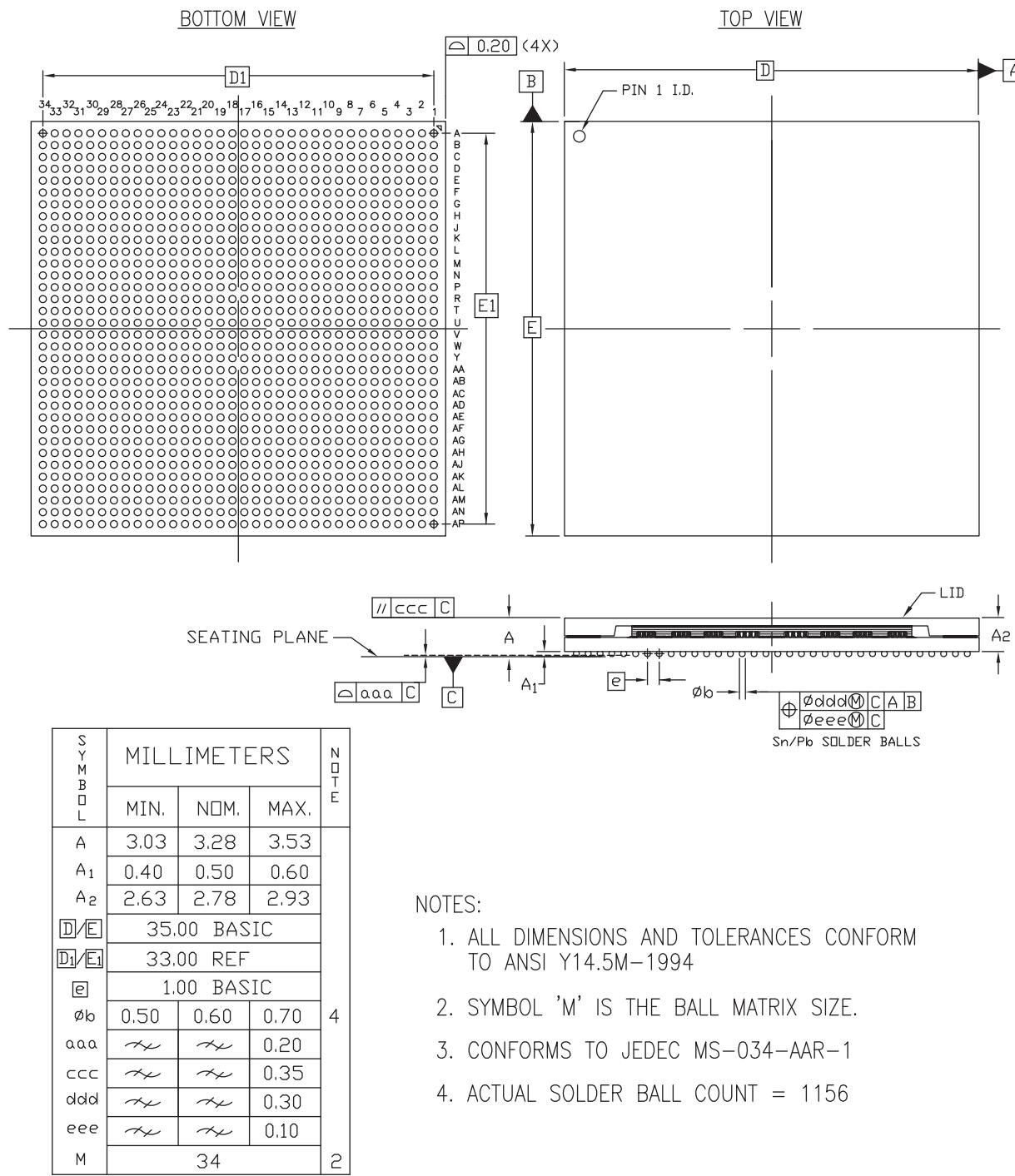


Figure 4-6: FF1156 Flip-Chip Fine-Pitch BGA Package Specifications

ug365_c4_05_100109

RF1156 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)



ug365_c4_14_11111

Figure 4-7: RF1156 Flip-Chip Fine-Pitch BGA Package Specifications

FF1759 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)

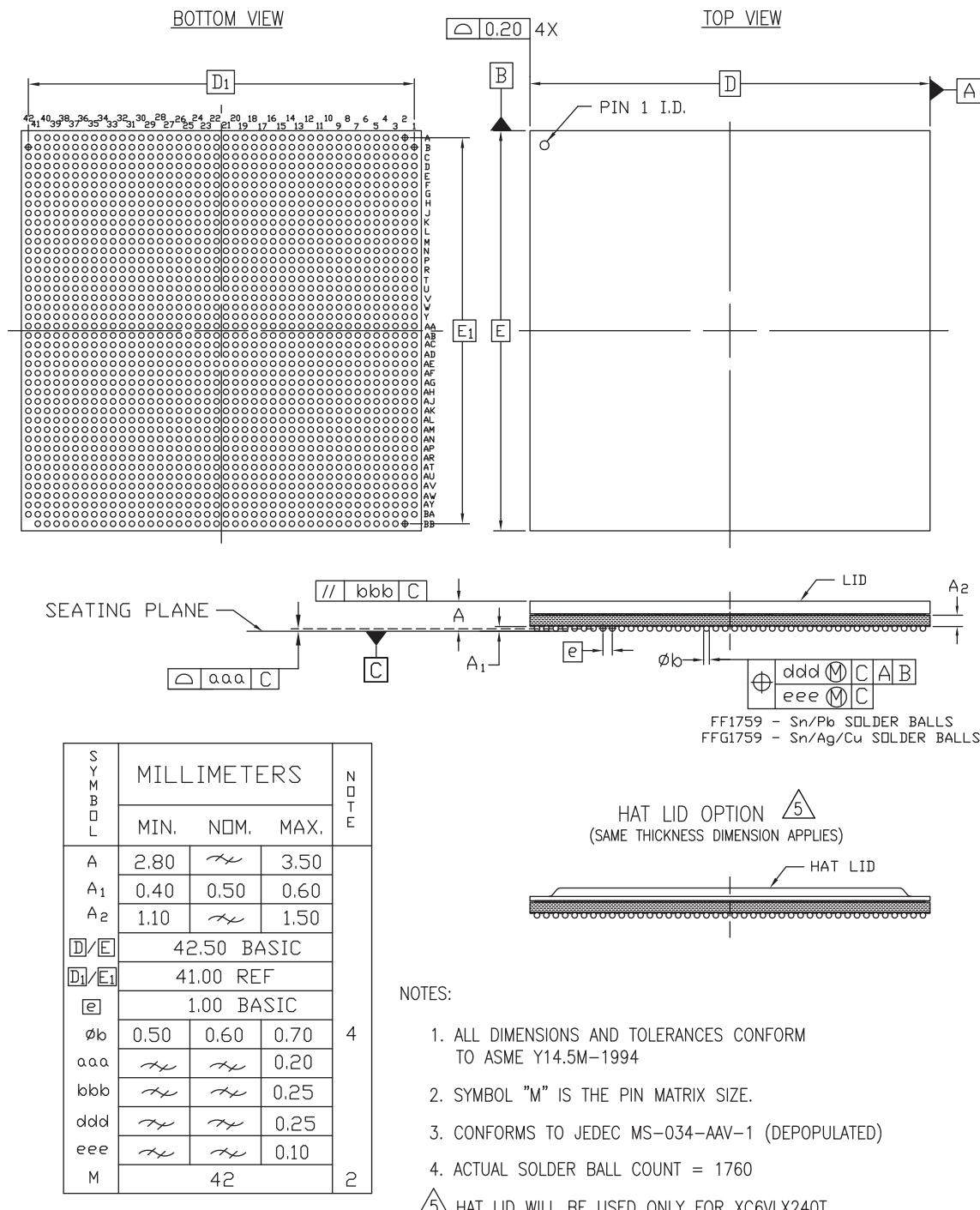


Figure 4-8: FF1759 Flip-Chip Fine-Pitch BGA Package Specification

RF1759 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)

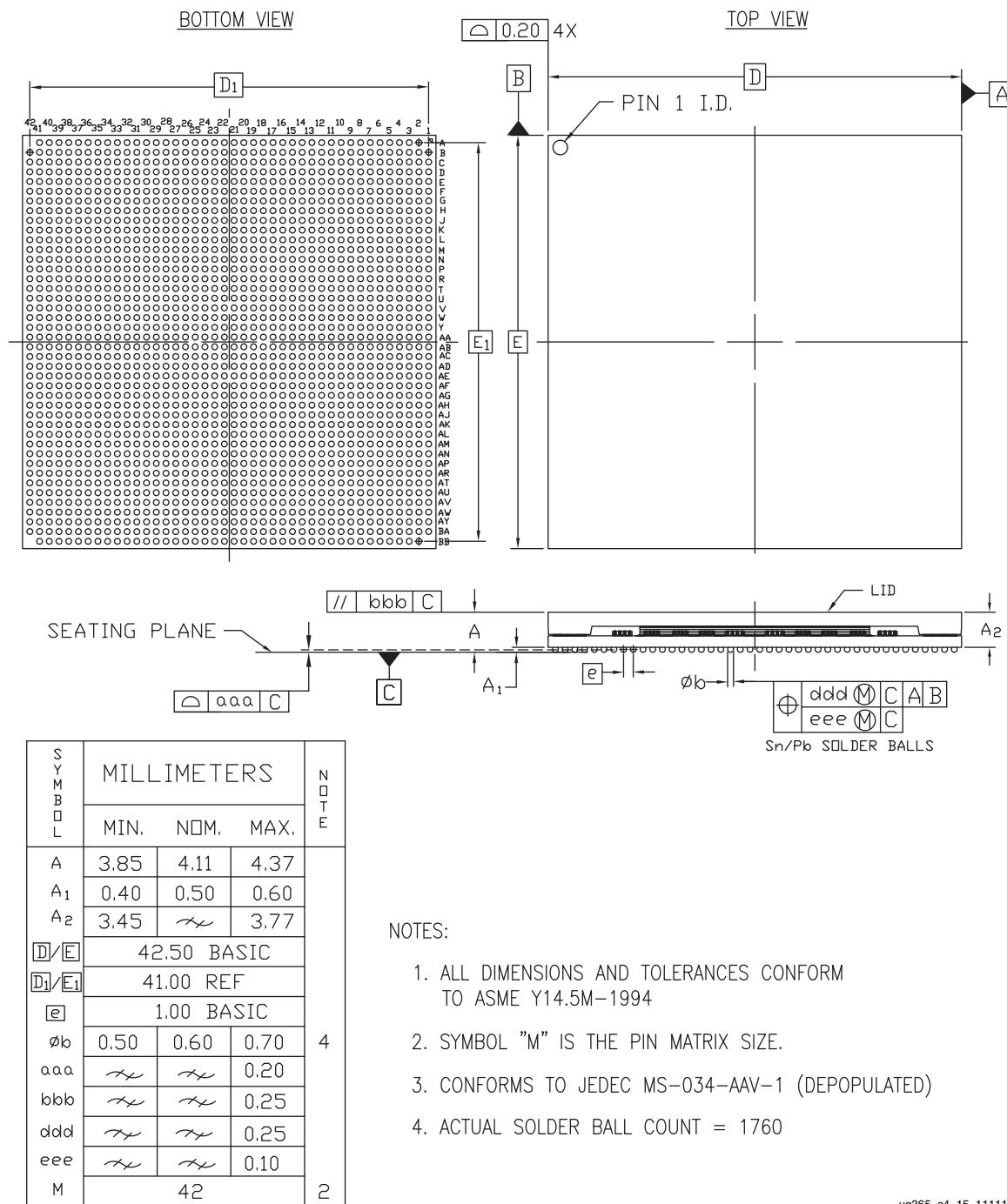
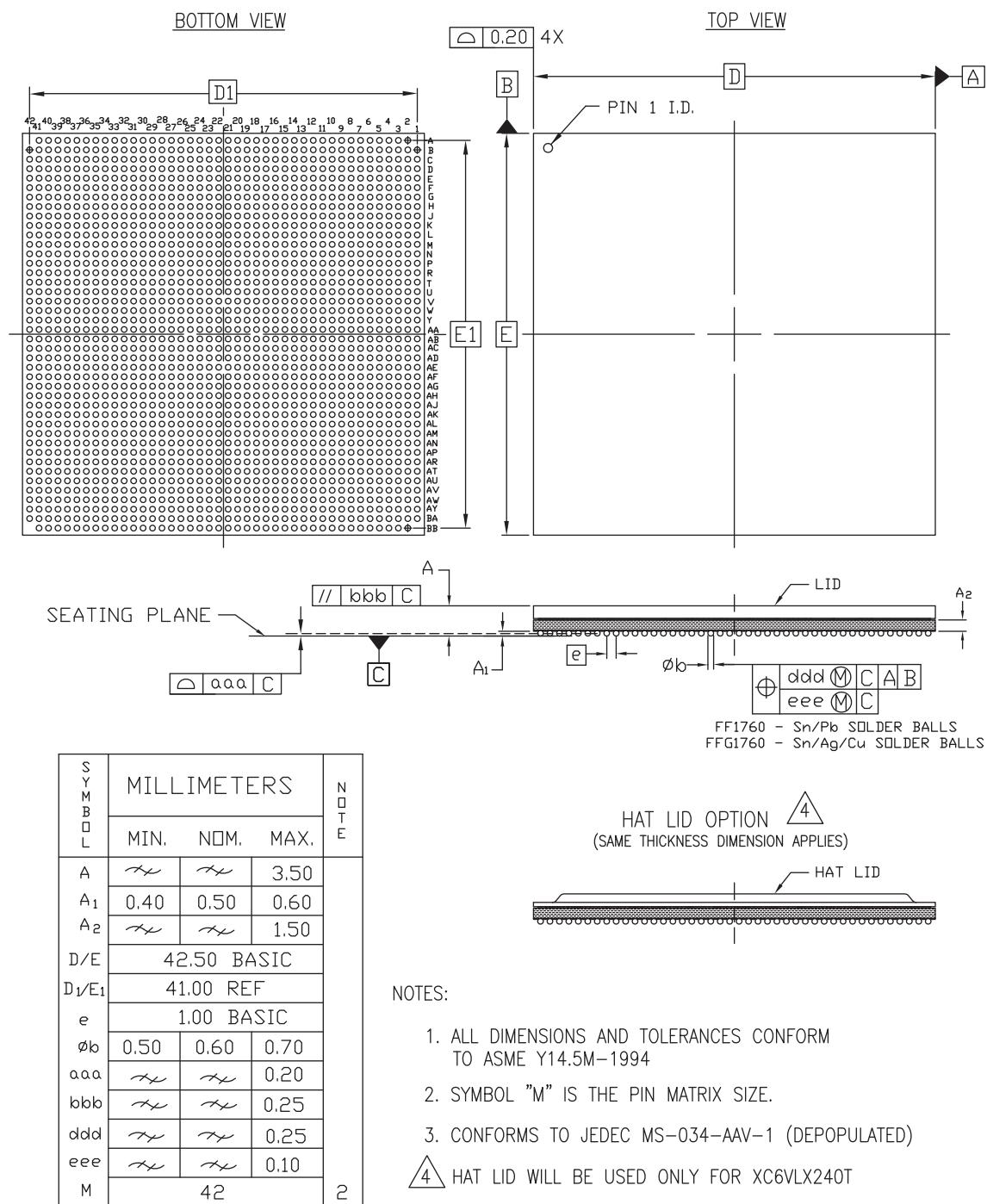


Figure 4-9: RF1759 Flip-Chip Fine-Pitch BGA Package Specification

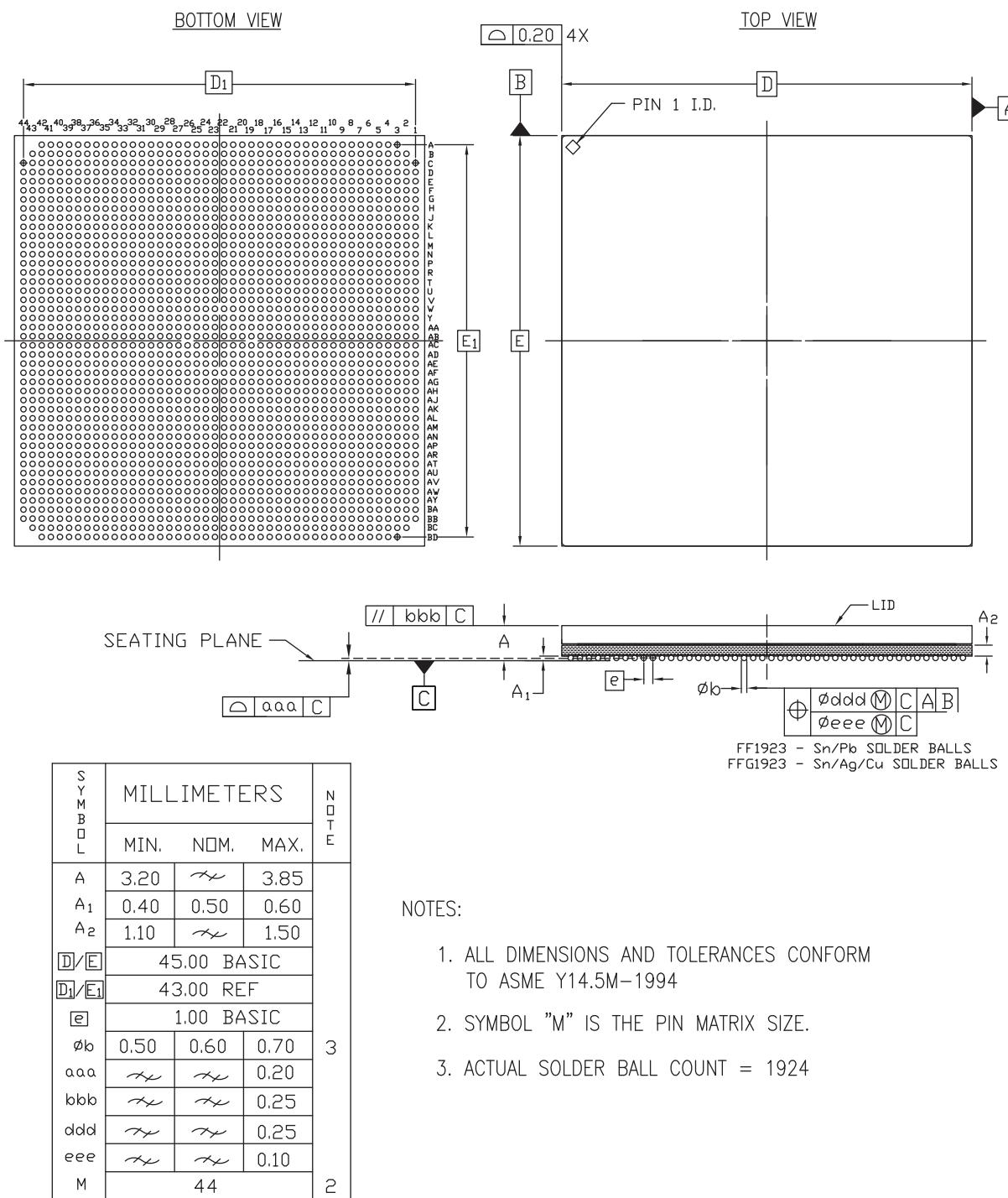
FF1760 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)



ug365_c4_07_100209

Figure 4-10: FF1760 Flip-Chip Fine-Pitch BGA Package Specification

FF1923 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)



ug365_c4_08_100209

Figure 4-11: FF1923 Flip-Chip Fine-Pitch BGA Package Specifications

FF1924 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm Pitch)

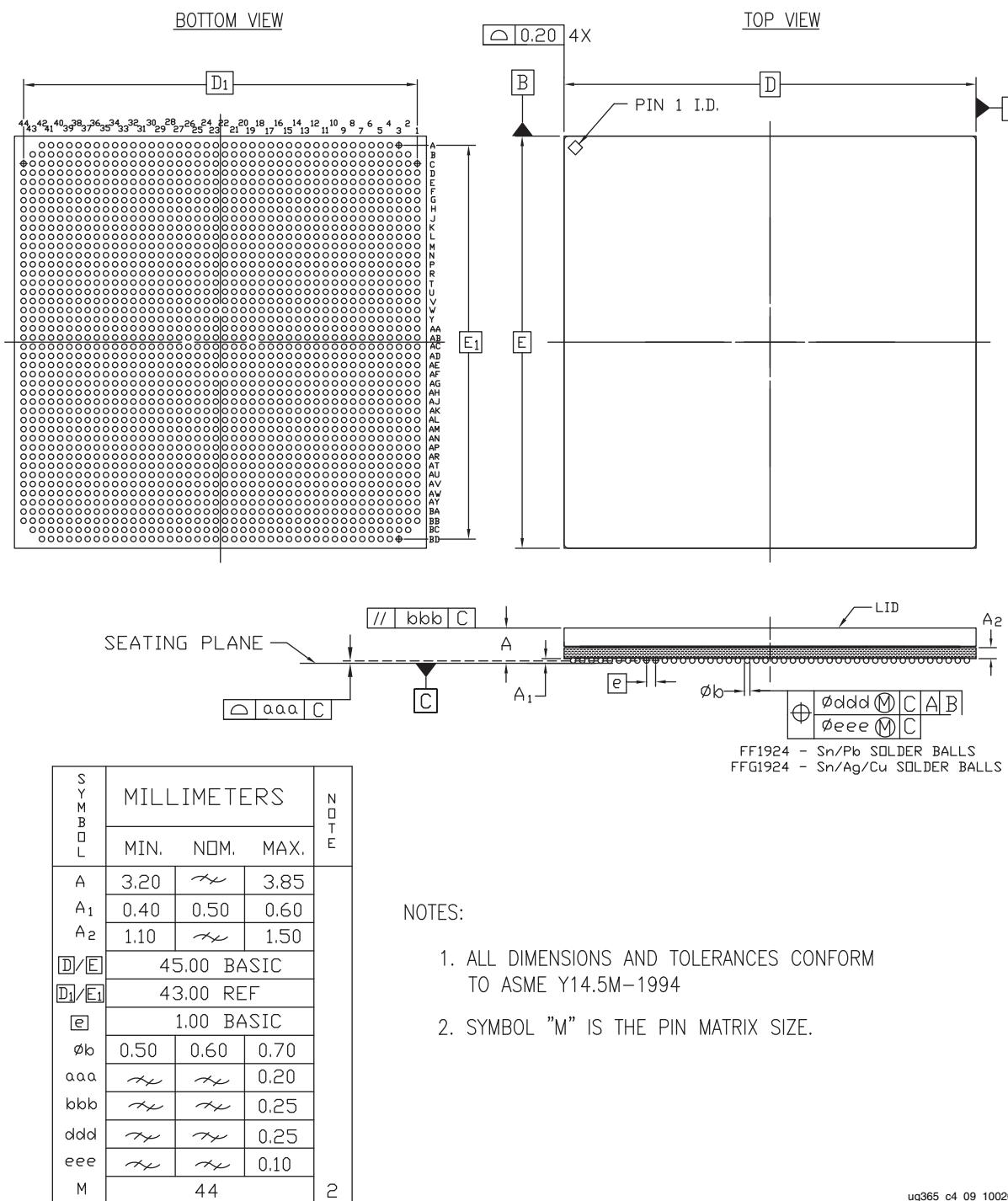


Figure 4-12: FF1924 Flip-Chip Fine-Pitch BGA Package Specifications

Thermal Specifications

Summary

This chapter provides thermal data associated with Virtex-6 FPGA packages. The following topics are discussed:

- [Introduction](#)
- [Thermal Management Strategy](#)
- [Some Thermal Management Options](#)
- [Support for Compact Thermal Models \(CTM\)](#)
- [Soldering Guidelines](#)
- [References](#)

Introduction

Virtex-6 devices are offered exclusively in thermally efficient flip-chip BGA packages. These 1.0 mm flip-chip packages range in pin-count from the smaller 23 x 23 mm FF484 to the 45 x 45 mm FF1924. The suite of packages is used to address the various power requirements of the Virtex-6 devices. All Virtex-6 devices are implemented in the 40 nm process technology.

Similar to Virtex-5 FPGAs, all Virtex-6 devices feature versatile SelectIO™ resources that support a variety of I/O standards. They also include a System Monitor, DSPs, and other traditional features and blocks (such as block RAM) contained in earlier Virtex products.

In line with Moore's law, the transistor count in this family of devices has been increased substantially. Though several innovative features at the silicon level have been deployed to minimize power dissipation, including leakage at the 40 nm node, these products have more densely packed transistors and embedded blocks with the capability to run faster than before. Thus, a fully configured Virtex-6 FPGA design that exploits the fabric speed and incorporates several embedded circuits and systems can present power consumption challenges that must be managed.

Unlike features in an ASIC or a microprocessor, the combination of FPGA features used in a user application are not known to the component supplier. Therefore, it remains a challenge for Xilinx to predict the power requirements of a given FPGA when it leaves the factory. Accurate estimates are obtained when the board design takes shape. For this purpose, Xilinx offers and supports a suite of integrated device power analysis tools to help users quickly and accurately estimate their design power requirements. Virtex-6 devices are supported similarly to previous FPGA products. The uncertainty of design power requirements makes it difficult to apply canned thermal solutions to fit all users. Therefore, Xilinx devices do not come with preset thermal solutions. The user's operating conditions dictate the appropriate solution.

Table 5-1 shows the thermal resistance data for Virtex-6 devices (grouped in the packages offered). The data includes junction-to-ambient in still air, junction-to-case, and junction-to-board data based on standard JEDEC four-layer measurements.

Note: The data in **Table 5-1** is for device/package comparison purposes only. Do not apply directly to your system design. Attempts to recreate this data are only valid using the steady-state measurement technique outlined in JESD51-2a, JESD51-6, and JESD51-8.

- Thermal data is available on the Xilinx website at:
<http://www.xilinx.com/cgi-bin/thermal/thermal.pl>
- Compact package thermal models for these products are available on the Xilinx support download center (under the Device Model tab) at:
www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/device-models.html

Table 5-1: Thermal Resistance Data—All Devices

Package	Package Body Size	Devices	θ_{JA} (°C/W)	θ_{JB} (°C/W)	θ_{JC} (°C/W)	θ_{JA} (°C/W) @ 250 LFM	θ_{JA} (°C/W) @ 500 LFM	θ_{JA} (°C/W) @ 750 LFM
FF484 FFG484	23x23	XC6VLX75T	13.1	3.5	0.28	8.9	7.4	6.8
		XC6VLX130T	12.6	3.1	0.17	8.3	7.0	6.4
FF784 FFG784 RF784	29x29	XC6VLX75T	11.8	3.5	0.28	7.5	6.4	5.8
		XC6VLX130T XQ6VLX130T	11.2	3.1	0.17	7.1	6.0	5.4
		XC6VLX195T	10.9	2.9	0.14	7.0	5.8	5.3
		XC6VLX240T XQ6VLX240T	10.8	2.7	0.11	6.8	5.7	5.2
FF1154 FFG1154	35x35	XC6VHX250T	9.7	2.5	0.09	5.8	4.8	4.3
		XC6VHX380T	9.5	2.3	0.06	5.6	4.6	4.1
FF1155 FFG1155	35x35	XC6VHX255T	9.5	2.3	0.06	5.6	4.6	4.1
		XC6VHX380T	9.5	2.3	0.06	5.6	4.6	4.1
FF1156 FFG1156 RF1156	35x35	XC6VLX130T XQ6VLX130T	10.0	2.9	0.16	6.1	5.1	4.6
		XC6VLX195T	9.9	2.7	0.12	6.0	5.0	4.5
		XC6VLX240T XQ6VLX240T	9.8	2.6	0.10	5.9	4.9	4.4
		XC6VLX365T	9.6	2.4	0.08	5.7	4.7	4.2
		XC6VSX315T XQ6VSX315T	9.6	2.4	0.08	5.7	4.7	4.2
		XC6VSX475T XQ6VSX475T	9.3	2.1	0.10	5.4	4.4	4.0

Table 5-1: Thermal Resistance Data—All Devices (Cont'd)

Package	Package Body Size	Devices	θ_{JA} (°C/W)	θ_{JB} (°C/W)	θ_{JC} (°C/W)	θ_{JA} (°C/W) @ 250 LFM	θ_{JA} (°C/W) @ 500 LFM	θ_{JA} (°C/W) @ 750 LFM
FF1759 FFG1759 RF1759	42.5x42.5	XC6VLX240T XQ6VLX240T	8.2	2.4	0.10	5.0	4.0	3.7
		XC6VLX365T	8.1	2.2	0.08	4.9	3.9	3.6
		XC6VLX550T XQ6VLX550T	7.8	2.0	0.10	4.7	3.8	3.4
		XC6VSX315T XQ6VSX315T	8.0	2.1	0.08	4.9	4.0	3.5
		XC6VSX475T XQ6VSX475T	7.8	1.9	0.10	4.7	3.8	3.3
FF1760 FFG1760	42.5x42.5	XC6VLX550T	7.8	2.0	0.10	4.7	3.8	3.4
		XC6VLX760	7.8	1.9	0.10	4.6	3.7	3.3
FF1923 FFG1923	45x45	XC6VHX255T	7.6	2.0	0.06	4.6	3.7	3.3
		XC6VHX380T	7.6	2.1	0.06	4.6	3.7	3.3
		XC6VHX565T	7.5	2.0	0.04	4.5	3.6	3.2
FF1924 FFG1924	45x45	XC6VHX380T	7.6	2.0	0.06	4.6	3.7	3.3
		XC6VHX565T	7.6	2.0	0.04	4.5	3.6	3.2

Thermal Management Strategy

Xilinx relies on a multi-prong approach with regards to the heat-dissipating potential of Virtex-6 devices:

- Design and Silicon

Significant power reduction in Virtex-6 devices at the 40 nm node is achieved through innovative process and circuit design. For example, transistor static leakage current is minimized by more than 50 percent (comparable devices) by deploying multi-gate oxide transistors in the power-efficient Virtex-6 architecture. Despite these improvements and a lower operating voltage, the base transistor counts are higher for these Virtex-6 devices. They pack higher gate densities and the fabric is faster.

Compared to previous generations, the power consumption is lower for the same design (same function and gate density) in a Virtex-6 FPGA implementation.

However, the increased resources and functionality associated with these higher gate density devices and faster switching fabric implies that more computation is possible in shorter time. Associated with this improved functionality is potential higher power dissipation that would have been worse without the silicon and device-based innovations.

- Packaging

At the package component level, Xilinx has selected the more efficient flip-chip BGA packages, which present a low thermal path to the outside. This package incorporates a heat spreader with a thermal interface material (TIM), as shown in Figure 5-1.

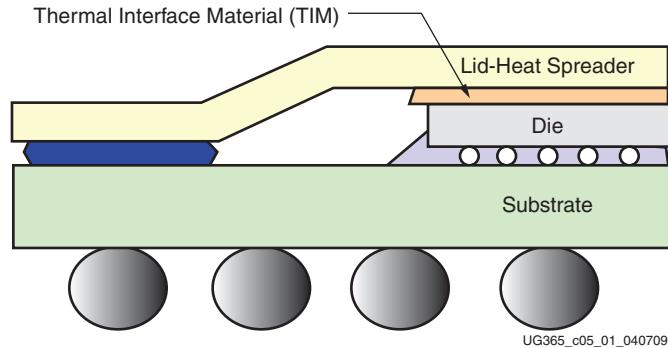


Figure 5-1: Heat Spreader with Thermal Interface Material

Materials with better thermal conductivity and consistent process applications deliver low thermal resistance up to the heat spreader. The junction-to-case thermal resistance (top of heat spreader) of all Virtex-6 FPGA packages is typically less than $0.20^{\circ}\text{C}/\text{W}$. These packages deliver a low resistance platform for heat sink applications.

The parallel effort to ensure optimized package electrical return paths has produced an added benefit of enhanced power and ground plane arrangement in the packages. The boost in copper density on the planes improves the overall thermal conductivity through the laminate. In addition, the extra dense and distributed via fields in the package increase the vertical thermal conductivity. These packages offer up to 20% lower θ_{JB} compared to previous flip-chip packages.

- Heat Sinking Solutions at the System Level

Depending on the system's physical as well as mechanical constraints, the expectation is that the thermal budget is maintained with custom or OEM heat sink solutions, providing the third prong in the thermal management strategy. At this point, Xilinx has left the heat sink solution to the system-level designers who can tailor the design and solution to the constraints of their systems, being fully aware that the part has certain inherent capabilities for delivering the heat to the surface. Heat sink solutions do exist and can be effective on these low θ_{JB} flip-chip platforms.

Table 5-2 illustrates a finned heat sink solution matrix in Network environment (1U and 2U) arrangement for 35 mm packages and up for power ranging from 15W to 40W. The AAVID standard finned heat sink offerings are used to illustrate the coverage given thermal budgets of $\Delta T = 35^{\circ}\text{C}$ and $\Delta T = 45^{\circ}\text{C}$ scenarios. Other heat sink configurations can be explored similarly.

Table 5-2: Finned Heat Sink Solution Matrix for Large Flip-chip BGA in Network

Package Power (W)		35 x 35 mm FF1156		42.5 x 42.5 mm FF1759/FF1760	
		$\Delta T=35^{\circ}\text{C}$	$\Delta T=45^{\circ}\text{C}$	$\Delta T=35^{\circ}\text{C}$	$\Delta T=45^{\circ}\text{C}$
15W	1U ⁽⁵⁾	Note 1		Note 1	
	2U ⁽⁶⁾	Note 1		Note 1	
25W	1U ⁽⁵⁾	Note 4	Note 2	Note 4	Note 2
	2U ⁽⁶⁾	Note 2	Note 1	Note 2	Note 1

Table 5-2: Finned Heat Sink Solution Matrix for Large Flip-chip BGA in Network

Package Power (W)		35 x 35 mm FF1156		42.5 x 42.5 mm FF1759/FF1760	
		$\Delta T=35^\circ\text{C}$	$\Delta T=45^\circ\text{C}$	$\Delta T=35^\circ\text{C}$	$\Delta T=45^\circ\text{C}$
35W	1U ⁽⁵⁾	Note 4	Note 3	Note 4	Note 3
	2U ⁽⁶⁾	Note 4	Note 2	Note 4	Note 2
40W	1U ⁽⁵⁾	–	–	Note 4	Note 3
	2U ⁽⁶⁾	–	–	Note 3	Note 2

Notes:

1. Solution available at 200 LFM, for example, AAVID finned part number 68520, 72390, 72415.
2. Solution available at 400 LFM, for example, AAVID finned part number 68520, 69920.
3. Solution available at 600 LFM, for example, AAVID finned part number 72390, 69920, 74590.
4. No standard. AAVID finned solution below 600 LFM—custom finned might be required.
5. For 1U height—(max heat sink height = 26 mm).
6. For 2U height—(max heat sink height = 64 mm).

The Virtex-6 FPGA packages can be described as medium- and high-performance packages based on their power handling capabilities. All Virtex-6 FPGA packages can use thermal enhancements, ranging from simple airflow to schemes that can include passive as well as active heat sinks. This is particularly true for the bigger flip-chip BGA packages where system designers have the option to further enhance the packages with bigger and more elaborate heat sinks to handle excesses of 25W with arrangements that consider system –physical constraints as illustrated in [Table 5-2](#).

Some Thermal Management Options

The flip-chip thermal management chart in [Figure 5-2](#) illustrates simple but incremental power management schemes that can be applied on a flip-chip BGA package.

Low End 1–6W	Bare Package with Moderate Air 8–12°C/W	Bare Package Package can be used with moderate airflow within a system	
Mid Range 10–25W	Passive H/S + Air 5–10°C/W	Packaged Used with Various Forms of Passive Heat Sinks Heat spreader techniques	
High End 25–50W	Active Heat Sink 2–3°C/W or Better	Package Used with Active Heat Sinks TEC and board level heat spreader techniques	

Figure 5-2: Thermal Management Options for Flip-Chip BGA Packages

- For moderate power dissipation (less than 10–25W), the use of passive heat sinks and heat spreaders attached with thermally conductive double-sided tapes or retainers (with TIM around 0.2°C/W) can offer quick thermal solutions in these packages.
- The use of finned, external, and passive heat sinks can be effective for dissipating up to 10–25W in the larger packages. Since the more efficient external heat sinks tend to be tall and heavy, additional design considerations can help protect component joints from heat sink induced stress cracks. Whenever a bulky heat sink is considered it is advisable to use of spring-loaded pins or clips that transfer the mounting stress to a circuit board.
- The flip-chip BGA packages offered for Virtex-6 devices are thermally enhanced BGAs with the die facing down (see [Note](#)). These packages have an exposed metal heat sink at the top. These high-end thermal packages lend themselves to the application of efficient external heat sinks (passive or active) for further heat removal efficiency. Again, precautions must be taken to prevent component damage when a bulky heat sink is attached. The thermal interface resistance needs to be controlled to take full advantage of these packages.

Note: Lidless (FB) packages are not thermally enhanced. See guidelines for applying heat sinks to lidless packages in [Appendix A, Recommended PCB Design Rules for BGA Packages](#).

- An active heat sink might include a simple heat sink incorporating a mini fan or even a Peltier Thermoelectric Cooler (TEC) with a fan to carry away any dissipated heat. When considering the use of a TEC for heat management, consultation with experts in using the device is important because these devices can be reversed and cause damage to components. Also condensation can be an issue with these devices.

- The printed circuit board on which the package is mounted can have a significant impact on thermal performance. As much as 60 to 80 percent of the dissipated heat can go through the BGA balls and thus to the board. A typical systems board is larger than the standard 4 x 4 in JEDEC thermal board. Components mounted on these boards with multiple copper layers and several internal vias show low effective junction-to-ambient thermal resistances.

Table 5-3 shows this impact as an FF1148 flip-chip package's effective junction to ambient resistance is changed depending on the mounting board.

Table 5-3: Impact of Mounted Board Characteristics on θ_{JA} (FF1148)

Xilinx 35 x 35mm FF1148		θ_{JA} (°C/W) for Different Board Sizes		
		4 x 4 in	10 x 10 in	20 x 20 in
Layer Count of Mounted Board	4	9.1 ⁽¹⁾	8.3	–
	8	8.0	5.5	4.9
	12	7.5	4.7	4.4
	16	7.2	4.5	4.2
	24	–	4.3	4.0

Notes:

- Base JEDEC Mount Conditions

- Designs can be implemented to take advantage of the board's ability to spread heat. The effect of the board is dependent on its size and how it conducts heat. Board size, the level of copper traces, and the number of buried copper planes all lower the junction-to-ambient thermal resistance for a package mounted on the board. The cold ring junction-to-board thermal data for Virtex-6 FPGA packages are given in Table 5-1. Users need to be aware that a direct heat path to the board from a component also exposes the component to the effect of other heat sources on the board, particularly if the board is not cooled effectively. An otherwise cooler component can be heated by other heat contributing components on the board.

Heat Sink Removal Procedure

The heat spreader on the package provides mechanical protection for the die and serves as the primary heat dissipation path. It is attached with an epoxy adhesive to provide the necessary adhesion strength to hold the package together. For an application in which an external heat sink subjects the lid adhesion joint to continuous tension or shear, extra support might be required.

In addition, if the removal of an attached external heat sink subjects the joint to tension, torque, or shear, care should be exercised to ensure that the lid itself does not come off. In such cases, it has been found useful to use a small metal blade or metal wire to break the lid to heat sink joint from the corners and carefully pry the heat sink off. The initial cut should reach far in enough so that the blade has leverage to exert upward pressure against the heat sink. Contact the heat sink and heat sink adhesive manufacturer for more specific recommendations on heat sink removal.

Package Pressure Handling Capacity

For mounted BGA packages, including flip chips, a direct compressive (non-varying) force applied normally to the lid or top of package with a tool head that coincides with the lid (or is slightly bigger) will not induce mechanical damage to the device including external balls, provided the force is not over 5.0 grams per external ball, and the device and board are supported to prevent any flexing or bowing.

These components are tested in sockets with loads in the 5 to 10 grams/ball range for short durations. Analysis using a 10g/ball (e.g., 11.56 kg for FF1156) showed little impact on short term but some creep over time. 20 grams/ball and 45 grams/ball loads at 85°C over a six week period has shown the beginning of bridging of some outer balls; these were static load tests. The component might survive forces greater than the 5 gram limit while in short-term situations. However, sustained higher loads should be avoided (particularly if they are overlaid with thermal or power cycle loads). Within the recommended limits, circuit board needs to be properly supported to prevent any flexing resulting from force application. Any flexing or bowing resulting from such a force can likely damage the package-to-board connections. Besides the damage that can occur from bending, the only major concern is long-term creep and bulging of the solder balls in compression to cause bridging. For the life of a part, staying below the recommended limit will ensure against that remote possibility.

Support for Compact Thermal Models (CTM)

[Table 5-1](#) provides the traditional thermal resistance data for Virtex-6 devices. These resistances are measured using a prescribed JEDEC standard that might not necessarily reflect the user's actual board conditions and environment. The quoted θ_{JA} and θ_{JC} numbers are environmentally dependent, and JEDEC has traditionally recommended that these be used with that awareness. For more accurate junction temperature prediction, these might not be enough, and a system-level thermal simulation might be required. Though Xilinx continues to support these figure of merit data, for Virtex-6 FPGAs, boundary conditions independent compact thermal models (BCI-CTM) are also available to assist users in their thermal simulations.

Two-resistor as well as eight to ten-resistor network models are offered for all Virtex-6 devices. These compact models seek to capture the thermal behavior of the packages more accurately at predetermined critical points (junction, case, top, leads, and so on) with the reduced set of nodes as illustrated in [Figure 5-3](#).

Unlike a full 3D model, these are computationally efficient and work well in an integrated system simulation environment. Delphi CTM models are available on the Xilinx support download center (under the Device Model tab) at:

www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/device-models.html

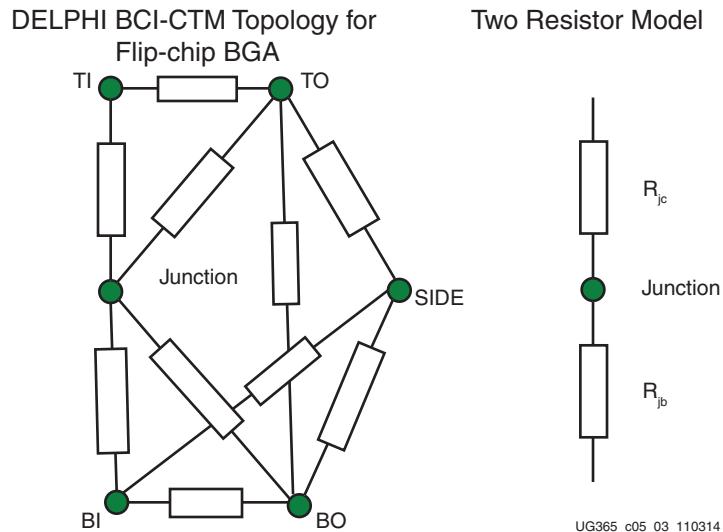


Figure 5-3: Thermal Model Topologies

The CTM models are based on the DELPHI approach that JEDEC has proposed. Since the JEDEC neutral (XML) format proposal has not been adopted yet, the DELPHI approach is used to generate these files and the data saved in the NATIVE and proprietary file formats of the targeted CFD tools - rather than follow a neutral file format. The CTM libraries are available in Flotherm (PDML) format – good for V5.1 and above and Icepak (version 4.2 and above) format. See [References](#).

Soldering Guidelines

To implement and control the production of surface-mount assemblies, the dynamics of the solder reflow process and how each element of the process is related to the end result must be thoroughly understood.

Note: Xilinx recommends that customers qualify their custom PCB assembly processes using package samples. [UG112: Device Package User Guide](#) contains further details on recommended assembly procedures.

The primary phases of the reflow process are:

1. Melting the particles in the solder paste
2. Wetting the surfaces to be joined
3. Solidifying the solder into a strong metallurgical bond

In a Pb-free soldering system, the sequences are the same. However, for the Pb-free soldering system, higher reflow temperature is applied. The peak reflow temperature of a plastic surface-mount component (PSMC) body should not be more than 250°C maximum (260°C for dry rework only) for Pb-free packages (220°C for eutectic packages), and is package size dependent. For multiple BGAs in a single board and because of surrounding component differences, Xilinx recommends checking all BGA sites for varying temperatures.

The infrared reflow (IR) process is strongly dependent on equipment and loading. Components might overheat due to lack of thermal constraints. Unbalanced loading can lead to significant temperature variation on the board. These guidelines are intended to assist users in avoiding damage to the components; the actual profile should be

determined by those using these guidelines. For complete information on package moisture / reflow classification and package reflow conditions, refer to the Joint IPC/JEDEC Standard J-STD-020C.

Sn/Pb Reflow Soldering

[Figure 5-4](#) shows typical conditions for solder reflow processing of Sn/Pb soldering using IR/convection. Both IR and convection furnaces are used for BGA assembly. The moisture sensitivity of PSMCs must be verified prior to surface-mount flow.

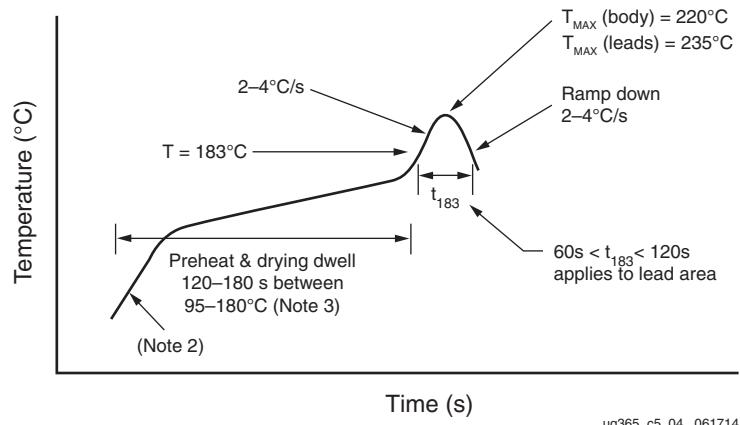


Figure 5-4: Typical Conditions for IR Reflow Soldering of Sn/Pb Solder

Notes for [Figure 5-4](#):

1. Maximum temperature range = 220°C (body). Minimum temperature range before 205°C (leads/balls).
2. Preheat drying transition rate 2–4°C/s
3. Preheat dwell 95–180°C for 120–180 seconds
4. IR reflow must be performed on dry packages

Pb-Free Reflow Soldering

Xilinx uses SnAgCu (SAC305) solder balls for BGA packages. In addition, suitable material are qualified for the higher reflow temperatures (245°C–250°C) required by Pb-free soldering processes. Xilinx recommends soldering SAC305 BGA packages with SAC305 solder paste.

The optimal profile must take into account the solder paste/flux used, the size of the board, the density of the components on the board, and the mix between large components and smaller, lighter components. Profiles should be established for all new board designs using thermocouples at multiple locations on the component. In addition, if there is a mixture of devices on the board, then the profile should be checked at various locations on the board. Ensure that the minimum reflow temperature is reached to reflow the larger components and at the same time, the temperature does not exceed the threshold temperature that might damage the smaller, heat sensitive components.

[Table 5-4](#) and [Figure 5-5](#) provide guidelines for profiling Pb-free solder reflow.

In general, a gradual, linear ramp into a spike has been shown by various sources to be the optimal reflow profile for Pb-free solders ([Figure 5-5](#)). SAC305 alloy reaches full liquidus

temperature at 235°C. When profiling, identify the possible locations of the coldest solder joints and ensure that those solder joints reach a minimum peak temperature of 235°C for at least 10 seconds. It might not be necessary to ramp to peak temperatures of 260°C. Reflowing at high peak temperatures of 260°C and above can damage the heat sensitive components and cause the board to warp.

Users should reference the latest IPC/JEDEC J-STD-020 standard for the allowable peak temperature on the component body. The allowable peak temperature on the component body is dependent on the size of the component. Refer to [Table 5-4](#) for peak package reflow body temperature information. In any case, use a reflow profile with the lowest peak temperature possible.

Table 5-4: Pb-Free Reflow Soldering Guidelines

Profile Feature	Convection, IR/Convection
Ramp-up rate	2°C/s maximum
Preheat Temperature 150°–200°C	60–120 seconds
Temperature maintained above 217°C	60–150 seconds (60–90 seconds typical)
Time within 5°C of actual peak temperature	30 seconds maximum
Peak Temperature (lead/ball)	235°C minimum, 245°C typical (depends on solder paste, board size, components mixture)
Peak Temperature (body)	245°C–250°C, package body size dependent (reference Table 5-5)
Ramp-down Rate	2°C/s maximum
Time 25°C to Peak Temperature	3.5 minutes minimum, 5.0 minutes typical, 8 minutes maximum

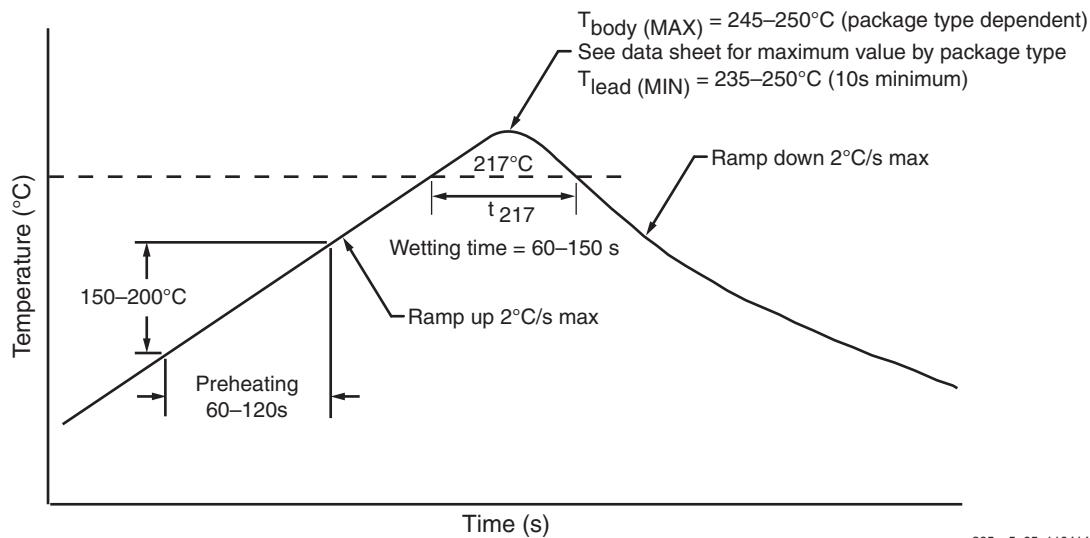


Figure 5-5: Typical Conditions for Pb-Free Reflow Soldering

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Post Reflow/Cleaning/Washing

Many PCB assembly subcontractors use a no-clean process in which no post-assembly washing is required. Although a no-clean process is recommended, if cleaning is required, Xilinx recommends a water-soluble paste and a washer using a deionized-water. Baking after the water wash is recommended to prevent fluid accumulation. Typical bake conditions are 125°C for 4-6 hours. These are guidelines only. Always use manufacturing best practices.

Cleaning solutions or solvents are not recommended because some solutions contain chemicals that can compromise the lid adhesive, thermal compound, or components inside the package.

Conformal Coating

Xilinx has no information about the reliability of flip-chip BGA packages on a board after exposure to conformal coating. Any process using conformal coating should be qualified for the specific use case to cover the materials and process steps.

Note: Xilinx does not recommend using Toluene-based conformal coatings because they can weaken the lid adhesive used in Xilinx packages.

**Table 5-5: Peak Package Reflow Body Temperature for Xilinx Pb-Free Packages
(Based on J-STD-020 Standard)**

Package	Peak Package Reflow Body Temperature	JEDEC Moisture Sensitivity Level (MSL)
BGA		
Flip-Chip	FFG484	
	FFG784	
	FFG1154	
	FFG1155	
	FFG1156	250°C
	FFG1759	
	FFG1760	
	FFG1923	
	FFG1924	
	RF784	
	RF1156	225°C
	RF1759	4

Notes:

- See the specific Virtex-6 device data sheets:
[DS150, Virtex-6 Family Overview](#)
[DS152, Virtex-6 FPGA Data Sheet: DC and AC Switching Characteristics](#)
[DS155, Defense-Grade Virtex-6Q Family Overview](#)

For sophisticated boards with a substantial mix of large and small components, it is critical to minimize the ΔT across the board ($<10^{\circ}\text{C}$) to minimize board warpage and thus, attain higher assembly yields. Minimizing the ΔT is accomplished by using a slower rate in the warm-up and preheating stages. Xilinx recommends a heating rate of less than $1^{\circ}\text{C}/\text{s}$ during the preheating and soaking stages, in combination with a heating rate of not more than $2^{\circ}\text{C}/\text{s}$ throughout the rest of the profile.

It is also important to minimize the temperature gradient on the component, between top surface and bottom side, especially during the cooling down phase. The key is to optimize cooling while maintaining a minimal temperature differential between the top surface of the package and the solder joint area. The temperature differential between the top surface of the component and the solder balls should be maintained at less than 7°C during the critical region of the cooling phase of the reflow process. This critical region is in the part of the cooling phase where the balls are not completely solidified to the board yet, usually between the 200°C – 217°C range. To efficiently cool the parts, divide the cooling section into multiple zones, with each zone operating at different temperatures.

Further information is available on Xilinx [Pb-free solutions](#), as well as the Pb-free reflow process at [XAPP427: Implementation and Solder Reflow Guidelines for Pb-Free Packages](#).

References

The following websites contain additional information on heat management and contact information.

- Wakefield: www.wakefield-vette.com
- Aavid: www.aavid.com
- Advanced Thermal Solutions: www.qats.com
- CTS: www.ctscorp.com

Refer to the following websites for interface material sources:

- Henkel: www.henkel.com
- Bergquist Company: www.bergquistcompany.com
- AOS Thermal Compound: www-aosco.com
- Chomerics: www.chomerics.com
- Kester: www kester.com

Refer to the following websites for CFD tools Xilinx supports with thermal models.

- Mentor: Flotherm <http://www.mentor.com>
- ANSYS: Icepak - www.ansys.com

Package Marking

All Virtex-6 devices have package top-markings similar to the example shown in [Figure 6-1](#) and explained in [Table 6-1](#).

Note: The informational product change customer notice [XCN11022: Product Marking Change](#) outlines a change to the top marking process from an ink mark to laser marking. The previous top mark included an ink patch.

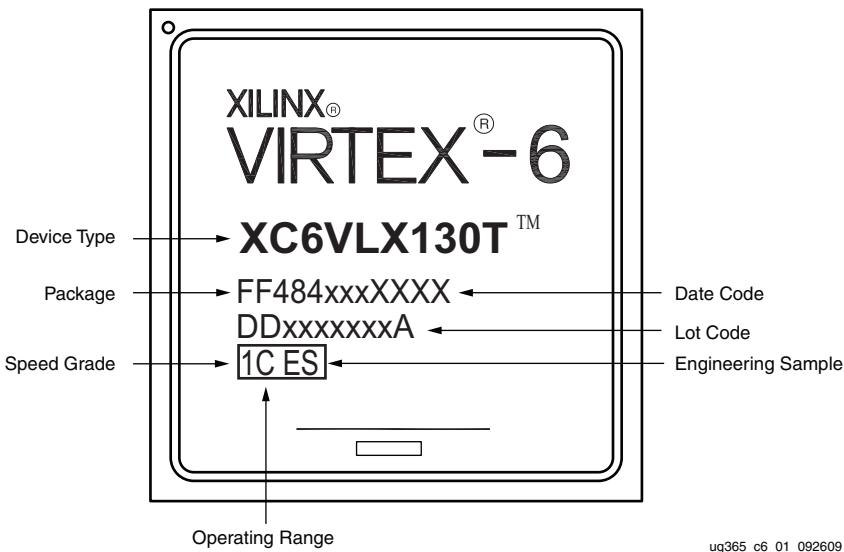


Figure 6-1: Virtex-6 Device Package Marking

Table 6-1: Xilinx Device Marking Definition—Example

Item	Definition
Xilinx Logo	Xilinx logo, Xilinx name with trademark, and trademark-registered status.
Family Brand Logo	Virtex-6 family name with trademark and trademark-registered status. This line is optional and could appear blank.
1st Line	Device type.
2nd Line	Package code, circuit design revision, the location code for the wafer fab, the geometry code, and date code. A G in the third letter of a package code indicates a Pb-free RoHS compliant package. For more information on these packages see Pb-Free and RoHS Compliant Products .
3rd Line	Ten alphanumeric characters for Assembly, Lot, and Step information. The last digit is usually an A or an M if a stepping version does not exist.

Table 6-1: Xilinx Device Marking Definition—Example (Cont'd)

Item	Definition	
4th Line	Device speed grade and temperature range. If a grade is not marked on the package, the product is considered commercial grade. Other variations for the 4th line:	
	L1C	The <i>L1C</i> indicates a lower-power (0.9V core voltage) device with a -1 speed grade in a commercial package.
	1C xxxx	The <i>xxxx</i> indicates the SCD for the device. An SCD is a special ordering code that is not always marked in the device top mark.
	1C ES	The <i>ES</i> indicates an Engineering Sample.

Packing and Shipping

Introduction

The Virtex-6 devices are packed in trays (Table 7-1). Trays are used to pack most of Xilinx surface-mount devices since they provide excellent protection from mechanical damage. In addition, they are manufactured using antistatic material to provide limited protection against ESD damage and can withstand a bake temperature of 125°C. The maximum operating temperature is 140°C.

Table 7-1: Standard Device Counts per Tray and Box

Package	Maximum Number of Devices Per Tray	Maximum Number of Units in One Internal Box
FF/FFG484	60	300
FF/FFG784	36	180
RF784		
FF/FFG1154		
FF/FFG1155	24	120
FF/FFG1156		
RF1156		
FF/FFG1760	12	60
FF/FFG1923	12	36
FF/FFG1924		

Recommended PCB Design Rules for BGA Packages

Xilinx® provides the diameter of a land pad on the component side. This information is required prior to the start of the board layout so the board pads can be designed to match the component-side land geometry. The typical values of these land pads are described in [Figure A-1](#) and summarized in [Table A-1](#). For Xilinx BGA packages, non-solder mask defined (NSMD) pads on the board are suggested to allow a clearance between the land metal (diameter L) and the solder mask opening (diameter M) as shown in [Figure A-1](#). An example of an NSMD PCB pad solder joint is shown in [Figure A-2](#). It is recommended to have the board land pad diameter with a 1:1 ratio to the package solder mask defined (SMD) pad for improved board level reliability.

The space between the NSMD pad and the solder mask as well as the actual signal trace widths depend on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller.

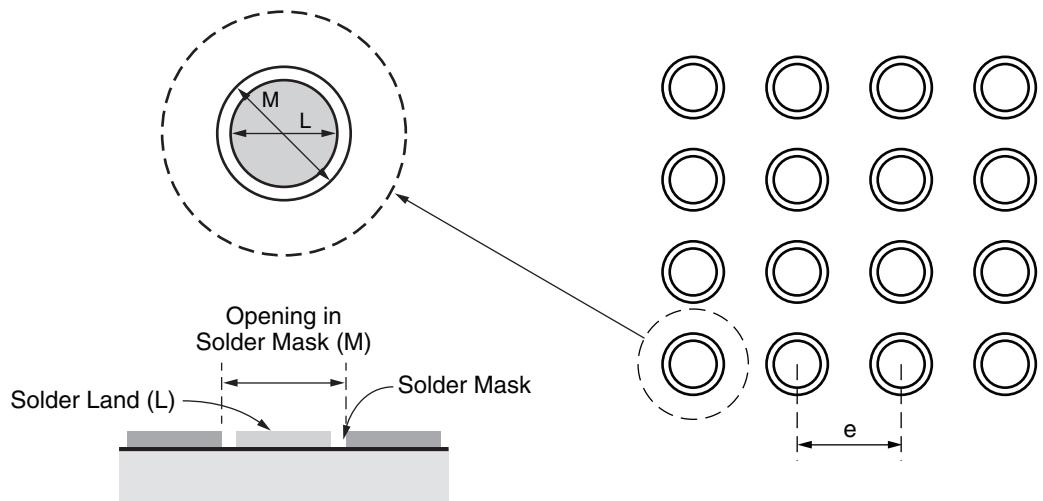
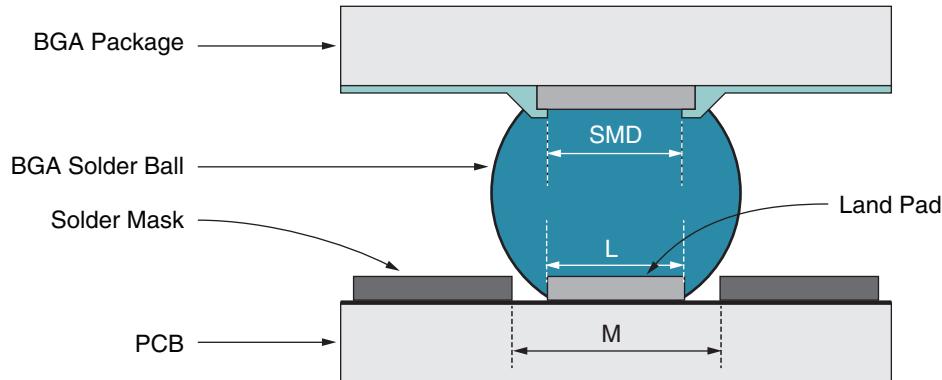


Figure A-1: Suggested Board Layout of Soldered Pads for BGA Packages



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Figure A-2: Example of an NSMD PCB Pad Solder Joint

Table A-1: Recommended PCB Design Rules for All FF(G) Packages

Design Rule	FF(G) Packages (Dimensions in mm)
Component Land Pad Diameter (SMD) ⁽¹⁾	0.53
Solder Land (L) Diameter	0.45
Opening in Solder Mask (M) Diameter	0.55
Solder (Ball) Land Pitch (e)	1.00
Line Width Between Via and Land (w)	0.13
Distance Between Via and Land (D)	0.70
Via Land (VL) Diameter	0.61
Through Hole (VH) Diameter	0.300

Notes:

1. Component land pad diameter refers to the pad opening on the component side (solder mask defined).