

The Electronics for the Upgrade of the CMS Outer Tracker

CMS Upgrade Comprehensive Review

29 June 2016

Francois Vasey

Many thanks to CMS Tracker collaborators,
too numerous to be acknowledged individually



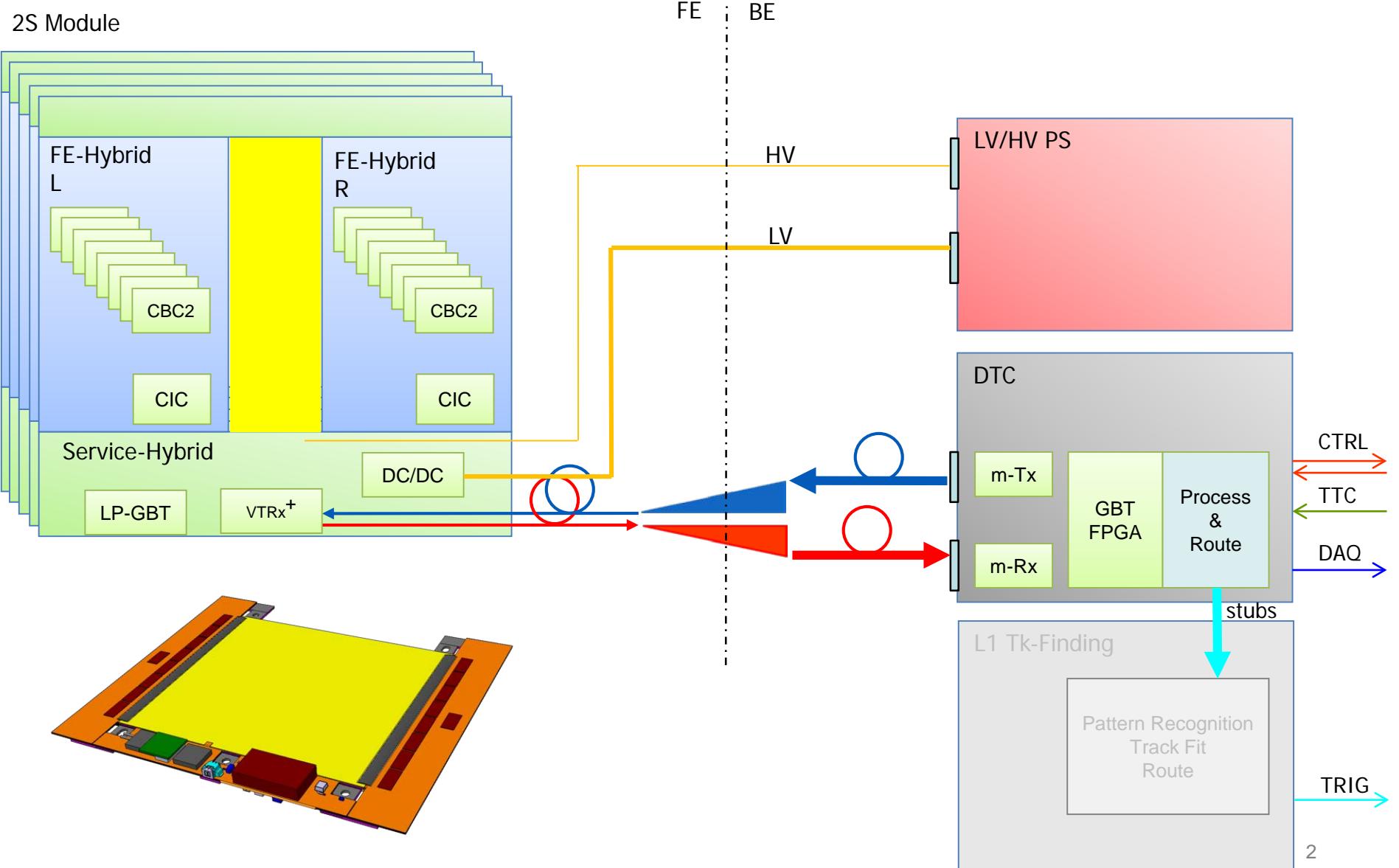
The Electronics for the Upgrade of the CMS Outer Tracker

Outline

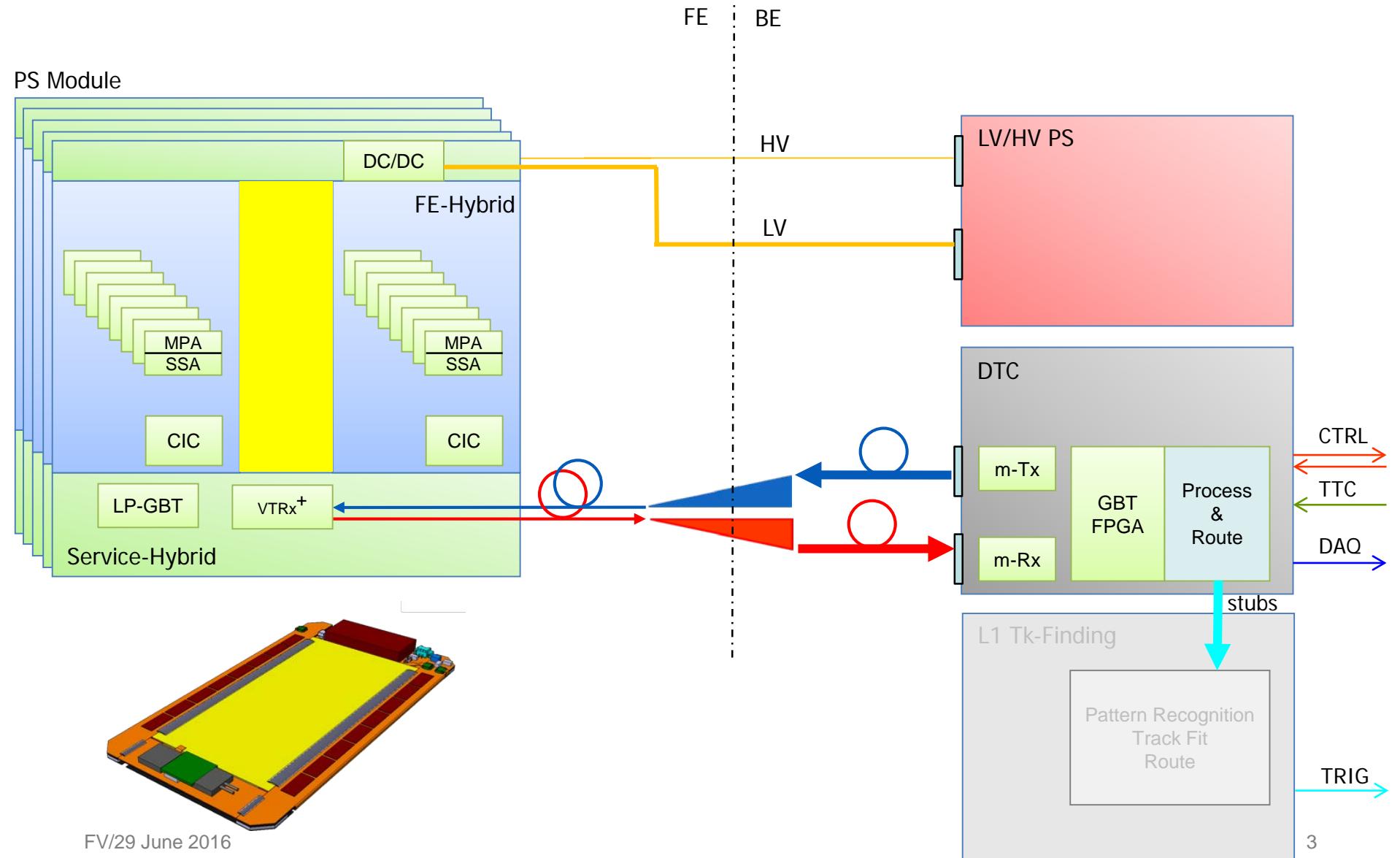
1. System Architecture
2. Front-End
3. Back-End
4. System Tests
5. Conclusions



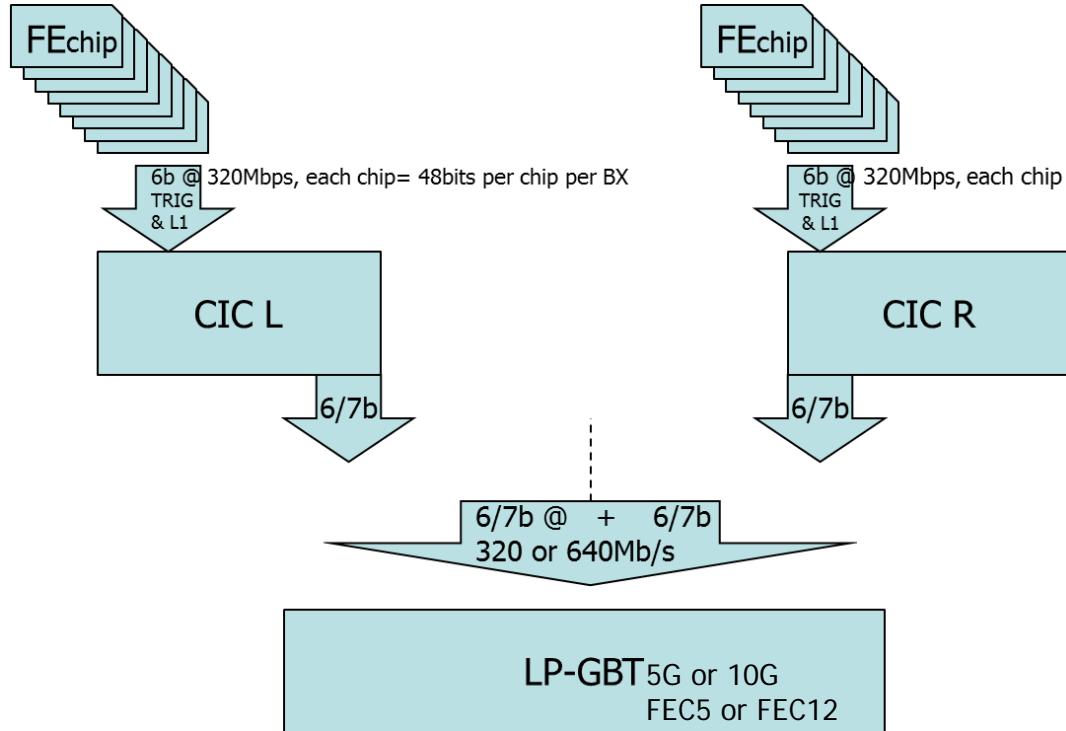
Electrical System Architecture: 2S



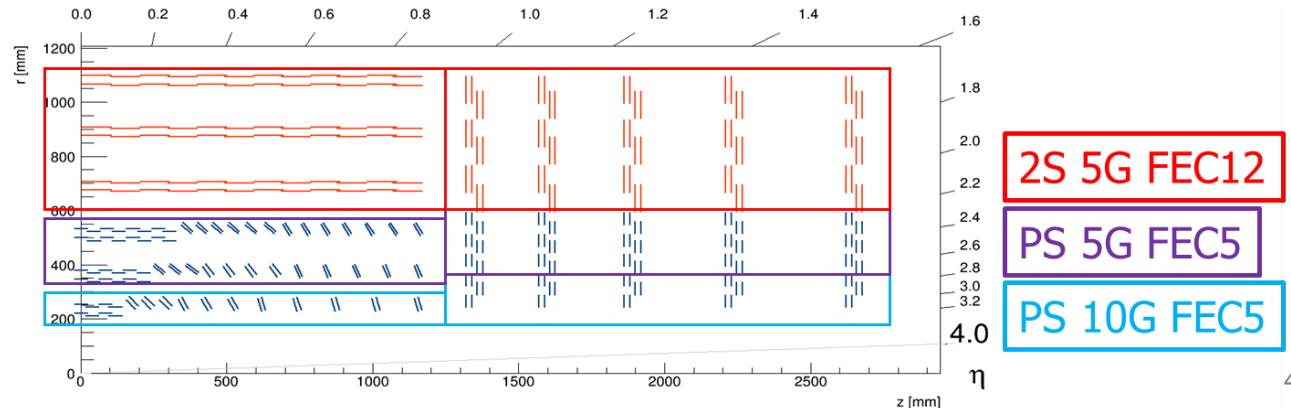
Electrical System Architecture: PS



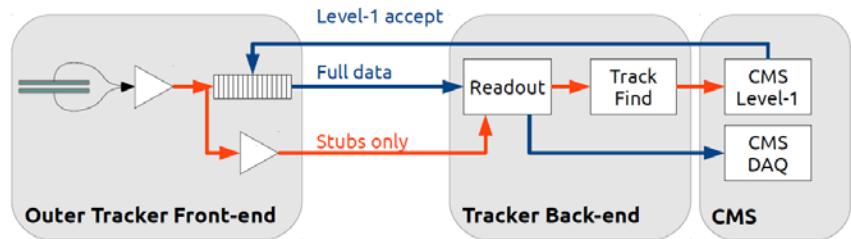
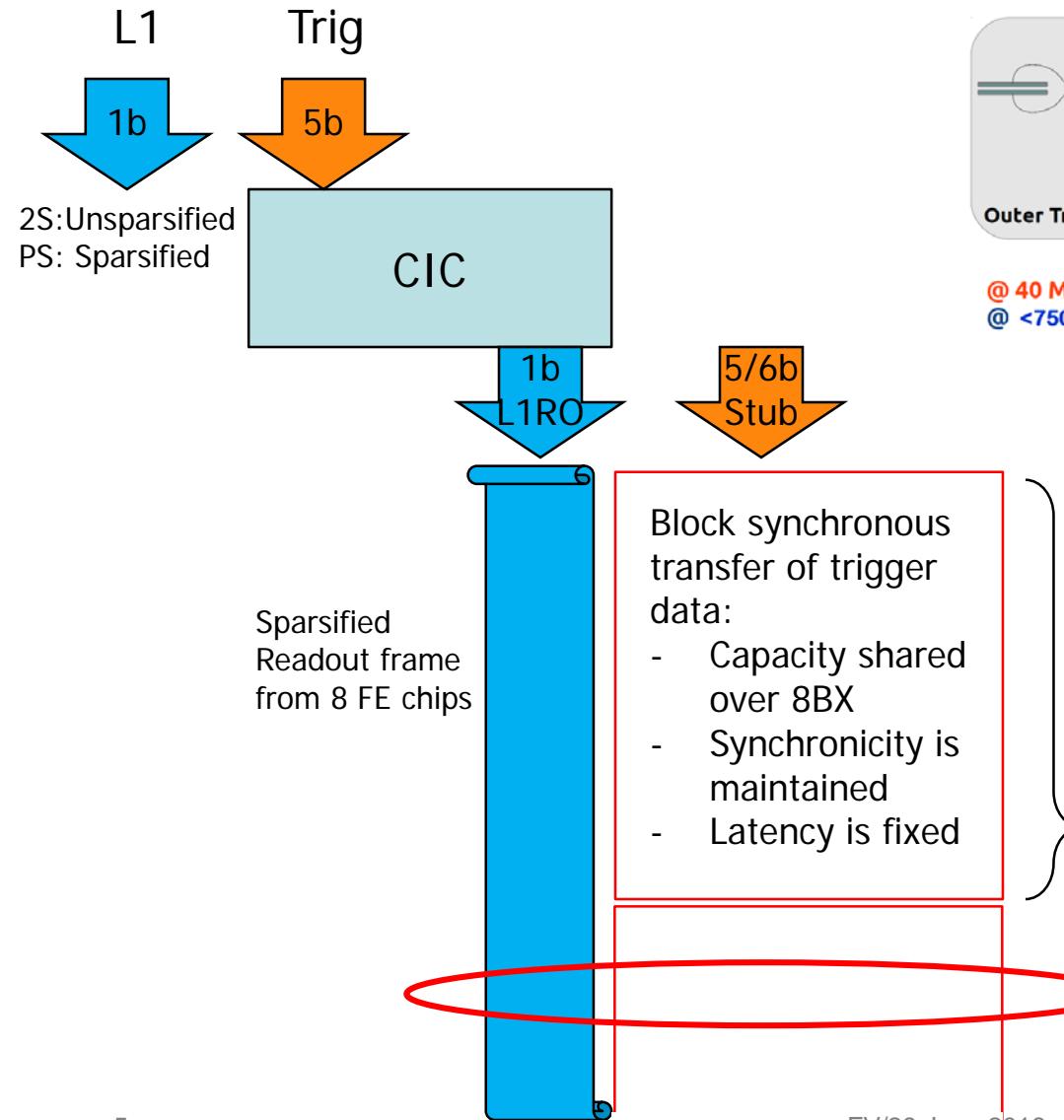
Data Aggregation Chain



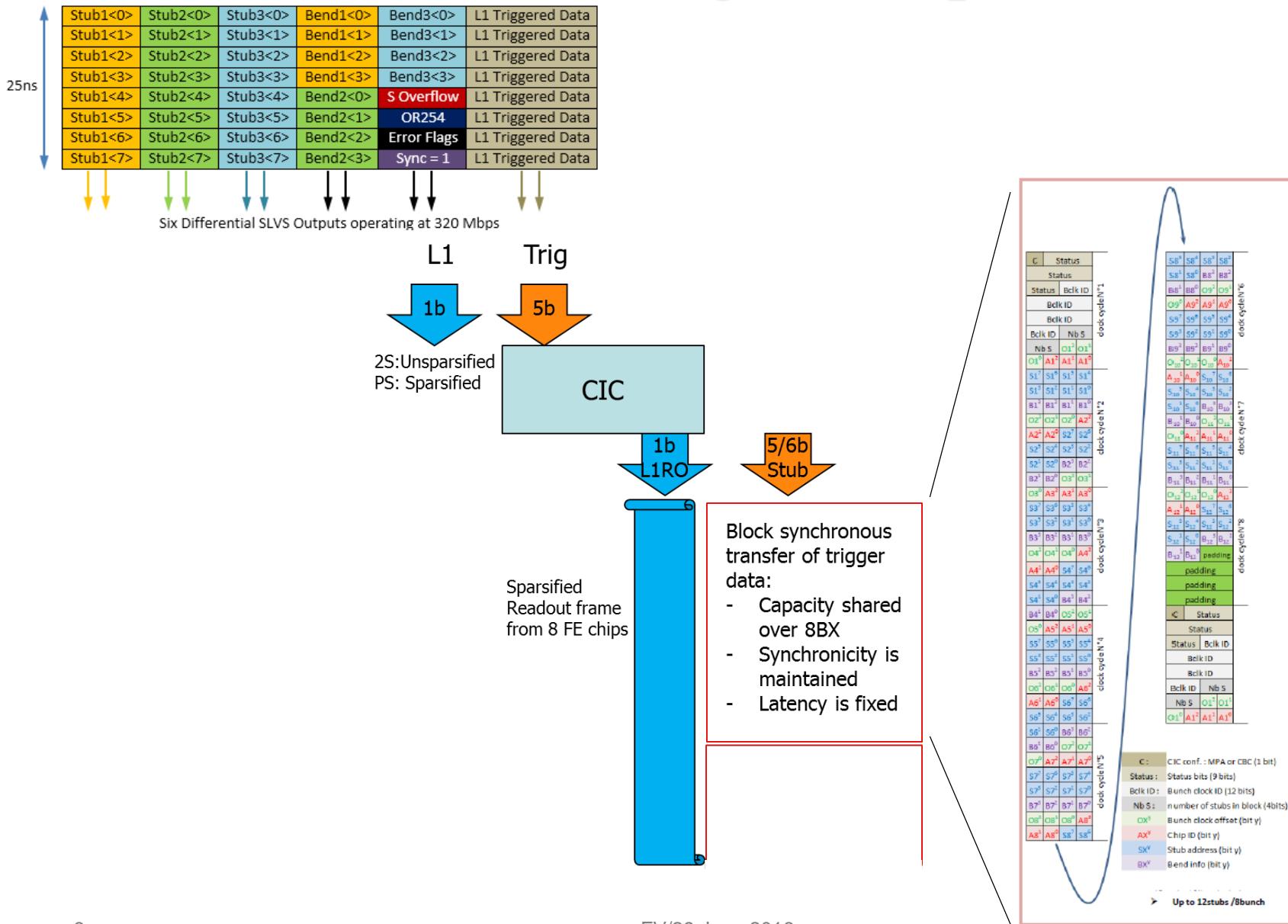
- Dual Data-Rate upstream: 5.12 Gbps or 10.24 Gbps
- FEC 5 or FEC 12
 - FEC 12 @5G: 96bits data field, 12 elinks @ 320Mbps
 - FEC 5 @ 5G: 112bits data field, 14 elinks @ 320Mbps
 - FEC 5 @ 10G: 224bits data field, 14 elinks @ 640Mbps



Data Formatting



Data Formatting Example (CBC case)



Data Formatting (reference)



I/O data formats for the Concentrator Integrated Circuit

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(1)- STFC - Rutherford Appleton Lab. (GB)

(2)-CERN

(3)- Imperial College Sci., Tech. & Med. (GB)

(4)-Institut de Physique Nucléaire de Lyon (FR)

Version 2.3

13/06/2016



Université Claude Bernard Lyon 1



https://espace.cern.ch/Tracker-Upgrade/Electronics/CIC/Shared%20Documents/Data%20formats/CIC_IO_Formats_V5.pdf

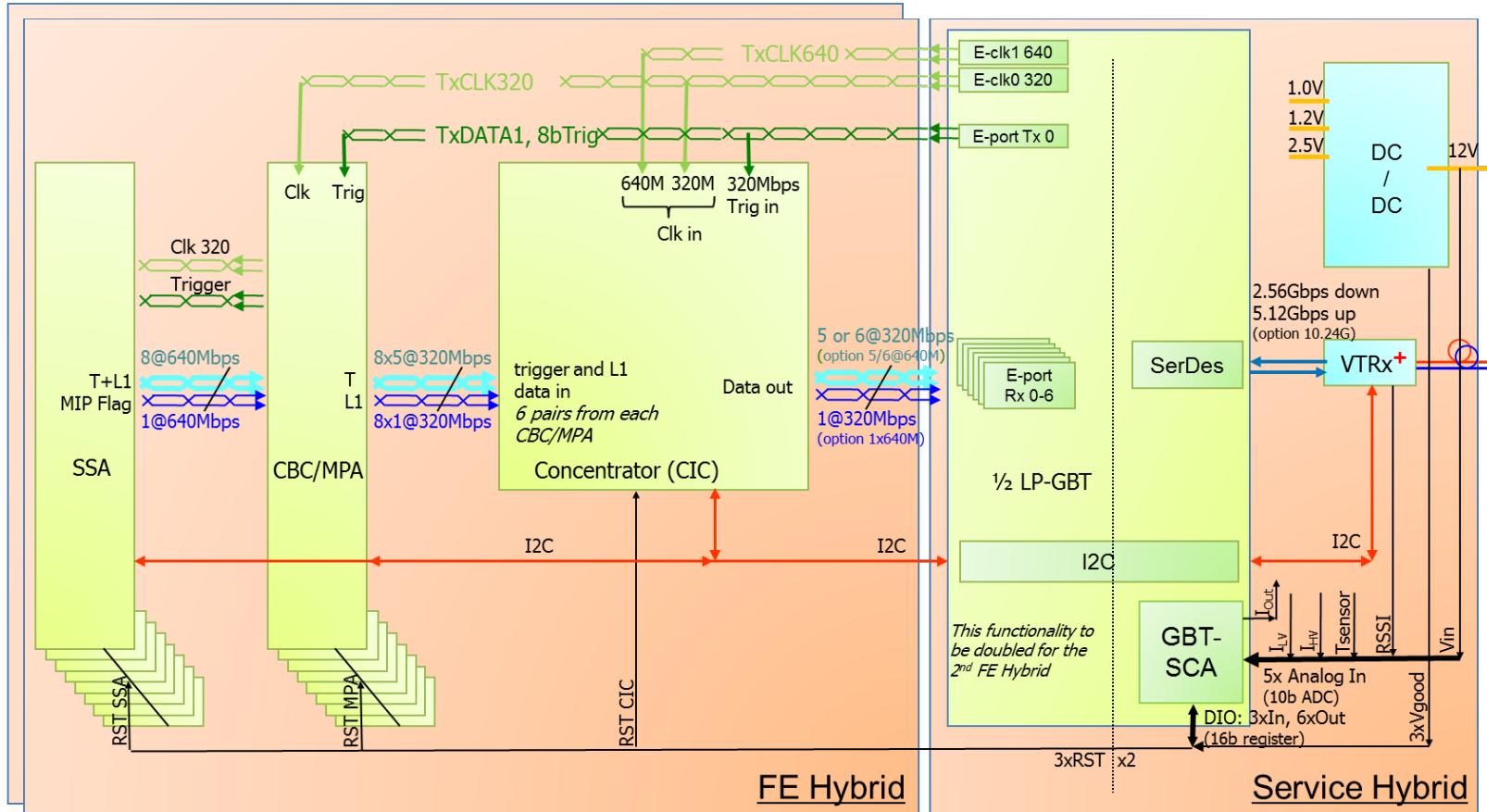
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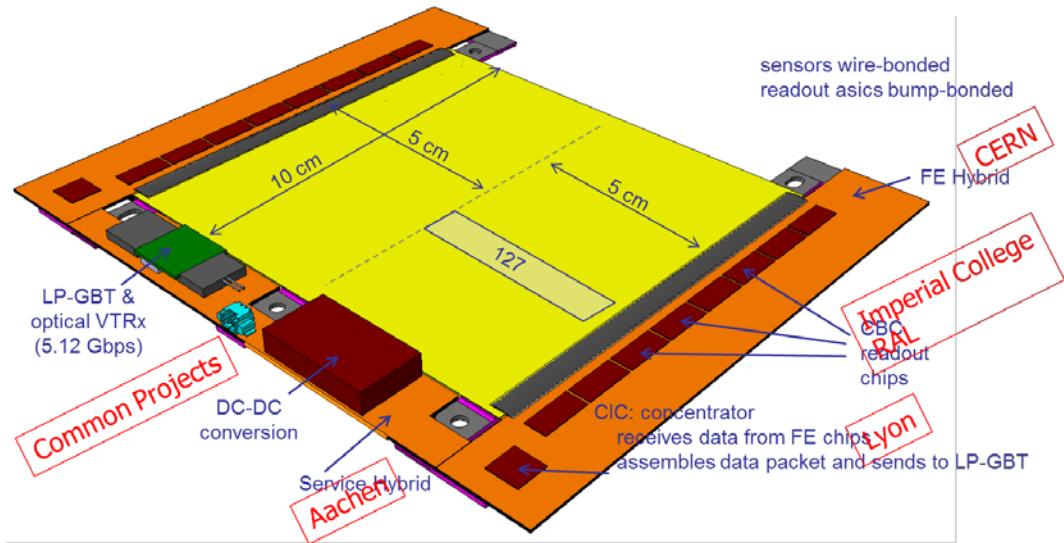
1. System Architecture
2. Front-End
3. Back-End
4. System Tests
5. Conclusions



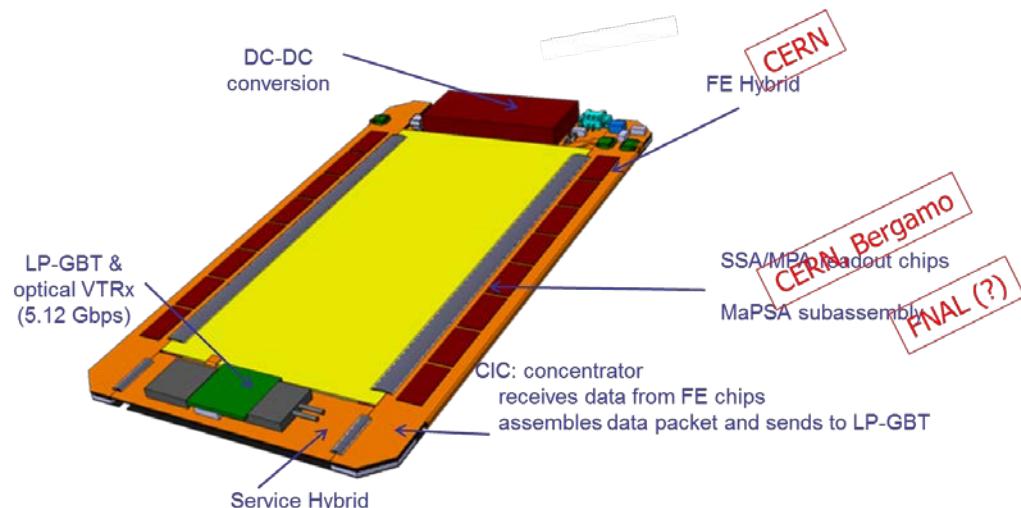
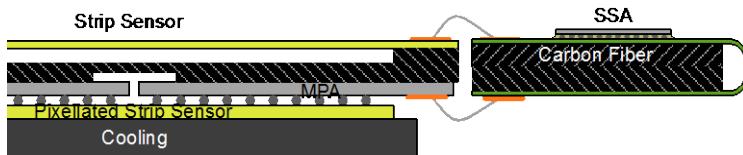
Front-End Block Diagram



2S module



PS module

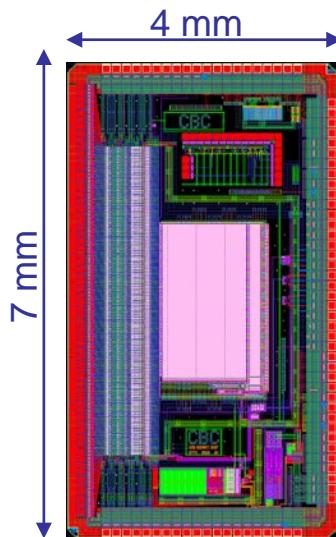


1. CBC Readout Chip Family

2 versions have been produced - both in 130nm CMOS

CBC1 (2011)

128 wire-bond pads, 50 μm pitch
front end designed for short strips, up to 5 cm
DC coupled, up to 1 μA leakage tolerant, both sensor polarities
binary unsparsified readout
pipeline length 6.4 μsec
no triggering features

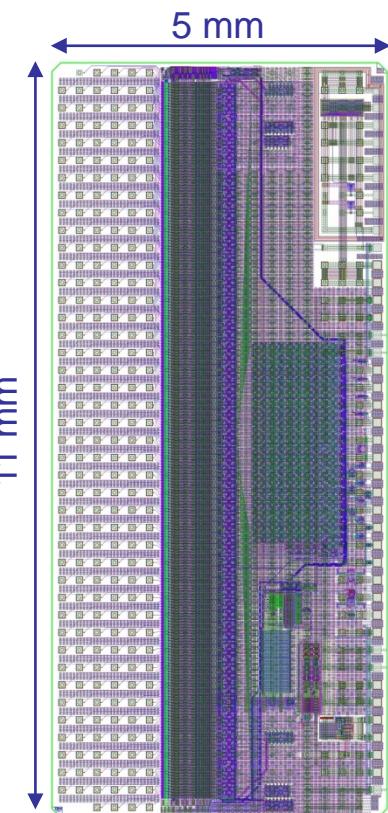


CBC1

CBC2 (January, 2013)

254 channels, 90 μm pitch
~same front end, pipeline, readout approach as CBC1
Rudimentary correlation and triggering features
plus

- bump-bond layout
 - C4 bump-bond layout, 250 μm pitch, 19 columns x 43 rows
 - includes triggering features
 - 30 interchip signals (15 in, 15 out), top and bottom



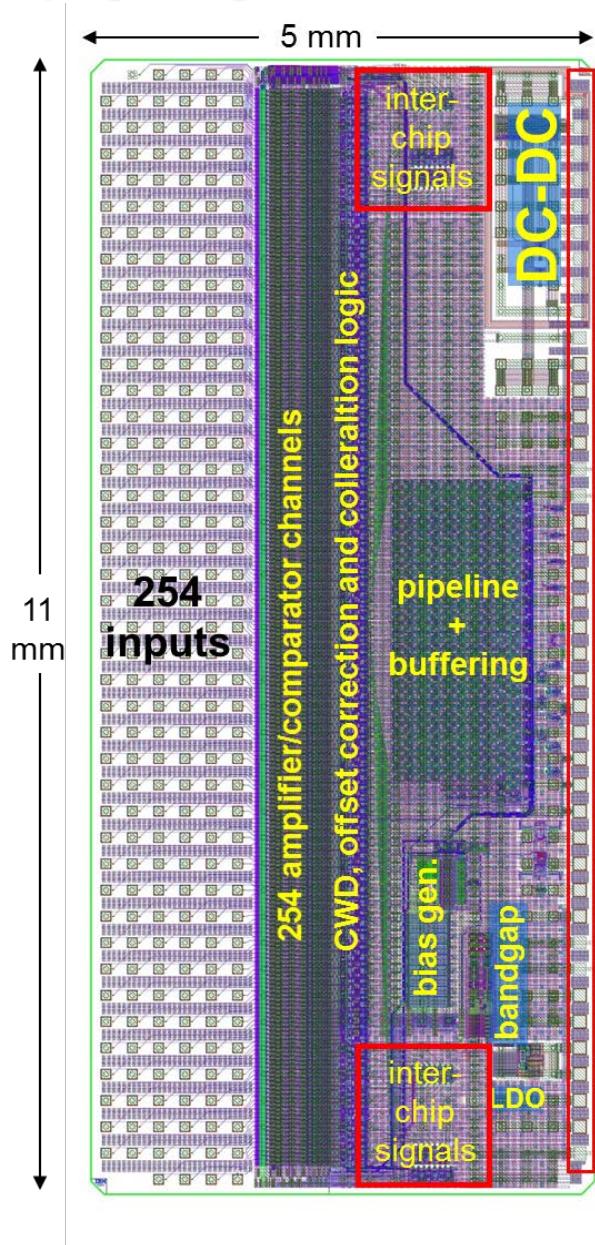
CBC2

CBC3 (in design, submission July 2016)

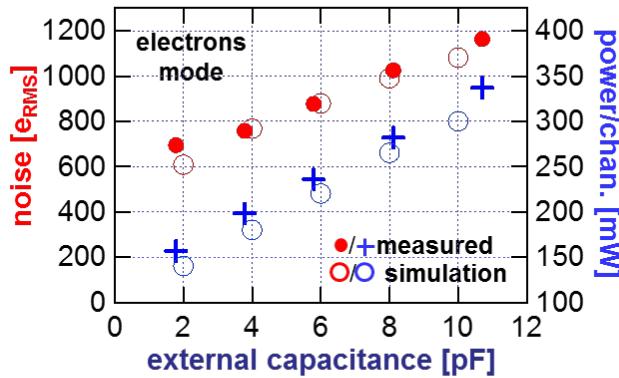
254 channels
front end optimized for 5cm strips (up to 8cm), n-polarity
Pipeline length 12.8 μsec , based on enclosed layout cell
plus

- Full correlation logic, 320Mbps digital interconnects

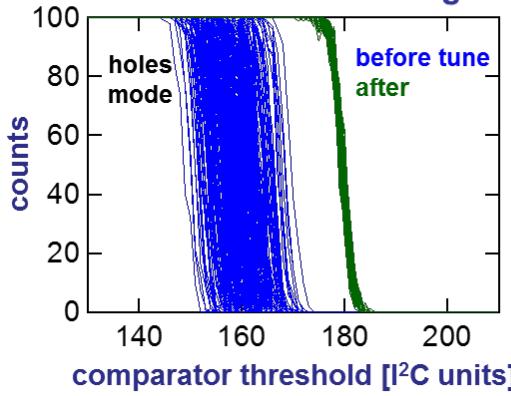
1. CBC2



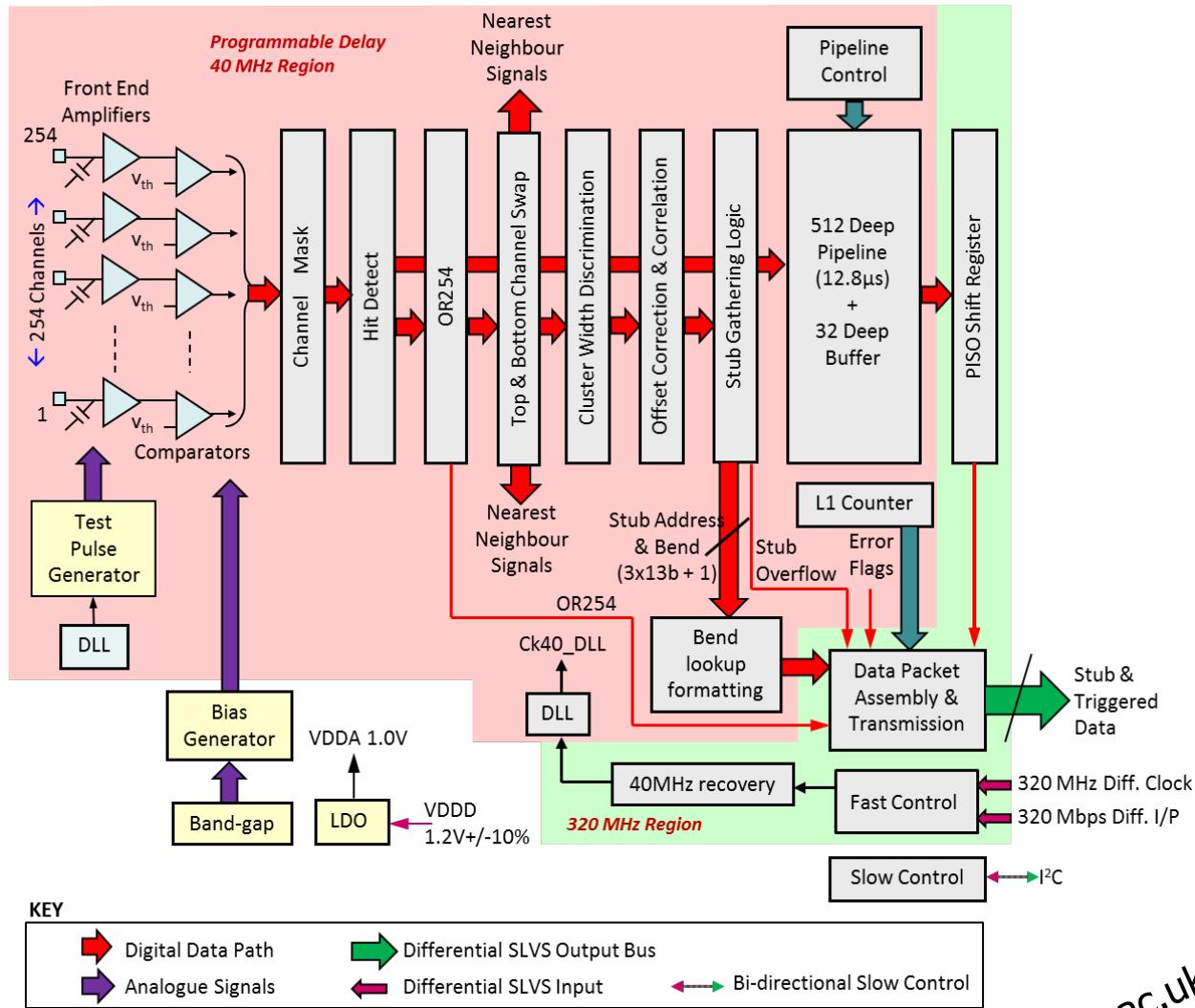
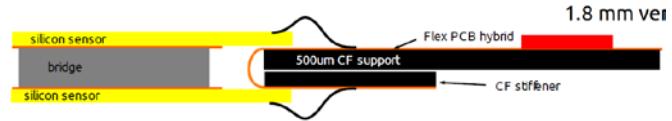
noise & power vs. external capacitance



channel offsets tuning

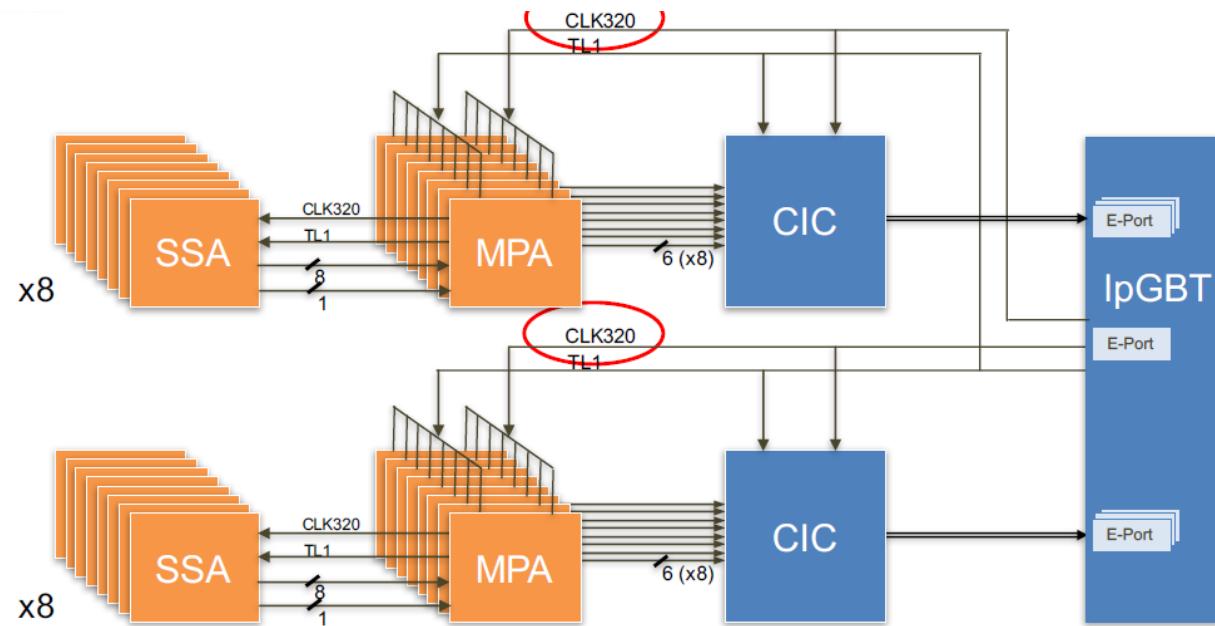


1. CBC3 Block Diagram



2. MPA-SSA-CIC

- 65nm CMOS
- ASICs are in design stage
- Digital system level modelling on-going
- Analog FE prototyped (MPA)



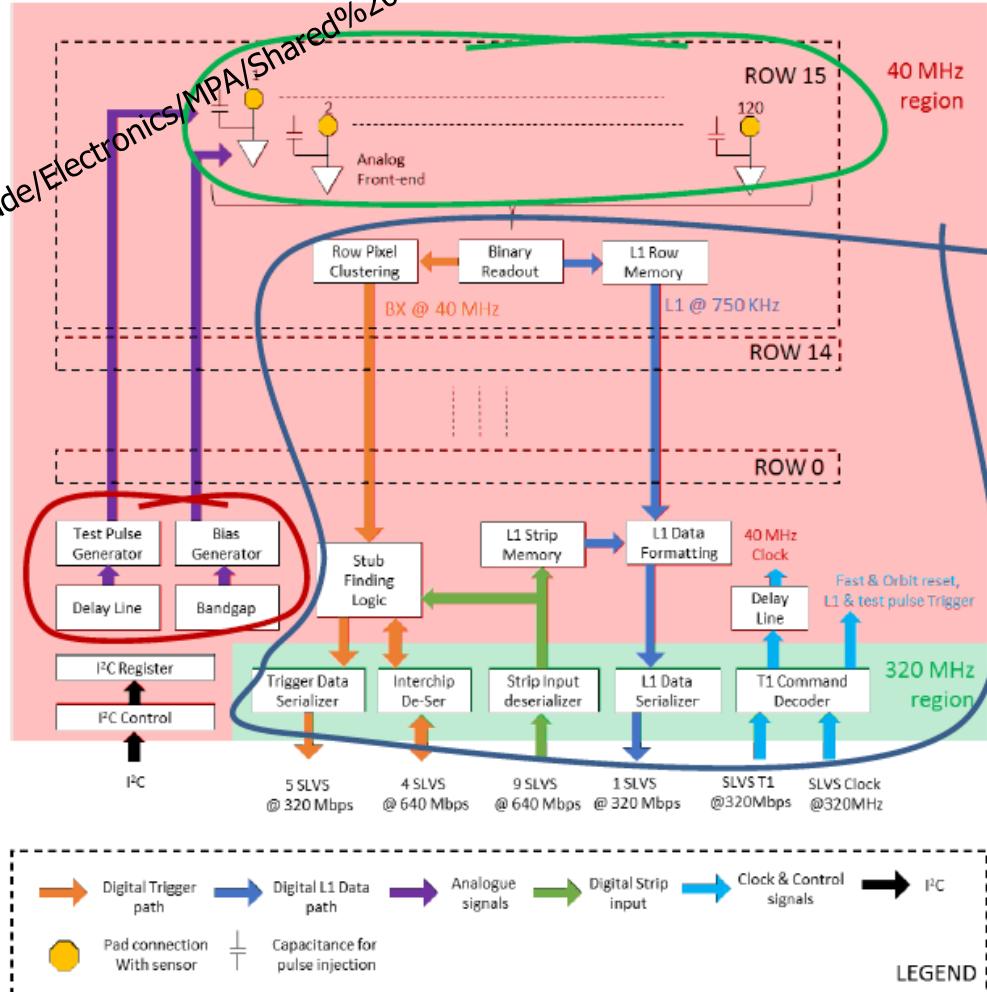
2. MPA Status

https://espace.cern.ch/Tracker-Upgrade/Electronics/MPA/Shared%20Documents/Specifications/MPA_Specs_v1_0.pdf

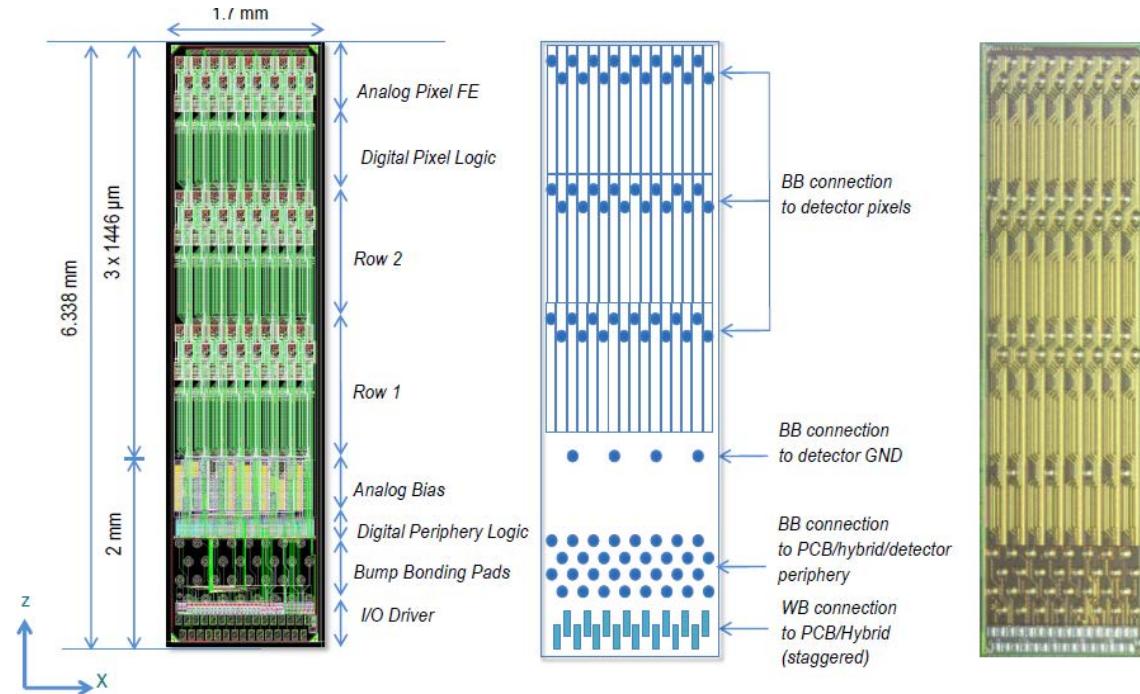
Analog FE from MPA-Light

Bias structure
Schematics ready

RTL model
Fully verified
(1 MPA)



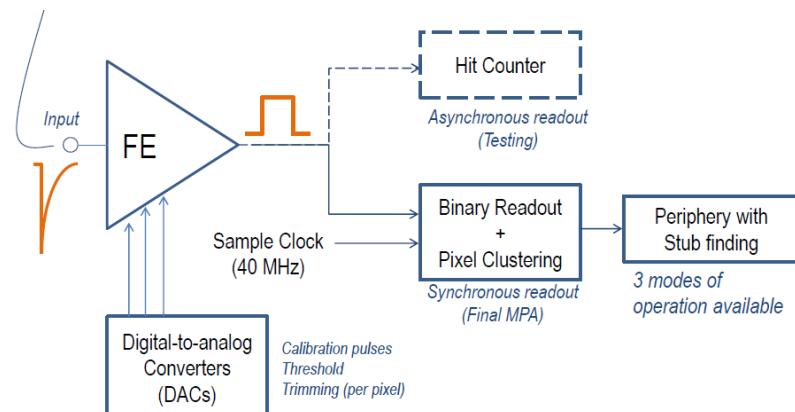
2.MPA-Light Mini-ASIC



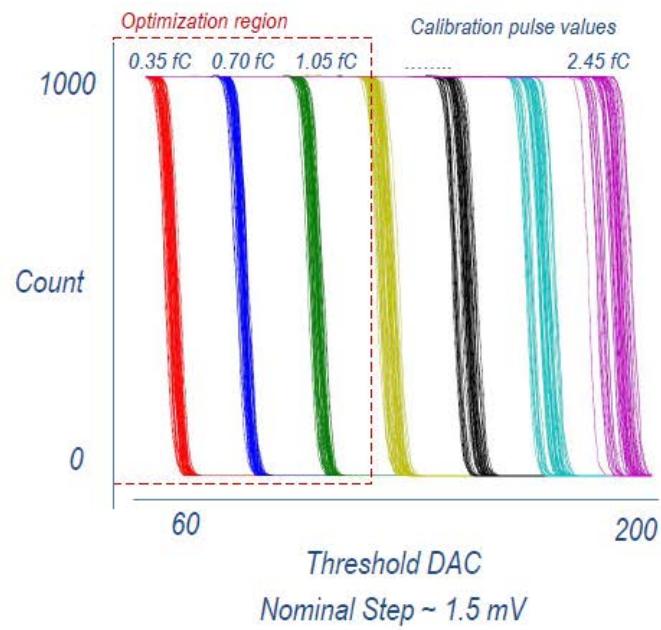
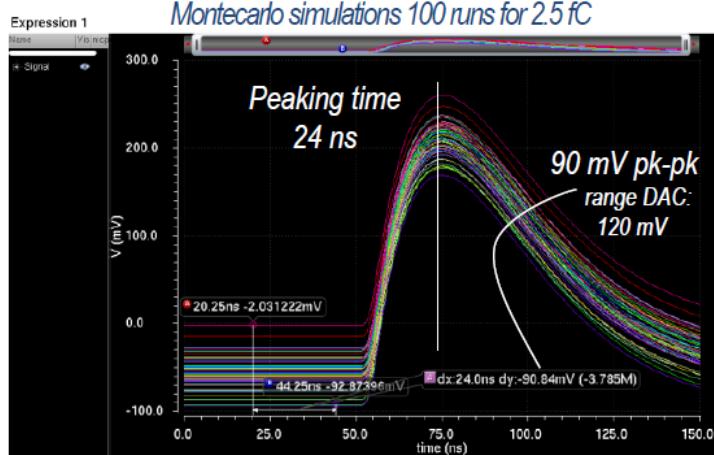
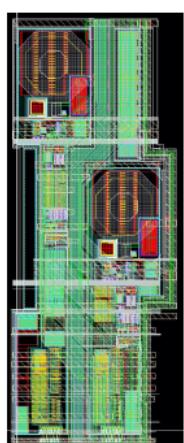
prototype version produced – 65nm CMOS

2015

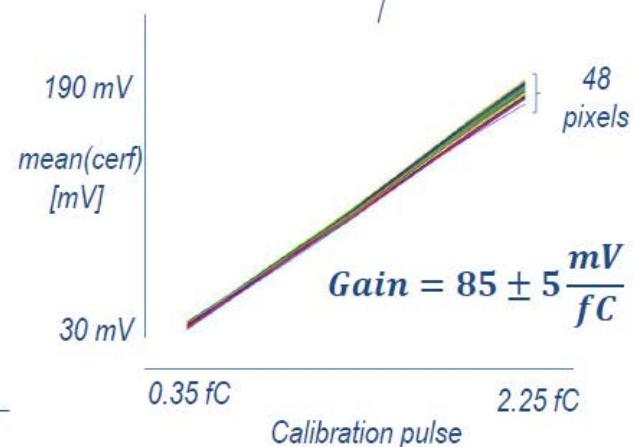
- 3x16 pixels (instead of 16x120)
- Analog pixel cell identical to final MPA one
- Rudimentary digital logic
- Possibility to daisy chain chips
- Possibility to emulate strip



2. MPA-Light Test Results

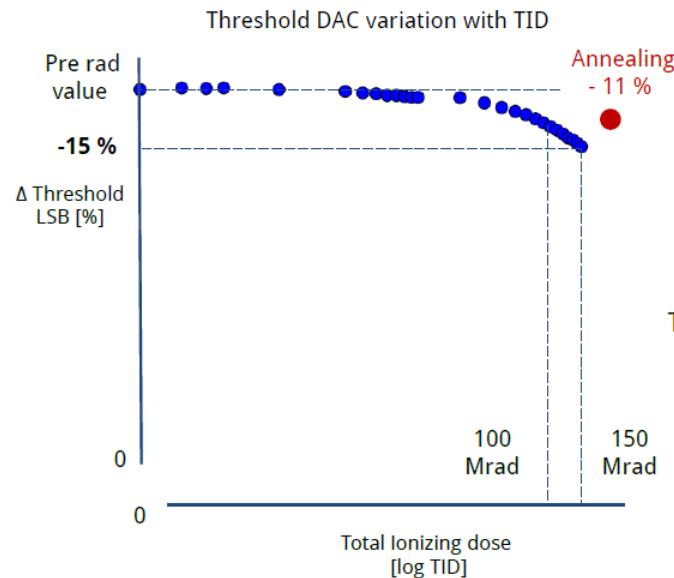


For every pixel, the gain is extracted with the complementary error function fitting



2. MPA-Light Radiation Test Results (1/2)

Analog FE characterization



The largest variation due to TID is observed on the threshold DAC.
The variation **can be compensated** thanks to the DAC range

Drift of discriminator offset

- Need of re-trimming after irradiation



Calibration DAC step variation is < 10 %

Analog power consumption decreased

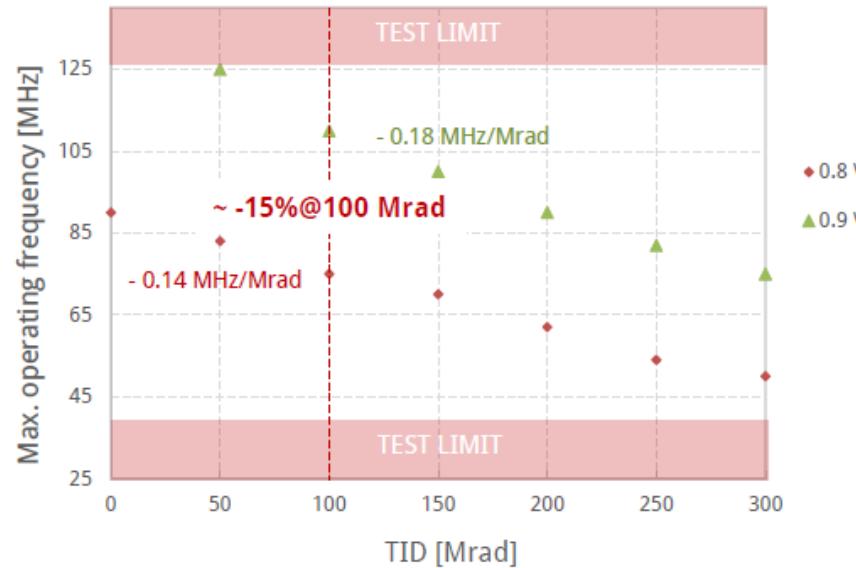
- - 7 % after 150 Mrad
- - 4 % after Annealing
- Digital power consumptions variation is negligible

Digital Pass/Fail checks do not show any fail at nominal condition (1.2 V, 40 MHz)

2. MPA-Light Radiation Test Results (2/2)

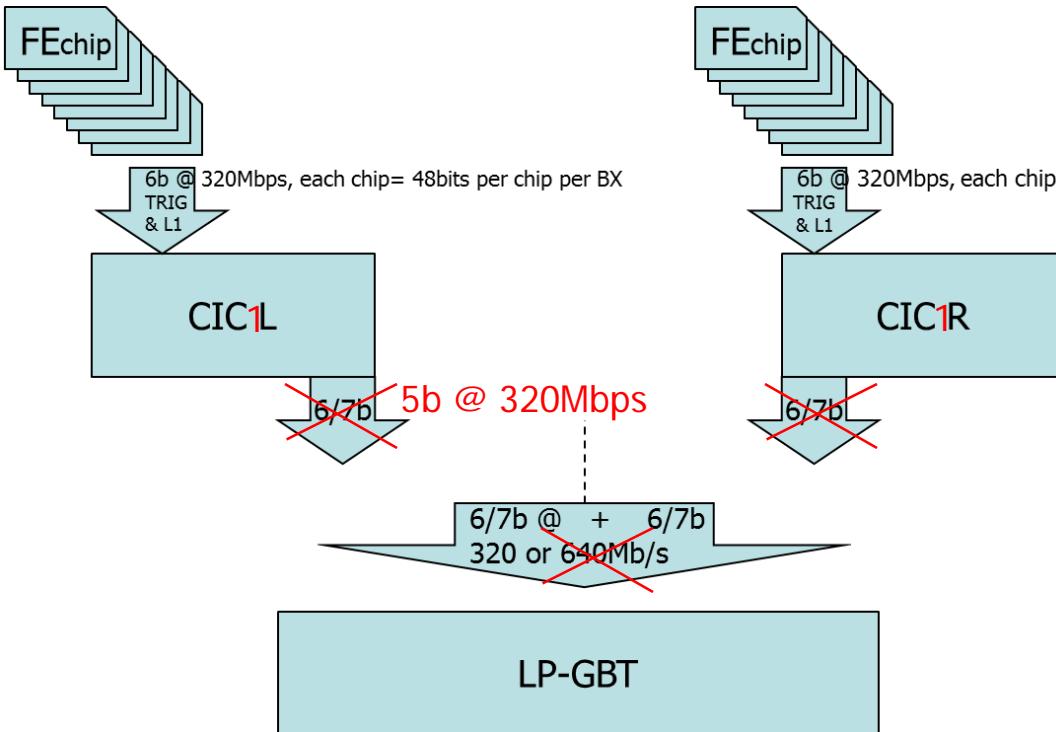
Digital characterization

We observe a **linear degradation** of the frequency between 0 and 300 Mrad



The effect is related with **short channel** in the periphery logic.
This is the dominant effect in standard cell logic.

3. CIC1



→ Raw data (L1) block:

- Full raw data transmission up to **750kHz (max acceptable L1A rate)**
 - No loss accepted (**<0.1%**)
- #### → Trigger block:
- Full trigger data (**stubs**) transmission up to **40MHz**
 - Small loss (~1%) in the innermost region for good stubs (i.e. coming from particles with $p_t > 2\text{GeV}$ and $d_0 < 5\text{mm}$)

➔ Documentation available on the sharepoint:

→ Analyse of the potential data transmission losses:

https://espace.cern.ch/Tracker-Upgrade/Electronics/CIC/Shared%20Documents/Simulation%20studies/FE_inneff_2.pdf

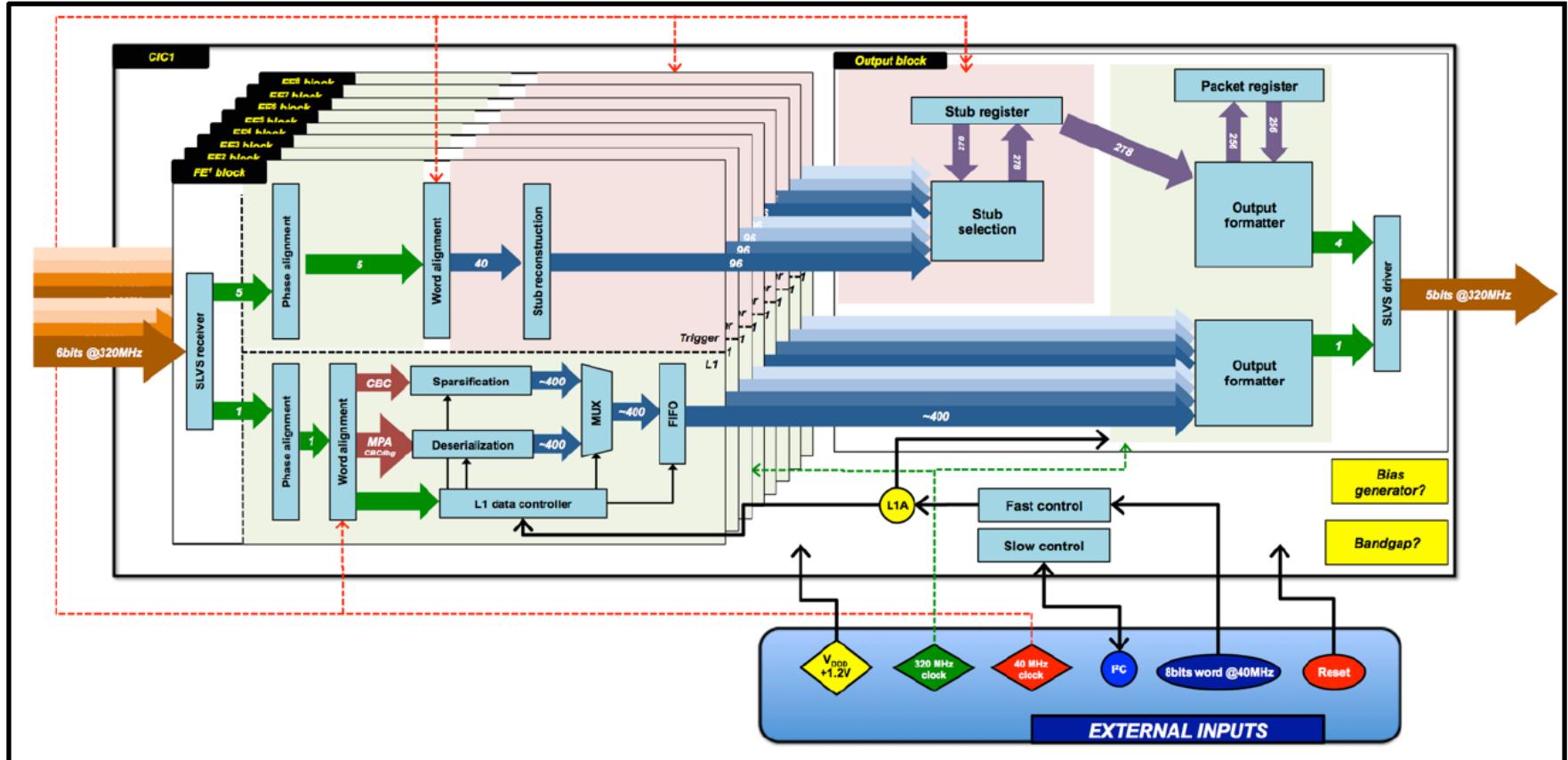
→ CIC I/O data formats:

https://espace.cern.ch/Tracker-Upgrade/Electronics/CIC/Shared%20Documents/Data%20formats/CIC_IO_Formats_v4.pdf

→ CIC1 specification document:

https://espace.cern.ch/Tracker-Upgrade/Electronics/CIC/Shared%20Documents/Specifications/CIC_specs_v1.1.pdf

3. CIC1 Block Diagram

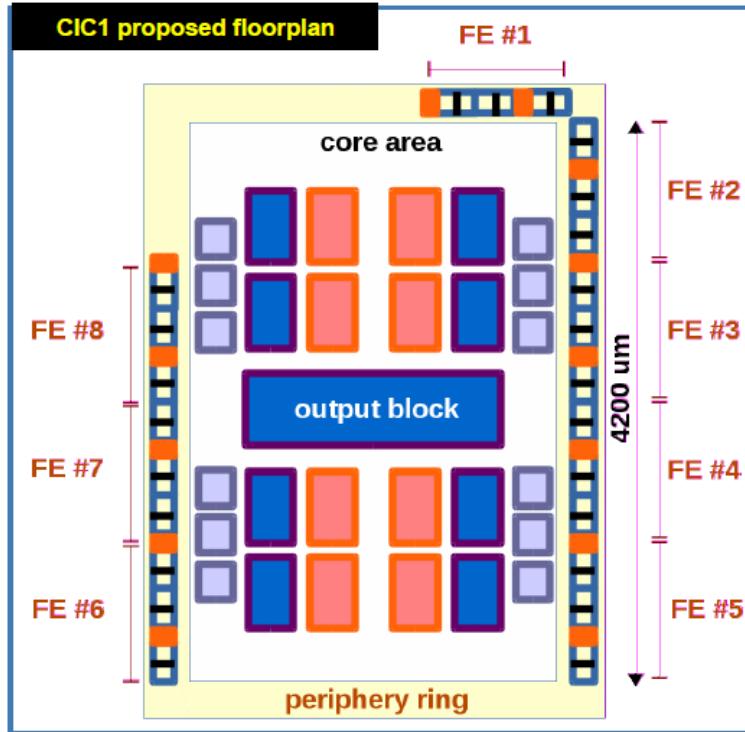


→ Two main parts:

- The **FE block**: receives and process the data from 1 FE chip
- The **output block**: merge the info and prepare the final packet

→ Verilog model of the complete system now done and tested

3. CIC1 Status

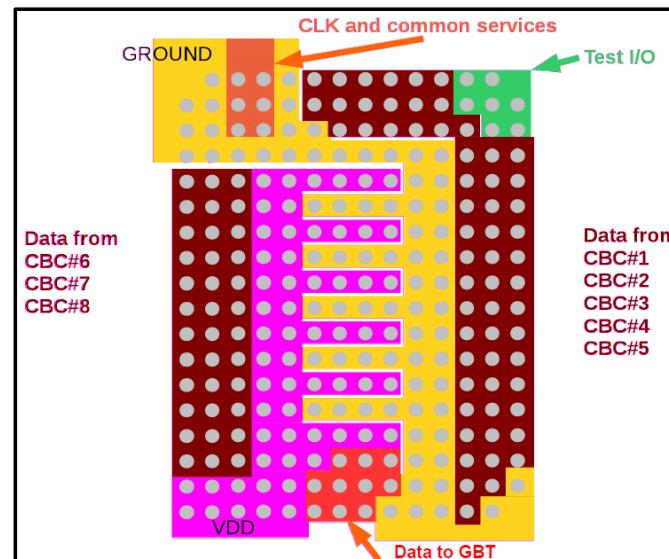


→ Synthesis of 1FE block (core+*FIFO*) successfully completed (*now need to test it*). Next steps will be implementation of the triplication.

→ Started the reflexion about blocks placement and routing

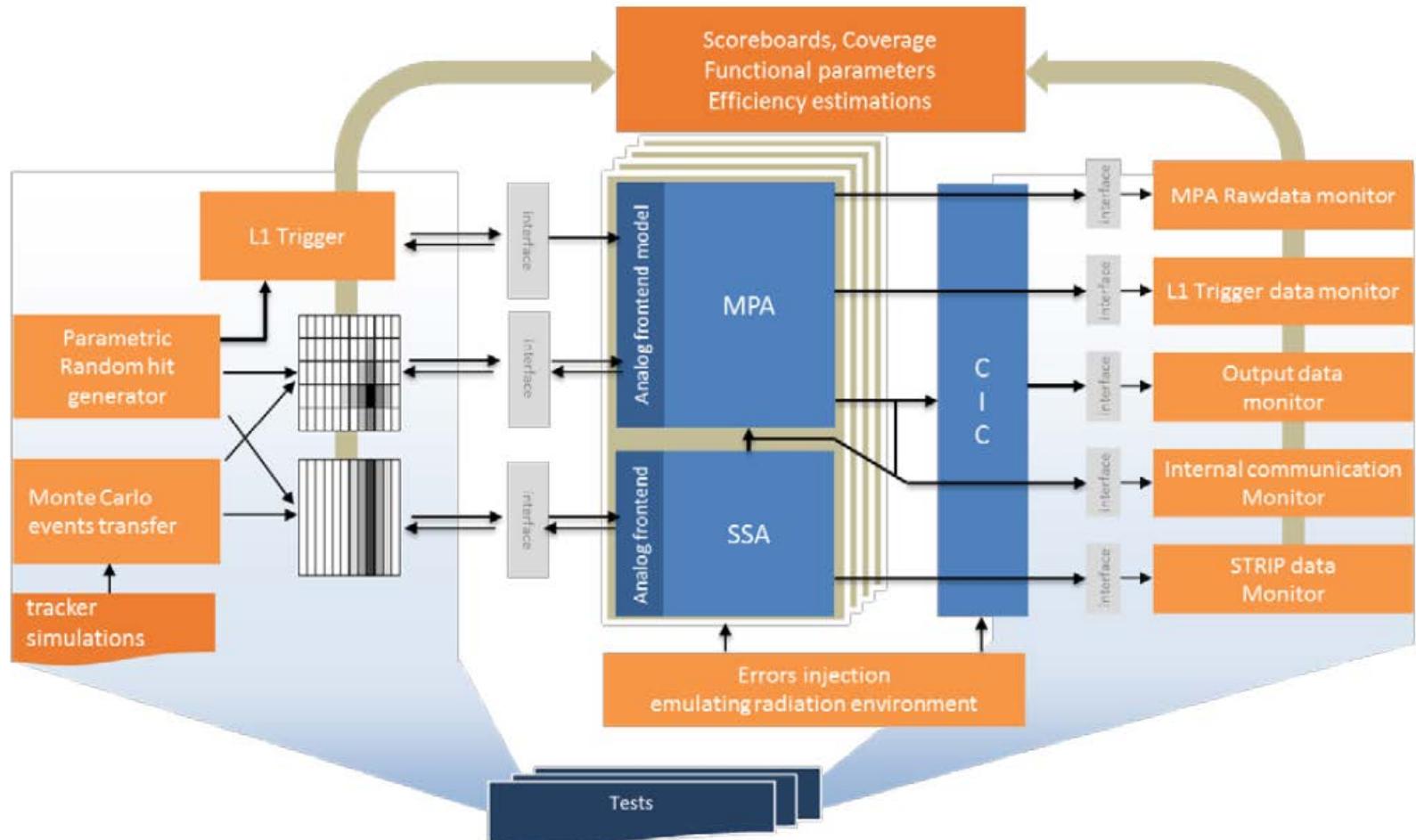
→ First estimation of the power dissipation was done: **25mW for 1 complete FE block (incl. sLVS and phase aligner)**

→ Floorplan proposal now in hands of hybrid designers for feedback.



4. SSA, MPA and CIC Simulation Framework

- Single MPA fully verified
- PS Module simulation ready (8 MPA + 8 SSA)
- CIC model received (by Y. Zoccarato)



4. SSA, MPA and CIC1 roadmap towards submission

CIC1 (submission Q4-16, MPW run):

RTL code completion

Architectural review

Physical implementation

MPA (submission Q1-17, engineering run):

Verification with System-Level framework

Architectural review

Physical implementation

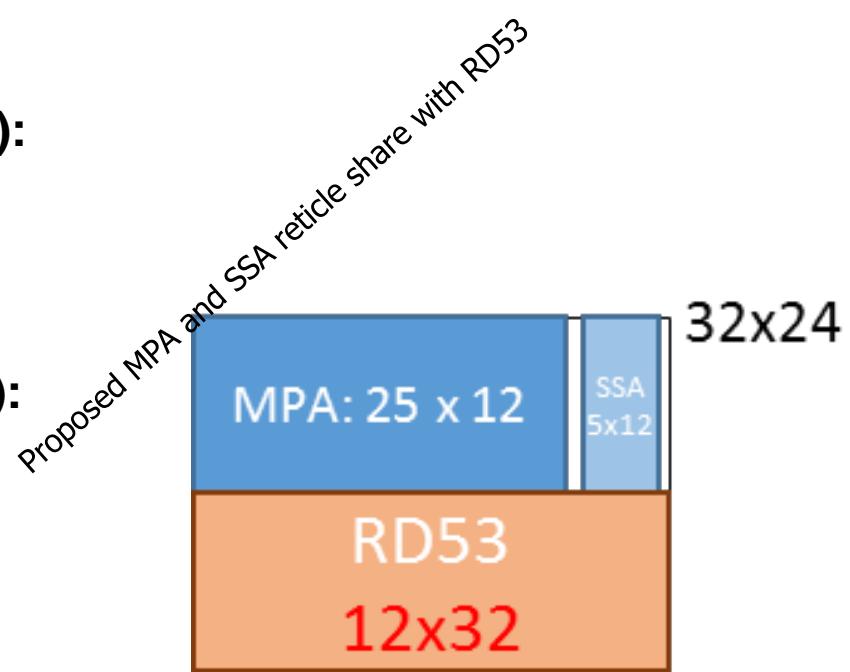
SSA (submission Q1-17, engineering run):

Analog Front-End completion

RTL code development

Architectural review

Physical implementation

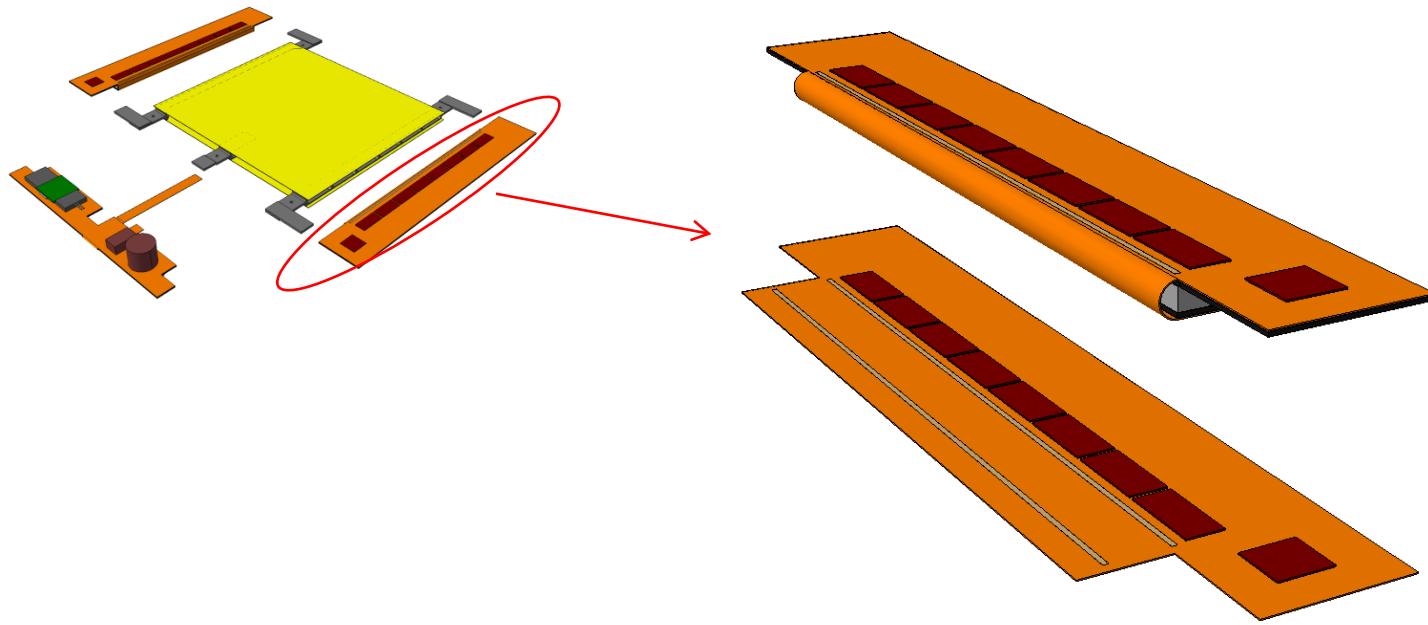


Common

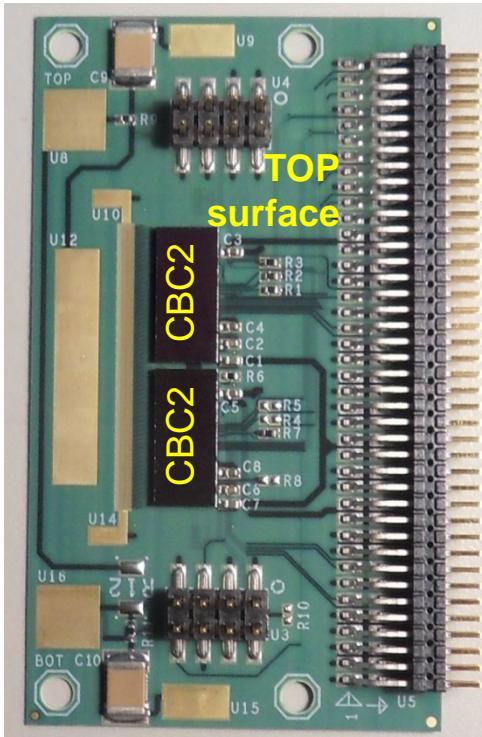
System-Level integration framework

Chip-level testability

5. Front-End Hybrid (FEH) Developments

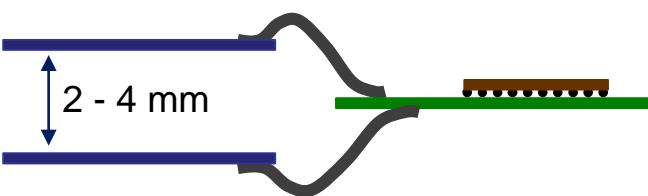


5. 2xCBC2 prototype

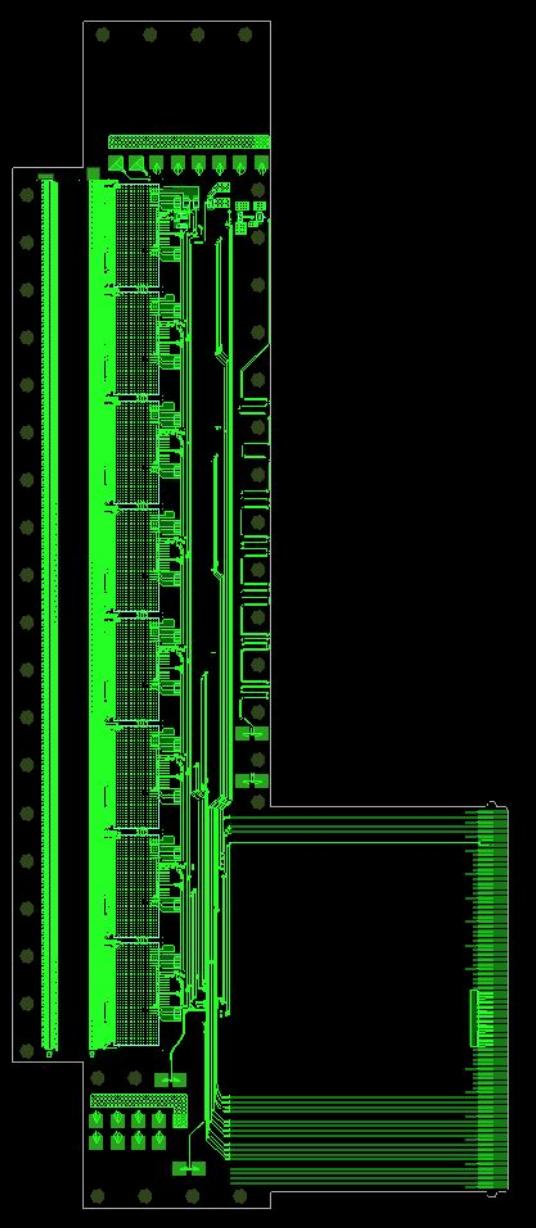


2 chips prototype - available since mid 2013

- 6 layer “rigid” technology - (actually quite flexible - 265 μm thick)
- For chip testing and mini-module assembly
- fully functional, but flexibility and thickness causes bonding problems when constructing modules

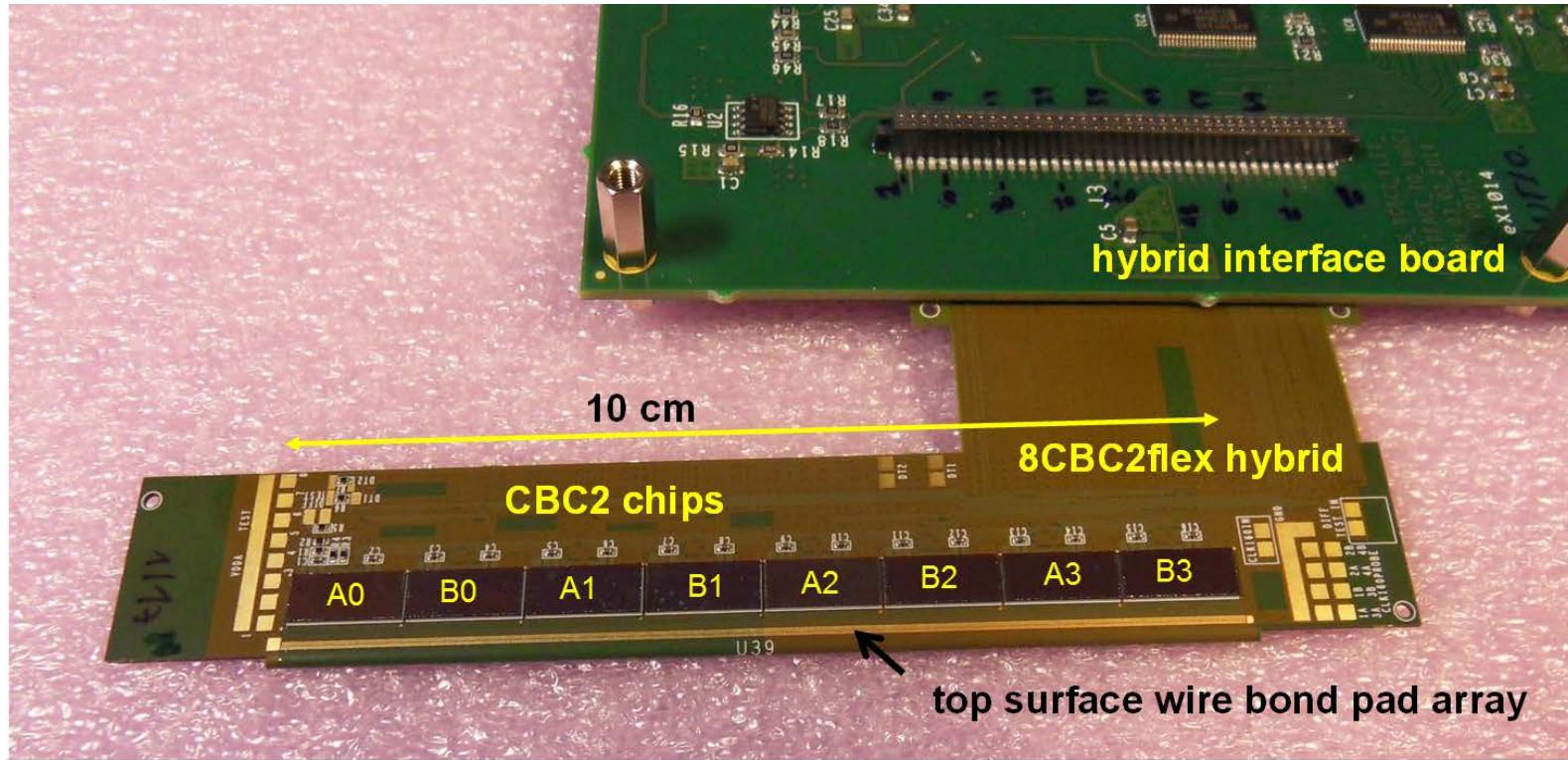


5. 2S FEH (1/2)

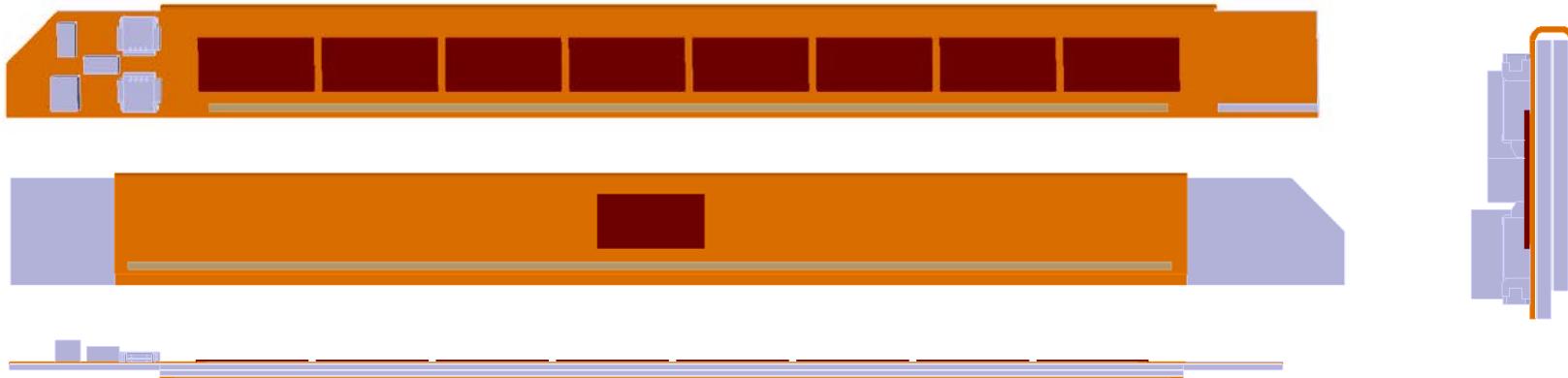
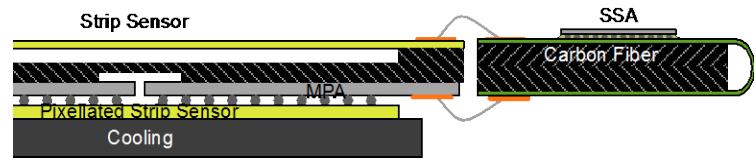


- **The 8CBC2Flex is a full 8 CBC2 readout system.**
 - 4 layers, 150 μ m thick
 - One 40 MHz clock input.
 - All chips configured separately through a common I2C bus.
 - All chips are powered at 1.25V.
- **Common back end signals to control the readout:**
 - Reset, Clock 40, I2C bus.
- **Paired control signals:**
 - Fast reset, I2C refresh, T1Trig, Test Pulse.
- **All readout signals are handled per chip:**
 - Trigger and Data lines.
- **All signals are brought to a FPC connector.**
 - No concentrator

5. 2S FEH (2/2)

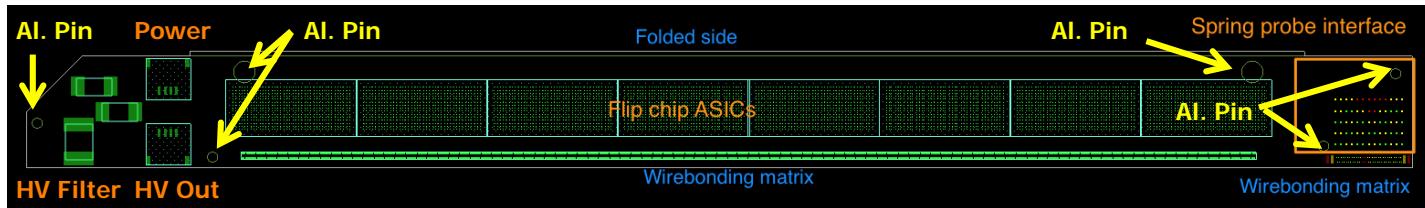


5. PS FEH Mockup

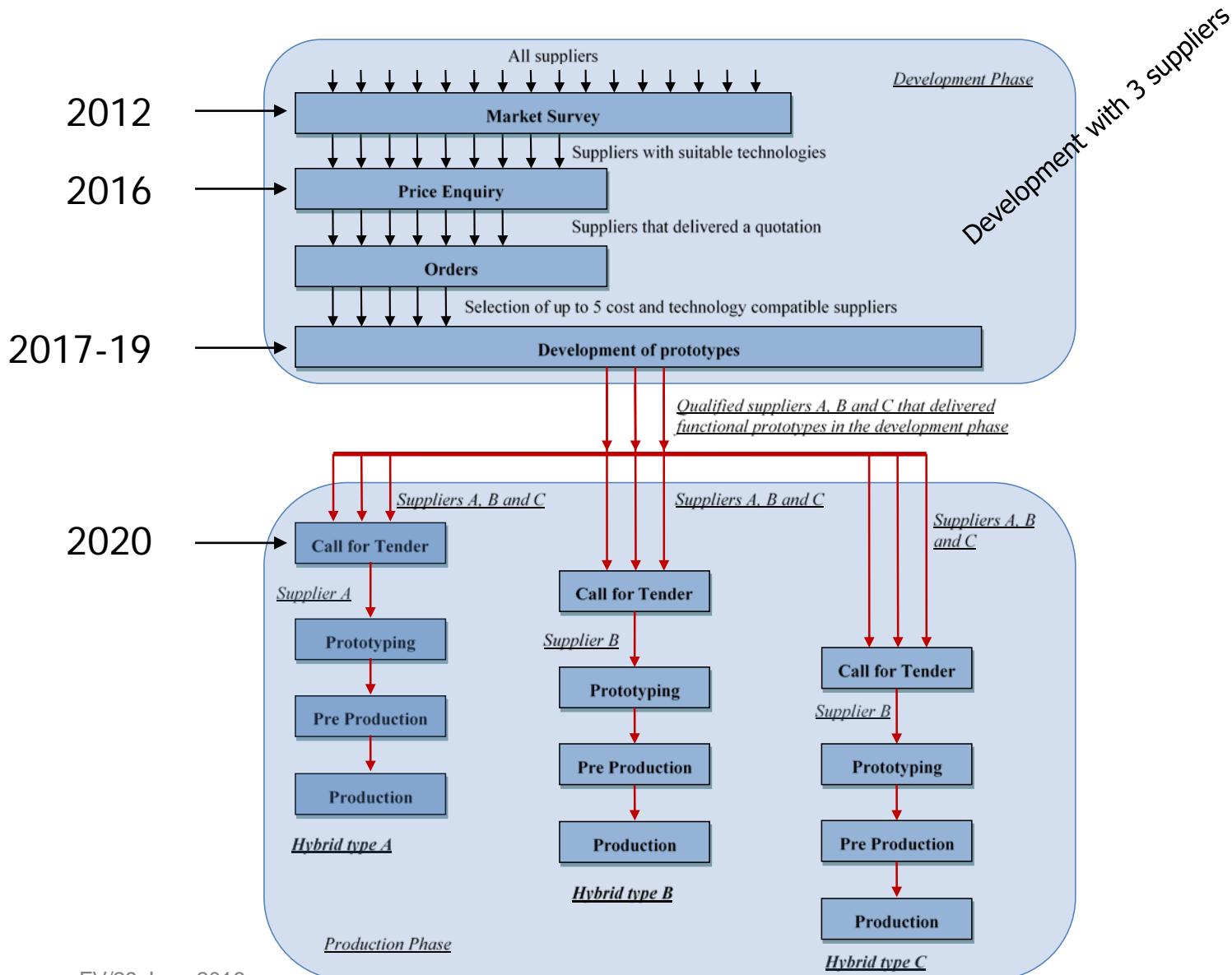


- **A baseline circuit has been drafted:**

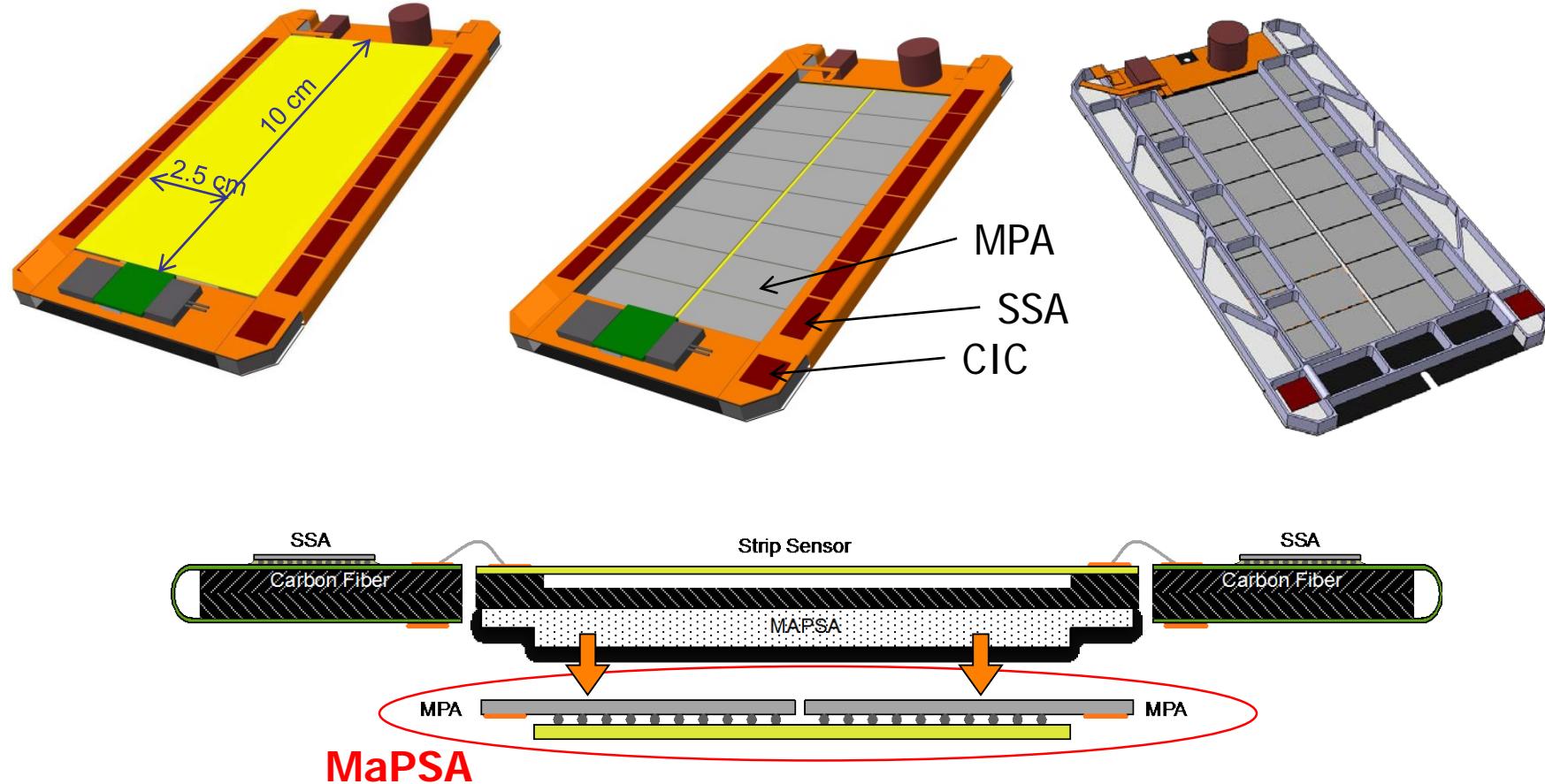
- Outline of the folded circuit to enable discussions with test probe suppliers.
- SSA and CIC footprint is the one of the CBC2, will be adjusted later.
 - SSA and MPA due Q2-2017
- Power and HV connectors placed, but we are still missing the input HV connection.
- Alignment holes for folding and electrical test socket
- Test probe interface proposal next to OPTO Service Hybrid wirebond interface.



5. FEH Development Roadmap

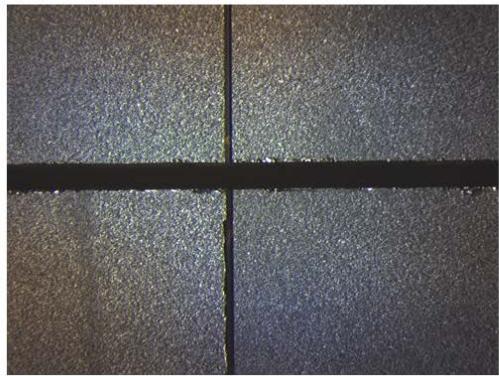


6. PS Macro Pixel SubAssembly (MaPSA)

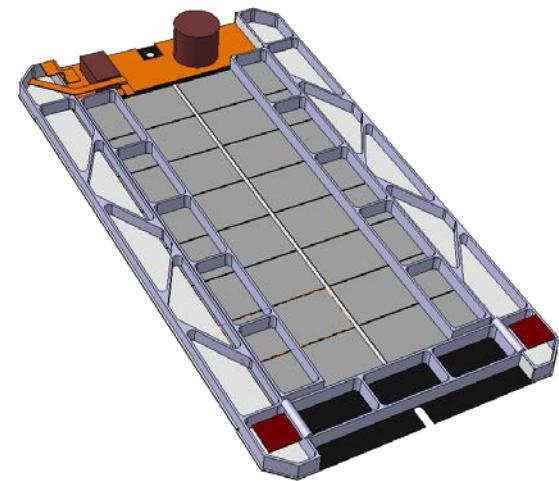
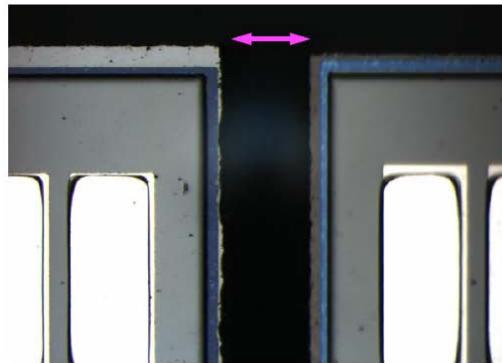


6. MaPSA

Typical inter-chip gaps:



Worst case edge alignment:



Full size mockup

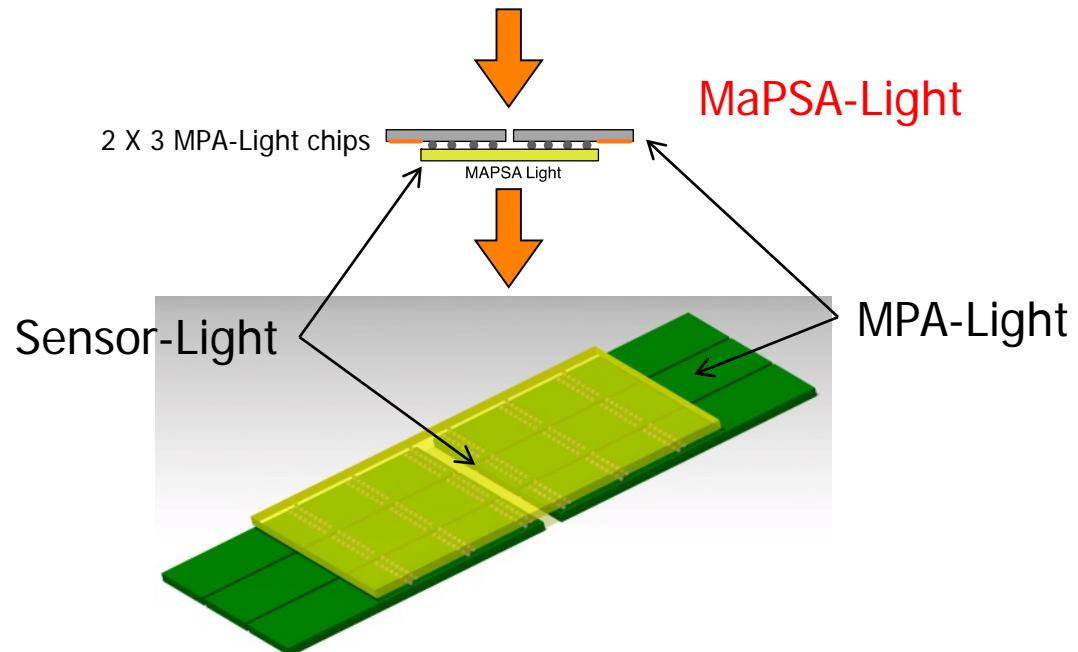
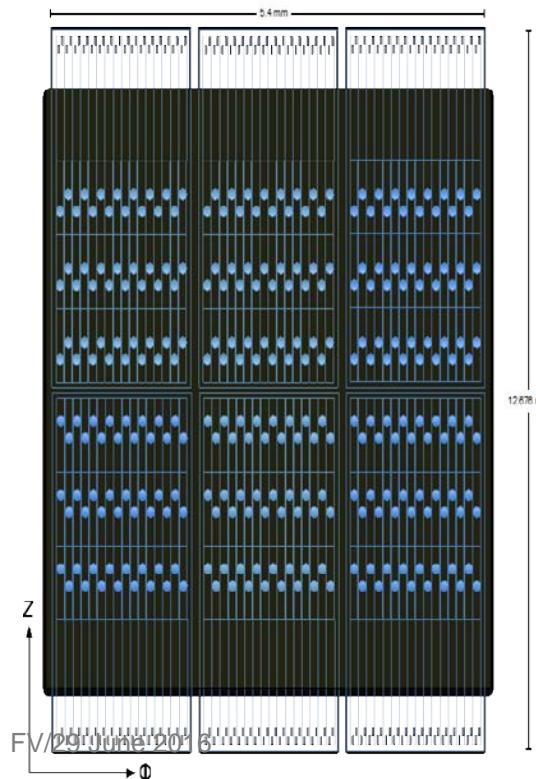


6. MaPSA-Light Development

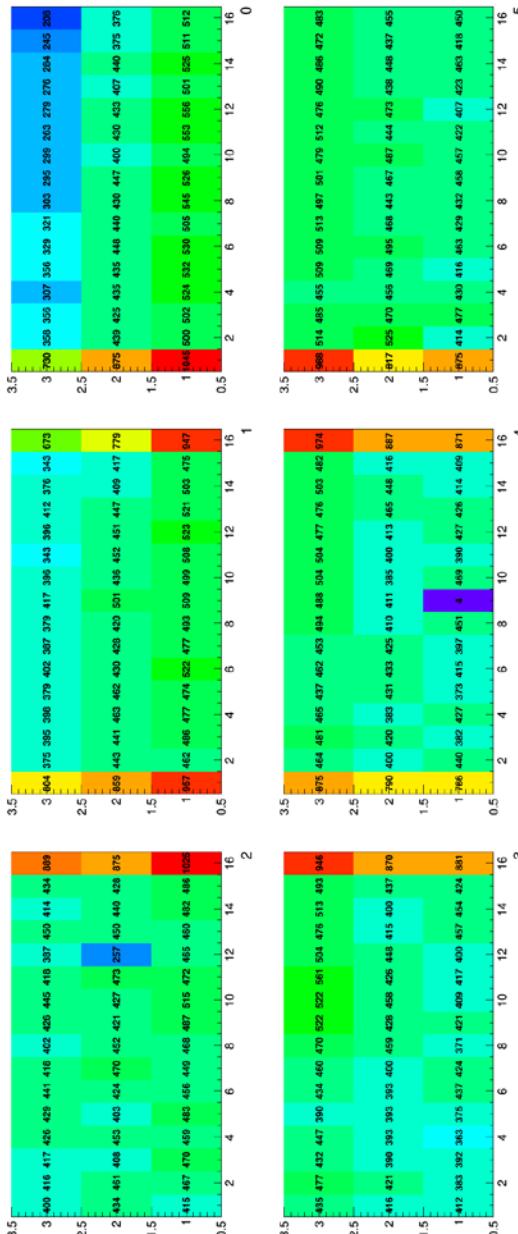
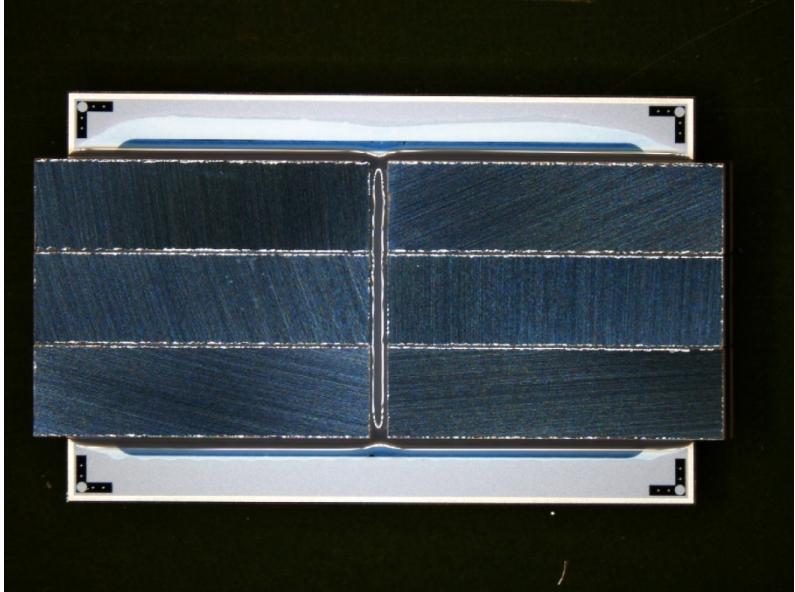
- Assembly of 3 x 2 MPA-light chips for a total of 288 pixels
 - Bump-bondable to detector
 - Wire-bondable to hybrid
 - 5.4mm x 12.7mm



- MaPSA-Light is test vehicle in 2015-2017 timeframe



6. MaPSA-Light Assemblies



6. MaPSA-Light Assemblies, Roadmap

2015 →

Manufacturer	ID Number	Wafer ID	Location	Particle Detector?	Electrically OK?	comments
(red = actively used, magenta=spare)						
NOVAPAC	0	34123603	Princeton	ok	5 out of 6	one MPALight unresponsive due to shorted wirebond
	1	34123603	Brown	good	good	
	2	34123603	Rutgers	good	good	
	3	34123603	CERN	good	good	Davide's tests
	4	34123603	CERN			
AE MTEC	0	34123606	Princeton	bad	5 out of 6	one MPALight unresponsive due to shorted wirebond
	1	34123606	Rutgers	bad	good	
	2	34123606	CERN			badly misaligned, cross-section tests
	3	34123606	CERN			Davide's tests, cross-section tests at AE MTECH
	4	34123606	CERN			From the first (bad) batch
	5	34123606	CERN	good	good	Davide's tests
LETI	3	34123605	FNAL	good	good	
	24	34123605	KIT	ok	good	16 dead channels (chip handling?)
	9	34123605	HEPHY	ok	5 out of 6	one MPALight unresponsive (chip handling?)
	15	34123605	CERN			
	23	34123605	CERN			
	2	34123605	CERN	good	good	Davide's tests

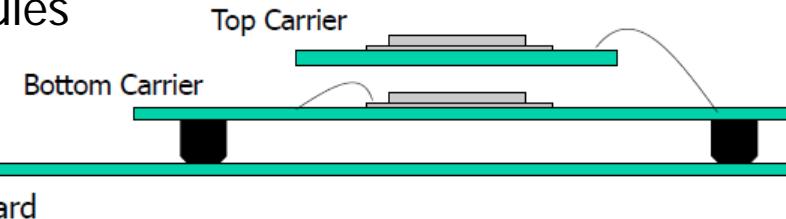
2016 →

Respin (up to 80pcs)

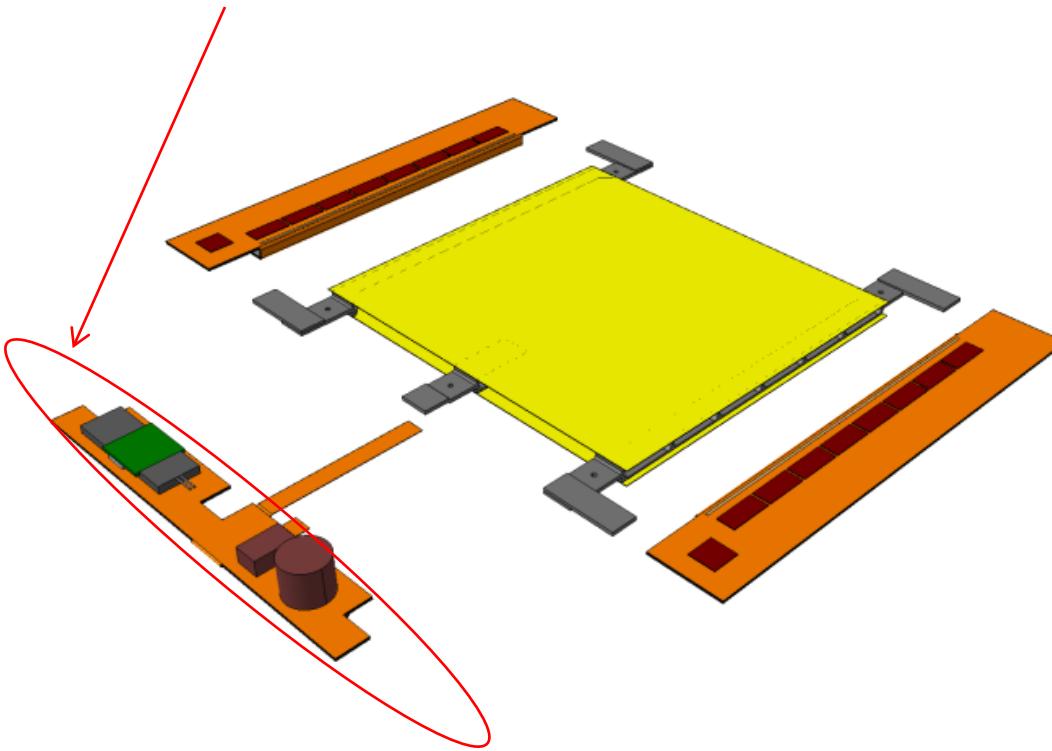
- Novapac, Aemtec (CERN)
- CVI (FNAL)
- KIT (KIT)

2017 →

Micro-Modules



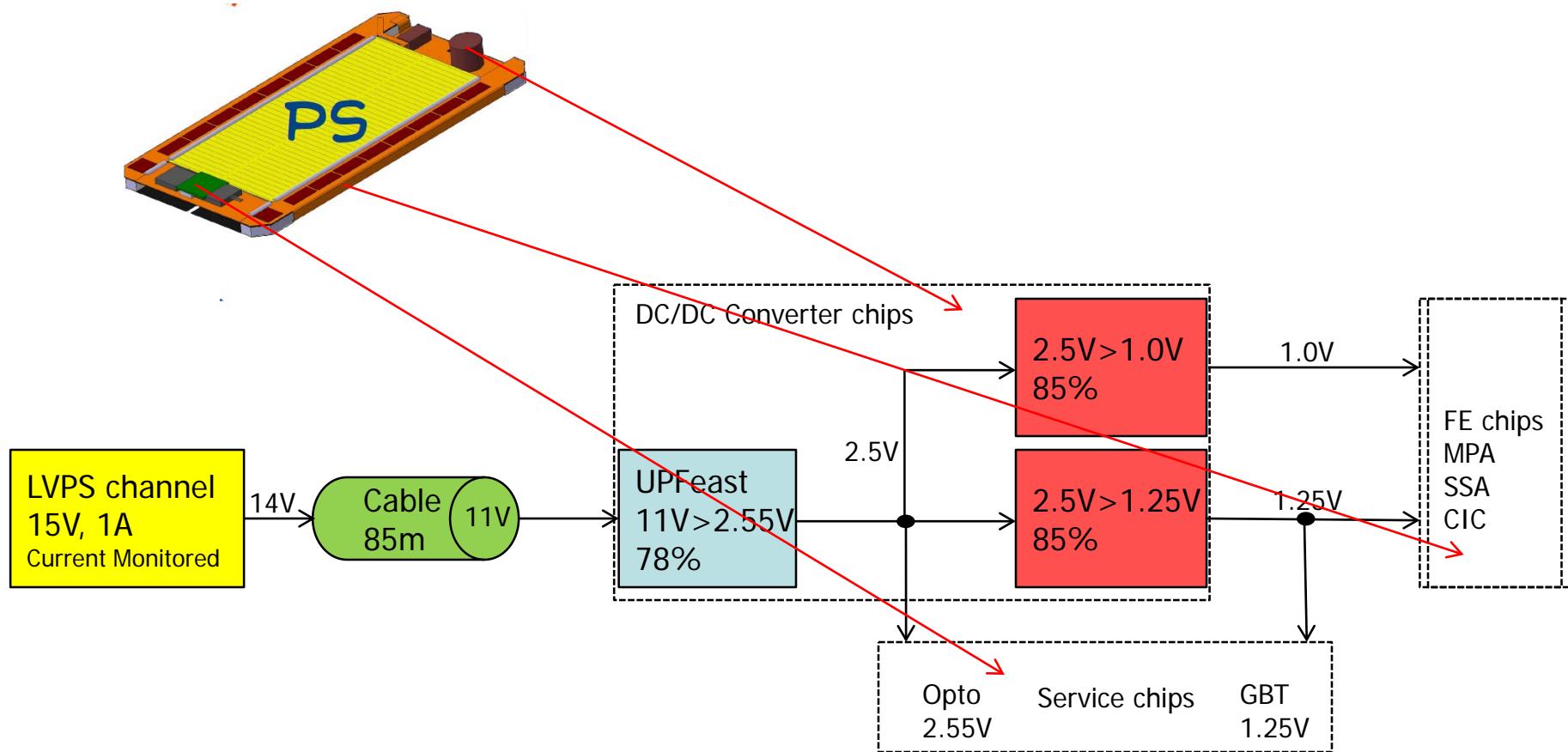
7. Front-End Services



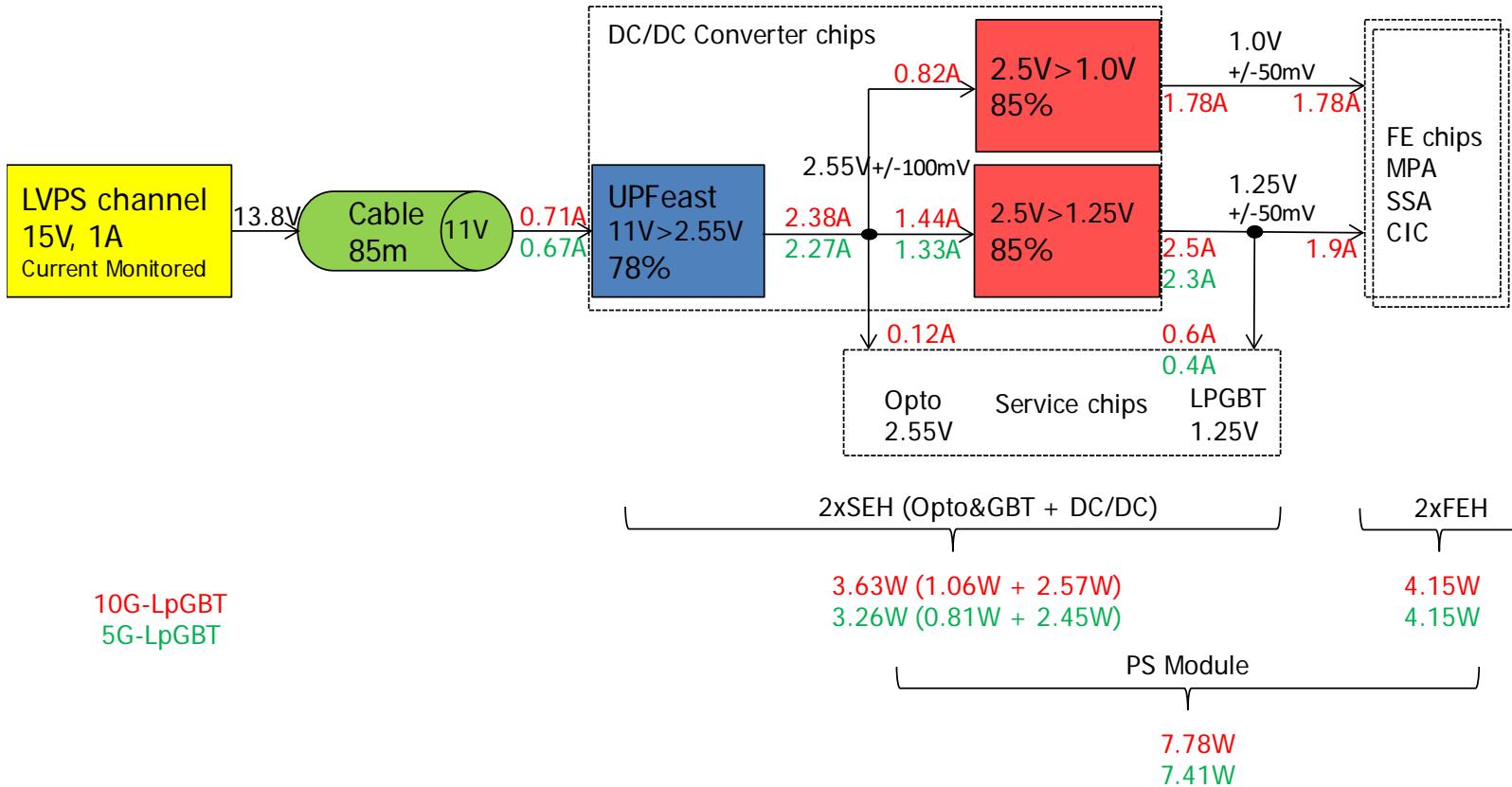
Counting exclusively on CERN EP-ESE common projects for phase II:

- DC/DC converters (UpFeast + DCDC2S)
- Lp-GBT
- VL+

7. FE Module Powering Scheme



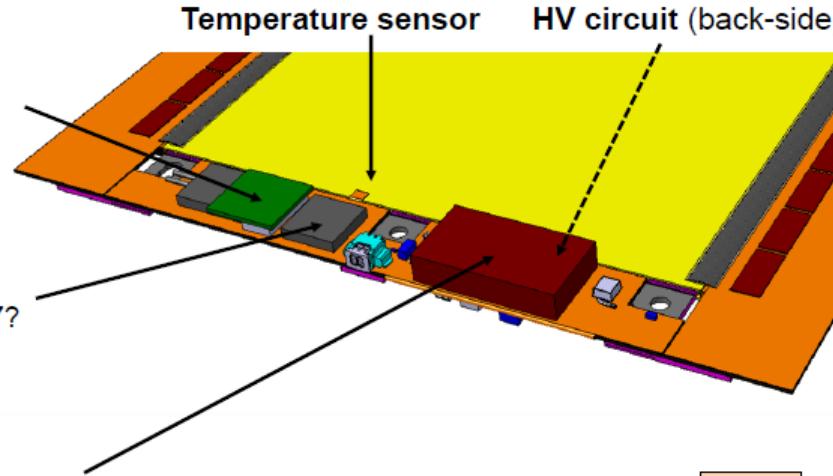
7. FE Module Power Budget



7. Service Hybrid

VTRx+

- Prototype exists
- not yet rad-hard
- not yet final geometry
- Feasibility demonstrator in Q2/2017

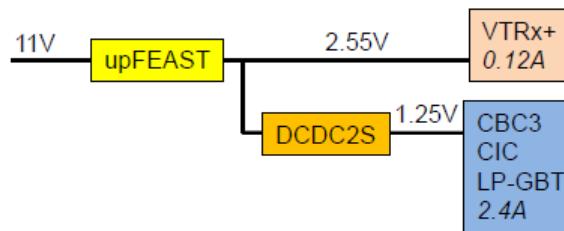


LP-GBT

- First prototype Q3/2017?

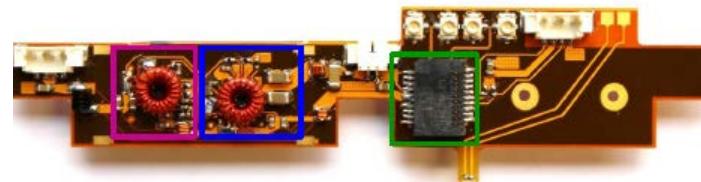
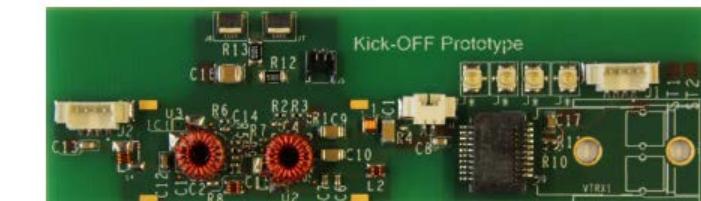
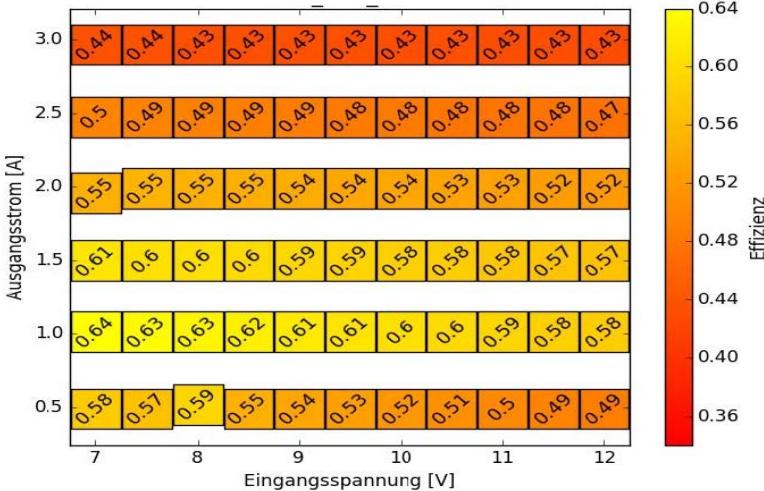
upFEAST

- First prototype exists
- Substrate noise → not for distribution
- Next version Q3/2016



DCDC2S

- Submission of first prototype May 2016
- Expected back Q3/2016



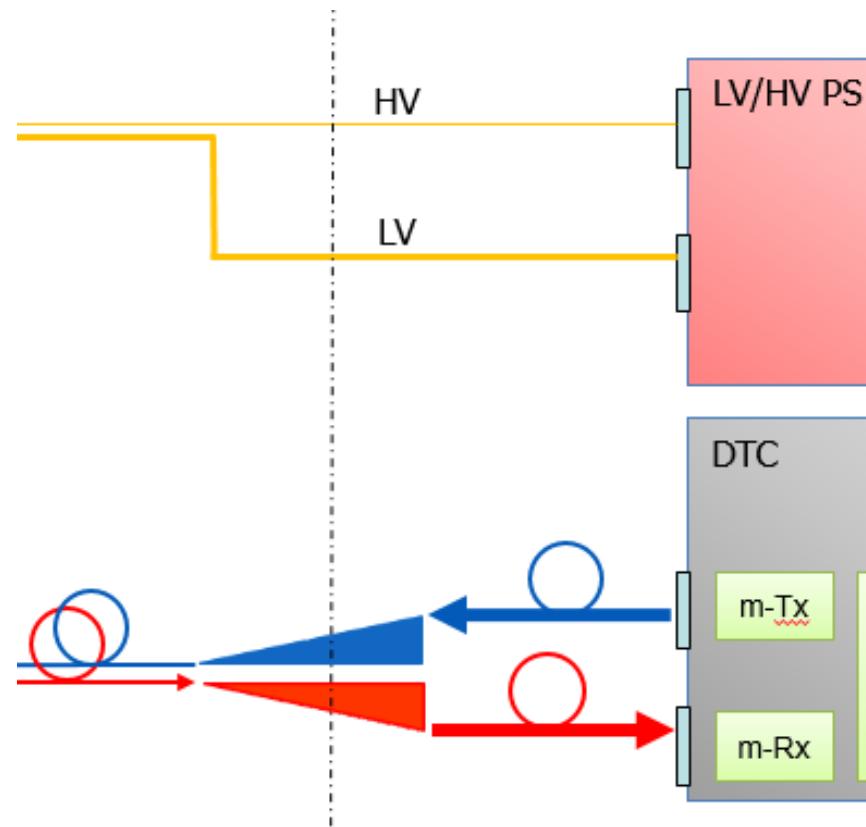
The Electronics for the Upgrade of the CMS Outer Tracker

Outline

1. System Architecture
2. Front-End
3. Back-End
4. System Tests
5. Conclusions

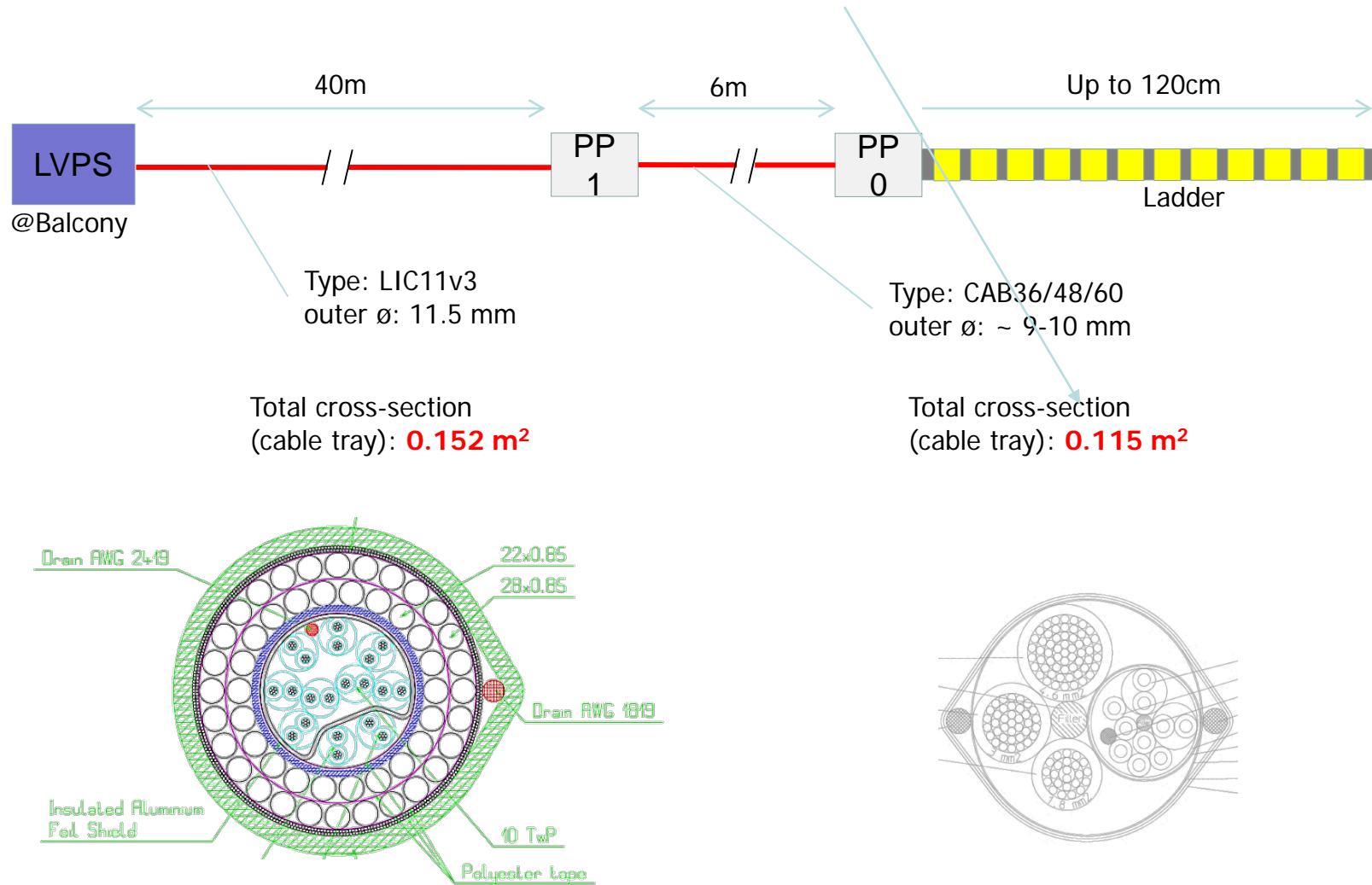


Back-End



1. LVPS System

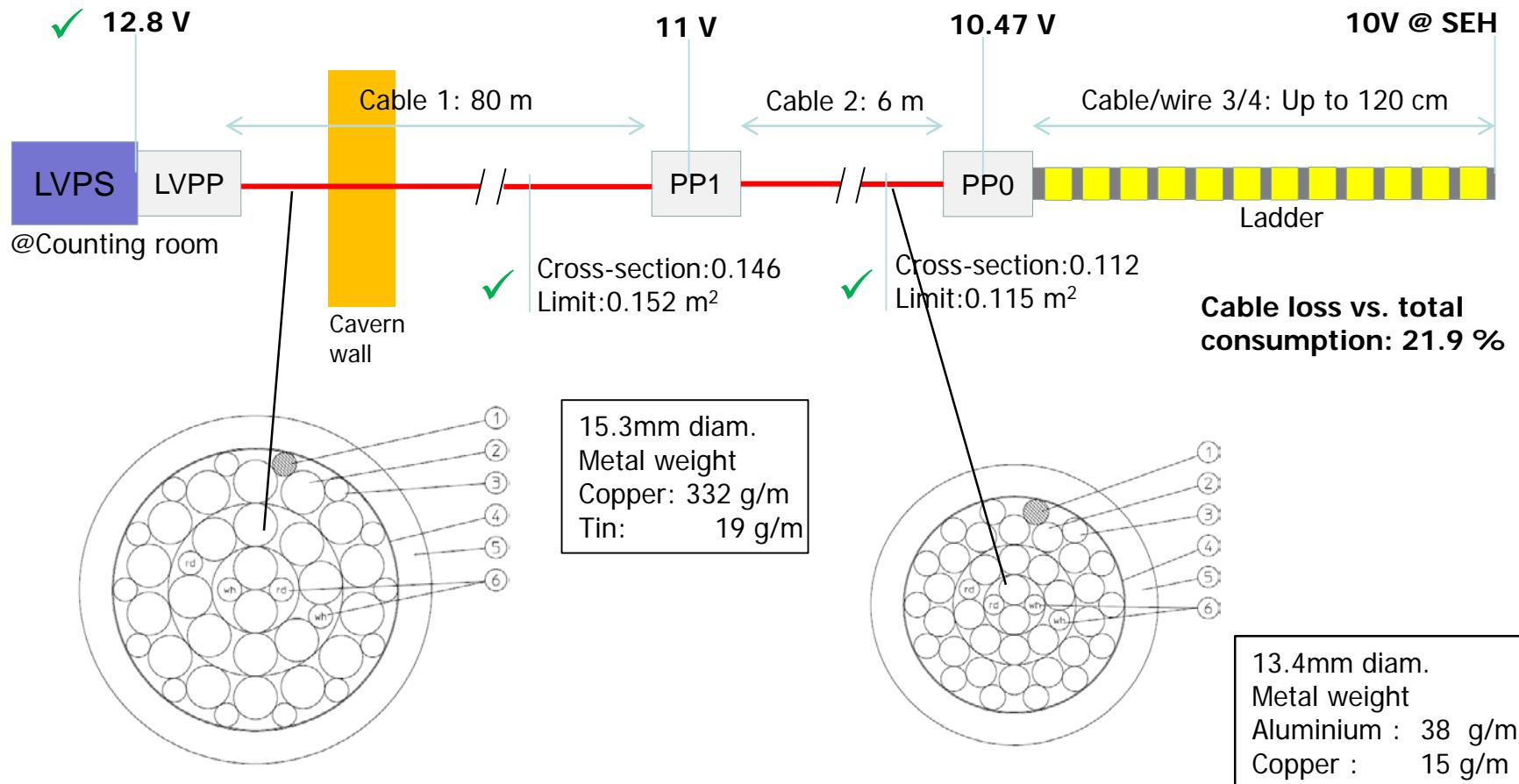
Reminder: Existing system



1. LVPS System

Proposed system for phase II

- Assumption: Tracker can count on same cross-section for services

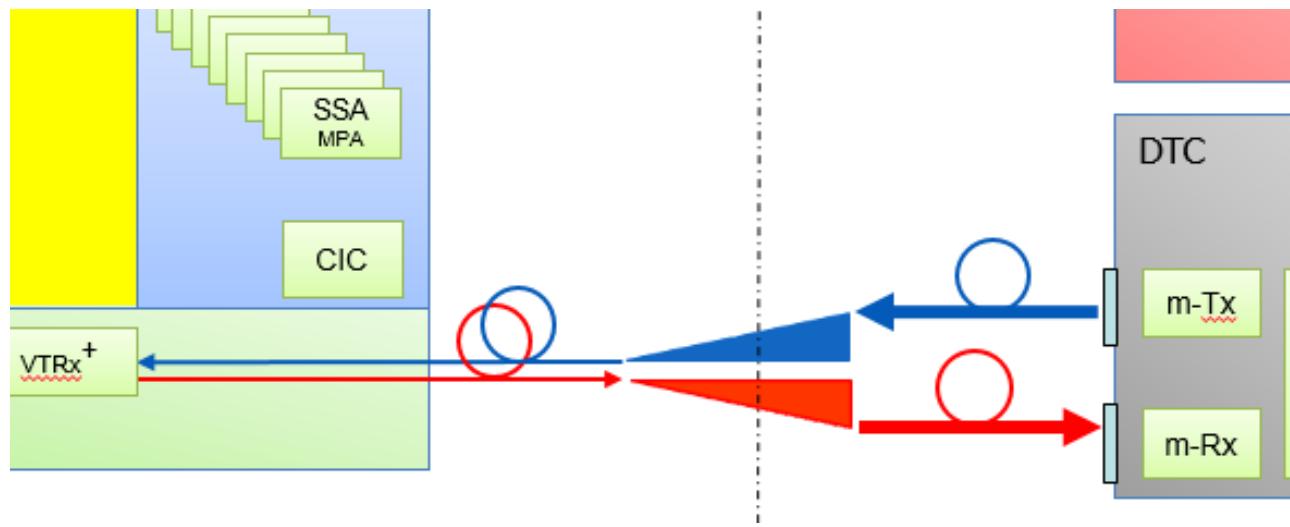


1. LVPS System

Roadmap

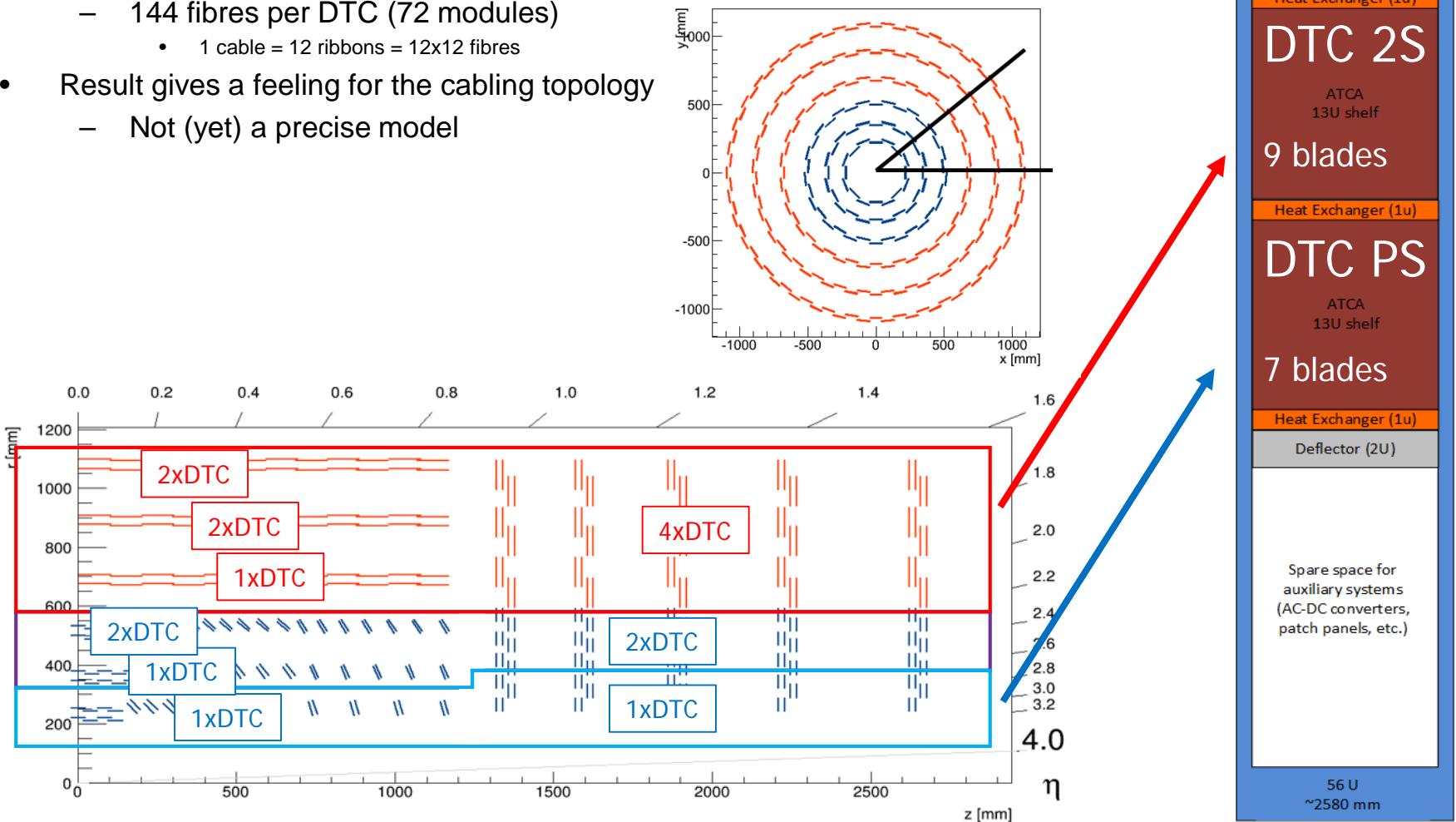
- 2016 → - Custom cable ordered
- Modified Power Supplies (current-based regulation) received (C) or ordered (W)
- Patch Panel prototype (LVPP) received
- 2017 → - Joint ATLAS/CMS project started
- Experimental validation and simulations

2. Opto System



2. Opto System

- Segmentation based on:
 - One octant (45°), $z+$
 - 144 fibres per DTC (72 modules)
 - 1 cable = 12 ribbons = 12×12 fibres
- Result gives a feeling for the cabling topology
 - Not (yet) a precise model



3. Back End Board

Final Back-End DTC will be developed as late as possible to profit from latest available technology and cost reduction.

In the meantime, GLIB and FC7 boards have been developed:



GLIB (Gigabit Link Interface Board)

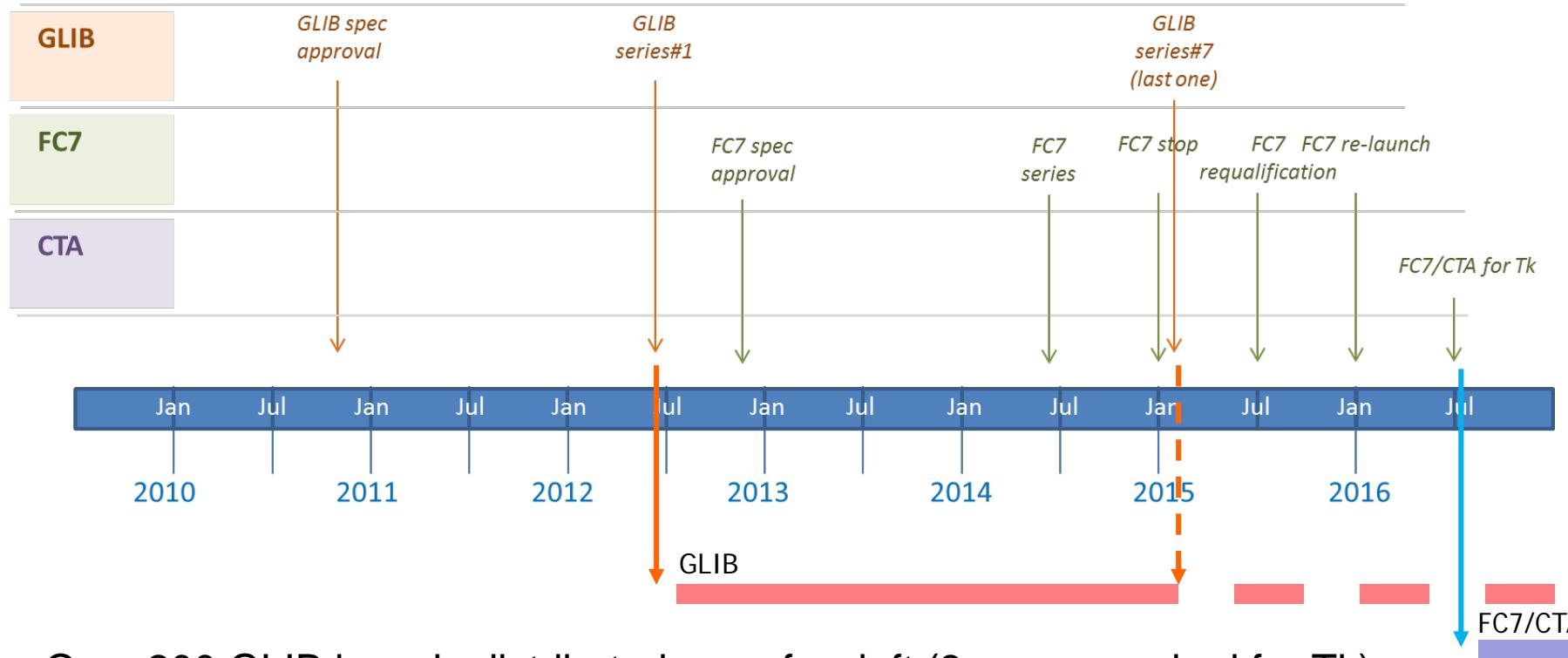
- FPGA **Virtex 6** (~130k logic cells)
- **4 I/O SFP+ native** up to 6.5 Gbps (were used to connect 2 GLIBs)
- Port **Gbit Ethernet**: 1 Gbps with IPBUS
- μTCA connector
- 2*72Mb **SRAM** (static)
- 2 FMC slot supporting **HPC** mezzanines



FC7 (FMC carrier - Xilinx Series 7)

- FPGA **Kintex 7** (~420k logic cells)
- **No native SFP+** cages
- **No port Gbit** Ethernet
- μTCA connector
- 4 Gb **DDR-3 RAM** (dynamic)
- 2 FMC slots supporting **LPC** mezzanines, located on the same side (front side of xTCA crates)
- μSD card to select f/w versions, I2C values...

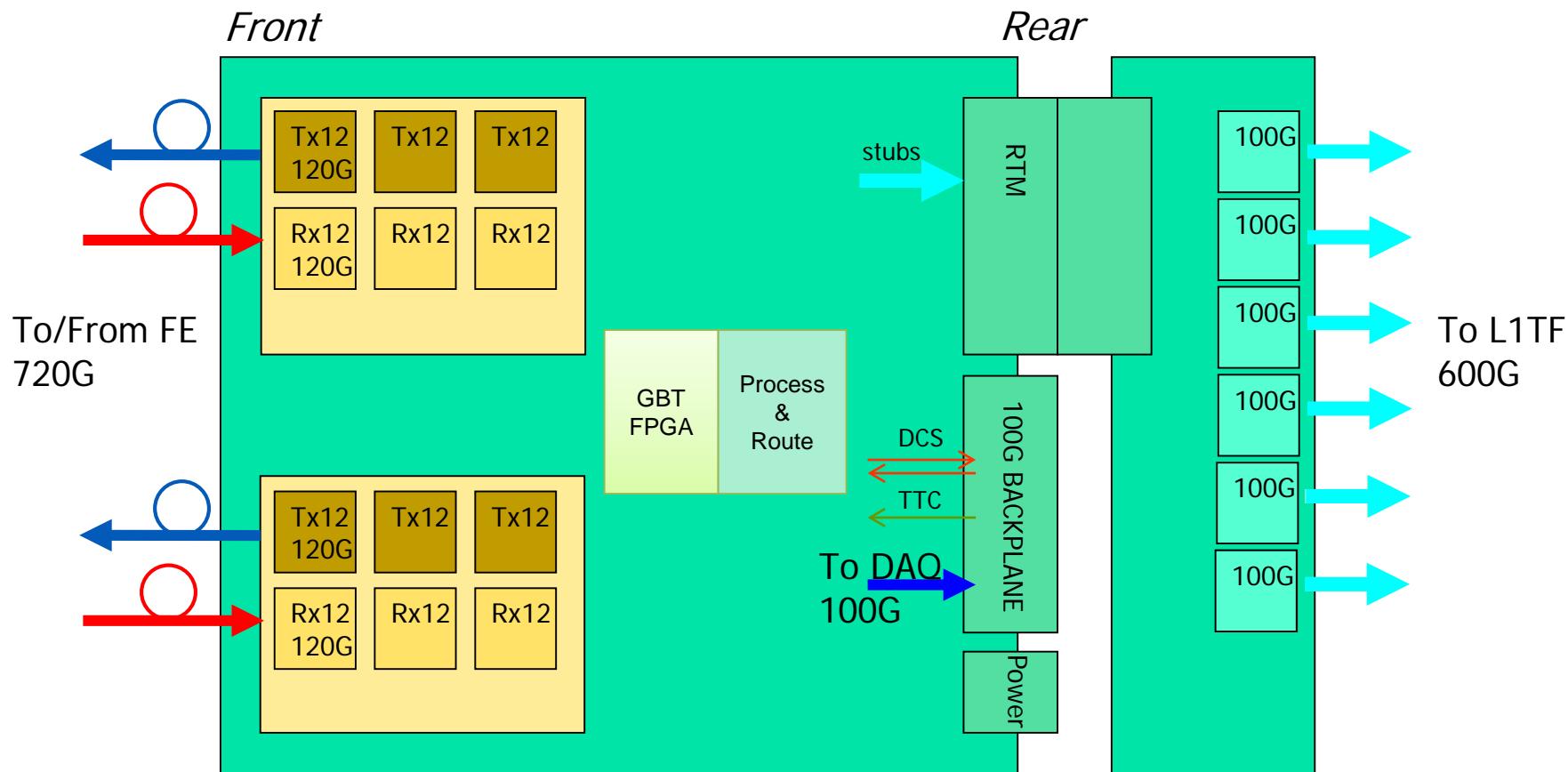
3. GLIB > FC7/CTA Transition



- Over 200 GLIB boards distributed, very few left (3pcs earmarked for Tk)
 - GLIB is a bench-top board for simple systems
- Systems targeted for 2017 and beyond will be based on FC7/CTA
 - FC7/CTA is an in-shelf board for multi-module systems

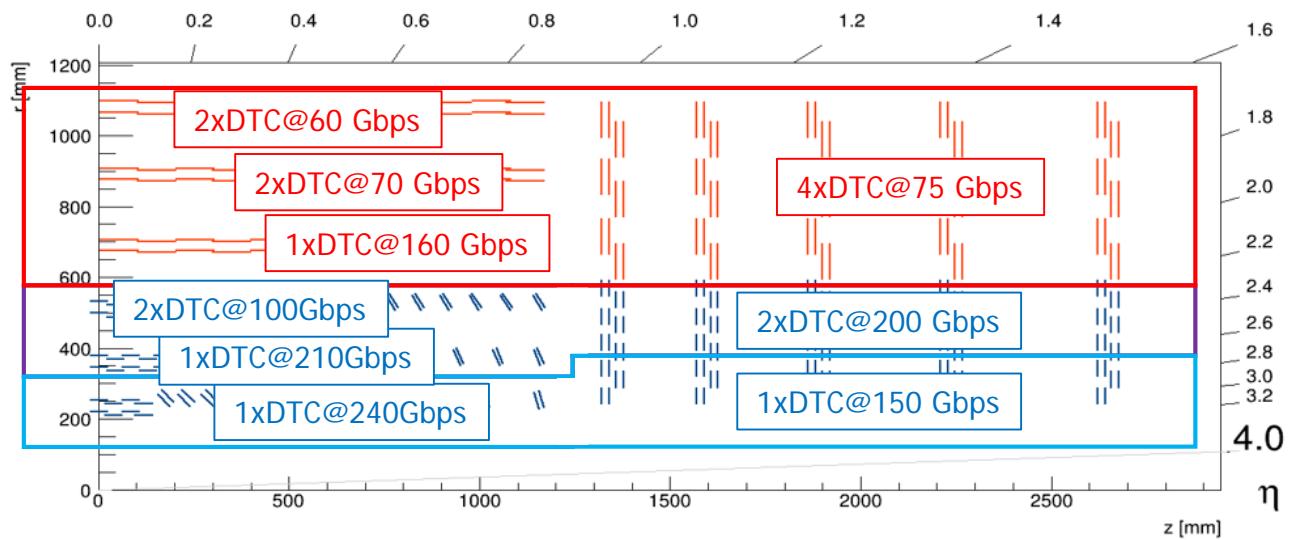
3. DTC Strawman

- ATCA Blade with Rear Transition Module
- FE: 72 x 10G Transceivers
- BE-TF: 24 x 25G Transceivers on RTM
- BE-DAQ: 4 x 25G Transceivers
- 100G ATCA backplane

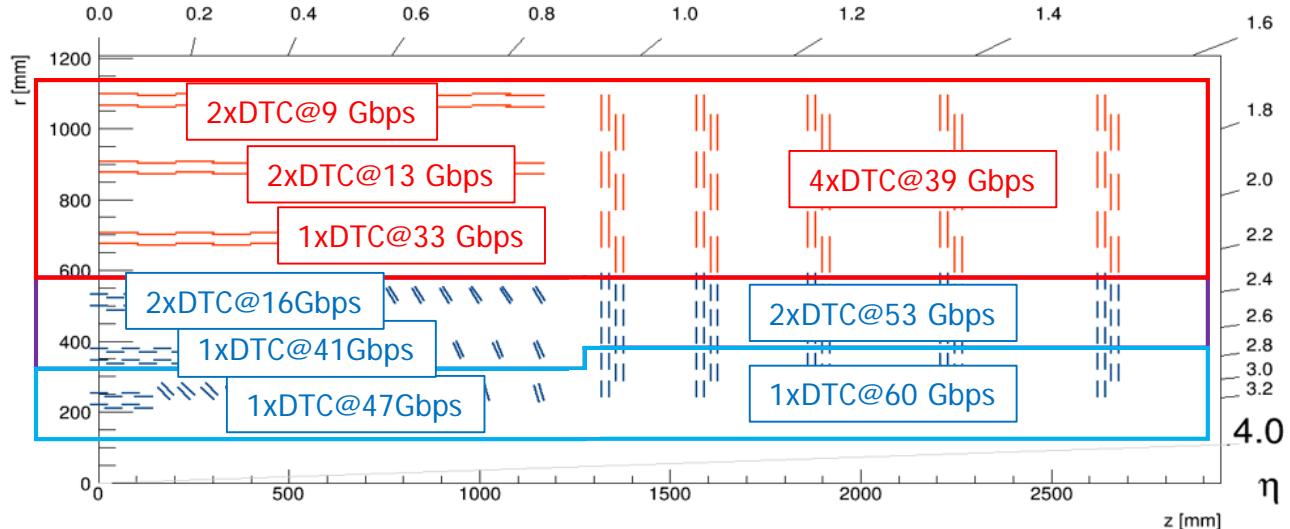


3. DTC estimated output streams

Average to L1-TF



Average to DAO

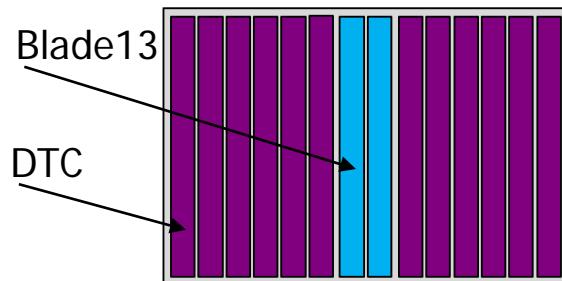


3. Integration into CMS Shelf

M. Hansen, 29 Feb 2016



Possible generic CMS ATCA shelf continuing the microTCA direction

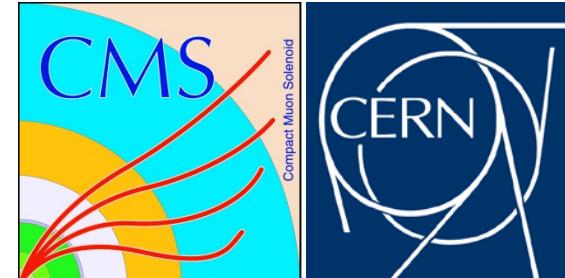


- Common shelf specification
- Generic Blade with, perhaps, custom FPGA and link count but *with standard services*
- Hub card with CMS interfaces: TCDS++ and DAQ *with standard services*
 - Allowing for 800 Gbps DAQ per shelf or more without bending standards

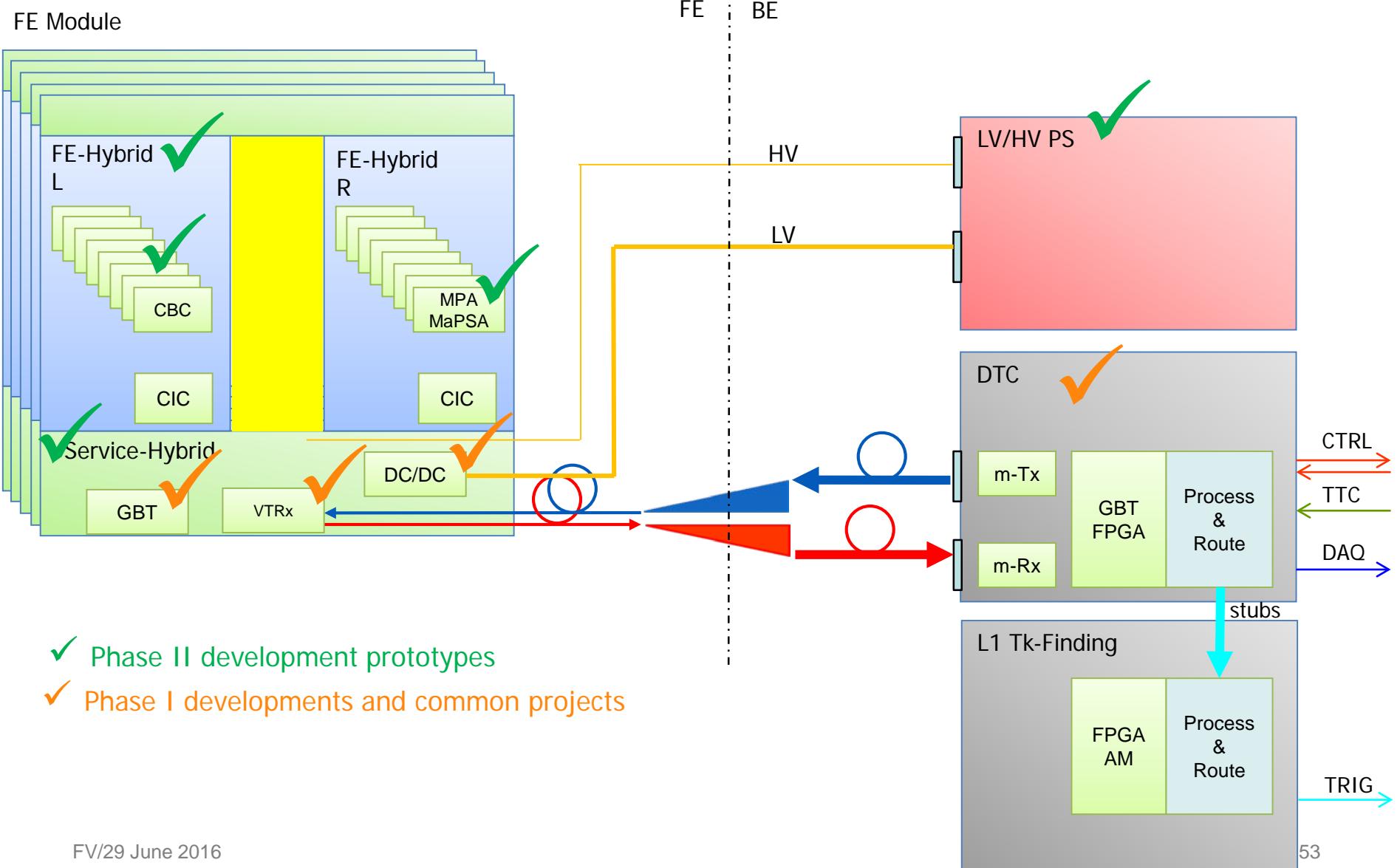
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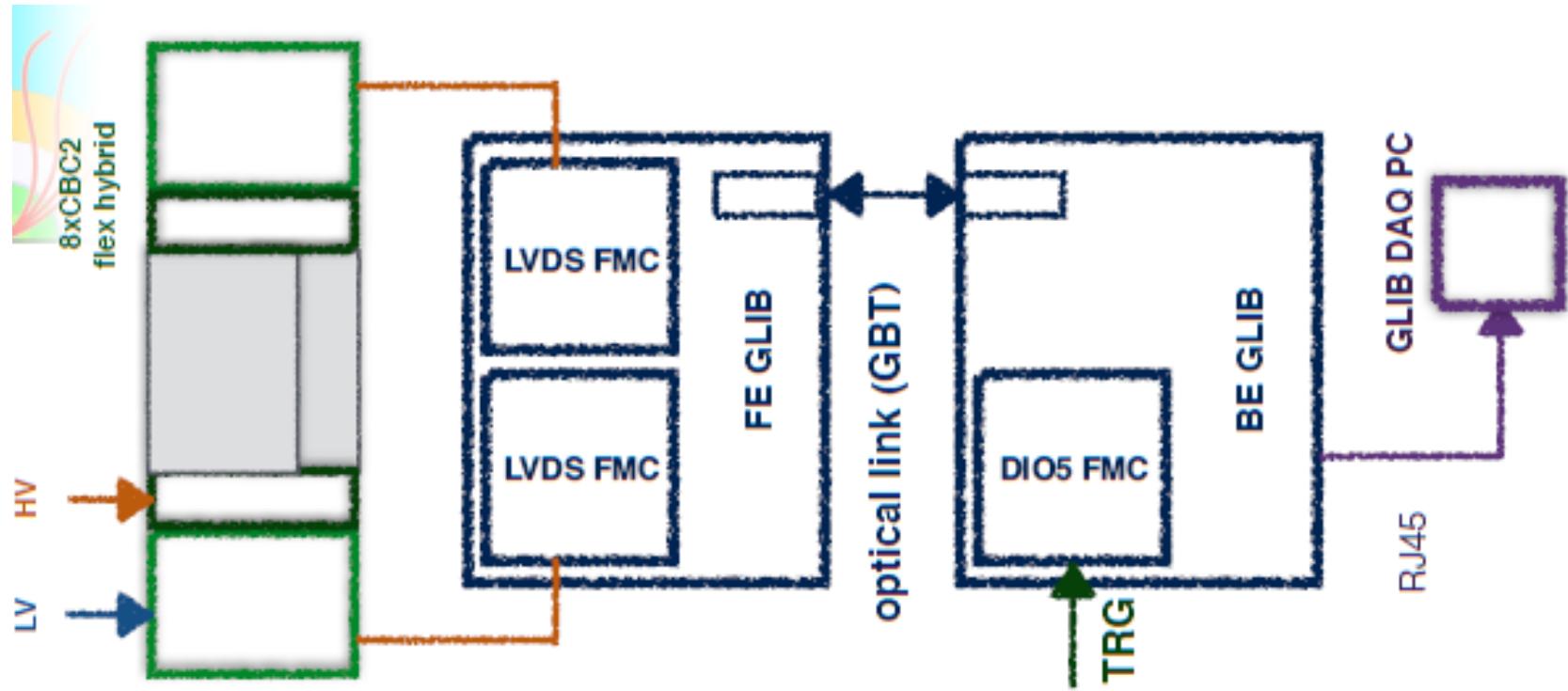
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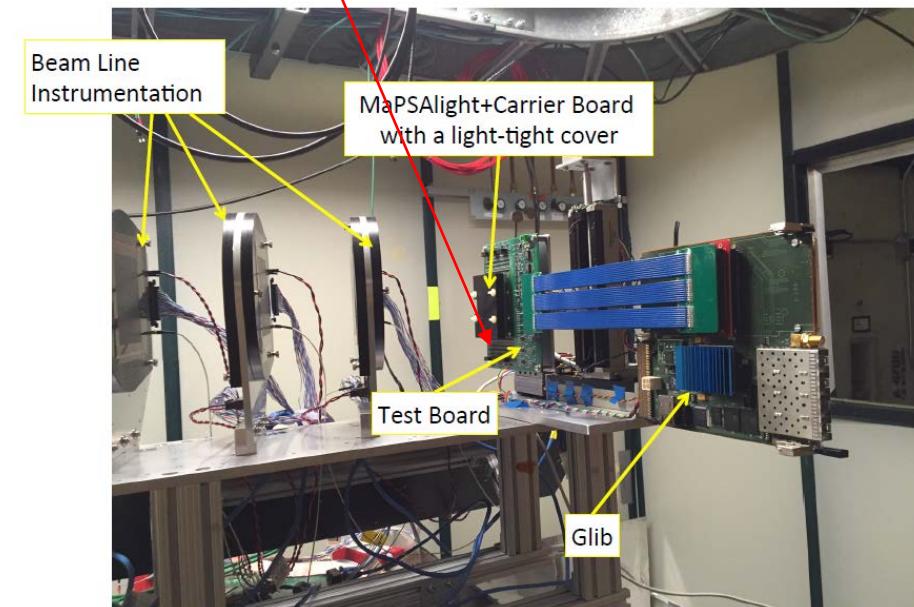
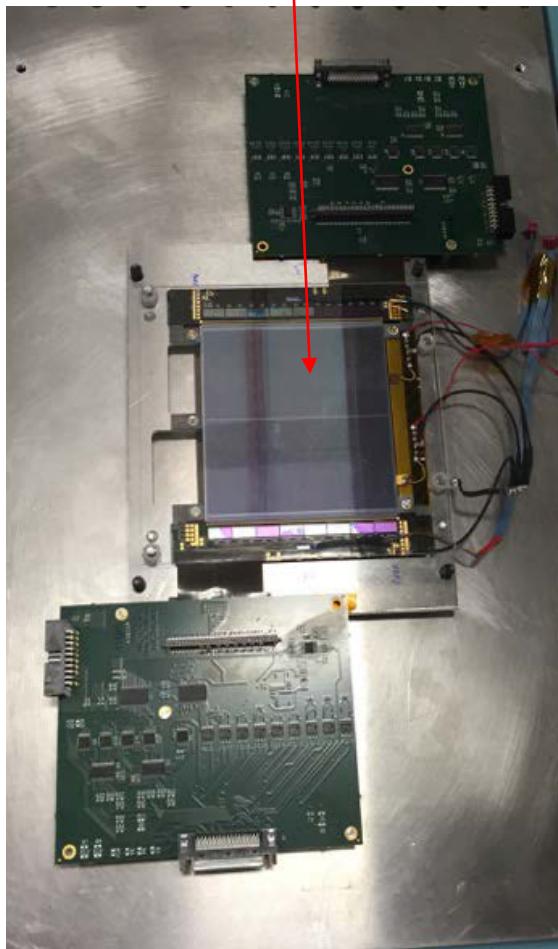
Electrical System: Recap



1. Beam Test: Typical Block Diagram

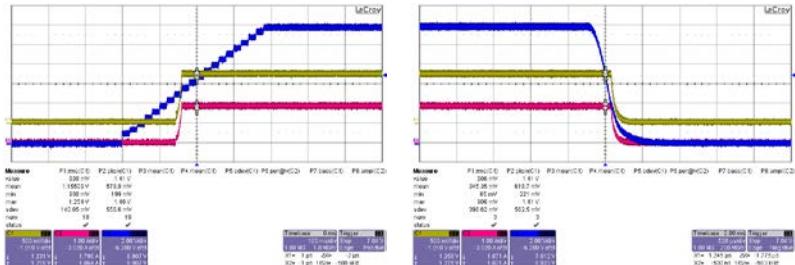


1. 2S-module and MaPSA-Light in beam 2015 and 2016



2. Powering system test 2016

- The power chain has been set up with presently available prototypes
 - CAEN A1516B power supply
 - An 86m long cable from the pixel detector
 - The rigid SH prototype with a hand-made shield
 - A 2-CBC2 mini-module with two sensors, read out electrically
- Allows to study module noise with different powering schemes, and dynamic behaviour of power supply

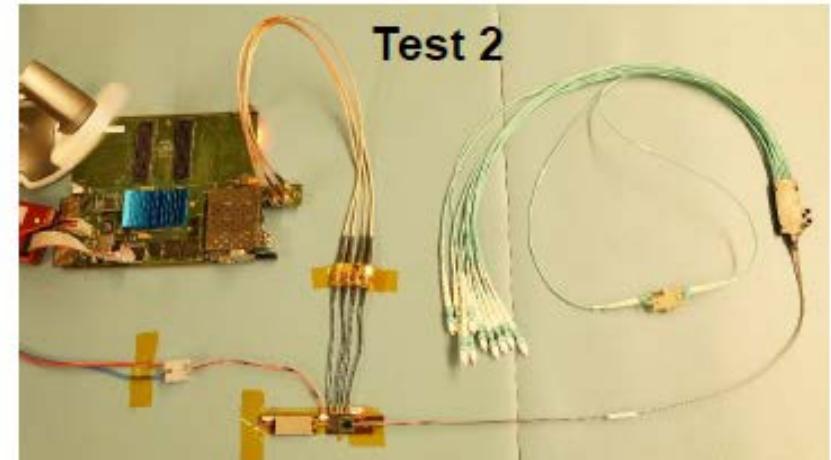
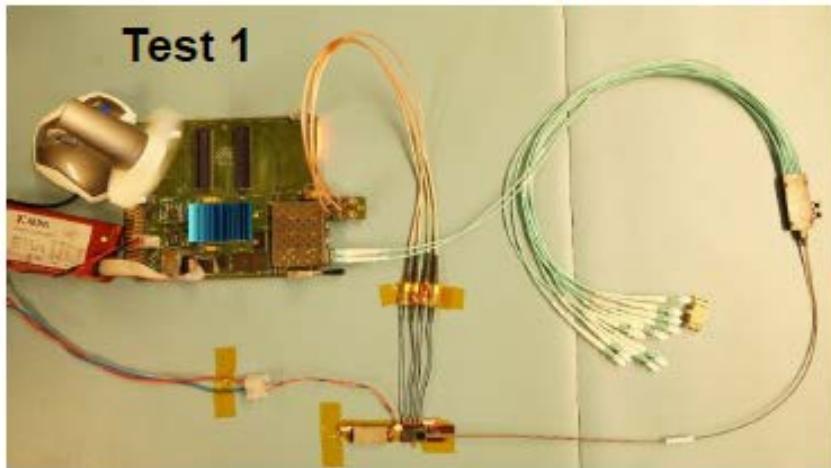
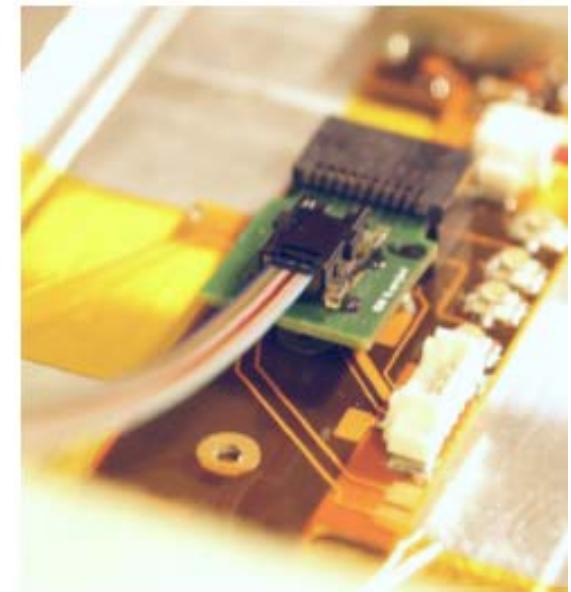


Vin at SH
Vout at SH (1.2V)
Iout of SH|



2. Readout system test 2016

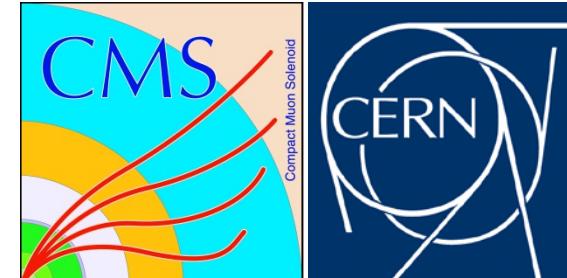
- VTRx+ prototype is powered by service hybrid
 - CERN TIA, commercial LD, PRIZM connector
- **Test 1:**
 - Data generated by GLIB, send electrically to SH, optically through VTRx+ to GLIB, and back
 - No errors with iBERT with “PRBS 31-bit” @ 5Gbps
- **Test 2:**
 - Data generated by GLIB, send electrically to SH, loop-back at VTRx+, and back
 - No errors with GBT protocol @ 5Gbps



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Conclusions

- Outer Tracker electronic system in good shape
 - Most FE functionality demonstrated with full-scale or mini-ASICs
 - Concentrator being simulated at system-level
 - Technology for FEH at industrial cutting edge
 - Power dissipation under constant scrutiny
- Rely heavily on common projects for data transfer and power
 - LpGBT, VTRx+, DC/DC converters, bulk power supplies
 - Need to continue support and identify people/groups in charge of Tk-specific implementation
- Full 2S DAQ chain demonstrated in beam (GLIB-based)
 - Prototype powering scheme demonstrated in lab
 - DTC backend being discussed, likely to be ATCA blade
- Next major demonstrators:
 - Full PS DAQ chain in 2016 (micro-module-based)
 - Full-size ASICs (CBC3, MPA, SSA, CIC) by late 2016 / early 2017
 - Full-size MaPSA in 2017
 - Full chain by late 2017
- Detailed system integration now starting
 - System-level simulation and Documentation
 - Large enterprise with many pitfalls
- On the radar screen
 - CIC and service chips
 - Irradiation tests of FE chips