Preliminary Implementation of the DTC-tester

Alishba Kanwal, Dr Awais M. Kamboh
National University of Sciences and Technology, Islamabad, Pakistan

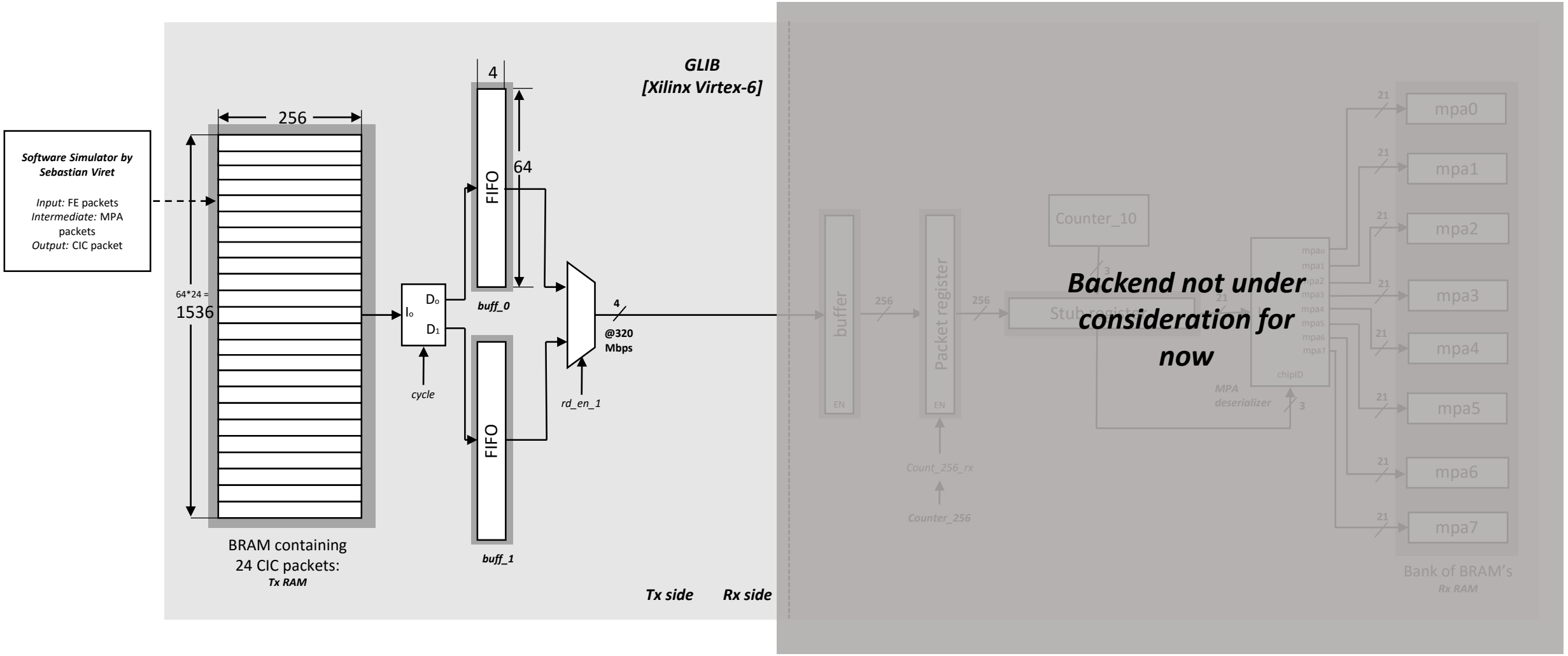
Aims

Create a pattern generator that will emulate a Tracker Phase-2 module to debug backend cards

Immediate tasks:

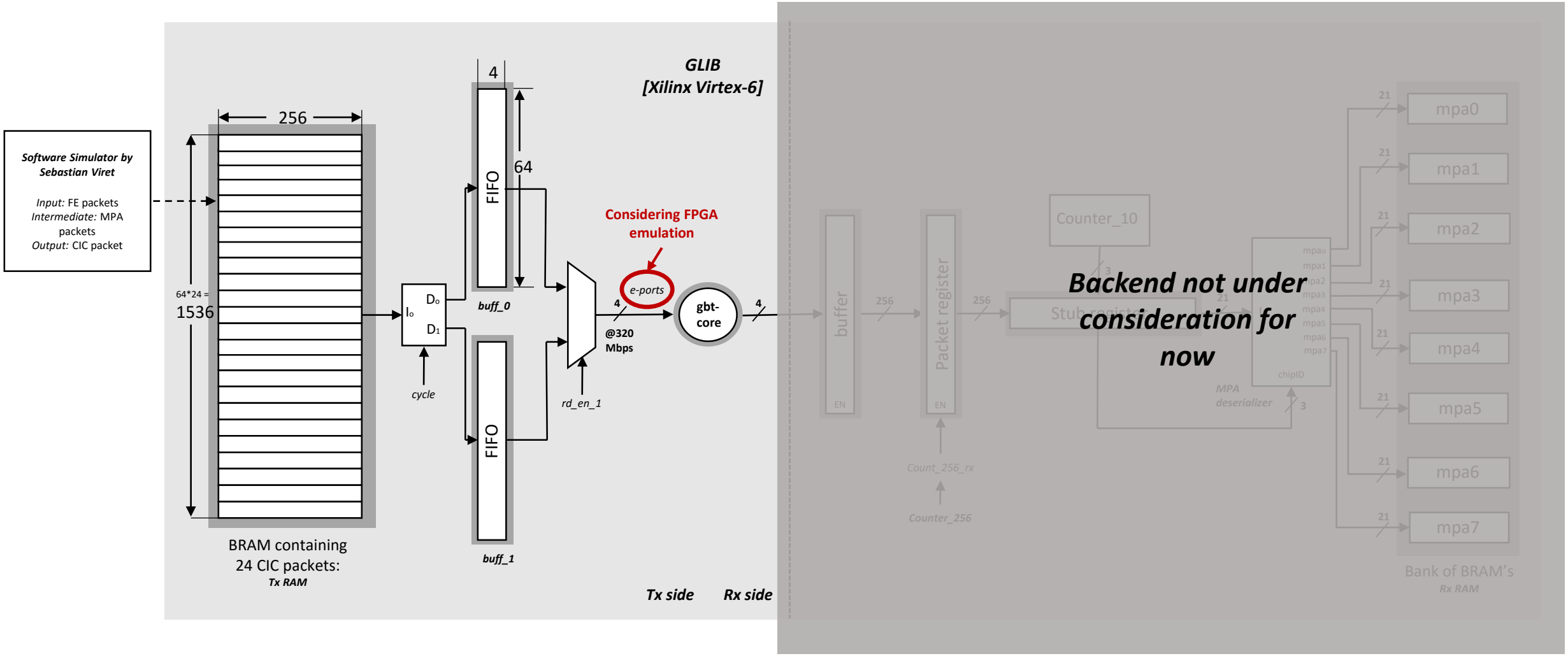
- Emulate the CIC payload sent to the lp-GBT using 4 lines running @320Mbps
- **Possibly emulate e-ports on FPGA**
- Consider size of input batch of patterns and consider use of off-chip memory [use of the two SRAM's on the GLIB]
- Connect a GBT-FPGA core to Tx side
- Explore Random Number Generators for generation of suitable input patterns [CIC packets]

Accomplished so far



Next step

Condition signals so they can be connected to a GBT-FPGA core transceiver



Summary

- Simulated data stored in a block RAM in Xilinx, initialized by a .coe file
- Tx and Rx functionality verified in Xilinx ChipScope
- Deserialized stubs information stored in separate BRAM's after reception
- Emulator gives expected deserialized outputs at up to 500 MHz (verified in ChipScope)
- System designed to process 24 packets at every hardware strobe. Greater packet influx from the simulator can be considered