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Data transmission efficiency of the phase II tracker front-end system using new GBT transmission scheme

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Abstract

Phase II outer tracker of the CMS experiment, due to the inclusion of the tracking at the first level of the trigger, will be a key component of CMS future triggering strategy. L1 tracking will be a very challenging task requiring the fast treatment of a huge data troughput. In order to meet this challenge, data rate reduction will be performed directly at the frontend level. The trigger signal will be compressed in two stages before being extracted from the detection module. The second compression step, performed by a concentrator chip (CIC), will heavily rely on average occupancy in the tracker. If this occupancy becomes to large, one has to evaluate how large the risk of data losses becomes. This document is an update of the previous losses study, based on newly proposed GBT transmission scheme.

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1 Introduction

CMS phase II outer tracker will be a key component of the future triggering system of the detector. L1 tracking is indeed mandatory in order to keep a good level of performance in very high pile-up conditions.

Performing L1 tracking is a complex task which is out of the scope of this note. This procedure will be performed at the backend level, using information extracted from all the detector channels at 40MHz. In order to extract this enormous amount of data, two compression stages will be applied at the frontend level, directly on the detector modules. This procedure will be shortly described in Section 2.

This procedure should not only enable the extraction of the the full trigger information at 40MHz, but also be able to extract the full raw data of the tracker at rates as high as 1MHz. Indeed, if an event pass the trigger L1, it will go trough the HLT where the complete raw tracker data will be necessary.

Thanks to a low detector occupancy, space and time compression is expected to provide a significant data rate reduction. It's therefore important to check that the compression factor will be sufficient everywhere. The equation is quite simple: one must be able to pass L1 raw data up to 1MHz without any losses, and trigger data up to 40MHz with losses sufficiently small to be neglected by the L1 tracking.

This document is an addendum to Ref. [1], based on the recent GBT evolution, presented in Ref. [2]. Introductive parts are repeated. Then, updated trigger and L1 data transmission efficiencies are presented in Sections 3 and 4 respectively. Finally, conclusions are provided.

2 Principle of the study

2.1 Front-end data extraction

Extraction of the future CMS digital tracker signal from the detector level to the backend is following a multi-step chain described in details in Ref. [3]. Baseline requirements are the following: the system must be able to extract simultaneously the trigger data at 40MHz and the raw data from event passing the first trigger level up to 750kHz frequencies.

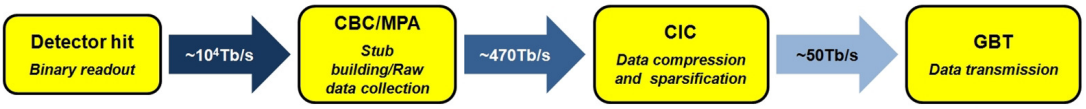

Figure 1: Phase II tracker front end data flow

The different front-end compression steps are represented on Fig. 1. Everything starts with the binary signals of the $\tilde{2}$50M channels of the future tracker. At 40MHz, it represents roughly a total amount of 10^4Tbps!!! These signals are collected in each module by 16 frontend (FE) chips. Each FE chip sends out its signal via 6 differential lines working at 320Mbps. The total output rate for one module is therefore equal to 16x6x320 = 30.7Gbps per module, so a total data rate of 470Tbps. This first step therefore provides a compression factor of around 20. At the other end, the data is extracted from the module by 5 or 10Gbps bi-directional optical link. In practice the available bandwidth for downstream data transfer is 3.7Gbps. Clearly, another data compression step in between is mandatory. This compression step, performed by the concentrator chips (CIC), strongly relies on a low tracker occupancy, both in space and time. Granularity of the future tracker will indeed be much higher than of the current one. In the CIC chip, the signal of every module will be gathered over time (8BX) and space (8 chips) as sketched on Fig. 2. There will be two CIC chips in every module.

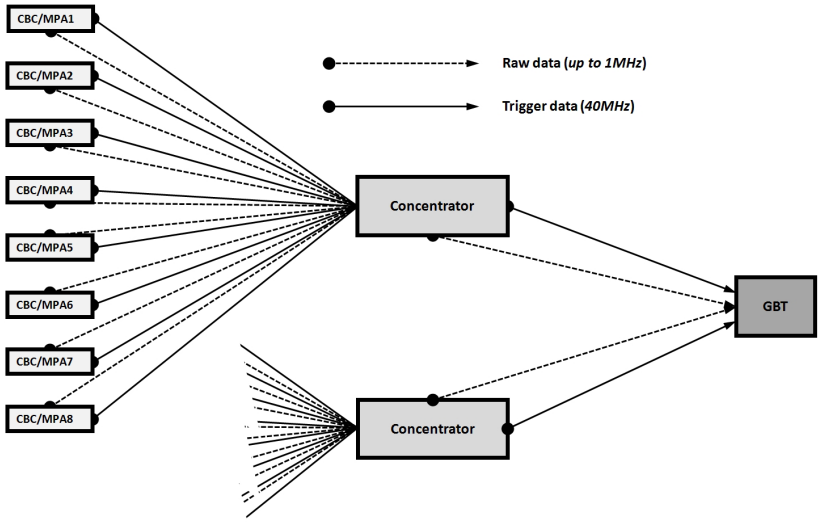

Figure 2: Data concentration principle in phase II tracker

The different CIC I/O data formats used along this note and the signal processing done within this chip are based on Ref. [4]. However, along this note we will also rely on the proposal described in Ref. [2].

By construction, the CIC output bandwidth will be 9.6 times smaller than it's input bandwith. As we have seen, this characteristic is driven by the low tracker occupancy assumption. It is mandatory to check that it will effectively be the case, otherwise the CIC might become a serious bottleneck in the tracker transmission chain. It is therefore particularly important to evaluate the data transmission efficiency at the CIC level, along with the average occupancies in the future detector. Currently, the only way to do that is to use simulated events in order to create large sequences of data and to pass these sequences trough an emulation of the FE data acquisition chain.

2.2 Events used

As already said, CIC will transmit two different data flavors: L1 and trigger. In the baseline scenario, both streams will be sent into fixed-size data blocks. Unless explicitely stated, we will always use this baseline block, ie 320 bits every 8BX divided into 80% for trigger (256 bits) and 20% for L1 (64 bits).

The trigger block will always contain synchronous data. It means that the trigger data transmitted into a concentrator block will correspond exactly to the data contained into the 8 bunch crossings covered by this block. On the other hand the L1 block will be fully asynchronous. It will indeed usually take much more than one CIC block to extract a complete L1 event. Up to a certain extent, this is however not a problem, as L1 data transmission latency is much less constrained.

These technical differences will lead to different methods to test the transmission efficiency, and also to different test samples. Events passing L1 trigger are indeed expected to be slightly more complex than raw events entering the tracker at 40 MHz. On the other hand, in the raw data flow, some busy events might appear at a certain frequency, so using only simple min-bias events might not be sufficient. Taking that into account, we defined two different type of test samples, for trigger and L1, based on the two following base data sets of 300 events each: a raw sample of basic minbias events, and a busy sample of minbias+4tops events. These samples are then used as follows:

- **Trigger block** transmission efficiency is tested using a random mix of 10% busy events and 90% raw minbias events. Using only minbias events would lead to a slight underestimation of the losses, whereas using a larger proportion of busy events was not considered to be realistic.
- **L1 block** transmission efficiency is tested using only busy events. This might be considered as a pessimistic approach. However, fututre L1 trigger, partly because of the inclusion of tracking, will tend to select more complex events than the current L1.

The two base datasets (min. bias and PU+4tops) were produced using the most recent CMSSW release at the time of the study: 620_SLHC16. Different average pile-up configuration were tested (140 and 200), using the latest minbias tuning available [5]. We also tested different thresholds for the trigger signal (this will be detailed in Section 3).

2.3 Algorithm principle

The simulation is performed using a dedicated tool, starting from the CMSSW events. The principle is sketched in Fig. 3. First of all, two data stores are generated using the two base datasets previously defined. These stores are C++ multimaps made of maps containing all the FE-relevant info of a given event. An event map is built as follows: the first entry contains the CIC chip ID, and the second entry contains all the data recorded by the corresponding CIC chip for this event.

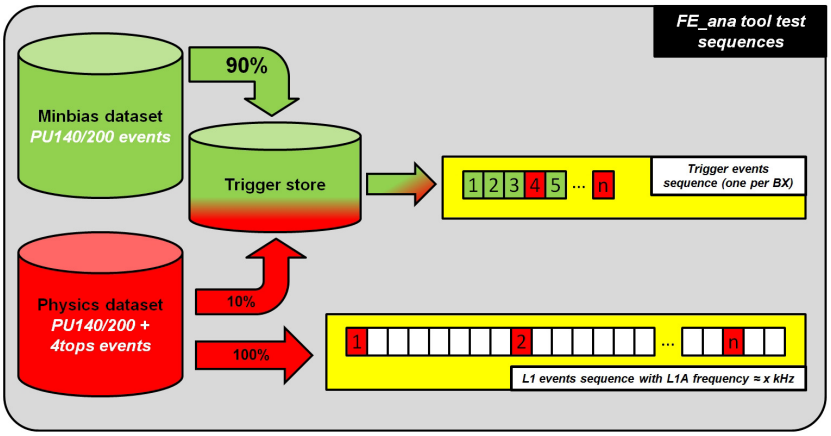

Figure 3: Data sequence building principle with the FE_ana tool

Data contained in the stores is pre-formated for a frontend analysis. The trigger store is made using a mix of physics and minbias sample and is containing only stub information. For the L1 store, only the physics events are

used (that's why the intermediate store step is not shown), and this is the digi information which is stored. The program can be configured to store info either at the FE level (CBC/MPA) or at the CIC level. Therefore, even if the CIC chip is the most critical point, one can study the data transmission efficiencies at the very front end level.

Once the stores are build, virtual sequences of events are created by randomly picking up events into them. The total length of the sequence to produce, given in number of 25ns clock cycles, is provided by the user. As shown in Fig. 3, the major difference between the two type of sequences is the data rate. Whereas for the trigger case, a new event is picked up at each clock cycle (40MHz), the L1 sequence is mostly empty. For the L1 case, a sequence of L1A is generated beforehand for the L1 sequence, at a given rate provided in input (in kHz). The delay between 2 consecutive L1A is not fully random, and is chosen in such a way that the average frequency corresponds to the required one. One also checks that basic trigger rules are fulfilled (at least the ones which are not enforcing the 750Hz requirement). The following rules are applied: no more than 1 L1A in 3BX's, 2 in 25, and 3 in 100 [6].

The analysis of each sequence will be detailed in the following sections.

3 Trigger block transmission

3.1 A qualitative introduction

Before explaining in details how the losses are computed, we will show that a simple look at stub rates could provide some hints concerning the data transmission efficiency.

As previously said, the transmission of the trigger information by the CIC is fully synchronous. Therefore, the amount of information which could be transmitted is strictly limited by the size of the trigger block in the CIC word. In the previous document [1], this size was limited to 256 bits for eight bunch crossings, and eight CBC/MPA chips. This represents 10 MPA stubs and 12 CBC stubs. The format of the CIC trigger block has been described in details in [4].

Four different transmission schemes are described in [2]. In all the cases, there is one more input line per GBT. Schemes are:

- **LP-SEC**: the future baseline, where the only difference w.r.t. the previous scheme is the new input line. If this new input line is allocated to trigger, the size of the trigger block goes to 320 bits (14/16 MPA/CBC stubs per block, 3.5/4 stubs/module/BX).
- **LP-LEC**: same as previous, but with a low error correction scheme (LEC). Trigger block size goes to 384 bits (17/19 MPA/CBC stubs per block, 4.25/4.75 stubs/module/BX).
- **10G-SEC**: if one uses the 10G version of the GBT, one can double the bandwidth and therefore extract up to 640 bits per trigger block (29/34 MPA/CBC stubs per block, 7.25/8.5 stubs/module/BX).
- **10G-LEC**: ultimate version, up to 768 bits per trigger block (8.75/10.25 MPA/CBC stubs per block, 3.5/4 stubs/module/BX).

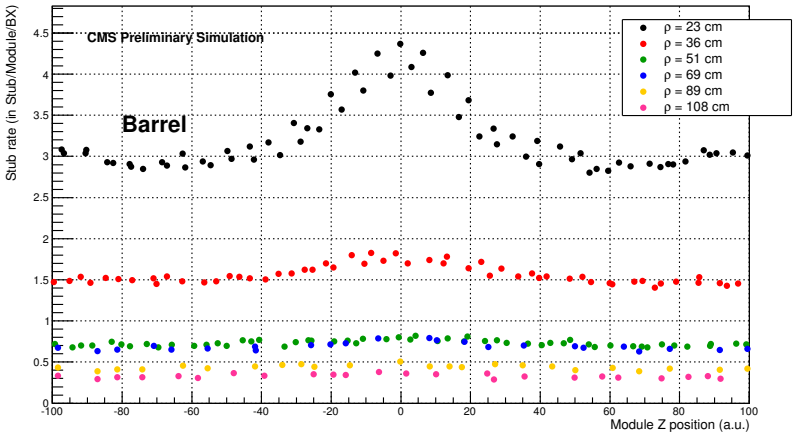

Figure 4: Average stubs rates in the tracker barrel for PU140 events

Figure 4 shows the average stub rates, in stubs/module/BX, measured for PU140 raw minbias events in the barrel layers, as a function of the layer radii and of the module Z position. The three innermost layers are made of PS modules.

Using this plot, one can affirm, without any calculation, that 10G transmssion scheme will be necessary at least in the innermost barrel layer.

3.2 How losses are measured?

When one creates the trigger sequence, the output of the FE_ana tool is a plain root file containing, for each block included in the sequence, one entry per chip (CIC or MPA/CBC, depending on what you asked) and per block. Each entry contains the following infos:

- BX: the BX number of the first event in the block. There is one block every BX the CBC, one block every 2BX's for the MPA, and one block every 8BX's for the CIC.

- CHP: the chip ID, with which one could retrieve all the necessary info about the chip position (layer, ladder, module,...)
- $WORD$: the complete binary trigger word for the corresponding chip and block. The format of this word is the one described in Ref. [4].
- l_{WORD}: the total length of the trigger word. This is one of the main info to evaluate the innefficiency. For example, in the baseline CIC scenario (LP-SEC), there will be a problem if $l_{WORD} \geq 320$.
- N: the total number of stubs seen be the FE chip (CBC/MPA) during the block. For the CIC, the one adds the stubs from all the FE chips.
- N_{FE}: the total number of stubs transmitted by the FE chip to the CIC during the block. Indeed CBC cannot transmit more than 3 stubs every BX, and MPA cannot transmit more than 5 stubs per 2BX block.
- N^g: the total number of good stubs seen by the FE chip during the block. By good stub we mean a stub induced by a primary particle with a $p_T > 2GeV/c$.
- N^g_{FE}: the total number of good stubs recorded by the chip and transmitted by the FE chip to the CIC during the block.

Inefficiencies are computed using the 5 last parameters. For the front-end chips the value of the inefficiency of a given chip is straightforward to extract. One has indeed simply:

$$loss_{FE} = 1 - \frac{\sum\limits_{blocks} N^g_{FE}}{\sum\limits_{events} N^g}$$

For the CIC one should take into account the fact that each chip cannot pass more than 320 bits every 8BX. Therefore, one evaluates the CIC inefficiencies by computing the total amount of stub lost during the whole sequence. CIC inefficiency is therefore given by the following formula:

$$loss^{320}_{CIC} = \frac{\sum\limits_{blocks|l_{WORD}\leq 320} N^g_{FE} + \sum\limits_{blocks|l_{WORD}\geq 320} N^g_{FE} \times \frac{320}{l_{WORD}}}{\sum\limits_{blocks} N^g}$$

As one can see this last expression is an approximation which tends to underestimate a bit the inefficiency. However, the difference w.r.t. to the exact formulae is not expected to be significant.

In the following we will present only the good stub losses. In most of the cases, they are compatible, within statistical errors, with the overall stub losses.

3.3 MPA/CBC losses

Figures 5 and 6 summmarize the average front-end losses measured in the different part of the tracker, for pile-up 200 case, for the 2GeV/c tight and 3GeV/c stub tunings respectively (these tunings are introduced in part 3.5.4 of [1]). The number of bits used to encode the bend are 4 in CBCs and 3 in MPA. Values are given in %. Errors are not mentionned, but they are below 0.05% in all the cases.

At this level, the only way of reducing the losses is the bend tuning. Indeed, one see for example that in ring 1 of disk 1, the loss is 2.24% with the 2GeV/c tight tuning and goes down to 0.41%. If one sets an arbitrary loss limit of 0.2%, one sees that 3GeV/c tuning will be mandatory in some detector regions, whatever GBT scheme will be chosen. These regions are: barrel layers 1 and 2 and disk rings 1,2, and 3. It is important to note that even with a 3GeV/c stub tuning, losses will remain larger than 0.2% in barrel layer 1 and disk ring 1. The only way to reduce these losses would be to increase the thickness of the modules (and therefore the stub discriminating power) in these modules.

However, it's possible to contain the losses to reasonable values, and therefore one should consider that FE to CIC data transmission will not be a problem for phase II.

R15	0,01	0,00	0,00	0,00	0,00				0,00	0,00	0,00	0,00	0,01	R15
R14	0,00	0,05	0,00	0,02	0,00	L6	0,19	L6	0,00	0,02	0,00	0,05	0,00	R14
R13	0,00	0,00	0,00	0,00	0,00				0,00	0,00	0,00	0,00	0,00	R13
R12	0,02	0,00	0,01	0,00	0,00	L5	0,13	L5	0,00	0,00	0,01	0,00	0,02	R12
R11	0,00	0,01	0,01	0,00	0,00				0,00	0,00	0,01	0,01	0,00	R11
R10	0,07	0,03	0,02	0,05	0,11	L4	0,16	L4	0,11	0,05	0,02	0,03	0,07	R10
R9	0,01	0,00	0,01	0,02	0,02				0,02	0,02	0,01	0,00	0,01	R9
R8		0,01	0,06	0,00	0,02	L3	0,08	L3	0,02	0,00	0,06	0,01		R8
R7		0,01	0,04	0,03	0,00				0,00	0,03	0,04	0,01		R7
R6		0,02	0,06	0,04	0,04	L2	0,22	L2	0,04	0,04	0,06	0,02		R6
R5			0,04	0,07	0,06				0,06	0,07	0,04			R5
R4			0,20	0,14	0,06	L1	1,14	L1	0,06	0,14	0,20			R4
R3				0,40	0,20				0,20	0,40				R3
R2					0,49				0,49					R2
R1					2,24				2,24					R1
	D5-	D4-	D3-	D2-	D1-	BARREL			D1+	D2+	D3+	D4+	D5+	

Figure 5: Proportion of good stubs lost after the CBC/MPA chips (in %), for PU200 events trigger sequences, using the 2GeV/c tight stub tuning.

R15	0,00	0,00	0,00	0,00	0,00				0,00	0,00	0,00	0,00	0,00	R15
R14	0,00	0,00	0,00	0,00	0,00	L6	0,09	L6	0,00	0,00	0,00	0,00	0,00	R14
R13	0,01	0,00	0,00	0,07	0,00				0,00	0,07	0,00	0,00	0,01	R13
R12	0,00	0,00	0,00	0,00	0,00	L5	0,06	L5	0,00	0,00	0,00	0,00	0,00	R12
R11	0,00	0,00	0,05	0,00	0,00				0,00	0,00	0,05	0,00	0,00	R11
R10	0,03	0,00	0,01	0,00	0,00	L4	0,08	L4	0,00	0,00	0,01	0,00	0,03	R10
R9	0,00	0,03	0,01	0,00	0,00				0,00	0,00	0,01	0,03	0,00	R9
R8		0,00	0,00	0,03	0,00	L3	0,04	L3	0,00	0,03	0,00	0,00		R8
R7		0,01	0,00	0,02	0,01				0,01	0,02	0,00	0,01		R7
R6		0,01	0,01	0,00	0,03	L2	0,08	L2	0,03	0,00	0,01	0,01		R6
R5			0,02	0,02	0,05				0,05	0,02	0,02			R5
R4			0,06	0,04	0,03	L1	0,61	L1	0,03	0,04	0,06			R4
R3				0,21	0,12				0,12	0,21				R3
R2					0,06				0,06					R2
R1					0,41				0,41					R1
	D5-	D4-	D3-	D2-	D1-	BARREL			D1+	D2+	D3+	D4+	D5+	

Figure 6: Proportion of good stubs lost after the CBC/MPA chips (in %), for PU200 events trigger sequences, using the 3GeV/c stub tuning.

3.4 CIC losses

Losses estimates after the CIC, for the 2GeV/c tight tuning, LP-SEC scenario, and PU200 events, are presented on Fig. 7:

R15	0,01	0,00	0,00	0,00	0,00				0,00	0,00	0,00	0,00	0,01	R15
R14	0,00	0,05	0,00	0,02	0,00	L6	0,19	L6	0,00	0,02	0,00	0,05	0,00	R14
R13	0,00	0,00	0,00	0,00	0,00				0,00	0,00	0,00	0,00	0,00	R13
R12	0,02	0,00	0,01	0,00	0,00	L5	0,14	L5	0,00	0,00	0,01	0,00	0,02	R12
R11	0,00	0,01	0,01	0,00	0,00				0,00	0,00	0,01	0,01	0,00	R11
R10	0,07	0,03	0,02	0,05	0,11	L4	0,17	L4	0,11	0,05	0,02	0,03	0,07	R10
R9	0,02	0,01	0,01	0,02	0,02				0,02	0,02	0,01	0,01	0,02	R9
R8		0,02	0,06	0,00	0,02	L3	0,11	L3	0,02	0,00	0,06	0,02		R8
R7		0,03	0,08	0,04	0,00				0,00	0,04	0,08	0,03		R7
R6		0,14	0,10	0,08	0,05	L2	1,67	L2	0,05	0,08	0,10	0,14		R6
R5			0,48	0,21	0,21				0,21	0,21	0,48			R5
R4			3,56	1,51	0,53	L1	27,24	L1	0,53	1,51	3,56			R4
R3				15,78	7,82				7,82	15,78				R3
R2					23,24				23,24					R2
R1					57,71				57,71					R1
	D5-	D4-	D3-	D2-	D1-	BARREL			D1+	D2+	D3+	D4+	D5+	

Figure 7: Proportion of good stubs lost after the CIC chips (in %), for PU200 events trigger sequences, using the 2GeV/c tight stub tuning and LP-SEC scheme.

It is interesting to compare those values to the ones of Fig. 5. Indeed, on Fig. 7, overall losses (FE+CIC) are given. Therefore, if for a given area losses on both Figures are equals, it means that there are no losses at the CIC level.

From this comparison one can conclude that LP-SEC scenario is sufficient for barrel layers 3 to 6 and rings 6 to 15 of all the disks.

The situation is also quite acceptable in ring 5 and barrel layer 2, where going to the LP-LEC scenario is sufficient. However, one observes a strong degradation for the innermost layers. In particular nearly 60% of the good stubs of disk rings 1 are lost at the CIC stage, which is clearly not acceptable.

R15	0,01	0,00	0,00	0,00	0,00				0,00	0,00	0,00	0,00	0,01	R15
R14	0,00	0,05	0,00	0,02	0,00	L6	0,19	L6	0,00	0,02	0,00	0,05	0,00	R14
R13	0,00	0,00	0,00	0,00	0,00				0,00	0,00	0,00	0,00	0,00	R13
R12	0,02	0,00	0,01	0,00	0,00	L5	0,13	L5	0,00	0,00	0,01	0,00	0,02	R12
R11	0,00	0,01	0,01	0,00	0,00				0,00	0,00	0,01	0,01	0,00	R11
R10	0,07	0,03	0,02	0,05	0,11	L4	0,16	L4	0,11	0,05	0,02	0,03	0,07	R10
R9	0,02	0,01	0,01	0,02	0,02				0,02	0,02	0,01	0,01	0,02	R9
R8		0,01	0,06	0,00	0,02	L3	0,08	L3	0,02	0,00	0,06	0,01		R8
R7		0,01	0,08	0,03	0,00				0,00	0,03	0,08	0,01		R7
R6		0,02	0,06	0,04	0,04	L2	0,22	L2	0,04	0,04	0,06	0,02		R6
R5			0,04	0,07	0,06				0,06	0,07	0,04			R5
R4			0,20	0,14	0,06	L1	1,30	L1	0,06	0,14	0,20			R4
R3				0,39	0,06				0,06	0,39				R3
R2					0,51				0,51					R2
R1					10,68				10,68					R1
	D5-	D4-	D3-	D2-	D1-	BARREL			D1+	D2+	D3+	D4+	D5+	

Figure 8: Proportion of good stubs lost after the CIC chips (in %), for PU200 events trigger sequences, using the 2GeV/c tight stub tuning and 10G-LEC scheme.

Figure 8 shows the losses estimates for the 10G-LEC scenario. The situation is clearly better, but there is still some tension for the 3 innermost rings and for barrel layer 1. For those modules, it is necessary to go to 3GeV/c threshold, thus confirming the front-end results. The outcome of the threshold increase on the 10G-LEC scenario is shown on Fig. 9.

R15	0,00	0,00	0,00	0,00	0,00				0,00	0,00	0,00	0,00	0,00	R15
R14	0,00	0,00	0,00	0,00	0,00	L6	0,09	L6	0,00	0,00	0,00	0,00	0,00	R14
R13	0,01	0,00	0,00	0,07	0,00				0,00	0,07	0,00	0,00	0,01	R13
R12	0,00	0,00	0,00	0,00	0,00	L5	0,06	L5	0,00	0,00	0,00	0,00	0,00	R12
R11	0,00	0,00	0,05	0,00	0,00				0,00	0,00	0,05	0,00	0,00	R11
R10	0,03	0,00	0,01	0,00	0,00	L4	0,08	L4	0,00	0,00	0,01	0,00	0,03	R10
R9	0,00	0,03	0,01	0,00	0,00				0,00	0,00	0,01	0,03	0,00	R9
R8		0,00	0,00	0,03	0,00	L3	0,04	L3	0,00	0,03	0,00	0,00		R8
R7		0,01	0,00	0,02	0,01				0,01	0,02	0,00	0,01		R7
R6		0,01	0,01	0,00	0,03	L2	0,08	L2	0,03	0,00	0,01	0,01		R6
R5			0,02	0,02	0,05				0,05	0,02	0,02			R5
R4			0,06	0,04	0,03	L1	0,61	L1	0,03	0,04	0,06			R4
R3				0,21	0,12				0,12	0,21				R3
R2					0,06				0,06					R2
R1					0,48				0,48					R1
	D5-	D4-	D3-	D2-	D1-	BARREL			D1+	D2+	D3+	D4+	D5+	

Figure 9: Proportion of good stubs lost after the CIC chips, for PU200 events trigger sequences, using the 3GeV/c stub tuning and 10G-LEC scheme.

On this plot one get back all the values of Fig. 6, thus showing that there are no more losses at the CIC level.

3.5 Summary

The results obtained on trigger block losses estimates show that if some irreducible losses at the FE level seems unavoidable, lossless CIC transmission up to PU200 looks possible. For this, the configuration shown on Fig. 10, where 3 means a 3GeV/c threshold, should be applied.

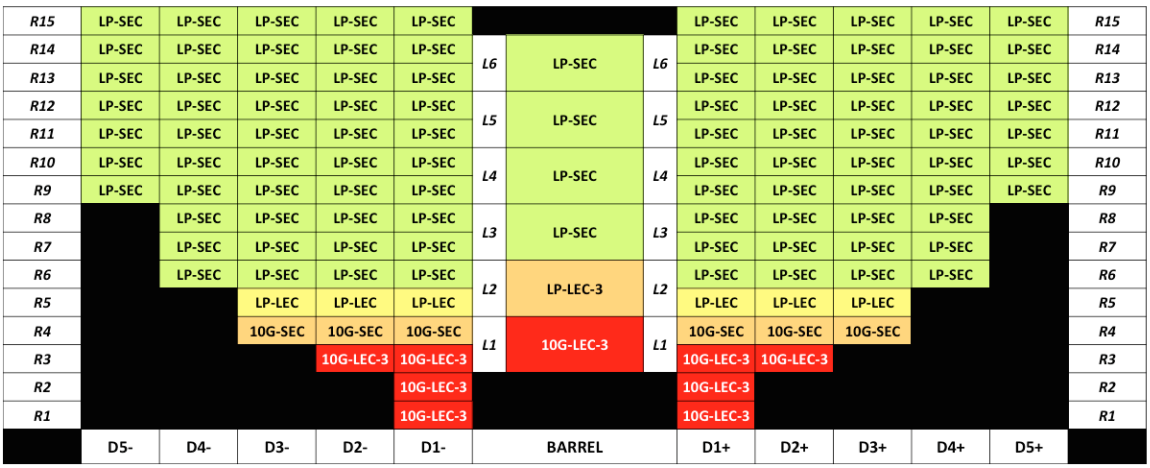

Figure 10: Recommended CIC output scheme for a lossless transmission at PU200.

4 L1 block transmission

4.1 How losses are measured?

Contrary to the trigger block, the L1 data transmission is asynchronous. The loss definition will therefore be completely different. An L1 event can be extracted from the CIC only when it's reception in the CIC has been completed. The total number of clusters in the word, provided in the L1 word header, is indeed known only at the end of the processing. The length of the L1 word depends on these numbers, and the DAQ must know them to process the L1 event. The CIC therefore contains a FIFO in which a certain amount of L1 events can be stored.

CIC FIFO will be able to store more than one L1 event. Indeed, event $n+1$ must be stored in the FIFO until event n transmission has been completed, moreover if event $n-1$ has not been transmitted, and so on. The key parameter for estimating the L1 losses is the time spent by the L1 event in the CIC. This period, called Δ_{CIC}^{L1} is very simply defined as the difference between the clock cycle at which it enters the CIC (Clk_{CIC}^{in}) and the clock cycle at which the last L1 block of this event goes out of the CIC (Clk_{CIC}^{out}):

$$\Delta_{CIC}^{L1} = Clk_{CIC}^{out} - Clk_{CIC}^{in}$$

The evolution of this parameter as a function of time is the observable we are looking for. Indeed, if Δ_{CIC}^{L1} is increasing against time, it means that the CIC FIFO size is also increasing regularly and that one will reach a point where the FIFO is full. In this case, any L1 event trying to enter the CIC will be rejected, and one will start to loose data. We assume that for a given L1A frequency, the evolution of Δ_{CIC}^{L1} is linear. Therefore we measure the drift by fitting the following linear function:

$$\Delta_{CIC}^{L1}(Clk) = drift \cdot Clk + \Delta_{CIC}^{L1}(0),$$

, where Clk is the clock cycle number (one cycle every 25ns), and $\Delta_{CIC}^{L1}(0)$ is approximately the time taken to extract the first L1 event.

Of course the evolution of this observable will be directly related to the rate of L1 accepts signals in CMS. The number of incoming L1 events will be different at a rate of 100kHz than at 1MHz. It will also depend on PU, as more clusters will be reconstructed at PU200 than at PU140. All these parameters are computed directly by the FE_ana tool. All the results presented below were obtained using a sequence of 50000 clock cycles, among which L1 accept signal are randomnly distributed at frequency between 100kHz and 1MHz. We consider that there are losses if the value of $drift$ is not compatible with 0.

4.2 L1 words size

Apart from the CBC chips, which are transmitting unsparsified L1 data, FE chips will have to deal with sparsified data. It means that L1 words of variable size will have to be temporarily stored before being extracted. The size and depth of this storage area (FIFO) must be adapted to the needs of the system.

Before doing any further L1 losses studies, we will estimate the best FIFO size for MPA and CIC, using PU200+4tops events.

4.2.1 MPA FIFO size and depth

The L1 clusters multiplicity at the MPA level, measured for 100 PU200+4tops events, is shown on Fig. 11. The 31 clusters limit is never reached for strip clusters, and very rarely reached for pixel clusters (less than 1ppm).

This first observation confirms that the size of the cluster multiplicity fields in the MPA L1 word is correctly set. Concerning the size of the sparsified L1 word, result is shown on Fig. 12. Here the 31 clusters limits are applied, but as one can see, the theoretical 787 bits limits is far from being reached. Only 1 word out of 10 millions is larger than 500 bits.

Therefore, an MPA FIFO size of 550 (500+10% safety) bits would be sufficient to ensure a lossless data transmission. This means that CIC FIFO size would be 550*8=4400 bits.

Concerning the depth of the FIFO, the value 5 seems appropriate for the whole detector, but more complete studies are necessary, in particular for the innermost rings of the last disks.

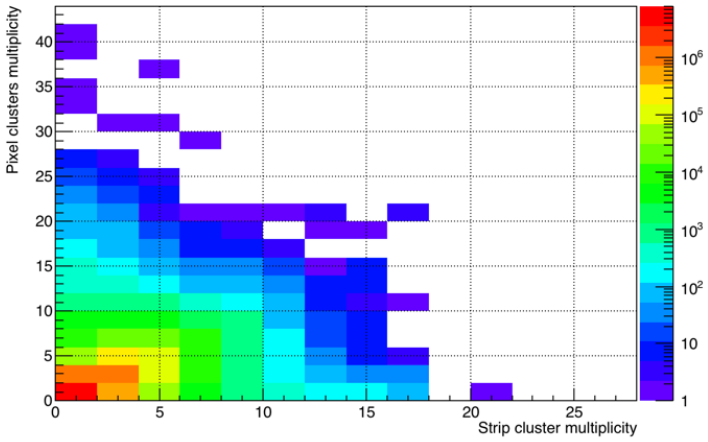

Figure 11: MPA L1 data cluster multiplicities, for PU200+4tops events

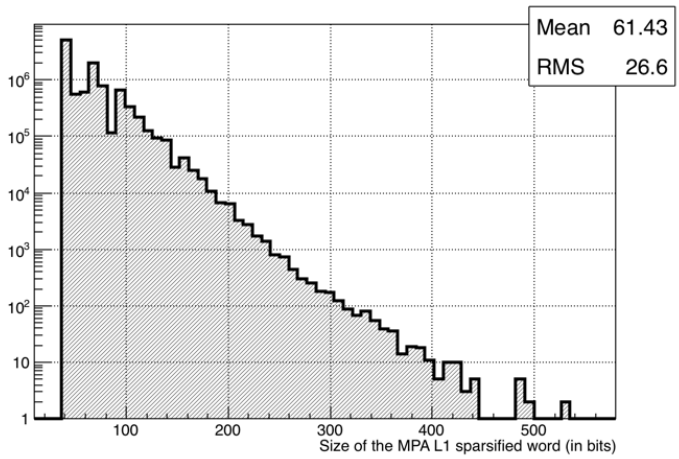

Figure 12: Size of the MPA L1 sparsified words, for PU200+4tops events

4.2.2 CIC FIFO size

As usual, the CIC situation should be more complex, as the data from eight chips is gathered in there. First of all, one has to check the cluster multiplicities.They are shown on Figs. 13 and 14, for PS and 2S modules respectively.

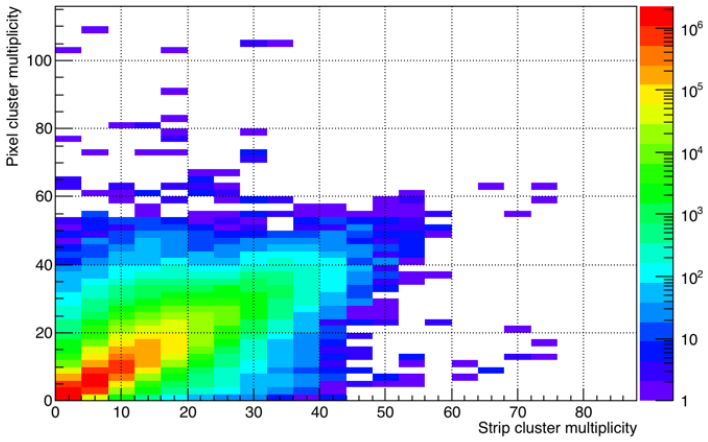

Figure 13: CIC PS L1 data cluster multiplicities, for PU200+4tops events

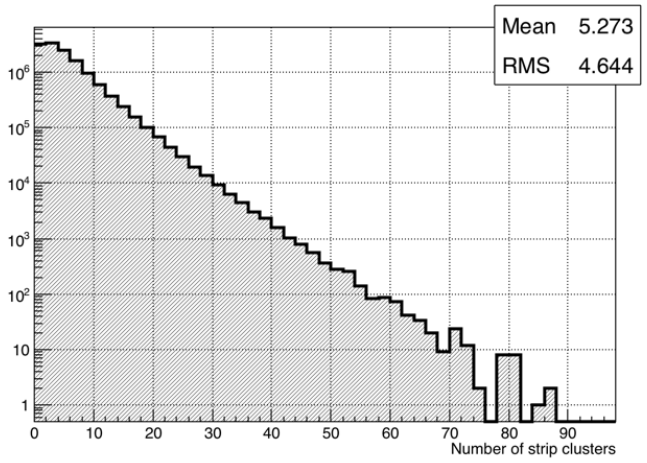

Figure 14: CIC 2S L1 data cluster multiplicities, for PU200+4tops events

First observation is that the 31 clusters limit is no longer valid in the CIC. 63 seems more reasonable for the PS modules, but not fully sufficient for the 2S. The proportion of CIC chips with a large L1 word, for different thresholds, is summarized in Table 1

Module type	PS	2S	Max th. PS size (in bits)	Mas th. 2S size (in bits)
31 clusters max	0.18	0.16	975	474
63 clusters max	0.0006	0.0009	1999	860
127 clusters max	0	0	3985	1693

Table 1: Proportion of CIC chips with large L1 word, in %, and corresponding maximum L1 word size, in bits

The proportion of CIC chips reaching the 63 clusters limit is very small. However, as it adds only few bits to the global payload, we will use the 127 clusters limits in the following. In this configuration, the size of the L1 words is shown on Figs. 15 and 16, for PS and 2S modules respectively.

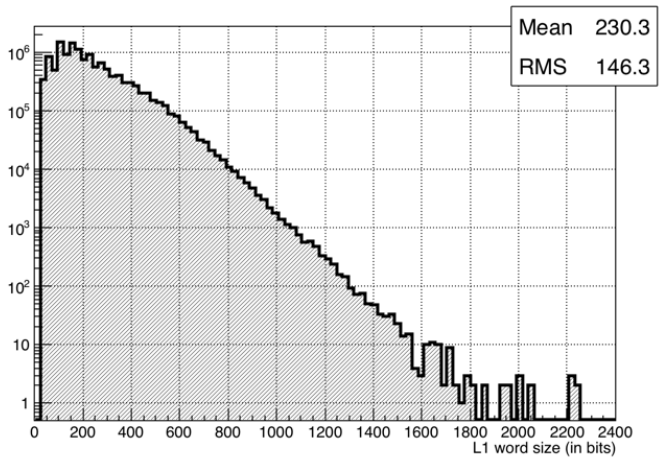

Figure 15: CIC PS L1 data sizes, for PU200+4tops events

As one can see, in any case the size of the FIFOs (550 bits per input chip) in the CIC will be sufficient to handle all the events (it will be by construction in the MPA anyway).

4.3 CIC L1 data losses

The average FIFO drift values for barrel modules, at PU200+4tops events and an L1 rate of 750kHz, are shown on Fig. 17. The corresponding result for the disks is presented in Fig. 18. Results are shown for a baseline

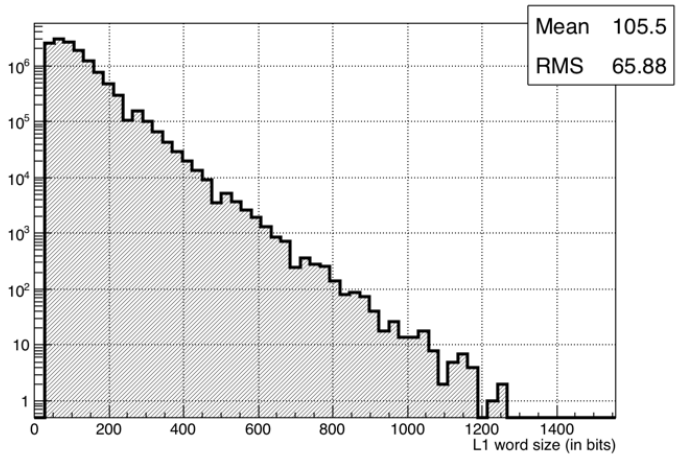

Figure 16: CIC 2S L1 data size, for PU200+4tops events

transmission scheme of LP-GBT. Therefore the amount of L1 data extracted per CIC block is equal to 64 bits for all the modules.

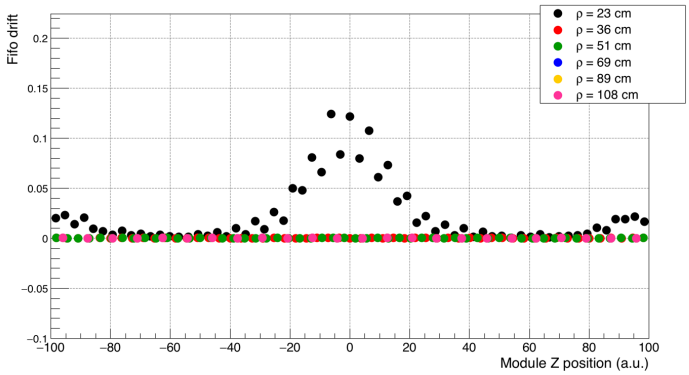

Figure 17: Average L1 FIFO drift value in the tracker barrel, fur PU200+4tops events, with an average L1 rate of 750kHz

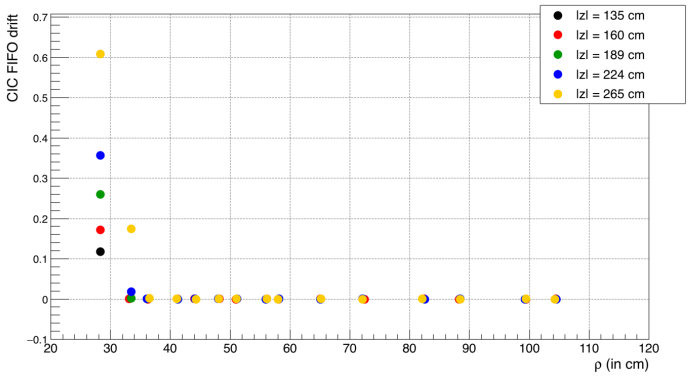

Figure 18: Average L1 FIFO drift value in the tracker disks, fur PU200+4tops events, with an average L1 rate of 750kHz

Contrary to the trigger case, there is only one problematic barrel layer in the L1 case: the innermost one. Looking at the endcap rings one reach the same conclusion, only the innermost rings shows a problematic behavior. For the endcap, contrary to the trigger, one has to take into account all the modules. Therefore, inner rings of the outer disks, are also included. Those parts of the detector are receiving larger data rate, and it is therefore not surprising to see that the largest drift is observed for the innermost ring of the last disk.

It is important to note that all drifts disappear if one goes to 10G transmission scheme (128 bits per block). Eventually, one sees that modules requiring a 10G transmission are the same than for the trigger. Therefore, the recommendations of Fig. 10 also stands for L1.

Concerning the depth of CIC FIFO, the value of 10 is appropriate for all the modules except for the innermost rings of the last disks. For these modules there is still some tension, as one can see on Fig. 19, where the number of events stored in the CIC as a function of the BX ID is shown.

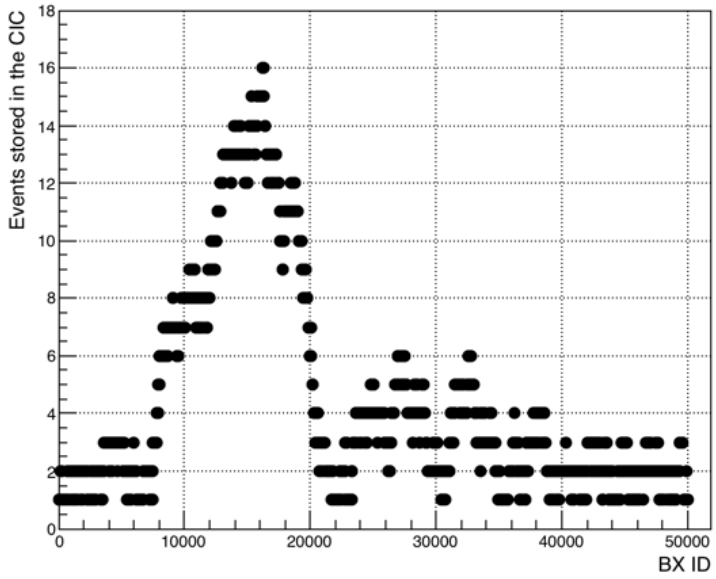

Figure 19: CIC FIFO necessary depth as a function of the BX ID, for a module belonging to the innermost ring of disk 5.

This plot shows that a larger depth will be necessary for those modules (20 per disk). One could also imagine to allocate more bandwidth to L1 only for those modules (which are not transmitting any trigger info).

5 Conclusion

In this document we presented a method to estimate the transmission efficiency of the future CMS tracker frontend chain. The bottleneck of this chain is by construction the CIC chip, where the data troughput must be reduced by one order of magnitude. The feasibility of such a rate reduction is strongly relying on the fact that tracker occupancy will remain sufficiently low, even in very high pile up condition.

The results presented in this note shows that the new baseline data transmission scenario from the GBT is sufficient for most of the future tracker modules. It also shows that high rate transmission scheme are sufficient for the innermost parts, where rates are larger. There is possibly one remaining source of tension at L1 in the innermost ring of the external disks (concerning about 40 modules) which will have to be addressed.

Results presented here are by no means definitive, they should just be considered as a starting point for the coming studies. Simulation improvement (more realistic geometry, digitization, pile-up tuning with 13TeV data,...) will help refining these estimations in the future.

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