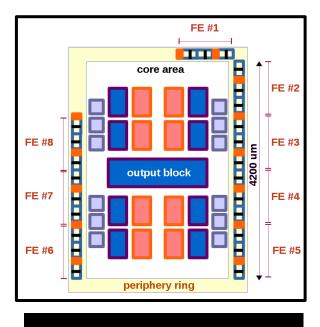


CIC status



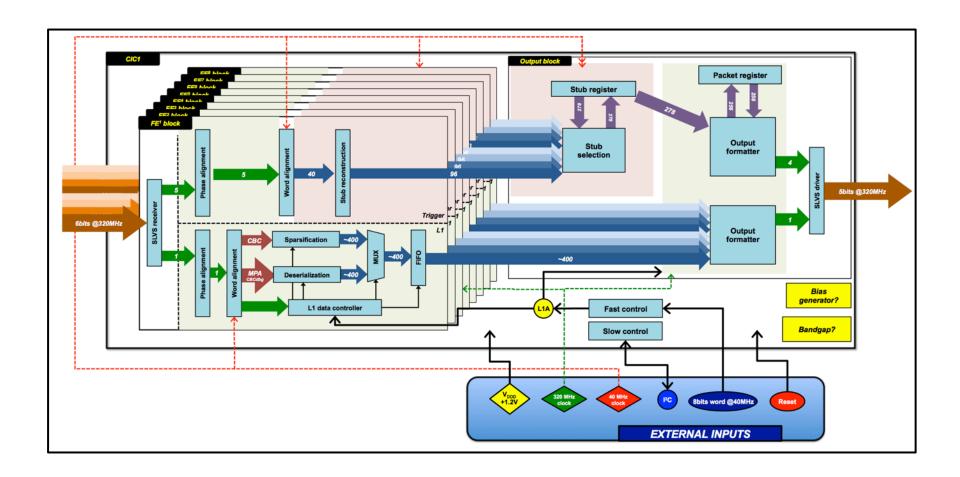


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Chip status



$\rightarrow \textbf{CIC1 block diagram:}$



2 S. Viret

1. Chip status





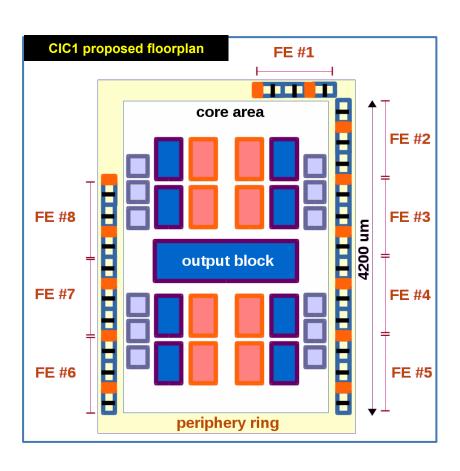
→ Model status and tests:

- → Inclusion of the pattern generator. I²C slave about to be added.
- → Addition of de-skewing capability for each input line (*necessary in addition to the phase aligner*).
- → Test tool from CMSSW stimuli was fully automatized (*python framework*), in order to speed up the verification process
- → Started to evaluate the model porting from SysVerilog to Verilog in order to use CERN triplication tool.

3 S. Viret



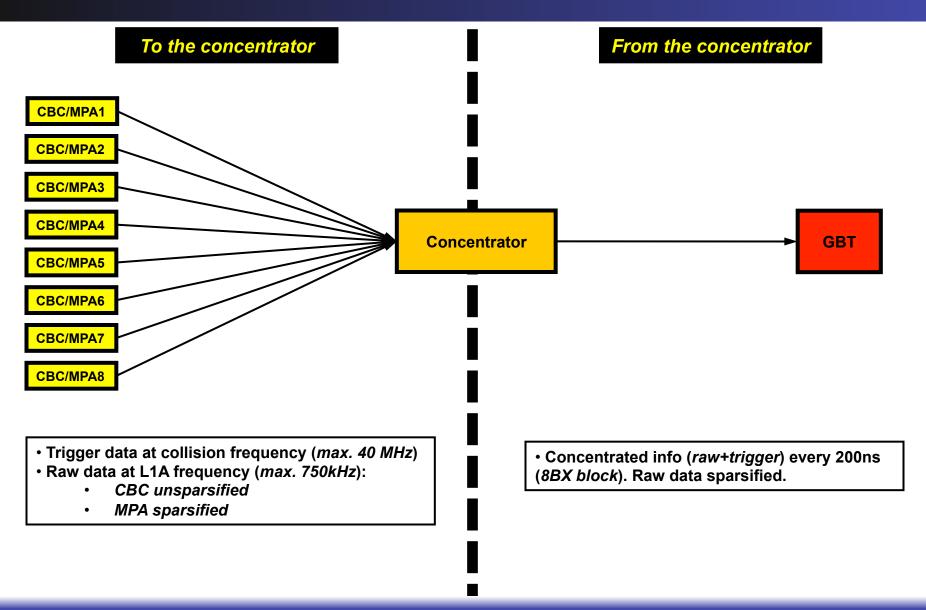
→ Model and design status:



- → Synthesis of 1FE block (core+FIFO) done.
- → Need to add the phase aligner block (have to check if the block designed for the GBT can be used as it stands).
- → Concerning the design, most of the technical points raised during the review have been solved.
- → Remaining points still have to be addressed (*eg ESD pads*)

4 S. Viret







→ The data transmission requirements:

→ Raw data (L1) block:

- Full raw data transmission up to 750kHz (max acceptable L1A rate)
- No loss accepted (<0.1%)

→ <u>Trigger block:</u>

- Full trigger data (stubs) transmission up to 40MHz
- ~90% of the stubs transmitted are not used by the L1 track trigger, we can/should accept losses on them.
- We cannot accept too many losses (<1%) on the remaining stub (aka good stubs, coming from particles with p_T >2GeV/c, d_0 <5mm).

→Documentation available on the sharepoint:

 \rightarrow Analyse of the potential data transmission losses:

https://espace.cern.ch/Tracker-Upgrade/Electronics/CIC/Shared%20Documents/Simulation%20studies/FE_inneff_2.pdf

→ CIC I/O data formats:

https://espace.cern.ch/Tracker-Upgrade/Electronics/CIC/Shared%20Documents/Data%20formats/CIC_IO_Formats_v5.pdf

→ CIC1 specification document:

https://espace.cern.ch/Tracker-Upgrade/Electronics/CIC/Shared%20Documents/Specifications/CIC_specs_v1.1.pdf