Migration from GLIB to FC7

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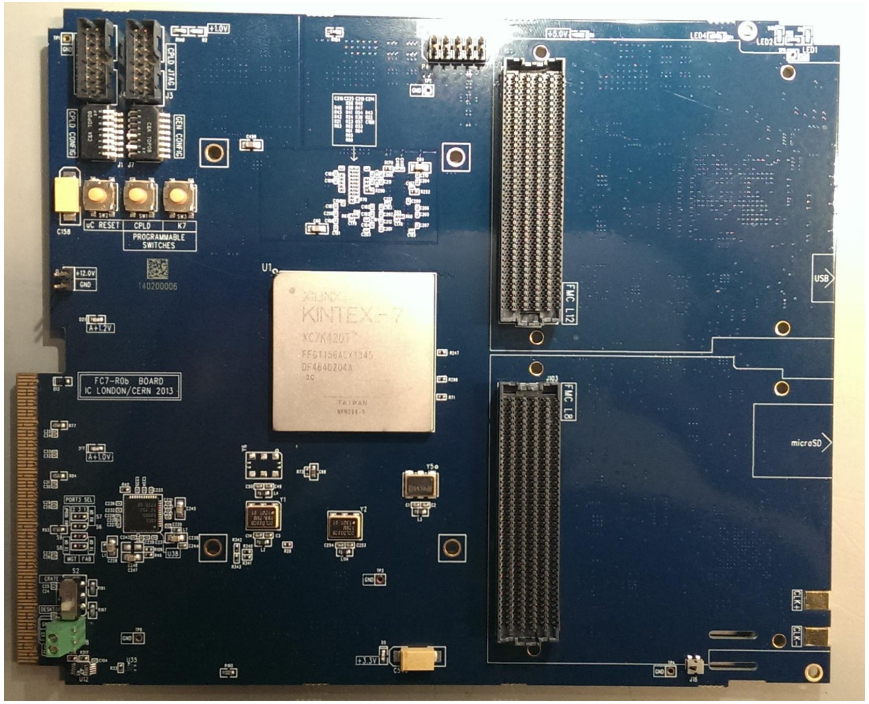
GLIB and FC7



GLIB (Gligabit Link Interface Board)

- FPGA **Virtex 6** (~130k logic cells)
- **4 I/O SFP+ native** up to 6.5 Gbps (were used to connect 2 GLIBs)
- Port **Gbit Ethernet**: 1 Gbps with IPBUS
- µTCA connector
- 2*72Mb **SRAM** (static)
- 2 FMC slot supporting **HPC** mezzanines

FC7 (FMC carrier - Xilinx Series 7)

- FPGA **Kintex 7** (~420k logic cells)
- **No native SFP+** cages
- **No port Gbit** Ethernet
- µTCA connector
- 4 Gb **DDR-3 RAM** (dynamic)
- 2 FMC slots supporting **LPC** mezzanines, located on the same side (front side of xTCA crates)
- µSD card to select f/w versions, I2C values…

Reminder on GLIB firmware

GLIB firmware for CBC2: https://svnweb.cern.ch/cern/wsvn/cmsptdaqup/

GLIB base system blocks

- **FMCs requirements**
- **IPBus communication**
- **CORE DAQ block**
- **GBT emulation block**

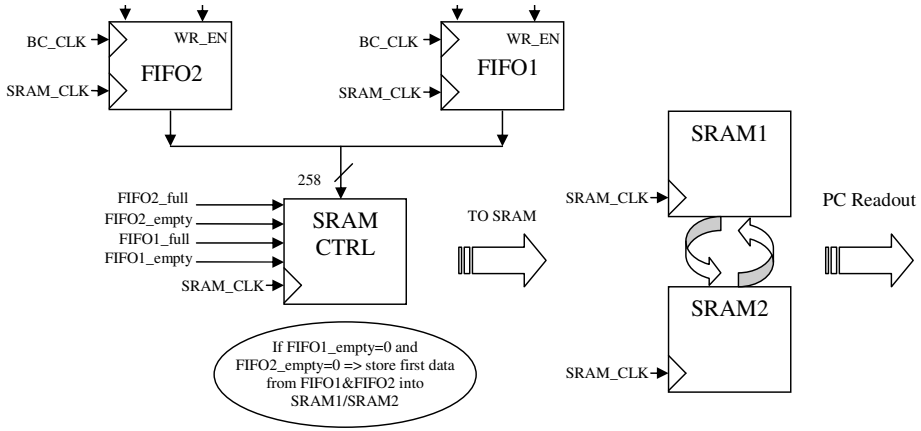
I2C Read/Write management block

- In GLIB firmware, I2C transactions are written in RAM (to save space on FIFO)
- **Write mode**
  - Write in GLIB RAM bank all the identifiers (I2C address + value to write), describing the write operations to be performed
  - Trigger write action on board
- **Read mode**
  - Write in GLIB RAM bank all the identifiers (I2C address), describing the read operations to be performed
  - Trigger read action on board
  - Read back I2C values from GLIB RAM bank

Reminder on GLIB firmware

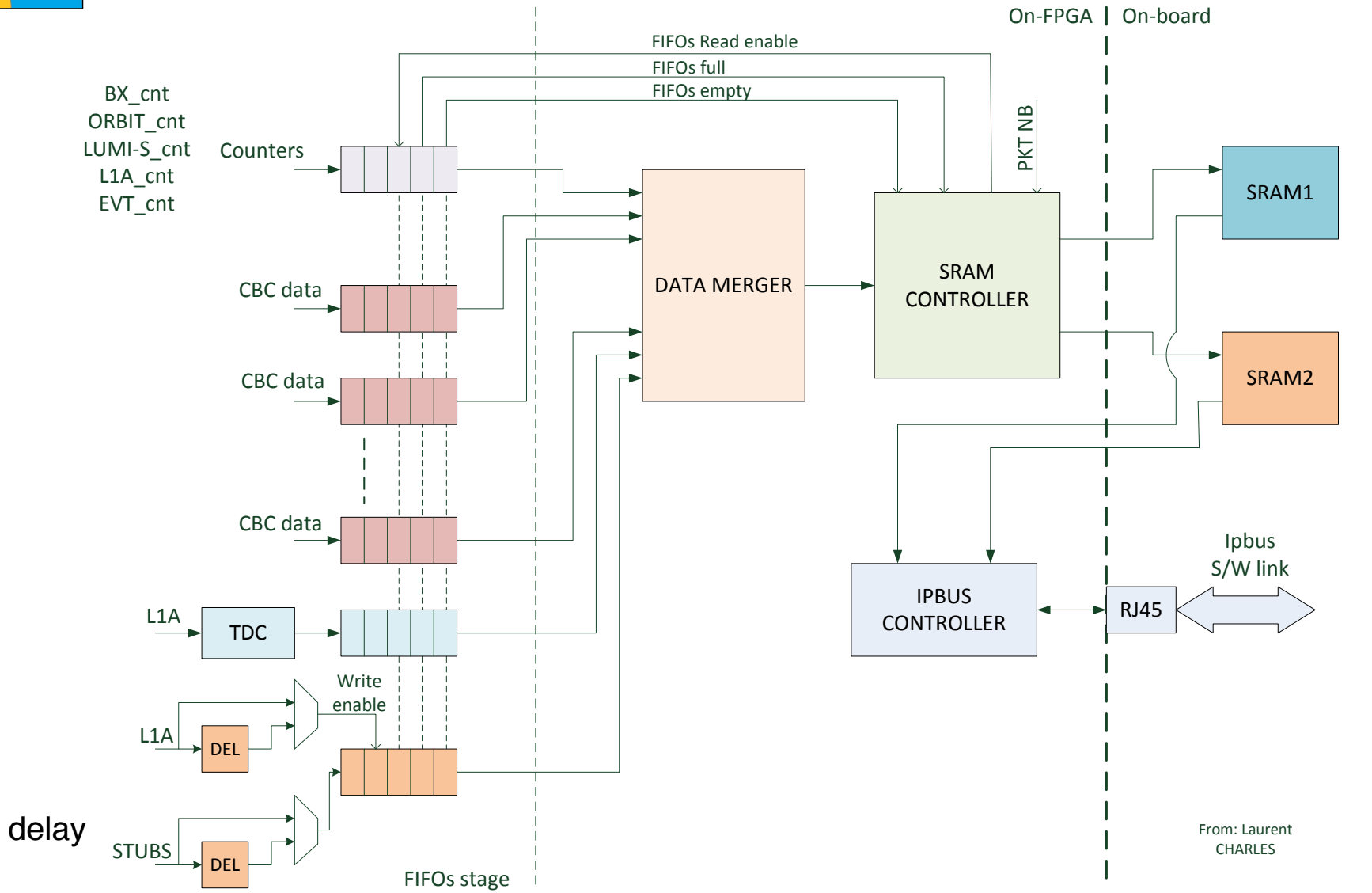
Data readout block

- **Trigger start_daq** action on board
- **Mode storage in continue** (simultaneous read write) using **two GLIB RAM banks**:
  - Data read out from FE are stacked into GLIB RAM bank 1
  - When GLIB RAM bank 1 is full
    - Data read out are stacked into GLIB RAM bank 2
    - In parallel, software reads out content of GLIB RAM bank 1
  - When GLIB RAM bank 2 is full
    - Data read out are stacked into GLIB RAM bank 1
    - In parallel, software reads out content of GLIB RAM bank 2



- All readout cycles are based on a synchronization/handshake mechanism between software and firmware
- In case software readout is too slow, trigger is back pressured: no data loss

GLIB functional diagram



Migrating GLIB firmware to FC7

I2C Operations:

- Critical point: **write operations**
- I2C transactions will not transit via RAM memory anymore (more FIFO available)
- Cannot use experience from Phase I, since TK-FEC does not configure I2C registers
- Address of registers changed. Needs update and testing (middleware side)
- Broadcasting + 1 MHz I2C to be implemented.

Core DAQ block:

- Experience with Phase I TK-FED. To be applied to phase II.
- **Simultaneous data read/write** on DDR-3 validated on FC7. Proven to work for Phase I.
- Middleware compatibility with GLIB will be preserved when possible (expected most of the time)

New possible functionalities

New options for I2C Operations:

- **I2C operations in parallel with data taking**:
  - With GLIB f/w, the same RAM banks were used for I2C and data readout, they were mutually exclusive
  - Can be directly written to FIFO since more FIFO available in FC7
- Add **read-back** once write done (would have been useful at Nov BT with 2 GLIBs) + write again if wrong value

New options for Data read out

- Further splitting in **several memory banks** inside RAM is possible.
  - Would it help to reduce dead time ? Needs to be tested.
- **Commissioning loop** directly in the firmware: make faster CBC calibration procedure. Does not need to readout full event.
- Option to **trigger data acquisition on stubs**

Test system on crate

FC7 does not have Gbit Ethernet port

- How to send the data to software ?
- If one wants **IPBUS** communication (e.g. for beam test), it has to go through the crate backplane: data readout through crate MCH1 slot
- Can also use **FEROL** card (link to CMS central DAQ)
  - No FEROL FMC (as far as we know), a FMC with SFP+ would work
  - slot MCH2 with AMC13 (has optical output 10 Gbps)

Trigger and clock:

- Until now in beam test, trigger from TLU through **FMC DIO-5**
  - Feasible for one FC7 card on crate, not possible for many FC7
  - Options to distribute clock on half a crate from one FC7+DIO-5: to be investigated
- **CMS Trigger Timing and Control system:**
  - CERN designed a TTC FMC for GLIB (high pin count mezzanine). Could be tested with FC7 (low pin count)
  - TTC support from back-plane is preferred over TTC FMC. AMC13 ?

Every change of architecture needs firmware development

Longer term plans

FC7 for CBC3/MPA + CIC

- **Reading out CIC data ?**
  - CIC prototype available by the end of 2016
  - 2 CIC chips per module, input each 8 CBC3 / MPA chips
  - CIC output data sent to **LP-GBT**
    - LP-GBT (65nm) not yet finalized, connect with CIC through GBT (130nm) instead ?
    - LP-GBT emulator already in place
  - How to handle **CIC I2C** registers ? (e.g. CIC configuration, number of lost stubs)
  - How will change **data acquisition** ?
    - Adapt to CBC3 / MPA formatted by CIC
    - CIC output data generator is available for tests
  - How to handle **L1** data to Tk-finding, and L1 decision for data acquisition (final DTC) ?

Conclusions

Migration of base GLIB functionalities to FC7:

- Data readout already tried for Tk-FED Phase I, no problem foreseen
- I2C transactions with FIFO instead of SRAM: needs some work
- Timeline: will finalise when core work on Phase I will be done (April)

New possible functionalities:

- I2C: Broadcasting + I2C 1 MHz, control of write operation
- I2C in parallel with data taking
- Elements of commissioning loop in firmware
- Triggering data acquisition on stubs

Test systems

- All test systems on crate: action plan needed for data readout and TTC

FC7 for CBC3/MPA+CIC:

- Work can start on CIC data output
- Waiting for LP-GBT availability