CIC1 technical specification

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Draft version 0.99

03/06/2015

Revision log	
03/06/15	*Version 0.99:* first complete version of the document
01/06/15	*Version 0.9:* first draft version of the document

1 Context

Figure 1 presents a part of the layout of future CMS Phase II tracker. The blue and red lines are the modules of the outer tracker, which is the object of this document. The two colors are used to differentiate the two types of detection units used in the future detector. Blue modules, named PS modules, have an higher granularity than the red ones, named 2S modules. Therefore they provide higher precision hits in the innermost region of the tracker: the inner barrel (TIB) and endcaps (TICs). The corresponding outer parts, made of 2S modules, are called outer barrel (TOB) and outer endcaps (TOCs).

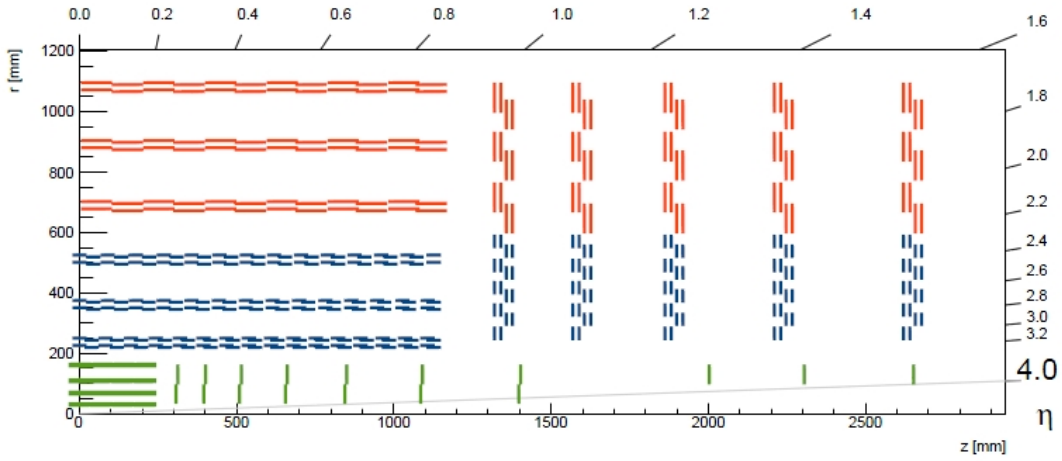

***Figure 1:* Sketch of one quarter of the Tracker Layout.**

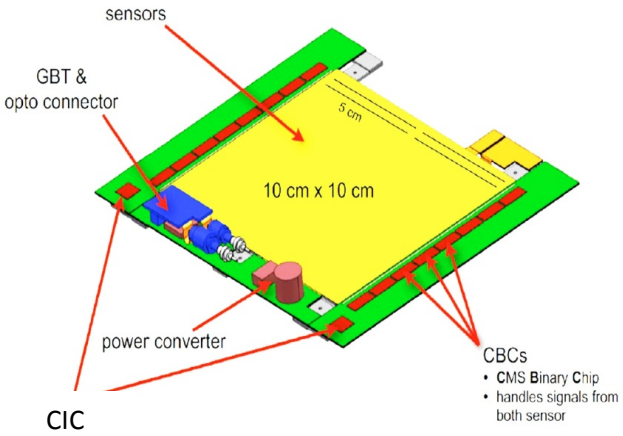

***Figure 2:* Outer module (2S)**

Figure 2 shows one of the two modules type: the 2S. Next to the yellow active area (silicon sensor), three hybrids host the module front-end electronic components. The sensor signals are collected on each side of the module via 2x8 front-end chips (CBC for the 2S, MPA for the PS). A CIC chip collects the digital data coming from each

group of 8 FE chips and transmits them to the GBT. There are therefore 2 CIC chips per module.

In order to minimize the noise induced by the large number of lines on the hybrid, all the lines between FE chips and CIC, and also between CIC and GBT, are differential (slvs). In order to limit the total number of lines their data rate is 320 Mbps. In CIC1 prototype, there will be 6 differential lines @320Mbps between each front end chip and the concentrator (48 lines in total), and 5 differential lines @320Mbps between each concentrator and the GBT (see Figure 3).

The concentrator I/O interface is adapted to the two FE chips (CBC / MPA), which are used in the two different module types (2S / PS). The CIC can switch between both formats via a simple configuration change.

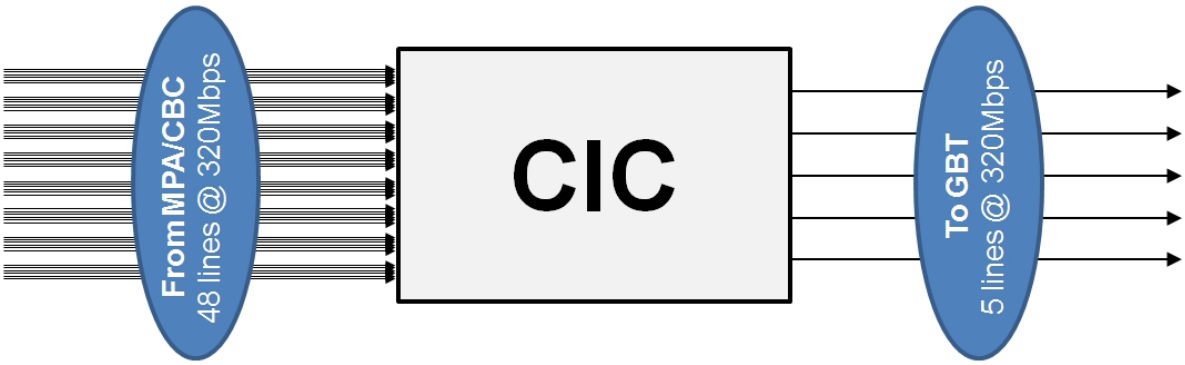

Figure 3: CIC block diagram.

FE chips are sending out two different data types:

- **Trigger data**: this data payload is produced at 40MHz and corresponds to the information necessary to the L1 track reconstruction system. It needs to be transmitted with minimum latency.
- **L1 data:** this data payload corresponds to the raw tracker data, and is sent on request each time an L1-accept signal is emitted by the CMS L1 global trigger decision unit. During LHC phase II, the CMS L1A rate might reach up to 1MHz.

2 Top level architecture

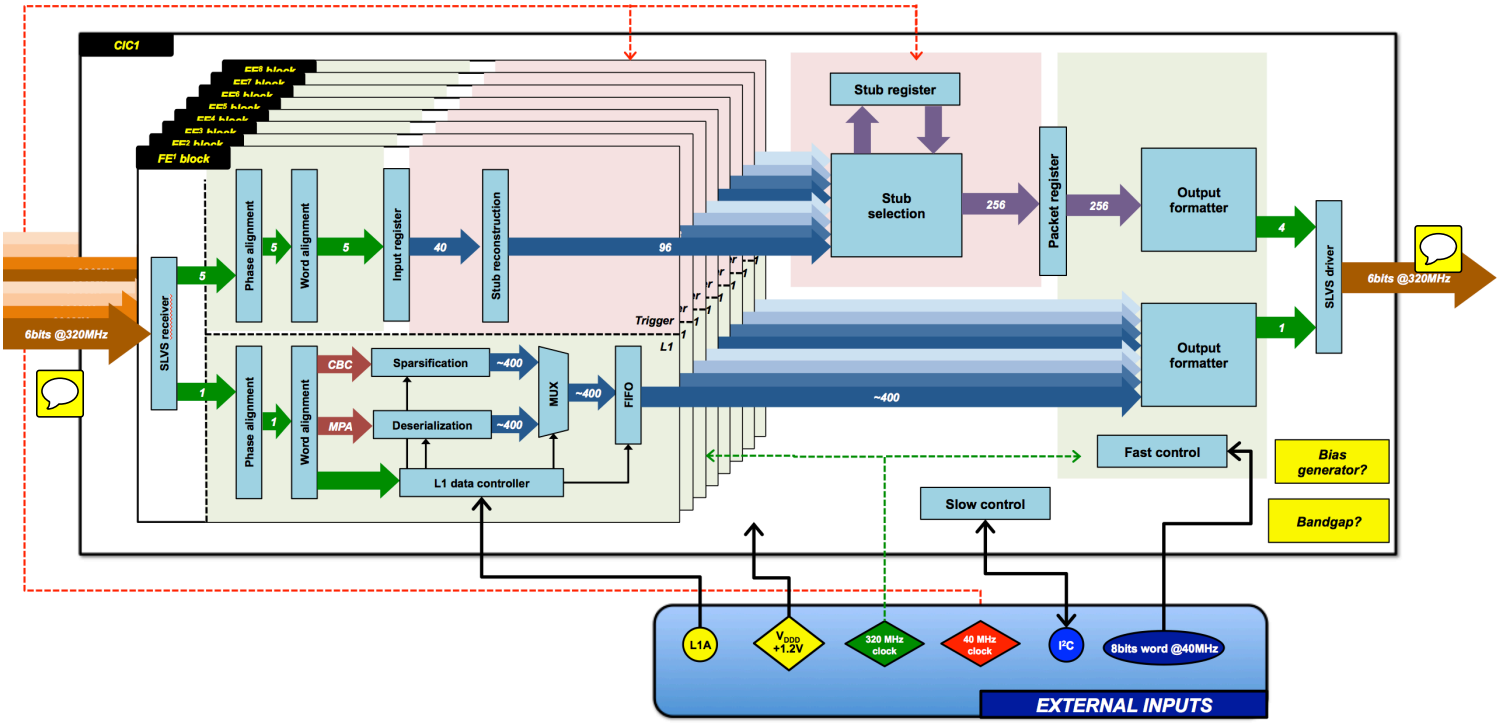

Figure 4: CIC1 block diagram.

The top-level architecture of CIC1 chip is presented on Fig.4. There are two main structures in the chip: the FE blocks, and the output block.

The FE blocks will perform the treatment of the data provided by the 8 FE chips feeding the CIC. There is one block per incoming chip. Each block will treat the trigger and L1 information separately. Whereas the treatment of the trigger information is the same for both FE chip type (*CBC and MPA*), three different modes will be possible for L1 data:

- **CBC sparsified:** the CBC L1 input will enter the CIC unsparsified. In order to reach the requested data compression factor at the CIC output, data sparsification will have to be performed in the block.
- **CBC deserialized:** this debug mode will allow transmitting raw CBC data out of the CIC, without any sparsification. This would work up to a given L1A rate (100kHz).
- **MPA deserialized:** MPA L1 information is already sparsified, there is therefore no specific treatment to apply to this data.

The output block will group the data retrieved from the 8 FE blocks, and format it in an output data packet. This block will perform stub selection.

CIC input/output (*I/O*) data formats considered to setup this document are taken from **[1].** For what concerns the CBC related information, we referred ourselves to the CBC3 specification document **[2].**

The rest of the document describes the different information of Fig.4 in details. The data treatment blocks are presented in part 3; external inputs are described in part 4. Power considerations are discussed in part 5, and finally, chip packaging is presented in part 6.

3 Data treatment

3.1 SLVS receivers

SLVS (*Sub-LVDS*) receivers IP blocks are being developed in TSMC 65nm in the framework of the GBT e-link. One differential receiver will be used for each of the 48 320Mbps input lines of the CIC1.

The design of this IP takes into account the harsh radiation environment and is carried out by the BG-PV INFN group. The voltage supply of the block is at 1.2V and its input common mode voltage will be between 550mV and 650mV.

A prototype of this block has already been tested at the moment of writing of this document and a modified design has been announced **[3].**

3.2 Phase alignment

Phase alignment is required in order to synchronize the signal incoming from the 6 lines of each MPA/CBC chip entering in the CIC.

It is planned to use the GBT phase aligner block (*which is currently ported to 65nm technology*) for this task.

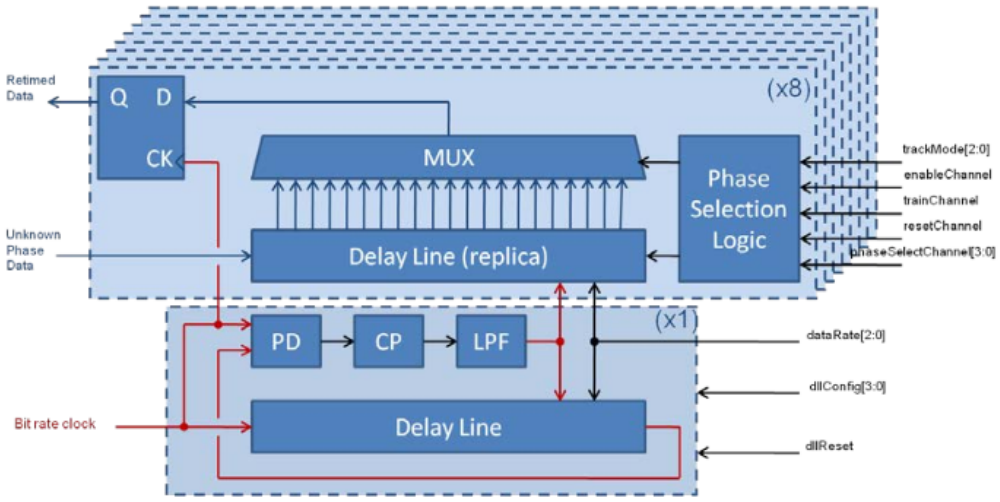

***Figure 5*: GBT phase alignment block**

Working principle of this block is sketched on Fig.5. It is made of 1 master DLL and 4 replica DLL, and is therefore sufficient to align four lines. We will use two such blocks for each FE block (*so 16 blocks for CIC1*), and adapt it to 6 input lines in the final chip.

It is planned to perform this alignment once, using normal patterns coming from CBC/MPA chips. But it will be possible to perform it again whenever necessary. To this end, the GBT phase alignment block can work in two modes:

- **Static phase selection**: the normal mode, used when the correction are known.
- **Initial training with learned static phase selection**: the initial mode, used to determine the correction at the detector startup.

3.3 Trigger path

3.3.1 Word alignment

The trigger information arriving from the FE chips is contained in 5 lines at 320MHz. The event payload received every 25ns is therefore made of 5 words of 8 bits. The format of this payload, for both FE chip flavors, is summarized in the CIC I/O format note. Each 40 bits block contains a synchronization bit, which has a constant value.

The main purpose of the word alignment block is to localize this synchronization bit in order to spot the beginning and the end of the packet and to align them with the 40MHz clock, as sketched on Fig.6

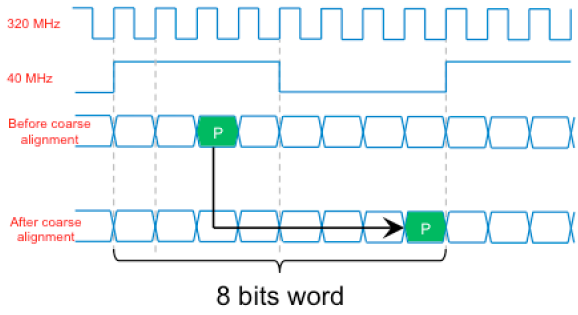

***Figure 6*: Word alignment principle**

The synchronization is located only on one line, but as all 5 lines are already phase aligned, one could consider that the word alignment correction will be the same for all the lines. It is therefore sufficient to perform the alignment only on the line receiving the synchronization bit. The alignment correction obtained is then applied to the 4 other lines.

As for the GBT phase aligner, the word aligner operates in two different modes: static phase selection and initial training.

3.3.2 Stub reconstruction

As seen on Fig.4, there is one stub reconstruction block per front-end chip, so 8 blocks per CIC.

Each stub reconstruction block receives 40 bits packets at 40MHz from the word alignment block. The synchronization bit position checked in every incoming packet (*should be always the same after the word alignment step*)

For MPA compatibility, the packets are processed by pairs at a frequency of 20MHz. In order to keep track of the stub origin, in particular for the CBC packets, an offset bit is affected to each stub recorded.

The size of the output is 96bits divided into six words of 16bits (*maximum stub length at this stage*). This is sufficient for both configurations (*maximum number of stubs arriving from the front-end for two BXs being 6 and 5 for the CBC and MPA respectively*).

The structure of the output register depends on the FE chip:

- ***CBC output register***

Structure of the stub output register for CBC configuration																
bit N°	***15***	***14***	***13***	***12***	***11***	***10***	***9***	***8***	***7***	***6***	***5***	***4***	***3***	***2***	***1***	***0***
stub N°1	**strip @**								**off**	**bend**				**x**	**x**	**x**
stub N°2	**strip @**								**off**	**bend**				**x**	**x**	**x**
stub N°3	**strip @**								**off**	**bend**				**x**	**x**	**x**
stub N°4	**strip @**								**off**	**bend**				**x**	**x**	**x**
stub N°5	**strip @**								**off**	**bend**				**x**	**x**	**x**
stub N°6	**strip @**								**off**	**bend**				**SO**	**EF**	**S**

  - **x**: not used
  - **SO** (***stub overflow***): corresponds to the logical OR of the SO information sent by the CBC over the two packets considered.
  - **EF** (***error flag***): corresponds to the logical OR of the EF flags sent out by the CBC over the two packets considered.
  - **S** (***synchronization bit flag***): set if at least if one of the two synchronization bits of the two stub packets sent by the CBC is wrong.

- ***MPA output register***

Structure of the stub output register for MPA configuration																
bit N°	***15***	***14***	***13***	***12***	***11***	***10***	***9***	***8***	***7***	***6***	***5***	***4***	***3***	***2***	***1***	***0***
stub N°1	**strip @**								**off**	**Zinfo**				**bend**		
stub N°2	**strip @**								**off**	**Zinfo**				**bend**		
stub N°3	**strip @**								**off**	**Zinfo**				**bend**		
stub N°4	**strip @**								**off**	**Zinfo**				**bend**		
stub N°5	**strip @**								**off**	**Zinfo**				**bend**		
stub N°6	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**S**

  - **x:** not used
  - **S** (***synchronization bit flag***): set if at least if one of the two synchronization bits of the two stub packets sent by the MPA is wrong.

3.3.3 Stub selection

This block collects the data produced by the 8 reconstruction blocks at a frequency of 20MHz, and stores it into a 278 bits internal register. The final output block containing data averaged over 8BXs, the total amount of data received is therefore equal to 4x8x96=3072 bits.

In most of the cases, the stub occupancy being very small, internal register size will be sufficient. In all the other cases, a selection based on the stub bend will be done. Priority will be given to the lower bends (*which are supposed to come from higher p_T tracks*).

The number of stubs lost this way for each FE chip is recorded on a 16 bits counter (*one counter per chip*). This parameter can be recovered via I^2C protocol in order to control data integrity at the CIC level. The frequency at which this parameter will be readout is not yet defined, but considering the size of the counter, the counter readout/reset can be done on an LHC orbit basis.

The CIC has two different configurations for the MPA output block, one with the stub bend encoded over 3 bits and the other one without the stub bend info **[1]**. Even in the configuration without the bend info, the bend is stored in the internal register in order to sort the stubs.

Every 8BXs (so at 5MHz), the block add the header information (*status bits, bunch crossing ID and number of stubs*) and write the final trigger frame in the output register. The header format is defined in the I/O format note.

The nine error bits contained in the header will be filled as follows. For the 8 FE chip bits, an OR of the different error signals available will be done (*synchronization bit error for MPA and CBC, plus stub overflow error and flag error for the CBC*). The CIC error bit will be set to one it a stub overflow occurs at this level.

Note to the DAQ: if there is still 3564 BXs in the future LHC orbit, some blocks will span over two LHC orbits. It is not foreseen to change anything in the CIC. In other words, the block starting at BXID 3560 will still contain the data from 8BXs: the four last BXs of the current orbit, and the four first BXs of the next one.

3.3.4 Output formatter

This block is a simple serializer, taking the final trigger frame built by the stubs selection block and serializing the data on the 4 CIC output lines reserved to trigger.

3.4 L1 path

3.4.1 L1 data controller

Contrary to the trigger data, L1 information is asynchronous. It is therefore particularly important to detect accurately the arrival of a new L1 data block.

This is the first function of this block, the second being to store the L1 words into a FIFO once they are completely received.

The L1 data start sequence lookup is performed only during a limited period of time in order to limit the power consumption. The lookup starts whenever a new L1 accept signal is

received by the CIC, a lasts during a given period. The length of this period can be set externally via I^2C register, and will be defined in agreement with CBC/MPA. One can in particular imagine different timeout period for both FE flavors.

If the start sequence is not detected during this period, the data controller block returns to idle state and raises a timeout error.

Start sequences for both FE chips are defined in the I/O note **[1]**.

For the MPA, one easily identifiable start sequence is necessary to readout the info of one chip.

Situation is a slightly different for the CBC, where L1 input frame size is the same for all the CBCs. The start sequence is therefore only 2 bits long, but all start sequences are supposed to be aligned in time. One searches the start sequences in parallel for all the CBC. A majority vote is required to decide whether or not to start the readout. If 4 start sequences are detected during the lookup, the readout is triggered.

Start sequence is not a problem for the MPA, but MPA L1 data size is not constant (*MPA info is already sparsified*). In this context, the only way to estimate the MPA word size is the number of clusters contained in the block header. If this number is not correct, 2 situations can occur:

- The frame is shorter or longer than expected, but the trailer bit is correct: in this case there is no way to retrieve the error, the frame is registered in FIFO without any error flag (*word reading is stopped at the trailer bit*).
- The frame has a wrong trailer bit or is cut by a new start sequence: in this case the frame is not registered in FIFO and an error flag is raised for the corresponding chip.

3.4.2 Sparsification (*for CBC only*)

This block is dedicated to the L1 data arriving from the CBC (*276 bits frame*). Data are received serially on one link at 320MHz with the following format:

header	error	L1 ID	pipeline address	channel data
2 bits	2 bits	9 bits	9 bits	254 bits

There are 8 sparsification blocks in the CIC (*1 per front end ASIC*), performing sparsification on the fly,

At the end of the CBC L1 frame readout, the internal data looks as follows:

header			payload				
status	L1 ID	nb clust	clust address	width	clust address	width	
							-------
3 bits	9 bits	5 bits	8 bits	3 bits	8 bits	3 bits	

In order to ensure MPA/CBC compatibility, the size of the register where this data is stored will be fixed by the size of the L1 data coming from the MPA. Recent studies **[5]** have shown that a size of 400 bits might be sufficient.

3.4.3 Deserialization (*for MPA and CBC-debug*)

This block is dedicated to the L1 data coming from the MPA or for the CBC data without sparsification required. Data are received serially on one link at 320MHz with the following format:

trame CBC

header	error	L1 ID	pipeline address	channel data
2 bits	2 bits	9 bits	9 bits	254 bits

tram MPA

header						payload						
						list of Sclust			list of Pclust			
error	L1 ID		nb Sclust	nb Pclust		Sclust address	width		Pclust address	width	z info	
		'0'			'0'			-------				-------
2 bits	9 bits	1 bit	5 bits	5 bits	1 bit	7 bits	3 bits		7 bits	3 bits	4 bits	

There are 8 deserialization blocks per CIC (*1 per front end ASIC*),

Once the L1 data controller block detects the start sequence, this block becomes active and starts the deserialization.

3.4.4 L1 FIFO

Memory used to store the L1 data coming from the CBC or MPA. There are 8 FIFOs in each CIC (*1 per front end ASIC*),

The FIFO stores data with a fixed size per event. As said earlier, its dimension will have to be defined according to simulations (*data size and depth*), and will mainly be driven by the size of MPA L1 events (*we will use 400 bits here*). The depth of the FIFO still has to be evaluated, but previous studies have shown that there should be never more than 10 L1 events stored in the meantime in the CIC. Therefore, a total memory size of 8x10x400=32000 bits is a reasonable starting point for CIC1 prototype.

The L1 data controller block generates the write signal on the FIFOs, whereas the output formatter block generates the read signal.

3.4.5 Output formatter

This block manages the read signal of the FIFOs and builds the final L1 data frame.

It implements a L1 trigger counter and a L1 data sent counter. Based on these counters and also on the L1ID info of the received frame (*from each front end ASICs*), this output formatter selects the FIFOs to read.

After an L1 trigger reception, a timeout is implemented in order to trigger the sending of the final L1 data frame even if one FIFO is empty.

If all the FIFOs have an L1ID that doesn't correspond to the expected one (*sent L1 data frame + 1*), an empty frame is build (*only header*) for the expected L1ID.

If due to an L1ID error, the frame stored in a FIFO has an L1ID corresponding to a frame already sent, or corresponding to an L1 trigger not already received → the frame is discarded.

3.5 SLVS drivers

Five differential lines send data at 320Mbps to the GBT: each line will be equipped with an SLVS driver. As in the case of the SLVS receivers discussed in 3.1, this driver is an IP block developed by the BG-PV INFN group **[3].**

4 External interfaces

4.1 Clocks

There will be two differential SLVS clock inputs, one at 40MHz and one at 320MHz.

4.2 Fast control

There will be a serial input operating at 320 MHz (*differential SLVS*) for fast commands. We will interpret these commands as planned for the CBC3, i.e. each of the bits will represent a single fast command.

Among the eight possible commands in a single bunch-crossing period of 25ns, CBC3 plans to use the first four bits, as shown in Figure 7.

Among these four bits, Fast Reset, Trigger, and L1 Counter Reset will also be used by CIC1. In particular, if the L1 counter reset corresponds to the LHC orbit reset, it will be particularly important for the L1 data controller.

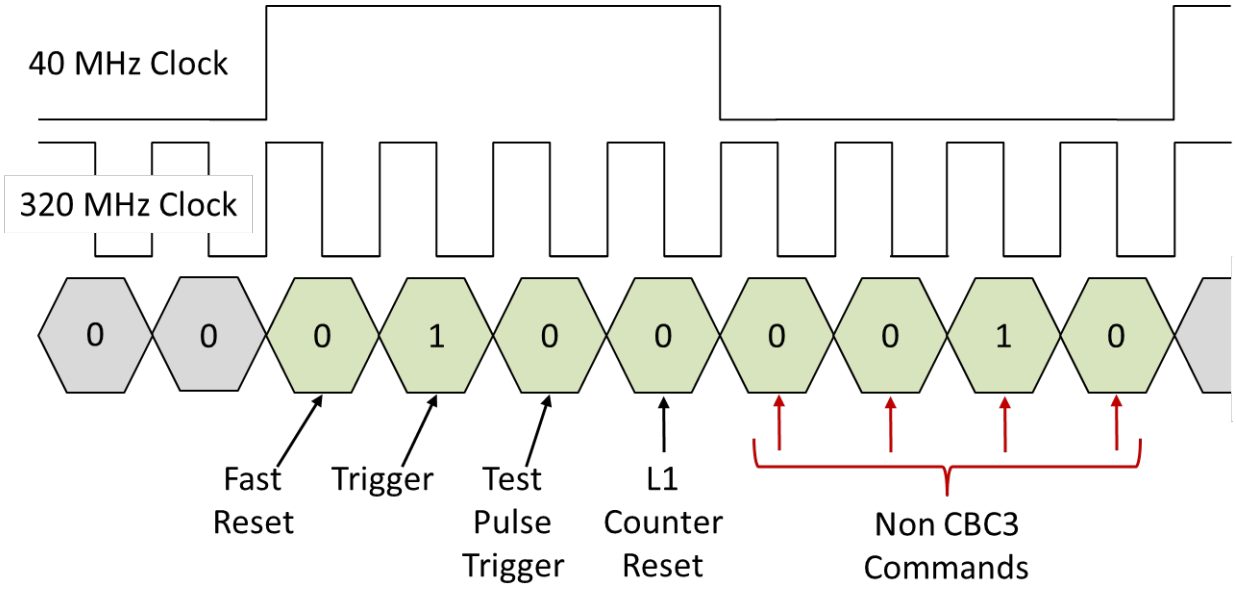

***Figure 7*: Proposed serial Fast Command data for the CBC3 (taken from [2]).**

4.3 Slow control

Slow control will be performed via I^2C protocol.

5 Power

The chip will work at 1.2V, which is the 65nm technology standard.

Power consumption is not yet estimated, but the current expectation is ~300mW per chip **[6]**.

6 Pads

A complete description of the constraints related to the CIC pinning is presented in **[4].** CIC1 will be based on the corresponding option : 0.4mm pitch BGA. Chip pinning is not yet finalized.

7 References

[1] 'I/O data formats for the Concentrator Integrated Circuit', https://espace.cern.ch/Tracker-Upgrade/Electronics/CIC/Shared Documents/Data formats/CIC_IO_Formats_v2.pdf

[2] 'CBC3 technical specification', http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC3_Technical_Spec_V1p03.doc

[3] 'Characterization of the reduced-swing LVDS links', https://indico.cern.ch/event/387147/session/0/contribution/6/material/slides/1.pdf

[4] 'CIC packaging options', https://indico.cern.ch/event/375536/session/4/contribution/20/material/slides/1.pdf

[5] 'CIC studies status', https://indico.cern.ch/event/375536/session/4/contribution/21/material/slides/0.pdf

[6] 'Powering the Phase II outer tracker', https://indico.cern.ch/event/394882/session/0/contribution/14/material/slides/1.pdf