# I/O data formats for the Concentrator Integrated Circuit

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# 1 Introduction

This note describes the proposed data formats for one of the main components of the CMS Phase II Tracker front-end (FE) chain: the Concentrator Integrated Circuit (CIC). The role of the CIC is to group the data coming from the tracker module FE chips, and to send this data to the GBT chip. By averaging data over time and space, the CIC enables a reduction of the data losses at the front end level by optimizing the usage of the available bandwidth.

After a short description of the CIC data transmission context in Section 2, data formats received from FE chips by CIC inputs are described in Section 3. Output data formats are described in details in Section 4. In each section, an estimation of the losses in Phase II conditions, estimated using simulated events, is provided. Finally, conclusions are given in Section 5.

## 2 Context

Figure 1 presents a part of the layout of future CMS Phase II tracker. The blue and red lines are the modules of the outer tracker, which is the object of this document. The two colors are used to differentiate the two types of detection units used in the future detector. Blue modules, named PS modules, have an higher granularity than the red ones, named 2S modules. Therefore they provide higher precision hits in the innermost region of the tracker: the inner barrel (TIB) and endcaps (TICs). The corresponding outer parts, made of 2S modules, are called outer barrel (TOB) and outer endcaps (TOCs).

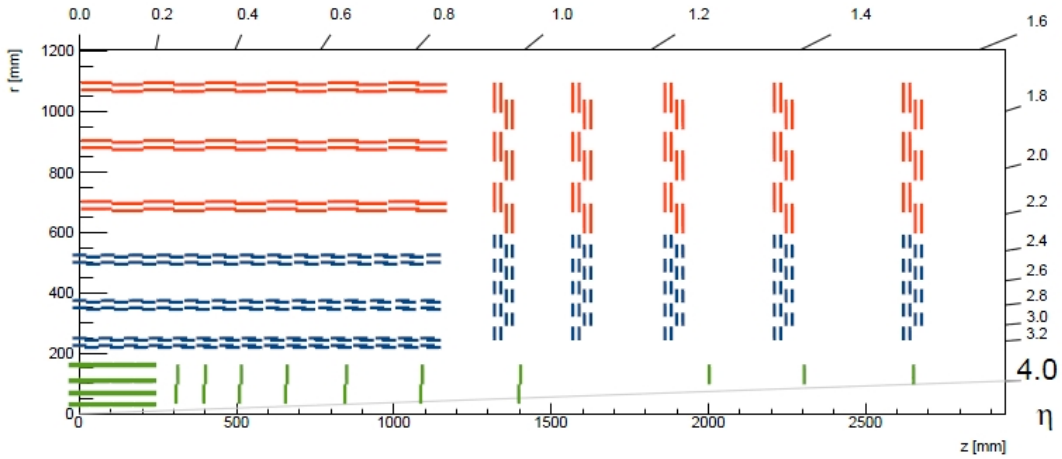


***Figure 1:** Sketch of one quarter of the Tracker Layout.*

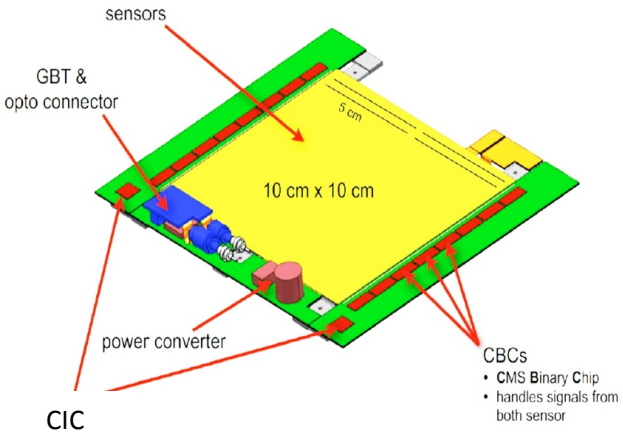


***Figure 2:** Outer module (2S)*

Figure 2 shows one of the two modules type: the 2S. Next to the yellow active area (silicon sensor), three hybrids host the module front-end electronic components. The sensor signals are collected on each side of the module via 2x8 front-end chips (CBC for the 2S, MPA for the PS). A CIC chip collects the digital data coming from each

group of 8 FE chips and transmits them to the GBT. There are therefore 2 CIC chips per module.

In order to minimize the noise induced by the large number of lines on the hybrid, all the lines between FE chips and CIC, and also between CIC and GBT, are differential (slvs). In order to limit the total number of lines their datarate is 320 Mbps. In the nominal version of the concentrator, there are 6 differential lines @320Mbps between each front end chip and the concentrator (48 lines in total), and 5 differential lines @320Mbps between each concentrator and the GBT (see Figure 3).

The concentrator I/O interface is adapted to the two FE chips (CBC / MPA) which are used in the two different module types (2S / PS). The CIC can switch between both formats via a simple configuration change.

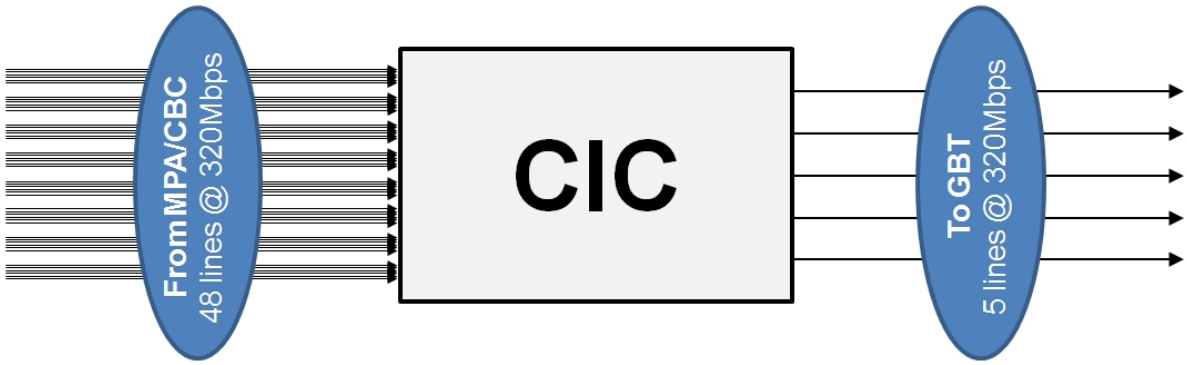


***Figure 3: CIC block diagram.***

FE chips are sending out two different data types:

- **Trigger data**: this data payload is sent at 40MHz and corresponds to the information necessary to the L1 track reconstruction system. It needs to be transmitted with minimum latency.
- **L1 data:** this data payload corresponds to the raw tracker data, and is sent on request each time an L1-accept signal is emitted by the CMS L1 global trigger decision unit. During LHC phase II, the CMS L1A rate might reach up to 1MHz.

## 3 CIC input data format

As said in the previous section, data is carried out from each FE chip to the concentrator via 6 differential lines @320MHz. For each FE type (CBC/MPA) this bus is split into two sub-buses:

- One line for the L1 data transmission (total BW=320Mbits/s),
- Five lines for the trigger data transmission (total BW=1.6Gbits/s).

We will now detail, for the two FE types, the data transmitted by these buses.

## 3.1 Input from CBC chip

### 3.1.1 Trigger bus

The trigger data sent by the CBC are LHC clock synchronous. At each bunch crossing (40MHz), each CBC chips sends the data block sketched in Figure 4. This 40 bits block can contain up to 3 stubs (stub is the name of the hit used by L1 tracking), with a stub encoding format on 13bits (8 bits for the address and 4 bits for the bend).

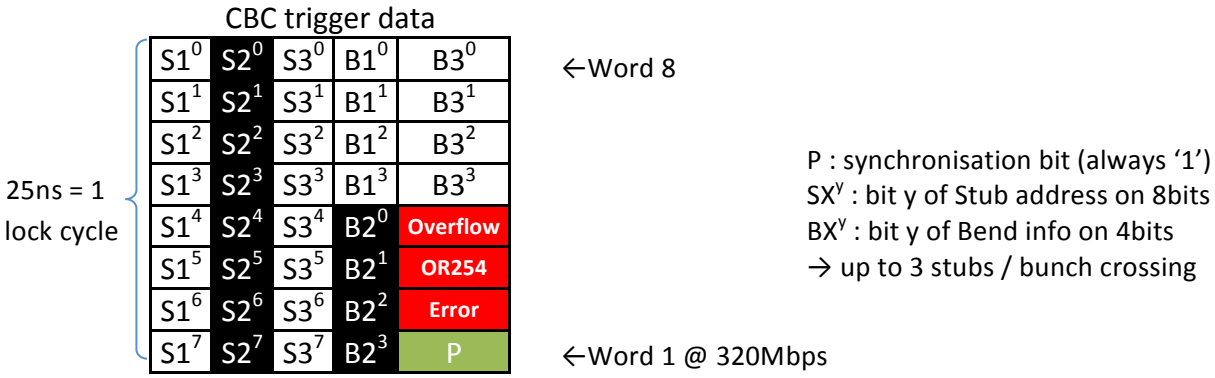


***Figure 4:* CBC output trigger data format**

To encode 3 stubs, 36 bits are needed. The four last bits are used to pass status information concerning the CBC. The last bit, marked P, is used to flag the last word of the block. Using this bit, the CIC can control at each bunch crossing if the incoming block still has the same phase.

### 3.1.2 L1 bus

The L1 data sent by the CBC chip is not sparsified. This data, which is sketched in Fig.5, consists in a digital header (2bits), 2 error bits, the CBC pipeline address (9bits), the L1 ID (9bits), and the data from all 254 channels. The full data stream is therefore 276 bits long.

| header | error | pipeline address | L1 ID | channel data |
|---|---|---|---|---|
| 2 bits | 2 bits | 9 bits | 9 bits | 254 bits |

***Figure 5:* CBC L1 data format**

### 3.1.3 Estimated losses

Losses were estimated using 200 sequences of events produced using the CMS simulation framework (CMSSW 620_SLHC15). Each trigger sequence is 1600 clock cycles long, and is obtained by mixing randomly 90% of simple pile-up (PU) events (average PU of 140 and 200) with 10% of complex PU events (PU140/200 and four tops signal).

The losses presented here correspond to the coding presented previously. They are shown for the different layers of the tracker barrel, and only for stubs induced by a primary particle with a transverse momentum large than 2GeV/c.

| *Layer* | *TOB1* | *TOB2* | *TOB3* |
|---|---|---|---|
| *PU140 loss (in %)* | **0.2** | **0.2** | **0.1** |
| *PU200 loss (in %)* | **0.2** | **0.2** | **0.2** |

***Table 1:* CBC trigger data losses.**

The CBC trigger data losses are negligible, and CBC L1 data can by construction be transmitted up to L1A rates of more than 1MHz. In conclusion data transmission between CBC and CIC is working within requirements.

## 3.2 Input from MPA chip

### 3.2.1 Trigger buses

As said earlier, bandwidth sharing between trigger and L1 is the same for the MPA and for the CBC. However, in order to handle the much higher occupancy in the tracker inner layer, trigger data from the MPA is sent in synchronous blocks of 2 clock cycles in order to average the stub rates. Trigger data format is shown in Fig. 6.

trigger data from MPA

| | | | | |
|---|---|---|---|---|
| P1 | $N^2$ | $N^1$ | $N^0$ | $S1^7$ |
| $S1^6$ | $S1^5$ | $S1^4$ | $S1^3$ | $S1^2$ |
| $S1^1$ | $S1^0$ | $B1^2$ | $B1^1$ | $B1^0$ |
| $Z1^3$ | $Z1^2$ | $Z1^1$ | $Z1^0$ | $S2^7$ |
| $S2^6$ | $S2^5$ | $S2^4$ | $S2^3$ | $S2^2$ |
| $S2^1$ | $S2^0$ | $B2^2$ | $B2^1$ | $B2^0$ |
| $Z2^3$ | $Z2^2$ | $Z2^1$ | $Z2^0$ | $S3^7$ |
| $S3^6$ | $S3^5$ | $S3^4$ | $S3^3$ | $S3^2$ |
| P2 | $S3^1$ | $S3^0$ | $B3^2$ | $B3^1$ |
| $B3^0$ | $Z3^3$ | $Z3^2$ | $Z3^1$ | $Z3^0$ |
| $S4^7$ | $S4^6$ | $S4^5$ | $S4^4$ | $S4^3$ |
| $S4^2$ | $S4^1$ | $S4^0$ | $B4^2$ | $B4^1$ |
| $B4^0$ | $Z4^3$ | $Z4^2$ | $Z4^1$ | $Z4^0$ |
| $S5^7$ | $S5^6$ | $S5^5$ | $S5^4$ | $S5^3$ |
| $S5^2$ | $S5^1$ | $S5^0$ | $B5^2$ | $B5^1$ |
| $B5^0$ | $Z5^3$ | $Z5^2$ | $Z5^1$ | $Z5^0$ |

**Px :** synchronisation bit (P1 always '1', P2 always '0'),

**$N^y$ :** bit y of stubs number in the 1st bunch crossing

**$SX^y$ :** bit y of Stub address on 8bits,

**$BX^y$ :** bit y of Bend info on 3bits,

**$ZX^y$ :** bit y of Z info on 4 bits

→ up to 5 stubs / 2 bunch crossings

***Figure 6:* MPA output trigger data format**

In order to determine the bunch crossing (BX) to which each stub belongs, the number of stubs in the first BX is encoded over 3 bits at the beginning of the data block. All stubs in the payload beyond this value belong to the second BX. The unused bits at the end of the 40 bits block are filled with 0's.

With the current configuration, the MPA can send out up to 5 stubs over 2 clock cycles.

As the packet is spanning over two clock cycles, 2 synchronisation bits are added to the packet in order to mark the first word of the first bunch clock (P1), and the first word of the second bunch clock (P2). The P1 bit is fixed to '1' and the P2 bit is fixed to '0'.

### 3.2.2 L1 bus

The L1 data sent out by the MPA is sparsified. The MPA L1 data format, sketched in Fig.9, consists of two basic parts: a header and a payload.

- The header has a fixed length and five data blocks: a start sequence (19bits), an error field (2bits), a L1ID (9bits), the strip cluster multiplicity (5bits) and finally the pixel cluster multiplicity (5bits).
- The payload has a variable length and is divided into two parts. The first part is the strip clusters list, each strip cluster being encoded on 10bits (7bits address and 3 bits width). The second part is the pixel cluster list, each pixel cluster being encoded on 14bits (7bits address, 3bits width and 4bits for the Z position).

The goal of the start sequence is to create a unique and well identified sequence of 19 bits that cannot be found anywhere else in the data format. In case of error in the L1 data format, at worst the erroneous L1 data frame will be lost, but the concentrator will be able to handle easily the next frame. In order to guarantee the uniqueness of the start sequence, a fixed '0' bit is inserted in the header part between the L1 ID field and the number of strip cluster, and also between the number of pixel cluster and the payload part.

Finally, the MPA L1 data format is completed by a trailer (one bit at '0' logic).

MPA output L1 data

| header | | | | | | | payload | | | | | | | T |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | list of Sclust | | | list of Pclust | | | | |
| start sequence | | error | L1 ID | | nb Sclust | nb Pclust | | Sclust address | width | | Pclust address | width | z info | | |
| start séquence : 18 bits at '1' | '0' | | | '0' | | | '0' | | | ------- | | | | ------- | trailer '0' |
| 19 bits | | 2 bits | 9 bits | 1 bit | 5 bits | 5 bits | 1 bit | 7 bits | 3 bits | | 7 bits | 3 bits | 4 bits | | 1 |

***Figure 7: MPA L1 data format***

### 3.2.3 Estimated losses

Losses were evaluated using the same method as for the CBC, for the trigger part only. Only a configuration with 5 bits for the bend has been tested for the moment.

| *Layer* | *TIB1* | *TIB2* | *TIB3* |
|---|---|---|---|
| *PU140 loss (in %)* | 1.05 | 0.2 | 0.05 |
| *PU200 loss (in %)* | 1.7 | 0.3 | 0.1 |

***Table 2:** MPA trigger data losses.*

Table 2 shows that a pressure starts to show up already at the front-end level in the barrel innermost layer. This means that one should expect more important losses at the concentrator output. However, for what concerns the MPA output level, the configuration described in Fig.6 should enable a significant reduction of the losses shown on Table 2.

For what concerns L1 data transmission, loss estimation was not done. However, due to the data sparsification at the MPA level, no transmission problems are expected at this stage up to an L1A rate of 1MHz.

# 4 CIC output data format

The data transmission from the concentrator to the GBT is done via 5 lines running at 320MHz. Two output repartitions are envisaged:

- **80/20:** this repartition is the same as for the FE chip outputs, 4 lines for trigger and 1 line for L1. It is the baseline scheme at the time of writing.
- **Priority to trigger:** all the BW (5 lines) is allocated to trigger during the colliding bunches, whereas the L1 data is stored in the specific concentrator memory and sent out to the GBT only during the bunch gaps upon reception of a dedicated trigger signal. This scheme is currently not the baseline and its data formats are not described below.

In order to minimise the data loss, while keeping a synchronous concentrator output bus, the concentrator sends out the trigger data in an 8 clock cycles synchronous block. The CIC stores the trigger data incoming from the FE chips during 8 BXs, sorts them within each BX w.r.t their bend info, and sends them out in an 8 clock cycles long packet.

At the beginning of a run, a bunch counter reset trigger is sent to the concentrator in order to restart a new packet of 8BXs with the new orbit. The LHC orbit has 3564BXs, and 3564/8=445.5 packet of 8BXs, so there is no entire number of packet in one orbit. It was decided to not cut the last 8BXs packet at the end of an orbit even if it is not completely finished. So the last 8BXs packet could belong on two orbits, but in any case, the BxID (header information) and the BxOffset of each stubs in the packet can determine without any ambiguity the orbit source of the stubs.

## 4.1 Concentrator output for CBC configuration

### 4.1.1 Trigger buses

The trigger data coming from the CBCs is sent out by the concentrator in a block synchronous way over 8 clock cycles. The trigger data format is divided into two basic parts, a header and a payload.

The frame starts with a 26 bits header:

- 1 bit for the FE type: ‘0’ for CBC,
- 9 status bits: 1bit for each FE chip status, 1bit for the CIC,
- 12 bits for the BX ID: timestamp within the LHC cycle,
- 4 bits for the packet stub multiplicity.

The stubs are then passed into the payload with the following format:

- 3 bits for timing offset within the 8 clock cycles,
- 3 bits for the FE chip ID,
- 8 bits for the stub address,
- 4 bits for the stub bend coding.

The CIC output trigger data formats for the 80/20 transmission scheme is shown in Figure 8. The frame being partly filled with the payload, it is padded with zeros.

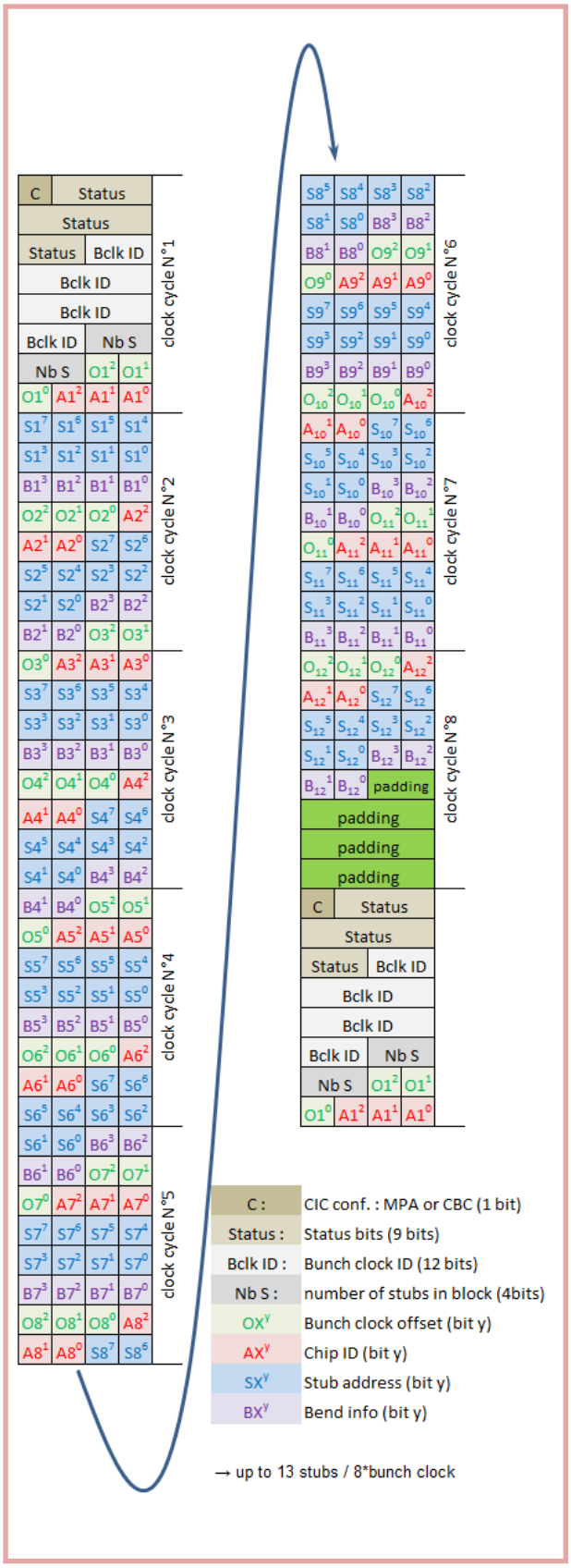

***Figure 8:* CIC output trigger data format (CBC configuration)**

### 4.1.2 L1 bus

The L1 data coming from the CBC is not sparsified. The concentrator can be configured to send either sparsified or unsparsified L1 CBC data. For the unsparsified configuration, the concentrator sends the data coming from the 8 CBCs in a row with a 16bits start sequence and a 1bit trailer (see Fig. 10). For the sparsified configuration, the CIC output format consists of two basic parts, a header and a payload (see Fig. 11):

- The header has a fixed length and four data fields: a start sequence (16 bits), a status field (9 bits), an L1 ID (9 bits), the payload cluster multiplicity (5 bits).
- The payload has a variable length and contains the clusters, each cluster being encoded on 14bits (3 bits chip ID, 8 bits address, and 3 bits width).

As for the MPA L1 format, the goal of the start sequence is to create a unique and well identified sequence of 16 bits that cannot be found anywhere else in the L1 word data. In order to guarantee the uniqueness of the start sequence (only for the sparsified configuration), the concentrator counts the number of consecutive logical '1' sent out in the data frame. If this number equals 14, the concentrator inserts one logical '0' directly after the 14$^{th}$ logical '1' in the output data frame. For the receiver, two situations are possible:

1. the receiver gets 15 consecutives '1' in the data frame → this is the header,
2. the receiver gets only 14 consecutives logical '1' → the following logical '0' must be removed (it was added by the concentrator).

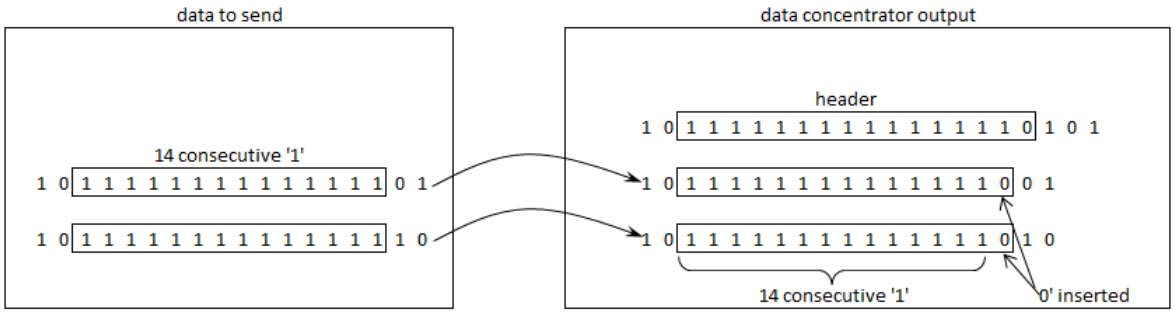


***Figure 9:* logical '0' insertion in the concentrator**

The concentrator L1 data format for both configurations is summarized in Figures 10 and 11:

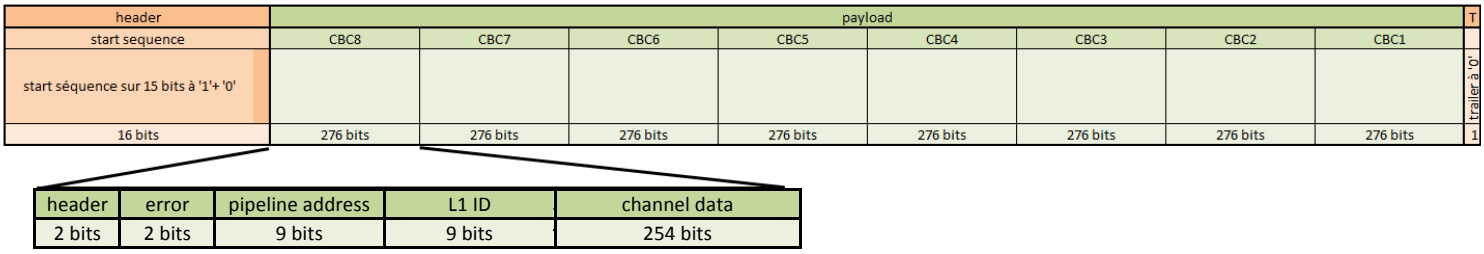


***Figure 10:* CIC L1 output for CBC unsparsified data**

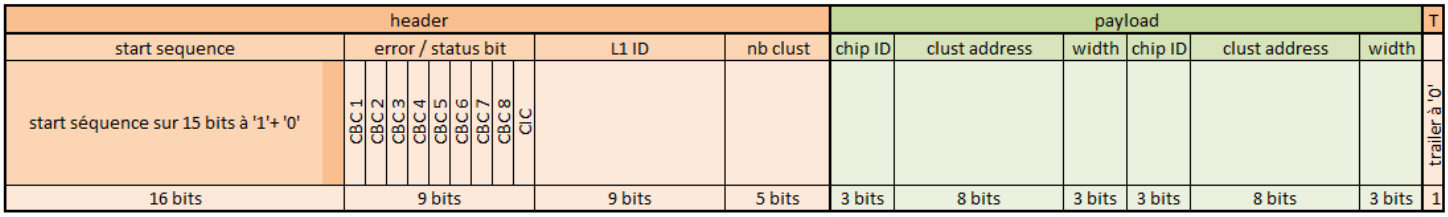


***Figure 11:* CIC L1 output for CBC sparsified data**

### 4.1.3 Estimated losses

Trigger losses were estimated using the same method and data samples as for the FE chips output. For what concerns the L1 block losses, the observable is the number of L1 events stored in the CIC FIFO w.r.t. the LHC running time, in number of BXs. In the current CIC version, one can store up to 34kbits of L1 data. This corresponds to about 16 unsparsified CBC events. A new L1 event is stored in the CIC FIFO each time the CIC is extracting a previously stored L1 event. If the FIFO is full, the CIC error bit for this event will be set to 1 and an empty frame will be sent. The occurrence of this type of error will be linked to the FIFO size, but also to the L1A frequency. The larger the L1 accept rate is, the faster the FIFO will fill up. At a certain point, the rate will become too large and the FIFO size will diverge with time. In this case, empty frames will be sent whatever the FIFO size is. What we are estimating here with our simulated events, is the L1 rate for which the FIFO starts to diverge for a large number of CIC chips. The events used for that are PU140/200+4 tops events.

#### 4.1.3.1 Trigger block

Trigger losses for the CBC part of the concentrator output are summarized in Table 3. As in the other tables, values are given in % for stubs induced by primary particles with a pT larger than 2Gev/c. The losses are below the 1% limit, and become

negligible if 3 bits are used for stub bend coding. It is also interesting to note that this behaviour is robust against pile-up.

This result is not really surprising. The rates in the tracker outer modules are indeed ~10 times lower than in the inner ones. One did not expect data transmission problems in this area.

| Layer | | TOB1 | TOB2 | TOB3 |
|---|---|---|---|---|
| Bend on 5 bits | PU140 loss (in %) | 0.35 | 0.25 | 0.15 |
| | PU200 loss (in %) | 0.4 | 0.3 | 0.3 |
| Bend on 3 bits | PU140 loss (in %) | 0.2 | 0.05 | 0.15 |
| | PU200 loss (in %) | 0.3 | 0.2 | 0.3 |

***Table 3:* CIC trigger data losses for outer layers (CBC).**

#### 4.1.3.2 L1 block

As for the trigger block, the L1 data transmission from the outer modules by the CIC is possible without any problem up to the required L1A frequency of 1MHz.

## 4.2 CIC output for MPA configuration

### 4.2.1 Trigger buses

The trigger data coming from the CBCs is sent out by the concentrator in a block synchronous way over 8 clock cycles. The trigger data format is divided into two basic parts, a header and a payload.

The frame starts with a 26 bits header:

- 1 bit for the FE type: '1' for MPA,
- 9 status bits: 1bit for each FE chip status, 1bit for the CIC,
- 12 bits for the BX ID: timestamp within the LHC cycle,
- 4 bits for the packet stub multiplicity.

The stubs are then passed into the payload with the following format:

- 3 bits for timing offset within the 8 clock cycles,
- 3 bits for the FE chip ID,
- 8 bits for the stub address,
- 3 bits for the stub bend coding,
- 4 bits for z position.

The CIC output trigger data formats for the 80/20 transmission scheme is shown on Figure 12. Configuration without bend info is also shown, as a reference, on Fig.13.

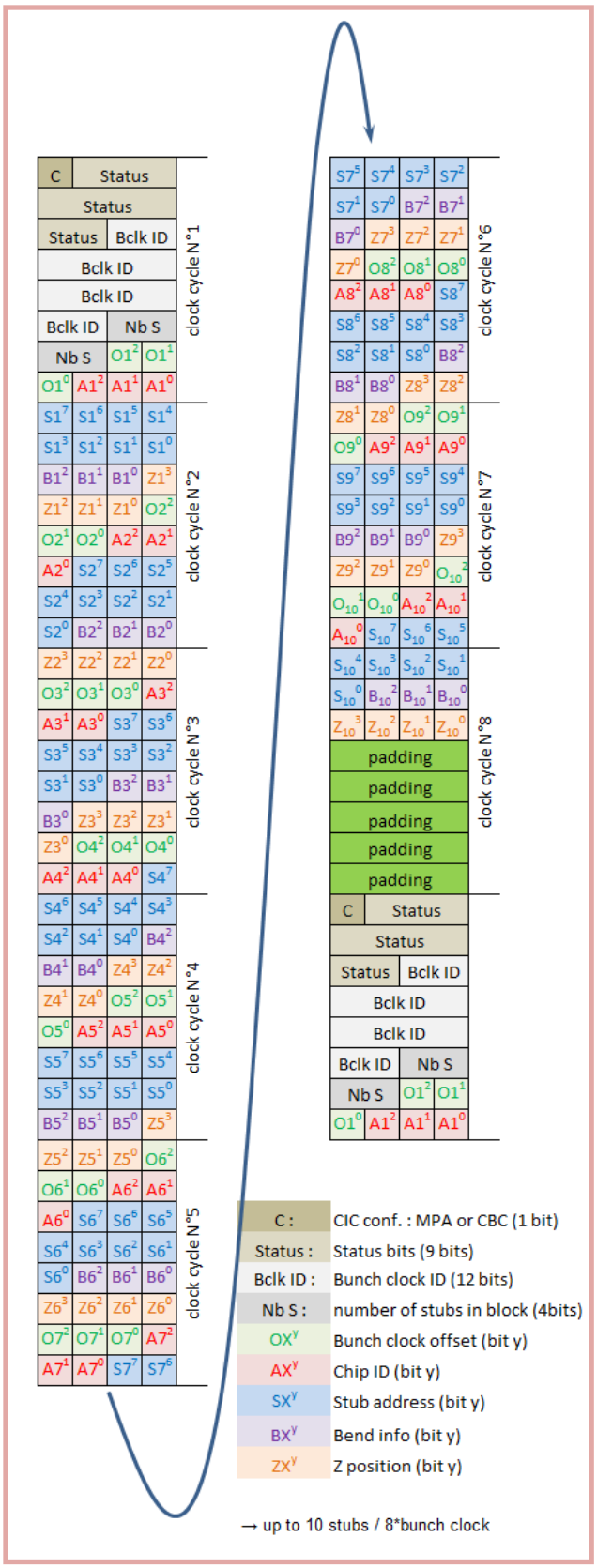


***Figure 12:* CIC output trigger data format (MPA configuration)**

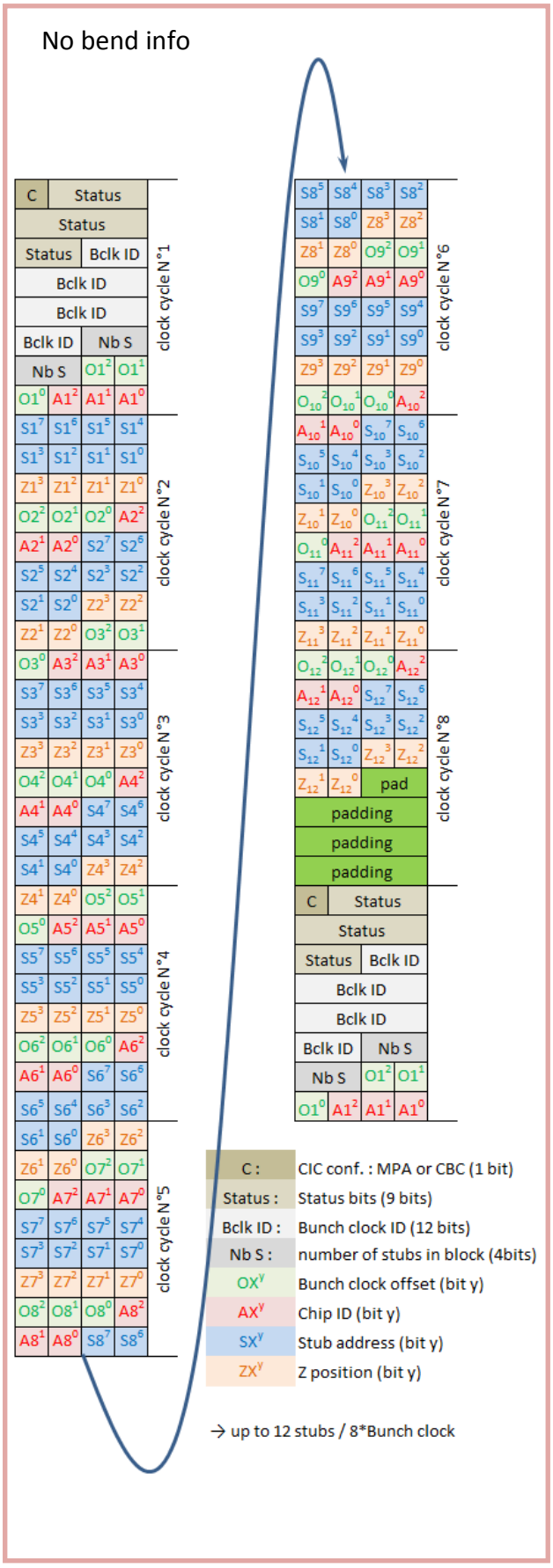


***Figure 13:*** ***CIC output trigger data format (MPA configuration)***

### 4.2.2 L1 bus

The CIC output format consists of two basic parts, a header and a payload:

- The header has a fixed length and five data fields: a start sequence (16 bits), a status field (9 bits), an L1 ID (9 bits), the payload strip cluster multiplicity (5 bits) and the payload pixel cluster multiplicity (5 bits).
- The payload has a variable length and contains the the two types of clusters in two distinct parts. Each strip cluster is encoded on 13 bits (3bits chip ID, 7bits address and 3 bits width), and each pixel cluster is encoded on 17bits (3bits chip ID, 7bits address, 3bits width and 4bits for the Z position).

The goal of the start sequence is to create a unique and well identified sequence of 16bits that can't be found anywhere in the data format.The same mechanism as for the CBC L1 sparsified block is applied.

The CIC L1 data format for the MPA is shown in Figure 14:

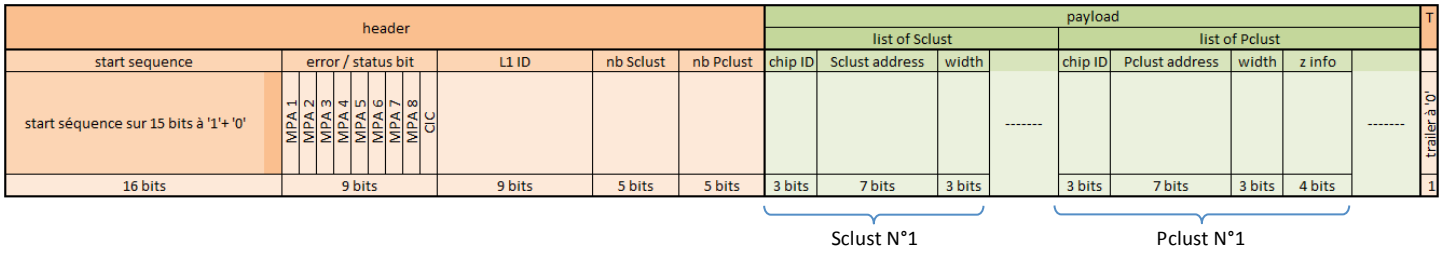


***Figure14:* CIC L1 output for MPA sparsified data**

### 4.2.3 Estimated losses

#### 4.2.3.1 Trigger block

For what concerns e trigger block, baseline results are summarized in Table 4.

| Layer | | TIB1 | TIB2 | TIB3 |
|---|---|---|---|---|
| Bend on 5 bits | PU140 loss (in %) | 30.95 | 4.2 | 0.3 |
| | PU200 loss (in %) | 50.8 | 12.5 | 0.9 |
| Bend on 3 bits | PU140 loss (in %) | 25.45 | 2.5 | 0.2 |
| | PU200 loss (in %) | 46.0 | 8.6 | 0.6 |
| No bend | PU140 loss (in %) | 16.8 | 1.1 | 0.15 |
| | PU200 loss (in %) | 38.5 | 4.9 | 0.3 |

***Table 4:* CIC trigger data losses for inner layers (MPA), in the 80/20 transmission scheme**

These results show a clear problem, in particular for the innermost barrel layer. One should expect a similar problem for the inner disk rings (some of them are necessary

to the trigger). In some cases, even the transmission for the second layer is problematic. The PU200 situation is even more critical.

To serve as a comparison, results obtained in the 'priority to trigger' transmission scheme are given in Table 5.

| Layer | | TIB1 | TIB2 | TIB3 |
|---|---|---|---|---|
| Bend on 5 bits | PU140 loss (in %) | 19.0 | 1.25 | 0.1 |
| | PU200 loss (in %) | 39.3 | 5.1 | 0.3 |
| Bend on 3 bits | PU140 loss (in %) | 14.1 | 0.7 | 0.1 |
| | PU200 loss (in %) | 33.8 | 2.9 | 0.2 |
| No bend | PU140 loss (in %) | 7.75 | 0.3 | 0.15 |
| | PU200 loss (in %) | 25.8 | 1.4 | 0.1 |

***Table 5:* CIC trigger data losses for inner layers (MPA), in the 'priority to trigger' transmission scheme**

This configuration provides an acceptable solution for layer 2 at PU140, however, even though the losses are significantly reduced, they are still not acceptable for layer 1.

In order to reduce the stub rate in the inner layers, one solution is to constrain the maximum acceptable stub width. This will however affect the pT threshold of the stub. Table 6 shows the results obtained in the 'priority to trigger' method, with stub width cut corresponding to a pT threshold of 3GeV/c.

| Layer | | TIB1 | TIB2 | TIB3 |
|---|---|---|---|---|
| Bend on 5 bits | PU140 loss (in %) | 9.1 | 0.4 | 0 |
| Bend on 3 bits | PU140 loss (in %) | 6.7 | 0.3 | 0 |
| No bend | PU140 loss (in %) | 3.0 | 0.2 | 0 |

***Table 6:* CIC trigger data losses for inner layers (MPA), in the 'priority to trigger' transmission scheme (3GeV/c threshold)**

This new cut provides a clear improvement, but losses are still large in the innermost part. The last improvement consists of using a tighter set of SW cuts. The cuts presented previously ensure a sharp turn-on at the required threshold. Therefore, with such cuts, stub efficiency at lower pT is not negligible. With tighter cuts, efficiency at the threshold is a bit lower, but the low pT background is strongly suppressed. Table 7 shows the results obtained by applying a tighter 3GeV cut. Only results for TIB1 are shown, as an acceptable solution exists for the other layers. With this last configuration, it is possible to go below the 1% limit. This requires more advanced studies, with more realistic simulations, but this shows that trigger block

transmission from the CIC in the inner modules looks possible using the formats described in this note, under certain conditions tough.

| Layer | | TIB1 |
|---|---|---|
| Bend on 5 bits | PU140 loss (in %) | 3.15 |
| Bend on 3 bits | PU140 loss (in %) | 1.95 |
| No bend | PU140 loss (in %) | 0.9 |

***Table 7:** CIC trigger data losses for inner layers (MPA), in the 'priority to trigger' transmission scheme (3GeV/c tight threshold)*

#### 4.2.3.2 L1 block

For the L1 block, analysis of the FIFO behavior of the CIC chips versus time was made using a sequence of L1A randomly generated over 50000 clock cycles. The L1A frequency was varied between 100 kHz and 1 MHz, with 100 kHz steps. The evolution of the time spent by L1 events in the CIC FIFO as a function of time was measured and fitted to a straight line. There is a risk of loss if the slope of this line (the FIFO drift) is not compatible with 0.

Figure 15 shows for example the average value of the FIFO drift for the barrel modules at PU140 with an L1 rate of 1MHz. The L1 data transmission here is the baseline one, ie 64 bits per CIC block for L1 transmission.

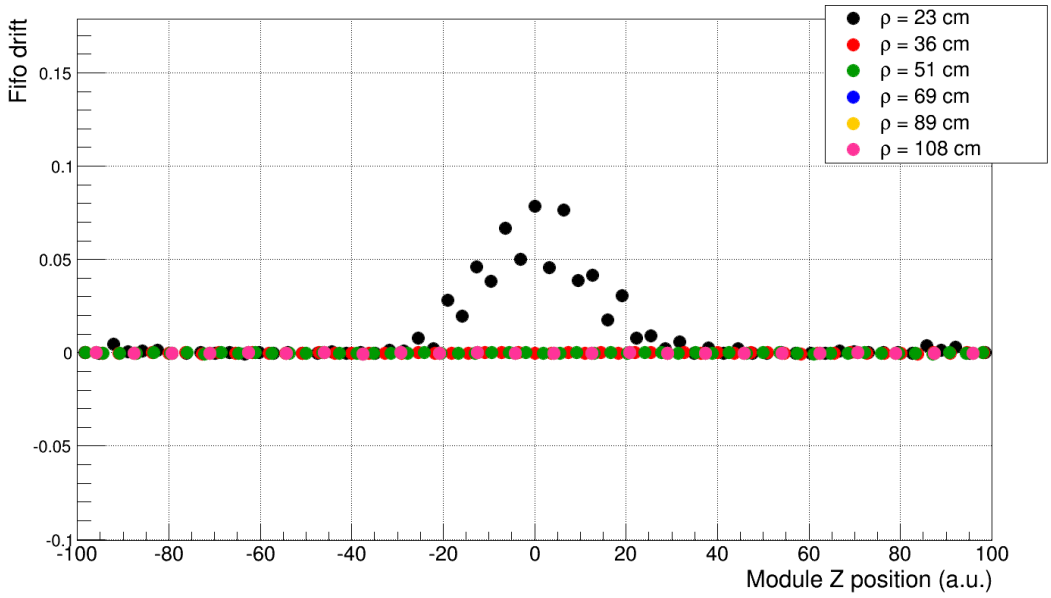


***Figure15:** Barrel modules FIFO drifts at PU140 and L1 rate of 1MHz*

In this plots one clearly see that the drift of some central modules of the innermost barrel layer are not compatible with 0. It means that these modules are not able to sustain an L1A rate of 1MHz in the baseline transmission scenario. The other modules, on the other hand, seem to work well under these conditions.

Looking at those plots different rates and PU conditions, one found that the maximum acceptable L1 rates observed were 800 kHz for PU140+4tops events and 500 kHz for PU200+4tops events. For larger rates, drifts are observed in the inner regions of the tracker.

### 4.2.4 Mitigating the losses

As we have seen, losses at the CIC output might be a critical point in the innermost layers of the tracker. However, it should be pointed out that these results are in constant evolution, in particular due to constant improvements of the simulation. They should therefore not be considered as definitive values.

Moreover, we have shown in the previous section that methods to reduce the losses exist. Other methods still have to be evaluated, like for example doubling the CIC output rate.

One could reasonably expect that the final CIC data transmission scheme will include a mix of these solutions. However, the application of these loss reduction techniques will concern only a small part of the detector, under certain data taking configuration. The CIC will therefore have to be highly configurable in order to switch between those options on request. From this document, one can already infer that the CIC might have to be able to:

- Switch between MPA and CBC I/O types
- Run with different stub encodings (bits for bend value)
- Send data to 2 different GBT configuration (5Gbps and 10 Gbps)
- Send also unsparsified raw data for the 2S modules
- Modify the trigger/L1 repartition of the concentrator block

# 5 Conclusion

The I/O data formats of the CIC chips were presented. For the output formats, a common scheme for both FE chip types, CBC and MPA, was established. Such a scheme will simplify the decoding of the tracker data by the DAQ.

First estimates of the data losses, done with the latest available simulations, were shown. Although these results should be considered with caution (we are for example still missing a proper estimation of min. bias at 14 TeV), they tend to confirm that outer layers modules will work without any problem under Phase II conditions. CIC chips should be able to transmit the data from these modules up to the required conditions. On the other hand, transmission of the data in the inner part of the detector will require some specific tuning, and therefore an high flexibility in the CIC chip configuration. The default transmission formats applicable to the outer modules will indeed not work for the first one or two innermost layers. Rate reduction strategies were presented, some of them showing encouraging results.