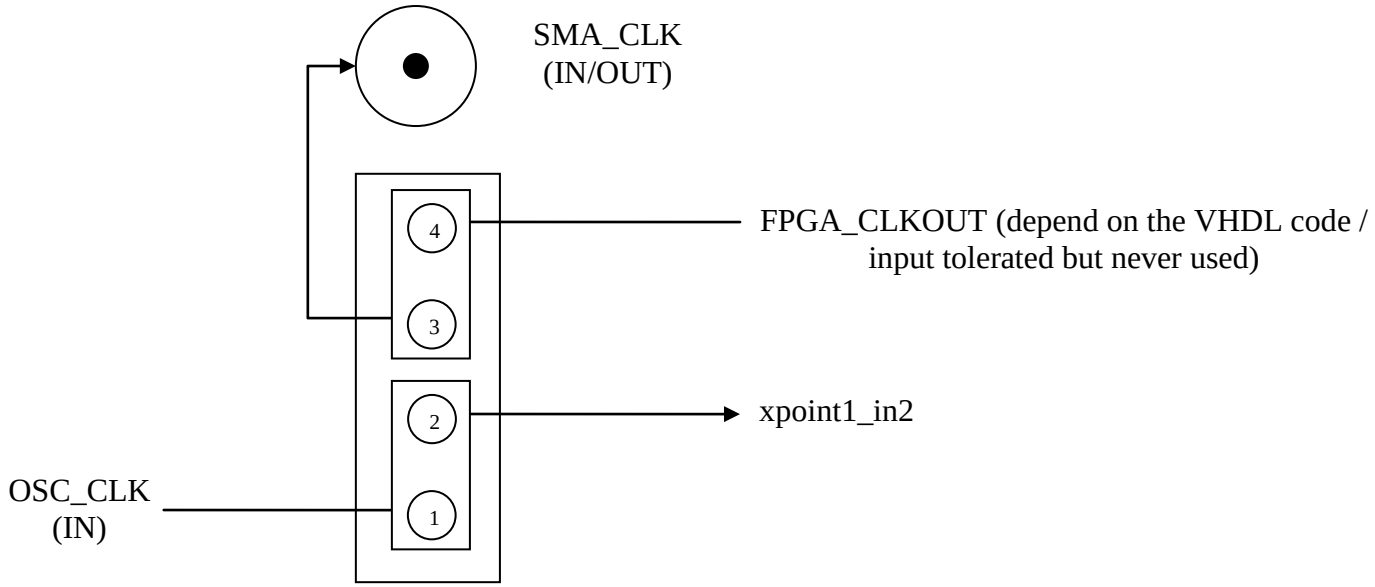
Clocking

BE: Open user_logic_be.vhd

The main clock is called" tx_frame_clk". Currently, it is provided by "cdce_out4_p/n" (coming directly from the clock synthesizer CDCE62005). Please verify if the two jumpers are well set like this:



The MGT112REFCLK0 = cdce_out0 is used as clock for GBT (frequency = 240MHz) both for BE & FE. The clock synthesizer CDCE62005 has to be well configured to provide this frequency.

For the GLIB(FE), the cdce_out4 has to be used as tx_frame clock. So you have to configure the external CDCE through the code Pychips provided in attached files.

To well verify that the frame clock are alright (BE side and FE side), please connect the SMA to a scope. Normally the clocks are both synchronous and have the same frequency (40 MHz).