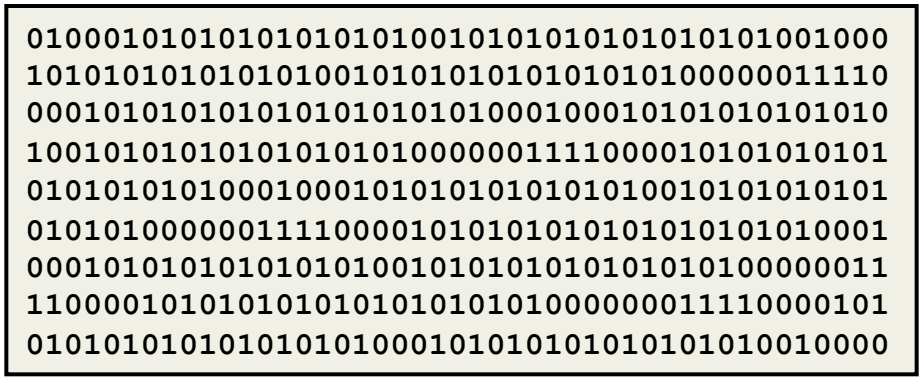
CIC status



Introduction
Chip status
Test tools

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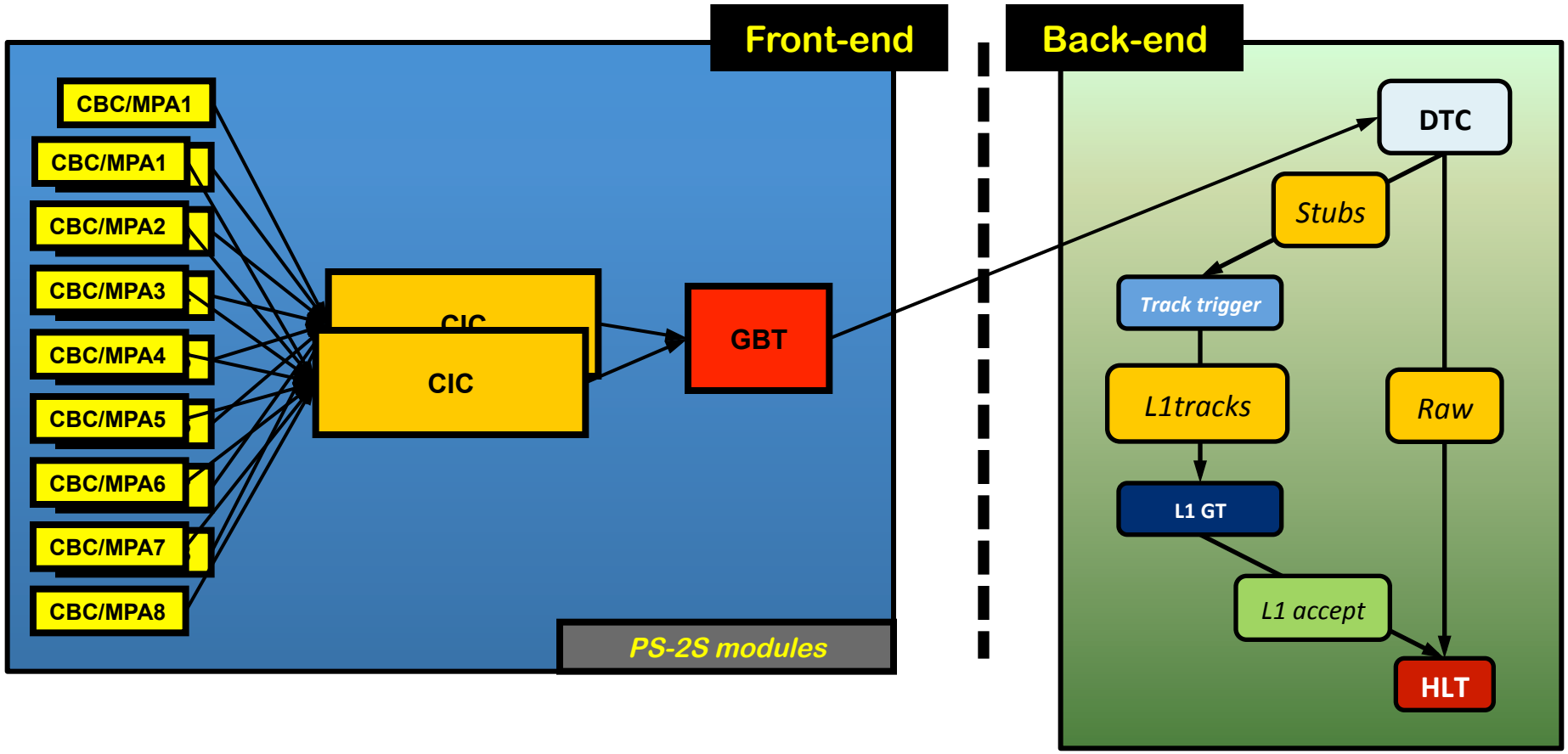
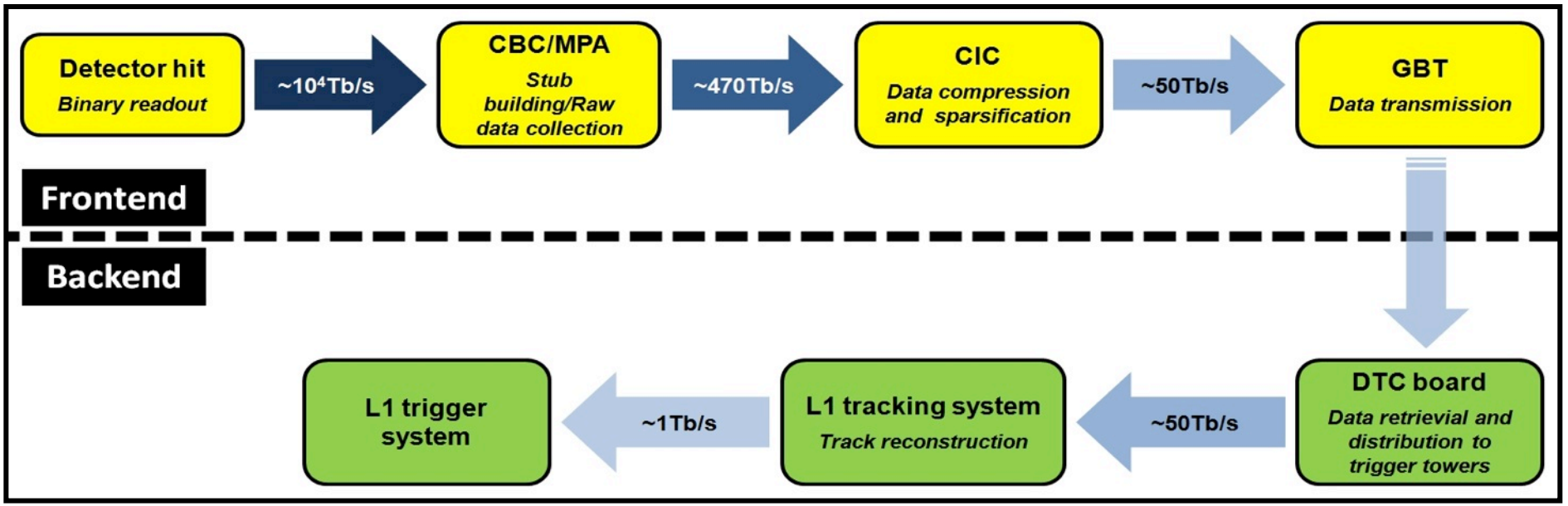
IPN Lyon

→ **Phase II tracker data extraction protocol:**



→ **19 ASICs per module**

→ **The data compression challenge:**



→ You must divide the amount of data by a factor ~200 in order to be able to extract tracker info to the backend at 40MHz

→ **CIC is a key element of the compression scheme, this is also where losses might occur (*see* *https://espace.cern.ch/Tracker-Upgrade/Electronics/CIC/Shared%20Documents/Simulation%20studies/FE_inneff_2.pdf*)**

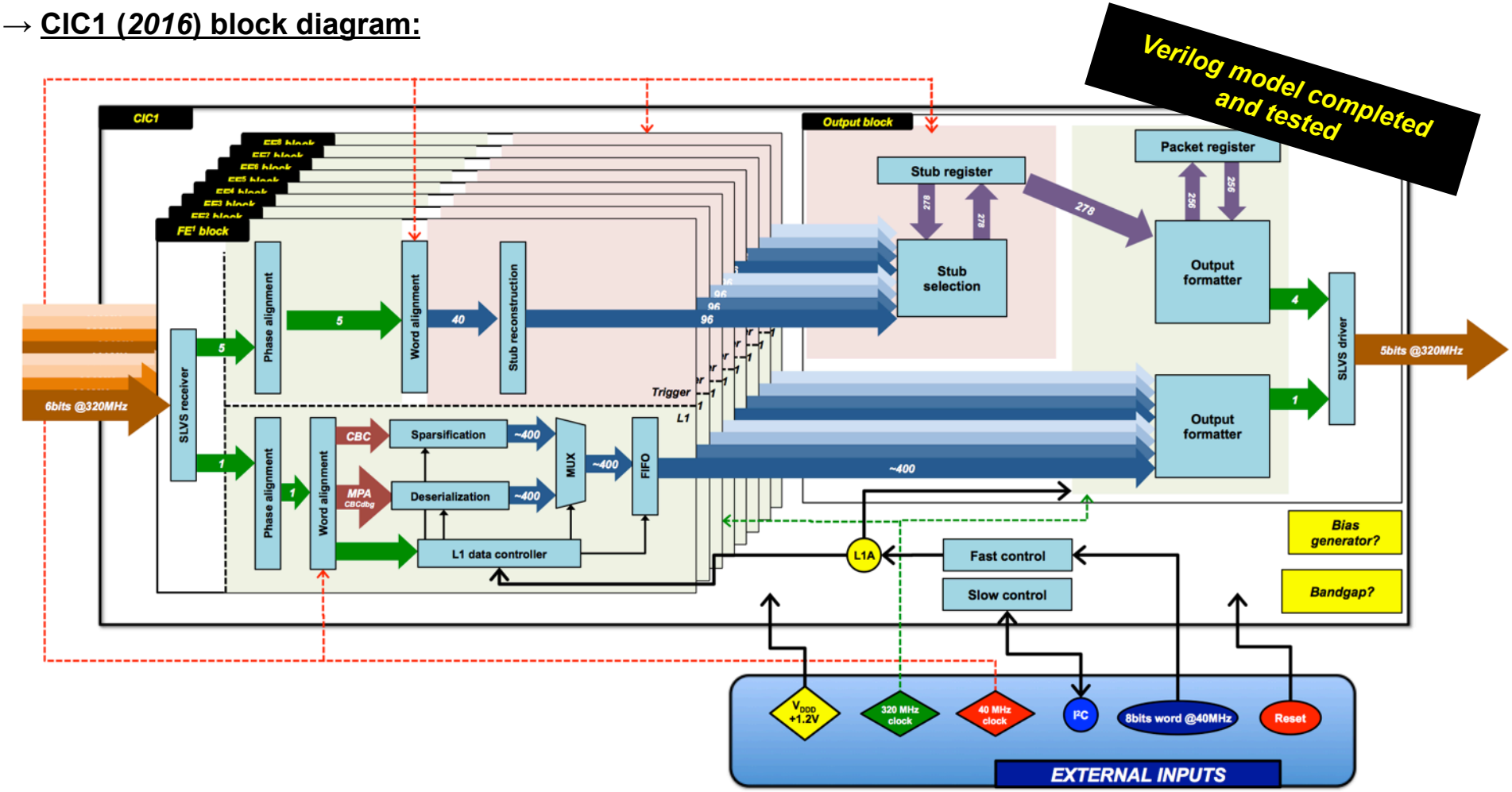
→ **The compatibility challenge:**

→ Every CIC (*65nm technology*) must be able to:

- Receive trigger data from 8 CBC chips (*130nm*)
- Receive trigger data from 8 MPA chips (*65nm*)
- Emit sorted trigger data to the GBT(*65nm*) at 320MHz
- Emit sorted trigger data to the GBT(*65nm*) at 640MHz
- Receive unsparsified L1 data from 8 CBCs
- Receive sparsified L1 data from 8 MPAs
- Emit sparsified L1 data to the GBT at 320MHz
- Emit sparsified L1 data to the GBT at 640MHz
- Emit unsparsified L1 data from the CBC to the GBT at 320MHz
- …

→ This flexibility has an impact on the chip complexity and specification: any change in the readout chain is affecting the CIC

→ **CIC1 (*2016*) block diagram:**



→ **CIC1 will only include the 320MHz output. Foundry planned in 2016.**

→ **Specification document is available:**

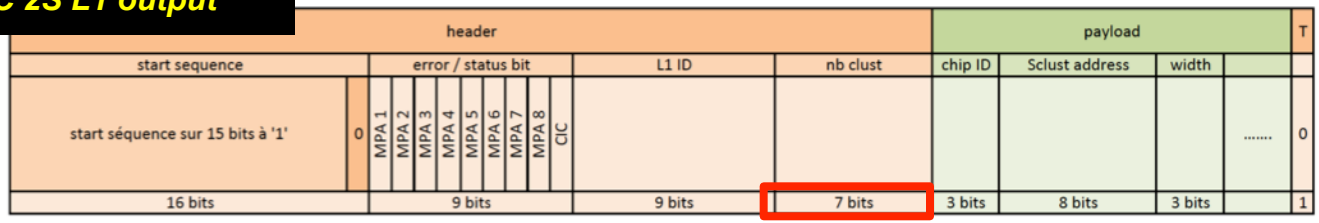
https://espace.cern.ch/Tracker-Upgrade/Electronics/CIC/Shared%20Documents/Specifications/CIC_specs_v1.1.pdf

→ L1 format modifications:

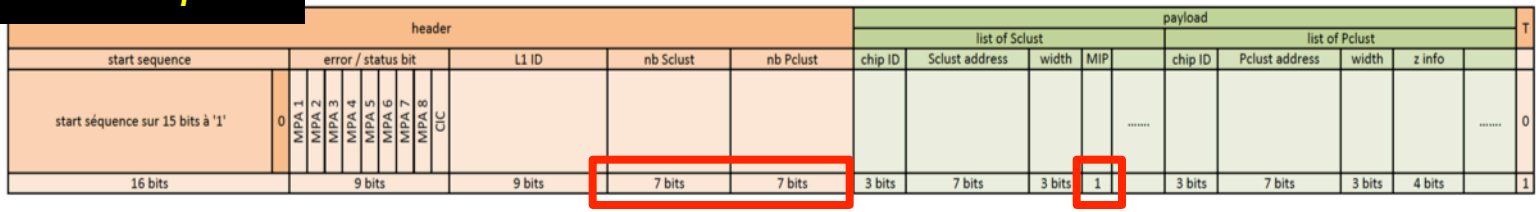
→ **MIP flag** included in the CIC L1 stream (*MPA strip clusters only*).

→ L1 cluster size field of the CIC output were modified (*5 bits was too low*): **all the fields are now 7 bits long.**

CIC 2S L1 output



CIC PS L1 output



→ **No changes in the Trigger output format.**

→ People working on PhaseII DAQ will find all relevant details in the I/O note:
https://espace.cern.ch/Tracker-Upgrade/Electronics/CIC/Shared%20Documents/Data%20formats/CIC_IO_Formats_v3.pdf

→ **Design planning:**

→ **STEP 1:**

→ Block level partitioning of the validated model + final validation with CBC/MPA models (*in 1 month*)

→ Synthesis and physical design of the optimised Verilog code (*FE channel block*) (*in 2 months*)

→ Introduction of test structures at block level

→ **STEP 2:**

→ Integration of the existing blocks (*phase aligner* + *SLVDS TX and RX* + *I2C*) at physical level

→ Design and integration of the FIFO RAM

→ Final synthesis and physical design of the optimised Verilog code (*CIC*)

→ Validation of the physical design with CBC/MPA models

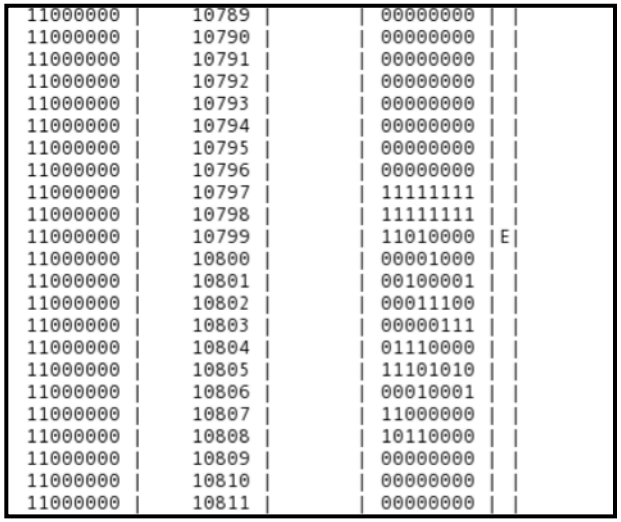
→ Final simulations at physical level

→ These elements being mandatory for the complete CIC1 design, **there will be some delay if they are not available very soon.**

→ Sequence generation tool update:

→ Sequence generation tool has been adapted to the latest format changes. CIC output comparison tool was written (*not on github yet*).

→ Also added some functions to randomly generate errors in the FE output stream



11000000	10789		00000000	
11000000	10790		00000000	
11000000	10791		00000000	
11000000	10792		00000000	
11000000	10793		00000000	
11000000	10794		00000000	
11000000	10795		00000000	
11000000	10796		00000000	
11000000	10797		11111111	
11000000	10798		11111111	
11000000	10799		11010000	E
11000000	10800		00001000	
11000000	10801		00100001	
11000000	10802		00011100	
11000000	10803		00000111	
11000000	10804		01110000	
11000000	10805		11101010	
11000000	10806		00010001	
11000000	10807		11000000	
11000000	10808		10110000	
11000000	10809		00000000	
11000000	10810		00000000	
11000000	10811		00000000	

→ One can select where to add the errors (*headers, cluster size fields, outside data*), in order to test different configurations. Pretty much everything can be added

→ Flipped chips position are marked in the input file, for easy crosscheck

→ Will be available soon in the github version

→ **Reminder, the sequence tool (*TRG and L1*) is documented in part 7 of the following page:**

https://sviret.web.cern.ch/sviret/Welcome.php?n=CMS.HLLHCTuto620

→ It can be easily interfaced to track trigger demonstrators looking for up-to-date input data.

→ CIC1 specifications and verilog model completed. Combined tests (*CBC/CIC, MPA/CIC*) still to be done

→ CIC L1 output format has changed: take note.

→ Chip design is clearly depending on availability of some specific blocks. Geometric constraints need to be known before starting physical design of the blocks at IPNL.