e-Port IP Core

Specifications document

Document History

V0.3 DRAFT

1 Introduction

The e-port IP core is a macro block designed to interface the User Application Logic residing in a generic Front-End ASICs with the Gigabit Transceiver (GBT) chip set via a communication protocol defined by the GBT called "e-link". It implements the e-link electrical interface and a serializer/deserializer block which matches the one contained in the GBT.

2 Features

Electrical interface based on the SLVS electrical protocol (see ref ???).

Synchronous operation at 80, 160 or 320 Mbps.

Deterministic link latency.

Full-duplex bi-directional operation.

GBT interface:

- 3-signal protocol: data input, data output, clock. Clock provided by GBT.

User interface:

- 8-bit data input bus
- 8-bit data output bus
- 40 MHz clock output
- Received clock output

Automatic data synchronization on the serial data input line.

No configuration required. Operation mode obtained by wiring some mode lines at block integration stage.

SEU-robust design.

Low-power design.

Available for ASIC implementation in CMOS 130nm technology.

3 General Description

3.1 Block diagram

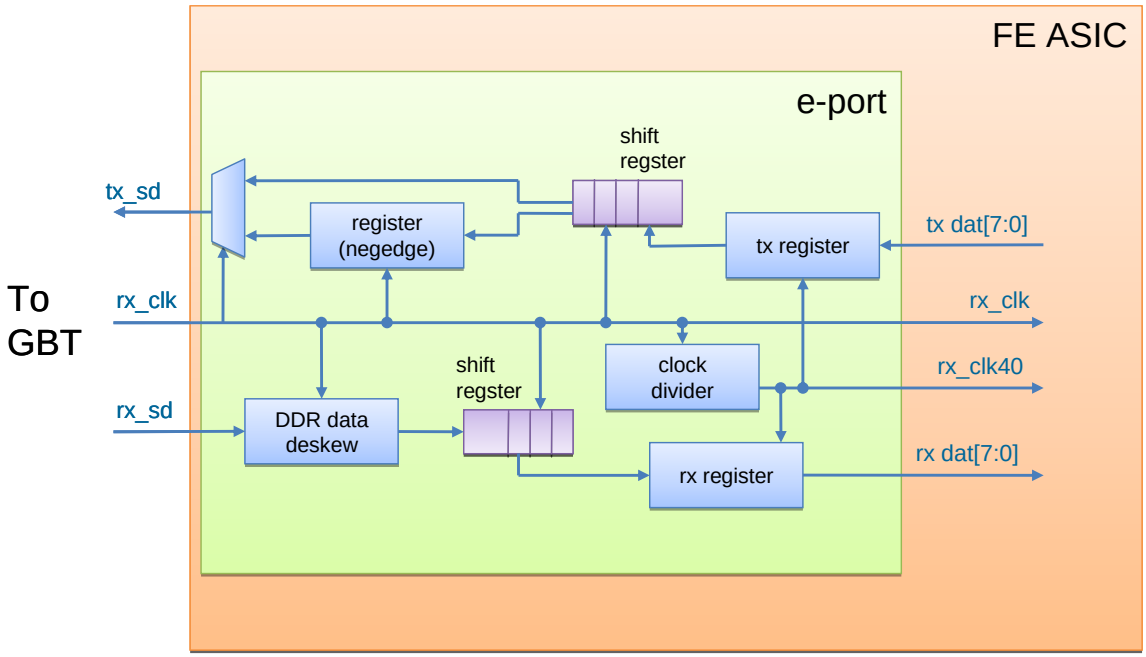

Figure 3-1 Block diagram of the e-port.

3.2 Block configuration mode pins

Parameter	Width	Default	Description
DATA_RATE	2	0x0	Sets the clock divider for the generation of the 40 MHz clock. Set to: ▪ 0 for 80 Mbps; ▪ 1 for 160 Mbps; ▪ 2 for 320 Mbps. ▪ 3 (reserved)

3.3 I/O Signal Description

3.3.1 FE side signals

Port	Width	Directio	Description
rx_clk	1	Output	Received clock
rx_clk40	1	Output	40 MHz received clock
tx_dat	2 @ 80 Mbps 4 @ 160 Mbps	Input	Data to be transmitted. Depending on DATA_RATE, most-significant bits are ignored.
rx_dat	8 @ 320 Mbps	Output	Received data. Depending on DATA_RATE, most-significant bits shall be ignored.

3.3.2 SLVS port connections

Port	Width	Direction	Description
rx_sd	1	Input	Transmitted serial data
tx_sd	1	Output	Received serial data
rx_clk	1	Input	Received clock

4 The e-Port

The e-Port is an IP block implementing serialization/deserialization. A copy of the e-port should be instantiated in the user application ASIC, at the other end of the link. In this case, the data and the clock output are given with a deterministic latency with respect to the off-detector electronics e-link transmit strobe input.

No word or symbol synchronization is provided by the e-Port. No framing is defined at the e-Port level; the user must implement framing if needed.

The e-Port provides serialization/deserialization at double data rate (DDR), therefore the clock frequency is half of the bit rate.