CERN PH-ESE-BE

The Gigabit Link Interface Board (GLIB) specifications

v1.99

2011.05.03

DRAFT

GLIB project homepage: https://espace.cern.ch/project-GBLIB/public

Contact: Paschalis.Vichoudis@cern.ch

Document History

- **v1.99, 2011.05.03:** GLIB team, §2.1, §2.2 (FMC section), §2.4, §2.6, §6 (reference [4]), and Fig. 4-2 modified. Appendix C added. Document template modified.
- **v1.9, 2010.10.07:** Fig. 3-1, Fig. 3-2, Fig. 3-4, §3.2, §3.3, §3.4, Appendix A & B modified.
- **v1.8, 2010.09.20:** Reference to MMC added. Project homepage added. Sections §3.3& §3.5, Fig. 3-1, Fig. 3-3, Fig. 3-11 & Fig. 4-2are modified.
- **v1.7, 2010.09.03:** Fig. A - 2 and Sections §5.2 are modified.
- **v1.6, 2010.09.01:** All figures of Chapter 1 and Appendices A are modified. Fig. 3-2 & Fig. 3-9 are modified. The text of Example1 in Appendix A is modified.
- **v1.5, 2010.08.20:** Section §2.5, Fig. 3-2, Fig. 3-3, Section §3.5, Fig. 3-10, Fig. 3-11, Fig. 4-2 and Appendices A & B are modified.
- **v1.4, 2010.08.13:** Chapter1, Sections §2.2, §3.1, §3.2, §3.6, §3.7, §3.8, Chapter 4 and Appendices A & B are modified. Chapter “Functional” is added. The numbering scheme of figures and tables has changed.
- **v1.3, 2010.05.31:** Colours of Fig.2, 15 & 16 changed. Minor correction in Fig.12. §2.5 modified. References changed accordingly.
- **v1.2, 2010.05.12:** The “Powering” section is slightly modified. Chapter 3 renamed to “Electrical”. The order of the sections in Chapter 3 is changed. Examples of typical GLIB use are added. Ambiguous sentences rephrased in few locations.
- **v1.1, 2010.05.06:** The XC2C64A CPLD is replaced by a XC2C128. A preliminary components list is added in Appendix B. §3.3 text, Fig.5 and §3.4 text are modified. Text is added in §3.1. The “Configuration and Testability” chapter is moved under Chapter 3 (as §3.8) and its text and associated Fig.12 are modified. Chapters “Mechanical” and “References” are now Chapter 4 and 5, respectively. Typos corrected in several locations.
- **v1.0, 2010.05.04:** Fig.3, 4 and 12 of v0.9 modified. Chapter 4 renamed to “Configuration and Testability” and expanded accordingly. Section “Module Management” added. Section “Examples of the GLIB use” moved to Appendices. SRAM type mentioned in §2.3.
- **v0.9, 2010.04.28:** Introduction has been added. Figures have been numbered. Page numbers have been added in the table of contents.
- **v0.8, 2010.04.23:** First draft in the document history.

GLIB team

- Sophie Baron, Manoel Barros Marin, Vincent Bobillier, Stefan Haas, Magnus Hansen, Markus Joos, Francois Vasey & Paschalis Vichoudis.

Table of Contents

1.INTRODUCTION

The Gigabit Link Interface Board (GLIB) is an evaluation platform and an easy entry point for users of high speed optical links in high energy physics experiments. Its intended use ranges from optical link evaluation in the laboratory, to control triggering and data acquisition from remote modules in beam or irradiation tests. The GLIB is a double width Advanced Mezzanine Card (AMC) conceived to serve a small and simple system residing either inside a µTCA crate or on a bench with an optional serial link to a PC.

Each GLIB card can process data to/from four SFP+ transceiver modules, each operating at bi-directional data rates of up to 6.5 Gbps. This performance matches comfortably the specifications of the GBT/Versatile Link project [1][2] with its targeted data rate of 4.8 Gbps. In its simplest form, one GLIB board thus interfaces with up to four GBT channels.

Fig. 1-1 highlights the baseline configuration of a GBT-Versatile Link-GLIB system, where the GLIB converts data to/from the optical domain, implements the GBT protocol and codes/decodes the user payload at the link back-end.

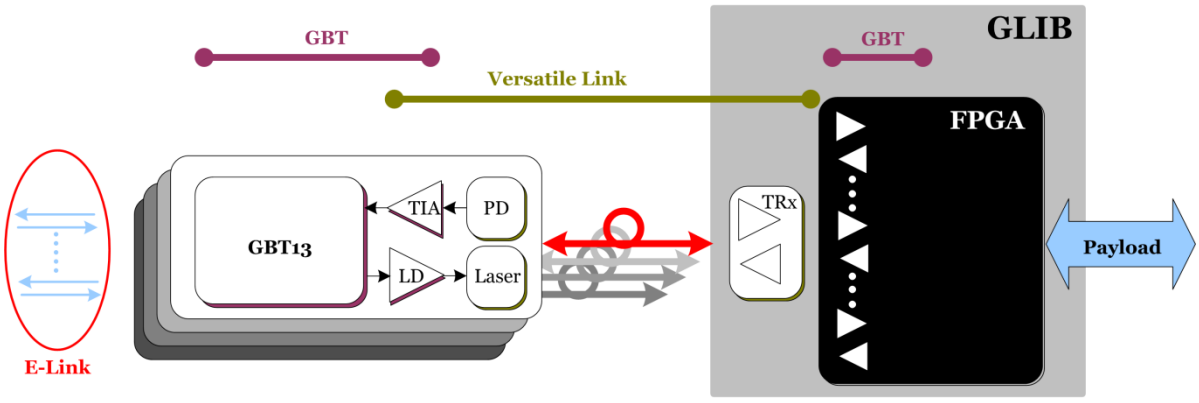

Fig. 1-1: The GLIB board in a GBT-Versatile Link system

The GLIB I/O capability can be further enhanced with two FPGA Mezzanine Cards (FMCs). This gives users the flexibility to adapt the GLIB interface to their system, by for instance adding connectivity to the TTC network at the backend, or connecting to e-links at the frontend. Fig. 1-2 illustrates a case where two GLIB boards are interconnected back-to-back, allowing implementing and experimenting with GBT-based systems well before full-fledged GBT ASICs become available.

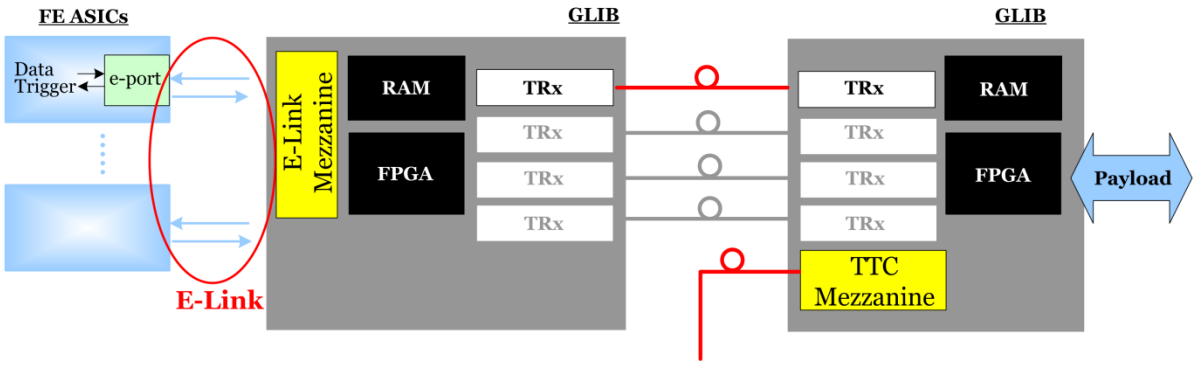

Fig. 1-2: Back-to-back interconnected GLIB boards with customization mezzanines (TTC and E-Link) drawn in yellow.

2.FEATURES

2.1 Overview

- General purpose double width AMC module for µTCA environment or bench-top use.
- Based on a high-performance Virtex-6 FPGA with up to 6.5Gbps transceivers.
- Up to four optical transceiver links on-board.
- Sockets for two expansion FMCs for user-specific I/Os and up to four additional 6.5Gbps transceiver lines (optional).

2.2 Interfaces

Optical

- Four cages for up to four hot-pluggable single-channel SFP+ transceiver modules (rated at 10Gbps) compatible with the GBT/versatile link.

AMC

- Port [0-1]: GbE.
- Port [4-7] (Fat Pipe): PCIe x4 GEN2. Possibility to implement other protocols.
- Port [8-11] (Extended Fat Pipe): PCIe x4 GEN2. Possibility to implement other protocols.
- Port [2:3]: LVDS I/O pairs. Possibility to implement other differential I/O standards.
- Port [12-15]: LVDS I/O pairs. Possibility to implement other differential I/O standards.
- Port [17-20]: M-LVDS.
- CLK1/TCLKA: M-LVDS clock input/output.
- CLK2/TCLKB: M-LVDS clock input/output.
- CLK3/FCLKA: HCSL/M-LVDS clock input.

FMC

- High-pin count (HPC) sockets rated at 18Gbps [3] for hosting up to two FMC mezzanines.
- Each HPC socket provides up to 160 user-specific I/Os (that can be configured both as single-ended or differential pairs) as well as 2 differential clock inputs and 2 differential clock outputs. The targeted I/O data rate is 320Mbps.
- One FMC (referred-to as primary or FMC#1) is accessible from the front panel while the other one (referred-to as secondary or FMC#2) is accessible from the rear.

- The primary FMC also provides four optional high-speed (up to 6.5Gbps) transceiver lines. No components will be placed under it to allow the use of optical transceiver modules that possibly violate the FMC specification's maximum I/O depth of 31mm.
- The two FMCs are not powered separately and therefore cannot be turned on/off independently. Additionally, the VADJ power lines are connected to 2.5V.

PC (only in bench-top operation)

- GbE RJ45 socket (1000BASE-T).
- PCIe 4x GEN2 adapter board.
- Possibility to implement additional PC interfaces on the FMC mezzanines.

2.3 On-board memory

- Two 72Mb (2M x 36bit) SRAM devices (CY7C1470 by Cypress) operating at up to 250MHz.

2.4 FPGA

- FPGA family: XILINX Virtex-6 LXT.
- FPGA device: VLX130T-1FF(G)1156C (speed grade:-1)
  - 600 I/O that can be configured to various differential or single-ended standards.
  - 4 Ethernet MAC and 2 PCIe Hard-IP blocks.
  - 20 5Gbps transceivers (MGTs) organized in 5 quads.
    - One MGT quad for the SFP+ modules.
    - One MGT quad for the optional FMC#1 transceivers.
    - One MGT quad for the AMC Port [4:7].
    - One MGT quad for the AMC Port [8:11].
    - One MGT quad for the AMC Port [0:1].
  - ~10Mb of block RAM.

2.5 Module Management Controller (MMC)

- Small footprint Mezzanine card [4] based on an ATMEL ATmega128L microcontroller.

2.6 Expansion/Upgradeability

- The system I/Os can be customized via FMC mezzanines.
- Possibility to use one of the following pin-to-pin compatible FPGAs:
  - VLX195 (~50% more logic resources, ~12Mb block RAM)
  - VLX240 (~85% more logic resources, ~14Mb block RAM)
  - VLX365 (~180% more logic resources, ~14Mb block RAM)
  - VSX315 (~140% more logic resources, ~25Mb block RAM)
- For 6.5Gbps transceivers (and faster logic), there is the possibility to use the compatible FPGAs with -2 or -3 speed grade (e.g. VLX130T-2FF(G)1156C).
- Possibility to use up to 1.125Gb SRAM devices once available.

3. ELECTRICAL

3.1 Architecture

Fig. 3-1 illustrates a block diagram of the GLIB architecture, where all major interconnections are shown.

- The clock distribution circuitry is presented in §3.2.
- The module management features are mentioned in §3.3.
- The JTAG circuitry is shown in §3.4.
- Various uses of the FMC sockets are proposed in §3.5.
- Some details concerning the powering of the system are provided in §3.6.
- The requirements of the µTCA environment are mentioned in §3.7 and §3.8.

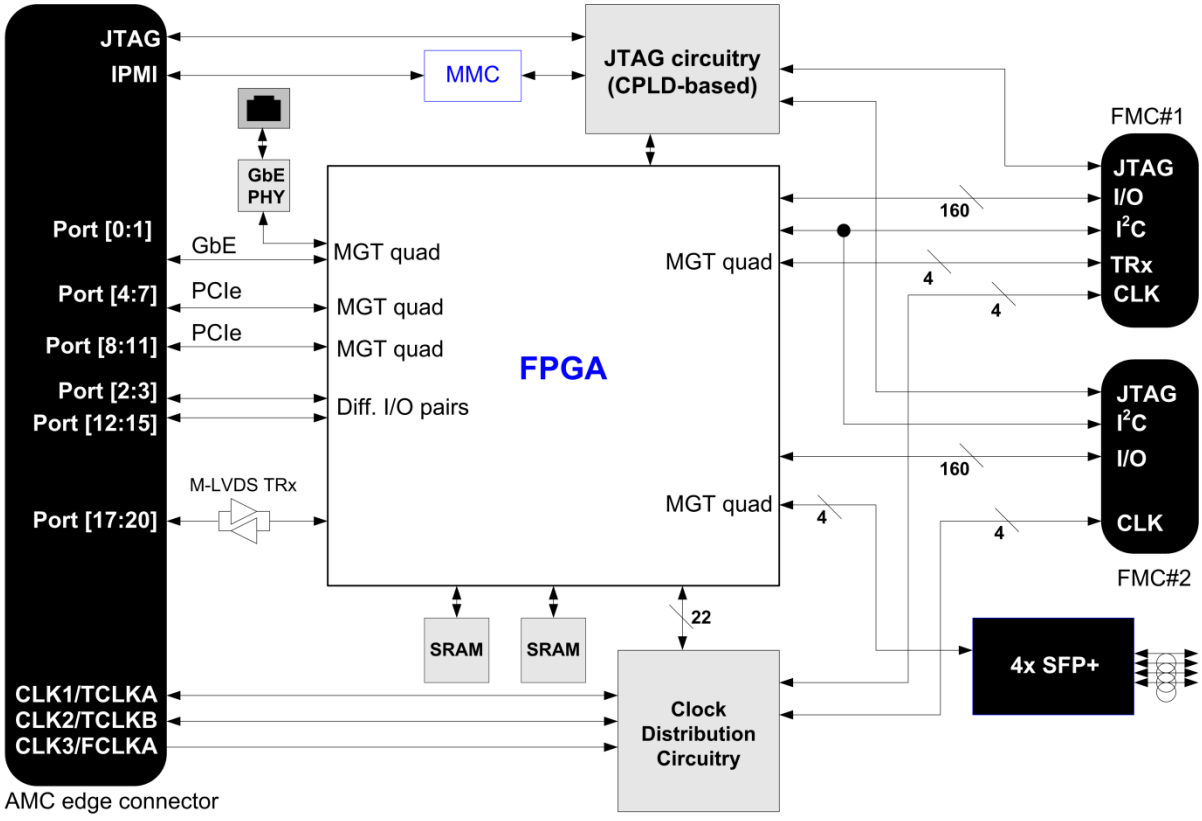

Fig. 3-1 : Block diagram of the GLIB AMC card.

3.2 Clock distribution

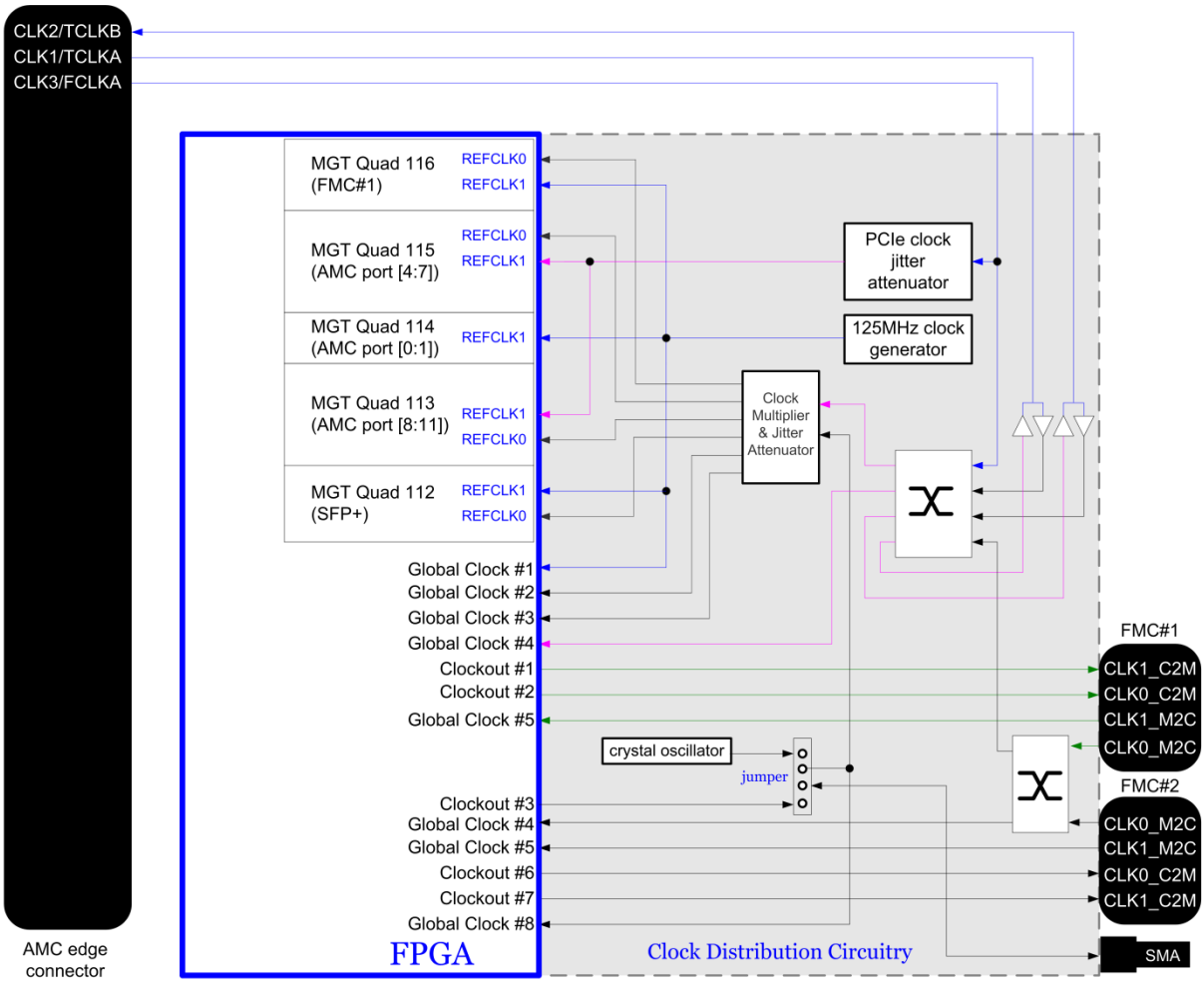

Fig. 3-2 : The clock distribution scheme.

- When the reference clocks of MGT quads are driven through the AMC edge connector, the use of jitter attenuators is strongly recommended by the FPGA vendor.
- The use of external clock multipliers is required in case the reference clocks of the MGTs are below 100MHz.
- The use of the external clock multipliers gives flexibility in the configuration of the MGTs, since depending on the preferred communication protocol different reference clocks are often required.
- A dedicated clock jitter attenuator is also used for PCIe applications.
- Each MGT Reference clock (REFCLK) can be used to clock its neighbouring MGTs (e.g. the MGT114 REFCLK0 can also clock the MGT quads 113 and 115. Details about the Virtex-6 clocking resources can be found in [5].
- The GLIB carries a 125MHz clock generator and a 40MHz crystal oscillator for stand-alone operation. Additionally, it can receive external clock through the front panel's SMA connector. Note that the SMA connector can also be used as a clock output.

3.3 Module Management

- Based on a Small footprint Mezzanine card [4].
- IPMI interface, geographical addressing and automatic module detection support.
- Hot swap support (by checking the state of the front Panel's module handle switch).
- Control of the front panel LEDs according to the specification.
- Monitoring of the on-board temperature and voltage regulation.
- Communication with CPLD through six I/O.

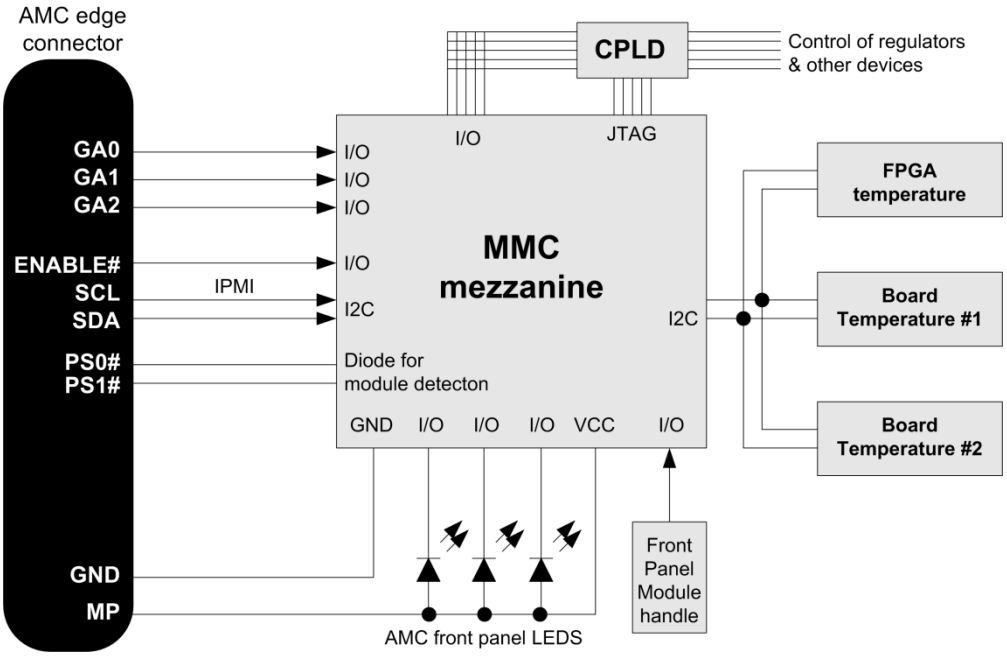

Fig. 3-3 : Module Management Controller circuitry.

3.4 Configuration and Testability

- The JTAG circuitry supports both device configuration and Boundary Scan testing.
- The JTAG circuitry is based on a XC2C128 Coolrunner-II CPLD with 80 I/O that is used as JTAG switch in order to provide various JTAG chain options.
- The device configuration options provided are:
  - Configuration of FPGA and FPGA EEPROM: by the JTAG header#2 or the AMC edge connector JTAG or the AMC edge connector I2C (through MMC). Additionally, the FPGA EEPROM can be configured by the AMC Port[0:1] (through FPGA). Note that the FPGA EEPROM will have two pages in order to allow reverting to a previous working FPGA firmware (in case of failure).
  - Configuration of MMC: by the dedicated connector of the MMC mezzanine.
  - Configuration of CPLD: by the JTAG header#1 (for safety reasons).
- For testability reasons, all other ICs on-board supporting Boundary Scan testing are chained and connected to the JTAG switch. The Boundary Scan testing procedure is to be defined.

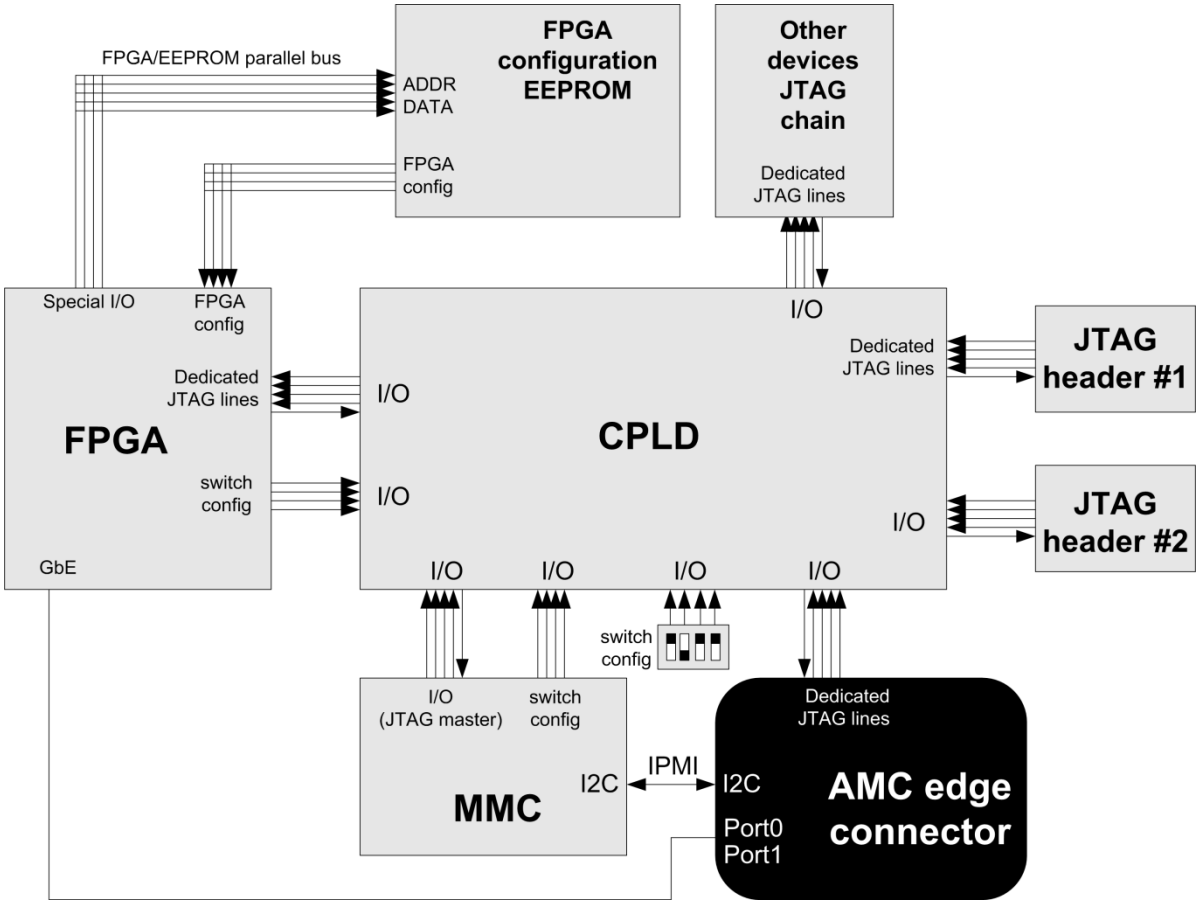

Fig. 3-4 : JTAG circuitry, for configuration and testability.

3.5 Mezzanine cards

The GLIB AMC card FMC connectors are of type Samtec SEAF-40-S-06.5-10-A. The mating connectors of the FMCs are of type Samtec SEAM with 10mm and 13mm stacking height. Typical FMC functionalities could be:

- "TTC mezzanine", for timing/trigger/clocking signals distribution (see Fig. 3-5). Alternatively, commercial Clock and Data Recovery ICs could be used instead of the custom ASICs shown.
- "High density E-Link Mezzanine", with two VHDCI connectors, each carrying 11 E-Links (see Fig. 3-6).
- "Low density E-Link Mezzanine", with four HDMI connectors, each carrying 1 E-Link (see Fig. 3-7).
- "GBTX Parallel Bus mezzanine", providing access t0 the 40+40bits of the GBTX parallel bus (see Fig. 3-8).
- "USB3.0 mezzanine", for high-speed connection to PC (see Fig. 3-9).
- "Optical interface extension mezzanines" equipped with SFP+, QSFP, partially connected SNAP12, XPAK or other optical module types (see Fig. 3-10), in order to take advantage of the four additional 6.5Gbps transceiver lines provided by the primary FMC socket. Various protocols could be implemented (e.g. 10GbE).

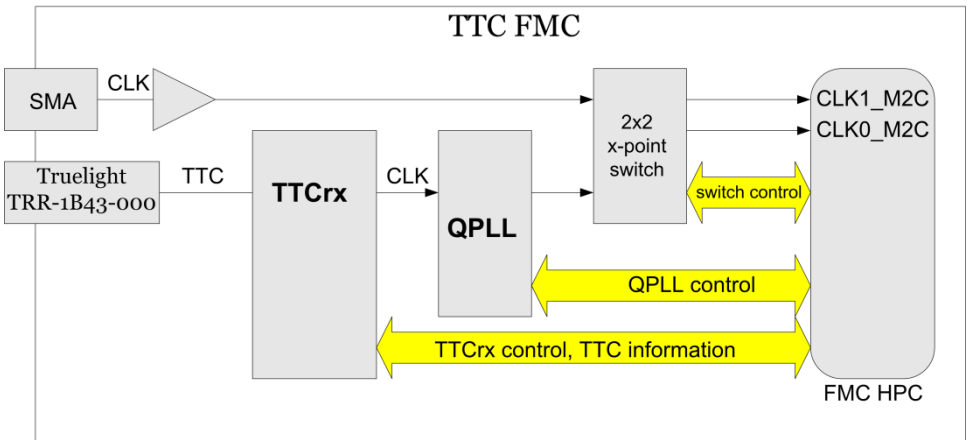

Fig. 3-5 : Block diagram of the TTC FMC.

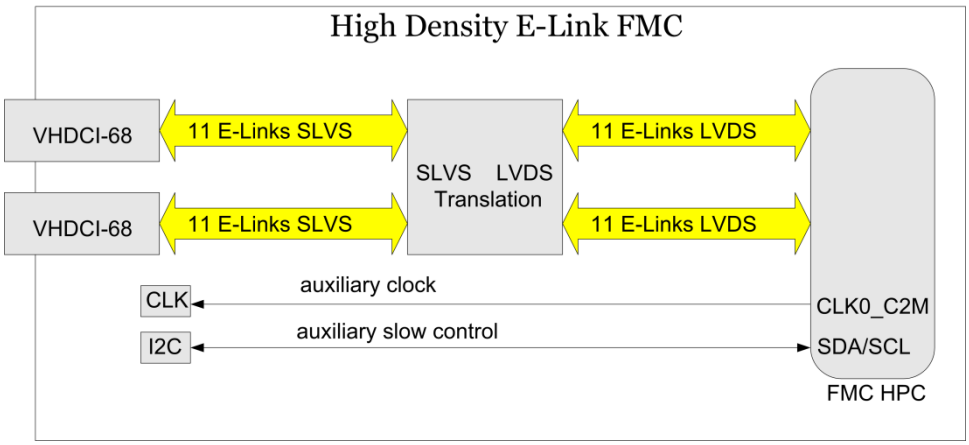

Fig. 3-6 : Block diagram of the High Density E-Link FMC.

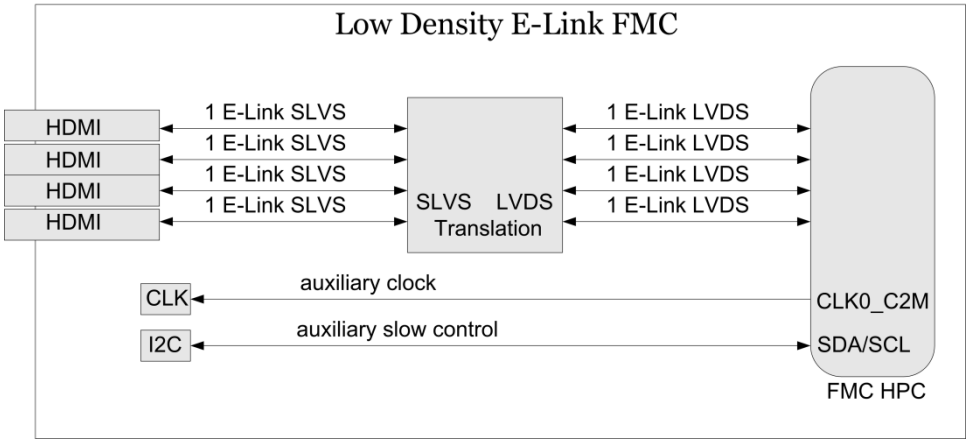

Fig. 3-7 : Block diagram of the Low Density E-Link FMC.

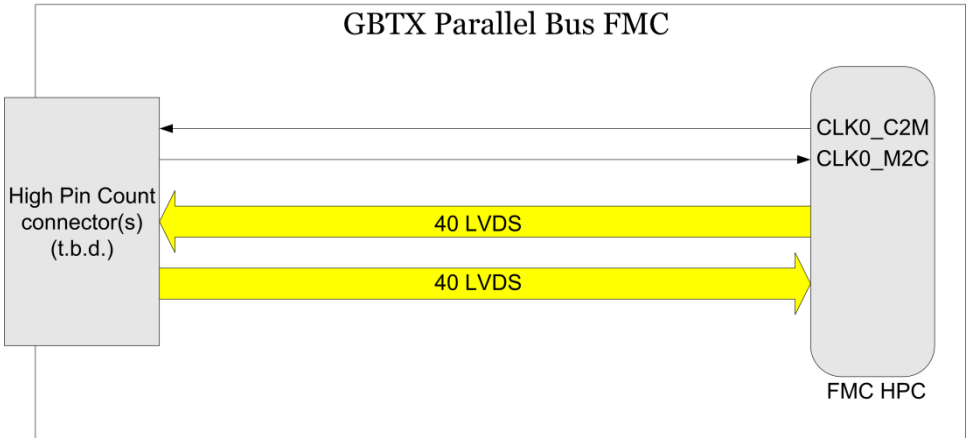

Fig. 3-8 : Block diagram of the GBTX Parallel Bus FMC.

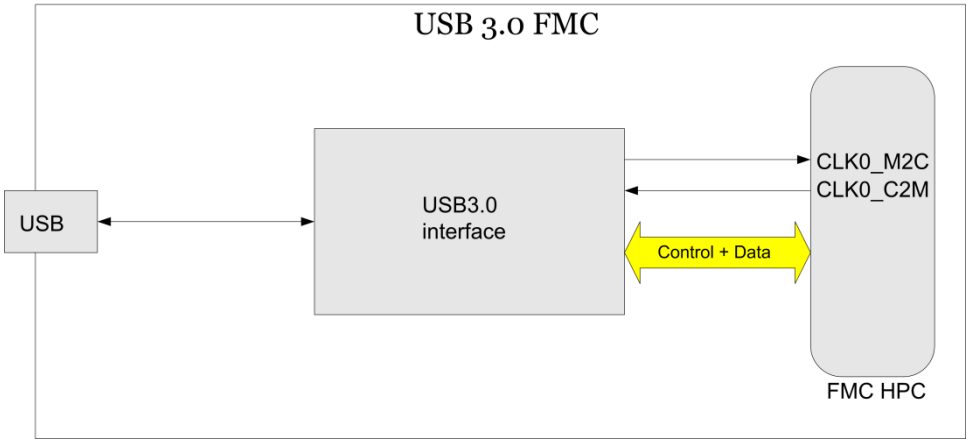

Fig. 3-9 : Block diagram of the USB3.0 FMC.

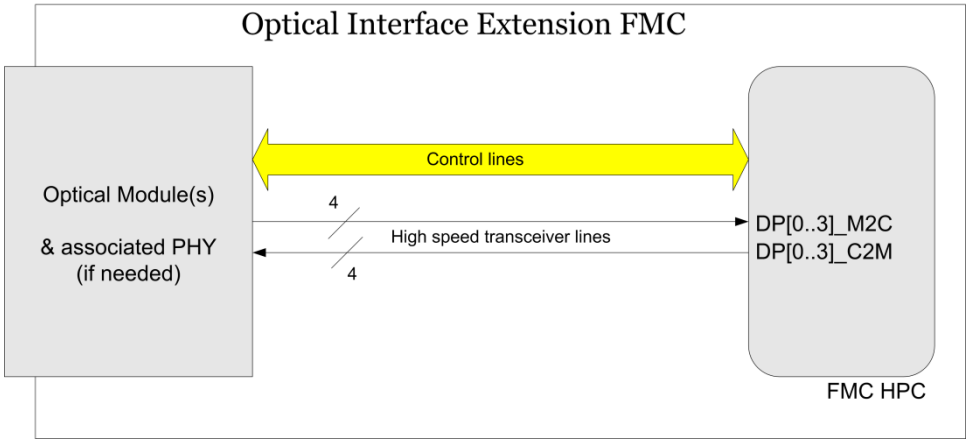

Fig. 3-10 : Block diagram of an optical interface extension FMC.

3.6 Powering

- The 3.3V management power (MP) provided by the AMC edge connector is used for the powering of the MMC and the CPLD while the 12V payload power (PWR) is used for the powering of all other components. Additionally, a connector for powering the GLIB in bench-top operation is also available. The powering scheme incorporating the LT3021 and MAX8556 linear regulators, the LTM4601 and LTM4606 switching regulators and the LTC6902 multi-phase oscillator is shown in Fig. 3-11.

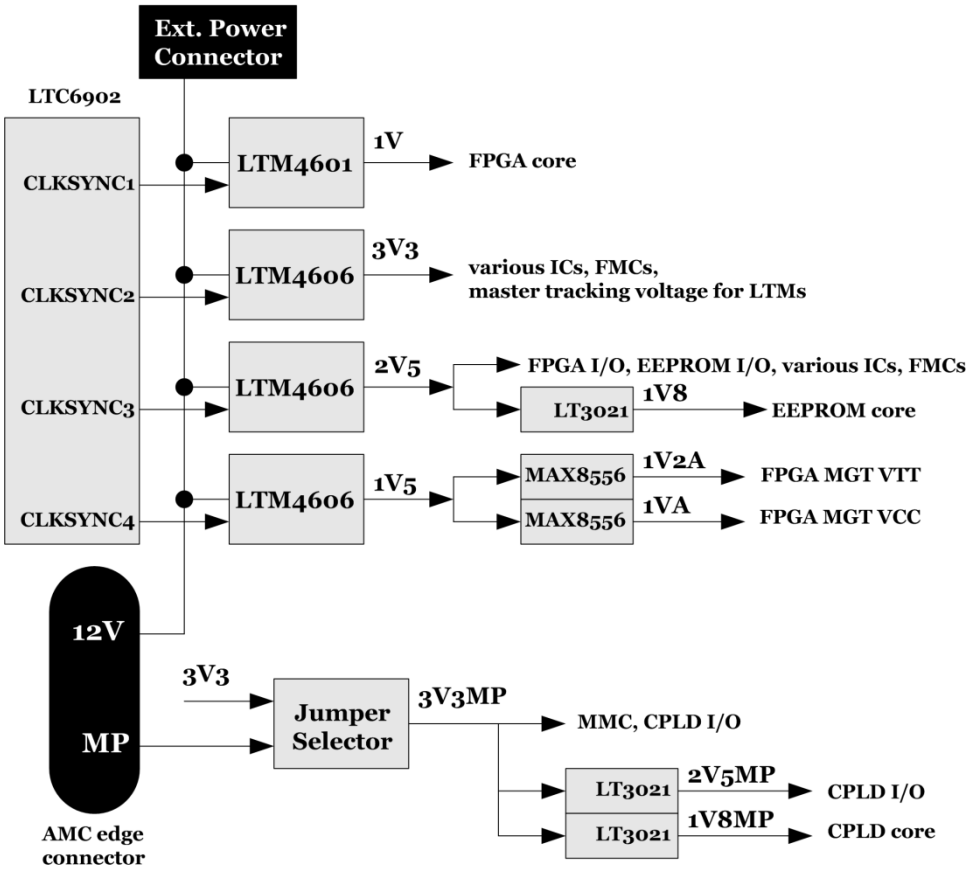

Fig. 3-11 : The powering scheme.

- A header for the powering of an optional fan for the cooling of the FPGA is also available.

3.7 MCH requirements

- GbE interface on MCH Fabric[A].
- PCIe Fabric clock to the MCH CLK3 (and/or MCH CLK1).
- Ability to receive the MCH CLK1 or MCH CLK2 (driven by an AMC card) and forward it to MCH CLK1 and/or MCH CLK3.
- Ability to receive clock from External CLK input and forward it to the MCH CLK1 and/or MCH CLK3.

- Note that the selection of the appropriate MCH Fabric[D:G] depends on the configuration of Port[4:7] and Port[8-11].

3.8 Backplane requirements

No special requirements for the backplane.

- For a non-redundant backplane architecture:
  - MCH 1 Fabric[A] routed to AMC Port[0] for all µTCA slots.
  - MCH 1 Fabric[D:G] routed to AMC Port[4:7] for all µTCA slots.
  - The MCH CLK1 and CLK3 drive the AMC [1:12] CLK1/TCLKA and CLK3/FCLKA, respectively, while the MCH receives the AMC CLK2/TCLKB from all µTCA slots.
- For a redundant backplane architecture:
  - MCH 1 Fabric[A] routed to AMC Port[0] for all µTCA slots.
  - MCH 1 Fabric[D:G] routed to AMC Port[4:7] for all µTCA slots.
  - MCH 2 Fabric[A] routed to AMC Port[1] for all µTCA slots.
  - MCH 2 Fabric[D:G] routed to AMC Port[8:11] for all µTCA slots.
  - The MCH1 CLK1 drives the AMC[1:6] CLK1/TCLKA and the MCH2 CLK1 drives the AMC[7:12] CLK3/FCLKA, while the MCH1 and MCH2 receive the AMC CLK2/TCLKB from all µTCA slots.
- GLIB is compatible with the µTCA Physics backplane.

4. MECHANICAL

- Double width, mid- or full- size AMC module (depending on configuration). Extended card-edge interface (two-sided, 170-pin).
- The PCB dimensions are shown in Fig. 4-1 (Component Side2 view).
- The floor-planning of the Component Side1 is shown in Fig. 4-2.
- All remaining components not shown in the floor-planning of Component Side1 (e.g. the clock distribution circuitry) are accommodated in Component Side2 since they are low-profile. The floor-planning of the Component Side2 is to be defined.

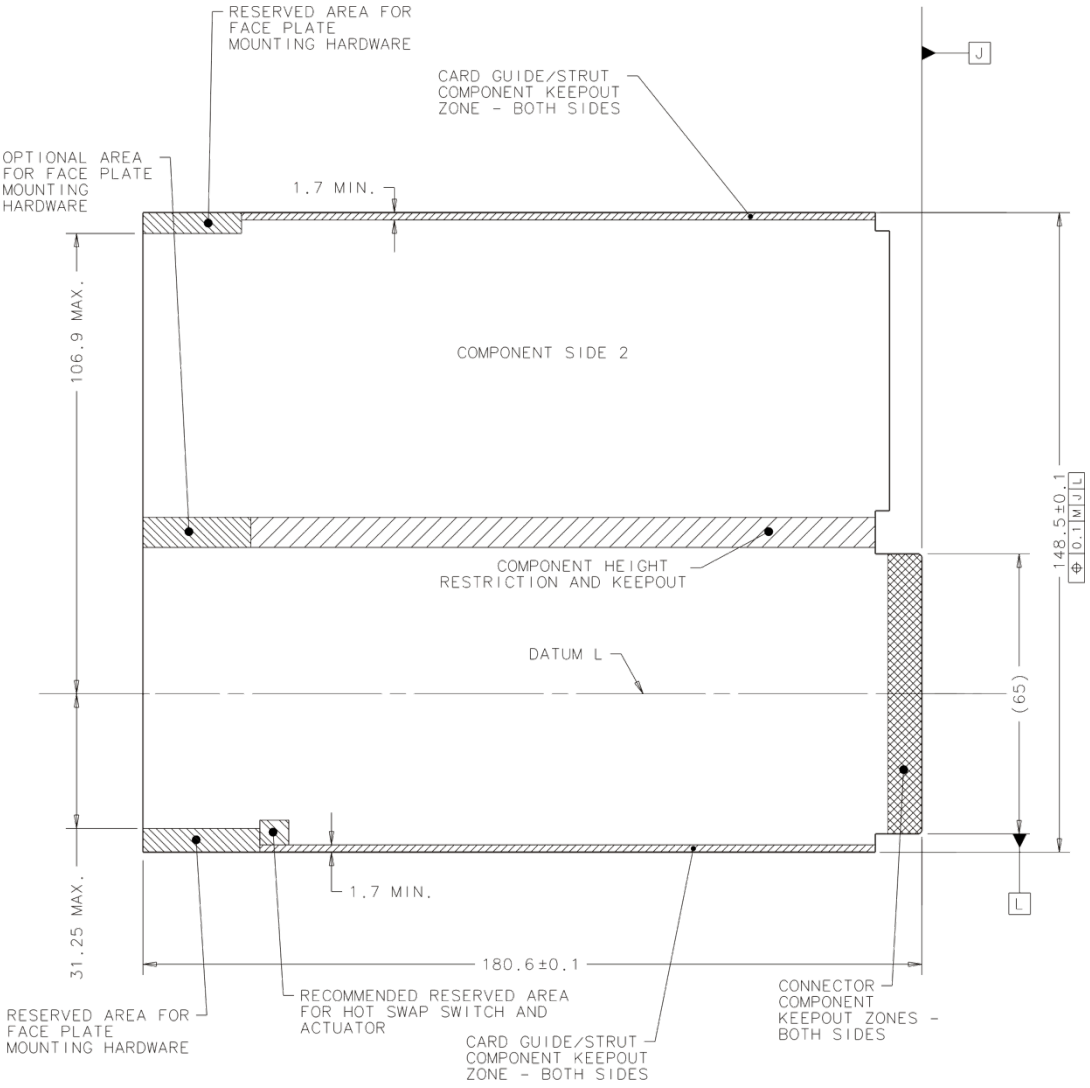

Fig. 4-1 : Double width AMC module PCB dimensions, Component Side 2 (bottom) view [6].

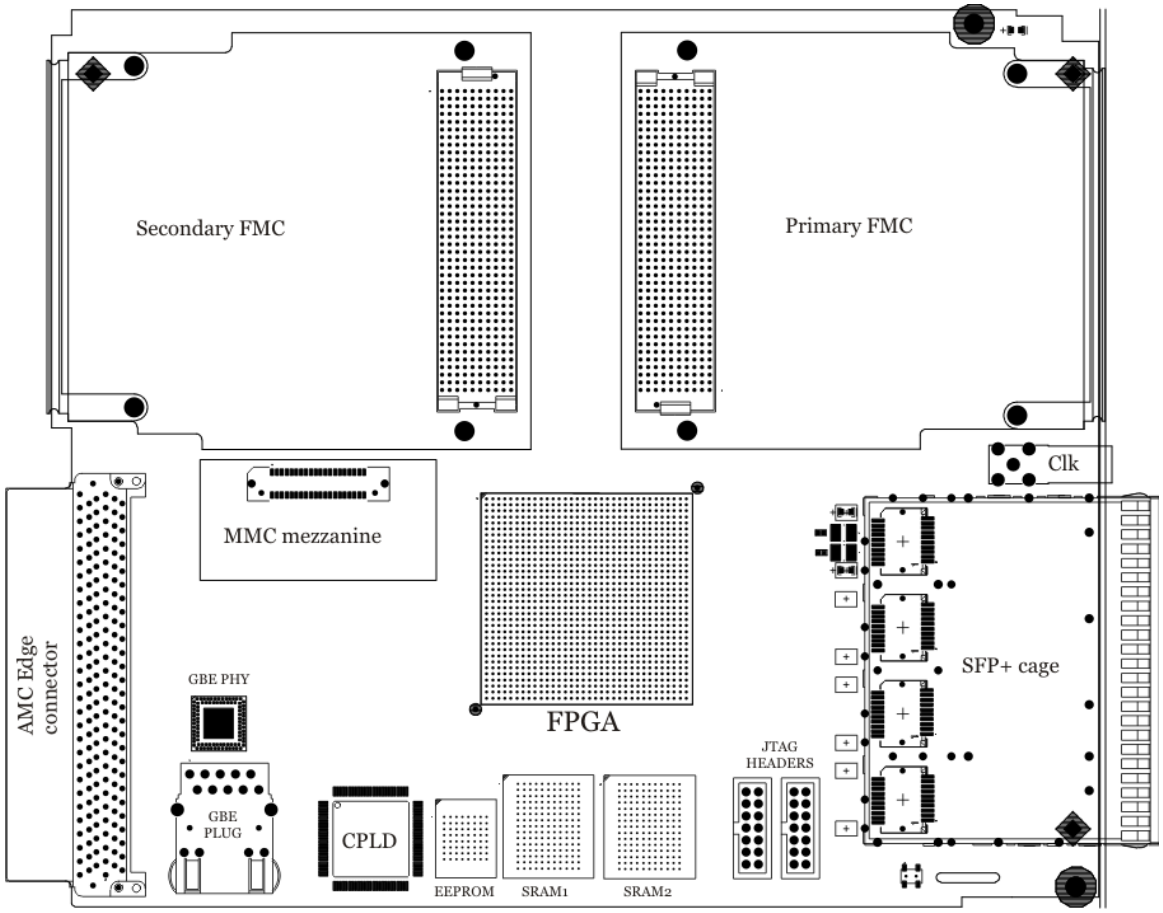

Fig. 4-2 : The GLIB floor planning, Component Side 1 (top) view.

5.FUNCTIONAL

5.1 Firmware Architecture

Fig. 5-1 shows the GLIB FPGA firmware architecture. The principle components are:

- The GbE interface (UDP protocol will be used).
- The Fat Pipe interfaces. Different flavors will be implemented.
- The external SRAM interface.
- The controller of the clock distribution circuit.
- The interfaces to the FMC mezzanines. Different flavors will be implemented depending on the hardware.
- A general purpose pattern generator.
- The GBT IP [7].
- The user logic block. This contains the treatment of the GBT payload, and differs depending on the application.

As shown in Fig. 5-1, most of the firmware blocks are attached to the FPGA local bus. The FPGA local bus is controlled either by the GbE or the Fat Pipe interface (depends on the user logic implementation).

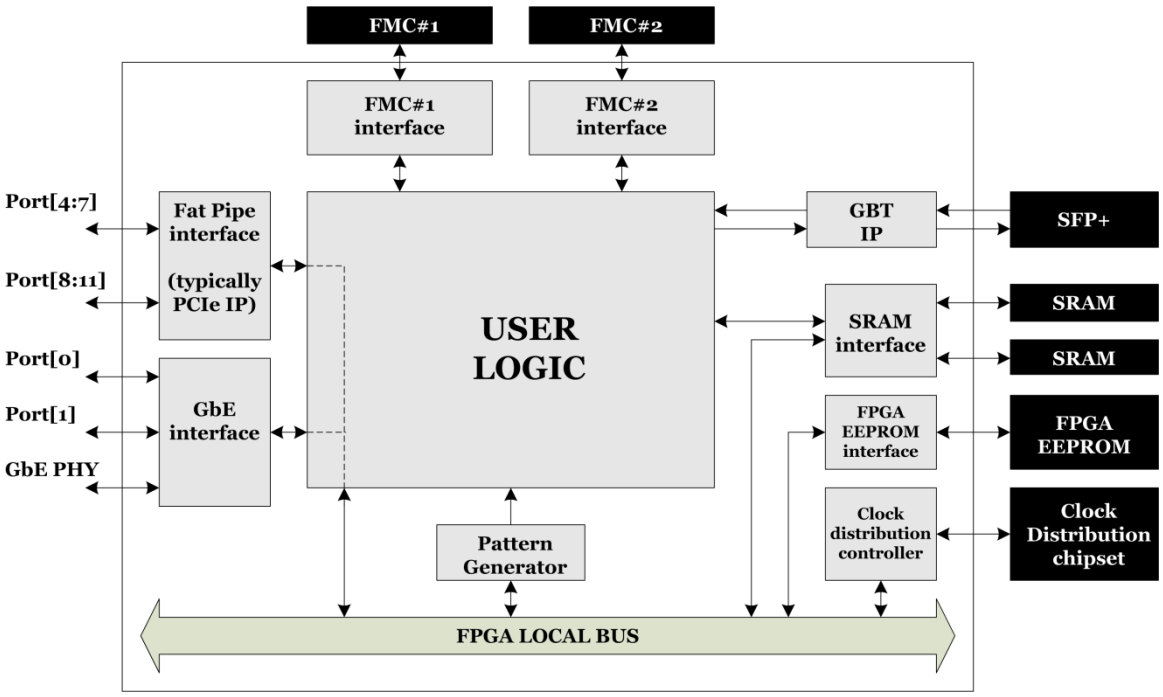

Fig. 5-1 : Firmware Architecture.

All firmware blocks illustrated will be provided and supported by the GLIB team, except of the user logic and the GBT IP blocks. However, few implementation examples including the user logic and the GBT IP blocks will also be provided.

5.2 Bandwidth Considerations

PCIe

- PCIe Transfer Rate: 2.5Gbps/lane for GEN1, 5.0Gbps/lane for GEN2 (per direction).
- PCIe Maximum Data Throughput (write) = 68.8% of PCIe Transfer Rate [8].
- PCIe Maximum Data Throughput (read) = 60.8% of PCIe Transfer Rate [8].
- GLIB PCIe links: Up to two PCIe x4 (GEN1 or GEN2).

GbE

- GbE Transfer Rate: 1.25Gbps (per direction).
- GbE Theoretical Bandwidth: 1.0Gbps.
- GbE Maximum Data Throughput: 800Mbps [9].
- GbE Maximum Data Throughput using existing Hardware Access Library (HAL) software/firmware: 200Mbps [10]& [11].

GBT

- GBT Transfer Rate: 4.8Gbps (per direction).
- GBT Data/TTC/EC throughput = 3.2Gbps.
- GBT Slow control throughput = 80Mbps.
- GBT control throughput = 80Mbps.
- GLIB GBT links: Up to four (plus up to additional four on the FMC#1).

E-Link

- 80Mpbs or 160Mbps or 320Mbps (configurable) [12].
- GLIB E-Links: Up to 22 per FMC.

Others

- Max GBT Event Size (assuming 100KHz trigger rate) = 3.2Gbps/100KHz=32Kbit.
- GLIB Storage capacity (assuming Max Event Size) = 144Mbit/32Kbit=4500 events.

6. REFERENCES

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[12] *Paulo Moreira, "GBT specifications draft v1.2"*

https://espace.cern.ch/GBT-Project/GBTX/Specifications/gbtxSpecsV1.2.pdf

APPENDIX A: TYPICAL GLIB USE CASES

EXAMPLE1: GLIB as Back-End system, bench-top mode.

The GLIB is operating in bench-top mode. An external power supply is used. For the reception of timing/trigger information, the GLIB is equipped with a TTC mezzanine. The GLIB communicates with the front-end via GBT links. In Fig. A - 1, the configuration of the GLIB as well as the transfer of the GBT payload from/to the PC is done through a GbE connection. The SRAM can be used for intermediate storage, if necessary. Fig. A - 2 and Fig. A - 3 show two different flavors of the GLIB as back-end system in bench-top operation. In Fig. A - 2, the configuration of the GLIB as well as the transfer of the GBT payload from/to the PC is done through the GLIB PCIe adapter. In Fig. A - 3, the GLIB is equipped with an Optical Extension mezzanine providing a fast optical interface (e.g. 10GbE) for the transfer of the GBT payload.

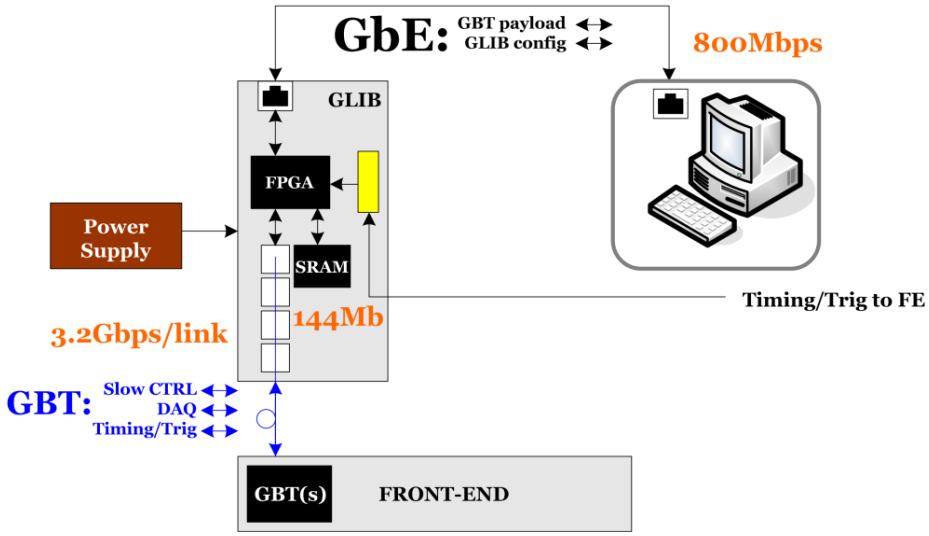

Fig. A - 1 : Example of the GLIB as back-end system. Mode: bench-top. Payload interface: GbE.

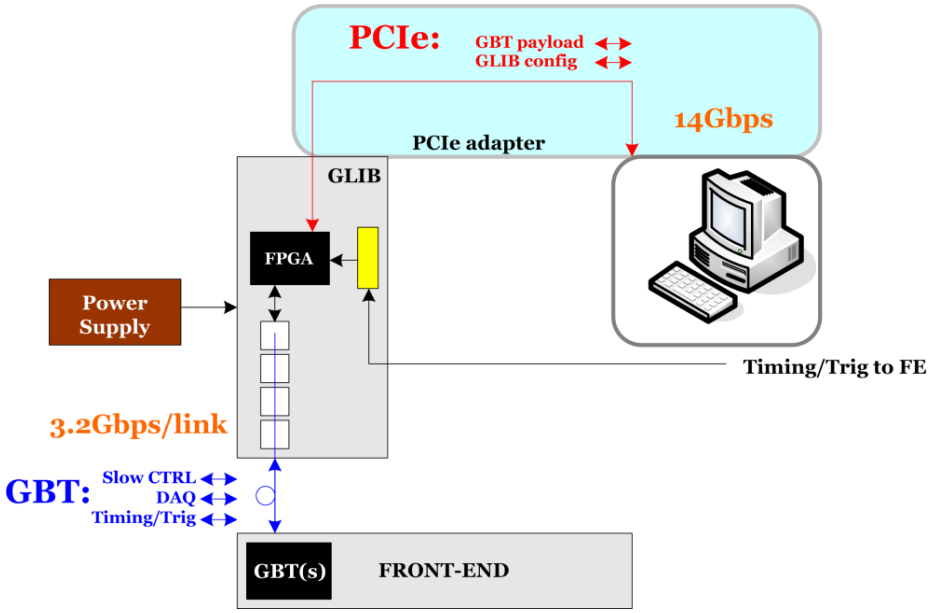

Fig. A - 2 : of the GLIB as back-end system. Mode: bench-top. Payload interface: PCIe.

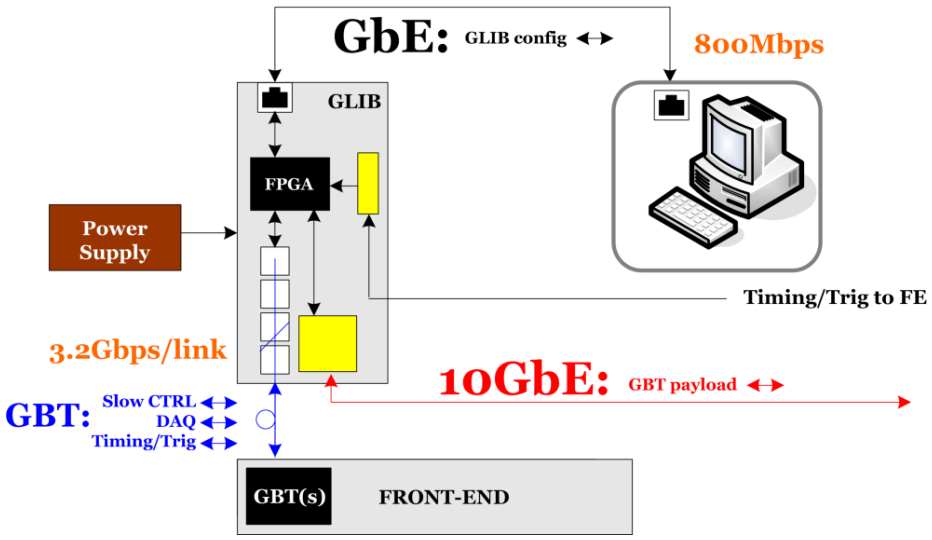

Fig. A - 3 : Example of the GLIB as back-end system. Mode: bench-top. Payload interface: 10GbE.

EXAMPLE2: GLIB interfacing directly with Front-End chips, bench-top mode.

The GLIB is operating in bench-top mode. An external power supply is used. For the reception of timing/trigger information, the GLIB is equipped with the TTC mezzanine. For the direct communication with the front-end chips (without the use of GBT), the GLIB is also equipped with an E-Link mezzanine. The configuration of the GLIB as well as the transfer of the GBT payload from/to the PC is done through a GbE connection. The SRAM can be used for intermediate storage, if necessary.

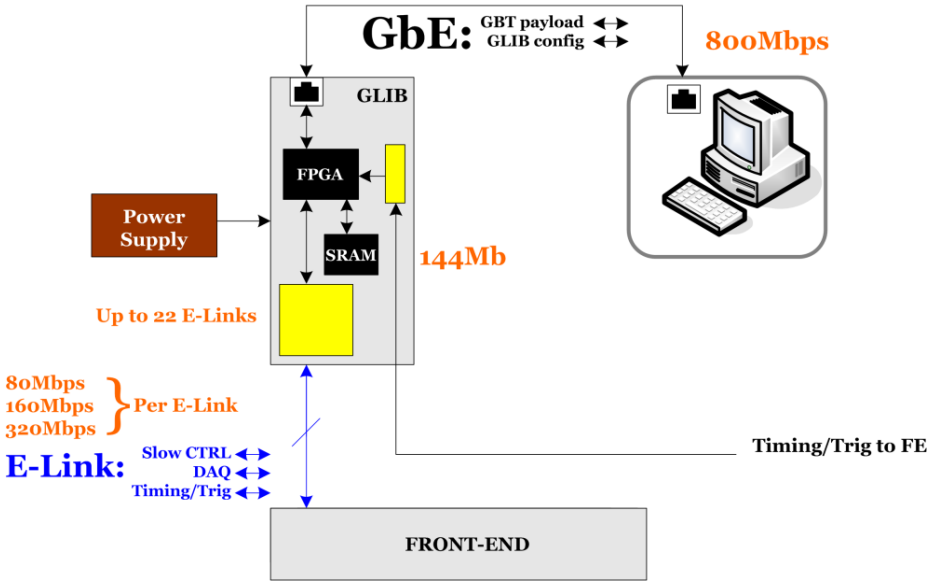

Fig. A - 4 : Example of the GLIB interfacing directly with front-end chips. Mode: bench-top. Payload interface: GbE.

Important note: *The bit rate shown in the figures of examples 1 & 2 concerning GbE refers to the maximum data throughput while concerning PCIe refers to the maximum data throughput (for write transaction) of PCIe GEN2 4x (see §5.2).*

EXAMPLE3: GLIB as Back-End system, µTCA crate mode.

The GLIB is operating inside a µTCA crate. The crate management by the MCH is controlled through a GbE link. For the reception of timing/trigger information, the GLIB is equipped with the TTC mezzanine. The GLIB communicates with the front-end via GBT links. In Fig. A - 5, the configuration of the GLIB as well as the transfer of the GBT payload from/to the PC is done by a GbE connection, through the MCH's GbE switch. The SRAM can be used for intermediate storage, if necessary. Fig. A - 6 shows a different flavour where configuration of the GLIB as well as the transfer of the GBT payload from/to an AMC CPU is done through the MCH's PCIe switch. The AMC CPU stores the data to an AMC storage medium through a SATA link.

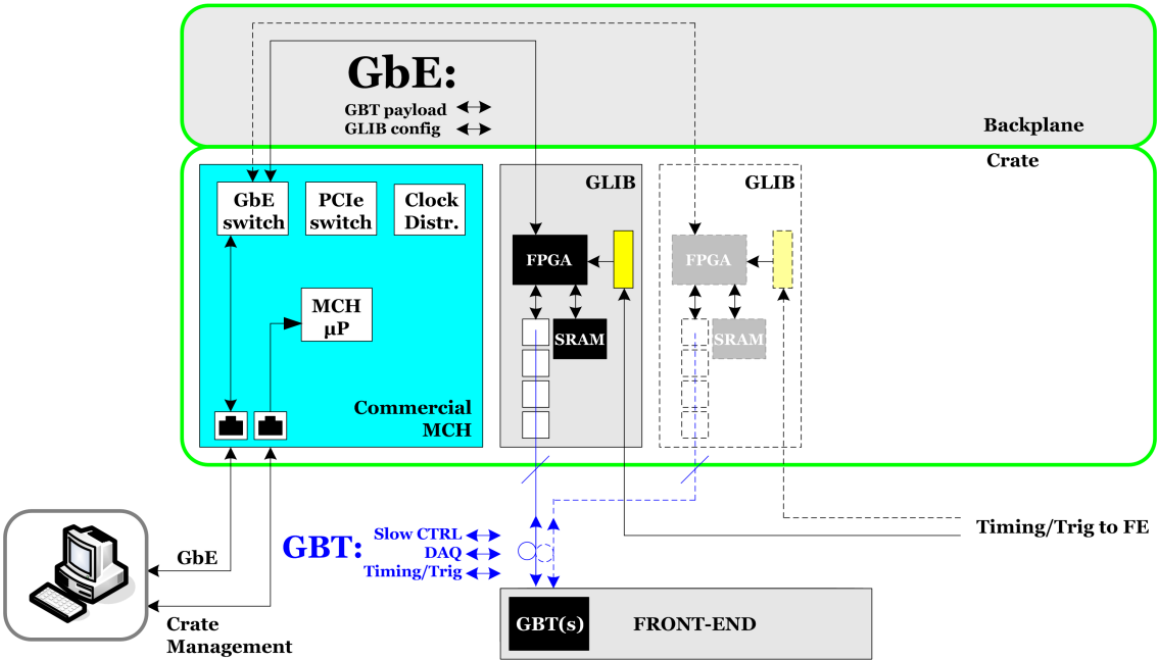

Fig. A - 5 : Example of the GLIB as back-end system. Mode: crate. Payload interface: GbE.

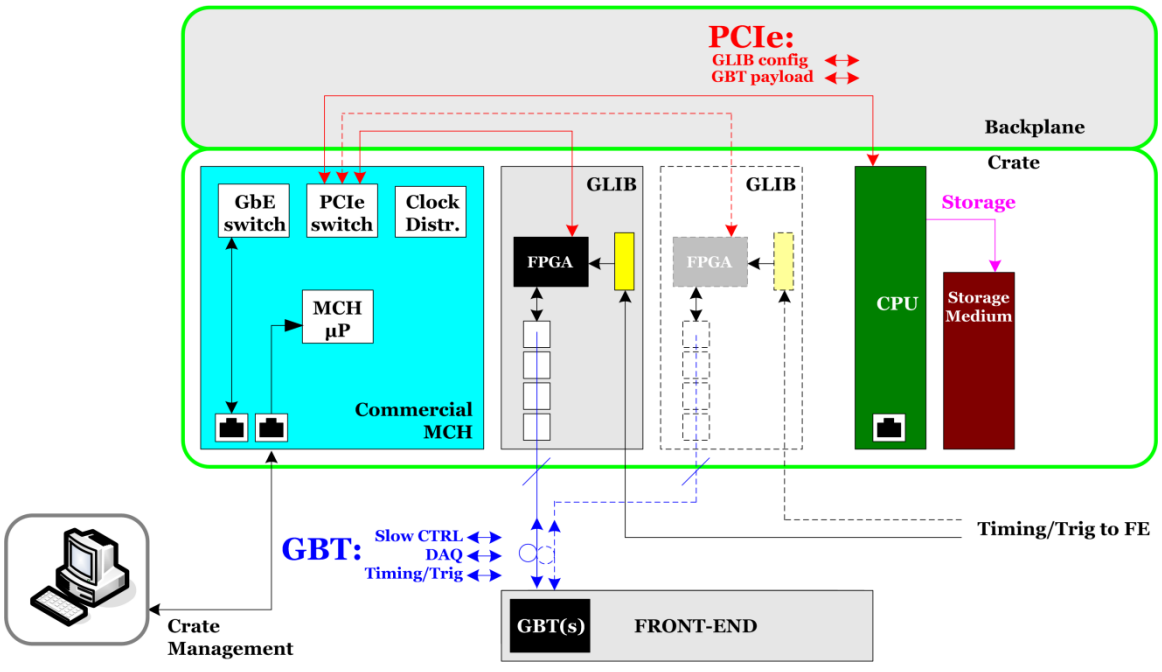

Fig. A - 6 : Example of the GLIB as back-end system. Mode: crate. Payload interface: PCIe.

APPENDIX B: COMPONENTS LIST

Component	Description	Manufacturer
XC6VLX130T-1FF1156C	Virtex-6 LXT series FPGA	XILINX
XCF128X-FTG64C	Platform Flash XL for Virtex-6	XILINX
XC2C128	Coolrunner II CPLD	XILINX
SEAF-40-S-06.5-10-A	FMC HPC connector, Female, 400-pin	SAMTEC
2007132-1	SFP+ 1X4 Ganged Cage Assembly without light pipe	TYCO
1888247-1	PT connector assembly, 20pos, 0.8mm pitch, for SFP+	TYCO
LTM4601EV#PBF	Adj. Voltage 12A DC/DC µModule	Linear Technology
LTM4606EV#PBF	Adj. Voltage 6A Ultralow EMI DC/DC µModule	Linear Technology
LTC6902	Multiphase Oscillator	Linear Technology
MAX8556	4A Ultra-Low-Input-Voltage LDO Regulators	MAXIM
LT3021	500mA, Low Voltage, Very Low Dropout Linear Regulator	Linear Technology
IDT5V5216PGG	Type-1/Type-2 M-LVDS to LVDS Transceiver	IDT
CDCE62005	Clock Multiplier/Jitter Attenuator	Texas Instruments
ICS874003-05	PCIe jitter attenuator	IDT
SN65LVDT125ADBT	LVDS 4x4 Crosspoint Switch	Texas Instruments
SN65LVDT122PW	LVDS 2x2 Crosspoint Switch	Texas Instruments
ICS874003-05	PCIe clock jitter attenuator	IDT
ICS557G-03	PCIe clock (100MHz or 125MHz)	IDT
CY7C1470	2Mx36 200MHz SRAM (upgradeable up to 32Mx72)	Cypress

Table B - 1 : Preliminary list of the major components

APPENDIX C: FMC/FPGA pin mapping

Table C – 1: FMC1/FPGA pin mapping

FMC1	FPGA		
Line name	**Pin**	**Line name**	**Comments**
CLK0_C2M_N	B32	IO_L0N_16	
CLK0_C2M_P	C32	IO_L0P_16	
CLK0_M2C_N	K12	IO_L18N_GC_35	FPGA global clock input, connected through x-point switch
CLK0_M2C_P	K13	IO_L18P_GC_35	FPGA global clock input, connected through x-point switch
CLK1_C2M_N	D32	IO_L15N_16	
CLK1_C2M_P	D31	IO_L15P_16	
CLK1_M2C_N	E11	IO_L19N_GC_35	FPGA global clock input
CLK1_M2C_P	D11	IO_L19P_GC_35	FPGA global clock input
DP0_C2M_N	D2	MGTTXN0_116	FPGA serializer output channel #0
DP0_C2M_P	D1	MGTTXP0_116	FPGA serializer output channel #0
DP0_M2C_N	G4	MGTRXN0_116	FPGA deserializer input channel #0
DP0_M2C_P	G3	MGTRXP0_116	FPGA deserializer input channel #0
DP1_C2M_N	C3	MGTTXP1_116	FPGA serializer output channel #1
DP1_C2M_P	C4	MGTTXN1_116	FPGA serializer output channel #1
DP1_M2C_N	E4	MGTRXN1_116	FPGA deserializer input channel #1
DP1_M2C_P	E3	MGTRXP1_116	FPGA deserializer input channel #1
DP2_C2M_N	B1	MGTTXP2_116	FPGA serializer output channel #2
DP2_C2M_P	B2	MGTTXN2_116	FPGA serializer output channel #2
DP2_M2C_N	D6	MGTRXN2_116	FPGA deserializer input channel #2
DP2_M2C_P	D5	MGTRXP2_116	FPGA deserializer input channel #2
DP3_C2M_N	A3	MGTTXP3_116	FPGA serializer output channel #3
DP3_C2M_P	A4	MGTTXN3_116	FPGA serializer output channel #3
DP3_M2C_N	B5	MGTRXP3_116	FPGA deserializer input channel #3
DP3_M2C_P	B6	MGTRXN3_116	FPGA deserializer input channel #3
HA00_N_CC	V27	IO_L11N_SRCC_14	HA00_N_CC
HA00_P_CC	V28	IO_L11P_SRCC_14	HA00_P_CC
HA01_N_CC	L30	IO_L11N_SRCC_15	HA01_N_CC
HA01_P_CC	L29	IO_L11P_SRCC_15	HA01_P_CC
HA02_N	B33	IO_L4N_VREF_16	HA02_N
HA02_P	A33	IO_L4P_16	HA02_P
HA03_N	W26	IO_L19N_14	HA03_N
HA03_P	W27	IO_L19P_14	HA03_P
HA04_N	T26	IO_L15N_SM15N_15	HA04_N
HA04_P	R26	IO_L15P_SM15P_15	HA04_P
HA05_N	U27	IO_L5N_14	HA05_N
HA05_P	U26	IO_L5P_14	HA05_P
HA06_N	C34	IO_L8N_SRCC_16	HA06_N
HA06_P	D34	IO_L8P_SRCC_16	HA06_P
HA07_N	B34	IO_L6N_16	HA07_N
HA07_P	C33	IO_L6P_16	HA07_P
HA08_N	H30	IO_L5N_16	HA08_N
HA08_P	G31	IO_L5P_16	HA08_P
HA09_N	M28	IO_L7N_SM12N_15	HA09_N

Table C - 1 : FMC1/FPGA pin mapping

HA09_P	L28	IO_L7P_SM12P_15
HA10_N	F34	IO_L12N_VRP_16
HA10_P	E34	IO_L12P_VRN_16
HA11_N	E33	IO_L2N_16
HA11_P	E32	IO_L2P_16
HA12_N	H32	IO_L17N_16
HA12_P	G32	IO_L17P_16
HA13_N	L26	IO_L18N_16
HA13_P	L25	IO_L18P_16
HA14_N	T25	IO_L0N_14
HA14_P	U25	IO_L0P_14
HA15_N	P26	IO_L12N_SM13N_15
HA15_P	P25	IO_L12P_SM13P_15
HA16_N	M27	IO_L3N_SM9N_15
HA16_P	M26	IO_L3P_SM9P_15
HA17_N_CC	G33	IO_L10N_MRCC_16
HA17_P_CC	F33	IO_L10P_MRCC_16
HA18_N	J32	IO_L19N_16
HA18_P	J31	IO_L19P_16
HA19_N	N30	IO_L17N_15
HA19_P	M30	IO_L17P_15
HA20_N	K31	IO_L2N_SM8N_15
HA20_P	K32	IO_L2P_SM8P_15
HA21_N	J34	IO_L16N_16
HA21_P	K33	IO_L16P_16
HA22_N	L34	IO_L16N_VRP_15
HA22_P	K34	IO_L16P_VRN_15
HA23_N	M32	IO_L6N_SM11N_15
HA23_P	L33	IO_L6P_SM11P_15
HB00_N_CC	AG28	IO_L9N_MRCC_12
HB00_P_CC	AG27	IO_L9P_MRCC_12
HB01_N	AE26	IO_L11N_SRCC_12
HB01_P	AF26	IO_L11P_SRCC_12
HB02_N	AE29	IO_L3N_12
HB02_P	AE28	IO_L3P_12
HB03_N	AD26	IO_L0N_12
HB03_P	AD25	IO_L0P_12
HB04_N	AK34	IO_L6N_12
HB04_P	AL34	IO_L6P_12
HB05_N	AF29	IO_L5N_12
HB05_P	AF28	IO_L5P_12
HB06_N_CC	AN34	IO_L8N_SRCC_12
HB06_P_CC	AN33	IO_L8P_SRCC_12
HB07_N	AL33	IO_L16N_12
HB07_P	AM33	IO_L16P_12
HB08_N	AH30	IO_L7N_12
HB08_P	AH29	IO_L7P_12
HB09_N	AM32	IO_L17N_12
HB09_P	AN32	IO_L17P_12
HB10_N	AK31	IO_L15N_12
HB10_P	AL31	IO_L15P_12
HB11_N	AM31	IO_L19N_12
HB11_P	AL30	IO_L19P_12

Table C - 1 (Continued - 1): FMC1/FPGA pin mapping

HB12_N	AJ32	IO_L12N_VRP_12
HB12_P	AJ31	IO_L12P_VRN_12
HB13_N	AD27	IO_L1N_12
HB13_P	AE27	IO_L1P_12
HB14_N	AH34	IO_L4N_VREF_12
HB14_P	AJ34	IO_L4P_12
HB15_N	AH32	IO_L2N_12
HB15_P	AH33	IO_L2P_12
HB16_N	AJ30	IO_L13N_12
HB16_P	AJ29	IO_L13P_12
HB17_N_CC	AG30	IO_L10N_MRCC_12
HB17_P_CC	AF30	IO_L10P_MRCC_12
HB18_N	AK32	IO_L14N_VREF_12
HB18_P	AK33	IO_L14P_12
HB19_N	AP33	IO_L18N_12
HB19_P	AP32	IO_L18P_12
HB20_N	AA33	IO_L0N_13
HB20_P	AA34	IO_L0P_13
HB21_N	Y34	IO_L14N_VREF_14
HB21_P	Y33	IO_L14P_14
LA00_N_CC	W30	IO_L9N_MRCC_14
LA00_P_CC	V30	IO_L9P_MRCC_14
LA01_N_CC	N29	IO_L9N_MRCC_15
LA01_P_CC	N28	IO_L9P_MRCC_15
LA02_N	G30	IO_L3N_16
LA02_P	F30	IO_L3P_16
LA03_N	E31	IO_L11N_SRCC_16
LA03_P	F31	IO_L11P_SRCC_16
LA04_N	R27	IO_L13N_SM14N_15
LA04_P	R28	IO_L13P_SM14P_15
LA05_N	P27	IO_L5N_SM10N_15
LA05_P	N27	IO_L5P_SM10P_15
LA06_N	M25	IO_L1N_15
LA06_P	N25	IO_L1P_15
LA07_N	Y31	IO_L13N_14
LA07_P	Y32	IO_L13P_14
LA08_N	T29	IO_L1N_14
LA08_P	T28	IO_L1P_14
LA09_N	J29	IO_L7N_16
LA09_P	K28	IO_L7P_16
LA10_N	K27	IO_L9N_MRCC_16
LA10_P	K26	IO_L9P_MRCC_16
LA11_N	H33	IO_L14N_VREF_16
LA11_P	H34	IO_L14P_16
LA12_N	K29	IO_L13N_16
LA12_P	J30	IO_L13P_16
LA13_N	J27	IO_L1N_16
LA13_P	J26	IO_L1P_16
LA14_N	G25	IO_L11N_SRCC_25
LA14_P	F25	IO_L11P_SRCC_25
LA15_N	L31	IO_L0N_15
LA15_P	M31	IO_L0P_15
LA16_N	V25	IO_L18N_14

Table C - 1 (Continued - 2): FMC1/FPGA pin mapping

LA16_P	W25	IO_L18P_14
LA17_N_CC	W34	IO_L10N_MRCC_14
LA17_P_CC	V34	IO_L10P_MRCC_14
LA18_N_CC	M33	IO_L10N_MRCC_15
LA18_P_CC	N33	IO_L10P_MRCC_15
LA19_N	P32	IO_L8N_SRCC_15
LA19_P	N32	IO_L8P_SRCC_15
LA20_N	P30	IO_L4N_VREF_15
LA20_P	P31	IO_L4P_15
LA21_N	R34	IO_L2N_14
LA21_P	R33	IO_L2P_14
LA22_N	P34	IO_L18N_15
LA22_P	N34	IO_L18P_15
LA23_N	E24	IO_L8N_SRCC_25
LA23_P	D24	IO_L8P_SRCC_25
LA24_N	U32	IO_L6N_14
LA24_P	U33	IO_L6P_14
LA25_N	T34	IO_L4N_VREF_14
LA25_P	T33	IO_L4P_14
LA26_N	Y27	IO_L17N_14
LA26_P	Y28	IO_L17P_14
LA27_N	R29	IO_L19N_15
LA27_P	P29	IO_L19P_15
LA28_N	R32	IO_L14N_VREF_15
LA28_P	R31	IO_L14P_15
LA29_N	W32	IO_L16N_14
LA29_P	W31	IO_L16P_14
LA30_N	U30	IO_L8N_SRCC_14
LA30_P	U31	IO_L8P_SRCC_14
LA31_N	T31	IO_L3N_14
LA31_P	T30	IO_L3P_14
LA32_N	Y29	IO_L15N_14
LA32_P	W29	IO_L15P_14
LA33_N	V29	IO_L7N_14
LA33_P	U28	IO_L7P_14

Table C - 1 (Continued - 3): FMC1/FPGA pin mapping

Table C – 2: FMC2/FPGA pin mapping

FMC2	FPGA		
Line name	**Pin**	**Line name**	**Comments**
CLK0_C2M_N	A29	IO_L13N_25	
CLK0_C2M_P	A28	IO_L13P_25	
CLK0_M2C_N	K12	IO_L18N_GC_35	FPGA global clock input, connected through x-point switch
CLK0_M2C_P	K13	IO_L18P_GC_35	FPGA global clock input, connected through x-point switch
CLK1_C2M_N	D30	IO_L17N_25	
CLK1_C2M_P	C30	IO_L17P_25	
CLK1_M2C_N	A31	IO_L19N_GC_25	FPGA global clock input
CLK1_M2C_P	B31	IO_L19P_GC_25	FPGA global clock input
HA00_N_CC	B28	IO_L9N_MRCC_25	
HA00_P_CC	C28	IO_L9P_MRCC_25	
HA01_N_CC	D29	IO_L10N_MRCC_25	
HA01_P_CC	C29	IO_L10P_MRCC_25	
HA02_N	J21	IO_L4N_VREF_26	
HA02_P	J20	IO_L4P_26	
HA03_N	B30	IO_L15N_25	
HA03_P	A30	IO_L15P_25	
HA04_N	F29	IO_L16N_VRP_25	
HA04_P	E29	IO_L16P_VRN_25	
HA05_N	C27	IO_L7N_25	
HA05_P	B27	IO_L7P_25	
HA06_N	AL10	IO_L5N_33	
HA06_P	AM10	IO_L5P_33	
HA07_N	J22	IO_L14N_VREF_26	
HA07_P	H22	IO_L14P_26	
HA08_N	K22	IO_L16N_26	
HA08_P	K21	IO_L16P_26	
HA09_N	A26	IO_L5N_25	
HA09_P	B26	IO_L5P_25	
HA10_N	AE11	IO_L4N_VREF_33	
HA10_P	AF11	IO_L4P_33	
HA11_N	AG10	IO_L6N_33	
HA11_P	AG11	IO_L6P_33	
HA12_N	E12	IO_L17N_35	
HA12_P	D12	IO_L17P_35	
HA13_N	E27	IO_L4N_VREF_25	
HA13_P	D27	IO_L4P_25	
HA14_N	AE12	IO_L0N_33	
HA14_P	AE13	IO_L0P_33	
HA15_N	C23	IO_L3N_26	
HA15_P	B23	IO_L3P_26	
HA16_N	D26	IO_L0N_25	
HA16_P	D25	IO_L0P_25	
HA17_N_CC	M11	IO_L10N_MRCC_35	

Table C - 2 : FMC2/FPGA pin mapping

HA17_P_CC	M12	IO_L10P_MRCC_35
HA18_N	B11	IO_L13N_SM6N_35
HA18_P	A11	IO_L13P_SM6P_35
HA19_N	A21	IO_L7N_26
HA19_P	A20	IO_L7P_26
HA20_N	AJ12	IO_L3N_33
HA20_P	AK12	IO_L3P_33
HA21_N	E14	IO_L5N_SM2N_35
HA21_P	F14	IO_L5P_SM2P_35
HA22_N	A14	IO_L3N_SM1N_35
HA22_P	A13	IO_L3P_SM1P_35
HA23_N	C14	IO_L1N_35
HA23_P	D14	IO_L1P_35
HB00_N_CC	L16	IO_L9N_MRCC_36
HB00_P_CC	K16	IO_L9P_MRCC_36
HB01_N	C15	IO_L19N_36
HB01_P	D15	IO_L19P_36
HB02_N	G16	IO_L12N_VRP_36
HB02_P	F16	IO_L12P_VRN_36
HB03_N	M17	IO_L7N_36
HB03_P	M18	IO_L7P_36
HB04_N	H18	IO_L8N_SRCC_36
HB04_P	G18	IO_L8P_SRCC_36
HB05_N	J19	IO_L6N_36
HB05_P	K19	IO_L6P_36
HB06_N_CC	L14	IO_L10N_MRCC_36
HB06_P_CC	L15	IO_L10P_MRCC_36
HB07_N	G17	IO_L3N_36
HB07_P	H17	IO_L3P_36
HB08_N	E17	IO_L0N_36
HB08_P	F18	IO_L0P_36
HB09_N	K17	IO_L2N_36
HB09_P	K18	IO_L2P_36
HB10_N	L18	IO_L4N_VREF_36
HB10_P	L19	IO_L4P_36
HB11_N	J15	IO_L18N_36
HB11_P	H15	IO_L18P_36
HB12_N	F15	IO_L16N_36
HB12_P	G15	IO_L16P_36
HB13_N	J16	IO_L14N_VREF_36
HB13_P	J17	IO_L14P_36
HB14_N	D16	IO_L13N_36
HB14_P	E16	IO_L13P_36
HB15_N	D17	IO_L1N_36
HB15_P	E18	IO_L1P_36
HB16_N	B17	IO_L5N_36
HB16_P	C17	IO_L5P_36
HB17_N_CC	B16	IO_L11N_SRCC_36
HB17_P_CC	A16	IO_L11P_SRCC_36
HB18_N	B15	IO_L15N_36

Table C - 2 (Continued - 1): FMC2/FPGA pin mapping

HB18_P	A15	IO_L15P_36
HB19_N	M15	IO_L17N_36
HB19_P	M16	IO_L17P_36
HB20_N	C18	IO_L17N_26
HB20_P	B18	IO_L17P_26
HB21_N	F13	IO_L15N_SM7N_35
HB21_P	E13	IO_L15P_SM7P_35
LA00_N_CC	G20	IO_L10N_MRCC_26
LA00_P_CC	F21	IO_L10P_MRCC_26
LA01_N_CC	H20	IO_L11N_SRCC_26
LA01_P_CC	H19	IO_L11P_SRCC_26
LA02_N	G22	IO_L2N_26
LA02_P	G21	IO_L2P_26
LA03_N	E28	IO_L14N_VREF_25
LA03_P	F28	IO_L14P_25
LA04_N	L21	IO_L18N_26
LA04_P	L20	IO_L18P_26
LA05_N	C25	IO_L1N_25
LA05_P	C24	IO_L1P_25
LA06_N	A25	IO_L3N_25
LA06_P	B25	IO_L3P_25
LA07_N	G27	IO_L6N_25
LA07_P	G26	IO_L6P_25
LA08_N	F11	IO_L2N_SM0N_35
LA08_P	G11	IO_L2P_SM0P_35
LA09_N	F26	IO_L2N_25
LA09_P	E26	IO_L2P_25
LA10_N	A24	IO_L1N_26
LA10_P	A23	IO_L1P_26
LA11_N	G28	IO_L12N_25
LA11_P	H27	IO_L12P_25
LA12_N	C12	IO_L11N_SRCC_35
LA12_P	C13	IO_L11P_SRCC_35
LA13_N	E23	IO_L6N_26
LA13_P	E22	IO_L6P_26
LA14_N	B22	IO_L5N_26
LA14_P	B21	IO_L5P_26
LA15_N	B13	IO_L7N_SM4N_35
LA15_P	B12	IO_L7P_SM4P_35
LA16_N	AK11	IO_L1N_33
LA16_P	AJ11	IO_L1P_33
LA17_N_CC	M13	IO_L9N_MRCC_35
LA17_P_CC	L13	IO_L9P_MRCC_35
LA18_N_CC	C19	IO_L9N_MRCC_26
LA18_P_CC	B20	IO_L9P_MRCC_26
LA19_N	AC14	IO_L2N_33
LA19_P	AD14	IO_L2P_33
LA20_N	D22	IO_L19N_26
LA20_P	C22	IO_L19P_26
LA21_N	AM11	IO_L7N_33

Table C - 2 (Continued - 2): FMC2/FPGA pin mapping

LA21_P	AL11	IO_L7P_33
LA22_N	F20	IO_L8N_SRCC_26
LA22_P	F19	IO_L8P_SRCC_26
LA23_N	E21	IO_L12N_VRP_26
LA23_P	D21	IO_L12P_VRN_26
LA24_N	H14	IO_L0N_35
LA24_P	G13	IO_L0P_35
LA25_N	D19	IO_L13N_26
LA25_P	E19	IO_L13P_26
LA26_N	D20	IO_L0N_26
LA26_P	C20	IO_L0P_26
LA27_N	A19	IO_L15N_26
LA27_P	A18	IO_L15P_26
LA28_N	G10	IO_L6N_SM3N_35
LA28_P	H10	IO_L6P_SM3P_35
LA29_N	J14	IO_L8N_SRCC_35
LA29_P	K14	IO_L8P_SRCC_35
LA30_N	J10	IO_L14N_VREF_35
LA30_P	J11	IO_L14P_35
LA31_N	H13	IO_L4N_VREF_35
LA31_P	G12	IO_L4P_35
LA32_N	L11	IO_L16N_VRP_35
LA32_P	K11	IO_L16P_VRN_35
LA33_N	J12	IO_L12N_SM5N_35
LA33_P	H12	IO_L12P_SM5P_35

Table C - 2 (Continued - 3): FMC2/FPGA pin mapping