PROIECT CIRCUITE INTEGRATE DIGITALE

Realizat de Alistar Vladut Mihai

Grupa: 2125

An universitar: II(2022-2023)

Cerințe pentru proiectul de laborator

CID 2022-2023

Se pot obține maximum 5 puncte.

1.Rezolvarea corectă a temei de proiect pe hârtie(0.5p)

2.Circuitul combinațional (0.5p)

a) Verificarea funcționalității circuitului

3.Circuitul secvențial (0.5p)

a) Verificarea funcționalității circuitului

4. Implementarea finală(Arhitectura se va descrie structural)(3p)

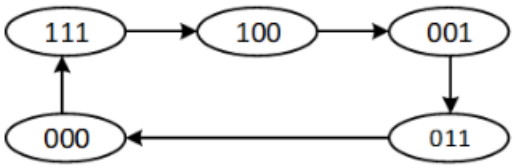
a) Verificarea funcționalității automatului

5.Aspect documentație (foi de capăt, pagini numerotate etc.)(0.5p)

Alocare proiect:

- Automat 1
- Bistabil A
- Multiplexor 1

1.

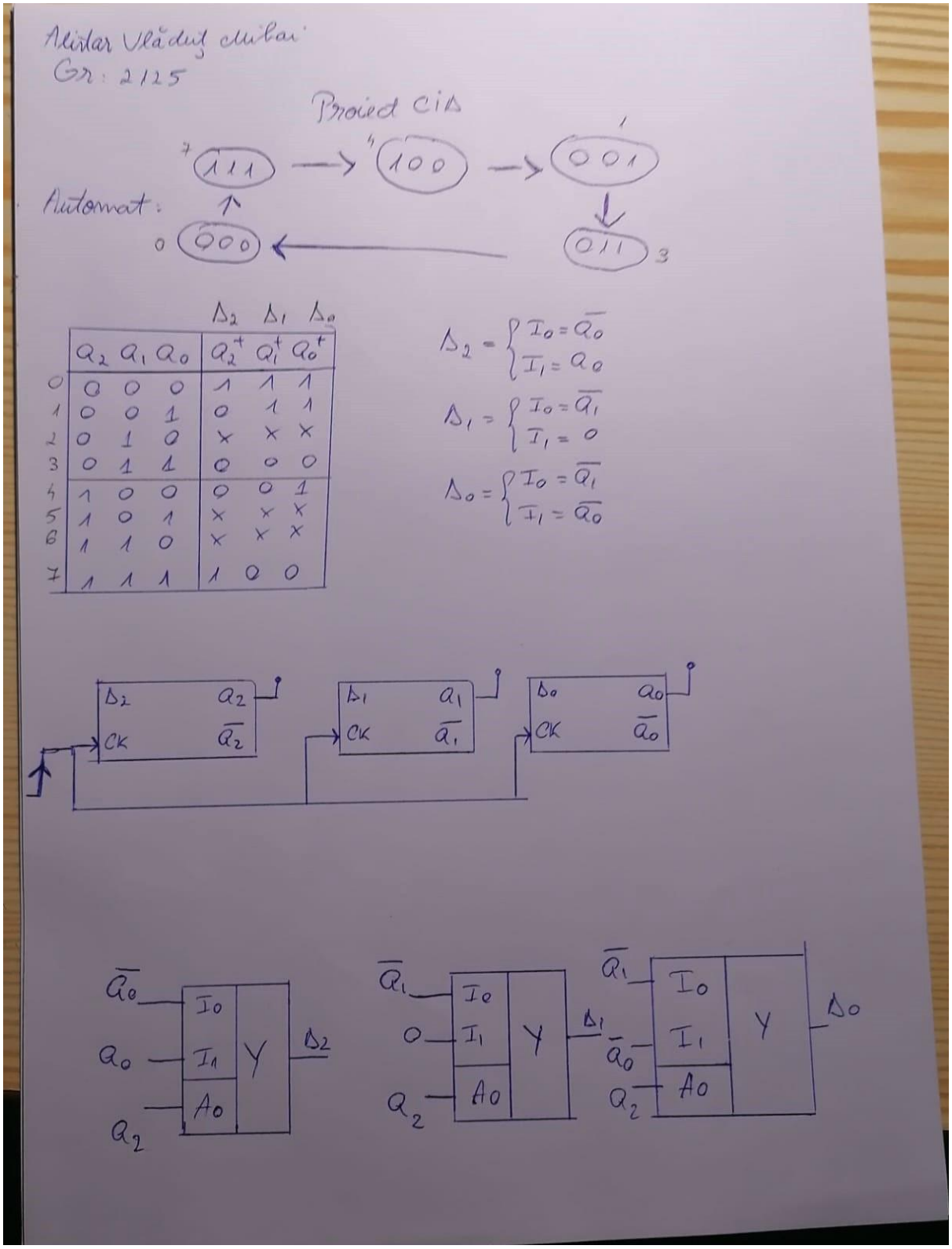


A.

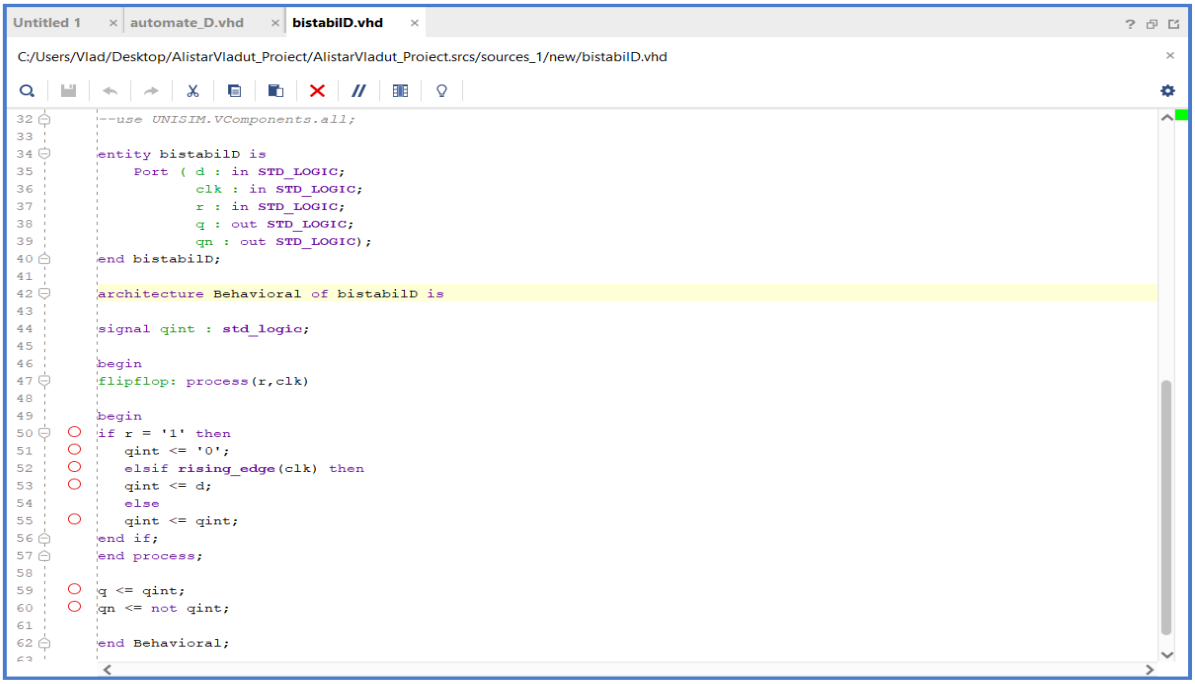
r	clk	Action
1	x	Reset
0	↑	$Q^+ = D$
otherwise		Wait

I. Doar MUX 2:1

REZOLVAREA CIRCUITULUI PE HARTIE (SECVENTIAL SI COMBINATIONAL)

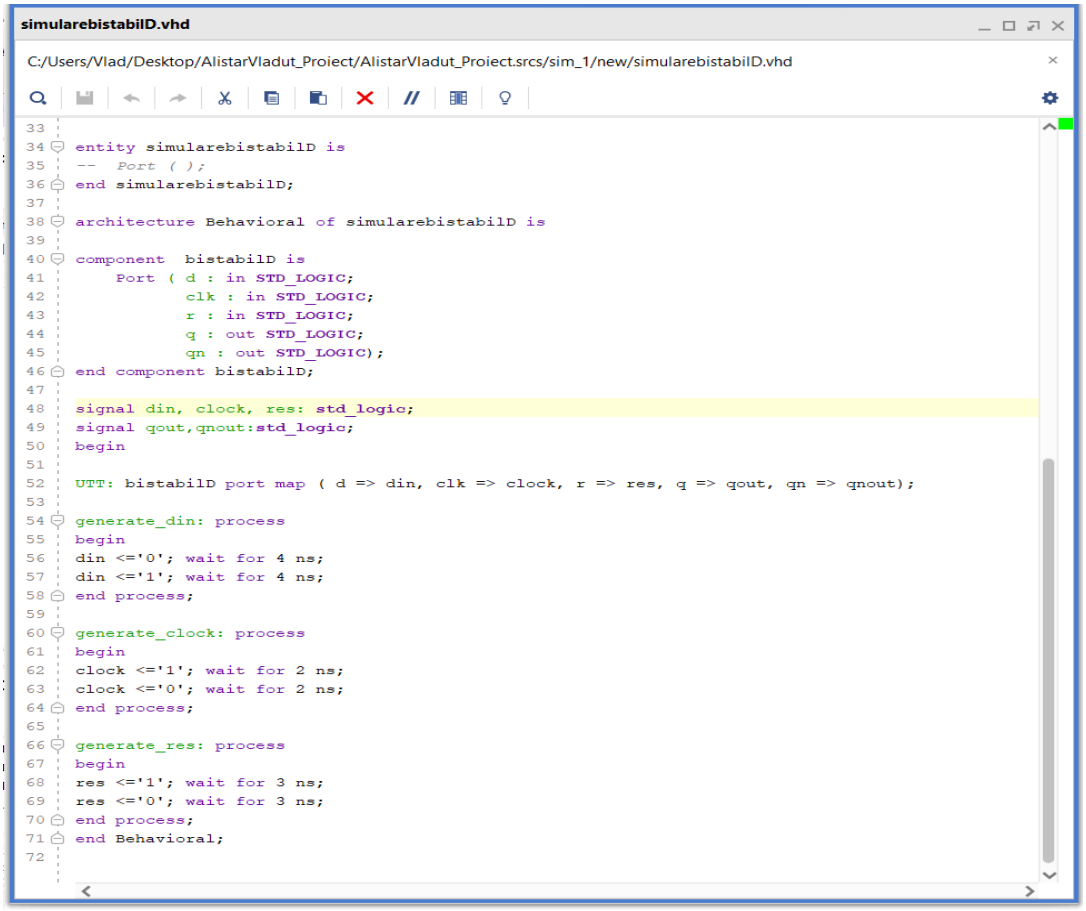


CREAREA UNEI SURSE DE TIP DESIGN PENTRU BISTABILUL D



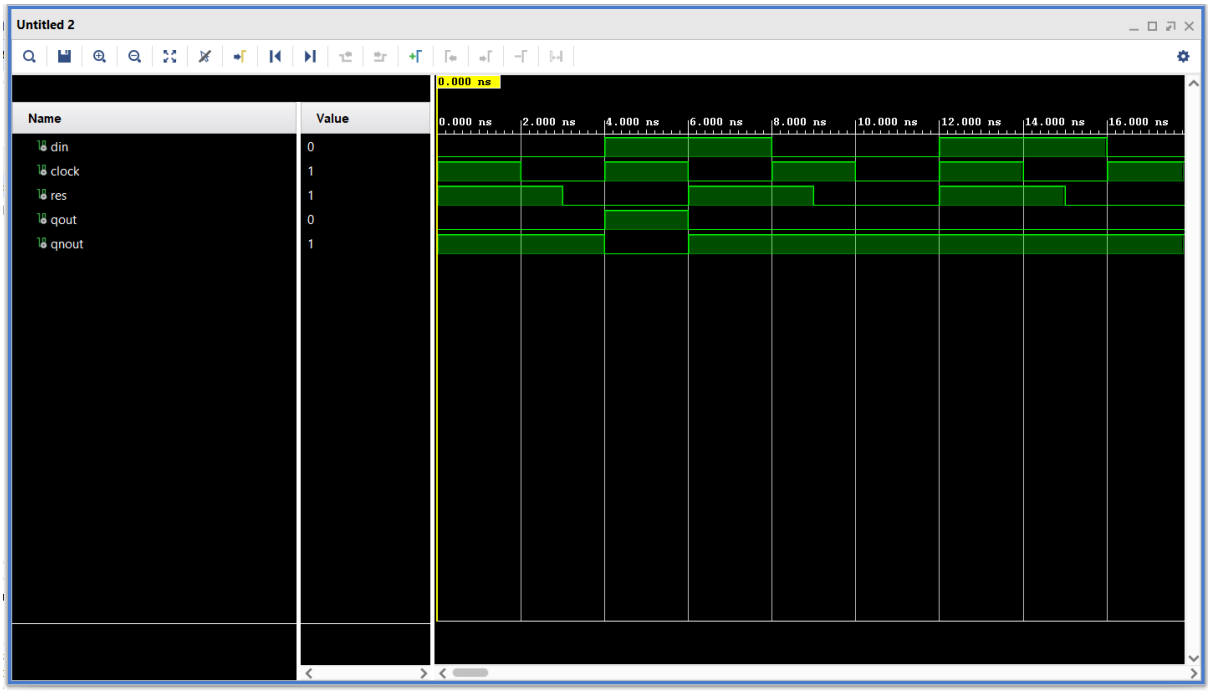

```
--use UNISIM.VComponents.all;

entity bistabilD is
    Port ( d : in STD_LOGIC;
           clk : in STD_LOGIC;
           r : in STD_LOGIC;
           q : out STD_LOGIC;
           qn : out STD_LOGIC);
end bistabilD;

architecture Behavioral of bistabilD is

signal qint : std_logic;

begin
flipflop: process(r,clk)

begin
if r = '1' then
   qint <= '0';
   elsif rising_edge(clk) then
   qint <= d;
   else
   qint <= qint;
end if;
end process;

q <= qint;
qn <= not qint;

end Behavioral;
```

CREAREA UNEI SURSE DE TIP SIMULATION A BISTABILULUI D

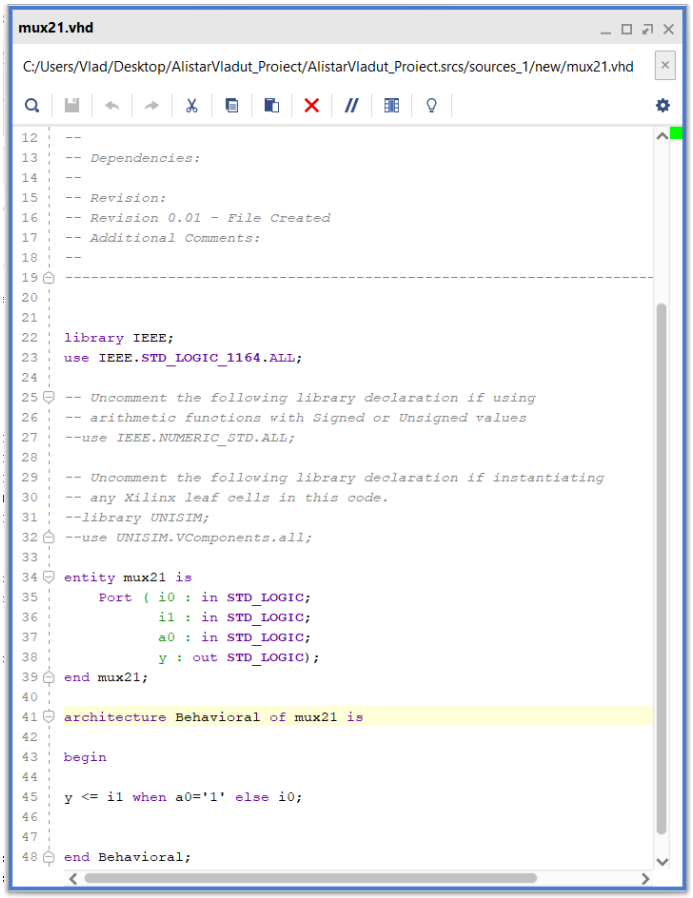



```
entity simularebistabilD is
--  Port ( );
end simularebistabilD;

architecture Behavioral of simularebistabilD is

component  bistabilD is
    Port ( d : in STD_LOGIC;
           clk : in STD_LOGIC;
           r : in STD_LOGIC;
           q : out STD_LOGIC;
           qn : out STD_LOGIC);
end component bistabilD;

signal din, clock, res: std_logic;
signal qout,qnout:std_logic;
begin

UTT: bistabilD port map ( d => din, clk => clock, r => res, q => qout, qn => qnout);

generate_din: process
begin
din <='0'; wait for 4 ns;
din <='1'; wait for 4 ns;
end process;

generate_clock: process
begin
clock <='1'; wait for 2 ns;
clock <='0'; wait for 2 ns;
end process;

generate_res: process
begin
res <='1'; wait for 3 ns;
res <='0'; wait for 3 ns;
end process;
end Behavioral;
```

RULAREA SIMULARII BISTABILULUI D



CREAREA UNEI SURSE DE TIP DESIGN PENTRU MULTIPLEXORUL 2:1



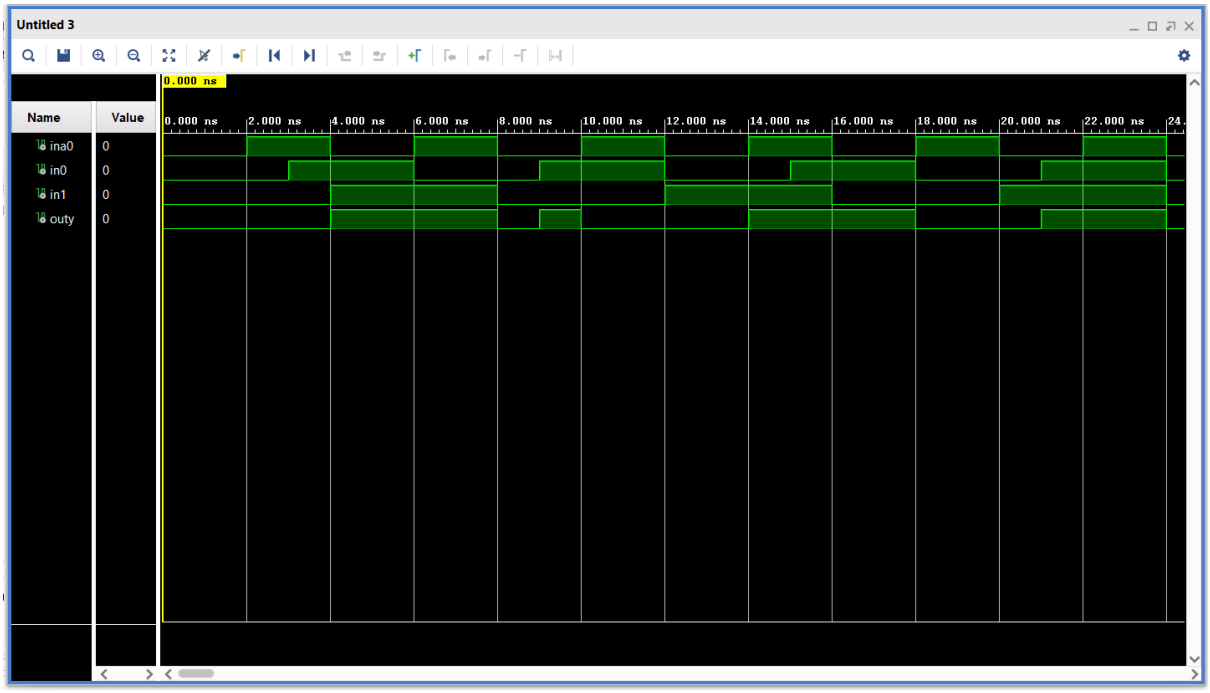
CREAREA UNEI SURSE DE TIP SIMULATION A MULTIPLEXORULUI 2:1

simularemux21.vhd

C:/Users/Vlad/Desktop/AlistarVladut_Proiect/AlistarVladut_Proiect.srcs/sim_1/new/simularemux21.vl

```
34  entity simularemux2_1 is
35  --  Port ( );
36  end simularemux2_1;
37
38  architecture Behavioral of simularemux2_1 is
39  component mux21 is
40      Port ( i0 : in STD_LOGIC;
41             i1 : in STD_LOGIC;
42             a0 : in STD_LOGIC;
43             y : out STD_LOGIC);
44  end component mux21;
45  signal ina0, in0, in1, outy:  std_logic;
46  begin
47  UTT: mux21 port map(i0=>in0,  i1=>in1, a0=>ina0, y=> outy);
48
49  generate_ina0: process
50  begin
51  ina0 <='0'; wait for 2 ns;
52  ina0 <='1'; wait for 2 ns;
53  end process;
54
55  generate_in0: process
56  begin
57  in0 <='0'; wait for 3 ns;
58  in0 <='1'; wait for 3 ns;
59  end process;
60
61  generate_in1: process
62  begin
63  in1 <='0'; wait for 4 ns;
64  in1 <='1'; wait for 4 ns;
65  end process;
66
67
68  end Behavioral;
69
70
```

RULAREA SIMULARII MULTIPLEXORULUI 2:1



CREAREA UNEI SURSE DE TIP DESIGN PENTRU AUTOMAT

automate_D.vhd

C:/Users/Vlad/Desktop/AlistarVladut_Proiect/AlistarVladut_Proiect.srcs/sources_1/new/automate_D.vhd

```
entity automate_D is
    Port ( CLK : in STD_LOGIC;
           R : in STD_LOGIC;
           Q : out STD_LOGIC_VECTOR(2 downto 0));
end automate_D;

architecture Behavioral of automate_D is

component mux21 is
    Port ( i0 : in STD_LOGIC;
           i1 : in STD_LOGIC;
           a0 : in STD_LOGIC;
           y : out STD_LOGIC);
end component mux21;

component bistabilD is
    Port ( d : in STD_LOGIC;
           clk : in STD_LOGIC;
           r : in STD_LOGIC;
           q : out STD_LOGIC;
           qn : out STD_LOGIC);
end component bistabilD;

signal net2, net1, net0:std_logic;
signal Qint:std_logic_vector(2 downto 0);
signal Q0_neg, Q1_neg, Q2_neg: std_logic;
begin

U1: bistabilD port map(clk=>CLK, r=>R, d=>net0, q=>Qint(0),qn=>Q0_neg);
U2: bistabilD port map(clk=>CLK, r=>R, d=>net1, q=>Qint(1),qn=>Q1_neg);
U3: bistabilD port map(clk=>CLK, r=>R, d=>net2, q=>Qint(2),qn=>Q2_neg);

U4: mux21 port map(i0=>Q0_neg,i1=>Qint(0), a0=>Qint(2), y=>net2);
U5: mux21 port map(i0=>Q1_neg,i1=>'0', a0=>Qint(2), y=>net1);
U6: mux21 port map(i0=>Q1_neg,i1=>Q0_neg, a0=>Qint(2), y=>net0);
Q<=Qint;
end Behavioral;
```

CREAREA UNEI SURSE DE TIP SIMULATION A AUTOMATULUI

automate_D.vhd | sim_auto.vhd

C:/Users/Vlad/Desktop/AlistarVladut_Proiect/AlistarVladut_Proiect.srcs/sim_1/new/sim_auto.vhd

```
-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity sim_auto is
--  Port ( );
end sim_auto;

architecture Behavioral of sim_auto is

component automate_D is
    Port ( CLK : in STD_LOGIC;
           R : in STD_LOGIC;
           Q : out STD_LOGIC_VECTOR(2 downto 0));
end component automate_D;
signal R,CLK:std_logic;
signal Q:std_logic_vector(2 downto 0);

begin

UTT: automate_D port map(R=>R, CLK=>CLK, Q=>Q);
R <= '1' after 0 ns, '0' after 2.2 ns;
process
begin
CLK<= '0'; wait for 5 ns;
CLK<= '1'; wait for 5 ns;
end process;
end Behavioral;
```

RULAREA SIMULARII AUTOMATULUI