

# **PROIECT CIRCUITE INTEGRATE DIGITALE**

**Realizat de Alistar Vladut Mihai**

**Grupa: 2125**

**An universitar: II(2022-2023)**

## Cerințe pentru proiectul de laborator

CID 2022-2023

Se pot obține maximum 5 puncte.

1.Rezolvarea corectă a temei de proiect pe hârtie(0.5p)

2.Circuitul combinațional (0.5p)

a) Verificarea funcționalității circuitului

3.Circuitul secvențial (0.5p)

a) Verificarea funcționalității circuitului

4. Implementarea finală(Aritectura se va descrie structural)(3p)

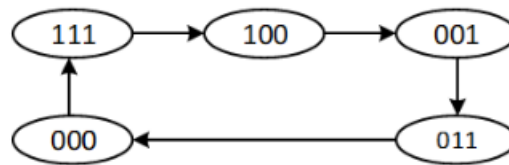
a) Verificarea funcționalității automatului

5.Aspect documentație (foi de capăt, pagini numerotate etc.)(0.5p)


Alocare proiect:

- Automat 1
- Bistabil A
- Multiplexor 1

1.



A.

r	clk	Action
1	x	Reset
0		$Q^+ = D$
otherwise		Wait

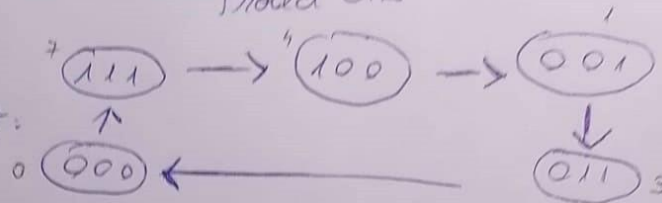
I. Doar MUX 2:1

# REZOLVAREA CIRCUITULUI PE HARTIE (SECVENTIAL SI COMBINATIONAL)

Alința Vlăduț Mihai  
Gr: 2125

Proiect C1A

Automat:

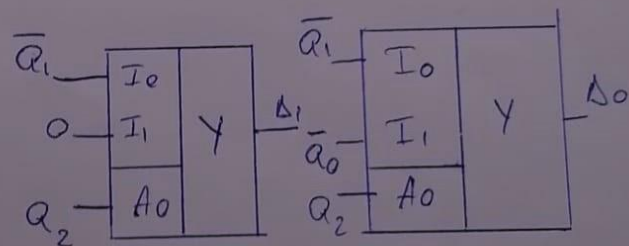
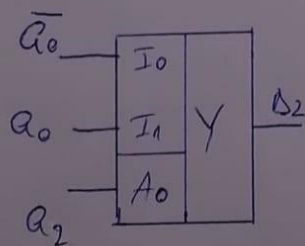
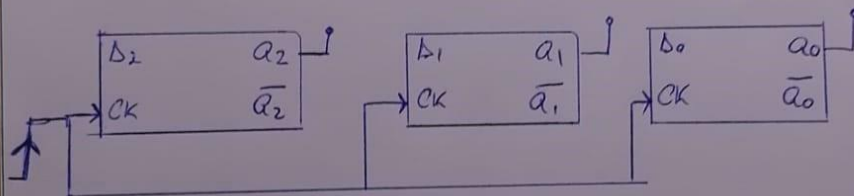


	$\Delta_2$			$\Delta_1$		$\Delta_0$
	$q_2$	$q_1$	$q_0$	$q_2^+$	$q_1^+$	$q_0^+$
0	0	0	0	1	1	1
1	0	0	1	0	1	1
2	0	1	0	x	x	x
3	0	1	1	0	0	0
4	1	0	0	0	0	1
5	1	0	1	x	x	x
6	1	1	0	x	x	x
7	1	1	1	1	0	0

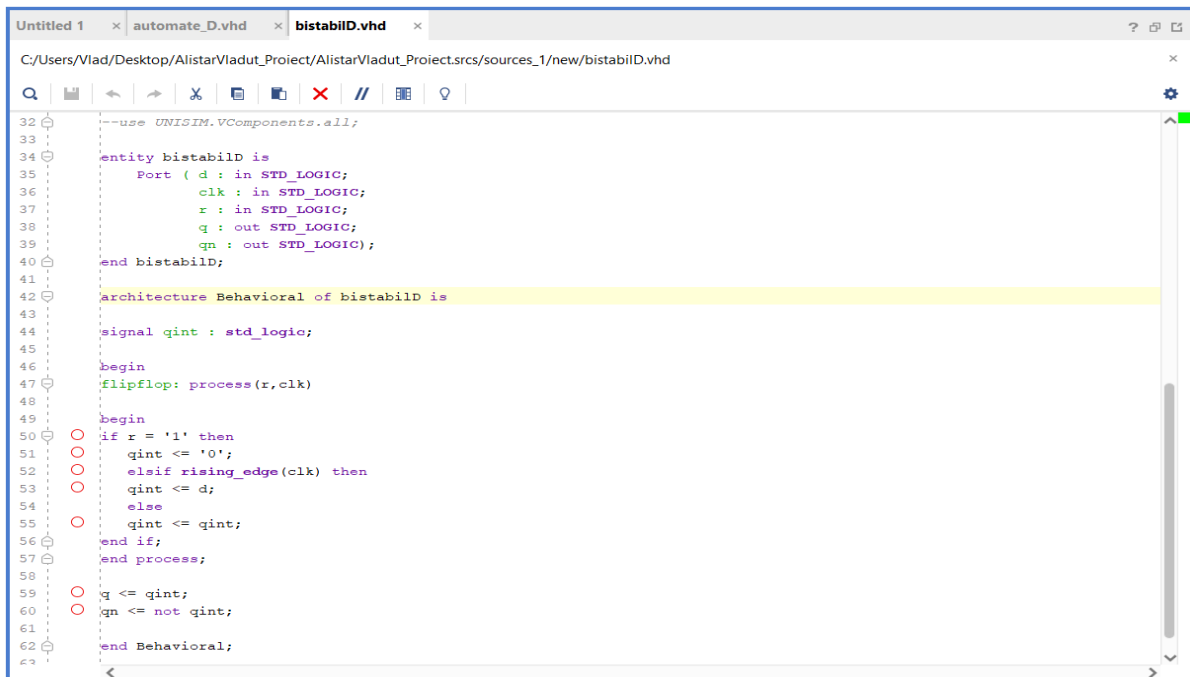
$$\Delta_2 = \begin{cases} I_0 = \bar{Q}_0 \\ I_1 = Q_0 \end{cases}$$

$$\Delta_1 = \begin{cases} I_0 = \bar{Q}_1 \\ I_1 = 0 \end{cases}$$

$$\Delta_0 = \begin{cases} I_0 = \bar{Q}_1 \\ I_1 = \bar{Q}_0 \end{cases}$$



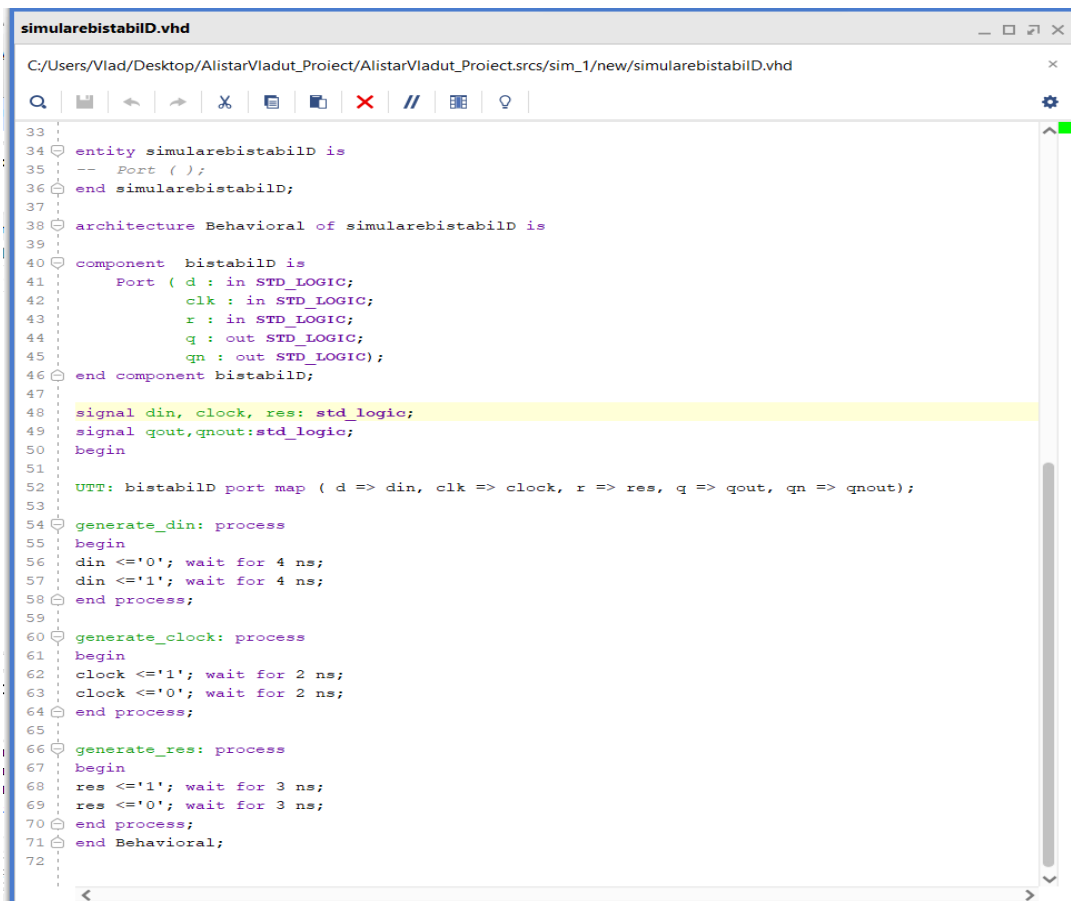
## CREAREA UNEI SURSE DE TIP DESIGN PENTRU BISTABILUL D



The screenshot shows a VHDL editor window titled 'bistabilD.vhd'. The code defines an entity 'bistabilD' with four ports: 'd' (input STD\_LOGIC), 'clk' (input STD\_LOGIC), 'r' (input STD\_LOGIC), 'q' (output STD\_LOGIC), and 'qn' (output STD\_LOGIC). The architecture 'Behavioral of bistabilD' includes a signal 'qint' of type 'std\_logic'. A process 'flipflop' is sensitive to 'r' and 'clk'. Inside the process, an if-else statement handles the reset and clock logic. When 'r' is '1', 'qint' is set to '0'. On the rising edge of 'clk', 'qint' is updated to 'd' if 'r' is not '1'. The outputs 'q' and 'qn' are assigned as 'qint' and 'not qint' respectively.

```
32 --use UNISIM.VComponents.all;
33
34 entity bistabilD is
35     Port ( d : in STD_LOGIC;
36           clk : in STD_LOGIC;
37           r : in STD_LOGIC;
38           q : out STD_LOGIC;
39           qn : out STD_LOGIC);
40 end bistabilD;
41
42 architecture Behavioral of bistabilD is
43
44     signal qint : std_logic;
45
46     begin
47     flipflop: process(r,clk)
48
49     begin
50         if r = '1' then
51             qint <= '0';
52         elsif rising_edge(clk) then
53             qint <= d;
54         else
55             qint <= qint;
56         end if;
57     end process;
58
59     q <= qint;
60     qn <= not qint;
61
62 end Behavioral;
```

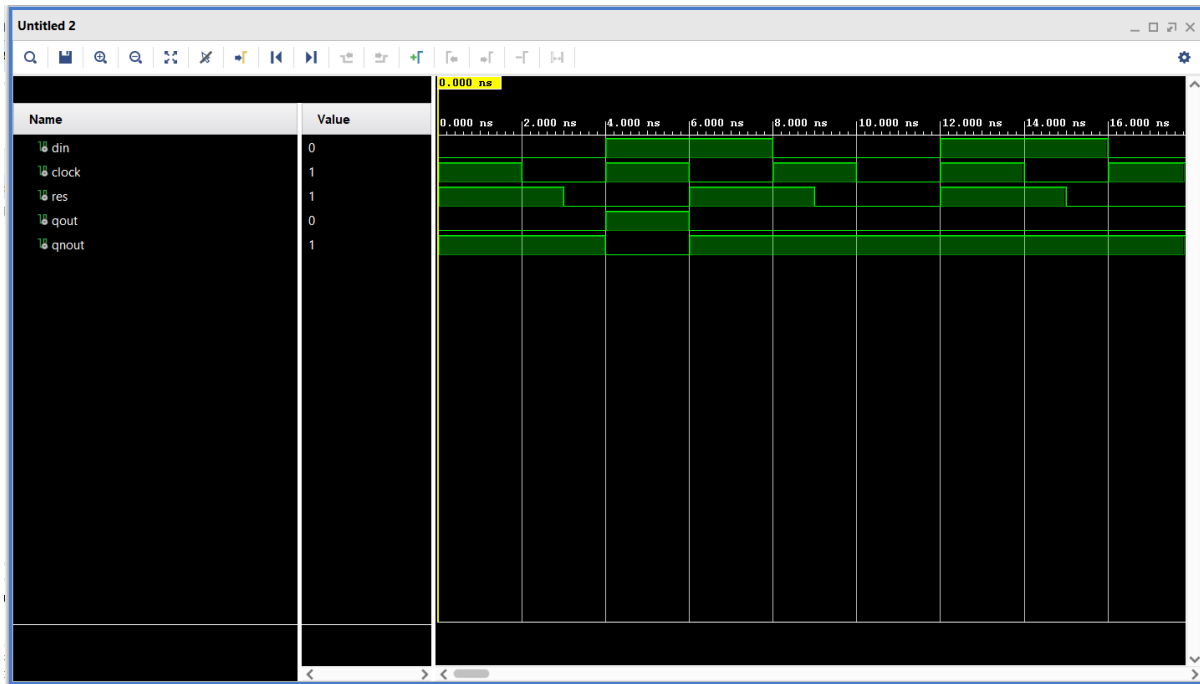
## CREAREA UNEI SURSE DE TIP SIMULATION A BISTABILULUI D



The screenshot shows a VHDL editor window titled 'simularebistabilD.vhd'. The code defines an entity 'simularebistabilD' with no ports. The architecture 'Behavioral of simularebistabilD' includes a component 'bistabilD' and three signals: 'din', 'clock', and 'res' of type 'std\_logic'. A process 'generate\_din' sets 'din' to '0' for 4 ns and then to '1' for 4 ns. A process 'generate\_clock' sets 'clock' to '1' for 2 ns and then to '0' for 2 ns. A process 'generate\_res' sets 'res' to '1' for 3 ns and then to '0' for 3 ns. The component 'bistabilD' is instantiated with 'din', 'clock', 'res', 'q', and 'qn' as inputs and outputs.

```
33
34 entity simularebistabilD is
35     -- Port ( );
36 end simularebistabilD;
37
38 architecture Behavioral of simularebistabilD is
39
40     component bistabilD is
41         Port ( d : in STD_LOGIC;
42               clk : in STD_LOGIC;
43               r : in STD_LOGIC;
44               q : out STD_LOGIC;
45               qn : out STD_LOGIC);
46     end component bistabilD;
47
48     signal din, clock, res: std_logic;
49     signal qout,qnout:std_logic;
50     begin
51
52     UTT: bistabilD port map ( d => din, clk => clock, r => res, q => qout, qn => qnout);
53
54     generate_din: process
55     begin
56         din <= '0'; wait for 4 ns;
57         din <= '1'; wait for 4 ns;
58     end process;
59
60     generate_clock: process
61     begin
62         clock <= '1'; wait for 2 ns;
63         clock <= '0'; wait for 2 ns;
64     end process;
65
66     generate_res: process
67     begin
68         res <= '1'; wait for 3 ns;
69         res <= '0'; wait for 3 ns;
70     end process;
71 end Behavioral;
72
```

## RULAREA SIMULARII BISTABILULUI D



## CREAREA UNEI SURSE DE TIP DESIGN PENTRU MULTIPLEXORUL 2:1

```

mux21.vhd
C:/Users/Vlad/Desktop/AlistarVladut_Proiect/AlistarVladut_Proiect/srcs/sources_1/new/mux21.vhd

12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19 -----
20
21 library IEEE;
22 use IEEE.STD_LOGIC_1164.ALL;
23
24
25 -- Uncomment the following library declaration if using
26 -- arithmetic functions with Signed or Unsigned values
27 --use IEEE.NUMERIC_STD.ALL;
28
29 -- Uncomment the following library declaration if instantiating
30 -- any Xilinx leaf cells in this code.
31 --library UNISIM;
32 --use UNISIM.VComponents.all;
33
34 entity mux21 is
35     Port ( i0 : in STD_LOGIC;
36           i1 : in STD_LOGIC;
37           a0 : in STD_LOGIC;
38           y : out STD_LOGIC);
39 end mux21;
40
41 architecture Behavioral of mux21 is
42
43 begin
44
45     y <= i1 when a0='1' else i0;
46
47
48 end Behavioral;

```

## CREAREA UNEI SURSE DE TIP SIMULATION A MULTIPLEXORULUI 2:1

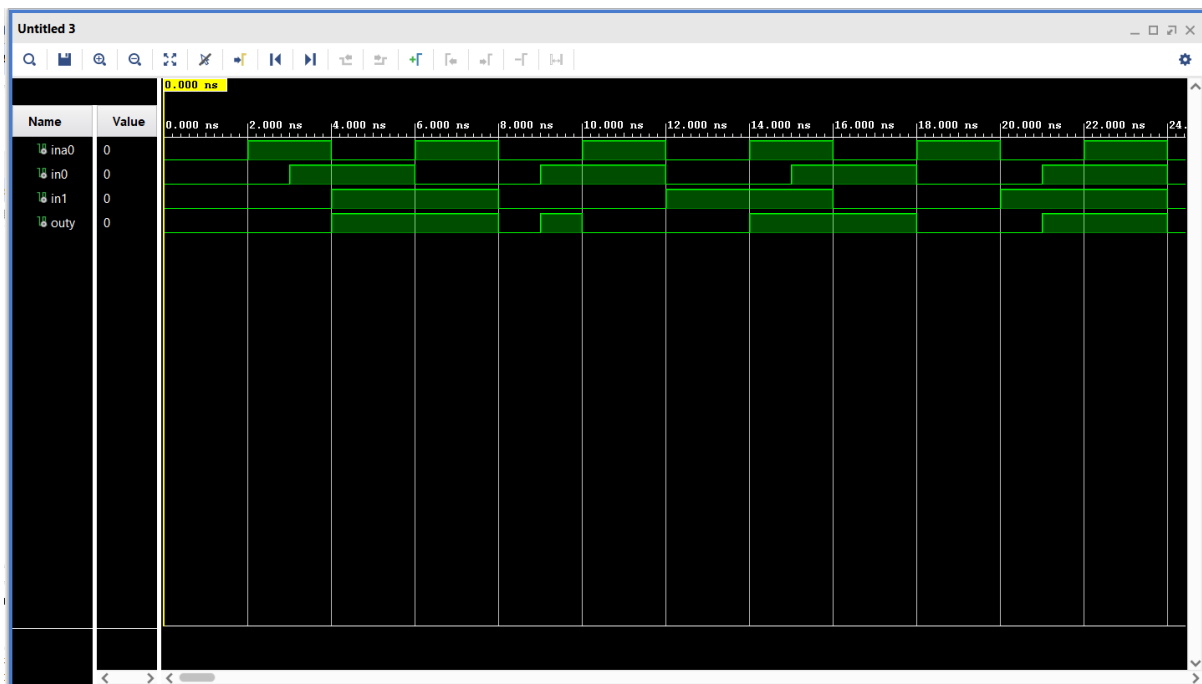
```

simularemux21.vhd
C:/Users/Vlad/Desktop/AlistarVladut_Proiect/AlistarVladut_Proiect.srscs/sim_1/new/simularemux21.vl

34 entity simularemux2_1 is
35     -- Port ( );
36 end simularemux2_1;
37
38 architecture Behavioral of simularemux2_1 is
39     component mux21 is
40         Port ( i0 : in STD_LOGIC;
41               i1 : in STD_LOGIC;
42               a0 : in STD_LOGIC;
43               y : out STD_LOGIC);
44     end component mux21;
45     signal ina0, in0, in1, outy: std_logic;
46 begin
47     UUT: mux21 port map(i0=>in0, i1=>in1, a0=>ina0, y=> outy);
48
49     generate_ina0: process
50     begin
51         ina0 <='0'; wait for 2 ns;
52         ina0 <='1'; wait for 2 ns;
53     end process;
54
55     generate_in0: process
56     begin
57         in0 <='0'; wait for 3 ns;
58         in0 <='1'; wait for 3 ns;
59     end process;
60
61     generate_in1: process
62     begin
63         in1 <='0'; wait for 4 ns;
64         in1 <='1'; wait for 4 ns;
65     end process;
66
67 end Behavioral;
68
69
70

```

## RULAREA SIMULARII MULTIPLEXORULUI 2:1



## CREAREA UNEI SURSE DE TIP DESIGN PENTRU AUTOMAT

```

automate_D.vhd
C:/Users/Vlad/Desktop/AlistarVladut_Proiect/AlistarVladut_Proiect.srcs/sources_1/new/automate_D.vhd

33
34 entity automate_D is
35     Port ( CLK : in STD_LOGIC;
36           R : in STD_LOGIC;
37           Q : out STD_LOGIC_VECTOR(2 downto 0));
38 end automate_D;
39
40 architecture Behavioral of automate_D is
41
42 component mux21 is
43     Port ( i0 : in STD_LOGIC;
44           i1 : in STD_LOGIC;
45           a0 : in STD_LOGIC;
46           y : out STD_LOGIC);
47 end component mux21;
48
49 component bistabilD is
50     Port ( d : in STD_LOGIC;
51           clk : in STD_LOGIC;
52           r : in STD_LOGIC;
53           q : out STD_LOGIC;
54           qn : out STD_LOGIC);
55 end component bistabilD;
56
57 signal net2, net1, net0:std_logic;
58 signal Qint:std_logic_vector(2 downto 0);
59 signal Q0_neg, Q1_neg, Q2_neg: std_logic;
60 begin
61
62 U1: bistabilD port map(clk=>CLK, r=>R, d=>net0, q=>Qint(0),qn=>Q0_neg);
63 U2: bistabilD port map(clk=>CLK, r=>R, d=>net1, q=>Qint(1),qn=>Q1_neg);
64 U3: bistabilD port map(clk=>CLK, r=>R, d=>net2, q=>Qint(2),qn=>Q2_neg);
65
66 U4: mux21 port map(i0=>Q0_neg,i1=>Qint(0), a0=>Qint(2), y=>net2);
67 U5: mux21 port map(i0=>Q1_neg,i1=>'0', a0=>Qint(2), y=>net1);
68 U6: mux21 port map(i0=>Q1_neg,i1=>Q0_neg, a0=>Qint(2), y=>net0);
69 Q<=Qint;
70 end Behavioral;
71

```

## CREAREA UNEI SURSE DE TIP SIMULATION A AUTOMATULUI

```

automate_D.vhd x sim_auto.vhd x
C:/Users/Vlad/Desktop/AlistarVladut_Proiect/AlistarVladut_Proiect.srcs/sim_1/new/sim_auto.vhd

28
29 -- Uncomment the following library declaration if instantiating
30 -- any Xilinx leaf cells in this code.
31 --library UNISIM;
32 --use UNISIM.VComponents.all;
33
34 entity sim_auto is
35     Port ( );
36 end sim_auto;
37
38 architecture Behavioral of sim_auto is
39
40 component automate_D is
41     Port ( CLK : in STD_LOGIC;
42           R : in STD_LOGIC;
43           Q : out STD_LOGIC_VECTOR(2 downto 0));
44 end component automate_D;
45 signal R,CLK:std_logic;
46 signal Q:std_logic_vector(2 downto 0);
47
48 begin
49
50 UUT: automate_D port map(R=>R, CLK=>CLK, Q=>Q);
51 R <= '1' after 0 ns, '0' after 2.2 ns;
52 process
53 begin
54 CLK<= '0'; wait for 5 ns;
55 CLK<= '1'; wait for 5 ns;
56 end process;
57 end Behavioral;
58

```

# RULAREA SIMULARII AUTOMATULUI

