Low-Power Applications Processor

Check for Samples: OMAPL137-HT

1 Low-Power Applications Processor

1.1 Features

- **Highlights**
  - **Dual Core SoC**
    - **300-MHz ARM926EJ-S™ RISC MPU**
    - **300-MHz C674x™ VLIW DSP**
  - **TMS320C674x Fixed/Floating-Point VLIW DSP Core**
  - **Enhanced Direct-Memory-Access Controller 3 (EDMA3)**
  - **128K-Byte RAM Shared Memory**
  - **Two External Memory Interfaces**
  - **Two External Memory Interfaces Modules**
  - **LCD Controller**
  - **Two Serial Peripheral Interfaces (SPI)**
  - **Multimedia Card (MMC)/Secure Digital (SD)**
  - **Two Master/Slave Inter-Integrated Circuit**
  - **One Host-Port Interface (HPI)**
  - **USB 1.1 OHCI (Host) With Integrated PHY (USB1)**
- **Applications**
  - **Industrial Diagnostics**
  - **Test and measurement**
  - **Military Sonar/Radar**
  - **Medical measurement**
  - **Professional Audio**
  - **Down Hole Industry**
- **Software Support**
  - **TI DSP/BIOS™**
  - **Chip Support Library and DSP Library**
- **ARM926EJ-S Core**
  - **32-Bit and 16-Bit (Thumb®) Instructions**
  - **DSP Instruction Extensions**
  - **Single Cycle MAC**
  - **ARM® Jazelle® Technology**
  - **EmbeddedICE-RT™ for Real-Time Debug**
- **ARM9 Memory Architecture**
- **C674x Instruction Set Features**
  - **Superset of the C67x+™ and C64x+™ ISAs**
  - **Up to 3648/2736 C674x MIPS/MFLOPS**
  - **Byte-Addressable (8-/16-/32-/64-Bit Data)**
  - **8-Bit Overflow Protection**
  - **Bit-Field Extract, Set, Clear**
  - **Normalization, Saturation, Bit-Counting**
  - **Compact 16-Bit Instructions**
- **C674x Two Level Cache Memory Architecture**
  - **32K-Byte L1P Program RAM/Cache**
  - **32K-Byte L1D Data RAM/Cache**
  - **256K-Byte L2 Unified Mapped RAM/Cache**
  - **Flexible RAM/Cache Partition (L1 and L2)**
  - **1024KB L2 ROM**
- **Enhanced Direct-Memory-Access Controller 3 (EDMA3):**
  - **2 Transfer Controllers**
  - **32 Independent DMA Channels**
  - **8 Quick DMA Channels**
  - **Programmable Transfer Burst Size**
- **TMS320C674x™ Fixed/Floating-Point VLIW DSP Core**
  - **Load-Store Architecture With Non-Aligned Support**
  - **64 General-Purpose Registers (32 Bit)**
  - **Six ALU (32-/40-Bit) Functional Units**
    - **Supports 32-Bit Integer, SP (IEEE Single Precision/32-Bit) and DP (IEEE Double Precision/64-Bit) Floating Point**
    - **Supports up to Four SP Additions Per Clock, Four DP Additions Every 2 Clocks**
    - **Supports up to Two Floating Point (SP or DP) Approximate Reciprocal or Square Root Operations Per Cycle**
  - **Two Multiply Functional Units**
    - **Mixed-Precision IEEE Floating Point Multiply Supported up to:**
      - **2 SP x SP -> SP Per Clock**
      - **2 SP x SP -> DP Every Two Clocks**
      - **2 SP x DP -> DP Every Three Clocks**
      - **2 DP x DP -> DP Every Four Clocks**
    - **Fixed Point Multiply Supports Two 32 x 32-Bit Multiplies, Four 16 x 16-Bit Multiplies, or Eight 8 x 8-Bit Multiplies per Clock Cycle, and Complex Multiples**
  - **Instruction Packing Reduces Code Size**

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  - All Instructions Conditional
  - Hardware Support for Modulo Loop Operation
  - Protected Mode Operation
  - Exceptions Support for Error Detection and Program Redirection
- 128K-Byte RAM Shared Memory
- 3.3V LVCMOS IOs (except for USB interfaces)
- Two External Memory Interfaces:
  - EMIFA
    - NOR (8-/16-Bit-Wide Data)
    - NAND (8-/16-Bit-Wide Data)
    - 16-Bit SDRAM With 128MB Address Space
  - EMIFB
    - 32-Bit or 16-Bit SDRAM With 256MB Address Space
- Three Configurable 16550 type UART Modules:
  - UART0 With Modem Control Signals
  - Autoflow control signals (CTS, RTS) on UART0 only
  - 16-byte FIFO
  - 16x or 13x Oversampling Option
- LCD Controller
- Two Serial Peripheral Interfaces (SPI) Each With One Chip-Select
- Multimedia Card (MMC)/Secure Digital (SD) Card Interface with Secure Data I/O (SDIO)
- Two Master/Slave Inter-Integrated Circuit (I^2C Bus™)
- One Host-Port Interface (HPI) With 16-Bit-Wide Muxed Address/Data Bus For High Bandwidth
- Programmable Real-Time Unit Subsystem (PRUSS)
  - Two Independent Programmable Realtime Unit (PRU) Cores
    - 32-Bit Load/Store RISC architecture
    - 4K Byte instruction RAM per core
    - 512 Bytes data RAM per core
    - PRU Subsystem (PRUSS) can be disabled via software to save power
  - Standard Power Management Mechanism
    - Clock Gating
    - Entire Subsystem Under a Single PSC Clock Gating Domain
  - Dedicated Interrupt Controller
  - Dedicated Switched Central Resource
- USB 1.1 OHCI (Host) With Integrated PHY (USB1)
- USB 2.0 OTG Port With Integrated PHY (USB0):
  - USB 2.0 High-/Full-Speed Client
  - USB 2.0 High-/Full-/Low-Speed Host
  - End Point 0 (Control)
  - End Points 1,2,3,4 (Control, Bulk, Interrupt or ISOC) Rx and Tx
- Three Multichannel Audio Serial Ports:
  - Six Clock Zones and 28 Serial Data Pins
  - Supports TDM, I2S, and Similar Formats
  - DIT-Capable (McASP2)
  - FIFO buffers for Transmit and Receive
- 10/100 Mb/s Ethernet MAC (EMAC):
  - IEEE 802.3 Compliant (3.3-V I/O Only)
  - RMII Media Independent Interface
  - Management Data I/O (MDIO) Module
- Real-Time Clock With 32 KHz Oscillator and Separate Power Rail
- Crystal oscillators not validated beyond 125°C. Recommend use of external oscillator.
- One 64-Bit General-Purpose Timer (Configurable as Two 32-Bit Timers)
- One 64-Bit General-Purpose Timer/Watchdog Timer (Configurable as Two 32-bit General-Purpose Timers)
- Three Enhanced Pulse Width Modulators (eHRPWM):
  - Dedicated 16-Bit Time-Base Counter With Period And Frequency Control
  - 6 Single Edge, 6 Dual Edge Symmetric or 3 Dual Edge Asymmetric Outputs
  - Dead-Band Generation
  - PWM Chopping by High-Frequency Carrier
  - Trip Zone Input
- Three 32-Bit Enhanced Capture Modules (eCAP):
  - Configurable as 3 Capture Inputs or 3 Auxiliary Pulse Width Modulator (APWM) outputs
  - Single Shot Capture of up to Four Event Time-Stamps
- Two 32-Bit Enhanced Quadrature Encoder Pulse Modules (eQEP)
- 176-pin PowerPAD™ Plastic Quad Flat Pack [PTP suffix], 0.5-mm Pin Pitch
- High Temperature (175°C) Application
- Texas Instruments High Temperature Products Use Highly Optimized Silicon Solutions with Design and Process Enhancements to Maximize Performance over Extended Temperatures. All Devices are Characterized and Qualified for 1000 Hours Continuous Operating Life at Maximum Rated Temperature
- Community Resources
  - TI E2E Community
  - TI Embedded Processors Wiki

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1.3 Description

The OMAPL137 is a low-power applications processor based on an ARM926EJ-S and a C674x DSP core. It consumes significantly lower power than other members of the TMS320C6000 platform of DSPs.

The OMAPL137 enables OEMs and ODMs to quickly bring to market devices featuring robust operating systems support, rich user interfaces, and high processing performance life through the maximum flexibility of a fully integrated mixed processor solution.

The dual-core architecture of the OMAPL137 provides benefits of both DSP and Reduced Instruction Set Computer (RISC) technologies, incorporating a high-performance TMS320C674x DSP core and an ARM926EJ-S core.

The ARM926EJ-S is a 32-bit RISC processor core that performs 32-bit or 16-bit instructions and processes 32-bit, 16-bit, or 8-bit data. The core uses pipelining so that all parts of the processor and memory system can operate continuously.

The ARM core has a coprocessor 15 (CP15), protection module, and Data and program Memory Management Units (MMUs) with table look-aside buffers. It has separate 16K-byte instruction and 16K-byte data caches. Both are four-way associative with virtual index virtual tag (VIVT). The ARM core also has a 8KB RAM (Vector Table) and 64KB ROM.

The OMAPL137 DSP core uses a two-level cache-based architecture. The Level 1 program cache (L1P) is a 32KB direct mapped cache and the Level 1 data cache (L1D) is a 32KB 2-way set-associative cache. The Level 2 program cache (L2P) consists of a 256KB memory space that is shared between program and data space. L2 memory can be configured as mapped memory, cache, or combinations of the two. Although the DSP L2 is accessible by ARM and other hosts in the system, an additional 128KB RAM shared memory is available for use by other hosts without affecting DSP performance.

The peripheral set includes: a 10/100 Mb/s Ethernet MAC (EMAC) with a Management Data Input/Output (MDIO) module; two inter-integrated circuit (I2C) bus interfaces; 3 multichannel audio serial ports (McASP) with 16/12/4 serializers and FIFO buffers; 2 64-bit general-purpose timers each configurable (one configurable as watchdog); a configurable 16-bit host port interface (HPI) ; up to 8 banks of 16 pins of general-purpose input/output (GPIO) with programmable interrupt/event generation modes, multiplexed with other peripherals; 3 UART interfaces (one with RTS and CTS); 3 enhanced high-resolution pulse width modulator (eHRPWM) peripherals; 3 32-bit enhanced capture (eCAP) module peripherals which can be configured as 3 capture inputs or 3 auxiliary pulse width modulator (APWM) outputs; 2 32-bit enhanced quadrature pulse (eQEP) peripherals; and 2 external memory interfaces: an asynchronous and SDRAM external memory interface (EMIFA) for slower memories or peripherals, and a higher speed memory interface (EMIFB) for SDRAM.

The Ethernet Media Access Controller (EMAC) provides an efficient interface between the OMAP-L137 and the network. The EMAC supports both 10Base-T and 100Base-TX, or 10 Mbits/second (Mbps) and 100 Mbps in either half- or full-duplex mode. Additionally an Management Data Input/Output (MDIO) interface is available for PHY configuration.

The HPI, I2C, SPI, USB1.1 and USB2.0 ports allow the device to easily control peripheral devices and/or communicate with host processors.

The rich peripheral set provides the ability to control external peripheral devices and communicate with external processors. For details on each of the peripherals, see the related sections later in this document and the associated peripheral reference guides.

The device has a complete set of development tools for both the ARM and DSP. These include C compilers, a DSP assembly optimizer to simplify programming and scheduling, and a Windows® debugger interface for visibility into source code execution.

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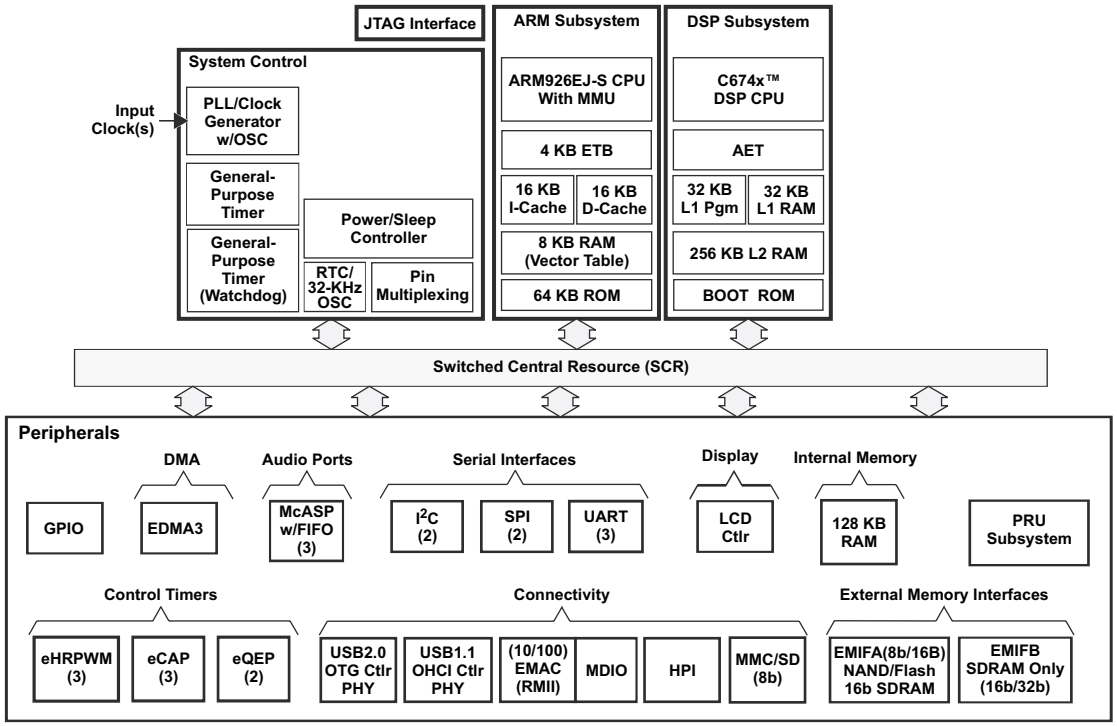
1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the device.



Note: Not all peripherals are available at the same time due to multiplexing.

Figure 1-1. OMAPL137 Functional Block Diagram

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2 Device Overview

2.1 Device Characteristics

Table 2-1 provides an overview of OMAPL137. The table shows significant features of the device, including the capacity of on-chip RAM, peripherals, and the package type with pin count.

Table 2-1. Characteristics of the OMAPL137 Processor

HARDWARE FEATURES		
Peripherals Not all peripherals pins are available at the same time (for more detail, see the Device Configurations section).	EMIFB	SDRAM only, 16-bit bus width, up to 256 Mbit
	EMIFA	Asynchronous (8-bit bus width) RAM, Flash, NOR, NAND
	Flash Card Interface	MMC and SD cards supported.
	EDMA3	32 independent channels, 8 QDMA channels, 2 Transfer controllers
	dMAX	16 independent channels
	Timers	2 64-Bit General Purpose (configurable as 2 separate 32-bit timers, 1 configurable as Watch Dog)
	UART	3 (one with RTS and CTS flow control)
	SPI	2 (Each with one hardware chip select)
	I^2C	2 (both Master/Slave)
	Multichannel Audio Serial Port [McASP]	3 (each with transmit/receive, FIFO buffer, 16/12/4 serializers)
	10/100 Ethernet MAC with Management Data I/O	1 (RMII Interface)
	eHRPWM	6 Single Edge, 6 Dual Edge Symmetric, or 3 Dual Edge Asymmetric Outputs
	eCAP	3 32-bit capture inputs or 3 32-bit auxiliary PWM outputs
	eQEP	2 32-bit QEP channels with 4 inputs/channel
	UHPI	-
	USB 2.0 (USB0)	Full Speed Host Or Device with On-Chip PHY
	USB 1.1 (USB1)	-
	General-Purpose Input/Output Port	8 banks of 16-bit
	LCD Controller	1
	RTC	1 (32 KHz oscillator and seperate power trail. Provides time and date tracking and alarm capability.)
On-Chip Memory	Size (Bytes)	488KB RAM, 1088KB ROM
	Organization	**DSP** 32KB L1 Program (L1P)/Cache (up to 32KB) 32KB L1 Data (L1D)/Cache (up to 32KB) 256KB Unified Mapped RAM/Cache (L2) 1024KB ROM (L2) DSP Memories can be made accessible to ARM, EDMA3, and other peripherals. **ARM** 16KB I-Cache 16KB D-Cache 8KB RAM (Vector Table) 64KB ROM **ADDITIONAL SHARED MEMORY** 128KB RAM
C674x CPU ID + CPU Rev ID	Control Status Register (CSR.[31:16])	0x1400
C674x Megamodule Revision	Revision ID Register (MM_REVID[15:0])	0x0000
JTAG BSDL_ID	DEVIDR0 register	0x8B7DF02F
CPU Frequency	MHz	674x DSP 300 MHz
		ARM926 300 MHz

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Table 2-1. Characteristics of the OMAPL137 Processor (continued)

HARDWARE FEATURES		
Cycle Time	ns	674x DSP 3.3$\overline{3}$ ns
		ARM926 3.3$\overline{3}$ ns
Voltage	Core (V)	1.2 V
	I/O (V)	3.3 V
Package		24 mm x 24 mm, 176-Pin, 0.5 mm pitch, TQFP (PTP)
Product Status(1)	Product Preview (PP), Advance Information (AI), or Production Data (PD)	AI

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2.2 Device Compatibility

The ARM926EJ-S RISC CPU is compatible with other ARM9 CPUs from ARM Holdings plc.

The C674x DSP core is code-compatible with the C6000™ DSP platform and supports features of both the C64x+ and C67x+ DSP families.

2.3 ARM Subsystem

The ARM Subsystem includes the following features:

- ARM926EJ-S RISC processor
- ARMv5TEJ (32/16-bit) instruction set
- Little endian
- System Control Co-Processor 15 (CP15)
- MMU
- 16KB Instruction cache
- 16KB Data cache
- Write Buffer
- Embedded Trace Module and Embedded Trace Buffer (ETM/ETB)
- ARM Interrupt controller

2.3.1 ARM926EJ-S RISC CPU

The ARM Subsystem integrates the ARM926EJ-S processor. The ARM926EJ-S processor is a member of ARM9 family of general-purpose microprocessors. This processor is targeted at multi-tasking applications where full memory management, high performance, low die size, and low power are all important. The ARM926EJ-S processor supports the 32-bit ARM and 16 bit THUMB instruction sets, enabling the user to trade off between high performance and high code density. Specifically, the ARM926EJ-S processor supports the ARMv5TEJ instruction set, which includes features for efficient execution of Java byte codes, providing Java performance similar to Just in Time (JIT) Java interpreter, but without associated code overhead.

The ARM926EJ-S processor supports the ARM debug architecture and includes logic to assist in both hardware and software debug. The ARM926EJ-S processor has a Harvard architecture and provides a complete high performance subsystem, including:

- ARM926EJ -S integer core
- CP15 system control coprocessor
- Memory Management Unit (MMU)

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- Separate instruction and data Caches
- Write buffer
- Separate instruction and data (internal RAM) interfaces
- Separate instruction and data AHB bus interfaces
- Embedded Trace Module and Embedded Trace Buffer (ETM/ETB)

For more complete details on the ARM9, refer to the ARM926EJ-S Technical Reference Manual, available at http://www.arm.com

2.3.2 CP15

The ARM926EJ-S system control coprocessor (CP15) is used to configure and control instruction and data caches, Memory Management Unit (MMU), and other ARM subsystem functions. The CP15 registers are programmed using the MRC and MCR ARM instructions, when the ARM in a privileged mode such as supervisor or system mode.

2.3.3 MMU

A single set of two level page tables stored in main memory is used to control the address translation, permission checks and memory region attributes for both data and instruction accesses. The MMU uses a single unified Translation Lookaside Buffer (TLB) to cache the information held in the page tables. The MMU features are:

- Standard ARM architecture v4 and v5 MMU mapping sizes, domains and access protection scheme.
- Mapping sizes are:
  - 1MB (sections)
  - 64KB (large pages)
  - 4KB (small pages)
  - 1KB (tiny pages)
- Access permissions for large pages and small pages can be specified separately for each quarter of the page (subpage permissions)
- Hardware page table walks
- Invalidate entire TLB, using CP15 register 8
- Invalidate TLB entry, selected by MVA, using CP15 register 8
- Lockdown of TLB entries, using CP15 register 10

2.3.4 Caches and Write Buffer

The size of the Instruction Cache is 16KB, Data cache is 16KB. Additionally, the Caches have the following features:

- Virtual index, virtual tag, and addressed using the Modified Virtual Address (MVA)
- Four-way set associative, with a cache line length of eight words per line (32-bytes per line) and with two dirty bits in the Dcache
- Dcache supports write-through and write-back (or copy back) cache operation, selected by memory region using the C and B bits in the MMU translation tables.
- Critical-word first cache refilling
- Cache lockdown registers enable control over which cache ways are used for allocation on a line fill, providing a mechanism for both lockdown, and controlling cache corruption
- Dcache stores the Physical Address TAG (PA TAG) corresponding to each Dcache entry in the TAG RAM for use during the cache line write-backs, in addition to the Virtual Address TAG stored in the TAG RAM. This means that the MMU is not involved in Dcache write-back operations, removing the possibility of TLB misses related to the write-back address.
- Cache maintenance operations provide efficient invalidation of, the entire Dcache or Icache, regions of the Dcache or Icache, and regions of virtual memory.

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The write buffer is used for all writes to a noncachable bufferable region, write-through region and write misses to a write-back region. A separate buffer is incorporated in the Dcache for holding write-back for cache line evictions or cleaning of dirty cache lines. The main write buffer has 16-word data buffer and a four-address buffer. The Dcache write-back has eight data word entries and a single address entry.

2.3.5 Advanced High-Performance Bus (AHB)

The ARM Subsystem uses the AHB port of the ARM926EJ-S to connect the ARM to the Config bus and the external memories. Arbiters are employed to arbitrate access to the separate D-AHB and I-AHB by the Config Bus and the external memories bus.

2.3.6 Embedded Trace Macrocell (ETM) and Embedded Trace Buffer (ETB)

To support real-time trace, the ARM926EJ-S processor provides an interface to enable connection of an Embedded Trace Macrocell (ETM). The ARM926EJ-S Subsystem in the device also includes the Embedded Trace Buffer (ETB). The ETM consists of two parts:

- Trace Port provides real-time trace capability for the ARM9.
- Triggering facilities provide trigger resources, which include address and data comparators, counter, and sequencers.

The device trace port is not pinned out and is instead only connected to the Embedded Trace Buffer. The ETB has a 4KB buffer memory. ETB enabled debug tools are required to read/interpret the captured trace data.

This device uses ETM9™ version r2p2 and ETB version r0p1. Documentation on the ETM and ETB is available from ARM Ltd. Reference the ' CoreSight™ ETM9™ Technical Reference Manual, revision r0p1' and the 'ETM9 Technical Reference Manual, revision r2p2'.

2.3.7 ARM Memory Mapping

By default the ARM has access to most on and off chip memory areas, including the DSP Internal memories, EMIFA, EMIFB, and the additional 128K byte on chip shared SRAM. Likewise almost all of the on chip peripherals are accessible to the ARM by default.

To improve security and/or robustness the device has extensive memory and peripheral protection units which can be configured to limit access rights to the various on / off chip resources to specific hosts; including the ARM as well as other master peripherals. This allows the system tasks to be partitioned between the ARM and DSP as best suites the particular application; while enhancing the overall robustness of the solution.

See Table 2-3 for a detailed top level OMAPL137 memory map that includes the ARM memory space.

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2.4 DSP Subsystem

The DSP Subsystem includes the following features:

- C674x DSP CPU
- 32KB L1 Program (L1P)/Cache (up to 32KB)
- 32KB L1 Data (L1D)/Cache (up to 32KB)
- 256KB Unified Mapped RAM/Cache (L2)
- 1MB Mask-programmable ROM
- Little endian

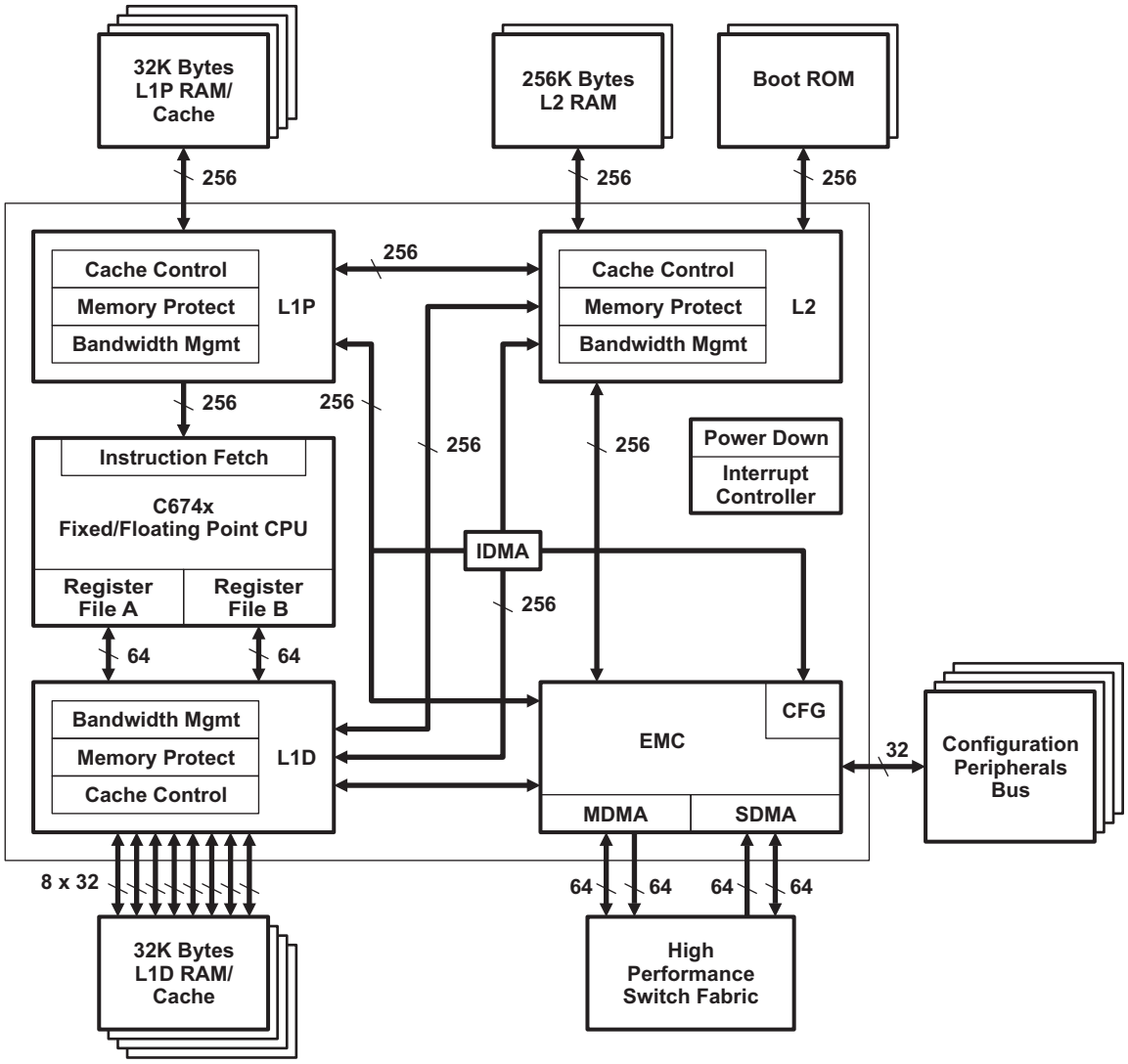

Figure 2-1. C674x Megamodule Block Diagram

2.4.1 C674x DSP CPU Description

The C674x Central Processing Unit (CPU) consists of eight functional units, two register files, and two data paths as shown in Figure 2-2. The two general-purpose register files (A and B) each contain 32 32-bit registers for a total of 64 registers. The general-purpose registers can be used for data or can be data address pointers. The data types supported include packed 8-bit data, packed 16-bit data, 32-bit data, 40-bit data, and 64-bit data. Values larger than 32 bits, such as 40-bit-long or 64-bit-long values are stored in register pairs, with the 32 LSBs of data placed in an even register and the remaining 8 or 32 MSBs in the next upper register (which is always an odd-numbered register).

The eight functional units (.M1, .L1, .D1, .S1, .M2, .L2, .D2, and .S2) are each capable of executing one instruction every clock cycle. The .M functional units perform all multiply operations. The .S and .L units perform a general set of arithmetic, logical, and branch functions. The .D units primarily load data from memory to the register file and store results from the register file into memory.

The C674x CPU combines the performance of the C64x+ core with the floating-point capabilities of the C67x core.

Each C674x .M unit can perform one of the following each clock cycle: one 32 x 32 bit multiply, one 16 x 32 bit multiply, two 16 x 16 bit multiplies, two 16 x 32 bit multiplies, two 16 x 16 bit multiplies with add/subtract capabilities, four 8 x 8 bit multiplies, four 8 x 8 bit multiplies with add operations, and four 16 x 16 multiplies with add/subtract capabilities (including a complex multiply). There is also support for Galois field multiplication for 8-bit and 32-bit data. Many communications algorithms such as FFTs and modems require complex multiplication. The complex multiply (CMPY) instruction takes four 16-bit inputs and produces a 32-bit real and a 32-bit imaginary output. There are also complex multiplies with rounding capability that produces one 32-bit packed output that contain 16-bit real and 16-bit imaginary values. The 32 x 32 bit multiply instructions provide the extended precision necessary for audio and other high-precision algorithms on a variety of signed and unsigned 32-bit data types.

The .L or (Arithmetic Logic Unit) now incorporates the ability to do parallel add/subtract operations on a pair of common inputs. Versions of this instruction exist to work on 32-bit data or on pairs of 16-bit data performing dual 16-bit add and subtracts in parallel. There are also saturated forms of these instructions.

The C674x core enhances the .S unit in several ways. On previous cores, dual 16-bit MIN2 and MAX2 comparisons were only available on the .L units. On the C674x core they are also available on the .S unit which increases the performance of algorithms that do searching and sorting. Finally, to increase data packing and unpacking throughput, the .S unit allows sustained high performance for the quad 8-bit/16-bit and dual 16-bit instructions. Unpack instructions prepare 8-bit data for parallel 16-bit operations. Pack instructions return parallel results to output precision including saturation support.

Other new features include:

- **SPLOOP** - A small instruction buffer in the CPU that aids in creation of software pipelining loops where multiple iterations of a loop are executed in parallel. The SPLOOP buffer reduces the code size associated with software pipelining. Furthermore, loops in the SPLOOP buffer are fully interruptible.
- **Compact Instructions** - The native instruction size for the C6000 devices is 32 bits. Many common instructions such as MPY, AND, OR, ADD, and SUB can be expressed as 16 bits if the C674x compiler can restrict the code to use certain registers in the register file. This compression is performed by the code generation tools.
- **Instruction Set Enhancement** - As noted above, there are new instructions such as 32-bit multiplications, complex multiplications, packing, sorting, bit manipulation, and 32-bit Galois field multiplication.
- **Exceptions Handling** - Intended to aid the programmer in isolating bugs. The C674x CPU is able to detect and respond to exceptions, both from internally detected sources (such as illegal op-codes) and from system events (such as a watchdog time expiration).
- **Privilege** - Defines user and supervisor modes of operation, allowing the operating system to give a basic level of protection to sensitive resources. Local memory is divided into multiple pages, each with read, write, and execute permissions.

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- **Time-Stamp Counter** - Primarily targeted for Real-Time Operating System (RTOS) robustness, a free-running time-stamp counter is implemented in the CPU which is ***not*** sensitive to system stalls.

For more details on the C674x CPU and its enhancements over the C64x architecture, see the following documents:

- *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide* (literature number SPRU732)
- *TMS320C64x Technical Overview* (literature number SPRU395)

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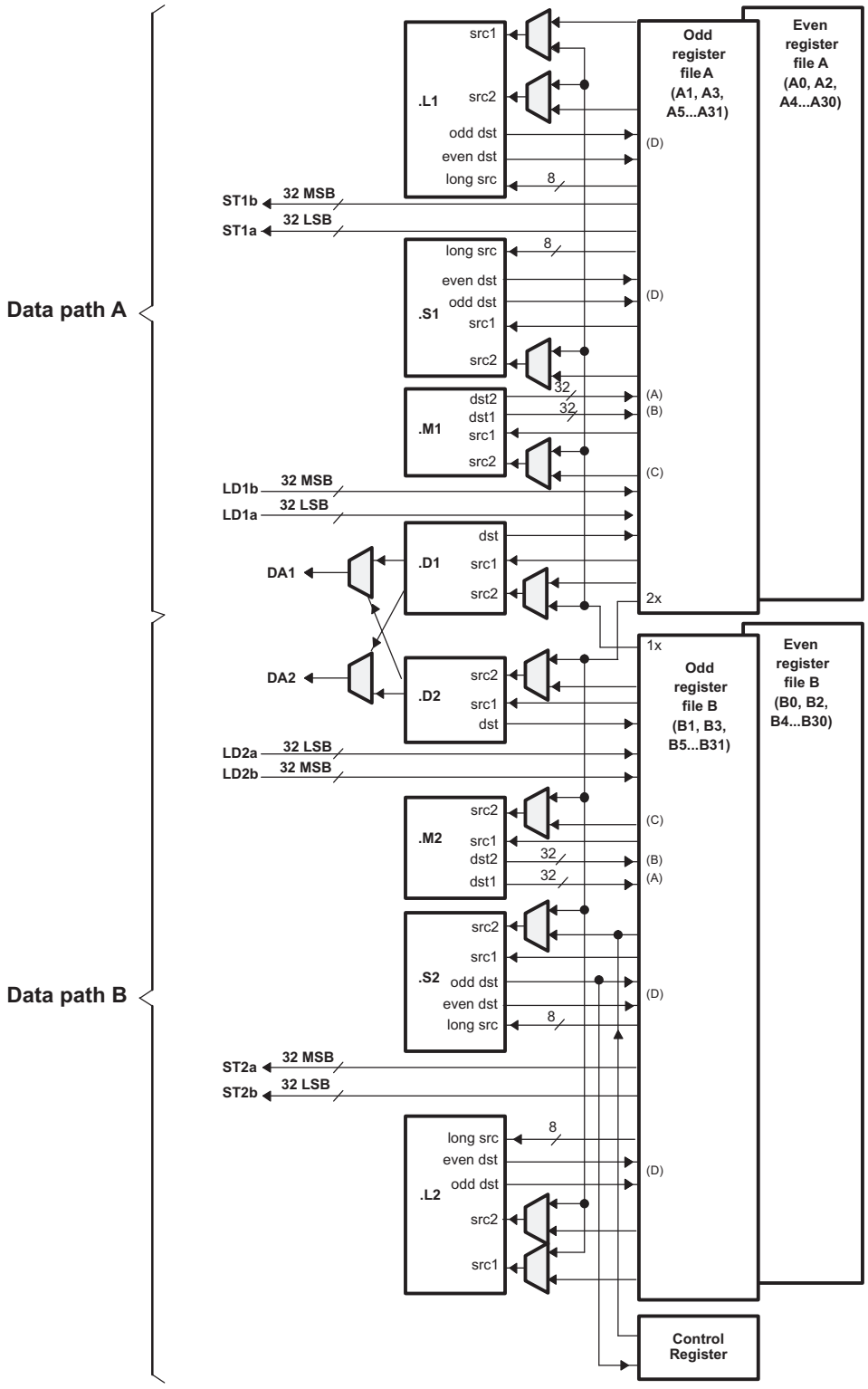

Figure 2-2. TMS320C674x™ CPU (DSP Core) Data Paths

2.4.2 DSP Memory Mapping

The DSP memory map is shown in Section 2.5

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By default the DSP also has access to most on and off chip memory areas, with the exception of the ARM RAM, ROM, and AINTC interrupt controller. The DSP also boots first, and must release the ARM from reset before the ARM can execute any code.

Additionally, the DSP megamodule includes the capability to limit access to its internal memories through its SDMA port; without needing an external MPU unit.

2.4.2.1 ARM Internal Memories

The DSP does not have access to the ARM internal memory.

2.4.2.2 External Memories

The DSP has access to the following External memories:

- Asynchronous EMIF / SDRAM / NAND / NOR Flash (EMIFA)
- SDRAM (EMIFB)

2.4.2.3 DSP Internal Memories

The DSP has access to the following DSP memories:

- L2 RAM
- L1P RAM
- L1D RAM

2.4.2.4 C674x CPU

The C674x core uses a two-level cache-based architecture. The Level 1 Program cache (L1P) is 32 KB direct mapped cache and the Level 1 Data cache (L1D) is 32 KB 2-way set associated cache. The Level 2 memory/cache (L2) consists of a 256 KB memory space that is shared between program and data space. L2 memory can be configured as mapped memory, cache, or a combination of both.

Table 2-2 shows a memory map of the C674x CPU cache registers for the device.

Table 2-2. C674x Cache Registers

HEX ADDRESS RANGE	REGISTER ACRONYM	DESCRIPTION
0x0184 0000	L2CFG	L2 Cache configuration register
0x0184 0020	L1PCFG	L1P Size Cache configuration register
0x0184 0024	L1PCC	L1P Freeze Mode Cache configuration register
0x0184 0040	L1DCFG	L1D Size Cache configuration register
0x0184 0044	L1DCC	L1D Freeze Mode Cache configuration register
0x0184 0048 - 0x0184 0FFC	-	Reserved
0x0184 1000	EDMAWEIGHT	L2 EDMA access control register
0x0184 1004 - 0x0184 1FFC	-	Reserved
0x0184 2000	L2ALLOC0	L2 allocation register 0
0x0184 2004	L2ALLOC1	L2 allocation register 1
0x0184 2008	L2ALLOC2	L2 allocation register 2
0x0184 200C	L2ALLOC3	L2 allocation register 3
0x0184 2010 - 0x0184 3FFF	-	Reserved
0x0184 4000	L2WBAR	L2 writeback base address register
0x0184 4004	L2WWC	L2 writeback word count register
0x0184 4010	L2WIBAR	L2 writeback invalidate base address register
0x0184 4014	L2WIWC	L2 writeback invalidate word count register
0x0184 4018	L2IBAR	L2 invalidate base address register
0x0184 401C	L2IWC	L2 invalidate word count register
0x0184 4020	L1PIBAR	L1P invalidate base address register

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Table 2-2. C674x Cache Registers (continued)

HEX ADDRESS RANGE	REGISTER ACRONYM	DESCRIPTION
0x0184 4024	L1PIWC	L1P invalidate word count register
0x0184 4030	L1DWIBAR	L1D writeback invalidate base address register
0x0184 4034	L1DWIWC	L1D writeback invalidate word count register
0x0184 4038	-	Reserved
0x0184 4040	L1DWBAR	L1D Block Writeback
0x0184 4044	L1DWWC	L1D Block Writeback
0x0184 4048	L1DIBAR	L1D invalidate base address register
0x0184 404C	L1DIWC	L1D invalidate word count register
0x0184 4050 - 0x0184 4FFF	-	Reserved
0x0184 5000	L2WB	L2 writeback all register
0x0184 5004	L2WBINV	L2 writeback invalidate all register
0x0184 5008	L2INV	L2 Global Invalidate without writeback
0x0184 500C - 0x0184 5027	-	Reserved
0x0184 5028	L1PINV	L1P Global Invalidate
0x0184 502C - 0x0184 5039	-	Reserved
0x0184 5040	L1DWB	L1D Global Writeback
0x0184 5044	L1DWBINV	L1D Global Writeback with Invalidate
0x0184 5048	L1DINV	L1D Global Invalidate without writeback
0x0184 8000 – 0x0184 80FF	MAR0 - MAR63	Reserved 0x0000 0000 – 0x3FFF FFFF
0x0184 8100 – 0x0184 817F	MAR64 – MAR95	Memory Attribute Registers for EMIFA SDRAM Data (CS0) 0x4000 0000 – 0x5FFF FFFF
0x0184 8180 – 0x0184 8187	MAR96 - MAR97	Memory Attribute Registers for EMIFA Async Data (CS2) 0x6000 0000 – 0x61FF FFFF
0x0184 8188 – 0x0184 818F	MAR98 – MAR99	Memory Attribute Registers for EMIFA Async Data (CS2) 0x6200 0000 – 0x63FF FFFF
0x0184 8190 – 0x0184 8197	MAR100 – MAR101	Memory Attribute Registers for EMIFA Async Data (CS2) 0x6400 0000 – 0x65FF FFFF
0x0184 8198 – 0x0184 819F	MAR102 – MAR103	Memory Attribute Registers for EMIFA Async Data (CS2) 0x6600 0000 – 0x67FF FFFF
0x0184 81A0 – 0x0184 81FF	MAR104 – MAR127	Reserved 0x6800 0000 – 0x7FFF FFFF
0x0184 8200	MAR128	Memory Attribute Register for Shared RAM 0x8000 0000 – 0x8001 FFFF
		Reserved 0x8002 0000 – 0x81FF FFFF
0x0184 8204 – 0x0184 82FF	MAR129 – MAR191	Reserved 0x8200 0000 – 0xBFFF FFFF
0x0184 8300 – 0x0184 837F	MAR192 – MAR223	Memory Attribute Registers for EMIFD SDRAM Data (CS2) 0xC000 0000 – 0xDFFF FFFF
0x0184 8380 – 0x0184 83FF	MAR224 – MAR255	Reserved 0xE000 0000 – 0xFFFF FFFF

See Table 2-3 for a detailed top level OMAPL137 memory map that includes the DSP memory space.

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2.5 Memory Map Summary

Table 2-3. OMAPL137 Top Level Memory Map

Start Address	End Address	Size	ARM Mem Map	DSP Mem Map	EDMA Mem Map	dMAX Mem Map	Master Peripheral Mem Map	LCDC Mem Map
0x0000 0000	0x0000 0FFF	4K	-			dMAX Local Address Space	-	
0x0000 1000	0x006F FFFF	6M + 1020K	-					
0x0070 0000	0x007F FFFF	1024K	-	DSP L2 ROM	-			
0x0080 0000	0x0083 FFFF	256K	-	DSP L2 RAM	-			
0x0084 0000	0x00DF FFFF	5M + 768K	-					
0x00E0 0000	0x00E0 7FFF	32K	-	DSP L1P RAM	-			
0x00E0 8000	0x00EF FFFF	992K	-					
0x00F0 0000	0x00F0 7FFF	32K	-	DSP L1D RAM	-			
0x00F0 8000	0x017F FFFF	8M + 992K	-					
0x0180 0000	0x0180 FFFF	64K	-	DSP Interrupt Controller	-			
0x0181 0000	0x0181 0FFF	4K	-	DSP Powerdown Controller	-			
0x0181 1000	0x0181 1FFF	4K	-	DSP Security ID	-			
0x0181 2000	0x0181 2FFF	4K	-	DSP Revision ID	-			
0x0181 3000	0x0181 FFFF	52K	-	-	-			
0x0182 0000	0x0182 FFFF	64K	-	DSP EMC	-			
0x0183 0000	0x0183 FFFF	64K	-	DSP Internal Reserved	-			
0x0184 0000	0x0184 FFFF	64K	-	DSP Memory System	-			
0x0185 0000	0x0187 FFFF	192K	-					
0x0188 0000	0x01BC 03FF	3M + 257K	-					
0x01BC 0400	0x01BC 042F	48	-					
0x01BC 0430	0x01BC 044F	32	-					
0x01BC 0000	0x01BC 0FFF	4K	ARM ETB memory	-				
0x01BC 1000	0x01BC 17FF	2K	ARM ETB reg	-				
0x01BC 1800	0x01BC 18FF	256	ARM Ice Crusher	-				
0x01BC 0500	0x01BC FFFF	62K + 768	-					
0x01BD 0000	0x01BD FFFF	64K	-					
0x01BE 0000	0x01BF FFFF	128K	-					
0x01C0 0000	0x01C0 7FFF	32K	EDMA3 CC					-
0x01C0 8000	0x01C0 83FF	1024	EDMA3 TC0					-
0x01C0 8400	0x01C0 87FF	1024	EDMA3 TC1					-
0x01C0 8800	0x01C0 FFFF	30K	-					
0x01C1 0000	0x01C1 0FFF	4K	PSC 0					-
0x01C1 1000	0x01C1 1FFF	4K	PLL Controller					-
0x01C1 2000	0x01C1 3FFF	8K	-					
0x01C1 4000	0x01C1 4FFF	4K	SYSCFG					-

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Table 2-3. OMAPL137 Top Level Memory Map (continued)

Start Address	End Address	Size	ARM Mem Map	DSP Mem Map	EDMA Mem Map	dMAX Mem Map	Master Peripheral Mem Map	LCDC Mem Map
0x01C1 5000	0x01C1 5FFF	4K	-					
0x01C1 6000	0x01C1 6FFF	4K	-					
0x01C1 7000	0x01C1 7FFF	4K	-					
0x01C1 8000	0x01C1 FFFF	32K	-					
0x01C2 0000	0x01C2 0FFF	4K	Timer64P 0					-
0x01C2 1000	0x01C2 1FFF	4K	Timer64P 1					-
0x01C2 2000	0x01C2 2FFF	4K	I2C 0					-
0x01C2 3000	0x01C2 3FFF	4K	RTC					-
0x01C2 4000	0x01C2 4FFF	4K	-					
0x01C2 5000	0x01C2 FFFF	44K	-					
0x01C3 0000	0x01C3 01FF	512	dMAX Data RAM 0					-
0x01C3 0200	0x01C3 1FFF	7K + 512	-					
0x01C3 2000	0x01C3 21FF	512	dMAX Data RAM 1					-
0x01C3 2200	0x01C3 3FFF	7K + 512	-					
0x01C3 4000	0x01C3 7FFF	16K	dMAX Control Registers					-
0x01C3 8000	0x01C3 8FFF	4K	dMAX MAX0 Configuration Memory					-
0x01C3 9000	0x01C3 BFFF	12K	-					
0x01C3 C000	0x01C3 CFFF	4K	dMAX MAX1 Configuration Memory					-
0x01C3 D000	0x01C3 FFFF	12K	-					
0x01C4 0000	0x01C4 0FFF	4K	MMC/SD 0					-
0x01C4 1000	0x01C4 1FFF	4K	SPI 0					-
0x01C4 2000	0x01C4 2FFF	4K	UART 0					-
0x01C4 3000	0x01C4 3FFF	4K	-					
0x01C4 4000	0x01CF FFFF	752K	-					
0x01D0 0000	0x01D0 0FFF	4K	McASP 0 Control					-
0x01D0 1000	0x01D0 1FFF	4K	McASP 0 AFIFO Ctrl					-
0x01D0 2000	0x01D0 2FFF	4K	McASP 0 Data					-
0x01D0 3000	0x01D0 3FFF	4K	-					
0x01D0 4000	0x01D0 4FFF	4K	McASP 1 Control					-
0x01D0 5000	0x01D0 5FFF	4K	McASP 1 AFIFO Ctrl					-
0x01D0 6000	0x01D0 6FFF	4K	McASP 1 Data					-
0x01D0 7000	0x01D0 7FFF	4K	-					
0x01D0 8000	0x01D0 8FFF	4K	McASP 2 Control					-
0x01D0 9000	0x01D0 9FFF	4K	McASP 2 AFIFO Ctrl					-
0x01D0 A000	0x01D0 AFFF	4K	McASP 2 Data					-
0x01D0 B000	0x01D0 BFFF	4K	-					
0x01D0 C000	0x01D0 CFFF	4K	UART 1					-
0x01D0 D000	0x01D0 DFFF	4K	UART 2					-
0x01D0 E000	0x01D0 EFFF	4K	-					
0x01D0 F000	0x01DF FFFF	964K	-					
0x01E0 0000	0x01E0 FFFF	64K	USB0					-
0x01E1 0000	0x01E1 0FFF	4K	UHPI					-
0x01E1 1000	0x01E1 1FFF	4K	-					
0x01E1 2000	0x01E1 2FFF	4K	SPI 1					-

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Table 2-3. OMAPL137 Top Level Memory Map (continued)

Start Address	End Address	Size	ARM Mem Map	DSP Mem Map	EDMA Mem Map	dMAX Mem Map	Master Peripheral Mem Map	LCDC Mem Map
0x01E1 3000	0x01E1 3FFF	4K	LCD Controller					-
0x01E1 4000	0x01E1 4FFF	4K	MPU 1					-
0x01E1 5000	0x01E1 5FFF	4K	MPU 2					-
0x01E1 6000	0x01E1 FFFF	40K	-					
0x01E2 0000	0x01E2 1FFF	8K	EMAC Control Module RAM					-
0x01E2 2000	0x01E2 2FFF	4K	EMAC Control Module Registers					-
0x01E2 3000	0x01E2 3FFF	4K	EMAC Control Registers					-
0x01E2 4000	0x01E2 4FFF	4K	EMAC MDIO port					-
0x01E2 5000	0x01E2 5FFF	4K	USB1					-
0x01E2 6000	0x01E2 6FFF	4K	GPIO					-
0x01E2 7000	0x01E2 7FFF	4K	PSC 1					-
0x01E2 8000	0x01E2 8FFF	4K	I2C 1					-
0x01E2 9000	0x01E2 9FFF	4K	-					
0x01E2 A000	0x01EF FFFF	856K	-					
0x01F0 0000	0x01F0 0FFF	4K	EPWM 0					-
0x01F0 1000	0x01F0 1FFF	4K	HRPWM 0					-
0x01F0 2000	0x01F0 2FFF	4K	eHRPWM 1					-
0x01F0 3000	0x01F0 3FFF	4K	HRPWM 1					-
0x01F0 4000	0x01F0 4FFF	4K	eHRPWM 2					-
0x01F0 5000	0x01F0 5FFF	4K	HRPWM 2					-
0x01F0 6000	0x01F0 6FFF	4K	ECAP 0					-
0x01F0 7000	0x01F0 7FFF	4K	ECAP 1					-
0x01F0 8000	0x01F0 8FFF	4K	ECAP 2					-
0x01F0 9000	0x01F0 9FFF	4K	EQEP 0					-
0x01F0 A000	0x01F0 AFFF	4K	EQEP 1					-
0x01F0 B000	0x01F0 BFFF	4K	-					
0x01F0 C000	0x116F FFFF	247M + 976K	-					
0x1170 0000	0x117F FFFF	1024K	DSP L2 ROM					-
0x1180 0000	0x1183 FFFF	256K	DSP L2 RAM					-
0x1184 0000	0x11DF FFFF	5M + 768K	-					
0x11E0 0000	0x11E0 7FFF	32K	DSP L1P RAM					-
0x11E0 8000	0x11EF FFFF	992K	-					
0x11F0 0000	0x11F0 7FFF	32K	DSP L1D RAM					-
0x11F0 8000	0x3FFF FFFF	736M + 992K	-					
0x4000 0000	0x5FFF FFFF	512M	EMIFA SDRAM data (CS0)					-
0x6000 0000	0x61FF FFFF	32M	EMIFA async data (CS2)					-
0x6200 0000	0x63FF FFFF	32M	EMIFA async data (CS3)					-
0x6400 0000	0x65FF FFFF	32M	EMIFA async data (CS4)					-
0x6600 0000	0x67FF FFFF	32M	EMIFA async data (CS5)					-
0x6800 0000	0x6800 7FFF	32K	EMIFA Control Regs					-
0x6800 8000	0x7FFF FFFF	383M + 992K	-					
0x8000 0000	0x8001 FFFF	128K	Shared RAM					-

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Table 2-3. OMAPL137 Top Level Memory Map (continued)

Start Address	End Address	Size	ARM Mem Map	DSP Mem Map	EDMA Mem Map	dMAX Mem Map	Master Peripheral Mem Map	LCDC Mem Map
0x8002 0000	0xAFFF FFFF	767M + 896K	-					
0xB000 0000	0xB000 7FFF	32K	EMIFB Control Regs					
0xB000 8000	0xBFFF FFFF	255M + 992K	-					
0xC000 0000	0xDFFF FFFF	512M	EMIFB SDRAM Data					
0xE000 0000	0xFFFC FFFF	511M + 832K	-					
0xFFFD 0000	0xFFFD FFFF	64K	ARM local ROM	-				
0xFFFE 0000	0xFFFE DFFF	56K	-					
0xFFFE E000	0xFFFE FFFF	8K	ARM Interrupt Controller	-				
0xFFFF 0000	0xFFFF 1FFF	8K	ARM local RAM	-				
0xFFFF 2000	0xFFFF FFFF	56K	-					

The DSP L2 ROM is used for boot purposes and cannot be programmed with application code.

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2.6 Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
380 µm	Silicon with backgrind	Floating	TaN/AlCu	1000 nm

Table 2-4. Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
AXR1_00	1	209.005	13.225	274.005	78.225
UART0_RXD	2	279.005	13.225	344.005	78.225
UART0_TXD	3	349.005	13.225	414.005	78.225
AXR1_10	4	419.005	13.225	484.005	78.225
VDDSHV	5	509.005	13.225	574.005	78.225
N/C	6	582.755	13.225	647.755	78.225
VSS	7	652.755	13.225	717.755	78.225
AXR1_11	8	722.755	13.225	787.755	78.225
SPI0_SCSN	9	792.755	13.225	857.755	78.225
VDD	10	862.755	13.225	927.755	78.225
SPI0_CLK	11	932.755	13.225	997.755	78.225
SPI0_ENAN	12	1002.755	13.225	1067.755	78.225
SPI1_SOMI	13	1072.755	13.225	1137.755	78.225
SPI1_SIMO	14	1142.755	13.225	1207.755	78.225
VDDSHV	15	1212.755	13.225	1277.755	78.225
VSS	16	1299.005	13.225	1364.005	78.225
N/C	17	1372.755	13.225	1437.755	78.225
SPI1_CLK	18	1442.755	13.225	1507.755	78.225
SPI0_SOMI	19	1512.755	13.225	1577.755	78.225
SPI0_SIMO	20	1582.755	13.225	1647.755	78.225
EMA_WAIT	21	1652.755	13.225	1717.755	78.225
VDD	22	1722.755	13.225	1787.755	78.225
EMA_OEN	23	1792.755	13.225	1857.755	78.225
EMA_CSN_2	24	1862.755	13.225	1927.755	78.225
VDDSHV	25	1932.755	13.225	1997.755	78.225
N/C	26	2002.755	13.225	2067.755	78.225
VSS	27	2089.005	13.225	2154.005	78.225
N/C	28	2159.005	13.225	2224.005	78.225
N/C	29	2229.005	13.225	2294.005	78.225
EMA_BA_1	30	2299.005	13.225	2364.005	78.225
EMA_A_10	31	2369.005	13.225	2434.005	78.225
VDD	32	2439.005	13.225	2504.005	78.225
EMA_A_00	33	2509.005	13.225	2574.005	78.225
EMA_A_01	34	2579.005	13.225	2644.005	78.225
EMA_A_02	35	2649.005	13.225	2714.005	78.225
EMA_A_03	36	2719.005	13.225	2784.005	78.225
VDDSHV	37	2789.005	13.225	2854.005	78.225
VSS	38	2879.005	13.225	2944.005	78.225
N/C	39	2954.005	13.225	3019.005	78.225
EMA_A_04	40	3024.005	13.225	3089.005	78.225
EMA_A_05	41	3094.005	13.225	3159.005	78.225
EMA_A_06	42	3164.005	13.225	3229.005	78.225
EMA_A_07	43	3234.005	13.225	3299.005	78.225
VDD	44	3304.005	13.225	3369.005	78.225
EMA_A_08	45	3374.005	13.225	3439.005	78.225
EMA_A_09	46	3444.005	13.225	3509.005	78.225
EMA_A_11	47	3514.005	13.225	3579.005	78.225

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Table 2-4. Bond Pad Coordinates in Microns (continued)

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
EMA_A_12	48	3584.005	13.225	3649.005	78.225
N/C	49	3654.005	13.225	3719.005	78.225
VDDSHV	50	3739.005	13.225	3804.005	78.225
N/C	51	3814.005	13.225	3879.005	78.225
N/C	52	3884.005	13.225	3949.005	78.225
N/C	53	3954.005	13.225	4019.005	78.225
N/C	54	4024.005	13.225	4089.005	78.225
VSS	55	4094.005	13.225	4159.005	78.225
N/C	56	4284.785	209.005	4349.785	274.005
EMA_D_00	57	4284.785	279.435	4349.785	344.435
N/C	58	4284.785	349.865	4349.785	414.865
EMA_D_01	59	4284.785	420.295	4349.785	485.295
EMA_D_02	60	4284.785	510.725	4349.785	575.725
N/C	61	4284.785	580.91	4349.785	645.91
N/C	62	4284.785	650.91	4349.785	715.91
VDDSHV	63	4284.785	720.91	4349.785	785.91
N/C	64	4284.785	790.91	4349.785	855.91
VSS	65	4284.785	860.91	4349.785	925.91
EMA_D_03	66	4284.785	930.91	4349.785	995.91
N/C	67	4284.785	1000.91	4349.785	1065.91
EMA_D_04	68	4284.785	1070.91	4349.785	1135.91
N/C	69	4284.785	1140.91	4349.785	1205.91
VDD	70	4284.785	1210.91	4349.785	1275.91
N/C	71	4284.785	1280.91	4349.785	1345.91
EMA_D_05	72	4284.785	1355.885	4349.785	1420.885
N/C	73	4284.785	1444.97	4349.785	1509.97
EMA_D_06	74	4284.785	1514.97	4349.785	1579.97
N/C	75	4284.785	1584.97	4349.785	1649.97
VSS	76	4284.785	1654.97	4349.785	1719.97
VDDSHV	77	4284.785	1724.97	4349.785	1789.97
N/C	78	4284.785	1794.97	4349.785	1859.97
N/C	79	4284.785	1864.97	4349.785	1929.97
N/C	80	4284.785	1934.97	4349.785	1999.97
EMA_D_07	81	4284.785	2004.97	4349.785	2069.97
N/C	82	4284.785	2074.97	4349.785	2139.97
EMA_WEN	83	4284.785	2150.615	4349.785	2215.615
N/C	84	4284.785	2235.345	4349.785	2300.345
VDD	85	4284.785	2305.345	4349.785	2370.345
VSS	86	4284.785	2375.345	4349.785	2440.345
N/C	87	4284.785	2445.345	4349.785	2510.345
VDDSHV	88	4284.785	2515.345	4349.785	2580.345
VDDSHV	89	4284.785	2585.345	4349.785	2650.345
VDD	90	4284.785	2655.345	4349.785	2720.345
VDD	91	4284.785	2725.345	4349.785	2790.345
N/C	92	4284.785	2795.345	4349.785	2860.345
VSS	93	4284.785	2865.345	4349.785	2930.345
N/C	94	4284.785	2935.345	4349.785	3000.345

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Table 2-4. Bond Pad Coordinates in Microns (continued)

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
VDDSHV	95	4284.785	3015.775	4349.785	3080.775
VDDAR1	96	4284.785	3106.205	4349.785	3171.205
N/C	97	4284.785	3176.635	4349.785	3241.635
N/C	98	4284.785	3247.065	4349.785	3312.065
VDDNWA1	99	4284.785	3325.925	4349.785	3390.925
VDDNWA1	100	4284.785	3400.02	4349.785	3465.02
VDD	101	4284.785	3470.02	4349.785	3535.02
VSS	102	4284.785	3540.02	4349.785	3605.02
VDDSHV	103	4284.785	3610.02	4349.785	3675.02
N/C	104	4284.785	3680.02	4349.785	3745.02
N/C	105	4284.785	3750.02	4349.785	3815.02
VSS	106	4284.785	3824.225	4349.785	3889.225
N/C	107	4284.785	3913.46	4349.785	3978.46
VDDSHV	108	4284.785	3983.46	4349.785	4048.46
VDD	109	4284.785	4053.46	4349.785	4118.46
N/C	110	4284.785	4123.46	4349.785	4188.46
N/C	111	4284.785	4193.46	4349.785	4258.46
VSS	112	4284.785	4263.46	4349.785	4328.46
N/C	113	4284.785	4333.46	4349.785	4398.46
VDDSHV	114	4284.785	4407.665	4349.785	4472.665
VSS	115	4284.785	4497.34	4349.785	4562.34
N/C	116	4284.785	4567.34	4349.785	4632.34
N/C	117	4284.785	4637.34	4349.785	4702.34
VDDSHV	118	4284.785	4707.34	4349.785	4772.34
VSS	119	4284.785	4777.34	4349.785	4842.34
VDDSHV	120	4284.785	4847.34	4349.785	4912.34
VDD	121	4284.785	4917.34	4349.785	4982.34
N/C	122	4284.785	4987.34	4349.785	5052.34
VSS	123	4284.785	5061.535	4349.785	5126.535
VDDSHV	124	4284.785	5150.345	4349.785	5215.345
VDD	125	4284.785	5220.345	4349.785	5285.345
VSS	126	4284.785	5290.345	4349.785	5355.345
VDDSHV	127	4284.785	5360.345	4349.785	5425.345
AXR0_00	128	4284.785	5430.345	4349.785	5495.345
N/C	129	4284.785	5500.345	4349.785	5565.345
AXR0_01	130	4284.785	5574.545	4349.785	5639.545
AXR0_02	131	4284.785	5665.445	4349.785	5730.445
VDD	132	4090.765	5861.225	4155.765	5926.225
N/C	133	4020.555	5861.225	4085.555	5926.225
N/C	134	3949.215	5861.225	4014.215	5926.225
N/C	135	3878.885	5861.225	3943.885	5926.225
N/C	136	3808.415	5861.225	3873.415	5926.225
N/C	137	3738.31	5861.225	3803.31	5926.225
AXR0_03	138	3663.735	5861.225	3728.735	5926.225
N/C	139	3588.51	5861.225	3653.51	5926.225
AXR0_05	140	3518.415	5861.225	3583.415	5926.225
AXR0_06	141	3447.745	5861.225	3512.745	5926.225

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Table 2-4. Bond Pad Coordinates in Microns (continued)

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
VSS	142	3376.035	5861.225	3441.035	5926.225
VDDSHV	143	3304.27	5861.225	3369.27	5926.225
AXR0_07	144	3233.645	5861.225	3298.645	5926.225
AXR0_08	145	3163.25	5861.225	3228.25	5926.225
AFSX0	146	3089.875	5861.225	3154.875	5926.225
VDDSHV	147	3019.115	5861.225	3084.115	5926.225
N/C	148	2948.625	5861.225	3013.625	5926.225
VSS	149	2869.395	5861.225	2934.395	5926.225
AHCLKR0	150	2798.835	5861.225	2863.835	5926.225
AFSR0	151	2726.12	5861.225	2791.12	5926.225
VPP	152	2652.81	5861.225	2717.81	5926.225
VPP	153	2581.05	5861.225	2646.05	5926.225
IFORCE	154	2510.13	5861.225	2575.13	5926.225
VSENSE	155	2439.42	5861.225	2504.42	5926.225
VDDA18V_USB1	156	2369.155	5861.225	2434.155	5926.225
VSS	157	2298.685	5861.225	2363.685	5926.225
USB1_DP	158	2228.45	5861.225	2293.45	5926.225
N/C	159	2158.275	5861.225	2223.275	5926.225
USB1_DM	160	2087.535	5861.225	2152.535	5926.225
VDDA33_USB1	161	2009.505	5861.225	2074.505	5926.225
VDD	162	1936.205	5861.225	2001.205	5926.225
VSS	163	1865.53	5861.225	1930.53	5926.225
USB0_ID	164	1795.4	5861.225	1860.4	5926.225
USB0_VBUS	165	1722.27	5861.225	1787.27	5926.225
VDDA12_USB0	166	1649.685	5861.225	1714.685	5926.225
VDDA18_USB0	167	1579.34	5861.225	1644.34	5926.225
VSSA_USB0	168	1509.05	5861.225	1574.05	5926.225
USB0_DP	169	1438.645	5861.225	1503.645	5926.225
N/C	170	1368.375	5861.225	1433.375	5926.225
USB0_DM	171	1298.05	5861.225	1363.05	5926.225
VSSA33_USB0	172	1219.04	5861.225	1284.04	5926.225
VDDA33_USB0	173	1147.91	5861.225	1212.91	5926.225
VSS	174	1076.44	5861.225	1141.44	5926.225
VDDA12_PLL	175	998.275	5861.225	1063.275	5926.225
VSSA12_PLL	176	925.39	5861.225	990.39	5926.225
OSCIN	177	854.085	5861.225	919.085	5926.225
OSCVSS	178	782.785	5861.225	847.785	5926.225
RESETN	179	709.655	5861.225	774.655	5926.225
VDD	180	637.15	5861.225	702.15	5926.225
N/C	181	559.62	5861.225	624.62	5926.225
RTC_XI	182	489.565	5861.225	554.565	5926.225
RTC_VSS	183	419.505	5861.225	484.505	5926.225
RTC_XO	184	349.49	5861.225	414.49	5926.225
VDD2	185	279.295	5861.225	344.295	5926.225
N/C	186	209.175	5861.225	274.175	5926.225
TRSTN	187	13.225	5666.345	78.225	5731.345
TRSTN	188	13.225	5595.145	78.225	5660.145

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Table 2-4. Bond Pad Coordinates in Microns (continued)

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
N/C	189	13.225	5524.925	78.225	5589.925
N/C	190	13.225	5454.07	78.225	5519.07
N/C	191	13.225	5382.485	78.225	5447.485
N/C	192	13.225	5311.205	78.225	5376.205
N/C	193	13.225	5228.885	78.225	5293.885
N/C	194	13.225	5154.21	78.225	5219.21
N/C	195	13.225	5079.015	78.225	5144.015
N/C	196	13.225	5008.685	78.225	5073.685
N/C	197	13.225	4937.99	78.225	5002.99
N/C	198	147.195	4831.665	212.195	4896.665
N/C	199	147.195	4735.485	212.195	4800.485
VSS	200	147.195	4622.615	212.195	4687.615
VDDSHV	201	147.195	4435.67	212.195	4500.67
N/C	202	147.195	4360.73	212.195	4425.73
TDI	203	147.795	4235.69	212.795	4300.69
VDD	204	147.795	4164.985	212.795	4229.985
N/C	205	147.795	4069.08	212.795	4134.08
TCK	206	147.795	3989.035	212.795	4054.035
N/C	207	13.225	3906.515	78.225	3971.515
TDO	208	13.225	3836.385	78.225	3901.385
VDDSHV	209	13.225	3766.245	78.225	3831.245
N/C	210	13.225	3696.23	78.225	3761.23
VSS	211	13.225	3626.11	78.225	3691.11
VDDAR	212	13.225	3548.85	78.225	3613.85
VDDNWA	213	13.225	3478.71	78.225	3543.71
VDD	214	13.225	3406.13	78.225	3471.13
VDD	215	13.225	3335.39	78.225	3400.39
VDDSHV	216	13.225	3264.465	78.225	3329.465
N/C	217	13.225	3193.185	78.225	3258.185
N/C	218	13.225	3121.465	78.225	3186.465
VSS	219	13.225	3051.285	78.225	3116.285
AFSR1	220	13.225	2977.55	78.225	3042.55
N/C	221	13.225	2907.235	78.225	2972.235
VDD	222	13.225	2830.14	78.225	2895.14
VDD	223	13.225	2746.55	78.225	2811.55
VDDSHV	224	13.225	2674	78.225	2739
VSS	225	13.225	2603.34	78.225	2668.34
VSS	226	13.225	2524.765	78.225	2589.765
N/C	227	13.225	2452.975	78.225	2517.975
AXR1_04	228	13.225	2380.355	78.225	2445.355
AXR1_03	229	13.225	2306.825	78.225	2371.825
AXR1_02	230	13.225	2236.715	78.225	2301.715
AXR1_01	231	13.225	2155.32	78.225	2220.32
N/C	232	13.225	2077.3	78.225	2142.3
N/C	233	13.225	2006.525	78.225	2071.525
N/C	234	13.225	1934.25	78.225	1999.25
N/C	235	13.225	1864.03	78.225	1929.03

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Table 2-4. Bond Pad Coordinates in Microns (continued)

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
N/C	236	13.225	1793.885	78.225	1858.885
N/C	237	13.225	1723.855	78.225	1788.855
N/C	238	13.225	1653.45	78.225	1718.45
N/C	239	13.225	1582.67	78.225	1647.67
N/C	240	13.225	1512.07	78.225	1577.07
N/C	241	13.225	1436.115	78.225	1501.115
N/C	242	13.225	1361.85	78.225	1426.85
N/C	243	13.225	1290.35	78.225	1355.35
N/C	244	13.225	1218.39	78.225	1283.39
N/C	245	13.225	1147.875	78.225	1212.875
N/C	246	13.225	1073.32	78.225	1138.32
N/C	247	13.225	1000.655	78.225	1065.655
N/C	248	13.225	929.045	78.225	994.045
N/C	249	13.225	858.22	78.225	923.22
N/C	250	13.225	788.035	78.225	853.035
N/C	251	13.225	715.485	78.225	780.485
N/C	252	13.225	641.13	78.225	706.13
N/C	253	13.225	570.685	78.225	635.685
N/C	254	13.225	488.67	78.225	553.67
N/C	255	13.225	417.65	78.225	482.65
N/C	256	13.225	346.84	78.225	411.84
N/C	257	13.225	275.62	78.225	340.62

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2.7 Pin Assignments

Extensive use of pin multiplexing is used to accommodate the largest number of peripheral functions in the smallest possible package. Pin multiplexing is controlled using a combination of hardware configuration at device reset and software programmable register settings.

2.7.1 Pin Map (Bottom View)

Figure 2-3 shows the pin assignments for the PTP package. Note that micro-vias are not required. Contact your TI representative for routing recommendations.

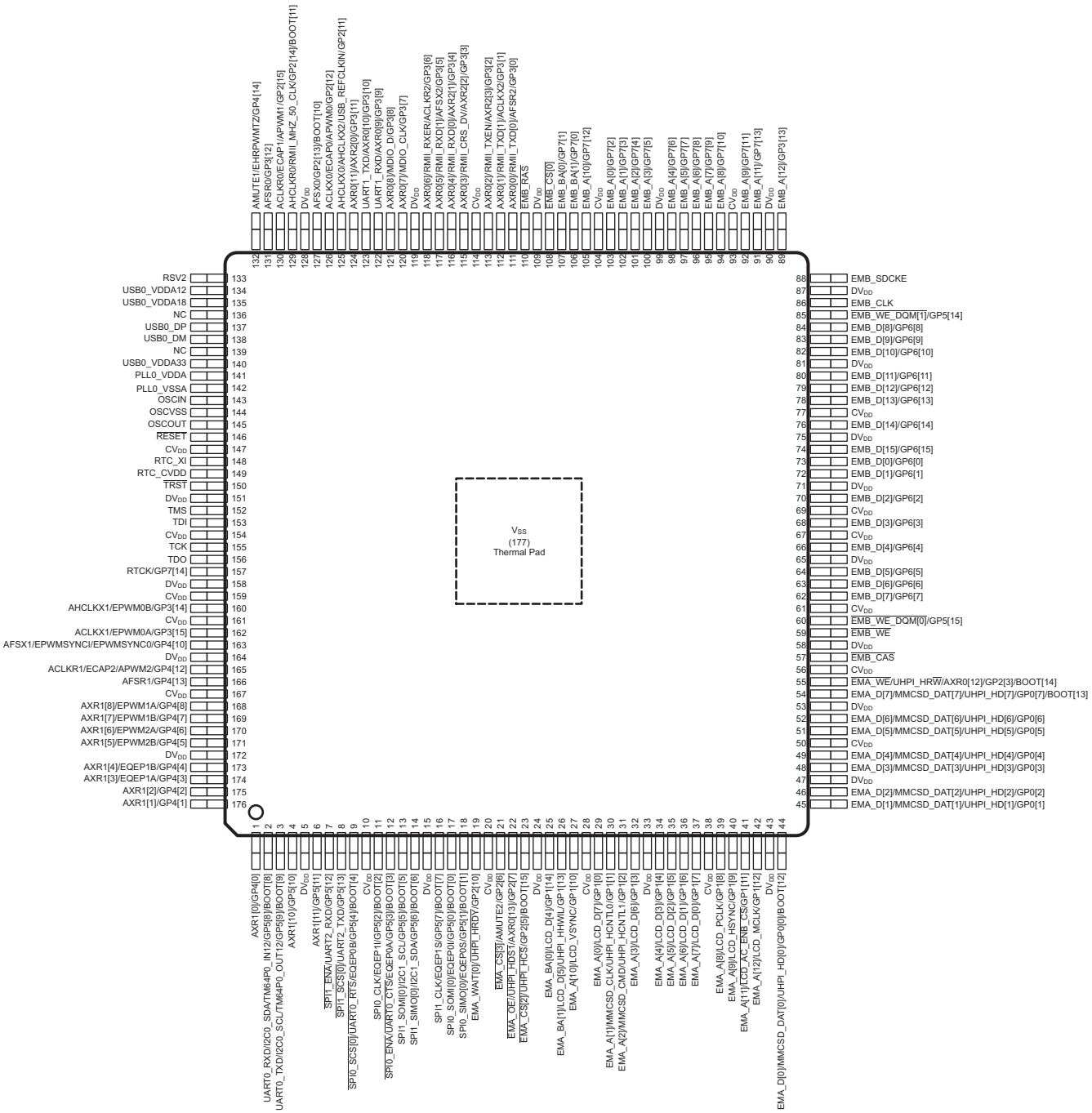

Figure 2-3. Pin Map (PTP)

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2.8 Terminal Functions

Table 2-5 to Table 2-25 identify the external signal names, the associated pin/ball numbers along with the mechanical package designator, the pin type (I, O, IO, OZ, or PWR), whether the pin/ball has any internal pullup/pulldown resistors, whether the pin/ball is configurable as an IO in GPIO mode, and a functional pin description.

2.8.1 Device Reset and JTAG

Table 2-5. Reset and JTAG Terminal Functions

SIGNAL NAME	PIN NO	TYPE(1)	PULL(2)	DESCRIPTION
	PTP			
RESET				
$\overline{\text{RESET}}$	146	I		Device reset input
JTAG				
TMS	152	I	IPU	JTAG test mode select
TDI	153	I	IPU	JTAG test data input
TDO	156	O	IPD	JTAG test data output
TCK	155	I	IPU	JTAG test clock
$\overline{\text{TRST}}$	150	I	IPD	JTAG test reset
RTCK/GP7[14]	157	I/O	IPD	JTAG test-port return clock output.

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor, IPU = Internal Pullup resistor

2.8.2 High-Frequency Oscillator and PLL

Table 2-6. High-Frequency Oscillator and PLL Terminal Functions

SIGNAL NAME	PIN NO	TYPE(1)	PULL(2)	DESCRIPTION
	PTP			
1.2-V OSCILLATOR				
OSCIN	143	I		Oscillator input
OSCOUT	145	O		Oscillator output
OSCVSS	144	GND		Oscillator ground (for filter only)
1.2-V PLL				
PLL0_VDDA	141	PWR		PLL analog V_{DD} (1.2-V filtered supply)
PLL0_VSSA	142	GND		PLL analog V_{SS} (for filter)

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor, IPU = Internal Pullup resistor

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2.8.3 Real-Time Clock and 32-kHz Oscillator

Table 2-7. Real-Time Clock (RTC) and 1.2-V, 32-kHz Oscillator Terminal Functions

SIGNAL NAME	PIN NO	TYPE(1)	PULL(2)	DESCRIPTION
	PTP			
RTC_CVDD	149	PWR		RTC module core power (isolated from rest of chip CV_{DD})
RTC_XI	148	I		Low-frequency (32-kHz) oscillator receiver for real-time clock

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor, IPU = Internal Pullup resistor

2.8.4 External Memory Interface A (ASYNC, SDRAM)

Table 2-8. External Memory Interface A (EMIFA) Terminal Functions

SIGNAL NAME	PIN NO	TYPE(1)	PULL(2)	MUXED	DESCRIPTION
	PTP				
EMA_D[7]/MMCSD_DAT[7]/UHPI_HD[7]/GP0[7]/BOOT[13]	54	I/O	IPU	MMC/SD, UHPI, GPIO, BOOT	EMIFA data bus
EMA_D[6]/MMCSD_DAT[6]/UHPI_HD[6]/GP0[6]	52	I/O	IPU	MMC/SD, UHPI, GPIO	
EMA_D[5]/MMCSD_DAT[5]/UHPI_HD[5]/GP0[5]	51	I/O	IPU		
EMA_D[4]/MMCSD_DAT[4]/UHPI_HD[4]/GP0[4]	49	I/O	IPU		
EMA_D[3]/MMCSD_DAT[3]/UHPI_HD[3]/GP0[3]	48	I/O	IPU		
EMA_D[2]/MMCSD_DAT[2]/UHPI_HD[2]/GP0[2]	46	I/O	IPU		
EMA_D[1]/MMCSD_DAT[1]/UHPI_HD[1]/GP0[1]	45	I/O	IPU		
EMA_D[0]/MMCSD_DAT[0]/UHPI_HD[0]/GP0[0]/BOOT[12]	44	I/O	IPU	MMC/SD, UHPI, GPIO, BOOT	
EMA_A[12]/ LCD_MCLK/GP1[12]	42	O	IPU	LCD, GPIO	EMIFA address bus
EMA_A[11]/ LCD_AC_ENB_CS/GP1[11]	41	O	IPU		
EMA_A[10]/ LCD_VSYNC/GP1[10]	27	O	IPU		
EMA_A[9]/ LCD_HSYNC/GP1[9]	40	O	IPU		
EMA_A[8]/ LCD_PCLK/GP1[8]	39	O	IPU		
EMA_A[7]/ LCD_D[0]/GP1[7]	37	O	IPD		
EMA_A[6]/ LCD_D[1]/GP1[6]	36	O	IPD		
EMA_A[5]/ LCD_D[2]/GP1[5]	35	O	IPD		
EMA_A[4]/ LCD_D[3]/GP1[4]	34	O	IPD		
EMA_A[3]/ LCD_D[6]/GP1[3]	32	O	IPD		
EMA_A[2]/MMCSD_CMD/UHPI_HCNTL1/GP1[2]	31	O	IPU	MMCSD, UHPI, GPIO	EMIFA address bus.
EMA_A[1]/MMCSD_CLK/UHPI_HCNTL0/GP1[1]	30	O	IPU		
EMA_A[0]/ LCD_D[7]/GP1[0]	29	O	IPD	LCD, GPIO	
EMA_BA[1]/ LCD_D[5]/UHPI_HHWIL/GP1[13]	26	O	IPU	LCD, UHPI, GPIO	EMIFA bank address
EMA_BA[0]/ LCD_D[4]/GP1[14]	25	O	IPU	LCD, GPIO	

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor, IPU = Internal Pullup resistor

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Table 2-8. External Memory Interface A (EMIFA) Terminal Functions (continued)

SIGNAL NAME	PIN NO	TYPE[1]	PULL[2]	MUXED	DESCRIPTION
	PTP				
EMA_CS[3] /AMUTE2/GP2[6]	21	O	IPU	McASP2, GPIO	EMIFA Async Chip Select
EMA_CS[2] /UHPI_HCS/GP2[5]/BOOT[15]	23	O	IPU	UHPI, GPIO, BOOT	
EMA_WE /UHPI_HRW/AXR0[12]/GP2[3]/BOOT[14]	55	O	IPU	UHPI, MCASP0, GOPIO, BOOT	EMIFA SDRAM write enable.
EMA_OE /UHPI_HDS1/AXR0[13]/GP2[7]	22	O	IPU	UHPI, McASP0, GPIO	EMIFA output enable.
EMA_WAIT[0]/ UHPI_HRDY/GP2[10]	19	I	IPU	UHPI, GPIO	EMIFA wait input/interrupt.

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2.8.5 External Memory Interface B (only SDRAM)

Table 2-9. External Memory Interface B (EMIFB) Terminal Functions

SIGNAL NAME	PIN NO	TYPE(1)	PULL(2)	MUXED	DESCRIPTION
	PTP				
EMB_D[15]/GP6[15]	74	I/O	IPD	GPIO	EMIFB SDRAM data bus.
EMB_D[14]/GP6[14]	76	I/O	IPD		
EMB_D[13]/GP6[13]	78	I/O	IPD		
EMB_D[12]/GP6[12]	79	I/O	IPD		
EMB_D[11]/GP6[11]	80	I/O	IPD		
EMB_D[10]/GP6[10]	82	I/O	IPD		
EMB_D[9]/GP6[9]	83	I/O	IPD		
EMB_D[8]/GP6[8]	84	I/O	IPD		
EMB_D[7]/GP6[7]	62	I/O	IPD		
EMB_D[6]/GP6[6]	63	I/O	IPD		
EMB_D[5]/GP6[5]	64	I/O	IPD		
EMB_D[4]/GP6[4]	66	I/O	IPD		
EMB_D[3]/GP6[3]	68	I/O	IPD		
EMB_D[2]/GP6[2]	70	I/O	IPD		
EMB_D[1]/GP6[1]	72	I/O	IPD		
EMB_D[0]/GP6[0]	73	I/O	IPD		
EMB_A[12]/GP3[13]	89	O	IPD	GPIO	EMIFB SDRAM row/column address bus.
EMB_A[11]/GP7[13]	91	O	IPD		
EMB_A[10]/GP7[12]	105	O	IPD		
EMB_A[9]/GP7[11]	92	O	IPD		
EMB_A[8]/GP7[10]	94	O	IPD		
EMB_A[7]/GP7[9]	95	O	IPD		
EMB_A[6]/GP7[8]	96	O	IPD		
EMB_A[5]/GP7[7]	97	O	IPD		
EMB_A[4]/GP7[6]	98	O	IPD	GPIO	EMIFB SDRAM row/column address.
EMB_A[3]/GP7[5]	100	O	IPD		
EMB_A[2]/GP7[4]	101	O	IPD		
EMB_A[1]/GP7[3]	102	O	IPD		
EMB_A[0]/GP7[2]	103	O	IPD		
EMB_BA[1]/GP7[0]	106	O	IPU		EMIFB SDRAM bank address.
EMB_BA[0]/GP7[1]	107	O	IPU		
EMB_CLK	86	O	IPU		EMIF SDRAM clock.
EMB_SDCKE	88	I/O	IPU		EMIFB SDRAM clock enable.
$\overline{\text{EMB_WE}}$	59	O	IPU		EMIFB write enable
$\overline{\text{EMB_RAS}}$	110	O	IPU		EMIFB SDRAM row address strobe.
$\overline{\text{EMB_CAS}}$	57	O	IPU		EMIFB column address strobe.
$\overline{\text{EMB_CS[0]}}$	108	O	IPU		EMIFB SDRAM chip select 0.

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor, IPU = Internal Pullup resistor

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Table 2-9. External Memory Interface B (EMIFB) Terminal Functions (continued)

SIGNAL NAME	PIN NO	TYPE(1)	PULL(2)	MUXED	DESCRIPTION
	PTP				
EMB_WE_DQM[1] /GP5[14]	85	O	IPU	GPIO	EMIFB write enable/data mask for EMB_D.
EMB_WE_DQM[0] /GP5[15]	60	O	IPU		

2.8.6 Serial Peripheral Interface Modules (SPI0, SPI1)

Table 2-10. Serial Peripheral Interface (SPI) Terminal Functions

SIGNAL NAME	PIN NO	TYPE(1)	PULL(2)	MUXED	DESCRIPTION
	PTP				
SPI0					
SPI0_SCS[0] /UART0_RTS/EQEP0B/GP5[4]/BOOT[4]	9	I/O	IPU	UART0, EQEP0B, GPIO, BOOT	SPI0 chip select.
SPI0_ENA /UART0_CTS/EQEP0A/GP5[3]/BOOT[3]	12	I/O	IPU	UART0, EQEP0A, GPIO, BOOT	SPI0 enable.
SPI0_CLK/EQEP1I/GP5[2]/BOOT[2]	11	I/O	IPD	eQEP1, GPIO, BOOT	SPI0 clock.
SPI0_SIMO[0]/EQEP0S/GP5[1]/BOOT[1]	18	I/O	IPD	eQEP0, GPIO, BOOT	SPI0 data slave-in-master-out.
SPI0_SOMI[0]/EQEP0I/GP5[0]/BOOT[0]	17	I/O	IPD		SPI0 data slave-out-master-in.
SPI1					
SPI1_SCS[0] /UART2_TXD/GP5[13]	8	I/O	IPU	UART2, GPIO	SPI1 chip select.
SPI1_ENA /UART2_RXD/GP5[12]	7	I/O	IPU		SPI1 enable.
SPI1_CLK/EQEP1S/GP5[7]/BOOT[7]`	16	I/O	IPD	eQEP1, GPIO, BOOT	SPI1 clock.
SPI1_SIMO[0]/I2C1_SDA/GP5[6]/BOOT[6]	14	I/O	IPU	I2C1, GPIO, BOOT	SPI1 data slave-in-master-out.
SPI1_SOMI[0]/I2C1_SCL/GP5[5]/BOOT[5]	13	I/O	IPU		SPI1 data slave-out-master-in.

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor, IPU = Internal Pullup resistor

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2.8.7 Enhanced Capture/Auxiliary PWM Modules (eCAP0, eCAP1, eCAP2)

The eCAP Module pins function as either input captures or auxiliary PWM 32-bit outputs, depending upon how the eCAP module is programmed.

Table 2-11. Enhanced Capture Module (eCAP) Terminal Functions

SIGNAL NAME	PIN NO	TYPE(1)	PULL(2)	MUXED	DESCRIPTION
	PTP				
eCAP0					
ACLKX0/**ECAP0/APWM0**/GP2[12]	126	I/O	IPD	McASP0, GPIO	enhanced capture 0 input or auxiliary PWM 0 output.
eCAP1					
ACLKR0/**ECAP1/APWM1**/GP2[15]	130	I/O	IPD	McASP0, GPIO	enhanced capture 1 input or auxiliary PWM 1 output.
eCAP2					
ACLKR1**/ECAP2/APWM2**/GP4[12]	165	I/O	IPD	McASP1, GPIO	enhanced capture 2 input or auxiliary PWM 2 output.

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor, IPU = Internal Pullup resistor

2.8.8 Enhanced Pulse Width Modulators (eHRPWM0, eHRPWM1, eHRPWM2)

Table 2-12. Enhanced Pulse Width Modulator (eHRPWM) Terminal Functions

SIGNAL NAME	PIN NO	TYPE(1)	PULL(2)	MUXED	DESCRIPTION
	PTP				
eHRPWM0					
ACLKX1/**EPWM0A**/GP3[15]	162	I/O	IPD	McASP1, GPIO	eHRPWM0 A output.
AHCLKX1/**EPWM0B**/GP3[14]	160	I/O	IPD		eHRPWM0 B output.
AMUTE1/**EPWMTZ**/GP4[14]	132	I/O	IPD	McASP1, eHRPWM1, GPIO, eHRPWM2	eHRPWM0 trip zone input.
AFSX1/**EPWMSYNCI/EPWMSYNCO**/GP4[10]	163	I/O	IPD	McASP1, eHRPWM0, GPIO	Sync input to eHRPWM0 module or sync output to external PWM.
eHRPWM1					
AXR1[8]/**EPWM1A**/GP4[8]	168	I/O	IPD	McASP1, GPIO	eHRPWM1 A (with high-resolution).
AXR1[7]/**EPWM1B**/GP4[7]	169	I/O	IPD		eHRPWM1 B.
AMUTE1/**EPWMTZ**/GP4[14]	132	I/O	IPD	McASP1, eHRPWM0, GPIO, eHRPWM2	eHRPWM1 trip zone input.
eHRPWM2					

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor, IPU = Internal Pullup resistor

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Table 2-12. Enhanced Pulse Width Modulator (eHRPWM) Terminal Functions (continued)

SIGNAL NAME	PIN NO	TYPE(1)	PULL(2)	MUXED	DESCRIPTION
	PTP				
AXR1[6]/**EPWM2A**/GP4[6]	170	I/O	IPD	McASP1, GPIO	eHRPWM2 A (with high-resolution).
AXR1[5]/**EPWM2B**/GP4[5]	171	I/O	IPD		eHRPWM2 B.
AMUTE1/**EPWMTZ**/GP4[14]	132	I/O	IPD	McASP1, eHRPWM0, GPIO, eHRPWM2	eHRPWM2 trip zone input.

2.8.9 Enhanced Quadrature Encoder Pulse Module (eQEP)

Table 2-13. Enhanced Quadrature Encoder Pulse Module (eQEP) Terminal Functions

SIGNAL NAME	PIN NO	TYPE(1)	PULL(2)	MUXED	DESCRIPTION
	PTP				
eQEP0					
$\overline{\text{SPI0_ENA}}$/$\overline{\text{UART0_CTS}}$/**EQEP0A**/GP5[3]/BOOT[3]	12	I	IPU	SPIO, UART0, GPIO, BOOT	eQEP0A quadrature input.
$\overline{\text{SPI0_SCS[0]}}$/$\overline{\text{UART0_RTS}}$/**EQEP0B**/GP5[4]/BOOT[4]	9	I	IPU		eQEP0B quadrature input.
SPI0_SOMI[0]/**EQEP0I**/GP5[0]/BOOT[0]	17	I	IPD	SPI0, GPIO, BOOT	eQEP0 index.
SPI0_SIMO[0]/**EQEP0S**/GP5[1]/BOOT[1]	18	I	IPD		eQEP0 strobe.
eQEP1					
AXR1[3]/**EQEP1A**/GP4[3]	174	I	IPD	McASP1, GPIO	eQEP1A quadrature input.
AXR1[4]/**EQEP1B**/GP4[4]	173	I	IPD		eQEP1B quadrature input.
SPI0_CLK/**EQEP1I**/GP5[2]/BOOT[2]	11	I	IPD	SPI0, GPIO, BOOT	eQEP1 index.
SPI1_CLK/**EQEP1S**/GP5[7]/BOOT[7]	16	I	IPD	SPI1, GPIO, BOOT	eQEP1 strobe.

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor, IPU = Internal Pullup resistor

2.8.10 Boot

Table 2-14. Boot Terminal Functions(1)

SIGNAL NAME	PIN NO	TYPE(2)	PULL(3)	MUXED	DESCRIPTION
	PTP				
$\overline{\text{EMA_CS[2]}}$/$\overline{\text{UHPI_HCS}}$/GP2[5]/**BOOT[15]**	23	I	IPU	EMIFA, UHPI, GPIO	BOOT[15].
$\overline{\text{EMA_WE}}$/UHPI_HR$\overline{\text{W}}$/AXR0[12]/GP2[3]/**BOOT[14]**	55	I	IPU	EMIFA, UHPI, McASP0, GPIO	BOOT[14].
EMA_D[7]/MMCSD_DAT[7]/UHPI_HD[7]/GP0[7]/**BOOT[13]**	54	I	IPU	EMIFA, MMC/SD, UHPI, GPIO	BOOT[13].
EMA_D[0]/MMCSD_DAT[0]/UHPI_HD[0]/GP0[0]/**BOOT[12]**	44	I	IPU		BOOT[12].
AHCLKR0/RMII_MHZ_50_CLK/GP2[14]/**BOOT[11]**	129	I	IPD	McASP0, EMAC, GPIO	BOOT[11].
AFSX0/GP2[13]/**BOOT[10]**	127	I	IPD	McASP0, GPIO	BOOT[10].

(1) Boot decoding will be defined in the ROM datasheet.
(2) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(3) IPD = Internal Pulldown resistor, IPU = Internal Pullup resistor

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Table 2-14. Boot Terminal Functions[1] (continued)

SIGNAL NAME	PIN NO	TYPE[2]	PULL[3]	MUXED	DESCRIPTION
	PTP				
UART0_TXD/I2C0_SCL/TM64P0_OUT12/GP5[9]/**BOOT[9]**	3	I	IPU	UART0, I2C0, Timer0, GPIO	BOOT[9].
UART0_RXD/I2C0_SDA/TM64P0_IN12/GP5[8]/**BOOT[8]**	2	I	IPU	UART0, I2C0, Timer0, GPIO	BOOT[8].
SPI1_CLK/EQEP1S/GP5[7]/**BOOT[7]**	16	I	IPD	SPI1, eQEP1, GPIO	BOOT[7].
SPI1_SIMO[0]/I2C1_SDA/GP5[6]/**BOOT[6]**	14	I	IPU	SPI1, I2C1, GPIO	BOOT[6].
SPI1_SOMI[0]/I2C1_SCL/GP5[5]/**BOOT[5]**	13	I	IPU		BOOT[5].
$\overline{\text{SPI0_SCS[0]}}$/$\overline{\text{UART0_RTS}}$/EQEP0B/GP5[4]/**BOOT[4]**	9	I	IPU	SPI0, UART0, eQEP0, GPIO	BOOT[4].
$\overline{\text{SPI0_ENA}}$/$\overline{\text{UART0_CTS}}$/EQEP0A/GP5[3]/**BOOT[3]**	12	I	IPU	SPI0, UART0, eQEP0, GPIO	BOOT[3].
SPI0_CLK/EQEP1I/GP5[2]/**BOOT[2]**	11	I	IPD	SPIO, eQEP1, GPIO	BOOT[2].
SPI0_SIMO[0]/EQEP0S/GP5[1]/**BOOT[1]**	18	I	IPD	SPI0, eQEP0, GPIO	BOOT[1].
SPI0_SOMI[0]/EQEP0I/GP5[0]/**BOOT[0]**	17	I	IPD		BOOT[0].

2.8.11 Universal Asynchronous Receiver/Transmitters (UART0, UART1, UART2)

Table 2-15. Universal Asynchronous Receiver/Transmitter (UART) Terminal Functions

SIGNAL NAME	PIN NO	TYPE[1]	PULL[2]	MUXED	DESCRIPTION
	PTP				
UART0					
UART0_RXD/I2C0_SDA/TM64P0_IN12/GP5[8]/BOOT[8]	2	I	IPU	I2C0, BOOT, Timer0, GPIO,	UART0 receive data.
UART0_TXD/I2C0_SCL/TM64P0_OUT12/GP5[9]/BOOT[9]	3	O	IPU	I2C0, Timer0, GPIO, BOOT	UART0 transmit data.
$\overline{\text{SPI0_SCS[0]}}$/ **$\overline{\text{UART0_RTS}}$** /EQEP0B/GP5[4]/BOOT[4]	9	O	IPU	SPIO, eQEP0, GPIO, BOOT	UART0 ready-to-send output
$\overline{\text{SPI0_ENA}}$/ **$\overline{\text{UART0_CTS}}$** /EQEP0A/GP5[3]/BOOT[3]	12	I	IPU		UART0 clear-to-send input
UART1					
UART1_RXD/AXR0[9]/GP3[9][3]	122	I	IPD	McASP0, GPIO	UART1 receive data.
UART1_TXD/AXR0[10]/GP3[10][3]	123	O	IPD		UART1 transmit data.
UART2					
$\overline{\text{SPI1_ENA}}$/**UART2_RXD**/GP5[12]	7	I	IPU	SPI1, GPIO	UART2 receive data.
$\overline{\text{SPI1_SCS[0]}}$/**UART2_TXD**/GP5[13]	8	O	IPU		UART2 transmit data.

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor, IPU = Internal Pullup resistor
(3) As these signals are internally pulled down while the device is in reset, it is necessary to externally pull them high with resistors if UART1 boot mode is used. See the OMAP-L137 Applications Processor Stsyem Reference Guide - Literature Number SPRUG84 for more for details on entering UART1 boot mode.

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2.8.12 Inter-Integrated Circuit Modules(I2C0, I2C1)

Table 2-16. Inter-Integrated Circuit (I2C) Terminal Functions

SIGNAL NAME	PIN NO	TYPE(1)	PULL(2)	MUXED	DESCRIPTION
	PTP				
I2C0					
UART0_RXD/**I2C0_SDA**/TM64P0_IN12/GP5[8]/BOOT[8]	2	I/O	IPU	UART0, Timer0, GPIO, BOOT	I2C0 serial data.
UART0_TXD/**I2C0_SCL**/TM64P0_OUT12/GP5[9]/BOOT[9]	3	I/O	IPU	UART0, Timer0, GPIO, BOOT	I2C0 serial clock.
I2C1					
SPI1_SIMO[0]/**I2C1_SDA**/GP5[6]/BOOT[6]	14	I/O	IPU	SPI1, GPIO, BOOT	I2C1 serial Data.
SPI1_SOMI[0]/**I2C1_SCL**/GP5[5]/BOOT[5]	13	I/O	IPU		I2C1 serial clock.

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor, IPU = Internal Pullup resistor

2.8.13 Timers

Table 2-17. Timers Terminal Functions

SIGNAL NAME	PIN NO	TYPE(1)	PULL(2)	MUXED	DESCRIPTION
	PTP				
TIMER0					
UART0_RXD/I2C0_SDA/**TM64P0_IN12**/GP5[8]/BOOT[8]	2	I	IPU	UART0, I2C0, GPIO, BOOT	Timer0 lower input.
UART0_TXD/I2C0_SCL/**TM64P0_OUT12**/GP5[9]/BOOT[9]	3	O	IPU		Timer0 lower output
TIMER1 (Watchdog)					
No external pins. The Timer1 peripheral pins are not pinned out as external pins.					

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor, IPU = Internal Pullup resistor

2.8.14 Universal Host-Port Interface (UHPI)

Note:

The UHPI module requires 16 data pins for the host port interface to function. Therefore on the PTP, the UHPI is not available.

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Table 2-18. Universal Host-Port Interface (UHPI) Terminal Functions

SIGNAL NAME	PIN NO	TYPE(1)	PULL(2)	MUXED	DESCRIPTION
	PTP				
EMA_D[7]/MMCSD_DAT[7]/**UHPI_HD[7]**/GP0[7]/ BOOT[13]	54	I/O	IPU	EMIFA, MMC/SD, GPIO, BOOT	UHPI data bus.
EMA_D[6]/MMCSD_DAT[6]/**UHPI_HD[6]**/GP0[6]	52	I/O	IPU	EMIFA, MMC/SD, GPIO	
EMA_D[5]/MMCSD_DAT[5]/**UHPI_HD[5]**/GP0[5]	51	I/O	IPU		
EMA_D[4]/MMCSD_DAT[4]/**UHPI_HD[4]**/GP0[4]	49	I/O	IPU		
EMA_D[3]/MMCSD_DAT[3]/**UHPI_HD[3]**/GP0[3]	48	I/O	IPU		
EMA_D[2]/MMCSD_DAT[2]/**UHPI_HD[2]**/GP0[2]	46	I/O	IPU		
EMA_D[1]/MMCSD_DAT[1]/**UHPI_HD[1]**/GP0[1]	45	I/O	IPU		
EMA_D[0]/MMCSD_DAT[0]/**UHPI_HD[0]**/GP0[0]/ BOOT[12]	44	I/O	IPU	EMIFA, MMC/SD, GPIO, BOOT	
EMA_A[2]/MMCSD_CMD/**UHPI_HCNTL1**/GP1[2]	31	I/O	IPU	EMIFA, MMCSD_CMD, GPIO	UHPI access control.
EMA_A[1]/MMCSD_CLK/**UHPI_HCNTL0**/GP1[1]	30	I/O	IPU		
EMA_BA[1]/LCD_D[5]/**UHPI_HHWIL**/GP1[13]	26	I/O	IPU	EMIFA, LCD, GPIO	UHPI half-word identification control.
$\overline{\text{EMA_WE}}$/**UHPI_HR$\overline{\text{W}}$** /AXR0[12]/GP2[3]/BOOT[14]	55	I/O	IPU	EMIFA, McASP, GPIO, BOOT	UHPI read/write.
$\overline{\text{EMA_CS[2]}}$/ **$\overline{\text{UHPI_HCS}}$** /GP2[5]/BOOT[15]	23	I/O	IPU	EMIFA, GPIO, BOOT	UHPI chip select.
$\overline{\text{EMA_OE}}$/ **$\overline{\text{UHPI_HDS1}}$** /AXR0[13]/GP2[7]	22	I/O	IPU	EMIFA, McASP0, GPIO	UHPI data strobe.
EMA_WAIT[0]/ **$\overline{\text{UHPI_HRDY}}$** /GP2[10]	19	I/O	IPU	EMIFA, GPIO	UHPI ready.

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor, IPU = Internal Pullup resistor

2.8.15 Multichannel Audio Serial Ports (McASP0, McASP1, McASP2)

Table 2-19. Multichannel Audio Serial Ports (McASPs) Terminal Functions

SIGNAL NAME	PIN NO	TYPE(1)	PULL(2)	MUXED	DESCRIPTION
	PTP				
McASP0					

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor, IPU = Internal Pullup resistor

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Table 2-19. Multichannel Audio Serial Ports (McASPs) Terminal Functions (continued)

SIGNAL NAME	PIN NO	TYPE(1)	PULL(2)	MUXED	DESCRIPTION
	PTP				
EMA_OE/UHPI_HDS1/**AXR0[13]**/GP2[7]	24	I/O	IPU	EMIFA, UHPI, GPIO	McASP0 serial data.
EMA_WE/UHPI_HRW/**AXR0[12]**/GP2[3]/BOOT[14]	55	I/O	IPU	EMIFA, UHPI, GPIO, BOOT	
AXR0[11]/ AXR2[0]/GP3[11]	124	I/O	IPD	McASP2, GPIO	
AXR0[10]/GP3[10]	123	I/O	IPD	GPIO	
AXR0[9]/GP3[9]	122	I/O	IPD	GPIO	
AXR0[8]/MDIO_D/GP3[8]	121	I/O	IPU	MDIO, GPIO	
AXR0[7]/MDIO_CLK/GP3[7]	120	I/O	IPD		
AXR0[6]/RMII_RXER[0]/ACLKR2/GP3[6]	118	I/O	IPD	EMAC, McASP2, GPIO	
AXR0[5]/RMII_RXD[1]/AFSX2/GP3[5]	117	I/O	IPD		
AXR0[4]/ RMII_RXD[0]/AXR2[1]/GP3[4]	116	I/O	IPD		
AXR0[3]/RMII_CRS_DV/AXR2[2]/GP3[3]	115	I/O	IPD		
AXR0[2]/RMII_TXEN/AXR2[3]/GP3[2]	113	I/O	IPD		
AXR0[1]/RMII_TXD[1]/ACLKX2/GP3[1]	112	I/O	IPD		
AXR0[0]/RMII_TXD[0]/AFSR2/GP3[0]	111	I/O	IPD		
AHCLKX0/AHCLKX2/USB_REFCLKIN/GP2[11]	125	I/O	IPD	McASP2, USB, GPIO	McASP0 transmit master clock.
ACLKX0/ECAP0/APWM0/GP2[12]	126	I/O	IPD	eCAP0, GPIO	McASP0 transmit bit clock.
AFSX0/GP2[13]/BOOT[10]	127	I/O	IPD	GPIO, BOOT	McASP0 transmit frame sync.
AHCLKR0/RMII_MHZ_50_CLK/GP2[14]/BOOT[11]	129	I/O	IPD	EMAC, GPIO, BOOT	McASP0 receive master clock.
ACLKR0/ECAP1/APWM1/GP2[15]	130	I/O	IPD	eCAP1, GPIO	McASP0 receive bit clock.
AFSR0/GP3[12]	131	I/O	IPD	GPIO	McASP0 receive frame sync.
McASP1					
AXR1[11]/GP5[11]	6	I/O	IPU	GPIO	McASP1 serial data.
AXR1[10]/GP5[10]	4	I/O	IPU		
AXR1[8]/EPWM1A/GP4[8]	168	I/O	IPD	eHRPWM1 A, GPIO	
AXR1[7]/EPWM1B/GP4[7]	169	I/O	IPD	eHRPWM1 B, GPIO	
AXR1[6]/EPWM2A/GP4[6]	170	I/O	IPD	eHRPWM2 A, GPIO	
AXR1[5]/EPWM2B/GP4[5]	171	I/O	IPD	eHRPWM2 B, GPIO	
AXR1[4]/EQEP1B/GP4[4]	173	I/O	IPD	eQEP, GPIO	
AXR1[3]/EQEP1A/GP4[3]	174	I/O	IPD		
AXR1[2]/GP4[2]	175	I/O	IPD	GPIO	
AXR1[1]/GP4[1]	176	I/O	IPD		
AXR1[0]/GP4[0]	1	I/O	IPD		
AHCLKX1/EPWM0B/GP3[14]	160	I/O	IPD	eHRPWM0, GPIO	McASP1 transmit master clock.

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Table 2-19. Multichannel Audio Serial Ports (McASPs) Terminal Functions (continued)

SIGNAL NAME	PIN NO	TYPE(1)	PULL(2)	MUXED	DESCRIPTION
	PTP				
ACLKX1/EPWM0A/GP3[15]	162	I/O	IPD	eHRPWM0, GPIO	McASP1 transmit bit clock.
AFSX1/EPWMSYNCI/EPWMSYNCO/GP4[10]	163	I/O	IPD	eHRPWM0, GPIO	McASP1 transmit frame sync.
ACLKR1/ECAP2/APWM2/GP4[12]	165	I/O	IPD	eCAP2, GPIO	McASP1 receive bit clock.
AFSR1/GP4[13]	166	I/O	IPD	GPIO	McASP1 receive frame sync.
AMUTE1/EPWMTZ/GP4[14]	132	O	IPD	eHRPWM0, eHRPWM1, GPIO, eHRPWM2	McASP1 mute output.
McASP2					
AXR0[2]/RMII_TXEN/ **AXR2[3]**/GP3[2]	113	I/O	IPD	McASP0, EMAC, GPIO	McASP2 serial data.
AXR0[3]/RMII_CRS_DV/ **AXR2[2]**/GP3[3]	115	I/O	IPD		
AXR0[4]/RMII_RXD[0]/ **AXR2[1]**/GP3[4]	116	I/O	IPD		
AXR0[11]/**AXR2[0]**/GP3[11]	124	I/O	IPD	McASP0, GPIO	
AHCLKX0/**AHCLKX2**/USB_REFCLKIN/GP2[11]	125	I/O	IPD	McASP0, USB, GPIO	McASP2 transmit master clock.
AXR0[1]/RMII_TXD[1]/ **ACLKX2**/GP3[1]	112	I/O	IPD		McASP2 transmit bit clock.
AXR0[5]/RMII_RXD[1]/ **AFSX2**/GP3[5]	117	I/O	IPD	McASP0, EMAC, GPIO	McASP2 transmit frame sync.
AXR0[6]/RMII_RXER[0]/ **ACLKR2**/GP3[6]	118	I/O	IPD	McASP0, EMAC, GPIO	McASP2 receive bit clock.
$\overline{\text{EMA_CS[3]}}$/**AMUTE2**/GP2[6]	21	O	IPU	EMIFA, GPIO	McASP2 mute output.

2.8.16 Universal Serial Bus Modules (USB0, USB1)

Table 2-20. Universal Serial Bus (USB) Terminal Functions

SIGNAL NAME	PIN NO	TYPE(1)	PULL(2)	DESCRIPTION
	PTP			
USB0 2.0 OTG				
USB0_DM	138	A		USB0 PHY data minus
USB0_DP	137	A		USB0 PHY data plus
USB0_VDDA33	140	PWR		USB0 PHY 3.3-V supply
USB0_VDDA18	135	PWR		USB0 PHY 1.8-V supply input
USB0_VDDA12(3)	134	PWR		USB0 PHY 1.2-V LDO output for bypass cap
AHCLKX0/AHCLKX2/**USB_REFCLKIN**/GP2[11]	125	I	IPD	USB_REFCLKIN. Optional 48 MHz clock input.

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor, IPU = Internal Pullup resistor
(3) Core power supply LDO output for USB PHY. This pin must be connected via a 0.22 -µF capacitor to VSS. When the USB peripheral is not used, the USB_VDDA12 signal should still be connected via a 1-µF capacitor to VSS.

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Table 2-20. Universal Serial Bus (USB) Terminal Functions (continued)

SIGNAL NAME	PIN NO	TYPE(1)	PULL(2)	DESCRIPTION
	PTP			
USB1 1.1 OHCI				
AHCLKX0/AHCLKX2/**USB_REFCLKIN**/GP2[11]	125	I	IPD	USB_REFCLKIN. Optional 48 MHz clock input.

2.8.17 Ethernet Media Access Controller (EMAC)

Table 2-21. Ethernet Media Access Controller (EMAC) Terminal Functions

SIGNAL NAME	PIN NO	TYPE(1)	PULL(2)	MUXED	DESCRIPTION
	PTP				
RMII					
AHCLKR0/**RMII_MHZ_50_CLK**/GP2[14]/BOOT[11]	129	I/O	IPD	McASP0, GPIO, BOOT	EMAC 50-MHz clock input or output.
AXR0[6]/**RMII_RXER[0]**/ACLKR2/GP3[6]	118	I	IPD	McASP0, McASP2, GPIO	EMAC RMII receiver error.
AXR0[5]/**RMII_RXD[1]**/AFSX2/GP3[5]	117	I	IPD		EMAC RMII receive data.
AXR0[4]/**RMII_RXD[0]**/AXR2[1]/GP3[4]	116	I	IPD		
AXR0[3]/**RMII_CRS_DV/**AXR2[2]/GP3[3]	115	I	IPD		EMAC RMII carrier sense data valid.
AXR0[2]/**RMII_TXEN**/AXR2[3]/GP3[2]	113	O	IPD		EMAC RMII transmit enable.
AXR0[1]/**RMII_TXD[1]/**ACLKX2/GP3[1]	112	O	IPD		EMAC RMII trasmit data.
AXR0[0]/**RMII_TXD[0]**/AFSR2/GP3[0]	111	O	IPD		
MDIO					
AXR0[8]/**MDIO_D/**GP3[8]	121	I/O	IPU	McASP0, GPIO	MDIO data clock.
AXR0[7]/**MDIO_CLK**/GP3[7]	120	O	IPD		

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor, IPU = Internal Pullup resistor

2.8.18 Multimedia Card/Secure Digital (MMC/SD)

Table 2-22. Multimedia Card/Secure Digital (MMC/SD) Terminal Functions

SIGNAL NAME	PIN NO	TYPE(1)	PULL(2)	MUXED	DESCRIPTION
	PTP				
EMA_A[1]/**MMCSD_CLK**/UHPI_HCNTL0/GP1[1]	30	O	IPU	EMIFA, UHPI, GPIO	MMCSD_CLK.
EMA_A[2]/**MMCSD_CMD**/UHPI_HCNTL1/GP1[2]	31	I/O	IPU		MMCSD_CMD.

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor, IPU = Internal Pullup resistor

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Table 2-22. Multimedia Card/Secure Digital (MMC/SD) Terminal Functions (continued)

SIGNAL NAME	PIN NO	TYPE[1]	PULL[2]	MUXED	DESCRIPTION
	PTP				
EMA_D[7]/**MMCSD_DAT[7]**/UHPI_HD[7]/GP0[7]/BOOT[13]	54	I/O	IPU	EMIFA, UHPI, GPIO, BOOT	MMC/SD data.
EMA_D[6]/**MMCSD_DAT[6]**/UHPI_HD[6]/GP0[6]	52	I/O	IPU	EMIFA, UHPI, GPIO	
EMA_D[5]/**MMCSD_DAT[5]**/UHPI_HD[5]/GP0[5]	51	I/O	IPU		
EMA_D[4]/**MMCSD_DAT[4]**/UHPI_HD[4]/GP0[4]	49	I/O	IPU		
EMA_D[3]/**MMCSD_DAT[3]**/UHPI_HD[3]/GP0[3]	48	I/O	IPU		
EMA_D[2]/**MMCSD_DAT[2]**/UHPI_HD[2]/GP0[2]	46	I/O	IPU		
EMA_D[1]/**MMCSD_DAT[1]**/UHPI_HD[1]/GP0[1]	45	I/O	IPU		
EMA_D[0]/**MMCSD_DAT[0]**/UHPI_HD[0]/GP0[0]/BOOT[12]	44	I/O	IPU	EMIFA, UHPI, GPIO, BOOT	

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2.8.19 Liquid Crystal Display Controller(LCD)

Table 2-23. Liquid Crystal Display Controller (LCD) Terminal Functions

SIGNAL NAME	PIN NO	TYPE(1)	PULL(2)	MUXED	DESCRIPTION
	PTP				
EMA_A[0]/**LCD_D[7]**/GP1[0]	29	I/O	IPD	EMIFA, GPIO	LCD data bus.
EMA_A[3]/**LCD_D[6]**/GP1[3]	32	I/O	IPD		
EMA_BA[1]/**LCD_D[5]**/UHPI_HHWIL/GP1[13]	26	I/O	IPU	EMIFA, UHPI, GPIO	
EMA_BA[0]/**LCD_D[4]**/GP1[14]	25	I/O	IPU	EMIFA, GPIO	
EMA_A[4]/**LCD_D[3]**/GP1[4]	34	I/O	IPD		
EMA_A[5]/**LCD_D[2]**/GP1[5]	35	I/O	IPD		
EMA_A[6]/**LCD_D[1]**/GP1[6]	36	I/O	IPD		
EMA_A[7]/**LCD_D[0]**/GP1[7]	37	I/O	IPD		
EMA_A[8]/**LCD_PCLK**/GP1[8]	39	O	IPU		LCD pixel clock.
EMA_A[9]/**LCD_HSYNC**/GP1[9]	40	O	IPU		LCD horizontal sync.
EMA_A[10]/**LCD_VSYNC**/GP1[10]	27	O	IPU		LCD vertical sync.
EMA_A[11]/ **$\overline{\text{LCD_AC_ENB_CS}}$** /GP1[11]	41	O	IPU		LCD AC bias enable chip select.
EMA_A[12]/**LCD_MCLK**/GP1[12]	42	O	IPU		LCD memory clock.

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
Note: The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor, IPU = Internal Pullup resistor

2.8.20 Reserved and No-connect

Table 2-24. Reserved and No-connect Terminal Functions

SIGNAL NAME	PIN NO	TYPE(1)	DESCRIPTION
	PTP		
RSV2	133	PWR	Reserved. For proper device operation, this pin **must** be tied directly to CV_{DD}.
NC	139	-	-
NC	136	-	-

(1) PWR = Supply voltage.

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2.8.21 Supply and Ground

Table 2-25. Supply and Ground Terminal Functions

SIGNAL NAME	PIN NO	TYPE(1)	DESCRIPTION
	PTP		
CVDD (Core supply)	10, 20, 28, 38, 50, 56, 61, 67, 69, 77, 93, 104, 114, 147, 154, 159, 161, 167,	PWR	1.2-V core supply voltage pins
DVDD (I/O supply)	5, 15, 24, 33, 43, 47, 53, 58, 65, 71, 75, 81, 87, 90, 99, 109, 119, 128, 151, 158, 164, 172,	PWR	3.3-V I/O supply voltage pins.
VSS (Ground)	177	GND	Ground pins.

(1) PWR = Supply voltage, GND - Ground.

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3 Device Configuration

3.1 Introduction

This device supports a variety of boot modes through an internal DSP ROM bootloader. This device does not support dedicated hardware boot modes; therefore, all boot modes utilize the internal DSP ROM. The input states of the BOOT pins are sampled and latched into the BOOTCFG register, which is part of the system configuration (SYSCFG) module, when device reset is deasserted. Boot mode selection is determined by the values of the BOOT pins.

See *Using the D800K001 Bootloader Application Report* (SPRAB04) for more details on the ROM Boot Loader.

3.2 Boot Modes Supported

The following boot modes are supported:

- NAND Flash boot
  - 8-bit NAND
  - 16-bit NAND
- NOR Flash boot
  - NOR Direct boot
  - NOR Legacy boot
  - NOR AIS boot
- HPI Boot
- I2C0/I2C1 Boot
  - Master boot
  - Slave boot
- SPI0/SPI1 Boot
  - Master boot
  - Slave boot

For more details on the boot mode selection, see *TMS320OMAPL137 Digital Audio System-on-Chip User's Guide* SPRUG83.

3.3 SYSCFG Module

The following system level features of the chip are controlled by the SYSCFG peripheral:

- Readable Device, Die, and Chip Revision ID
- Control of Pin Multiplexing
- Priority of bus accesses different bus masters in the system
- Capture at power on reset the chip BOOT[15:0] pin values and make them available to software
- Special case settings for peripherals:
  - Locking of PLL controller settings
  - Default burst sizes for EDMA3 TC0 and TC1
  - Selection of the source for the eCAP module input capture (including on chip sources)
  - McASP AMUTEIN selection and clearing of AMUTE status for the three McASP peripherals
  - Control of the reference clock source and other side-band signals for both of the integrated USB PHYs
  - Clock source selection for EMIFA and EMIFB
- Selects the source of emulation suspend signal (from either ARM or DSP) from peripherals supporting this function.
- Control of on-chip inter-processor interrupts for signaling between ARM and DSP

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Since the SYSCFG peripheral controls global operation of the device, its registers are protected against erroneous accesses by several mechanisms:

- A special key sequence must be written to KICK0, KICK1 registers before any other registers are writeable.
- Additionally, many registers are accessible only by a host (ARM or DSP) when it is operating in its privileged mode. (ex. from the kernel, but not from user space code).
- On a secure OMAPL137 device, some accesses are further restricted to the DSP running in secure mode. Note that this protection does not apply to OMAPL137 devices that are ordered with the "No Security Option".

Table 3-1. System Configuration (SYSCFG) Module Register Access

Offset	Acronym	Register Description	Access
0x01C1 4000	REVID	Revision Identification Register	—
0x01C14008	DIEIDR0	Device Identification Register 0	—
0x01C1 400C	DIEIDR1	Device Identification Register 1	—
0x01C1 4010	DIEIDR2	Device Identification Register 2	—
0x01C1 4014	DIEIDR3	Device Identification Register 3	—
0x01C1 4018	DEVIDR0	Device Identification Register 0	—
0x01C1 4020	BOOTCFG	Boot Configuration Register	Privileged mode
0x01C1 4038	KICK0R	Kick 0 Register	Privileged mode
0x01C1 403C	KICK1R	Kick 1 Register	Privileged mode
0x01C1 4040	HOST0CFG	Host 0 Configuration Register	—
0x01C1 4044	HOST1CFG	Host 1 Configuration Register	—
0x01C1 40E0	IRAWSTAT	Interrupt Raw Status/Set Register	Privileged mode
0x01C1 40E4	IENSTAT	Interrupt Enable Status/Clear Register	Privileged mode
0x01C1 40E8	IENSET	Interrupt Enable Register	Privileged mode
0x01C1 40EC	IENCLR	Interrupt Enable Clear Register	Privileged mode
0x01C1 40F0	EOI	End of Interrupt Register	Privileged mode
0x01C1 40F4	FLTADDRR	Fault Address Register	Privileged mode
0x01C1 40F8	FLTSTAT	Fault Status Register	—
0x01C1 4110	MSTPRI0	Master Priority 0 Register	Privileged mode
0x01C1 4114	MSTPRI1	Master Priority 1 Register	Privileged mode
0x01C1 4118	MSTPRI2	Master Priority 2 Register	Privileged mode
0x01C1 4120	PINMUX0	Pin Multiplexing Control 0 Register	Privileged mode
0x01C1 4124	PINMUX1	Pin Multiplexing Control 1 Register	Privileged mode
0x01C1 4128	PINMUX2	Pin Multiplexing Control 2 Register	Privileged mode
0x01C1 412C	PINMUX3	Pin Multiplexing Control 3 Register	Privileged mode
0x01C1 4130	PINMUX4	Pin Multiplexing Control 4 Register	Privileged mode
0x01C1 4134	PINMUX5	Pin Multiplexing Control 5 Register	Privileged mode
0x01C1 4138	PINMUX6	Pin Multiplexing Control 6 Register	Privileged mode
0x01C1 413C	PINMUX7	Pin Multiplexing Control 7 Register	Privileged mode
0x01C1 4140	PINMUX8	Pin Multiplexing Control 8 Register	Privileged mode
0x01C1 4144	PINMUX9	Pin Multiplexing Control 9 Register	Privileged mode
0x01C1 4148	PINMUX10	Pin Multiplexing Control 10 Register	Privileged mode
0x01C1 414C	PINMUX11	Pin Multiplexing Control 11 Register	Privileged mode
0x01C1 4150	PINMUX12	Pin Multiplexing Control 12 Register	Privileged mode
0x01C1 4154	PINMUX13	Pin Multiplexing Control 13 Register	Privileged mode
0x01C1 4158	PINMUX14	Pin Multiplexing Control 14 Register	Privileged mode
0x01C1 415C	PINMUX15	Pin Multiplexing Control 15 Register	Privileged mode

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Table 3-1. System Configuration (SYSCFG) Module Register Access (continued)

Offset	Acronym	Register Description	Access
0x01C1 4160	PINMUX16	Pin Multiplexing Control 16 Register	Privileged mode
0x01C1 4164	PINMUX17	Pin Multiplexing Control 17 Register	Privileged mode
0x01C1 4168	PINMUX18	Pin Multiplexing Control 18 Register	Privileged mode
0x01C1 416C	PINMUX19	Pin Multiplexing Control 19 Register	Privileged mode
0x01C1 4170	SUSPSRC Reserved	Suspend Source Register —	Privileged mode —
0x01C1 4174	CHIPSIG	Chip Signal Register	—
0x01C1 4178	CHIPSIG_CLR	Chip Signal Clear Register	—
0x01C1 417C	CFGCHIP0	Chip Configuration 0 Register	Privileged mode
0x01C1 4180	CFGCHIP1	Chip Configuration 1 Register	Privileged mode
0x01C1 4184	CFGCHIP2	Chip Configuration 2 Register	Privileged mode
0x01C1 4188	CFGCHIP3	Chip Configuration 3 Register	Privileged mode
0x01C1 418C	CFGCHIP4	Chip Configuration 4 Register	Privileged mode

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4 Device Operating Conditions

4.1 Absolute Maximum Ratings Over Operating Case Temperature Range (Unless Otherwise Noted) (1)

Supply voltage ranges	Core (CVDD, RTC_CVDD, PLL0_VDDA(2)) (3)	-0.5 V to 1.4 V
	I/O, 1.8V (USB0_VDDA18, USB1_VDDA18) (3)	-0.5 V to 2 V
	I/O, 3.3V (DVDD, USB0_VDDA33, USB1_VDDA33) (3)	-0.5 V to 3.8 V
Input voltage ranges	V_I I/O, 1.2V (OSCIN, RTC_XI)	-0.3 V to CVDD + 0.3V
	V_I I/O, 3.3V (Steady State)	-0.3V to DVDD + 0.3V
	V_I I/O, 3.3V (Transient)	DVDD + 20% up to 20% of Signal Period
	V_I I/O, USB 5V Tolerant Pins: (USB0_DM, USB0_DP, USB0_ID, USB1_DM, USB1_DP)	5.25V(4)
	V_I I/O, USB0 VBUS	5.50V(4)
Output voltage ranges	V_O I/O, 3.3V (Steady State)	-0.5 V to DVDD + 0.3V
	V_O I/O, 3.3V (Transient Overshoot/Undershoot)	20% of DVDD for up to 20% of the signal period
Clamp Current	Input or Output Voltages 0.3V above or below their respective power rails. Limit clamp current that flows through the I/O's internal diode protection cells.	±20mA
Operating Junction Temperature ranges, T_J		-55°C to 175°C
Storage temperature range, T_{stg}		-55°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This pin is an internal LDO output and connected via 0.22 µF capacitor to USB0_VDDA12.
(3) All voltage values are with respect to VSS, PLL0_VSSA, OSCVSS, RTC_VSS
(4) Up to a max of 24 hours.

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4.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
CVDD	Supply voltage, Core (CVDD, RTC_CVDD, PLL0_VDDA , USB0_VDDA12(1))	1.14	1.2	1.32	V
DVDD	Supply voltage, I/O, 1.8V (USB0_VDDA18, USB1_VDDA18)	1.71	1.8	1.89	V
	Supply voltage, I/O, 3.3V (DVDD, USB0_VDDA33, USB1_VDDA33)	3.15	3.3	3.45	V
VSS	Supply ground (VSS, PLL0_VSSA, OSCVSS(2), RTC_VSS(2))	0	0	0	V
V_{IH} (3)	High-level input voltage, I/O, 3.3V	2			V
	High-level input voltage, RTC_XI	0.8*RTC_CVDD			V
	High-level input voltage, OSCIN	0.8*CVDD			
V_{IL} (3)	Low-level input voltage, I/O, 3.3V			0.8	V
	Low-level input voltage, RTC_XI			0.2*RTC_CVDD	V
	Low-level input voltage, OSCIN			0.2*CVDD	
V_{HYS}	Input Hysteresis		160		mV
USB	USB0_VBUS	4.75	5	5.25	V
t_t	Transition time, 10%-90%, All Inputs			10	ns
T_A	Operating ambient temperature range	-55		175	°C
$F_{SYSCLK1,6}$	DSP and ARM Operating Frequency (SYSCLK1,6)	0		300	MHz

(1) This pin is an internal LDO output and connected via 0.22 µF capacitor to VSS.
(2) When an external crystal is used, oscillator ground (OSC_VSS, RTC_VSS) must be kept separate from other grounds and connected directly to the crystal load capacitor ground. These pins are shorted to VSS on the device itself and should not be connected to VSS on the circuit board. If a crystal is not used and the clock input is driven directly, then the oscillator VSS may be connected to board ground.
(3) These I/O specifications do not apply to USB I/Os. USB0 I/Os adhere to USB2.0 specification. USB1 I/Os adhere to USB1.1 specification.

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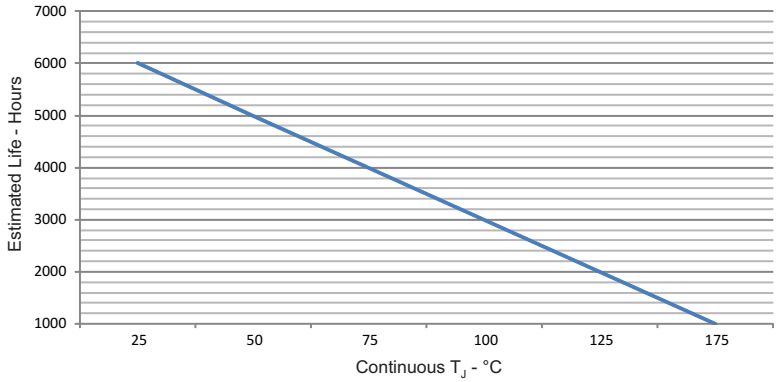
4.3 Electrical Characteristics(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Low/full speed: USB0_DM and USB0_DP		2.8		USB0_VDDA33	V
	High speed: USB0_DM and USB0_DP		360		440	mV
	Low/full speed: USB1_DM and USB1_DP		2.8		USB1_VDDA33	V
	High-level output voltage (3.3V I/O)	DVDD= 3.15V, I_{OH} = -4 mA	2.4			V
		DVDD= 3.15V, I_{OH} = -100 µA	2.95			V
V_{OL}	Low/full speed: USB0_DM and USB0_DP		0.0		0.3	V
	High speed: USB0_DM and USB0_DP		-10		10	mV
	Low/full speed: USB1_DM and USB1_DP		0.0		0.3	V
	Low-level output voltage (3.3V I/O)	DVDD= 3.15V, I_{OL} = 4mA			0.4	V
		DVDD= 3.15V, I_{OL} = +100 µA			0.2	V
I_I (2)	Input current	V_I = VSS to DVDD without opposing internal resistor			±35	µA
		V_I = VSS to DVDD with opposing internal pullup resistor (3)	-30		-200	µA
		V_I = VSS to DVDD with opposing internal pulldown resistor (3)	50		300	µA
		V_I = VSS to USB1_VDDA33 - USB1_DM and USB1_DP			±40	µA
I_{OH}	High-level output current	All peripherals			-4	mA
I_{OL}	Low-level output current	All peripherals			4	mA
I_{OZ} (4)	I/O Off-state output current	VO = VDD or VSS; Internal pull disabled			±35	µA
C_I	Input capacitance	LVCMOS signals		3		pF
		OSCIN		5		
		RTC_XI		2		
C_O	Output capacitance	LVCMOS signals		3		pF

(1) Parameters are characterized over -40°C to 125°C unless otherwise noted.
(2) I_I applies to input-only pins and bi-directional pins. For input-only pins, I_I indicates the input leakage current. For bi-directional pins, I_I indicates the input leakage current and off-state (Hi-Z) output leakage current. Does not apply to USB0 pins. Please see USB2.0 specification.
(3) Applies only to pins with an internal pullup (IPU) or pulldown (IPD) resistor.
(4) I_{OZ} applies to output-only pins, indicating off-state (Hi-Z) output leakage current.



A. See datasheet for absolute maximum and minimum recommended operating conditions.
B. The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

Figure 4-1. OMAPL137 Operating Life Derating Chart at 300 MHz, Core 1.2 V

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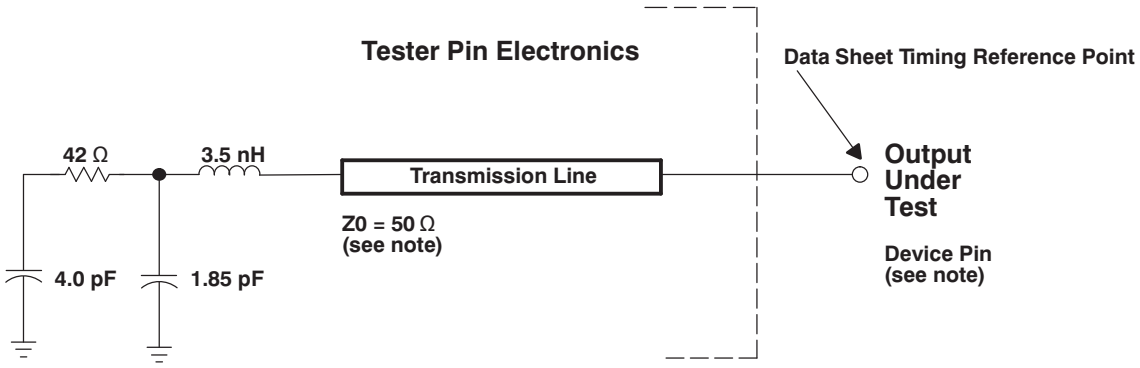
5 Peripheral Information and Electrical Specifications

5.1 Parameter Information

5.1.1 Parameter Information Device-Specific Information



A. The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timings.
Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

Figure 5-1. Test Load Circuit for AC Timing Measurements

The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

5.1.1.1 Signal Transition Levels

All input and output timing parameters are referenced to V_{ref} for both "0" and "1" logic levels. For 3.3 V I/O, V_{ref} = 1.65 V. For 1.8 V I/O, V_{ref} = 0.9 V. For 1.2 V I/O, V_{ref} = 0.6 V."

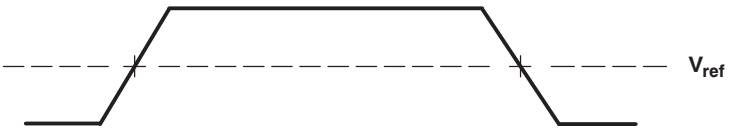


Figure 5-2. Input and Output Voltage Reference Levels for AC Timing Measurements

All rise and fall transition timing parameters are referenced to V_{IL} MAX and V_{IH} MIN for input clocks, V_{OL}MAX and V_{OH} MIN for output clocks.

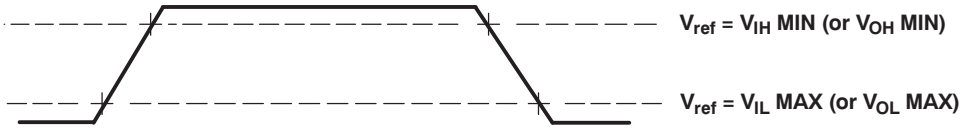


Figure 5-3. Rise and Fall Transition Time Voltage Reference Levels

5.2 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals ***must*** transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

5.3 Power Supplies

5.3.1 Power-on Sequence

OMAPL137 devices include on chip logic that ensures I/O pins are tri-stated during the power on ramp, as long as the RESET pin is asserted. This is true even if the core voltage (CVDD) has not yet ramped.

Normally, the only requirement during the power on ramp is that both the RESET and TRST pins remain asserted (low) until after the power supply rails have fully ramped.

However, if the on chip USB modules are used; then to limit any noise on the USB0_DM, andUSB0_DP, USB1_DM, and USB1_DP pins to less than 200mV during the power on ramp, the sequence illustrated in Figure 5-4 must be followed. The requirement is that the core supply (CVDD) must ramp to at least 0.9V (1) before the IO supply (DVDD) reaches the 1.65V point in its ramp (2). And as is always the case, RESET and TRST must remain asserted during the power on ramp and released only after CVDD and DVDD are within their specified ranges.

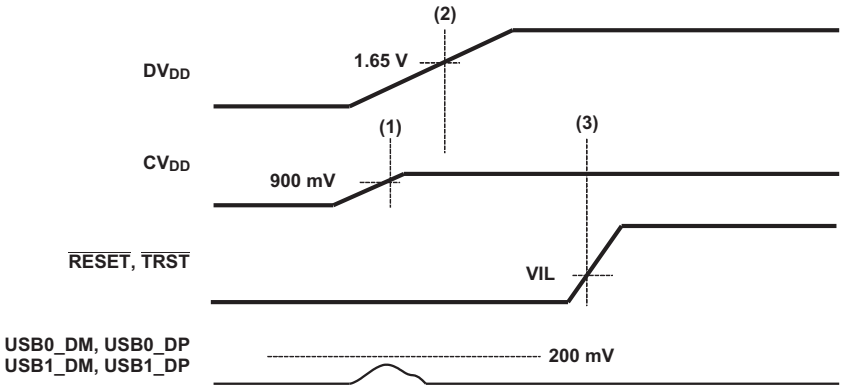


Figure 5-4. Power Sequence

5.3.2 Unused USB0 (USB2.0) and USB1 (USB1.1) Pin Configurations

If one or both USB modules on the device are not used, then some of the power supplies to those modules may not be required. This can eliminate the requirement for a 1.8V power supply to the USB modules. The required pin configurations for unused USB modules are shown below.

Table 5-1. Unused USB0 and USB1 Pin Configurations

SIGNAL NAME	Configuration (When USB0 and USB1 are not used)	Configuration (When USB0 is used and USB1 is not used)
USB0_DM	No connect	Use as USB0 function
USB0_DP	No connect	Use as USB0 function
USB0_VDDA33	No connect	3.3V
USB0_VDDA18	No connect	1.8V
USB0_ID	No connect	Use as USB0 function
USB0_VBUS	No connect	Use as USB0 function
USB0_DRVVBUS/GP4[15]	No connect or use as alternate function	Use as USB0 or alternate function
USB0_VDDA12	No connect	Internal USB0 PHY output connected to an external filter capacitor
USB1_DM	No connect	Ground
USB1_DP	No connect	Ground
USB1_VDDA33	No connect	No connect
USB1_VDDA18	No connect	No connect

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Table 5-1. Unused USB0 and USB1 Pin Configurations (continued)

SIGNAL NAME	Configuration (When USB0 and USB1 are not used)	Configuration (When USB0 is used and USB1 is not used)
AHCLKX0/AHCLKX2/USB_REFCLKIN/ GP2[11]	No connect or use as alternate function	Use as USB0 or alternate function

5.4 Reset

5.4.1 Power-On Reset (POR)

A power-on reset (POR) is required to place the device in a known good state after power-up. Power-On Reset is initiated by bringing $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$ low at the same time. POR sets all of the device internal logic to its default state. All pins are tri-stated with the exception of $\overline{\text{RESETOUT}}$ which remains active through the reset sequence. $\overline{\text{RESETOUT}}$ is an output for use by other controllers in the system that indicates the device is currently in reset.

RTCK is maintained active through a POR.

A summary of the effects of Power-On Reset is given below:

- All internal logic (including emulation logic and the PLL logic) is reset to its default state
- Internal memory is not maintained through a POR
- $\overline{\text{RESETOUT}}$ goes active
- All device pins go to a high-impedance state
- The RTC peripheral is not reset during a POR. A software sequence is required to reset the RTC

CAUTION

A watchdog reset triggers a POR.

5.4.2 Warm Reset

A warm reset provides a limited reset to the device. Warm Reset is initiated by bringing only $\overline{\text{RESET}}$ low ($\overline{\text{TRST}}$ is maintained high through a warm reset). Warm reset sets certain portions of the device to their default state while leaving others unaltered. All pins are tri-stated with the exception of RESETOUT which remains active through the reset sequence. $\overline{\text{RESETOUT}}$ is an output for use by other controllers in the system that indicates the device is currently in reset.

During emulation, the emulator will maintain $\overline{\text{TRST}}$ high and hence only warm reset (not POR) is available during emulation debug and development.

RTCK is maintained active through a POR.

A summary of the effects of Warm Reset is given below:

- All internal logic (except for the emulation logic and the PLL logic) is reset to its default state
- Internal memory is maintained through a warm reset
- $\overline{\text{RESETOUT}}$ goes active
- All device pins go to a high-impedance state
- The RTC peripheral is not reset during a warm reset. A software sequence is required to reset the RTC

5.4.3 Reset Electrical Data Timings

Table 5-2 assumes testing over the recommended operating conditions.

Table 5-2. Reset Timing Requirements (1)(2) (3)

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{w(RSTL)}$	Pulse width, RESET/TRST low	100		ns
2	$t_{su(BPV-RSTH)}$	Setup time, boot pins valid before RESET/TRST high	20		ns
3	$t_{h(RSTH-BPV)}$	Hold time, boot pins valid after RESET/TRST high	20		ns
4	$t_{d(RSTH-RESETOUTH)}$	RESET high to RESETOUT high; Warm reset	4096		cycles (4)
		RESET high to RESETOUT high; Power-on Reset	6192		

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(2) RESETOUT is multiplexed with other pin functions. See the Terminal Functions table, Table 2-5 for details.
(3) For power-on reset (POR), the reset timings in this table refer to RESET and TRST together. For warm reset, the reset timings in this table refer to RESET only (TRST is held high).
(4) OSCIN cycles

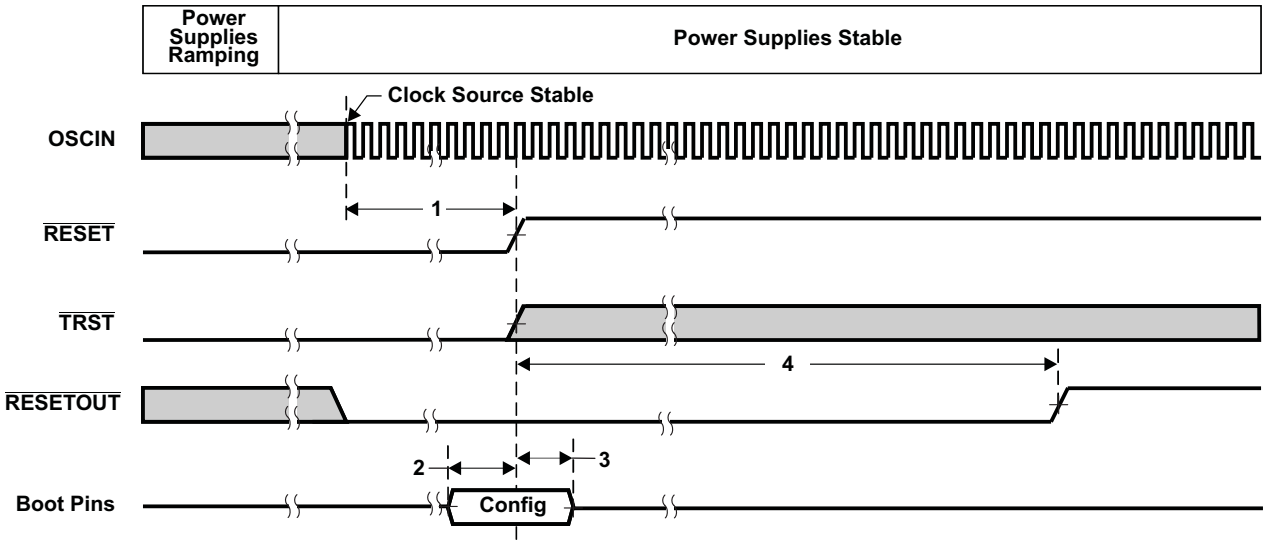

Figure 5-5. Power-On Reset (RESET and TRST active) Timing

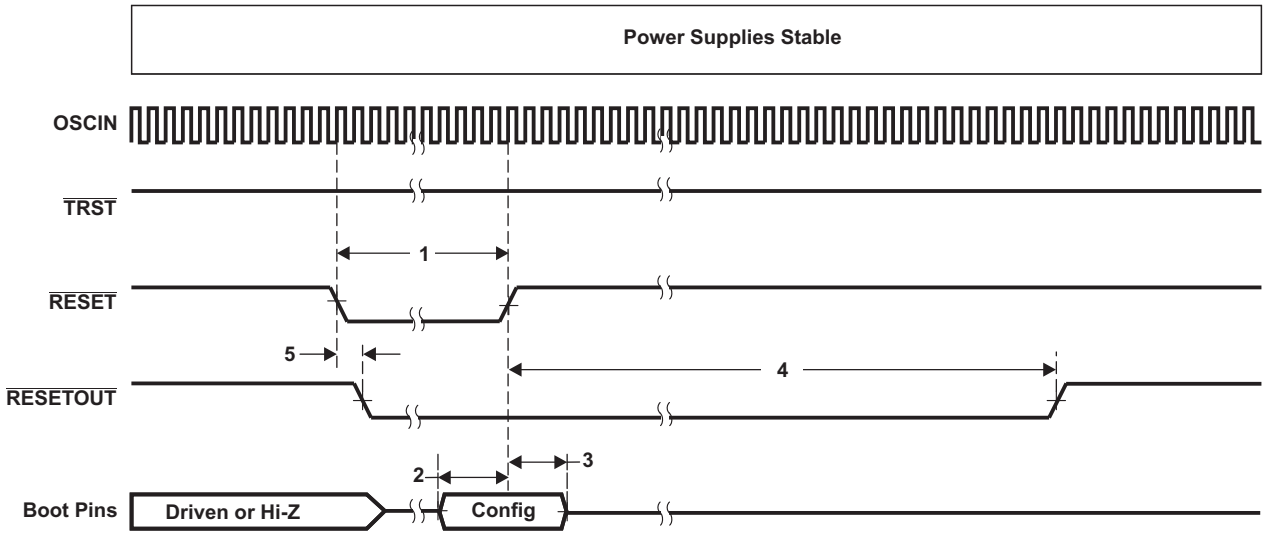

Figure 5-6. Warm Reset (RESET active, TRST high) Timing

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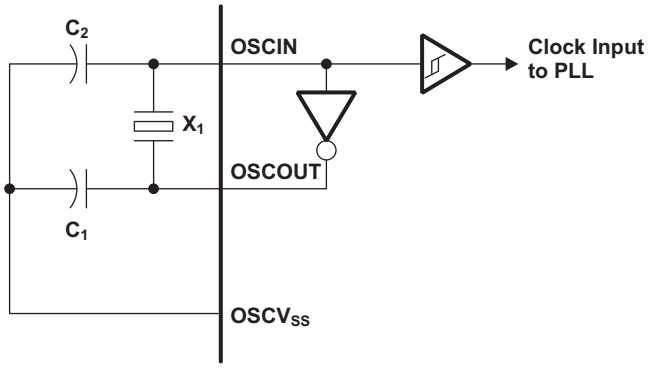
5.5 Crystal Oscillator or External Clock Input

The device includes two choices to provide an external clock input, which is fed to the on-chip PLL to generate high-frequency system clocks. These options are illustrated in Figure 5-7 and Figure 5-8. For input clock frequencies between 12 and 20 MHz, a crystal with 80 ohm max ESR is recommended. For input clock frequencies between 20 and 30 MHz, a crystal with 60 Ω max ESR is recommended. Typical C1, C2 values are 10-20 pF.

The CLKMODE bit in the PLLCTL register must be 0 to use the on-chip oscillator. If CLKMODE is set to 1, the internal oscillator is disabled.

- Figure 5-7 illustrates the option that uses on-chip 1.2V oscillator with external crystal circuit.
- Figure 5-8 illustrates the option that uses an external 1.2V clock input.



The oscillator performance is validated up to 125°C, operating above 125°C is recommended to be driven with an external clock source.

Figure 5-7. On-Chip 1.2V Oscillator

Table 5-3. Oscillator Timing Requirements

NO.	PARAMETER	MIN	MAX	UNIT
f_{osc}	Oscillator frequency range (OSCIN/OSCOUT)	12	30	MHz

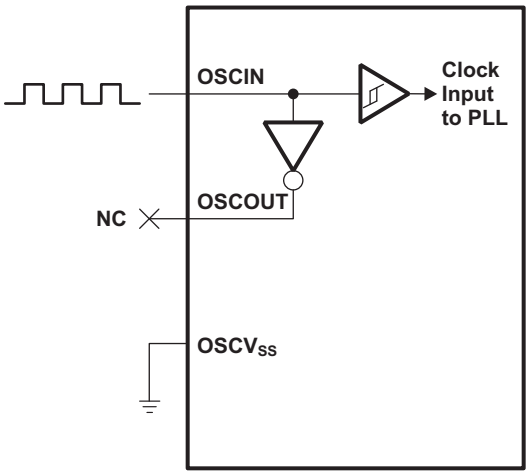


Figure 5-8. External 1.2V Clock Source

Table 5-4. OSCIN Timing Requirements

NO.	PARAMETER	MIN	MAX	UNIT
f_{OSCIN}	OSCIN frequency range (OSCIN)	12	50	MHz
$t_{c(OSCIN)}$	Cycle time, external clock driven on OSCIN	20		ns

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Table 5-4. OSCIN Timing Requirements (continued)

NO.	PARAMETER	MIN	MAX	UNIT
$t_{w(OSCINH)}$	Pulse width high, external clock on OSCIN	0.4 $t_{c(OSCIN)}$		ns
$t_{w(OSCINL)}$	Pulse width low, external clock on OSCIN	0.4 $t_{c(OSCIN)}$		ns
$t_{t(OSCIN)}$	Transition time, OSCIN	5		ns
$t_{j(OSCIN)}$	Period jitter, OSCIN	0.02P		ns

5.6 Clock PLLs

The device has one PLL controller that provides clock to different parts of the system. PLL0 provides clocks (though various dividers) to most of the components of the device.

The PLL controller provides the following:

- Glitch-Free Transitions (on changing clock settings)
- Domain Clocks Alignment
- Clock Gating
- PLL power down

The various clock outputs given by the controller are as follows:

- Domain Clocks: SYSCLK [1:n]
- Auxiliary Clock from reference clock source: AUXCLK

Various dividers that can be used are as follows:

- Post-PLL Divider: POSTDIV
- SYSCLK Divider: D1, ¼, Dn

Various other controls supported are as follows:

- PLL Multiplier Control: PLLM
- Software programmable PLL Bypass: PLLEN

5.6.1 PLL Device-Specific Information

The device DSP generates the high-frequency internal clocks it requires through an on-chip PLL.

The PLL requires some external filtering components to reduce power supply noise as shown in Figure 5-9.

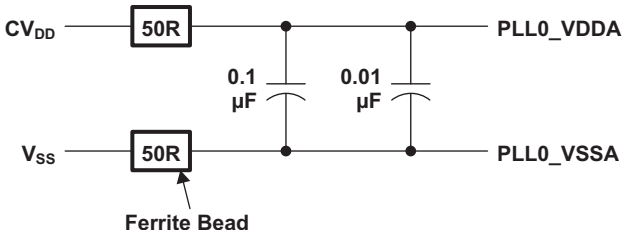

Figure 5-9. PLL External Filtering Components

The input to the PLL is either from the on-chip oscillator (OSCIN pin) or from an external clock on the CLKIN pin. The PLL outputs seven clocks that have programmable divider options. Figure 5-10 illustrates the PLL Topology.

The PLL is disabled by default after a device reset. It must be configured by software according to the allowable operating conditions listed in Table 5-5 before enabling the DSP to run from the PLL by setting PLLEN = 1.

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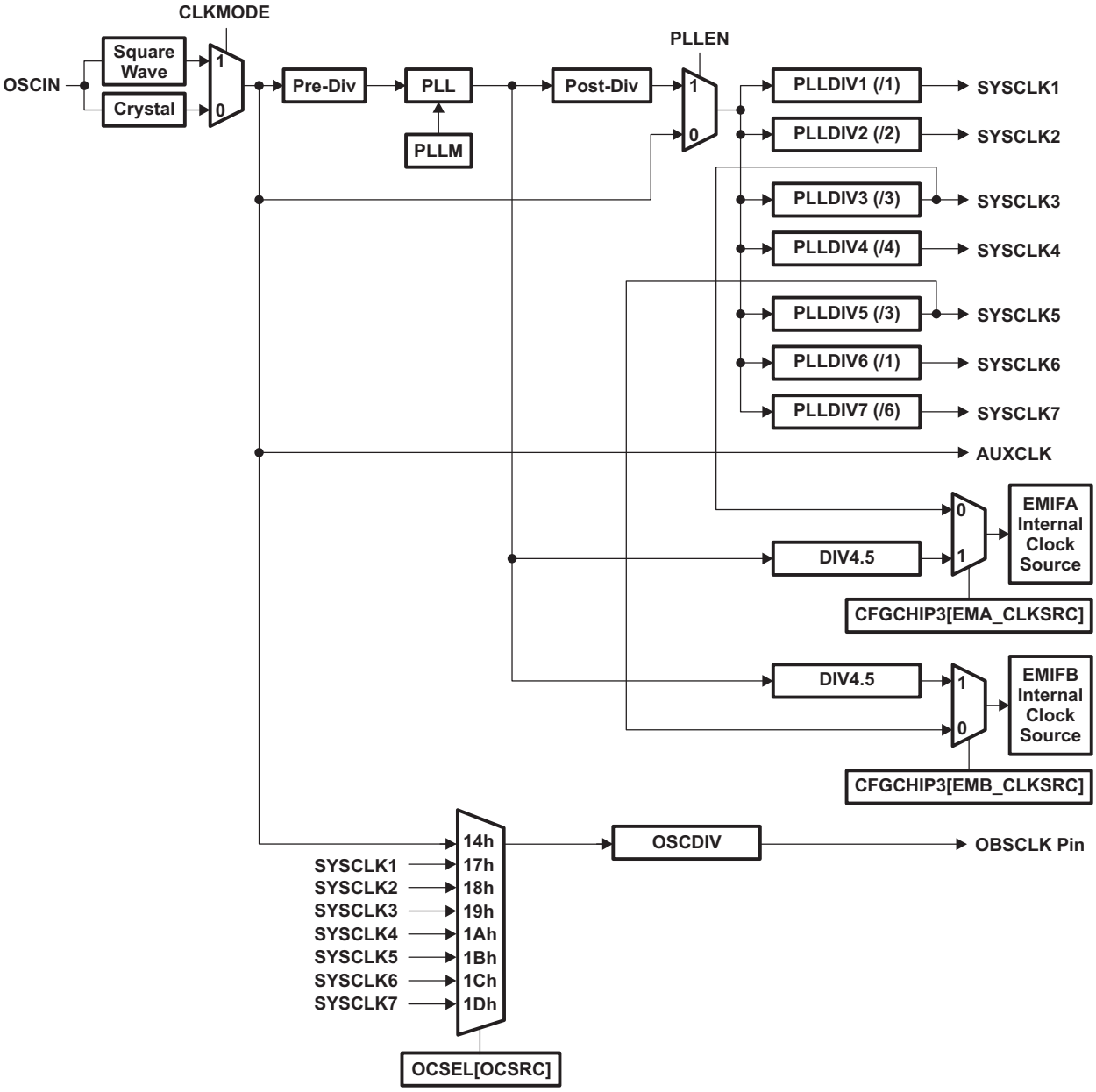

Figure 5-10. PLL Topology

Table 5-5. Allowed PLL Operating Conditions

NO.	PARAMETER	Default Value	MIN	MAX	UNIT
1	PLLRST: Assertion time during initialization	N/A	125	N/A	ns
2	Lock time: The time that the application has to wait for the PLL to acquire locks before setting PLLEN, after changing PREDIV, PLLM, or OSCIN	N/A	N/A	$\frac{2000\ N}{\sqrt{M}}$ where N = Pre-Divider Ratio M = PLL Multiplier (1)	ns
3	PREDIV	/1	/1	/32	ns
4	PLL input frequency (PLLREF)		12	30 (if internal oscillator is used) 50 (if external clock sourcce is used)	MHz
5	PLL multiplier values (PLLM)	x20	x4	x32	
6	PLL output frequency. (PLLOUT)	N/A	400	600 (1)	MHz
7	POSTDIV	/1	/2 (1)	/32	ns

(1) PLL post divider / 2 must be used. The /4.5 clock path can be used to generate an EMIF clock from the undivided (i.e. 600 MHz) PLL output clock.

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5.6.2 Device Clock Generation

PLL0 is controlled by PLL Controller 0. The PLLC0 manages the clock ratios, alignment, and gating for the system clocks to the chip. The PLLC is responsible for controlling all modes of the PLL through software, in terms of pre-division of the clock inputs, multiply factor within the PLL, and post-division for each of the chip-level clocks from the PLL output. The PLLC also controls reset propagation through the chip, clock alignment, and test points.

5.6.3 PLL Controller 0 Registers

Table 5-6. PLL Controller 0 Registers

ADDRESS	ACRONYM	REGISTER DESCRIPTION
0x01C1 1000	REVID	Revision Identification Register
0x01C1 10E4	RSTYPE	Reset Type Status Register
0x01C1 1100	PLLCTL	PLL Control Register
0x01C1 1104	OCSEL	OBSCLK Select Register
0x01C1 1110	PLLM	PLL Multiplier Control Register
0x01C1 1114	PREDIV	PLL Pre-Divider Control Register
0x01C1 1118	PLLDIV1	PLL Controller Divider 1 Register
0x01C1 111C	PLLDIV2	PLL Controller Divider 2 Register
0x01C1 1120	PLLDIV3	PLL Controller Divider 3 Register
0x01C1 1124	OSCDIV	Oscillator Divider 1 Register (OBSCLK)
0x01C1 1128	POSTDIV	PLL Post-Divider Control Register
0x01C1 1138	PLLCMD	PLL Controller Command Register
0x01C1 113C	PLLSTAT	PLL Controller Status Register
0x01C1 1140	ALNCTL	PLL Controller Clock Align Control Register
0x01C1 1144	DCHANGE	PLLDIV Ratio Change Status Register
0x01C1 1148	CKEN	Clock Enable Control Register
0x01C1 114C	CKSTAT	Clock Status Register
0x01C1 1150	SYSTAT	SYSCLK Status Register
0x01C1 1160	PLLDIV4	PLL Controller Divider 4 Register
0x01C1 1164	PLLDIV5	PLL Controller Divider 5 Register
0x01C1 1168	PLLDIV6	PLL Controller Divider 6 Register
0x01C1 116C	PLLDIV7	PLL Controller Divider 7 Register
0x01C1 11F0	EMUCNT0	Emulation Performance Counter 0 Register
0x01C1 11F4	EMUCNT1	Emulation Performance Counter 1 Register

5.7 Interrupts

The device has a large number of interrupts to service the needs of its many peripherals and subsystems. Both the ARM and C674x CPUs are capable of servicing these interrupts equally. The interrupts can be selectively enabled or disabled in either of the controllers. Also, the ARM and DSP can communicate with each other through interrupts controlled by registers in the SYSCFG module.

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5.7.1 ARM CPU Interrupts

The ARM9 CPU core supports 2 direct interrupts: FIQ and IRQ. The ARM Interrupt Controller on the OMAPL137 extends the number of interrupts to 100, and provides features like programmable masking, priority, hardware nesting support, and interrupt vector generation. The OMAPL137 ARM Interrupt controller is enhanced from previous devices like the DM6446 and DM355.

5.7.1.1 ARM Interrupt Controller (AINTC) Interrupt Signal Hierarchy

On OMAPL137, the ARM Interrupt controller organizes interrupts into the following hierarchy:

- Peripheral Interrupt Requests
  - Individual Interrupt Sources from Peripherals
- 100 System Interrupts
  - One or more Peripheral Interrupt Requests are combined (fixed configuration) to generate a System Interrupt.
  - After prioritization, the AINTC will provide an interrupt vector based unique to each System Interrupt
- 32 Interrupt Channels
  - Each System Interrupt is mapped to one of the 32 Interrupt Channels
  - Channel Number determines the first level of prioritization, Channel 0 is highest priority and 31 lowest.
  - If more than one system interrupt is mapped to a channel, priority within the channel is determined by system interrupt number (0 highest priority)
- Host Interrupts (FIQ and IRQ)
  - Interrupt Channels 0 and 1 generate the ARM FIQ interrupt
  - Interrupt Channels 2 through 31 Generate the ARM IRQ interrupt
- Debug Interrupts
  - Two Debug Interrupts are supported and can be used to trigger events in the debug subsystem
  - Sources can be selected from any of the System Interrupts or Host Interrupts

5.7.1.2 AINTC Hardware Vector Generation

The AINTC also generates an interrupt vector in hardware for both IRQ and FIQ host interrupts. This may be used to accelerate interrupt dispatch. A unique vector is generated for each of the 100 system interrupts. The vector is computed in hardware as:

VECTOR = BASE + (SYSTEM INTERRUPT NUMBER × SIZE)

Where BASE and SIZE are programmable. The computed vector is a 32-bit address which may dispatched to using a single instruction of type LDR PC, [PC, #-<offset_12>] at the FIQ and IRQ vector locations (0xFFFF0018 and 0xFFFF001C respectively).

5.7.1.3 AINTC Hardware Interrupt Nesting Support

Interrupt nesting occurs when an interrupt service routine re-enables interrupts, to allow the CPU to interrupt the ISR if a higher priority event occurs. The AINTC provides hardware support to facilitate interrupt nesting. It supports both global and per host interrupt (FIQ and IRQ in this case) automatic nesting. If enabled, the AINTC will automatically update an internal nesting register that temporarily masks interrupts at and below the priority of the current interrupt channel. Then if the ISR re-enables interrupts; only higher priority channels will be able to interrupt it. The nesting level is restored by the ISR by writing to the nesting level register on completion. Support for nesting can be enabled/disabled by software, with the option of automatic nesting on a global or per host interrupt basis; or manual nesting.

5.7.1.4 AINTC System Interrupt Assignments on OMAPL137

System Interrupt assignments for the OMAPL137 are listed in Table 5-7

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Table 5-7. AINTC System Interrupt Assignments

System Interrupt	Interrupt Name	Source	System Interrupt	Interrupt Name	Source
0	COMMTX	ARM	51	IIC1_INT	I2C1
1	COMMRX	ARM	52	LCDC_INT	LCD Controller
2	NINT	ARM	53	UART_INT1	UART1
3	PRU_EVTOUT0	PRU Interrupt	54	MCASP_INT	McASP0, 1, 2 Combined RX / TX Interrupts
4	PRU_EVTOUT1	PRU Interrupt	55	PSC1_ALLINT	PSC1
5	PRU_EVTOUT2	PRU Interrupt	56	SPI1_INT	SPI1
6	PRU_EVTOUT3	PRU Interrupt	57	UHPI_ARMINT	UHPI Arm Interrupt
7	PRU_EVTOUT4	PRU Interrupt	58	USB0_INT	USB0 Interrupt
8	PRU_EVTOUT5	PRU Interrupt	59	USB1_HCINT	USB1 OHCI Host Controller Interrupt
9	PRU_EVTOUT6	PRU Interrupt	60	USB1_RWAKEUP	USB1 Remote Wakeup Interrupt
10	PRU_EVTOUT7	PRU Interrupt	61	UART2_INT	UART2
11	EDMA3_CC0_CCINT	EDMA CC Region 0	62	-	Reserved
12	EDMA3_CC0_CCERRINT	EDMA CC	63	EHRPWM0	HiResTimer / PWM0 Interrupt
13	EDMA3_TC0_TCERRINT	EDMA TC0	64	EHRPWM0TZ	HiResTimer / PWM0 Trip Zone Interrupt
14	EMIFA_INT	EMIFA	65	EHRPWM1	HiResTimer / PWM1 Interrupt
15	IIC0_INT	I2C0	66	EHRPWM1TZ	HiResTimer / PWM1 Trip Zone Interrupt
16	MMCSD_INT0	MMCSD	67	EHRPWM2	HiResTimer / PWM2 Interrupt
17	MMCSD_INT1	MMCSD	68	EHRPWM2TZ	HiResTimer / PWM2 Trip Zone Interrupt
18	PSC0_ALLINT	PSC0	69	ECAP0	ECAP0
19	RTC_IRQS[1:0]	RTC	70	ECAP1	ECAP1
20	SPI0_INT	SPI0	71	ECAP2	ECAP2
21	T64P0_TINT12	Timer64P0 Interrupt 12	72	EQEP0	EQEP0
22	T64P0_TINT34	Timer64P0 Interrupt 34	73	EQEP1	EQEP1
23	T64P1_TINT12	Timer64P1 Interrupt 12	74	T64P0_CMPINT0	Timer64P0 - Compare 0
24	T64P1_TINT34	Timer64P1 Interrupt 34	75	T64P0_CMPINT1	Timer64P0 - Compare 1
25	UART0_INT	UART0	76	T64P0_CMPINT2	Timer64P0 - Compare 2
26	-	Reserved	77	T64P0_CMPINT3	Timer64P0 - Compare 3
27	PROTERR	MPU1, 2, and SYSCFG Protection Shared Interrupt	78	T64P0_CMPINT4	Timer64P0 - Compare 4
28	SYSCFG_CHIPINT0	SYSCFG CHIPSIG Register	79	T64P0_CMPINT5	Timer64P0 - Compare 5
29	SYSCFG_CHIPINT1	SYSCFG CHIPSIG Register	80	T64P0_CMPINT6	Timer64P0 - Compare 6
30	SYSCFG_CHIPINT2	SYSCFG CHIPSIG Register	81	T64P0_CMPINT7	Timer64P0 - Compare 7
31	SYSCFG_CHIPINT3	SYSCFG CHIPSIG Register	82	T64P1_CMPINT0	Timer64P1 - Compare 0
32	EDMA3_TC1_TCERRINT	EDMA TC1	83	T64P1_CMPINT1	Timer64P1 - Compare 1
33	EMAC_C0RXTHRESH	EMAC - Core 0 Receive Threshold Interrupt	84	T64P1_CMPINT2	Timer64P1 - Compare 2
34	EMAC_C0RX	EMAC - Core 0 Receive Interrupt	85	T64P1_CMPINT3	Timer64P1 - Compare 3

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Table 5-7. AINTC System Interrupt Assignments (continued)

System Interrupt	Interrupt Name	Source	System Interrupt	Interrupt Name	Source
35	EMAC_C0TX	EMAC - Core 0 Transmit Interrupt	86	T64P1_CMPINT4	Timer64P1 - Compare 4
36	EMAC_C0MISC	EMAC - Core 0 Miscellaneous Interrupt	87	T64P1_CMPINT5	Timer64P1 - Compare 5
37	EMAC_C1RXTHRESH	EMAC - Core 1 Receive Threshold Interrupt	88	T64P1_CMPINT6	Timer64P1 - Compare 6
38	EMAC_C1RX	EMAC - Core 1 Receive Interrupt	89	T64P1_CMPINT7	Timer64P1 - Compare 7
39	EMAC_C1TX	EMAC - Core 1 Transmit Interrupt	90	ARMCLKSTOPREQ	PSC0
40	EMAC_C1MISC	EMAC - Core 1 Miscellaneous Interrupt	91	-	Reserved
41	EMIF_MEMERR	EMIFB	92	-	Reserved
42	GPIO_B0INT	GPIO Bank 0 Interrupt	93	-	Reserved
43	GPIO_B1INT	GPIO Bank 1 Interrupt	94	-	Reserved
44	GPIO_B2INT	GPIO Bank 2 Interrupt	95	-	Reserved
45	GPIO_B3INT	GPIO Bank 3 Interrupt	96	-	Reserved
46	GPIO_B4INT	GPIO Bank 4 Interrupt	97	-	Reserved
47	GPIO_B5INT	GPIO Bank 5 Interrupt	98	-	Reserved
48	GPIO_B6INT	GPIO Bank 6 Interrupt	99	-	Reserved
49	GPIO_B7INT	GPIO Bank 7 Interrupt	100	-	Reserved
50	-	Reserved			

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5.7.1.5 AINTC Memory Map

Table 5-8. AINTC Memory Map

BYTE ADDRESS	REGISTER NAME	DESCRIPTION
0xFFFE E000	REV	Revision Register
0xFFFE E004	CR	Control Register
0xFFFE E008 - 0xFFFE E00F	-	Reserved
0xFFFE E010	GER	Global Enable Register
0xFFFE E014 - 0xFFFE E01B	-	Reserved
0xFFFE E01C	GNLR	Global Nesting Level Register
0xFFFE E020	SISR	System Interrupt Status Indexed Set Register
0xFFFE E024	SICR	System Interrupt Status Indexed Clear Register
0xFFFE E028	EISR	System Interrupt Enable Indexed Set Register
0xFFFE E02C	EICR	System Interrupt Enable Indexed Clear Register
0xFFFE E030	-	Reserved
0xFFFE E034	HIEISR	Host Interrupt Enable Indexed Set Register
0xFFFE E038	HIDISR	Host Interrupt Enable Indexed Clear Register
0xFFFE E03C - 0xFFFE E04F	-	Reserved
0xFFFE E050	VBR	Vector Base Register
0xFFFE E054	VSR	Vector Size Register
0xFFFE E058	VNR	Vector Null Register
0xFFFE E05C - 0xFFFE E07F	-	Reserved
0xFFFE E080	GPIR	Global Prioritized Index Register
0xFFFE E084	GPVR	Global Prioritized Vector Register
0xFFFE E088 - 0xFFFE E1FF	-	Reserved
0xFFFE E200 - 0xFFFE E20F	SRSR[1] - SRSR[3]	System Interrupt Status Raw / Set Registers
0xFFFE E20C - 0xFFFE E27F	-	Reserved
0xFFFE E280 - 0xFFFE E28B	SECR[1] - SECR[3]	System Interrupt Status Enabled / Clear Registers
0xFFFE E28C - 0xFFFE E2FF	-	Reserved
0xFFFE E300 - 0xFFFE E30B	ESR[1] - ESR[3]	System Interrupt Enable Set Registers
0xFFFE E30C - 0xFFFE E37F	-	Reserved
0xFFFE E380 - 0xFFFE E38B	ECR[1] - ECR[3]	System Interrupt Enable Clear Registers
0xFFFE E38C - 0xFFFE E3FF	-	Reserved
0xFFFE E400 - 0xFFFE E458	CMR[0] - CMR[22]	Channel Map Registers (Byte Wide Registers)
0xFFFE E459 - 0xFFFE E7FF	-	Reserved
0xFFFE E800 - 0xFFFE E81F	-	Reserved
0xFFFE E820 - 0xFFFE E8FF	-	Reserved
0xFFFE E900 - 0xFFFE E904	HIPIR[1] - HIPIR[2]	Host Interrupt Prioritized Index Registers
0xFFFE E908 - 0xFFFE EEFF	-	Reserved
0xFFFE EF00 - 0xFFFE EF04	-	Reserved
0xFFFE EF08 - 0xFFFE F0FF	-	Reserved
0xFFFE F100 - 0xFFFE F104	HINLR[1] - HINLR[2]	Host Interrupt Nesting Level Registers
0xFFFE F108 - 0xFFFE F4FF	-	Reserved
0xFFFE F500	HIER	Host Interrupt Enable Register
0xFFFE F504 - 0xFFFE F5FF	-	Reserved
0xFFFE F600	HIPVR[1] - HIPVR[2]	Host Interrupt Prioritized Vector Registers
0xFFFE F608 - 0xFFFE FFFF	-	Reserved

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5.7.2 DSP Interrupts

The C674x DSP interrupt controller combines device events into 12 prioritized interrupts. The source for each of the 12 CPU interrupts is user programmable and is listed in Table 5-9. Also, the interrupt controller controls the generation of the CPU exception, NMI, and emulation interrupts. Table 5-10 summarizes the C674x interrupt controller registers and memory locations. For more details on DSP interrupt control, see the TMS320C64x+ DSP Megamodule Reference Guide, Literature Number - SPRU871.

Table 5-9. OMAPL137 DSP Interrupts

EVT#	Interrupt Name	Source	EVT#	Interrupt Name	Source
0	EVT0	C674x Int Ctl 0	64	T64P0_TINT34	Timer64P0 Interrupt 34
1	EVT1	C674x Int Ctl 1	65	GPIO_B0INT	GPIO Bank 0 Interrupt
2	EVT2	C674x Int Ctl 2	66	PRU_EVTOUT4	PRU Interrupt
3	EVT3	C674x Int Ctl 3	67	SYSCFG_CHIPINT3	SYSCFG_CHIPSIG Register
4	T64P0_TINT12	Timer64P0 - TINT12	68	EQEP0	EQEP0
5	SYSCFG_CHIPINT2	SYSCFG _CHIPSIG Register	69	UART2_INT	UART2
6	PRU_EVTOUT0	PRU Interrupt	70	PSC0_ALLINT	PSC0
7	EHRPWM0	HiResTimer/PWM0 Interrupt	71	PSC1_ALLINT	PSC1
8	EDMA3_CC0_INT1	EDMA3 CC0 Region 1 interrupt	72	GPIO_B7INT	GPIO Bank 7 Interrupt
9	EMU-DTDMA	C674x-ECM	73	LCDC_INT -	LCD ControllerReserved
10	EHRPWM0TZ	HiResTimer/PWM0 Trip Zone Interrupt	74	PROTERR	MPU1, 2, SYSCFG Protection Shared Interrupt
11	EMU-RTDXRX	C674x-RTDX	75	-	Reserved
12	EMU-RTDXTX	C674x-RTDX	76	-	Reserved
13	IDMAINT0	C674x-EMC	77	-	Reserved
14	IDMAINT1	C674x-EMC	78	T64P0_CMPINT0	Timer64P0 - Compare 0
15	MMCSD_INT0	MMCSD MMC/SD Interrupt	79	T64P0_CMPINT1	Timer64P0 - Compare 1
16	MMCSD_INT1	MMCSD SDIO Interrupt	80	T64P0_CMPINT2	Timer64P0 - Compare 2
17	PRU_EVTOUT1	PRU Interrupt	81	T64P0_CMPINT3	Timer64P0 - Compare 3
18	EHRPWM1	HiResTimer/PWM1 Interrupt	82	T64P0_CMPINT4	Timer64P0 - Compare 4
19	USB0_INT	USB0 Interrupt	83	T64P0_CMPINT5	Timer64P0 - Compare 5
20	USB1_HCINT -	USB1 OHCI Host Controller Interrupt Reserved	84	T64P0_CMPINT6	Timer64P0 - Compare 6
21	USB1_RWAKEUP -	USB1 Remote Wakeup Interrupt Reserved	85	T64P0_CMPINT7	Timer64P0 - Compare 7
22	PRU_EVTOUT2	PRU Interrupt	86	T64P1_CMPINT0	Timer64P1 - Compare 0
23	EHRPWM1TZ	HiResTimer/PWM1 Trip Zone Interrupt	87	T64P1_CMPINT1	Timer64P1 - Compare 1
24	EHRPWM2	HiResTimer/PWM2 Interrupt	88	T64P1_CMPINT2	Timer64P1 - Compare 2
25	EHRPWM2TZ	HiResTimer/PWM2 Trip Zone Interrupt	89	T64P1_CMPINT3	Timer64P1 - Compare 3
26	EMAC_C0RXTHRESH -	EMAC - Core 0 Receive Threshold Interrupt Reserved	90	T64P1_CMPINT4	Timer64P1 - Compare 4
27	EMAC_C0RX -	EMAC - Core 0 Receive Interrupt Reserved	91	T64P1_CMPINT5	Timer64P1 - Compare 5
28	EMAC_C0TX -	EMAC - Core 0 Transmit Interrupt Reserved	92	T64P1_CMPINT6	Timer64P1 - Compare 6
29	EMAC_C0MISC -	EMAC - Core 0 Miscellaneous Interrupt Reserved	93	T64P1_CMPINT7	Timer64P1 - Compare 7
30	EMAC_C1RXTHRESH -	EMAC - Core 1 Receive Threshold Interrupt Reserved	94	-	Reserved
31	EMAC_C1RX -	EMAC - Core 1 Receive Interrupt Reserved	95	-	Reserved

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Table 5-9. OMAPL137 DSP Interrupts (continued)

EVT#	Interrupt Name	Source	EVT#	Interrupt Name	Source
32	EMAC_C1TX -	EMAC - Core 1 Transmit Interrupt Reserved	96	INTERR	C674x-Int Ctl
33	EMAC_C1MISC -	EMAC - Core 1 Miscellaneous Interrupt Reserved	97	EMC_IDMAERR	C674x-EMC
34	UHPI_DSPINT	UHPI DSP Interrupt	98	-	Reserved
35	PRU_EVTOUT3	PRU Interrupt	99	-	Reserved
36	IIC0_INT	I2C0	100	-	Reserved
37	SP0_INT	SPI0	101	-	Reserved
38	UART0_INT	UART0	102	-	Reserved
39	PRU_EVTOUT5	PRU Interrupt	103	-	Reserved
40	T64P1_TINT12	Timer64P1 Interrupt 12	104	-	Reserved
41	GPIO_B1INT	GPIO Bank 1 Interrupt	105	-	Reserved
42	IIC1_INT	I2C1	106	-	Reserved
43	SPI1_INT	SPI1	107	-	Reserved
44	PRU_EVTOUT6	PRU Interrupt	108	-	Reserved
45	ECAP0	ECAP0	109	-	Reserved
46	UART_INT1	UART1	110	-	Reserved
47	ECAP1	ECAP1	111	-	Reserved
48	T64P1_TINT34	Timer64P1 Interrupt 34	112	-	Reserved
49	GPIO_B2INT	GPIO Bank 2 Interrupt	113	PMC_ED	C674x-PMC
50	PRU_EVTOUT7	PRU Interrupt	114	-	Reserved
51	ECAP2	ECAP2	115	-	Reserved
52	GPIO_B3INT	GPIO Bank 3 Interrupt	116	UMC_ED1	C674x-UMC
53	EQEP1	EQEP1	117	UMC_ED2	C674x-UMC
54	GPIO_B4INT	GPIO Bank 4 Interrupt	118	PDC_INT	C674x-PDC
55	EMIFA_INT	EMIFA	119	SYS_CMPA	C674x-SYS
56	EDMA3_CC0_ERRINT	EDMA3 Channel Controller 0	120	PMC_CMPA	C674x-PMC
57	EDMA3_TC0_ERRINT	EDMA3 Transfer Controller 0	121	PMC_CMPA	C674x-PMC
58	EDMA3_TC1_ERRINT	EDMA3 Transfer Controller 1	122	DMC_CMPA	C674x-DMC
59	GPIO_B5INT	GPIO Bank 5 Interrupt	123	DMC_CMPA	C674x-DMC
60	EMIFB_INT	EMIFB Memory Error Interrupt	124	UMC_CMPA	C674x-UMC
61	MCASP_INT	McASP0,1,2 Combined RX/TX Interrupts	125	UMC_CMPA	C674x-UMC
62	GPIO_B6INT	GPIO Bank 6 Interrupt	126	EMC_CMPA	C674x-EMC
63	RTC_IRQS	RTC Combined	127	EMC_BUSERR	C674x-EMC

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Table 5-10. C674x DSP Interrupt Controller Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION
0x0180 0000	EVTFLAG0	Event flag register 0
0x0180 0004	EVTFLAG1	Event flag register 1
0x0180 0008	EVTFLAG2	Event flag register 2
0x0180 000C	EVTFLAG3	Event flag register 3
0x0180 0020	EVTSET0	Event set register 0
0x0180 0024	EVTSET1	Event set register 1
0x0180 0028	EVTSET2	Event set register 2
0x0180 002C	EVTSET3	Event set register 3
0x0180 0040	EVTCLR0	Event clear register 0
0x0180 0044	EVTCLR1	Event clear register 1
0x0180 0048	EVTCLR2	Event clear register 2
0x0180 004C	EVTCLR3	Event clear register 3
0x0180 0080	EVTMASK0	Event mask register 0
0x0180 0084	EVTMASK1	Event mask register 1
0x0180 0088	EVTMASK2	Event mask register 2
0x0180 008C	EVTMASK3	Event mask register 3
0x0180 00A0	MEVTFLAG0	Masked event flag register 0
0x0180 00A4	MEVTFLAG1	Masked event flag register 1
0x0180 00A8	MEVTFLAG2	Masked event flag register 2
0x0180 00AC	MEVTFLAG3	Masked event flag register 3
0x0180 00C0	EXPMASK0	Exception mask register 0
0x0180 00C4	EXPMASK1	Exception mask register 1
0x0180 00C8	EXPMASK2	Exception mask register 2
0x0180 00CC	EXPMASK3	Exception mask register 3
0x0180 00E0	MEXPFLAG0	Masked exception flag register 0
0x0180 00E4	MEXPFLAG1	Masked exception flag register 1
0x0180 00E8	MEXPFLAG2	Masked exception flag register 2
0x0180 00EC	MEXPFLAG3	Masked exception flag register 3
0x0180 0104	INTMUX1	Interrupt mux register 1
0x0180 0108	INTMUX2	Interrupt mux register 2
0x0180 010C	INTMUX3	Interrupt mux register 3
0x0180 0140 - 0x0180 0144	-	Reserved
0x0180 0180	INTXSTAT	Interrupt exception status
0x0180 0184	INTXCLR	Interrupt exception clear
0x0180 0188	INTDMASK	Dropped interrupt mask register
0x0180 01C0	EVTASRT	Event assert register

5.7.3 ARM/DSP Communications Interrupts

Communications Interrupts between the ARM and DSP are part of the SYSCFG module on the OMAPL137 family of devices.

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5.8 General-Purpose Input/Output (GPIO)

The GPIO peripheral provides general-purpose pins that can be configured as either inputs or outputs. When configured as an output, a write to an internal register can control the state driven on the output pin. When configured as an input, the state of the input is detectable by reading the state of an internal register. In addition, the GPIO peripheral can produce CPU interrupts and EDMA events in different interrupt/event generation modes. The GPIO peripheral provides generic connections to external devices. The GPIO pins are grouped into banks of 16 pins per bank (i.e., bank 0 consists of GPIO [0:15]).

The device GPIO peripheral supports the following:

- Up to 109 Pins on PTP package configurable as GPIO
- External Interrupt and DMA request Capability
  - Every GPIO pin may be configured to generate an interrupt request on detection of rising and/or falling edges on the pin.
  - The interrupt requests within each bank are combined (logical or) to create eight unique bank level interrupt requests.
  - The bank level interrupt service routine may poll the INTSTATx register for its bank to determine which pin(s) have triggered the interrupt.
  - GPIO Banks 0, 1, 2, 3, 4, 5, 6, and 7 Interrupts assigned to ARM INTC Interrupt Requests 42, 43, 44, 45, 46, 47, 48, and 49 respectively
  - GPIO Banks 0, 1, 2, 3, 4, 5, 6, and 7 Interrupts assigned to DSP Events 65, 41, 49, 52, 54, 59, 62 and 72 respectively
  - Additionally, GPIO Banks 0, 1, 2, 3, 4, and 5 Interrupts assigned to EDMA events 6, 7, 22, 23, 28, and 29 respectively.
- Set/clear functionality: Firmware writes 1 to corresponding bit position(s) to set or to clear GPIO signal(s). This allows multiple firmware processes to toggle GPIO output signals without critical section protection (disable interrupts, program GPIO, re-enable interrupts, to prevent context switching to anther process during GPIO programming).
- Separate Input/Output registers
- Output register in addition to set/clear so that, if preferred by firmware, some GPIO output signals can be toggled by direct write to the output register(s).
- Output register, when read, reflects output drive status. This, in addition to the input register reflecting pin status and open-drain I/O cell, allows wired logic be implemented.

The memory map for the GPIO registers is shown in Table 5-11. See the *TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.* – Literature Number SPRUFK9 for more details.

5.8.1 GPIO Register Description(s)

Table 5-11. GPIO Registers

GPIO BYTE ADDRESS	Acronym	Register Description
0x01E2 6000	REV	Peripheral Revision Register
0x01E2 6004	-	Reserved
0x01E2 6008	BINTEN	GPIO Interrupt Per-Bank Enable Register
GPIO Banks 0 and 1		
0x01E2 6010	DIR01	GPIO Banks 0 and 1 Direction Register
0x01E2 6014	OUT_DATA01	GPIO Banks 0 and 1 Output Data Register
0x01E2 6018	SET_DATA01	GPIO Banks 0 and 1 Set Data Register
0x01E2 601C	CLR_DATA01	GPIO Banks 0 and 1 Clear Data Register
0x01E2 6020	IN_DATA01	GPIO Banks 0 and 1 Input Data Register
0x01E2 6024	SET_RIS_TRIG01	GPIO Banks 0 and 1 Set Rising Edge Interrupt Register
0x01E2 6028	CLR_RIS_TRIG01	GPIO Banks 0 and 1 Clear Rising Edge Interrupt Register

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Table 5-11. GPIO Registers (continued)

GPIO BYTE ADDRESS	Acronym	Register Description
0x01E2 602C	SET_FAL_TRIG01	GPIO Banks 0 and 1 Set Falling Edge Interrupt Register
0x01E2 6030	CLR_FAL_TRIG01	GPIO Banks 0 and 1 Clear Falling Edge Interrupt Register
0x01E2 6034	INTSTAT01	GPIO Banks 0 and 1 Interrupt Status Register
GPIO Banks 2 and 3		
0x01E2 6038	DIR23	GPIO Banks 2 and 3 Direction Register
0x01E2 603C	OUT_DATA23	GPIO Banks 2 and 3 Output Data Register
0x01E2 6040	SET_DATA23	GPIO Banks 2 and 3 Set Data Register
0x01E2 6044	CLR_DATA23	GPIO Banks 2 and 3 Clear Data Register
0x01E2 6048	IN_DATA23	GPIO Banks 2 and 3 Input Data Register
0x01E2 604C	SET_RIS_TRIG23	GPIO Banks 2 and 3 Set Rising Edge Interrupt Register
0x01E2 6050	CLR_RIS_TRIG23	GPIO Banks 2 and 3 Clear Rising Edge Interrupt Register
0x01E2 6054	SET_FAL_TRIG23	GPIO Banks 2 and 3 Set Falling Edge Interrupt Register
0x01E2 6058	CLR_FAL_TRIG23	GPIO Banks 2 and 3 Clear Falling Edge Interrupt Register
0x01E2 605C	INTSTAT23	GPIO Banks 2 and 3 Interrupt Status Register
GPIO Banks 4 and 5		
0x01E2 6060	DIR45	GPIO Banks 4 and 5 Direction Register
0x01E2 6064	OUT_DATA45	GPIO Banks 4 and 5 Output Data Register
0x01E2 6068	SET_DATA45	GPIO Banks 4 and 5 Set Data Register
0x01E2 606C	CLR_DATA45	GPIO Banks 4 and 5 Clear Data Register
0x01E2 6070	IN_DATA45	GPIO Banks 4 and 5 Input Data Register
0x01E2 6074	SET_RIS_TRIG45	GPIO Banks 4 and 5 Set Rising Edge Interrupt Register
0x01E2 6078	CLR_RIS_TRIG45	GPIO Banks 4 and 5 Clear Rising Edge Interrupt Register
0x01E2 607C	SET_FAL_TRIG45	GPIO Banks 4 and 5 Set Falling Edge Interrupt Register
0x01E2 6080	CLR_FAL_TRIG45	GPIO Banks 4 and 5 Clear Falling Edge Interrupt Register
0x01E2 6084	INTSTAT45	GPIO Banks 4 and 5 Interrupt Status Register
GPIO Banks 6 and 7		
0x01E2 6088	DIR67	GPIO Banks 6 and 7 Direction Register
0x01E2 608C	OUT_DATA67	GPIO Banks 6 and 7 Output Data Register
0x01E2 6090	SET_DATA67	GPIO Banks 6 and 7 Set Data Register
0x01E2 6094	CLR_DATA67	GPIO Banks 6 and 7 Clear Data Register
0x01E2 6098	IN_DATA67	GPIO Banks 6 and 7 Input Data Register
0x01E2 609C	SET_RIS_TRIG67	GPIO Banks 6 and 7 Set Rising Edge Interrupt Register
0x01E2 60A0	CLR_RIS_TRIG67	GPIO Banks 6 and 7 Clear Rising Edge Interrupt Register
0x01E2 60A4	SET_FAL_TRIG67	GPIO Banks 6 and 7 Set Falling Edge Interrupt Register
0x01E2 60A8	CLR_FAL_TRIG67	GPIO Banks 6 and 7 Clear Falling Edge Interrupt Register
0x01E2 60AC	INTSTAT67	GPIO Banks 6 and 7 Interrupt Status Register

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5.8.2 GPIO Peripheral Input/Output Electrical Data/Timing

Table 5-12. Timing Requirements for GPIO Inputs(1) (see Figure 5-11)

NO.			MIN	MAX	UNIT
1	$t_{w(GPIH)}$	Pulse duration, GPIx high	2C(1) (2)		ns
2	$t_{w(GPIL)}$	Pulse duration, GPIx low	2C(1) (2)		ns

(1) The pulse width given is sufficient to generate a CPU interrupt or an EDMA event. However, if a user wants to have the device recognize the GPIx changes through software polling of the GPIO register, the GPIx duration must be extended to allow the device enough time to access the GPIO register through the internal bus.
(2) C=SYSCLK4 period in ns. For example, when running parts at 300 MHz, C=13.33 ns.

Table 5-13. Switching Characteristics Over Recommended Operating Conditions for GPIO Outputs (see Figure 5-11)

NO.	PARAMETER		MIN	MAX	UNIT
3	$t_{w(GPOH)}$	Pulse duration, GPOx high	2C(1) (2)		ns
4	$t_{w(GPOL)}$	Pulse duration, GPOx low	2C(1) (2)		ns

(1) This parameter value should not be used as a maximum performance specification. Actual performance of back-to-back accesses of the GPIO is dependent upon internal bus activity.
(2) C=SYSCLK4 period in ns. For example, when running parts at 300 MHz, C=13.33 ns.

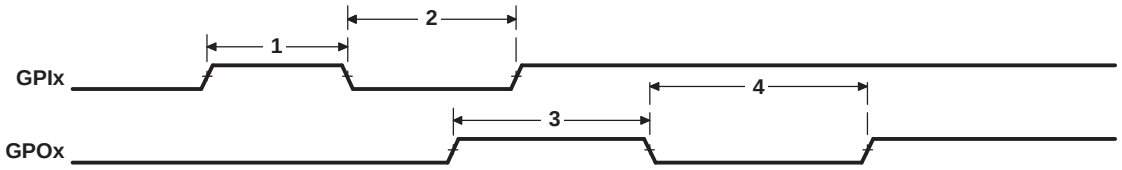

Figure 5-11. GPIO Port Timing

5.8.3 GPIO Peripheral External Interrupts Electrical Data/Timing

Table 5-14. Timing Requirements for External Interrupts(1) (see Figure 5-12)

NO.			MIN	MAX	UNIT
1	$t_{w(ILOW)}$	Width of the external interrupt pulse low	2C(1) (2)		ns
2	$t_{w(IHIGH)}$	Width of the external interrupt pulse high	2C(1) (2)		ns

(1) The pulse width given is sufficient to generate an interrupt or an EDMA event. However, if a user wants to have the device recognize the GPIO changes through software polling of the GPIO register, the GPIO duration must be extended to allow the device enough time to access the GPIO register through the internal bus.
(2) C=SYSCLK4 period in ns. For example, when running parts at 300 MHz, C=13.33 ns.

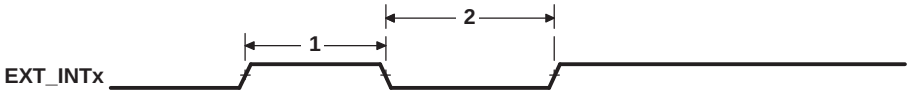

Figure 5-12. GPIO External Interrupt Timing

5.9 EDMA

Table 5-15 is the list of EDMA3 Channel Contoller Registers and Table 5-16 is the list of EDMA3 Transfer Controller registers. See the *TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.* – Literature Number SPRUFK9 for more details.

Table 5-15. EDMA3 Channel Controller (EDMA3CC) Registers

BYTE ADDRESS	Acronym	Register Description
0x01C0 0000	PID	Peripheral Identification Register
0x01C0 0004	CCCFG	EDMA3CC Configuration Register
Global Registers		
0x01C0 0200	QCHMAP0	QDMA Channel 0 Mapping Register
0x01C0 0204	QCHMAP1	QDMA Channel 1 Mapping Register
0x01C0 0208	QCHMAP2	QDMA Channel 2 Mapping Register
0x01C0 020C	QCHMAP3	QDMA Channel 3 Mapping Register
0x01C0 0210	QCHMAP4	QDMA Channel 4 Mapping Register
0x01C0 0214	QCHMAP5	QDMA Channel 5 Mapping Register
0x01C0 0218	QCHMAP6	QDMA Channel 6 Mapping Register
0x01C0 021C	QCHMAP7	QDMA Channel 7 Mapping Register
0x01C0 0240	DMAQNUM0	DMA Channel Queue Number Register 0
0x01C0 0244	DMAQNUM1	DMA Channel Queue Number Register 1
0x01C0 0248	DMAQNUM2	DMA Channel Queue Number Register 2
0x01C0 024C	DMAQNUM3	DMA Channel Queue Number Register 3
0x01C0 0260	QDMAQNUM	QDMA Channel Queue Number Register
0x01C0 0284	QUEPRI	Queue Priority Register(1)
0x01C0 0300	EMR	Event Missed Register
0x01C0 0308	EMCR	Event Missed Clear Register
0x01C0 0310	QEMR	QDMA Event Missed Register
0x01C0 0314	QEMCR	QDMA Event Missed Clear Register
0x01C0 0318	CCERR	EDMA3CC Error Register
0x01C0 031C	CCERRCLR	EDMA3CC Error Clear Register
0x01C0 0320	EEVAL	Error Evaluate Register
0x01C0 0340	DRAE0	DMA Region Access Enable Register for Region 0
0x01C0 0348	DRAE1	DMA Region Access Enable Register for Region 1
0x01C0 0350	DRAE2	DMA Region Access Enable Register for Region 2
0x01C0 0358	DRAE3	DMA Region Access Enable Register for Region 3
0x01C0 0380	QRAE0	QDMA Region Access Enable Register for Region 0
0x01C0 0384	QRAE1	QDMA Region Access Enable Register for Region 1
0x01C0 0388	QRAE2	QDMA Region Access Enable Register for Region 2
0x01C0 038C	QRAE3	QDMA Region Access Enable Register for Region 3
0x01C0 0400 - 0x01C0 043C	Q0E0-Q0E15	Event Queue Entry Registers Q0E0-Q0E15
0x01C0 0440 - 0x01C0 047C	Q1E0-Q1E15	Event Queue Entry Registers Q1E0-Q1E15
0x01C0 0600	QSTAT0	Queue 0 Status Register
0x01C0 0604	QSTAT1	Queue 1 Status Register
0x01C0 0620	QWMTHRA	Queue Watermark Threshold A Register
0x01C0 0640	CCSTAT	EDMA3CC Status Register
Global Channel Registers		
0x01C0 1000	ER	Event Register

(1) On previous architectures, the EDMA3TC priority was controlled by the queue priority register (QUEPRI) in the EDMA3CC memory-map. However for this device, the priority control for the transfer controllers is controlled by the chip-level registers in the System Configuration Module. You should use the chip-level registers and not QUEPRI to configure the TC priority.

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Table 5-15. EDMA3 Channel Controller (EDMA3CC) Registers (continued)

BYTE ADDRESS	Acronym	Register Description
0x01C0 1008	ECR	Event Clear Register
0x01C0 1010	ESR	Event Set Register
0x01C0 1018	CER	Chained Event Register
0x01C0 1020	EER	Event Enable Register
0x01C0 1028	EECR	Event Enable Clear Register
0x01C0 1030	EESR	Event Enable Set Register
0x01C0 1038	SER	Secondary Event Register
0x01C0 1040	SECR	Secondary Event Clear Register
0x01C0 1050	IER	Interrupt Enable Register
0x01C0 1058	IECR	Interrupt Enable Clear Register
0x01C0 1060	IESR	Interrupt Enable Set Register
0x01C0 1068	IPR	Interrupt Pending Register
0x01C0 1070	ICR	Interrupt Clear Register
0x01C0 1078	IEVAL	Interrupt Evaluate Register
0x01C0 1080	QER	QDMA Event Register
0x01C0 1084	QEER	QDMA Event Enable Register
0x01C0 1088	QEECR	QDMA Event Enable Clear Register
0x01C0 108C	QEESR	QDMA Event Enable Set Register
0x01C0 1090	QSER	QDMA Secondary Event Register
0x01C0 1094	QSECR	QDMA Secondary Event Clear Register
Shadow Region 0 Channel Registers		
0x01C0 2000	ER	Event Register
0x01C0 2008	ECR	Event Clear Register
0x01C0 2010	ESR	Event Set Register
0x01C0 2018	CER	Chained Event Register
0x01C0 2020	EER	Event Enable Register
0x01C0 2028	EECR	Event Enable Clear Register
0x01C0 2030	EESR	Event Enable Set Register
0x01C0 2038	SER	Secondary Event Register
0x01C0 2040	SECR	Secondary Event Clear Register
0x01C0 2050	IER	Interrupt Enable Register
0x01C0 2058	IECR	Interrupt Enable Clear Register
0x01C0 2060	IESR	Interrupt Enable Set Register
0x01C0 2068	IPR	Interrupt Pending Register
0x01C0 2070	ICR	Interrupt Clear Register
0x01C0 2078	IEVAL	Interrupt Evaluate Register
0x01C0 2080	QER	QDMA Event Register
0x01C0 2084	QEER	QDMA Event Enable Register
0x01C0 2088	QEECR	QDMA Event Enable Clear Register
0x01C0 208C	QEESR	QDMA Event Enable Set Register
0x01C0 2090	QSER	QDMA Secondary Event Register
0x01C0 2094	QSECR	QDMA Secondary Event Clear Register
Shadow Region 1 Channel Registers		
0x01C0 2200	ER	Event Register
0x01C0 2208	ECR	Event Clear Register
0x01C0 2210	ESR	Event Set Register
0x01C0 2218	CER	Chained Event Register

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Table 5-15. EDMA3 Channel Controller (EDMA3CC) Registers (continued)

BYTE ADDRESS	Acronym	Register Description
0x01C0 2220	EER	Event Enable Register
0x01C0 2228	EECR	Event Enable Clear Register
0x01C0 2230	EESR	Event Enable Set Register
0x01C0 2238	SER	Secondary Event Register
0x01C0 2240	SECR	Secondary Event Clear Register
0x01C0 2250	IER	Interrupt Enable Register
0x01C0 2258	IECR	Interrupt Enable Clear Register
0x01C0 2260	IESR	Interrupt Enable Set Register
0x01C0 2268	IPR	Interrupt Pending Register
0x01C0 2270	ICR	Interrupt Clear Register
0x01C0 2278	IEVAL	Interrupt Evaluate Register
0x01C0 2280	QER	QDMA Event Register
0x01C0 2284	QEER	QDMA Event Enable Register
0x01C0 2288	QEECR	QDMA Event Enable Clear Register
0x01C0 228C	QEESR	QDMA Event Enable Set Register
0x01C0 2290	QSER	QDMA Secondary Event Register
0x01C0 2294	QSECR	QDMA Secondary Event Clear Register
0x01C0 4000 - 0x01C0 4FFF	—	Parameter RAM (PaRAM)

Table 5-16. EDMA3 Transfer Controller (EDMA3TC) Registers

Offset	Transfer Controller 0 BYTE ADDRESS	Transfer Controller 1 BYTE ADDRESS	Acronym	Register Description
0h	0x01C0 8000	0x01C0 8400	PID	Peripheral Identification Register
4h	0x01C0 8004	0x01C0 8404	TCCFG	EDMA3TC Configuration Register
100h	0x01C0 8100	0x01C0 8500	TCSTAT	EDMA3TC Channel Status Register
120h	0x01C0 8120	0x01C0 8520	ERRSTAT	Error Status Register
124h	0x01C0 8124	0x01C0 8524	ERREN	Error Enable Register
128h	0x01C0 8128	0x01C0 8528	ERRCLR	Error Clear Register
12Ch	0x01C0 812C	0x01C0 852C	ERRDET	Error Details Register
130h	0x01C0 8130	0x01C0 8530	ERRCMD	Error Interrupt Command Register
140h	0x01C0 8140	0x01C0 8540	RDRATE	Read Command Rate Register
240h	0x01C0 8240	0x01C0 8640	SAOPT	Source Active Options Register
244h	0x01C0 8244	0x01C0 8644	SASRC	Source Active Source Address Register
248h	0x01C0 8248	0x01C0 8648	SACNT	Source Active Count Register
24Ch	0x01C0 824C	0x01C0 864C	SADST	Source Active Destination Address Register
250h	0x01C0 8250	0x01C0 8650	SABIDX	Source Active B-Index Register
254h	0x01C0 8254	0x01C0 8654	SAMPPRXY	Source Active Memory Protection Proxy Register
258h	0x01C0 8258	0x01C0 8658	SACNTRLD	Source Active Count Reload Register
25Ch	0x01C0 825C	0x01C0 865C	SASRCBREF	Source Active Source Address B-Reference Register
260h	0x01C0 8260	0x01C0 8660	SADSTBREF	Source Active Destination Address B-Reference Register
280h	0x01C0 8280	0x01C0 8680	DFCNTRLD	Destination FIFO Set Count Reload Register
284h	0x01C0 8284	0x01C0 8684	DFSRCBREF	Destination FIFO Set Source Address B-Reference Register
288h	0x01C0 8288	0x01C0 8688	DFDSTBREF	Destination FIFO Set Destination Address B-Reference Register
300h	0x01C0 8300	0x01C0 8700	DFOPT0	Destination FIFO Options Register 0
304h	0x01C0 8304	0x01C0 8704	DFSRC0	Destination FIFO Source Address Register 0
308h	0x01C0 8308	0x01C0 8708	DFCNT0	Destination FIFO Count Register 0

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Table 5-16. EDMA3 Transfer Controller (EDMA3TC) Registers (continued)

Offset	Transfer Controller 0 BYTE ADDRESS	Transfer Controller 1 BYTE ADDRESS	Acronym	Register Description
30Ch	0x01C0 830C	0x01C0 870C	DFDST0	Destination FIFO Destination Address Register 0
310h	0x01C0 8310	0x01C0 8710	DFBIDX0	Destination FIFO B-Index Register 0
314h	0x01C0 8314	0x01C0 8714	DFMPPRXY0	Destination FIFO Memory Protection Proxy Register 0
340h	0x01C0 8340	0x01C0 8740	DFOPT1	Destination FIFO Options Register 1
344h	0x01C0 8344	0x01C0 8744	DFSRC1	Destination FIFO Source Address Register 1
348h	0x01C0 8348	0x01C0 8748	DFCNT1	Destination FIFO Count Register 1
34Ch	0x01C0 834C	0x01C0 874C	DFDST1	Destination FIFO Destination Address Register 1
350h	0x01C0 8350	0x01C0 8750	DFBIDX1	Destination FIFO B-Index Register 1
354h	0x01C0 8354	0x01C0 8754	DFMPPRXY1	Destination FIFO Memory Protection Proxy Register 1
380h	0x01C0 8380	0x01C0 8780	DFOPT2	Destination FIFO Options Register 2
384h	0x01C0 8384	0x01C0 8784	DFSRC2	Destination FIFO Source Address Register 2
388h	0x01C0 8388	0x01C0 8788	DFCNT2	Destination FIFO Count Register 2
38Ch	0x01C0 838C	0x01C0 878C	DFDST2	Destination FIFO Destination Address Register 2
390h	0x01C0 8390	0x01C0 8790	DFBIDX2	Destination FIFO B-Index Register 2
394h	0x01C0 8394	0x01C0 8794	DFMPPRXY2	Destination FIFO Memory Protection Proxy Register 2
3C0h	0x01C0 83C0	0x01C0 87C0	DFOPT3	Destination FIFO Options Register 3
3C4h	0x01C0 83C4	0x01C0 87C4	DFSRC3	Destination FIFO Source Address Register 3
3C8h	0x01C0 83C8	0x01C0 87C8	DFCNT3	Destination FIFO Count Register 3
3CCh	0x01C0 83CC	0x01C0 87CC	DFDST3	Destination FIFO Destination Address Register 3
3D0h	0x01C0 83D0	0x01C0 87D0	DFBIDX3	Destination FIFO B-Index Register 3
3D4h	0x01C0 83D4	0x01C0 87D4	DFMPPRXY3	Destination FIFO Memory Protection Proxy Register 3

Table 5-17 shows an abbreviation of the set of registers which make up the parameter set for each of 128 EDMA events. Each of the parameter register sets consist of 8 32-bit word entries. Table 5-18 shows the parameter set entry registers with relative memory address locations within each of the parameter sets.

Table 5-17. EDMA Parameter Set RAM

HEX ADDRESS RANGE	DESCRIPTION
0x01C0 4000 - 0x01C0 401F	Parameters Set 0 (8 32-bit words)
0x01C0 4020 - 0x01C0 403F	Parameters Set 1 (8 32-bit words)
0x01C0 4040 - 0x01cC0 405F	Parameters Set 2 (8 32-bit words)
0x01C0 4060 - 0x01C0 407F	Parameters Set 3 (8 32-bit words)
0x01C0 4080 - 0x01C0 409F	Parameters Set 4 (8 32-bit words)
0x01C0 40A0 - 0x01C0 40BF	Parameters Set 5 (8 32-bit words)
...	...
0x01C0 4FC0 - 0x01C0 4FDF	Parameters Set 126 (8 32-bit words)
0x01C0 4FE0 - 0x01C0 4FFF	Parameters Set 127 (8 32-bit words)

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Table 5-18. Parameter Set Entries

HEX OFFSET ADDRESS WITHIN THE PARAMETER SET	ACRONYM	PARAMETER ENTRY
0x0000	OPT	Option
0x0004	SRC	Source Address
0x0008	A_B_CNT	A Count, B Count
0x000C	DST	Destination Address
0x0010	SRC_DST_BIDX	Source B Index, Destination B Index
0x0014	LINK_BCNTRLD	Link Address, B Count Reload
0x0018	SRC_DST_CIDX	Source C Index, Destination C Index
0x001C	CCNT	C Count

Table 5-19. EDMA Events

Event	Event Name / Source	Event	Event Name / Source
0	McASP0 Receive	16	MMCSD Receive
1	McASP0 Transmit	17	MMCSD Transmit
2	McASP1 Receive	18	SPI1 Receive
3	McASP1 Transmit	19	SPI1 Transmit
4	McASP2 Receive	20	dMAX EVTOUT[6]
5	McASP2 Transmit	21	dMAX EVTOUT[7]
6	GPIO Bank 0 Interrupt	22	GPIO Bank 2 Interrupt
7	GPIO Bank 1 Interrupt	23	GPIO Bank 3 Interrupt
8	UART0 Receive	24	I2C0 Receive
9	UART0 Transmit	25	I2C0 Transmit
10	Timer64P0 Event Out 12	26	I2C1 Receive
11	Timer64P0 Event Out 34	27	I2C1 Transmit
12	UART1 Receive	28	GPIO Bank 4 Interrupt
13	UART1 Transmit	29	GPIO Bank 5 Interrupt
14	SPI0 Receive	30	UART2 Receive
15	SPI0 Transmit	31	UART2 Transmit

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5.10 External Memory Interface A (EMIFA)

EMIFA is one of two external memory interfaces supported on the device. It is primarily intended to support asynchronous memory types, such as NAND and NOR flash and Asynchronous SRAM. However on this device, EMIFA also provides a secondary interface to SDRAM. See the *TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.* – Literature Number SPRUFK9 for more details.

5.10.1 EMIFA Asynchronous Memory Support

EMIFA supports asynchronous:

- SRAM memories
- NAND Flash memories
- NOR Flash memories

The EMIFA data bus width is up to 8 bits on the PTP package. The device supports up to fifteen address lines and an external wait/interrupt input. Up to four asynchronous chip selects are supported by EMIFA (EMA_CS[5:2]) . Two of the four chip selects are available on the PTP package (EMA_CS[3:2]).

Each chip select has the following individually programmable attributes:

- Data Bus Width
- Read cycle timings: setup, hold, strobe
- Write cycle timings: setup, hold, strobe
- Bus turn around time
- Extended Wait Option With Programmable Timeout
- Select Strobe Option
- NAND flash controller supports 1-bit and 4-bit ECC calculation on blocks of 512 bytes.

5.10.2 EMIFA Connection Examples

Figure 5-13 illustrates an example of how SDRAM, NOR, and NAND flash devices might be connected to EMIFA of the device simultaneously. The SDRAM chip select must be EMA_CS[0]. Note that the NOR flash is connected to EMA_CS[2] and the NAND flash is connected to EMA_CS[3] in this example. Note that any type of asynchronous memory may be connected to EMA_CS[5:2].

The on-chip bootloader makes some assumptions on which chip select the contains the boot image, and this depends on the boot mode. For NOR boot mode; the on-chip bootloader requires that the image be stored in NOR flash on EMA_CS[2]. For NAND boot mode, the bootloader requires that the boot image is stored in NAND flash on EMA_CS[3]. It is always possible to have the image span multiple chip selects, but this must be supported by second stage boot code stored in the external flash.

A likely use case with more than one EMIFA chip select used for NAND flash is illustrated in Figure 5-14. This figure shows how two multiplane NAND flash devices with two chip selects each would connect to the device EMIFA. In this case if NAND is the boot memory, then the boot image needs to be stored in the NAND area selected by EMA_CS[3]. Part of the application image could spill over into the NAND regions selected by other EMIFA chip selects; but would rely on the code stored in the EMA_CS[3] area to bootload it. Note that this example could also apply to the OMAPL137 device; except only one multiplane NAND could be supported with only EMA_CS[3:2] available.

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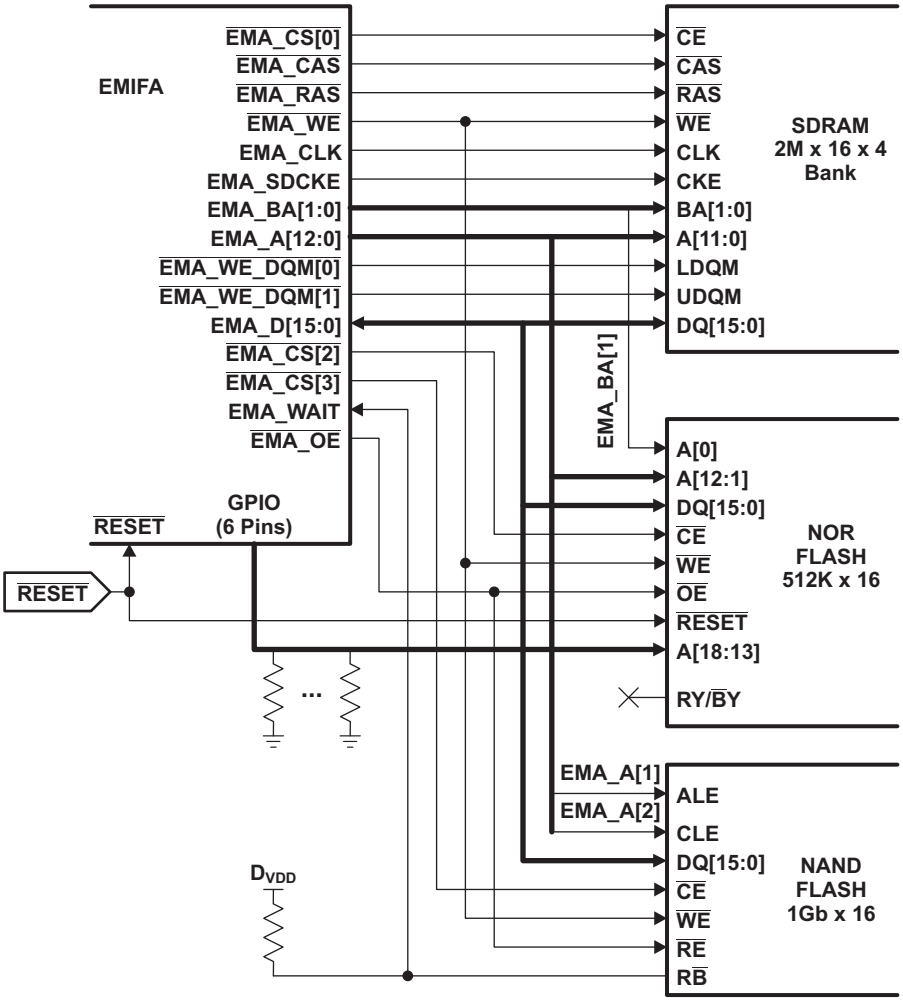

Figure 5-13. OMAPL137 Connection Diagram: SDRAM, NOR, NAND

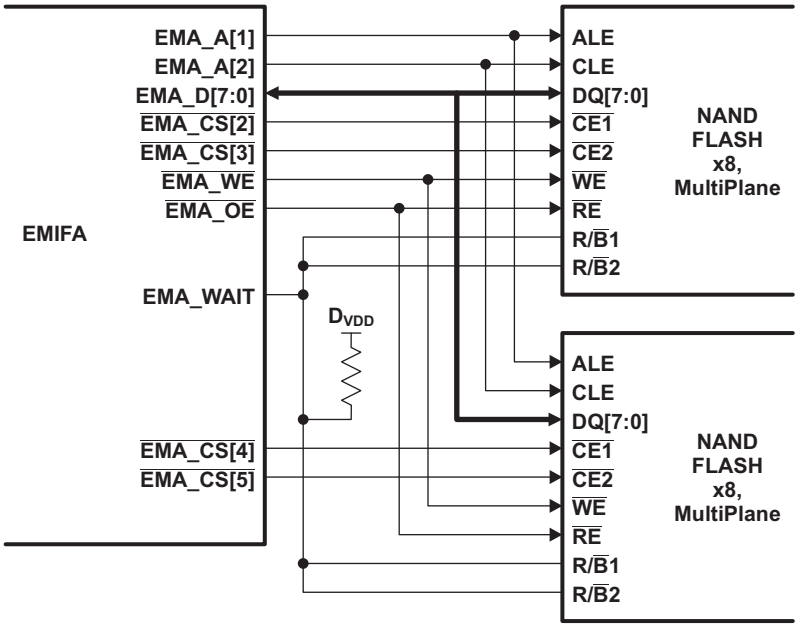

Figure 5-14. OMAPL137 EMIFA Connection Diagram: Multiple NAND Flash Planes

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5.10.3 External Memory Interface (EMIF)

Table 5-20 is a list of the EMIF registers. For more information about these registers, see the C674x DSP External Memory Interface (EMIF) User's Guide (literature number SPRU711).

Table 5-20. External Memory Interface (EMIFA) Registers

BYTE ADDRESS	Register Name	Register Description
0x6800 0000	MIDR	Module ID Register
0x6800 0004	AWCC	Asynchronous Wait Cycle Configuration Register
0x6800 0008	SDCR	SDRAM Configuration Register
0x6800 000C	SDRCR	SDRAM Refresh Control Register
0x6800 0010	CE2CFG	Asynchronous 1 Configuration Register
0x6800 0014	CE3CFG	Asynchronous 2 Configuration Register
0x6800 0018	CE4CFG	Asynchronous 3 Configuration Register
0x6800 001C	CE5CFG	Asynchronous 4 Configuration Register
0x6800 0020	SDTIMR	SDRAM Timing Register
0x6800 003C	SDSRETR	SDRAM Self Refresh Exit Timing Register
0x6800 0040	INTRAW	EMIFA Interrupt Raw Register
0x6800 0044	INTMSK	EMIFA Interrupt Mask Register
0x6800 0048	INTMSKSET	EMIFA Interrupt Mask Set Register
0x6800 004C	INTMSKCLR	EMIFA Interrupt Mask Clear Register
0x6800 0060	NANDFCR	NAND Flash Control Register
0x6800 0064	NANDFSR	NAND Flash Status Register
0x6800 0070	NANDF1ECC	NAND Flash 1 ECC Register (CS2 Space)
0x6800 0074	NANDF2ECC	NAND Flash 2 ECC Register (CS3 Space)
0x6800 0078	NANDF3ECC	NAND Flash 3 ECC Register (CS4 Space)
0x6800 007C	NANDF4ECC	NAND Flash 4 ECC Register (CS5 Space)
0x6800 00BC	NAND4BITECCLOAD	NAND Flash 4-Bit ECC Load Register
0x6800 00C0	NAND4BITECC1	NAND Flash 4-Bit ECC Register 1
0x6800 00C4	NAND4BITECC2	NAND Flash 4-Bit ECC Register 2
0x6800 00C8	NAND4BITECC3	NAND Flash 4-Bit ECC Register 3
0x6800 00CC	NAND4BITECC4	NAND Flash 4-Bit ECC Register 4
0x6800 00D0	NANDERRADD1	NAND Flash 4-Bit ECC Error Address Register 1
0x6800 00D4	NANDERRADD2	NAND Flash 4-Bit ECC Error Address Register 2
0x6800 00D8	NANDERRVAL1	NAND Flash 4-Bit ECC Error Value Register 1
0x6800 00DC	NANDERRVAL2	NAND Flash 4-Bit ECC Error Value Register 2

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5.10.4 EMIFA Electrical Data/Timing

Table 5-21 through Table 5-22 assume testing over recommended operating conditions.

Table 5-21. EMIFA Asynchronous Memory Timing Requirements(1)(2)

NO.			MIN	Nom	MAX	UNIT
READS and WRITES						
2	$t_{w(EM_WAIT)}$	Pulse duration, EM_WAIT assertion and deassertion	2E			ns
READS						
12	$t_{su(EMDV-EMOEH)}$	Setup time, EM_D[15:0] valid before $\overline{EM_OE}$ high	3			ns
13	$t_{h(EMOEH-EMDIV)}$	Hold time, EM_D[15:0] valid after $\overline{EM_OE}$ high	0.5			ns
14	$t_{su\ (EMOEL-EMWAIT)}$	Setup Time, EM_WAIT asserted before end of Strobe Phase(3)	4E+3			ns
WRITES						
28	$t_{su\ (EMWEL-EMWAIT)}$	Setup Time, EM_WAIT asserted before end of Strobe Phase(3)	4E+3			ns

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(2) E = EMA_CLK period or in ns. EMA_CLK is selected either as SYSCLK3 or the PLL output clock divided by 4.5. As an example, when SYSCLK3 is selected and set to 100MHz, E=10ns.
(3) Setup before end of STROBE phase (if no extended wait states are inserted) by which EM_WAIT must be asserted to add extended wait states. Figure 5-19 and Figure 5-20 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.

Table 5-22. EMIFA Asynchronous Memory Switching Characteristics(1)(2) (3) (4)

NO.	PARAMETER		MIN	Nom	MAX	UNIT
READS and WRITES						
1	$t_{d(TURNAROUND)}$	Turn around time	(TA)*E - 3	(TA)*E	(TA)*E + 3	ns
READS						
3	$t_{c(EMRCYCLE)}$	EMIF read cycle time (EW = 0)	(RS+RST+RH)*E - 3	(RS+RST+RH)*E	(RS+RST+RH)*E + 3	ns
		EMIF read cycle time (EW = 1)	(RS+RST+RH+(EWC*16))*E - 3	(RS+RST+RH+(EWC*16))*E	(RS+RST+RH+(EWC*16))*E + 3	ns
4	$t_{su(EMCEL-EMOEL)}$	Output setup time, $\overline{EMA_CE[5:2]}$ low to $\overline{EMA_OE}$ low (SS = 0)	(RS)*E-3	(RS)*E	(RS)*E+3	ns
		Output setup time, $\overline{EMA_CE[5:2]}$ low to $\overline{EMA_OE}$ low (SS = 1)	-3	0	+3	ns
5	$t_{h(EMOEH-EMCEH)}$	Output hold time, $\overline{EMA_OE}$ high to $\overline{EMA_CE[5:2]}$ high (SS = 0)	(RH)*E - 3	(RH)*E	(RH)*E + 3	ns
		Output hold time, $\overline{EMA_OE}$ high to $\overline{EMA_CE[5:2]}$ high (SS = 1)	-3	0	+3	ns
6	$t_{su(EMBAV-EMOEL)}$	Output setup time, $\overline{EMA_BA[1:0]}$ valid to $\overline{EMA_OE}$ low	(RS)*E-3	(RS)*E	(RS)*E+3	ns
7	$t_{h(EMOEH-EMBAIV)}$	Output hold time, $\overline{EMA_OE}$ high to $\overline{EMA_BA[1:0]}$ invalid	(RH)*E-3	(RH)*E	(RH)*E+3	ns
8	$t_{su(EMBAV-EMOEL)}$	Output setup time, $\overline{EMA_A[13:0]}$ valid to $\overline{EMA_OE}$ low	(RS)*E-3	(RS)*E	(RS)*E+3	ns
9	$t_{h(EMOEH-EMAIV)}$	Output hold time, $\overline{EMA_OE}$ high to $\overline{EMA_A[13:0]}$ invalid	(RH)*E-3	(RH)*E	(RH)*E+3	ns

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(2) TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed via the Asynchronous Bank and Asynchronous Wait Cycle Configuration Registers. These support the following range of values: TA[4-1], RS[16-1], RST[64-1], RH[8-1], WS[16-1], WST[64-1], WH[8-1], and MEW[1-256].
(3) E = EMA_CLK period or in ns. EMA_CLK is selected either as SYSCLK3 or the PLL output clock divided by 4.5. As an example, when SYSCLK3 is selected and set to 100MHz, E=10ns.
(4) EWC = external wait cycles determined by EMA_WAIT input signal. EWC supports the following range of values EWC[256-1]. Note that the maximum wait time before timeout is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register.

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Table 5-22. EMIFA Asynchronous Memory Switching Characteristics[1][2] [3] [4] (continued)

NO.	PARAMETER		MIN	Nom	MAX	UNIT
10	$t_{w(EMOEL)}$	$\overline{EMA_OE}$ active low width (EW = 0)	(RST)*E-3	(RST)*E	(RST)*E+3	ns
		$\overline{EMA_OE}$ active low width (EW = 1)	(RST+(EWC*16))*E-3	(RST+(EWC*16))*E	(RST+(EWC*16))*E+3	ns
11	$t_{d(EMWAITH-EMOEH)}$	Delay time from EMA_WAIT deasserted to $\overline{EMA_OE}$ high	3E-3	4E	4E+3	ns
WRITES						
15	$t_{c(EMWCYCLE)}$	EMIF write cycle time (EW = 0)	(WS+WST+WH)*E-3	(WS+WST+WH)*E	(WS+WST+WH)*E+3	ns
		EMIF write cycle time (EW = 1)	(WS+WST+WH+(EWC*16))*E - 3	(WS+WST+WH+(EWC*16))*E	(WS+WST+WH+(EWC*16))*E + 3	ns
16	$t_{su(EMCEL-EMWEL)}$	Output setup time, $\overline{EMA_CE[5:2]}$ low to $\overline{EMA_WE}$ low (SS = 0)	(WS)*E - 3	(WS)*E	(WS)*E + 3	ns
		Output setup time, $\overline{EMA_CE[5:2]}$ low to $\overline{EMA_WE}$ low (SS = 1)	-3	0	+3	ns
17	$t_{h(EMWEH-EMCEH)}$	Output hold time, $\overline{EMA_WE}$ high to $\overline{EMA_CE[5:2]}$ high (SS = 0)	(WH)*E-3	(WH)*E	(WH)*E+3	ns
		Output hold time, $\overline{EMA_WE}$ high to $\overline{EMA_CE[5:2]}$ high (SS = 1)	-3	0	+3	ns
18	$t_{su(EMDQMV-EMWEL)}$	Output setup time, $\overline{EMA_BA[1:0]}$ valid to $\overline{EMA_WE}$ low	(WS)*E-3	(WS)*E	(WS)*E+3	ns
19	$t_{h(EMWEH-EMDQMIV)}$	Output hold time, $\overline{EMA_WE}$ high to $\overline{EMA_BA[1:0]}$ invalid	(WH)*E-3	(WH)*E	(WH)*E+3	ns
20	$t_{su(EMBAV-EMWEL)}$	Output setup time, $\overline{EMA_BA[1:0]}$ valid to $\overline{EMA_WE}$ low	(WS)*E-3	(WS)*E	(WS)*E+3	ns
21	$t_{h(EMWEH-EMBAIV)}$	Output hold time, $\overline{EMA_WE}$ high to $\overline{EMA_BA[1:0]}$ invalid	(WH)*E-3	(WH)*E	(WH)*E+3	ns
22	$t_{su(EMAV-EMWEL)}$	Output setup time, $\overline{EMA_A[13:0]}$ valid to $\overline{EMA_WE}$ low	(WS)*E-3	(WS)*E	(WS)*E+3	ns
23	$t_{h(EMWEH-EMAIV)}$	Output hold time, $\overline{EMA_WE}$ high to $\overline{EMA_A[13:0]}$ invalid	(WH)*E-3	(WH)*E	(WH)*E+3	ns
24	$t_{w(EMWEL)}$	$\overline{EMA_WE}$ active low width (EW = 0)	(WST)*E-3	(WST)*E	(WST)*E+3	ns
		$\overline{EMA_WE}$ active low width (EW = 1)	(WST+(EWC*16))*E-3	(WST+(EWC*16))*E	(WST+(EWC*16))*E+3	ns
25	$t_{d(EMWAITH-EMWEH)}$	Delay time from EMA_WAIT deasserted to $\overline{EMA_WE}$ high	3E-3	4E	4E+3	ns
26	$t_{su(EMDV-EMWEL)}$	Output setup time, $\overline{EMA_D[15:0]}$ valid to $\overline{EMA_WE}$ low	(WS)*E-3	(WS)*E	(WS)*E+3	ns
27	$t_{h(EMWEH-EMDIV)}$	Output hold time, $\overline{EMA_WE}$ high to $\overline{EMA_D[15:0]}$ invalid	(WH)*E-3	(WH)*E	(WH)*E+3	ns

Table 5-23. Timing Requirements for EMIFA SDRAM Interface

Parameters are characterized from -40°C to 125°C unless otherwise noted.

NO.	PARAMETER		1.2V		1.1V		1.0V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
19	$t_{su(EMA_DV-EM_CLKH)}$	Input setup time, read data valid on EMA_D[15:0] before EMA_CLK rising	2		3		3		ns
20	$t_{h(CLKH-DIV)}$	Input hold time, read data valid on EMA_D[15:0] after EMA_CLK rising	1.6		1.6		1.6		ns

Table 5-24. Switching Characteristics for EMIFA SDRAM Interface

Parameters are characterized from -40°C to 125°C unless otherwise noted.

NO.	PARAMETER		1.2V		1.1V		1.0V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(CLK)}$	Cycle time, EMIF clock EMA_CLK	10		15		20		ns
2	$t_{w(CLK)}$	Pulse width, EMIF clock EMA_CLK high or low	3		5		8		ns
3	$t_{d(CLKH-CSV)}$	Delay time, EMA_CLK rising to $\overline{EMA_CS[0]}$ valid		7		9.5		13	ns
4	$t_{oh(CLKH-CSIV)}$	Output hold time, EMA_CLK rising to $\overline{EMA_CS[0]}$ invalid	1		1		1		ns

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Table 5-24. Switching Characteristics for EMIFA SDRAM Interface (continued)

Parameters are characterized from -40°C to 125°C unless otherwise noted.

NO.	PARAMETER		1.2V		1.1V		1.0V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
5	$t_{d(CLKH-DQMV)}$	Delay time, EMA_CLK rising to EMA_$\overline{WE}$_DQM[1:0] valid		7		9.5		13	ns
6	$t_{oh(CLKH-DQMIV)}$	Output hold time, EMA_CLK rising to EMA_$\overline{WE}$_DQM[1:0] invalid	1		1		1		ns
7	$t_{d(CLKH-AV)}$	Delay time, EMA_CLK rising to EMA_A[12:0] and EMA_BA[1:0] valid		7		9.5		13	ns
8	$t_{oh(CLKH-AIV)}$	Output hold time, EMA_CLK rising to EMA_A[12:0] and EMA_BA[1:0] invalid	1		1		1		ns
9	$t_{d(CLKH-DV)}$	Delay time, EMA_CLK rising to EMA_D[15:0] valid		7		9.5		13	ns
10	$t_{oh(CLKH-DIV)}$	Output hold time, EMA_CLK rising to EMA_D[15:0] invalid	1		1		1		ns
11	$t_{d(CLKH-RASV)}$	Delay time, EMA_CLK rising to $\overline{EMA_RAS}$ valid		7		9.5		13	ns
12	$t_{oh(CLKH-RASIV)}$	Output hold time, EMA_CLK rising to $\overline{EMA_RAS}$ invalid	1		1		1		ns
13	$t_{d(CLKH-CASV)}$	Delay time, EMA_CLK rising to $\overline{EMA_CAS}$ valid		7		9.5		13	ns
14	$t_{oh(CLKH-CASIV)}$	Output hold time, EMA_CLK rising to $\overline{EMA_CAS}$ invalid	1		1		1		ns
15	$t_{d(CLKH-WEV)}$	Delay time, EMA_CLK rising to $\overline{EMA_WE}$ valid		7		9.5		13	ns
16	$t_{oh(CLKH-WEIV)}$	Output hold time, EMA_CLK rising to $\overline{EMA_WE}$ invalid	1		1		1		ns
17	$t_{dis(CLKH-DHZ)}$	Delay time, EMA_CLK rising to EMA_D[15:0] tri-stated		7		9.5		13	ns
18	$t_{ena(CLKH-DLZ)}$	Output hold time, EMA_CLK rising to EMA_D[15:0] driving	1		1		1		ns

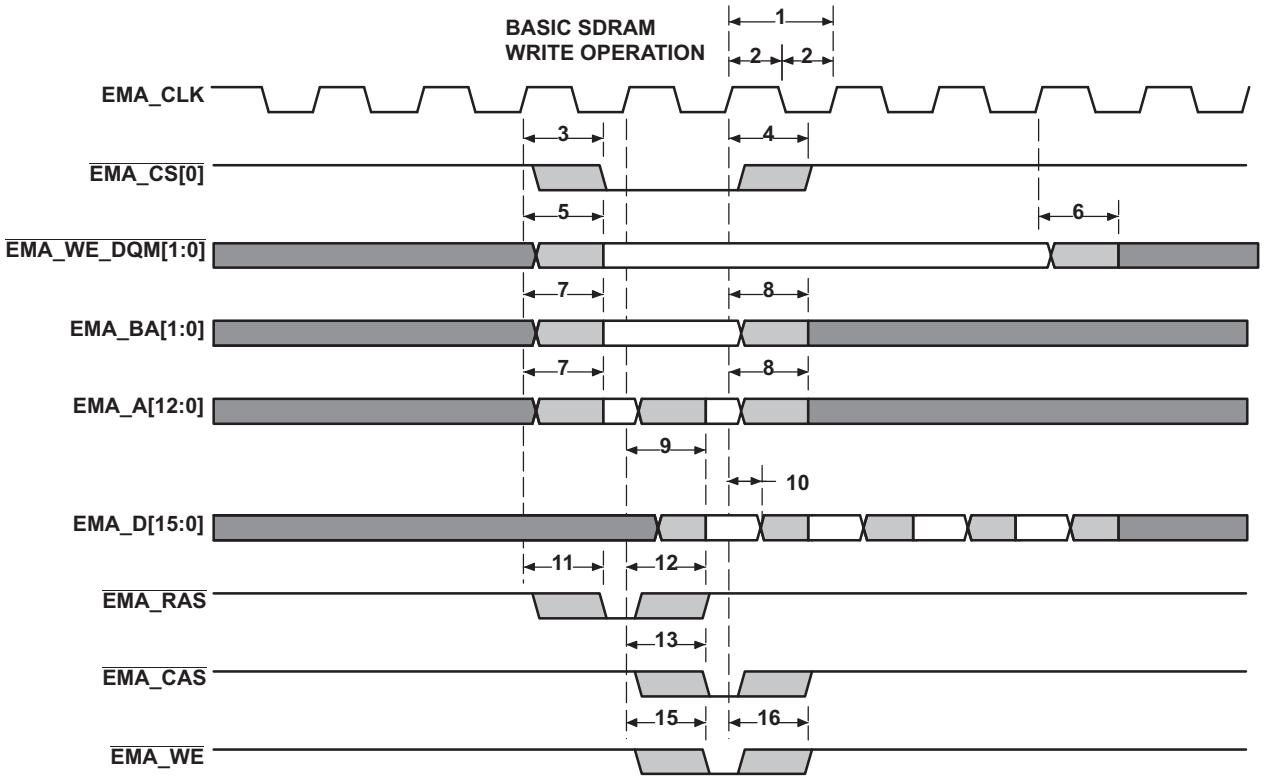

Figure 5-15. EMIFA Basic SDRAM Write Operation

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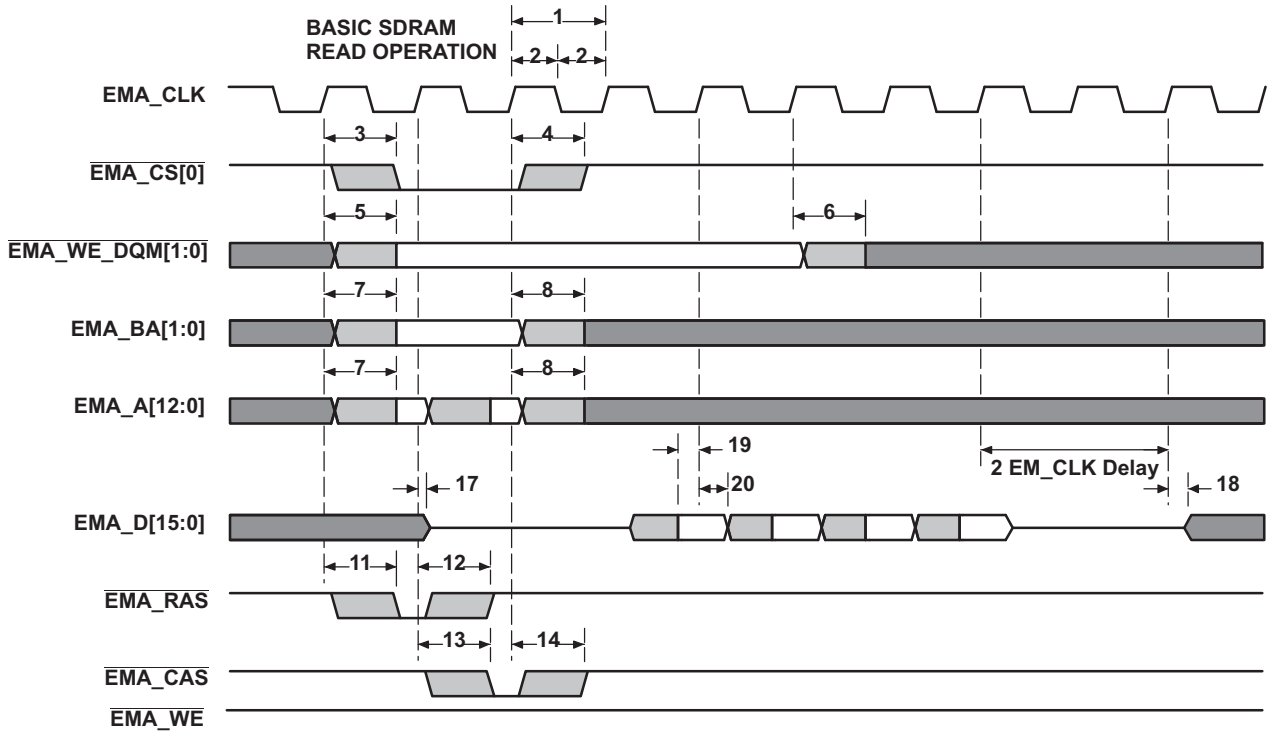

Figure 5-16. EMIFA Basic SDRAM Read Operation

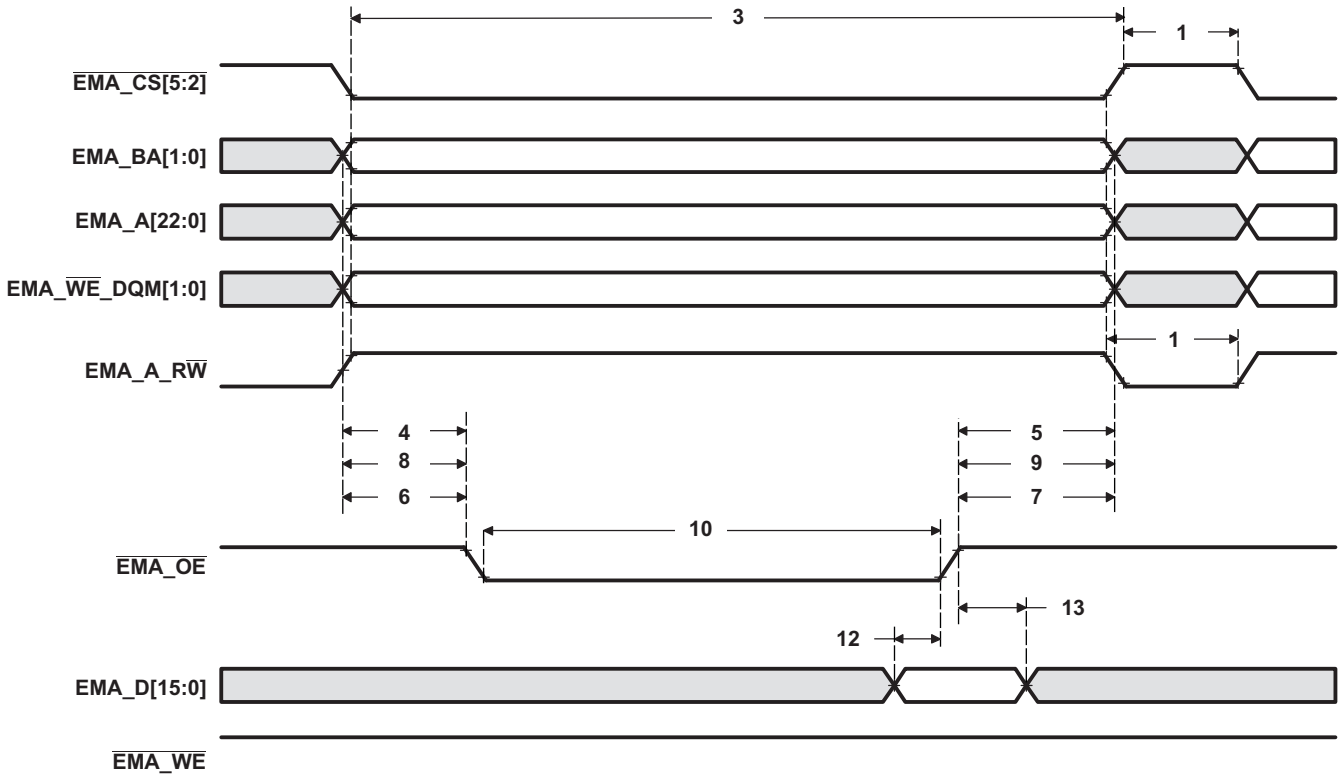

Figure 5-17. Asynchronous Memory Read Timing for EMIFA

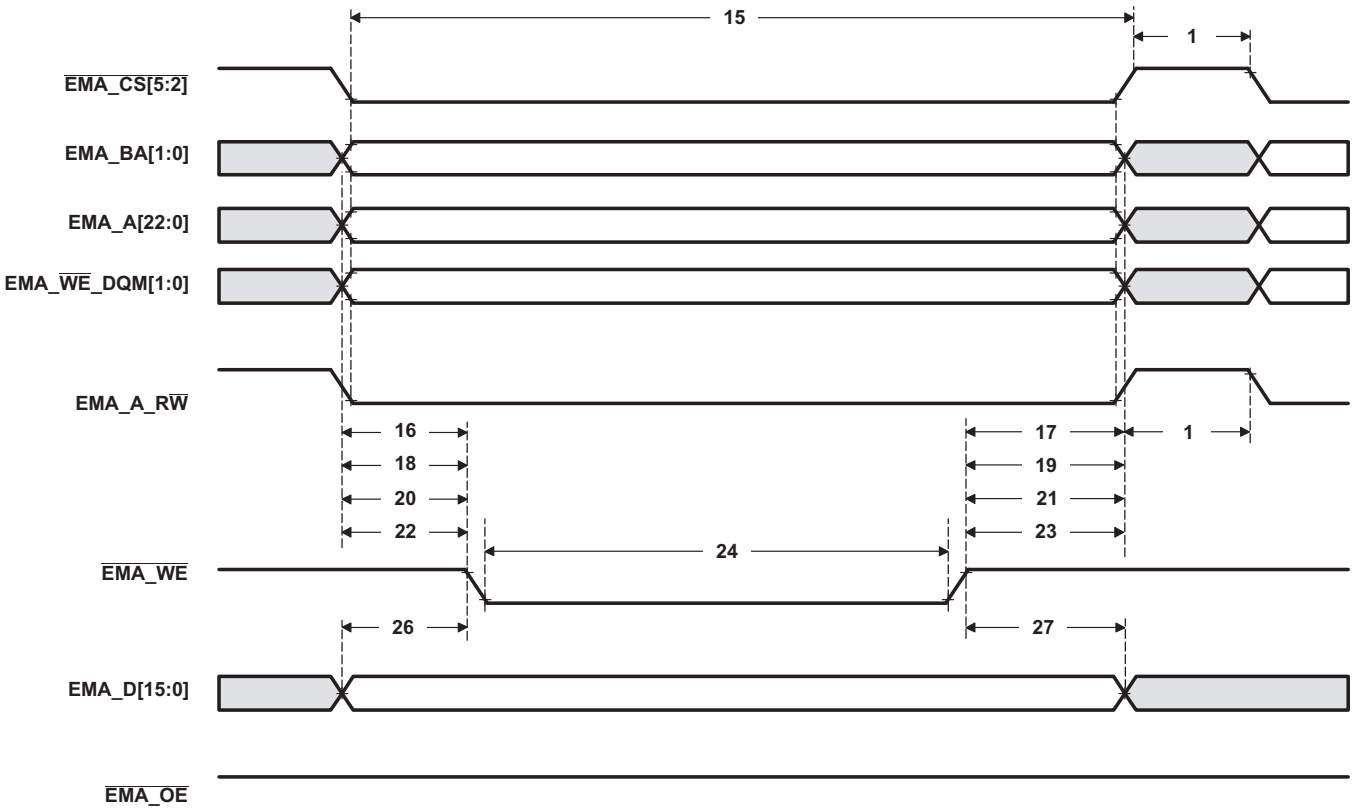

Figure 5-18. Asynchronous Memory Write Timing for EMIFA

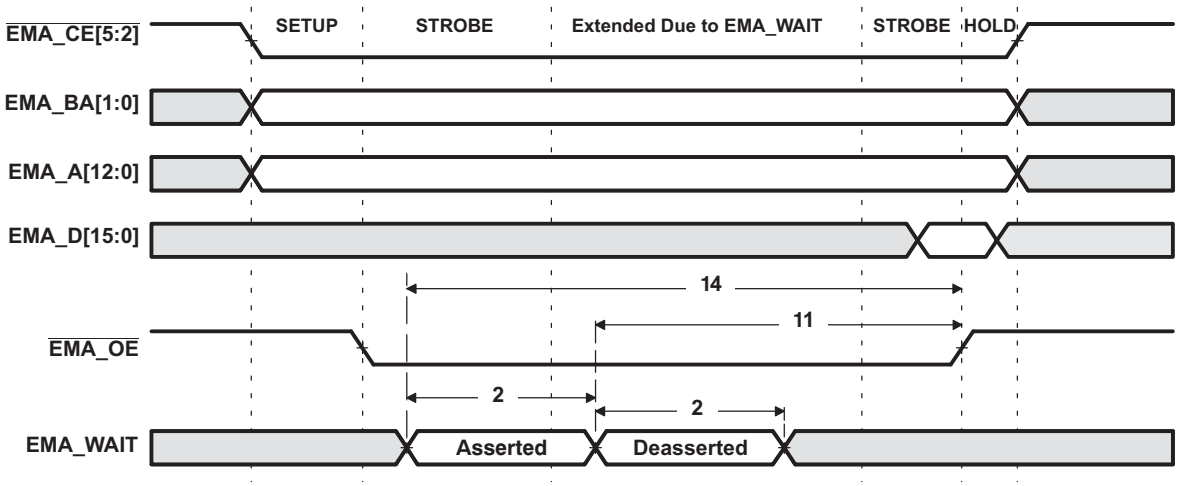

Figure 5-19. EMA_WAIT Read Timing Requirements

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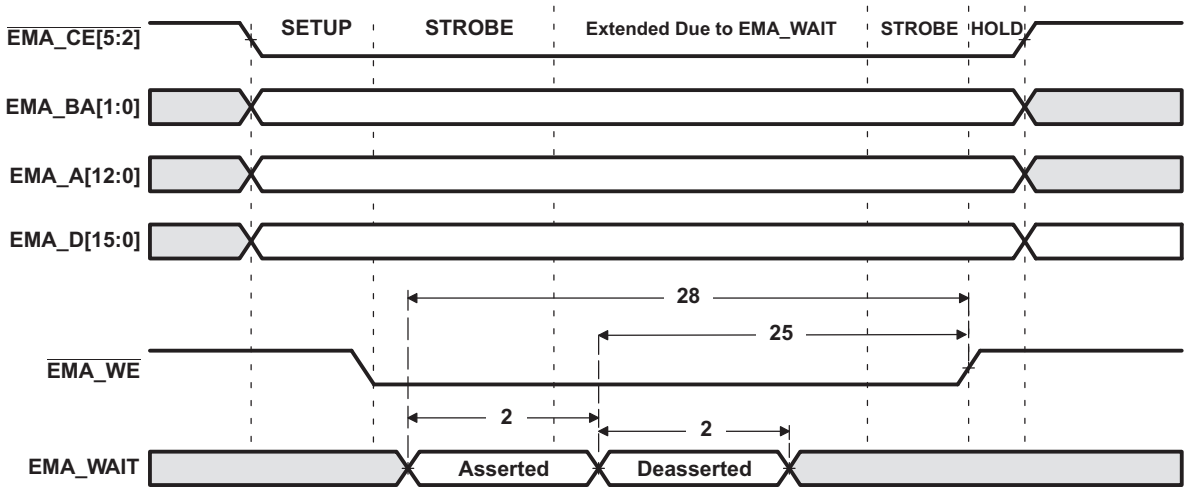

Figure 5-20. EMA_WAIT Write Timing Requirements

5.11 External Memory Interface B (EMIFB)

Figure 5-21, EMIFB Functional Block Diagram illustrates a high-level view of the EMIFB and its connections within the device. Multiple requesters have access to EMIFB through a switched central resource (indicated as crossbar in the figure). The EMIFB implements a split transaction internal bus, allowing concurrence between reads and writes from the various requesters. See the *TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.* – Literature Number SPRUFK9 for more details.

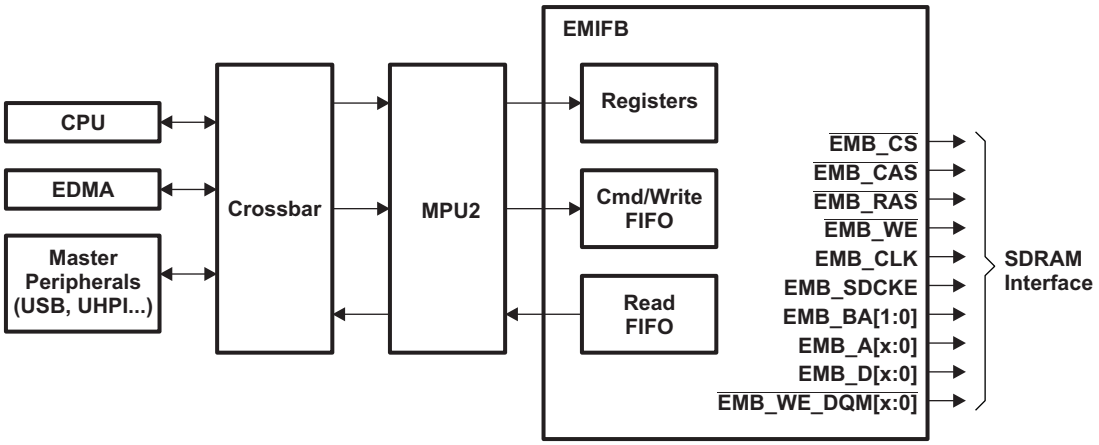

Figure 5-21. EMIFB Functional Block Diagram

EMIFB supports a 3.3V LVCMOS Interface.

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5.11.1 Interfacing to SDRAM

The EMIFB supports a glueless interface to SDRAM devices with the following characteristics:

- Pre-charge bit is A[10]
- The number of column address bits is 8, 9, 10 or 11
- The number of row address bits is 13 (in case of mobile SDR, number of row address bits can be 9, 10, 11, 12, or 13)
- The number of internal banks is 1, 2 or 4

Figure 5-22 shows an interface between the EMIFB and a 2M × 16 × 4 bank SDRAM device. In addition, Figure 5-23 shows an interface between the EMIFB and a 2M × 32 × 4 bank SDRAM device and Figure 5-24 shows an interface between the EMIFB and two 4M × 16 × 4 bank SDRAM devices. Refer to Table 5-25, as an example that shows additional list of commonly-supported SDRAM devices and the required connections for the address pins. Note that in Table 5-25, page size/column size (not indicated in the table) is varied to get the required addressability range.

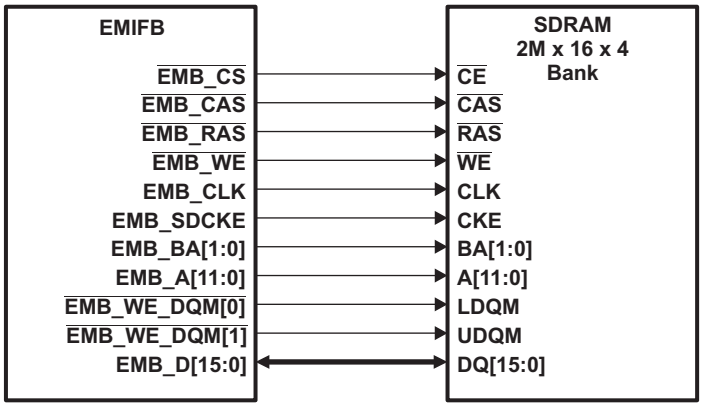

Figure 5-22. EMIFB to 2M × 16 × 4 bank SDRAM Interface

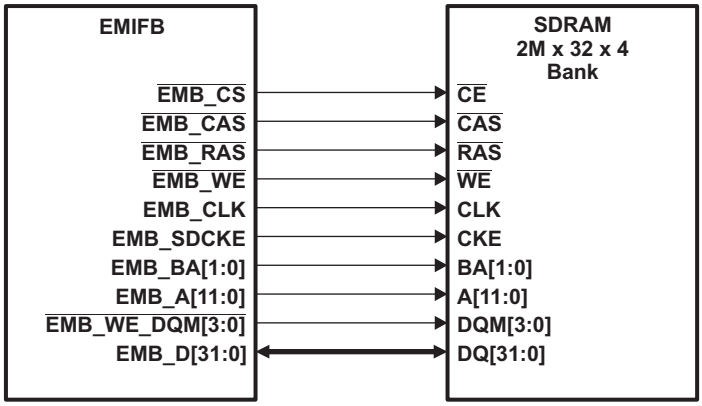

Figure 5-23. EMIFB to 2M × 32 × 4 bank SDRAM Interface

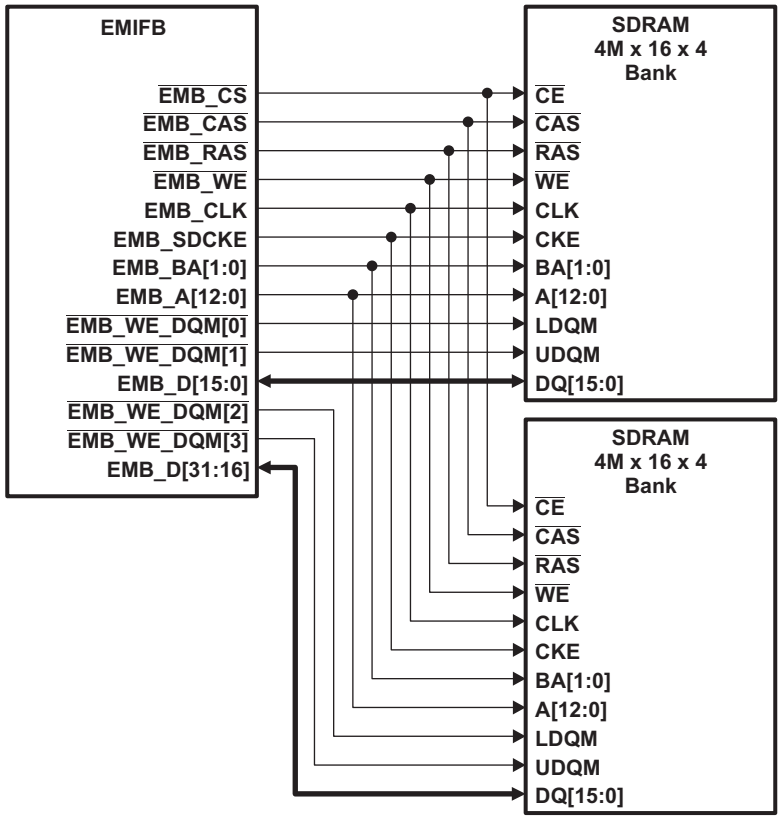

Figure 5-24. EMIFB to Dual 4M × 16 × 4 bank SDRAM Interface

Table 5-25. Example of 16/32-bit EMIFB Address Pin Connections

SDRAM Size	Width	Banks		Address Pins
64M bits	×16	4	SDRAM	A[11:0]
			EMIFB	EMB_A[11:0]
	×32	4	SDRAM	A[10:0]
			EMIFB	EMB_A[10:0]
128M bits	×16	4	SDRAM	A[11:0]
			EMIFB	EMB_A[11:0]
	×32	4	SDRAM	A[11:0]
			EMIFB	EMB_A[11:0]
256M bits	×16	4	SDRAM	A[12:0]
			EMIFB	EMB_A[12:0]
	×32	4	SDRAM	A[11:0]
			EMIFB	EMB_A[11:0]
512M bits	×16	4	SDRAM	A[12:0]
			EMIFB	EMB_A[12:0]
	×32	4	SDRAM	A[12:0]
			EMIFB	EMB_A[12:0]

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Table 5-26 is a list of the EMIFB registers.

Table 5-26. EMIFB Base Controller Registers

BYTE ADDRESS	Acronym	Register
0xB000 0000	MIDR	Module ID Register
0xB000 0008	SDCFG	SDRAM Configuration Register
0xB000 000C	SDRFC	SDRAM Refresh Control Register
0xB000 0010	SDTIM1	SDRAM Timing Register 1
0xB000 0014	SDTIM2	SDRAM Timing Register 2
0xB000 001C	SDCFG2	SDRAM Configuration 2 Register
0xB000 0020	BPRIO	Peripheral Bus Burst Priority Register
0xB000 0040	PC1	Performance Counter 1 Register
0xB000 0044	PC2	Performance Counter 2 Register
0xB000 0048	PCC	Performance Counter Configuration Register
0xB000 004C	PCMRS	Performance Counter Master Region Select Register
0xB000 0050	PCT	Performance Counter Time Register
0xB000 00C0	IRR	Interrupt Raw Register
0xB000 00C4	IMR	Interrupt Mask Register
0xB000 00C8	IMSR	Interrupt Mask Set Register
0xB000 00CC	IMCR	Interrupt Mask Clear Register

5.11.2 EMIFB Electrical Data/Timing

Table 5-27. EMIFB SDRAM Interface Timing Requirements

NO.			MIN	MAX	UNIT
19	$t_{su(DV-CLKH)}$	Input setup time, read data valid on EMB_D[31:0] before EMB_CLK rising	0.8		ns
20	$t_{h(CLKH-DIV)}$	Input hold time, read data valid on EMB_D[31:0] after EMB_CLK rising	1.6		ns

Table 5-28. EMIFB SDRAM Interface Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
1(1)	$t_{c(CLK)}$	Cycle time, EMIF clock EMB_CLK	7.5		ns
2(1)	$t_{w(CLK)}$	Pulse width, EMIF clock EMB_CLK high or low	3		ns
3	$t_{d(CLKH-CSV)}$	Delay time, EMB_CLK rising to $\overline{\text{EMB_CS[0]}}$ valid		7	ns
4	$t_{oh(CLKH-CSIV)}$	Output hold time, EMB_CLK rising to $\overline{\text{EMB_CS[0]}}$ invalid	0.9		ns
5	$t_{d(CLKH-DQMV)}$	Delay time, EMB_CLK rising to EMB_$\overline{\text{WE}}$_DQM[3:0] valid		7	ns
6	$t_{oh(CLKH-DQMIV)}$	Output hold time, EMB_CLK rising to EMB_$\overline{\text{WE}}$_DQM[3:0] invalid	0.9		ns
7	$t_{d(CLKH-AV)}$	Delay time, EMB_CLK rising to EMB_A[12:0] and EMB_BA[1:0] valid		7	ns
8	$t_{oh(CLKH-AIV)}$	Output hold time, EMB_CLK rising to EMB_A[12:0] and EMB_BA[1:0] invalid	0.9		ns
9	$t_{d(CLKH-DV)}$	Delay time, EMB_CLK rising to EMB_D[31:0] valid		7	ns
10	$t_{oh(CLKH-DIV)}$	Output hold time, EMB_CLK rising to EMB_D[31:0] invalid	0.9		ns
11	$t_{d(CLKH-RASV)}$	Delay time, EMB_CLK rising to $\overline{\text{EMB_RAS}}$ valid		7	ns
12	$t_{oh(CLKH-RASIV)}$	Output hold time, EMB_CLK rising to $\overline{\text{EMB_RAS}}$ invalid	0.9		ns
13	$t_{d(CLKH-CASV)}$	Delay time, EMB_CLK rising to $\overline{\text{EMB_CAS}}$ valid		7	ns
14	$t_{oh(CLKH-CASIV)}$	Output hold time, EMB_CLK rising to $\overline{\text{EMB_CAS}}$ invalid	0.9		ns

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.

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Table 5-28. EMIFB SDRAM Interface Switching Characteristics (continued)

NO.	PARAMETER		MIN	MAX	UNIT
15	$t_{d(CLKH-WEV)}$	Delay time, EMB_CLK rising to $\overline{\text{EMB_WE}}$ valid		7	ns
16	$t_{oh(CLKH-WEIV)}$	Output hold time, EMB_CLK rising to $\overline{\text{EMB_WE}}$ invalid	0.9		ns
17	$t_{dis(CLKH-DHZ)}$	Delay time, EMB_CLK rising to EMB_D[31:0] tri-stated		7	ns
18	$t_{ena(CLKH-DLZ)}$	Output hold time, EMB_CLK rising to EMB_D[31:0] driving	0.9		ns

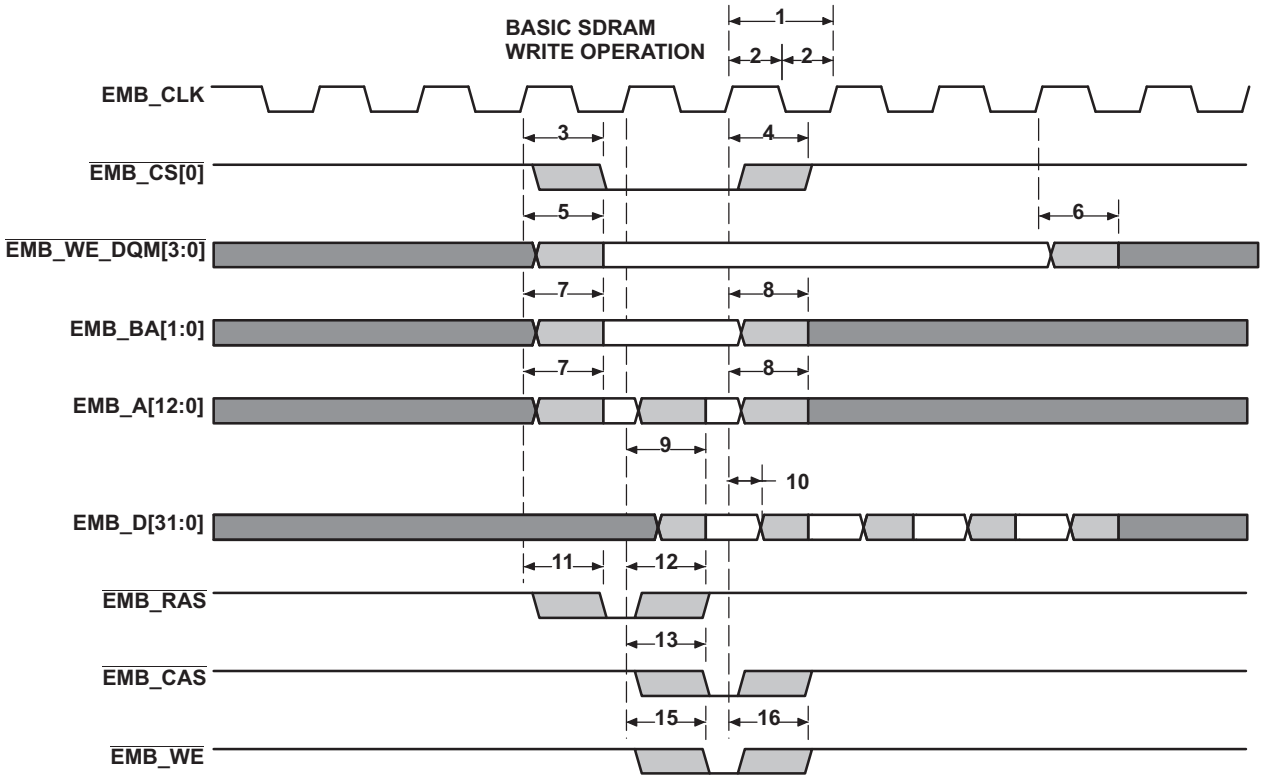

Figure 5-25. EMIFB Basic SDRAM Write Operation

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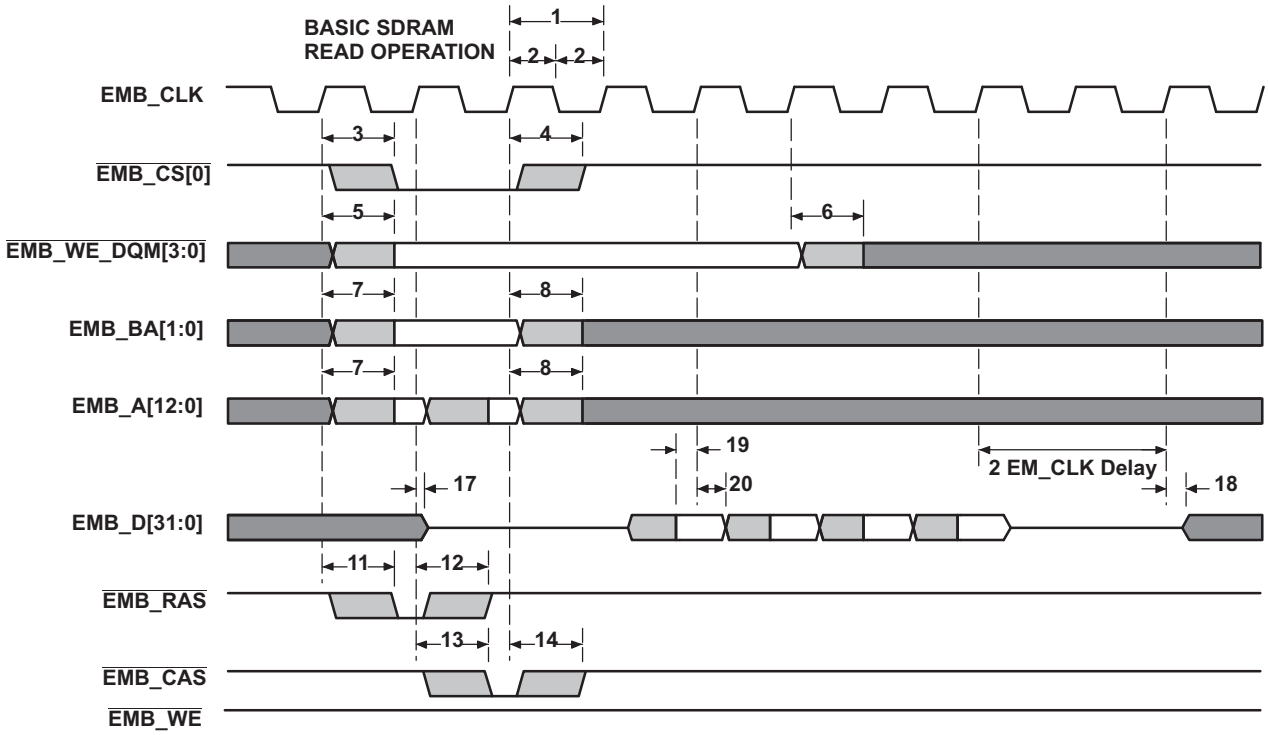

Figure 5-26. EMIFB Basic SDRAM Read Operation

5.12 MMC / SD / SDIO (MMCSD)

5.12.1 MMCSD Peripheral Description

The device includes an MMCSD controller which are compliant with MMC V3.31, Secure Digital Part 1 Physical Layer Specification V1.1 and Secure Digital Input Output (SDIO) V2.0 specifications.

The device MMC/SD Controller has following features:

- MultiMediaCard (MMC).
- Secure Digital (SD) Memory Card.
- MMC/SD protocol support.
- SDIO protocol support.
- Programmable clock frequency.
- 512 bit Read/Write FIFO to lower system overhead.
- Slave EDMA transfer capability.
- SD high capacity support.

The MMC/SD Controller does not support SPI mode. See the *TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.* – Literature Number SPRUFK9 for more details.

5.12.2 MMCSD Peripheral Register Description(s)

Table 5-29. Multimedia Card/Secure Digital (MMC/SD) Card Controller Registers

Offset	Acronym	Register Description
0x01C4 0000	MMCCTL	MMC Control Register
0x01C4 0004	MMCCLK	MMC Memory Clock Control Register
0x01C4 0008	MMCST0	MMC Status Register 0
0x01C4 000C	MMCST1	MMC Status Register 1
0x01C4 0010	MMCIM	MMC Interrupt Mask Register
0x01C4 0014	MMCTOR	MMC Response Time-Out Register
0x01C4 0018	MMCTOD	MMC Data Read Time-Out Register
0x01C4 001C	MMCBLEN	MMC Block Length Register
0x01C4 0020	MMCNBLK	MMC Number of Blocks Register
0x01C4 0024	MMCNBLC	MMC Number of Blocks Counter Register
0x01C4 0028	MMCDRR	MMC Data Receive Register
0x01C4 002C	MMCDXR	MMC Data Transmit Register
0x01C4 0030	MMCCMD	MMC Command Register
0x01C4 0034	MMCARGHL	MMC Argument Register
0x01C4 0038	MMCRSP01	MMC Response Register 0 and 1
0x01C4 003C	MMCRSP23	MMC Response Register 2 and 3
0x01C4 0040	MMCRSP45	MMC Response Register 4 and 5
0x01C4 0044	MMCRSP67	MMC Response Register 6 and 7
0x01C4 0048	MMCDRSP	MMC Data Response Register
0x01C4 0050	MMCCIDX	MMC Command Index Register
0x01C4 0064	SDIOCTL	SDIO Control Register
0x01C4 0068	SDIOST0	SDIO Status Register 0
0x01C4 006C	SDIOIEN	SDIO Interrupt Enable Register
0x01C4 0070	SDIOIST	SDIO Interrupt Status Register
0x01C4 0074	MMCFIFOCTL	MMC FIFO Control Register

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5.12.3 MMC/SD Electrical Data/Timing

Table 5-30. Timing Requirements for MMC/SD Module(1)

NO.			MIN	MAX	UNIT
1	$t_{su(CMDV-CLKH)}$	Setup time, MMCSD_CMD valid before MMCSD_CLK high	3.2		ns
2	$t_{h(CLKH-CMDV)}$	Hold time, MMCSD_CMD valid after MMCSD_CLK high	1.5		ns
3	$t_{su(DATV-CLKH)}$	Setup time, MMCSD_DATx valid before MMCSD_CLK high	3.2		ns
4	$t_{h(CLKH-DATV)}$	Hold time, MMCSD_DATx valid after MMCSD_CLK high	1.5		ns

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.

Table 5-31. Switching Characteristics Over Recommended Operating Conditions for MMC/SD Module(1)

NO.	PARAMETER		MIN	MAX	UNIT
7	$f_{(CLK)}$	Operating frequency, MMCSD_CLK	0	52	MHz
8	$f_{(CLK_ID)}$	Identification mode frequency, MMCSD_CLK	0	400	KHz
9	$t_{W(CLKL)}$	Pulse width, MMCSD_CLK low	6.5		ns
10	$t_{W(CLKH)}$	Pulse width, MMCSD_CLK high	6.5		ns
11	$t_{r(CLK)}$	Rise time, MMCSD_CLK		3	ns
12	$t_{f(CLK)}$	Fall time, MMCSD_CLK		3	ns
13	$t_{d(CLKL-CMD)}$	Delay time, MMCSD_CLK low to MMCSD_CMD transition	-4.5	2.5	ns
14	$t_{d(CLKL-DAT)}$	Delay time, MMCSD_CLK low to MMCSD_DATx transition	-4.5	2.5	ns

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.

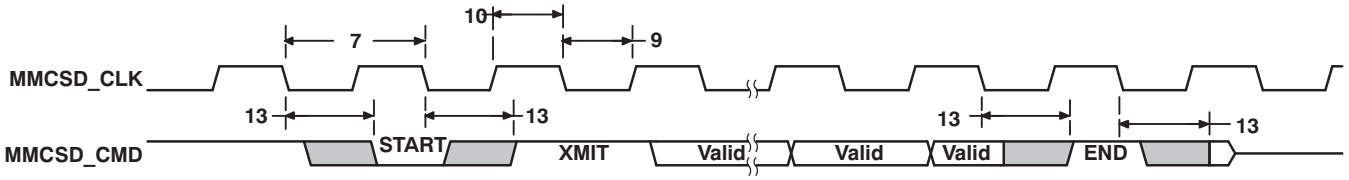

Figure 5-27. MMC/SD Host Command Timing

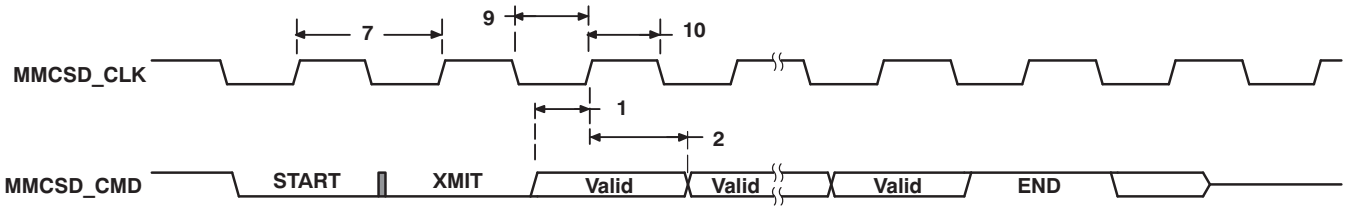

Figure 5-28. MMC/SD Card Response Timing

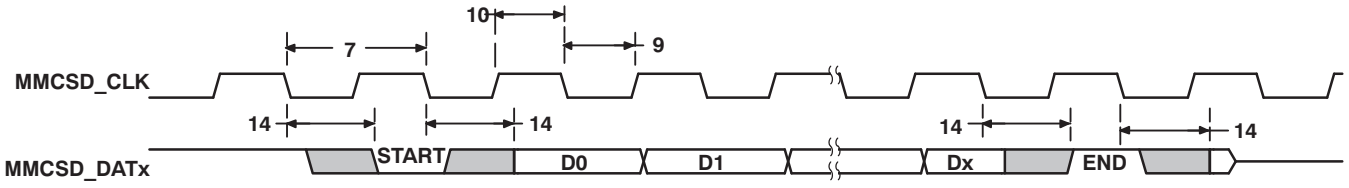

Figure 5-29. MMC/SD Host Write Timing

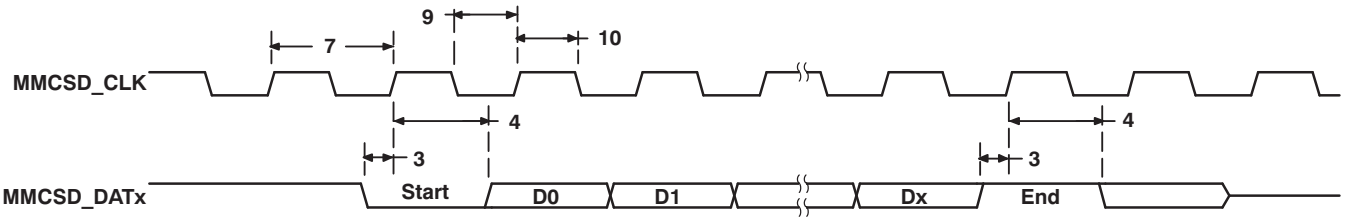

Figure 5-30. MMC/SD Host Read and Card CRC Status Timing

5.13 Ethernet Media Access Controller (EMAC)

The Ethernet Media Access Controller (EMAC) provides an efficient interface between device and the network. The device EMAC supports both 10Base-T and 100Base-TX, or 10 Mbits/second (Mbps) and 100 Mbps in either half- or full-duplex mode, with hardware flow control and quality of service (QOS) support.

The EMAC controls the flow of packet data from the device to the PHY. The MDIO module controls PHY configuration and status monitoring.

Both the EMAC and the MDIO modules interface to the device through a custom interface that allows efficient data transmission and reception. This custom interface is referred to as the EMAC control module, and is considered integral to the EMAC/MDIO peripheral. The control module is also used to multiplex and control interrupts. See the *TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.* – Literature Number SPRUFK9 for more details.

5.13.1 EMAC Peripheral Register Description(s)

Table 5-32. Ethernet Media Access Controller (EMAC) Registers

BYTE ADDRESS	REGISTER	Register Description
0x01E2 3000	TXREV	Transmit Revision Register
0x01E2 3004	TXCONTROL	Transmit Control Register
0x01E2 3008	TXTEARDOWN	Transmit Teardown Register
0x01E2 3010	RXREV	Receive Revision Register
0x01E2 3014	RXCONTROL	Receive Control Register
0x01E2 3018	RXTEARDOWN	Receive Teardown Register
0x01E2 3080	TXINTSTATRAW	Transmit Interrupt Status (Unmasked) Register
0x01E2 3084	TXINTSTATMASKED	Transmit Interrupt Status (Masked) Register
0x01E2 3088	TXINTMASKSET	Transmit Interrupt Mask Set Register
0x01E2 308C	TXINTMASKCLEAR	Transmit Interrupt Clear Register
0x01E2 3090	MACINVECTOR	MAC Input Vector Register
0x01E2 3094	MACEOIVECTOR	MAC End Of Interrupt Vector Register
0x01E2 30A0	RXINTSTATRAW	Receive Interrupt Status (Unmasked) Register
0x01E2 30A4	RXINTSTATMASKED	Receive Interrupt Status (Masked) Register
0x01E2 30A8	RXINTMASKSET	Receive Interrupt Mask Set Register
0x01E2 30AC	RXINTMASKCLEAR	Receive Interrupt Mask Clear Register
0x01E2 30B0	MACINTSTATRAW	MAC Interrupt Status (Unmasked) Register
0x01E2 30B4	MACINTSTATMASKED	MAC Interrupt Status (Masked) Register
0x01E2 30B8	MACINTMASKSET	MAC Interrupt Mask Set Register
0x01E2 30BC	MACINTMASKCLEAR	MAC Interrupt Mask Clear Register
0x01E2 3100	RXMBPENABLE	Receive Multicast/Broadcast/Promiscuous Channel Enable Register
0x01E2 3104	RXUNICASTSET	Receive Unicast Enable Set Register
0x01E2 3108	RXUNICASTCLEAR	Receive Unicast Clear Register
0x01E2 310C	RXMAXLEN	Receive Maximum Length Register

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Table 5-32. Ethernet Media Access Controller (EMAC) Registers (continued)

BYTE ADDRESS	REGISTER	Register Description
0x01E2 3110	RXBUFFEROFFSET	Receive Buffer Offset Register
0x01E2 3114	RXFILTERLOWTHRESH	Receive Filter Low Priority Frame Threshold Register
0x01E2 3120	RX0FLOWTHRESH	Receive Channel 0 Flow Control Threshold Register
0x01E2 3124	RX1FLOWTHRESH	Receive Channel 1 Flow Control Threshold Register
0x01E2 3128	RX2FLOWTHRESH	Receive Channel 2 Flow Control Threshold Register
0x01E2 312C	RX3FLOWTHRESH	Receive Channel 3 Flow Control Threshold Register
0x01E2 3130	RX4FLOWTHRESH	Receive Channel 4 Flow Control Threshold Register
0x01E2 3134	RX5FLOWTHRESH	Receive Channel 5 Flow Control Threshold Register
0x01E2 3138	RX6FLOWTHRESH	Receive Channel 6 Flow Control Threshold Register
0x01E2 313C	RX7FLOWTHRESH	Receive Channel 7 Flow Control Threshold Register
0x01E2 3140	RX0FREEBUFFER	Receive Channel 0 Free Buffer Count Register
0x01E2 3144	RX1FREEBUFFER	Receive Channel 1 Free Buffer Count Register
0x01E2 3148	RX2FREEBUFFER	Receive Channel 2 Free Buffer Count Register
0x01E2 314C	RX3FREEBUFFER	Receive Channel 3 Free Buffer Count Register
0x01E2 3150	RX4FREEBUFFER	Receive Channel 4 Free Buffer Count Register
0x01E2 3154	RX5FREEBUFFER	Receive Channel 5 Free Buffer Count Register
0x01E2 3158	RX6FREEBUFFER	Receive Channel 6 Free Buffer Count Register
0x01E2 315C	RX7FREEBUFFER	Receive Channel 7 Free Buffer Count Register
0x01E2 3160	MACCONTROL	MAC Control Register
0x01E2 3164	MACSTATUS	MAC Status Register
0x01E2 3168	EMCONTROL	Emulation Control Register
0x01E2 316C	FIFOCONTROL	FIFO Control Register
0x01E2 3170	MACCONFIG	MAC Configuration Register
0x01E2 3174	SOFTRESET	Soft Reset Register
0x01E2 31D0	MACSRCADDRLO	MAC Source Address Low Bytes Register
0x01E2 31D4	MACSRCADDRHI	MAC Source Address High Bytes Register
0x01E2 31D8	MACHASH1	MAC Hash Address Register 1
0x01E2 31DC	MACHASH2	MAC Hash Address Register 2
0x01E2 31E0	BOFFTEST	Back Off Test Register
0x01E2 31E4	TPACETEST	Transmit Pacing Algorithm Test Register
0x01E2 31E8	RXPAUSE	Receive Pause Timer Register
0x01E2 31EC	TXPAUSE	Transmit Pause Timer Register
0x01E2 3200 - 0x01E2 32FC	(see Table 5-33)	EMAC Statistics Registers
0x01E2 3500	MACADDRLO	MAC Address Low Bytes Register, Used in Receive Address Matching
0x01E2 3504	MACADDRHI	MAC Address High Bytes Register, Used in Receive Address Matching
0x01E2 3508	MACINDEX	MAC Index Register
0x01E2 3600	TX0HDP	Transmit Channel 0 DMA Head Descriptor Pointer Register
0x01E2 3604	TX1HDP	Transmit Channel 1 DMA Head Descriptor Pointer Register
0x01E2 3608	TX2HDP	Transmit Channel 2 DMA Head Descriptor Pointer Register
0x01E2 360C	TX3HDP	Transmit Channel 3 DMA Head Descriptor Pointer Register
0x01E2 3610	TX4HDP	Transmit Channel 4 DMA Head Descriptor Pointer Register
0x01E2 3614	TX5HDP	Transmit Channel 5 DMA Head Descriptor Pointer Register
0x01E2 3618	TX6HDP	Transmit Channel 6 DMA Head Descriptor Pointer Register
0x01E2 361C	TX7HDP	Transmit Channel 7 DMA Head Descriptor Pointer Register
0x01E2 3620	RX0HDP	Receive Channel 0 DMA Head Descriptor Pointer Register
0x01E2 3624	RX1HDP	Receive Channel 1 DMA Head Descriptor Pointer Register
0x01E2 3628	RX2HDP	Receive Channel 2 DMA Head Descriptor Pointer Register

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Table 5-32. Ethernet Media Access Controller (EMAC) Registers (continued)

BYTE ADDRESS	REGISTER	Register Description
0x01E2 362C	RX3HDP	Receive Channel 3 DMA Head Descriptor Pointer Register
0x01E2 3630	RX4HDP	Receive Channel 4 DMA Head Descriptor Pointer Register
0x01E2 3634	RX5HDP	Receive Channel 5 DMA Head Descriptor Pointer Register
0x01E2 3638	RX6HDP	Receive Channel 6 DMA Head Descriptor Pointer Register
0x01E2 363C	RX7HDP	Receive Channel 7 DMA Head Descriptor Pointer Register
0x01E2 3640	TX0CP	Transmit Channel 0 Completion Pointer Register
0x01E2 3644	TX1CP	Transmit Channel 1 Completion Pointer Register
0x01E2 3648	TX2CP	Transmit Channel 2 Completion Pointer Register
0x01E2 364C	TX3CP	Transmit Channel 3 Completion Pointer Register
0x01E2 3650	TX4CP	Transmit Channel 4 Completion Pointer Register
0x01E2 3654	TX5CP	Transmit Channel 5 Completion Pointer Register
0x01E2 3658	TX6CP	Transmit Channel 6 Completion Pointer Register
0x01E2 365C	TX7CP	Transmit Channel 7 Completion Pointer Register
0x01E2 3660	RX0CP	Receive Channel 0 Completion Pointer Register
0x01E2 3664	RX1CP	Receive Channel 1 Completion Pointer Register
0x01E2 3668	RX2CP	Receive Channel 2 Completion Pointer Register
0x01E2 366C	RX3CP	Receive Channel 3 Completion Pointer Register
0x01E2 3670	RX4CP	Receive Channel 4 Completion Pointer Register
0x01E2 3674	RX5CP	Receive Channel 5 Completion Pointer Register
0x01E2 3678	RX6CP	Receive Channel 6 Completion Pointer Register
0x01E2 367C	RX7CP	Receive Channel 7 Completion Pointer Register

Table 5-33. EMAC Statistics Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01E2 3200	RXGOODFRAMES	Good Receive Frames Register
0x01E2 3204	RXBCASTFRAMES	Broadcast Receive Frames Register (Total number of good broadcast frames received)
0x01E2 3208	RXMCASTFRAMES	Multicast Receive Frames Register (Total number of good multicast frames received)
0x01E2 320C	RXPAUSEFRAMES	Pause Receive Frames Register
0x01E2 3210	RXCRCERRORS	Receive CRC Errors Register (Total number of frames received with CRC errors)
0x01E2 3214	RXALIGNCODEERRORS	Receive Alignment/Code Errors Register (Total number of frames received with alignment/code errors)
0x01E2 3218	RXOVERSIZED	Receive Oversized Frames Register (Total number of oversized frames received)
0x01E2 321C	RXJABBER	Receive Jabber Frames Register (Total number of jabber frames received)
0x01E2 3220	RXUNDERSIZED	Receive Undersized Frames Register (Total number of undersized frames received)
0x01E2 3224	RXFRAGMENTS	Receive Frame Fragments Register
0x01E2 3228	RXFILTERED	Filtered Receive Frames Register
0x01E2 322C	RXQOSFILTERED	Received QOS Filtered Frames Register
0x01E2 3230	RXOCTETS	Receive Octet Frames Register (Total number of received bytes in good frames)
0x01E2 3234	TXGOODFRAMES	Good Transmit Frames Register (Total number of good frames transmitted)
0x01E2 3238	TXBCASTFRAMES	Broadcast Transmit Frames Register
0x01E2 323C	TXMCASTFRAMES	Multicast Transmit Frames Register
0x01E2 3240	TXPAUSEFRAMES	Pause Transmit Frames Register

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Table 5-33. EMAC Statistics Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01E2 3244	TXDEFERRED	Deferred Transmit Frames Register
0x01E2 3248	TXCOLLISION	Transmit Collision Frames Register
0x01E2 324C	TXSINGLECOLL	Transmit Single Collision Frames Register
0x01E2 3250	TXMULTICOLL	Transmit Multiple Collision Frames Register
0x01E2 3254	TXEXCESSIVECOLL	Transmit Excessive Collision Frames Register
0x01E2 3258	TXLATECOLL	Transmit Late Collision Frames Register
0x01E2 325C	TXUNDERRUN	Transmit Underrun Error Register
0x01E2 3260	TXCARRIERSENSE	Transmit Carrier Sense Errors Register
0x01E2 3264	TXOCTETS	Transmit Octet Frames Register
0x01E2 3268	FRAME64	Transmit and Receive 64 Octet Frames Register
0x01E2 326C	FRAME65T127	Transmit and Receive 65 to 127 Octet Frames Register
0x01E2 3270	FRAME128T255	Transmit and Receive 128 to 255 Octet Frames Register
0x01E2 3274	FRAME256T511	Transmit and Receive 256 to 511 Octet Frames Register
0x01E2 3278	FRAME512T1023	Transmit and Receive 512 to 1023 Octet Frames Register
0x01E2 327C	FRAME1024TUP	Transmit and Receive 1024 to 1518 Octet Frames Register
0x01E2 3280	NETOCTETS	Network Octet Frames Register
0x01E2 3284	RXSOFOVERRUNS	Receive FIFO or DMA Start of Frame Overruns Register
0x01E2 3288	RXMOFOVERRUNS	Receive FIFO or DMA Middle of Frame Overruns Register
0x01E2 328C	RXDMAOVERRUNS	Receive DMA Start of Frame and Middle of Frame Overruns Register

Table 5-34. EMAC Control Module Registers

BYTE ADDRESS	Acronym	Register Description
0x01E2 2000	REV	EMAC Control Module Revision Register
0x01E2 2004	SOFTRESET	EMAC Control Module Software Reset Register
0x01E2 200C	INTCONTROL	EMAC Control Module Interrupt Control Register
0x01E2 2010	C0RXTHRESHEN	EMAC Control Module Interrupt Core 0 Receive Threshold Interrupt Enable Register
0x01E2 2014	C0RXEN	EMAC Control Module Interrupt Core 0 Receive Interrupt Enable Register
0x01E2 2018	C0TXEN	EMAC Control Module Interrupt Core 0 Transmit Interrupt Enable Register
0x01E2 201C	C0MISCEN	EMAC Control Module Interrupt Core 0 Miscellaneous Interrupt Enable Register
0x01E2 2020	C1RXTHRESHEN	EMAC Control Module Interrupt Core 1 Receive Threshold Interrupt Enable Register
0x01E2 2024	C1RXEN	EMAC Control Module Interrupt Core 1 Receive Interrupt Enable Register
0x01E2 2028	C1TXEN	EMAC Control Module Interrupt Core 1 Transmit Interrupt Enable Register
0x01E2 202C	C1MISCEN	EMAC Control Module Interrupt Core 1 Miscellaneous Interrupt Enable Register
0x01E2 2030	C2RXTHRESHEN	EMAC Control Module Interrupt Core 2 Receive Threshold Interrupt Enable Register
0x01E2 2034	C2RXEN	EMAC Control Module Interrupt Core 2 Receive Interrupt Enable Register
0x01E2 2038	C2TXEN	EMAC Control Module Interrupt Core 2 Transmit Interrupt Enable Register
0x01E2 203C	C2MISCEN	EMAC Control Module Interrupt Core 2 Miscellaneous Interrupt Enable Register
0x01E2 2040	C0RXTHRESHSTAT	EMAC Control Module Interrupt Core 0 Receive Threshold Interrupt Status Register
0x01E2 2044	C0RXSTAT	EMAC Control Module Interrupt Core 0 Receive Interrupt Status Register
0x01E2 2048	C0TXSTAT	EMAC Control Module Interrupt Core 0 Transmit Interrupt Status Register
0x01E2 204C	C0MISCSTAT	EMAC Control Module Interrupt Core 0 Miscellaneous Interrupt Status Register

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Table 5-34. EMAC Control Module Registers (continued)

BYTE ADDRESS	Acronym	Register Description
0x01E2 2050	C1RXTHRESHSTAT	EMAC Control Module Interrupt Core 1 Receive Threshold Interrupt Status Register
0x01E2 2054	C1RXSTAT	EMAC Control Module Interrupt Core 1 Receive Interrupt Status Register
0x01E2 2058	C1TXSTAT	EMAC Control Module Interrupt Core 1 Transmit Interrupt Status Register
0x01E2 205C	C1MISCSTAT	EMAC Control Module Interrupt Core 1 Miscellaneous Interrupt Status Register
0x01E2 2060	C2RXTHRESHSTAT	EMAC Control Module Interrupt Core 2 Receive Threshold Interrupt Status Register
0x01E2 2064	C2RXSTAT	EMAC Control Module Interrupt Core 2 Receive Interrupt Status Register
0x01E2 2068	C2TXSTAT	EMAC Control Module Interrupt Core 2 Transmit Interrupt Status Register
0x01E2 206C	C2MISCSTAT	EMAC Control Module Interrupt Core 2 Miscellaneous Interrupt Status Register
0x01E2 2070	C0RXIMAX	EMAC Control Module Interrupt Core 0 Receive Interrupts Per Millisecond Register
0x01E2 2074	C0TXIMAX	EMAC Control Module Interrupt Core 0 Transmit Interrupts Per Millisecond Register
0x01E2 2078	C1RXIMAX	EMAC Control Module Interrupt Core 1 Receive Interrupts Per Millisecond Register
0x01E2 207C	C1TXIMAX	EMAC Control Module Interrupt Core 1 Transmit Interrupts Per Millisecond Register
0x01E2 2080	C2RXIMAX	EMAC Control Module Interrupt Core 2 Receive Interrupts Per Millisecond Register
0x01E2 2084	C2TXIMAX	EMAC Control Module Interrupt Core 2 Transmit Interrupts Per Millisecond Register

Table 5-35. EMAC Control Module RAM

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01E2 0000 - 0x01E2 1FFF		EMAC Local Buffer Descriptor Memory

Table 5-36. RMII Timing Requirements

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1(1)	tc(RMII_MHZ_50_CLK)	Cycle Time, RMII_MHZ_50_CLK		20		ns
2(1)	tw(RMII_MHZ_50_CLKH)	Pulse Width, RMII_MHZ_50_CLK High	7		13	ns
3(1)	tw(RMII_MHZ_50_CLKL)	Pulse Width, RMII_MHZ_50_CLK Low	7		13	ns
6	tsu(RXD-RMII_MHZ_50_CLK)	Input Setup Time, RXD Valid before RMII_MHZ_50_CLK High	4.5			ns
7	th(RMII_MHZ_50_CLK-RXD)	Input Hold Time, RXD Valid after RMII_MHZ_50_CLK High	2.1			ns
8	tsu(CRSDV-RMII_MHZ_50_CLK)	Input Setup Time, CRSDV Valid before RMII_MHZ_50_CLK High	4.5			ns
9	th(RMII_MHZ_50_CLK-CRSDV)	Input Hold Time, CRSDV Valid after RMII_MHZ_50_CLK High	2.1			ns
10	tsu(RXER-RMII_MHZ_50_CLK)	Input Setup Time, RXER Valid before RMII_MHZ_50_CLK High	4.5			ns
11	th(RMII_MHZ_50_CLK-RXER)	Input Hold Time, RXER Valid after RMII_MHZ_50_CLK High	2.1			ns

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.

Table 5-37. RMII Timing Requirements

NO.	PARAMETER		MIN	TYP	MAX	UNIT
4	td(RMII_MHZ_50_CLK-TXD)	Output Delay Time, RMII_MHZ_50_CLKHigh to TXD Valid	1.8		14	ns

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Table 5-37. RMII Timing Requirements (continued)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
5	td(RMII_MHZ_50_CLK-TXEN)	Output Delay Time, RMII_MHZ_50_CLK High to TXEN Valid	1.8		14	ns

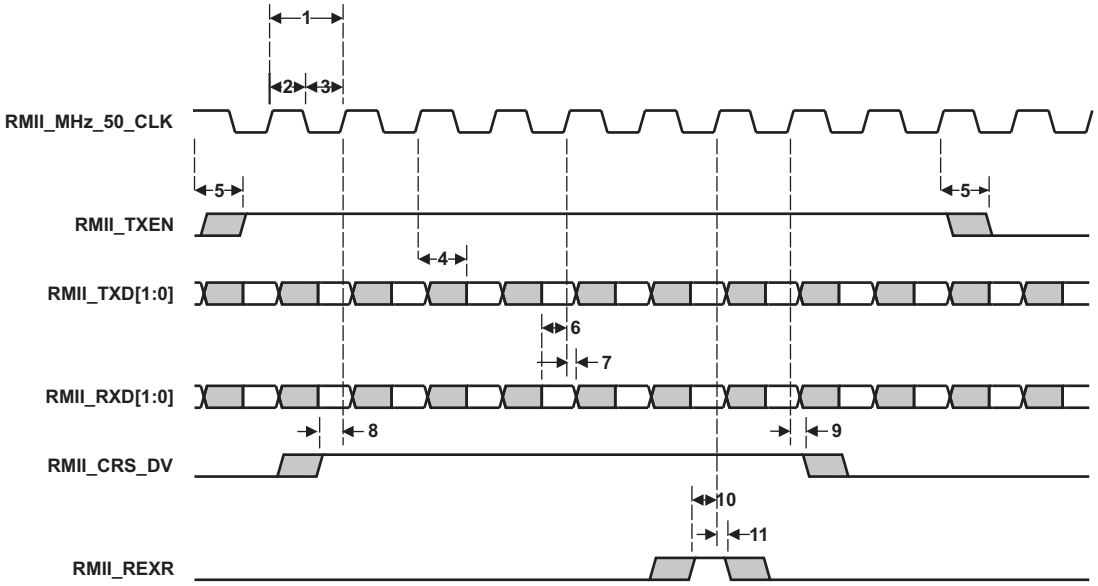

Figure 5-31. RMII Timing Diagram

5.14 Management Data Input/Output (MDIO)

The Management Data Input/Output (MDIO) module continuously polls all 32 MDIO addresses in order to enumerate all PHY devices in the system.

The Management Data Input/Output (MDIO) module implements the 802.3 serial management interface to interrogate and control Ethernet PHY(s) using a shared two-wire bus. Host software uses the MDIO module to configure the auto-negotiation parameters of each PHY attached to the EMAC, retrieve the negotiation results, and configure required parameters in the EMAC module for correct operation. The module is designed to allow almost transparent operation of the MDIO interface, with very little maintenance from the core processor. Only one PHY may be connected at any given time. See the *TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.* – Literature Number SPRUFK9 for more details.

5.14.1 MDIO Registers

For a list of supported MDIO registers see Table 5-38 [MDIO Registers].

Table 5-38. MDIO Register Memory Map

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0x01E2 4000	REV	Revision Identification Register
0x01E2 4004	CONTROL	MDIO Control Register
0x01E2 4008	ALIVE	MDIO PHY Alive Status Register
0x01E2 400C	LINK	MDIO PHY Link Status Register
0x01E2 4010	LINKINTRAW	MDIO Link Status Change Interrupt (Unmasked) Register
0x01E2 4014	LINKINTMASKED	MDIO Link Status Change Interrupt (Masked) Register
0x01E2 4018	–	Reserved
0x01E2 4020	USERINTRAW	MDIO User Command Complete Interrupt (Unmasked) Register
0x01E2 4024	USERINTMASKED	MDIO User Command Complete Interrupt (Masked) Register
0x01E2 4028	USERINTMASKSET	MDIO User Command Complete Interrupt Mask Set Register
0x01E2 402C	USERINTMASKCLEAR	MDIO User Command Complete Interrupt Mask Clear Register
0x01E2 4030 - 0x01E2 407C	–	Reserved
0x01E2 4080	USERACCESS0	MDIO User Access Register 0
0x01E2 4084	USERPHYSEL0	MDIO User PHY Select Register 0
0x01E2 4088	USERACCESS1	MDIO User Access Register 1
0x01E2 408C	USERPHYSEL1	MDIO User PHY Select Register 1
0x01E2 4090 - 0x01E2 47FF	–	Reserved

5.14.2 Management Data Input/Output (MDIO) Electrical Data/Timing

Table 5-39. Timing Requirements for MDIO Input(1) (see Figure 5-32 and Figure 5-33)

NO.			MIN	MAX	UNIT
1	$t_{c(MDIO_CLK)}$	Cycle time, MDIO_CLK	400		ns
2	$t_{w(MDIO_CLK)}$	Pulse duration, MDIO_CLK high/low	180		ns
3	$t_{t(MDIO_CLK)}$	Transition time, MDIO_CLK		5	ns
4	$t_{su(MDIO\text{-}MDIO_CLKH)}$	Setup time, MDIO data input valid before MDIO_CLK high	10		ns
5	$t_{h(MDIO_CLKH\text{-}MDIO)}$	Hold time, MDIO data input valid after MDIO_CLK high	0		ns

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.

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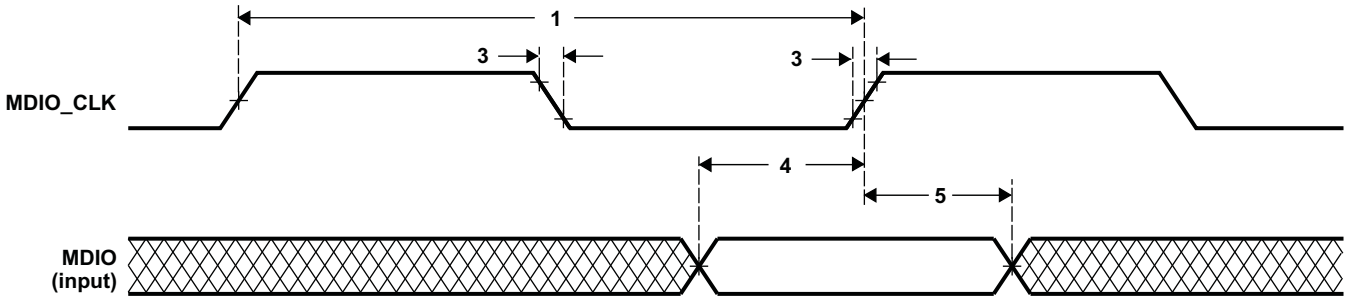

Figure 5-32. MDIO Input Timing

Table 5-40. Switching Characteristics Over Recommended Operating Conditions for MDIO Output(1) (see Figure 5-33)

NO.		MIN	MAX	UNIT
7	$t_{d(MDIO_CLKL-MDIO)}$ Delay time, MDIO_CLK low to MDIO data output valid	0	100	ns

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.

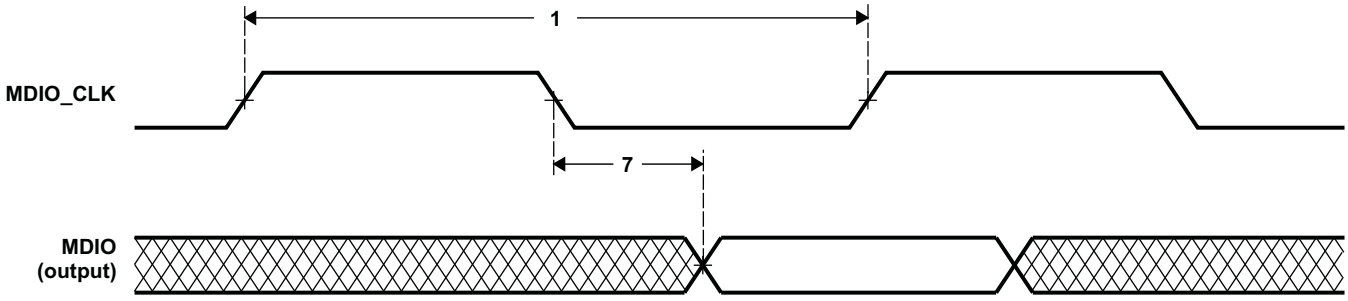

Figure 5-33. MDIO Output Timing

5.15 Multichannel Audio Serial Ports (McASP0, McASP1, and McASP2)

The McASP serial port is specifically designed for multichannel audio applications. Its key features are:

- Flexible clock and frame sync generation logic and on-chip dividers
- Up to sixteen transmit or receive data pins and serializers
- Large number of serial data format options, including:
  - TDM Frames with 2 to 32 time slots per frame (periodic) or 1 slot per frame (burst)
  - Time slots of 8,12,16, 20, 24, 28, and 32 bits
  - First bit delay 0, 1, or 2 clocks
  - MSB or LSB first bit order
  - Left- or right-aligned data words within time slots
- DIT Mode (optional) with 384-bit Channel Status and 384-bit User Data registers
- Extensive error checking and mute generation logic
- All unused pins GPIO-capable

Additionally, while the OMAPL137 McASP modules are backward compatible with the McASP on previous devices, the OMAPL137 McASP includes the following new features:

- Transmit & Receive FIFO Buffers for each McASP. Allows the McASP to operate at a higher sample rate by making it more tolerant to DMA latency.
- Dynamic Adjustment of Clock Dividers
  - Clock Divider Value may be changed without resetting the McASP

The three McASPs on the device are configured with the following options:

Table 5-41. OMAPL137 McASP Configurations(1)

Module	Serializers	AFIFO	DIT	Pins
McASP0	16	64 Word RX 64 Word TX	N	AXR0[13:0], AHCLKR0, ACLKR0, AFSR0, AHCLKX0, ACLKX0, AFSX0
McASP1	12	64 Word RX 64 Word TX	N	AXR1[11:10], AXR1[8:0], ACLKR1, AFSR1, AHCLKX1, ACLKX1, AFSX1, AMUTE1
McASP2	4	16 Word RX 16 Word TX	Y	AXR2[3:0], ACLKR2, AFSR2, AHCLKX2, ACLKX2, AFSX2, AMUTE2

(1) Pins available are the maximum number of pins that may be configured for a particular McASP; not including pin multiplexing.

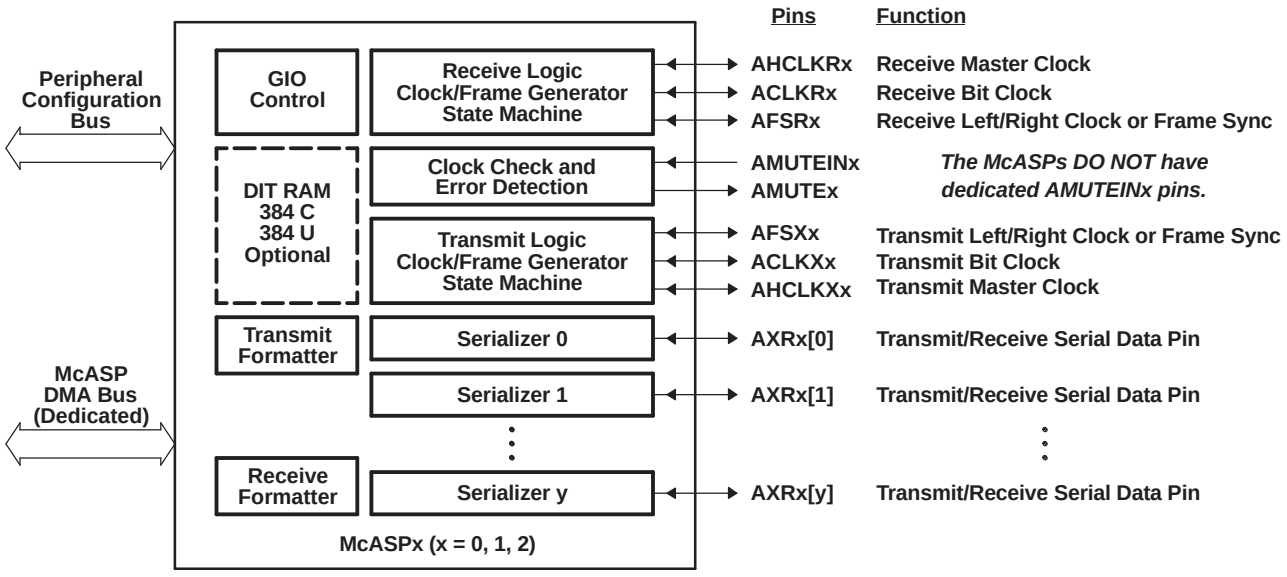

Figure 5-34. McASP Block Diagram

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5.15.1 McASP Peripheral Registers Description(s)

Registers for the McASP are summarized in Table 5-42. The registers are accessed through the peripheral configuration port. The receive buffer registers (RBUF) and transmit buffer registers (XBUF) can also be accessed through the DMA port, as listed in Table 5-43

Registers for the McASP Audio FIFO (AFIFO) are summarized in Table 5-44. Note that the AFIFO Write FIFO (WFIFO) and Read FIFO (RFIFO) have independent control and status registers. The AFIFO control registers are accessed through the peripheral configuration port. See the *TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.* – Literature Number SPRUFK9 for more details.

Table 5-42. McASP Registers Accessed Through Peripheral Configuration Port

Offset	McASP0 BYTE ADDRESS	McASP1 BYTE ADDRESS	McASP2 BYTE ADDRESS	Acronym	Register Description
0h	0x01D0 0000	0x01D0 4000	0x01D0 8000	REV	Revision identification register
10h	0x01D0 0010	0x01D0 4010	0x01D0 8010	PFUNC	Pin function register
14h	0x01D0 0014	0x01D0 4014	0x01D0 8014	PDIR	Pin direction register
18h	0x01D0 0018	0x01D0 4018	0x01D0 8018	PDOUT	Pin data output register
1Ch	0x01D0 001C	0x01D0 401C	0x01D0 801C	PDIN	Read returns: Pin data input register
1Ch	0x01D0 001C	0x01D0 401C	0x01D0 801C	PDSET	Writes affect: Pin data set register (alternate write address: PDOUT)
20h	0x01D0 0020	0x01D0 4020	0x01D0 8020	PDCLR	Pin data clear register (alternate write address: PDOUT)
44h	0x01D0 0044	0x01D0 4044	0x01D0 8044	GBLCTL	Global control register
48h	0x01D0 0048	0x01D0 4048	0x01D0 8048	AMUTE	Audio mute control register
4Ch	0x01D0 004C	0x01D0 404C	0x01D0 804C	DLBCTL	Digital loopback control register
50h	0x01D0 0050	0x01D0 4050	0x01D0 8050	DITCTL	DIT mode control register
60h	0x01D0 0060	0x01D0 4060	0x01D0 8060	RGBLCTL	Receiver global control register: Alias of GBLCTL, only receive bits are affected - allows receiver to be reset independently from transmitter
64h	0x01D0 0064	0x01D0 4064	0x01D0 8064	RMASK	Receive format unit bit mask register
68h	0x01D0 0068	0x01D0 4068	0x01D0 8068	RFMT	Receive bit stream format register
6Ch	0x01D0 006C	0x01D0 406C	0x01D0 806C	AFSRCTL	Receive frame sync control register
70h	0x01D0 0070	0x01D0 4070	0x01D0 8070	ACLKRCTL	Receive clock control register
74h	0x01D0 0074	0x01D0 4074	0x01D0 8074	AHCLKRCTL	Receive high-frequency clock control register
78h	0x01D0 0078	0x01D0 4078	0x01D0 8078	RTDM	Receive TDM time slot 0-31 register
7Ch	0x01D0 007C	0x01D0 407C	0x01D0 807C	RINTCTL	Receiver interrupt control register
80h	0x01D0 0080	0x01D0 4080	0x01D0 8080	RSTAT	Receiver status register
84h	0x01D0 0084	0x01D0 4084	0x01D0 8084	RSLOT	Current receive TDM time slot register
88h	0x01D0 0088	0x01D0 4088	0x01D0 8088	RCLKCHK	Receive clock check control register
8Ch	0x01D0 008C	0x01D0 408C	0x01D0 808C	REVTCTL	Receiver DMA event control register
ACh	0x01D0 00A0	0x01D0 40A0	0x01D0 80A0	XGBLCTL	Transmitter global control register. Alias of GBLCTL, only transmit bits are affected - allows transmitter to be reset independently from receiver
A4h	0x01D0 00A4	0x01D0 40A4	0x01D0 80A4	XMASK	Transmit format unit bit mask register
A8h	0x01D0 00A8	0x01D0 40A8	0x01D0 80A8	XFMT	Transmit bit stream format register
ACh	0x01D0 00AC	0x01D0 40AC	0x01D0 80AC	AFSXCTL	Transmit frame sync control register
B0h	0x01D0 00B0	0x01D0 40B0	0x01D0 80B0	ACLKXCTL	Transmit clock control register
B4h	0x01D0 00B4	0x01D0 40B4	0x01D0 80B4	AHCLKXCTL	Transmit high-frequency clock control register
B8h	0x01D0 00B8	0x01D0 40B8	0x01D0 80B8	XTDM	Transmit TDM time slot 0-31 register
BCh	0x01D0 00BC	0x01D0 40BC	0x01D0 80BC	XINTCTL	Transmitter interrupt control register
C0h	0x01D0 00C0	0x01D0 40C0	0x01D0 80C0	XSTAT	Transmitter status register
C4h	0x01D0 00C4	0x01D0 40C4	0x01D0 80C4	XSLOT	Current transmit TDM time slot register

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Table 5-42. McASP Registers Accessed Through Peripheral Configuration Port (continued)

Offset	McASP0 BYTE ADDRESS	McASP1 BYTE ADDRESS	McASP2 BYTE ADDRESS	Acronym	Register Description
C8h	0x01D0 00C8	0x01D0 40C8	0x01D0 80C8	XCLKCHK	Transmit clock check control register
CCh	0x01D0 00CC	0x01D0 40CC	0x01D0 80CC	XEVTCTL	Transmitter DMA event control register
100h	0x01D0 0100	0x01D0 4100	0x01D0 8100	DITCSRA0	Left (even TDM time slot) channel status register (DIT mode) 0
104h	0x01D0 0104	0x01D0 4104	0x01D0 8104	DITCSRA1	Left (even TDM time slot) channel status register (DIT mode) 1
108h	0x01D0 0108	0x01D0 4108	0x01D0 8108	DITCSRA2	Left (even TDM time slot) channel status register (DIT mode) 2
10Ch	0x01D0 010C	0x01D0 410C	0x01D0 810C	DITCSRA3	Left (even TDM time slot) channel status register (DIT mode) 3
110h	0x01D0 0110	0x01D0 4110	0x01D0 8110	DITCSRA4	Left (even TDM time slot) channel status register (DIT mode) 4
114h	0x01D0 0114	0x01D0 4114	0x01D0 8114	DITCSRA5	Left (even TDM time slot) channel status register (DIT mode) 5
118h	0x01D0 0118	0x01D0 4118	0x01D0 8118	DITCSRB0	Right (odd TDM time slot) channel status register (DIT mode) 0
11Ch	0x01D0 011C	0x01D0 411C	0x01D0 811C	DITCSRB1	Right (odd TDM time slot) channel status register (DIT mode) 1
120h	0x01D0 0120	0x01D0 4120	0x01D0 8120	DITCSRB2	Right (odd TDM time slot) channel status register (DIT mode) 2
124h	0x01D0 0124	0x01D0 4124	0x01D0 8124	DITCSRB3	Right (odd TDM time slot) channel status register (DIT mode) 3
128h	0x01D0 0128	0x01D0 4128	0x01D0 8128	DITCSRB4	Right (odd TDM time slot) channel status register (DIT mode) 4
12Ch	0x01D0 012C	0x01D0 412C	0x01D0 812C	DITCSRB5	Right (odd TDM time slot) channel status register (DIT mode) 5
130h	0x01D0 0130	0x01D0 4130	0x01D0 8130	DITUDRA0	Left (even TDM time slot) channel user data register (DIT mode) 0
134h	0x01D0 0134	0x01D0 4134	0x01D0 8134	DITUDRA1	Left (even TDM time slot) channel user data register (DIT mode) 1
138h	0x01D0 0138	0x01D0 4138	0x01D0 8138	DITUDRA2	Left (even TDM time slot) channel user data register (DIT mode) 2
13Ch	0x01D0 013C	0x01D0 413C	0x01D0 813C	DITUDRA3	Left (even TDM time slot) channel user data register (DIT mode) 3
140h	0x01D0 0140	0x01D0 4140	0x01D0 8140	DITUDRA4	Left (even TDM time slot) channel user data register (DIT mode) 4
144h	0x01D0 0144	0x01D0 4144	0x01D0 8144	DITUDRA5	Left (even TDM time slot) channel user data register (DIT mode) 5
148h	0x01D0 0148	0x01D0 4148	0x01D0 8148	DITUDRB0	Right (odd TDM time slot) channel user data register (DIT mode) 0
14Ch	0x01D0 014C	0x01D0 414C	0x01D0 814C	DITUDRB1	Right (odd TDM time slot) channel user data register (DIT mode) 1
150h	0x01D0 0150	0x01D0 4150	0x01D0 8150	DITUDRB2	Right (odd TDM time slot) channel user data register (DIT mode) 2
154h	0x01D0 0154	0x01D0 4154	0x01D0 8154	DITUDRB3	Right (odd TDM time slot) channel user data register (DIT mode) 3
158h	0x01D0 0158	0x01D0 4158	0x01D0 8158	DITUDRB4	Right (odd TDM time slot) channel user data register (DIT mode) 4
15Ch	0x01D0 015C	0x01D0 415C	0x01D0 815C	DITUDRB5	Right (odd TDM time slot) channel user data register (DIT mode) 5
180h	0x01D0 0180	0x01D0 4180	0x01D0 8180	SRCTL0	Serializer control register 0
184h	0x01D0 0184	0x01D0 4184	0x01D0 8184	SRCTL1	Serializer control register 1
188h	0x01D0 0188	0x01D0 4188	0x01D0 8188	SRCTL2	Serializer control register 2

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Table 5-42. McASP Registers Accessed Through Peripheral Configuration Port (continued)

Offset	McASP0 BYTE ADDRESS	McASP1 BYTE ADDRESS	McASP2 BYTE ADDRESS	Acronym	Register Description
18Ch	0x01D0 018C	0x01D0 418C	0x01D0 818C	SRCTL3	Serializer control register 3
190h	0x01D0 0190	0x01D0 4190	0x01D0 8190	SRCTL4	Serializer control register 4
194h	0x01D0 0194	0x01D0 4194	0x01D0 8194	SRCTL5	Serializer control register 5
198h	0x01D0 0198	0x01D0 4198	0x01D0 8198	SRCTL6	Serializer control register 6
19Ch	0x01D0 019C	0x01D0 419C	0x01D0 819C	SRCTL7	Serializer control register 7
1A0h	0x01D0 01A0	0x01D0 41A0	0x01D0 81A0	SRCTL8	Serializer control register 8
1A4h	0x01D0 01A4	0x01D0 41A4	0x01D0 81A4	SRCTL9	Serializer control register 9
1A8h	0x01D0 01A8	0x01D0 41A8	0x01D0 81A8	SRCTL10	Serializer control register 10
1ACh	0x01D0 01AC	0x01D0 41AC	0x01D0 81AC	SRCTL11	Serializer control register 11
1B0h	0x01D0 01B0	0x01D0 41B0	0x01D0 81B0	SRCTL12	Serializer control register 12
1B4h	0x01D0 01B4	0x01D0 41B4	0x01D0 81B4	SRCTL13	Serializer control register 13
1B8h	0x01D0 01B8	0x01D0 41B8	0x01D0 81B8	SRCTL14	Serializer control register 14
1BCh	0x01D0 01BC	0x01D0 41BC	0x01D0 81BC	SRCTL15	Serializer control register 15
200h	0x01D0 0200	0x01D0 4200	0x01D0 8200	XBUF0(1)	Transmit buffer register for serializer 0
204h	0x01D0 0204	0x01D0 4204	0x01D0 8204	XBUF1(2)	Transmit buffer register for serializer 1
208h	0x01D0 0208	0x01D0 4208	0x01D0 8208	XBUF2(2)	Transmit buffer register for serializer 2
20Ch	0x01D0 020C	0x01D0 420C	0x01D0 820C	XBUF3(2)	Transmit buffer register for serializer 3
210h	0x01D0 0210	0x01D0 4210	0x01D0 8210	XBUF4(2)	Transmit buffer register for serializer 4
214h	0x01D0 0214	0x01D0 4214	0x01D0 8214	XBUF5(2)	Transmit buffer register for serializer 5
218h	0x01D0 0218	0x01D0 4218	0x01D0 8218	XBUF6(2)	Transmit buffer register for serializer 6
21Ch	0x01D0 021C	0x01D0 421C	0x01D0 821C	XBUF7(2)	Transmit buffer register for serializer 7
220h	0x01D0 0220	0x01D0 4220	0x01D0 8220	XBUF8(2)	Transmit buffer register for serializer 8
224h	0x01D0 0224	0x01D0 4224	0x01D0 8224	XBUF9(2)	Transmit buffer register for serializer 9
228h	0x01D0 0228	0x01D0 4228	0x01D0 8228	XBUF10(2)	Transmit buffer register for serializer 10
22Ch	0x01D0 022C	0x01D0 422C	0x01D0 822C	XBUF11(2)	Transmit buffer register for serializer 11
230h	0x01D0 0230	0x01D0 4230	0x01D0 8230	XBUF12(2)	Transmit buffer register for serializer 12
234h	0x01D0 0234	0x01D0 4234	0x01D0 8234	XBUF13(2)	Transmit buffer register for serializer 13
238h	0x01D0 0238	0x01D0 4238	0x01D0 8238	XBUF14(2)	Transmit buffer register for serializer 14
23Ch	0x01D0 023C	0x01D0 423C	0x01D0 823C	XBUF15(2)	Transmit buffer register for serializer 15
280h	0x01D0 0280	0x01D0 4280	0x01D0 8280	RBUF0(3)	Receive buffer register for serializer 0
284h	0x01D0 0284	0x01D0 4284	0x01D0 8284	RBUF1(3)	Receive buffer register for serializer 1
288h	0x01D0 0288	0x01D0 4288	0x01D0 8288	RBUF2(3)	Receive buffer register for serializer 2
28Ch	0x01D0 028C	0x01D0 428C	0x01D0 828C	RBUF3(3)	Receive buffer register for serializer 3
290h	0x01D0 0290	0x01D0 4290	0x01D0 8290	RBUF4(3)	Receive buffer register for serializer 4
294h	0x01D0 0294	0x01D0 4294	0x01D0 8294	RBUF5(3)	Receive buffer register for serializer 5
298h	0x01D0 0298	0x01D0 4298	0x01D0 8298	RBUF6(3)	Receive buffer register for serializer 6
29Ch	0x01D0 029C	0x01D0 429C	0x01D0 829C	RBUF7(3)	Receive buffer register for serializer 7
2A0h	0x01D0 02A0	0x01D0 42A0	0x01D0 82A0	RBUF8(3)	Receive buffer register for serializer 8
2A4h	0x01D0 02A4	0x01D0 42A4	0x01D0 82A4	RBUF9(3)	Receive buffer register for serializer 9
2A8h	0x01D0 02A8	0x01D0 42A8	0x01D0 82A8	RBUF10(3)	Receive buffer register for serializer 10
2ACh	0x01D0 02AC	0x01D0 42AC	0x01D0 82AC	RBUF11(3)	Receive buffer register for serializer 11
2B0h	0x01D0 02B0	0x01D0 42B0	0x01D0 82B0	RBUF12(3)	Receive buffer register for serializer 12
2B4h	0x01D0 02B4	0x01D0 42B4	0x01D0 82B4	RBUF13(3)	Receive buffer register for serializer 13
2B8h	0x01D0 02B8	0x01D0 42B8	0x01D0 82BB	RBUF14(3)	Receive buffer register for serializer 14

(1) Writes to XRBUF originate from peripheral configuration port only when XBUSEL = 1 in XFMT.
(2) Writes to XRBUF originate from peripheral configuration port only when XBUSEL = 1 in XFMT.
(3) Reads from XRBUF originate on peripheral configuration port only when RBUSEL = 1 in RFMT.

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Table 5-42. McASP Registers Accessed Through Peripheral Configuration Port (continued)

Offset	McASP0 BYTE ADDRESS	McASP1 BYTE ADDRESS	McASP2 BYTE ADDRESS	Acronym	Register Description
2BCh	0x01D0 02BC	0x01D0 42BC	0x01D0 82BC	RBUF15[3]	Receive buffer register for serializer 15

Table 5-43. McASP Registers Accessed Through DMA Port

Hex Address	Register Name	McASP0 BYTE ADDRESS	McASP1 BYTE ADDRESS	McASP2 BYTE ADDRESS	Register Description
Read Accesses	RBUF	01D0 2000	01D0 6000	01D0 A000	Receive buffer DMA port address. Cycles through receive serializers, skipping over transmit serializers and inactive serializers. Starts at the lowest serializer at the beginning of each time slot. Reads from DMA port only if XBUSEL = 0 in XFMT.
Write Accesses	XBUF	01D0 2000	01D0 6000	01D0 A000	Transmit buffer DMA port address. Cycles through transmit serializers, skipping over receive and inactive serializers. Starts at the lowest serializer at the beginning of each time slot. Writes to DMA port only if RBUSEL = 0 in RFMT.

Table 5-44. McASP AFIFO Registers Accessed Through Peripheral Configuration Port

McASP0 BYTE ADDRESS	McASP1 BYTE ADDRESS	McASP2 BYTE ADDRESS	Acronym	Register Description
0x01D0 1000	0x01D0 5000	0x01D0 9000	AFIFOREV	AFIFO revision identification register
0x01D0 1010	0x01D0 5010	0x01D0 9010	WFIFOCTL	Write FIFO control register
0x01D0 1014	0x01D0 5014	0x01D0 9014	WFIFOSTS	Write FIFO status register
0x01D0 1018	0x01D0 5018	0x01D0 9018	RFIFOCTL	Read FIFO control register
0x01D0 101C	0x01D0 501C	0x01D0 901C	RFIFOSTS	Read FIFO status register

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5.15.2 McASP Electrical Data/Timing

5.15.2.1 Multichannel Audio Serial Port 0 (McASP0) Timing

Table 5-45 and Table 5-46 assume testing over recommended operating conditions (see Figure 5-35 and Figure 5-36).

Table 5-45. McASP0 Timing Requirements(1) (2)

NO.			MIN	MAX	UNIT
1(3)	$t_{c(AHCLKRX)}$	Cycle time, AHCLKR0 external, AHCLKR0 input	20		ns
		Cycle time, AHCLKX0 external, AHCLKX0 input	20		
2(3)	$t_{w(AHCLKRX)}$	Pulse duration, AHCLKR0 external, AHCLKR0 input	10		ns
		Pulse duration, AHCLKX0 external, AHCLKX0 input	10		
3(3)	$t_{c(ACLKRX)}$	Cycle time, ACLKR0 external, ACLKR0 input	greater of 2P or 20		ns
		Cycle time, ACLKX0 external, ACLKX0 input	greater of 2P or 20		
4(3)	$t_{w(ACLKRX)}$	Pulse duration, ACLKR0 external, ACLKR0 input	10		ns
		Pulse duration, ACLKX0 external, ACLKX0 input	10		
5	$t_{su(AFSRX-ACLKRX)}$	Setup time, AFSR0 input to ACLKR0 internal(4)	10		ns
		Setup time, AFSX0 input to ACLKX0 internal	10		
		Setup time, AFSR0 input to ACLKR0 external input(4)	3.2		
		Setup time, AFSX0 input to ACLKX0 external input	3.2		
		Setup time, AFSR0 input to ACLKR0 external output(4)	3.2		
		Setup time, AFSX0 input to ACLKX0 external output	3.2		
6	$t_{h(ACLKRX-AFSRX)}$	Hold time, AFSR0 input after ACLKR0 internal(4)	-0.8		ns
		Hold time, AFSX0 input after ACLKX0 internal	-0.8		
		Hold time, AFSR0 input after ACLKR0 external input(4)	0.6		
		Hold time, AFSX0 input after ACLKX0 external input	0.9		
		Hold time, AFSR0 input after ACLKR0 external output(4)	0.6		
		Hold time, AFSX0 input after ACLKX0 external output	0.9		
7	$t_{su(AXR-ACLKRX)}$	Setup time, AXR0[n] input to ACLKR0 internal(4)	10		ns
		Setup time, AXR0[n] input to ACLKX0 internal(5)	10		
		Setup time, AXR0[n] input to ACLKR0 external input(4)	3.2		
		Setup time, AXR0[n] input to ACLKX0 external input(5)	3.2		
		Setup time, AXR0[n] input to ACLKR0 external output(4)	3.2		
		Setup time, AXR0[n] input to ACLKX0 external output(5)	3.2		

(1) ACLKX0 internal – McASP0 ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX0 external input – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX0 external output – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
ACLKR0 internal – McASP0 ACLKRCTL.CLKRM = 1, PDIR.ACLKR =1
ACLKR0 external input – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR0 external output – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
(2) P = SYSCLK2 period
(3) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(4) McASP0 ACLKXCTL.ASYNC=1: Receiver is clocked by its own ACLKR0
(5) McASP0 ACLKXCTL.ASYNC=0: Receiver is clocked by transmitter's ACLKX0

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Table 5-45. McASP0 Timing Requirements[1] [2] (continued)

NO.			MIN	MAX	UNIT
8	$t_{h(ACLKRX-AXR)}$	Hold time, AXR0[n] input after ACLKR0 internal[4]	-1.25		ns
		Hold time, AXR0[n] input after ACLKX0 internal[5]	-1.25		
		Hold time, AXR0[n] input after ACLKR0 external input[4]	0.9		
		Hold time, AXR0[n] input after ACLKX0 external input[5]	0.9		
		Hold time, AXR0[n] input after ACLKR0 external output[4]	0.9		
		Hold time, AXR0[n] input after ACLKX0 external output[5]	0.9		

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Table 5-46. McASP0 Switching Characteristics(1)

NO.	PARAMETER		MIN	MAX	UNIT
9(2)	$t_{c(AHCLKRX)}$	Cycle time, AHCLKR0 internal, AHCLKR0 output	20		ns
		Cycle time, AHCLKR0 external, AHCLKR0 output	20		
		Cycle time, AHCLKX0 internal, AHCLKX0 output	20		
		Cycle time, AHCLKX0 external, AHCLKX0 output	20		
10(2)	$t_{w(AHCLKRX)}$	Pulse duration, AHCLKR0 internal, AHCLKR0 output	(AHR/2) – 2.5(3)		ns
		Pulse duration, AHCLKR0 external, AHCLKR0 output	(AHR/2) – 2.5(3)		
		Pulse duration, AHCLKX0 internal, AHCLKX0 output	(AHX/2) – 2.5(4)		
		Pulse duration, AHCLKX0 external, AHCLKX0 output	(AHX/2) – 2.5(4)		
11(2)	$t_{c(ACLKRX)}$	Cycle time, ACLKR0 internal, ACLKR0 output	greater of 2P or 20 ns(5)		ns
		Cycle time, ACLKR0 external, ACLKR0 output	greater of 2P or 20 ns(5)		
		Cycle time, ACLKX0 internal, ACLKX0 output	greater of 2P or 20 ns(5)		
		Cycle time, ACLKX0 external, ACLKX0 output	greater of 2P or 20 ns(5)		
12(2)	$t_{w(ACLKRX)}$	Pulse duration, ACLKR0 internal, ACLKR0 output	(AR/2) – 2.5(6)		ns
		Pulse duration, ACLKR0 external, ACLKR0 output	(AR/2) – 2.5(6)		
		Pulse duration, ACLKX0 internal, ACLKX0 output	(AX/2) – 2.5(7)		
		Pulse duration, ACLKX0 external, ACLKX0 output	(AX/2) – 2.5(7)		
13	$t_{d(ACLKRX-AFSRX)}$	Delay time, ACLKR0 internal, AFSR output(8)	0	6.2	ns
		Delay time, ACLKX0 internal, AFSX output	0	6.2	
		Delay time, ACLKR0 external input, AFSR output(8)	2.25	12.5	
		Delay time, ACLKX0 external input, AFSX output	2.25	12.5	
		Delay time, ACLKR0 external output, AFSR output(8)	2.25	12.5	
		Delay time, ACLKX0 external output, AFSX output	2.25	12.5	
14	$t_{d(ACLKX-AXRV)}$	Delay time, ACLKX0 internal, AXR0[n] output	0	6.2	ns
		Delay time, ACLKX0 external input, AXR0[n] output	2.25	12.5	
		Delay time, ACLKX0 external output, AXR0[n] output	2.25	12.5	
15	$t_{dis(ACLKX-AXRHZ)}$	Disable time, ACLKX0 internal, AXR0[n] output	0	6.2	ns
		Disable time, ACLKX0 external input, AXR0[n] output	2.25	12.5	
		Disable time, ACLKX0 external output, AXR0[n] output	2.25	12.5	

(1) McASP0 ACLKX0 internal – ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX0 external input – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX0 external output – McASP0ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
ACLKR0 internal – McASP0 ACLKR0CTL.CLKRM = 1, PDIR.ACLKR =1
ACLKR0 external input – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR0 external output – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
(2) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(3) AHR - Cycle time, AHCLKR0.
(4) AHX - Cycle time, AHCLKX0.
(5) P = SYSCLK2 period
(6) AR - ACLKR0 period.
(7) AX - ACLKX0 period.
(8) McASP0 ACLKXCTL.ASYNC=1: Receiver is clocked by its own ACLKR0

5.15.2.2 Multichannel Audio Serial Port 1 (McASP1) Timing

Table 5-47 and Table 5-48 assume testing over recommended operating conditions (see Figure 5-35 and Figure 5-36).

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Table 5-47. McASP1 Timing Requirements(1) (2)

NO.			MIN	MAX	UNIT
1(3)	$t_{c(AHCLKRX)}$	Cycle time, AHCLKR1 external, AHCLKR1 input	20		ns
		Cycle time, AHCLKX1 external, AHCLKX1 input	20		
2(3)	$t_{w(AHCLKRX)}$	Pulse duration, AHCLKR1 external, AHCLKR1 input	10		ns
		Pulse duration, AHCLKX1 external, AHCLKX1 input	10		
3(3)	$t_{c(ACLKRX)}$	Cycle time, ACLKR1 external, ACLKR1 input	greater of 2P or 20		ns
		Cycle time, ACLKX1 external, ACLKX1 input	greater of 2P or 20		
4(3)	$t_{w(ACLKRX)}$	Pulse duration, ACLKR1 external, ACLKR1 input	10		ns
		Pulse duration, ACLKX1 external, ACLKX1 input	10		
5	$t_{su(AFSRX-ACLKRX)}$	Setup time, AFSR1 input to ACLKR1 internal(4)	11		ns
		Setup time, AFSX1 input to ACLKX1 internal	11		
		Setup time, AFSR1 input to ACLKR1 external input(4)	2.7		
		Setup time, AFSX1 input to ACLKX1 external input	2.7		
		Setup time, AFSR1 input to ACLKR1 external output(4)	2.7		
		Setup time, AFSX1 input to ACLKX1 external output	2.7		
6	$t_{h(ACLKRX-AFSRX)}$	Hold time, AFSR1 input after ACLKR1 internal(4)	-1.4		ns
		Hold time, AFSX1 input after ACLKX1 internal	-1.4		
		Hold time, AFSR1 input after ACLKR1 external input(4)	0.7		
		Hold time, AFSX1 input after ACLKX1 external input	0.7		
		Hold time, AFSR1 input after ACLKR1 external output(4)	0.9		
		Hold time, AFSX1 input after ACLKX1 external output	0.9		
7	$t_{su(AXR-ACLKRX)}$	Setup time, AXR1[n] input to ACLKR1 internal(4)	11		ns
		Setup time, AXR1[n] input to ACLKX1 internal(5)	11		
		Setup time, AXR1[n] input to ACLKR1 external input(4)	2.7		
		Setup time, AXR1[n] input to ACLKX1 external input(5)	2.7		
		Setup time, AXR1[n] input to ACLKR1 external output(4)	2.7		
		Setup time, AXR1[n] input to ACLKX1 external output(5)	2.7		
8	$t_{h(ACLKRX-AXR)}$	Hold time, AXR1[n] input after ACLKR1 internal(4)	-1.4		ns
		Hold time, AXR1[n] input after ACLKX1 internal(5)	-1.4		
		Hold time, AXR1[n] input after ACLKR1 external input(4)	0.6		
		Hold time, AXR1[n] input after ACLKX1 external input(5)	0.9		
		Hold time, AXR1[n] input after ACLKR1 external output(4)	0.9		
		Hold time, AXR1[n] input after ACLKX1 external output(5)	0.9		

(1) ACLKX1 internal – McASP1 ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX1 external input – McASP1 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX1 external output – McASP1 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
ACLKR1 internal – McASP1 ACLKRCTL.CLKRM = 1, PDIR.ACLKR =1
ACLKR1 external input – McASP1 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR1 external output – McASP1 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
(2) P = SYSCLK2 period
(3) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(4) McASP1 ACLKXCTL.ASYNC=1: Receiver is clocked by its own ACLKR1
(5) McASP1 ACLKXCTL.ASYNC=0: Receiver is clocked by transmitter's ACLKX1

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Table 5-48. McASP1 Switching Characteristics[1]

NO.	PARAMETER		MIN	MAX	UNIT
9[2]	$t_{c(AHCLKRX)}$	Cycle time, AHCLKR1 internal, AHCLKR1 output	20		ns
		Cycle time, AHCLKR1 external, AHCLKR1 output	20		
		Cycle time, AHCLKX1 internal, AHCLKX1 output	20		
		Cycle time, AHCLKX1 external, AHCLKX1 output	20		
10[2]	$t_{w(AHCLKRX)}$	Pulse duration, AHCLKR1 internal, AHCLKR1 output	(AHR/2) – 2.5[3]		ns
		Pulse duration, AHCLKR1 external, AHCLKR1 output	(AHR/2) – 2.5[3]		
		Pulse duration, AHCLKX1 internal, AHCLKX1 output	(AHX/2) – 2.5[4]		
		Pulse duration, AHCLKX1 external, AHCLKX1 output	(AHX/2) – 2.5[4]		
11[2]	$t_{c(ACLKRX)}$	Cycle time, ACLKR1 internal, ACLKR1 output	greater of 2P or 20 ns[5]		ns
		Cycle time, ACLKR1 external, ACLKR1 output	greater of 2P or 20 ns[5]		
		Cycle time, ACLKX1 internal, ACLKX1 output	greater of 2P or 20 ns[5]		
		Cycle time, ACLKX1 external, ACLKX1 output	greater of 2P or 20 ns[5]		
12[2]	$t_{w(ACLKRX)}$	Pulse duration, ACLKR1 internal, ACLKR1 output	(AR/2) – 2.5[6]		ns
		Pulse duration, ACLKR1 external, ACLKR1 output	(AR/2) – 2.5[6]		
		Pulse duration, ACLKX1 internal, ACLKX1 output	(AX/2) – 2.5[7]		
		Pulse duration, ACLKX1 external, ACLKX1 output	(AX/2) – 2.5[7]		
13	$t_{d(ACLKRX-AFSRX)}$	Delay time, ACLKR1 internal, AFSR output[8]	0.3	7	ns
		Delay time, ACLKX1 internal, AFSX output	0.3	7	
		Delay time, ACLKR1 external input, AFSR output[8]	3	14.5	
		Delay time, ACLKX1 external input, AFSX output	3	14.5	
		Delay time, ACLKR1 external output, AFSR output[8]	3	14.5	
		Delay time, ACLKX1 external output, AFSX output	3	14.5	
14	$t_{d(ACLKX-AXRV)}$	Delay time, ACLKX1 internal, AXR1[n] output	0.3	7	ns
		Delay time, ACLKX1 external input, AXR1[n] output	3	14.5	
		Delay time, ACLKX1 external output, AXR1[n] output	3	14.5	
15	$t_{dis(ACLKX-AXRHZ)}$	Disable time, ACLKX1 internal, AXR1[n] output	0.3	7	ns
		Disable time, ACLKX1 external input, AXR1[n] output	3	14.5	
		Disable time, ACLKX1 external output, AXR1[n] output	3	14.5	

(1) McASP1 ACLKX1 internal – ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
McASP1 ACLKX1 external input – ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
McASP1 ACLKX1 external output – ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
McASP1 ACLKR1 internal – ACLKR1CTL.CLKRM = 1, PDIR.ACLKR =1
McASP1 ACLKR1 external input – ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
McASP1 ACLKR1 external output – ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
(2) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(3) AHR - Cycle time, AHCLKR1.
(4) AHX - Cycle time, AHCLKX1.
(5) P = SYSCLK2 period
(6) AR - ACLKR1 period.
(7) AX - ACLKX1 period.
(8) McASP1 ACLKXCTL.ASYNC=1: Receiver is clocked by its own ACLKR1

5.15.2.3 Multichannel Audio Serial Port 2 (McASP2) Timing

Table 5-49 and Table 5-50 assume testing over recommended operating conditions (see Figure 5-35 and Figure 5-36).

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Table 5-49. McASP2 Timing Requirements(1) (2)

NO.			MIN	MAX	UNIT
1(3)	$t_{c(AHCLKRX)}$	Cycle time, AHCLKR2 external, AHCLKR2 input	13		ns
		Cycle time, AHCLKX2 external, AHCLKX2 input	13		
2(3)	$t_{w(AHCLKRX)}$	Pulse duration, AHCLKR2 external, AHCLKR2 input	6.5		ns
		Pulse duration, AHCLKX2 external, AHCLKX2 input	6.5		
3(3)	$t_{c(ACLKRX)}$	Cycle time, ACLKR2 external, ACLKR2 input	greater of 2P or 13		ns
		Cycle time, ACLKX2 external, ACLKX2 input	greater of 2P or 13		
4(3)	$t_{w(ACLKRX)}$	Pulse duration, ACLKR2 external, ACLKR2 input	6.5		ns
		Pulse duration, ACLKX2 external, ACLKX2 input	6.5		
5	$t_{su(AFSRX-ACLKRX)}$	Setup time, AFSR2 input to ACLKR2 internal(4)	11		ns
		Setup time, AFSX2 input to ACLKX2 internal	11		
		Setup time, AFSR2 input to ACLKR2 external input(4)	1.7		
		Setup time, AFSX2 input to ACLKX2 external input	1.7		
		Setup time, AFSR2 input to ACLKR2 external output(4)	1.7		
		Setup time, AFSX2 input to ACLKX2 external output	1.7		
6	$t_{h(ACLKRX-AFSRX)}$	Hold time, AFSR2 input after ACLKR2 internal(4)	-1.25		ns
		Hold time, AFSX2 input after ACLKX2 internal	-1.25		
		Hold time, AFSR2 input after ACLKR2 external input(4)	1.3		
		Hold time, AFSX2 input after ACLKX2 external input	1.3		
		Hold time, AFSR2 input after ACLKR2 external output(4)	1.3		
		Hold time, AFSX2 input after ACLKX2 external output	1.3		
7	$t_{su(AXR-ACLKRX)}$	Setup time, AXR2[n] input to ACLKR2 internal(4)	11		ns
		Setup time, AXR2[n] input to ACLKX2 internal(5)	11		
		Setup time, AXR2[n] input to ACLKR2 external input(4)	1.7		
		Setup time, AXR2[n] input to ACLKX2 external input(5)	1.7		
		Setup time, AXR2[n] input to ACLKR2 external output(4)	1.7		
		Setup time, AXR2[n] input to ACLKX2 external output(5)	1.7		
8	$t_{h(ACLKRX-AXR)}$	Hold time, AXR2[n] input after ACLKR2 internal(4)	-1.7		ns
		Hold time, AXR2[n] input after ACLKX2 internal(5)	-1.7		
		Hold time, AXR2[n] input after ACLKR2 external input(4)	1.3		
		Hold time, AXR2[n] input after ACLKX2 external input(5)	1.3		
		Hold time, AXR2[n] input after ACLKR2 external output(4)	1.3		
		Hold time, AXR2[n] input after ACLKX2 external output(5)	1.3		

(1) ACLKX2 internal – McASP2 ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX2 external input – McASP2 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX2 external output – McASP2 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
ACLKR2 internal – McASP2 ACLKRCTL.CLKRM = 1, PDIR.ACLKR =1
ACLKR2 external input – McASP2 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR2 external output – McASP2 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
(2) P = SYSCLK2 period
(3) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(4) McASP2 ACLKXCTL.ASYNC=1: Receiver is clocked by its own ACLKR2
(5) McASP2 ACLKXCTL.ASYNC=0: Receiver is clocked by transmitter's ACLKX2

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Table 5-50. McASP2 Switching Characteristics(1)

NO.	PARAMETER		MIN	MAX	UNIT
9(2)	$t_{c(AHCLKRX)}$	Cycle time, AHCLKR2 internal, AHCLKR2 output	13		ns
		Cycle time, AHCLKR2 external, AHCLKR2 output	13		
		Cycle time, AHCLKX2 internal, AHCLKX2 output	13		
		Cycle time, AHCLKX2 external, AHCLKX2 output	13		
10(2)	$t_{w(AHCLKRX)}$	Pulse duration, AHCLKR2 internal, AHCLKR2 output	(AHR/2) – 2.5(3)		ns
		Pulse duration, AHCLKR2 external, AHCLKR2 output	(AHR/2) – 2.5(3)		
		Pulse duration, AHCLKX2 internal, AHCLKX2 output	(AHX/2) – 2.5(4)		
		Pulse duration, AHCLKX2 external, AHCLKX2 output	(AHX/2) – 2.5(4)		
11(2)	$t_{c(ACLKRX)}$	Cycle time, ACLKR2 internal, ACLKR2 output	greater of 2P or 13 ns(5)		ns
		Cycle time, ACLKR2 external, ACLKR2 output	greater of 2P or 13 ns(5)		
		Cycle time, ACLKX2 internal, ACLKX2 output	greater of 2P or 13 ns(5)		
		Cycle time, ACLKX2 external, ACLKX2 output	greater of 2P or 13 ns(5)		
12(2)	$t_{w(ACLKRX)}$	Pulse duration, ACLKR2 internal, ACLKR2 output	(AR/2) – 2.5(6)		ns
		Pulse duration, ACLKR2 external, ACLKR2 output	(AR/2) – 2.5(6)		
		Pulse duration, ACLKX2 internal, ACLKX2 output	(AX/2) – 2.5(7)		
		Pulse duration, ACLKX2 external, ACLKX2 output	(AX/2) – 2.5(7)		
13	$t_{d(ACLKRX-AFSRX)}$	Delay time, ACLKR2 internal, AFSR output(8)	-1.5	3	ns
		Delay time, ACLKX2 internal, AFSX output	-1.5	3	
		Delay time, ACLKR2 external input, AFSR output(8)	1.6	11	
		Delay time, ACLKX2 external input, AFSX output	1.6	11	
		Delay time, ACLKR2 external output, AFSR output(8)	1.6	11	
		Delay time, ACLKX2 external output, AFSX output	1.6	11	
14	$t_{d(ACLKX-AXRV)}$	Delay time, ACLKX2 internal, AXR2[n] output	-1.5	3	ns
		Delay time, ACLKX2 external input, AXR2[n] output	1.6	11	
		Delay time, ACLKX2 external output, AXR2[n] output	1.6	11	
15	$t_{dis(ACLKX-AXRHZ)}$	Disable time, ACLKX2 internal, AXR2[n] output	-1.5	3	ns
		Disable time, ACLKX2 external input, AXR2[n] output	1.6	11	
		Disable time, ACLKX2 external output, AXR2[n] output	1.6	11	

(1) McASP2 ACLKX2 internal – ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
McASP2 ACLKX2 external input – ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
McASP2 ACLKX2 external output – ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
McASP2 ACLKR2 internal – ACLKR2CTL.CLKRM = 1, PDIR.ACLKR =1
McASP2 ACLKR2 external input – ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
McASP2 ACLKR2 external output – ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
(2) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(3) AHR - Cycle time, AHCLKR2.
(4) AHX - Cycle time, AHCLKX2.
(5) P = SYSCLK2 period
(6) AR - ACLKR2 period.
(7) AX - ACLKX2 period.
(8) McASP2 ACLKXCTL.ASYNC=1: Receiver is clocked by its own ACLKR2

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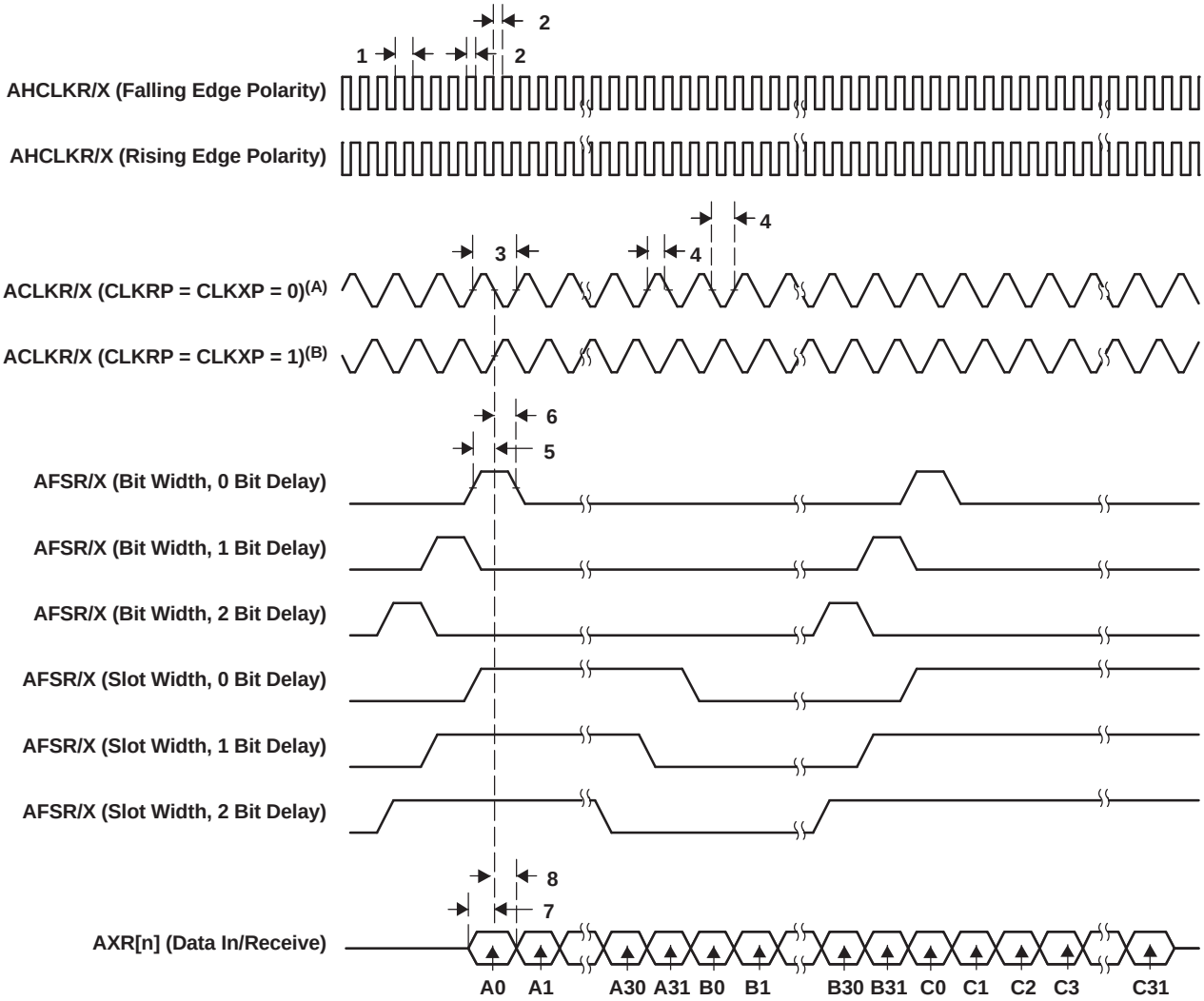

A. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

B. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

Figure 5-35. McASP Input Timings

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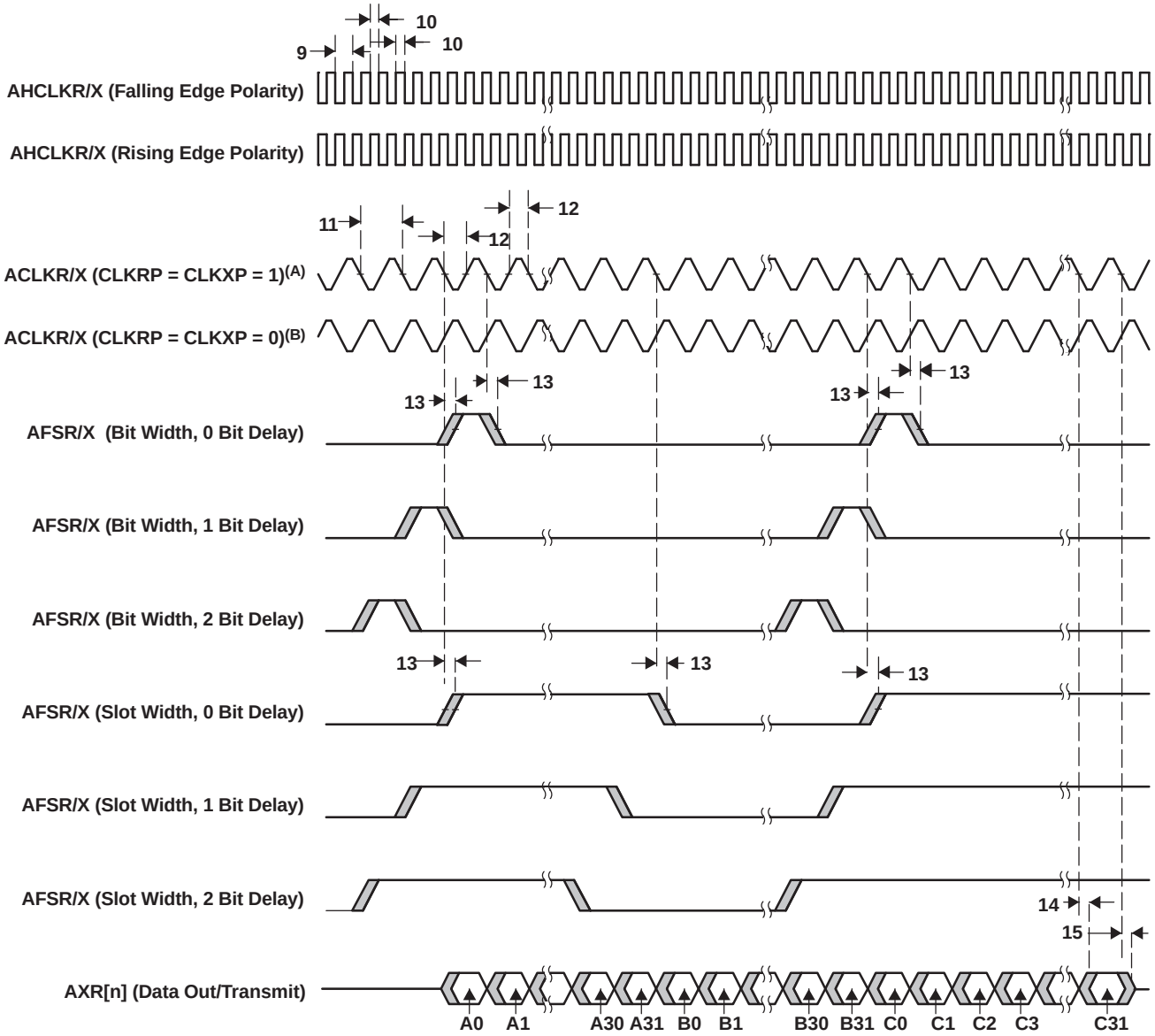

A. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

B. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

Figure 5-36. McASP Output Timings

5.16 Serial Peripheral Interface Ports (SPI0, SPI1)

Figure 5-37 is a block diagram of the SPI module, which is a simple shift register and buffer plus control logic. Data is written to the shift register before transmission occurs and is read from the buffer at the end of transmission. The SPI can operate either as a master, in which case, it initiates a transfer and drives the SPIx_CLK pin, or as a slave. Four clock phase and polarity options are supported as well as many data formatting options.

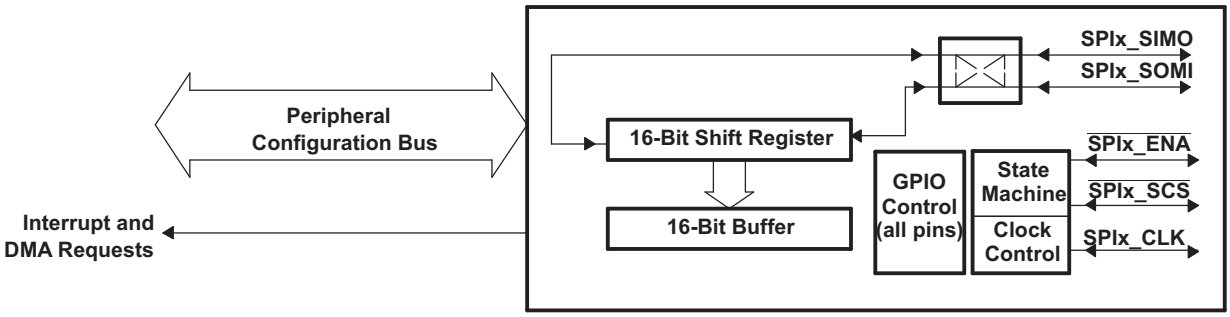

Figure 5-37. Block Diagram of SPI Module

The SPI supports 3-, 4-, and 5-pin operation with three basic pins (SPIx_CLK, SPIx_SIMO, and SPIx_SOMI) and two optional pins ($\overline{\text{SPIx_SCS}}$, $\overline{\text{SPIx_ENA}}$).

The optional $\overline{\text{SPIx_SCS}}$ (Slave Chip Select) pin is most useful to enable in slave mode when there are other slave devices on the same SPI port. The device will only shift data and drive the SPIx_SOMI pin when $\overline{\text{SPIx_SCS}}$ is held low.

In slave mode, $\overline{\text{SPIx_ENA}}$ is an optional output and can be driven in either a push-pull or open-drain manner. The $\overline{\text{SPIx_ENA}}$ output provides the status of the internal transmit buffer (SPIDAT0/1 registers). In four-pin mode with the enable option, $\overline{\text{SPIx_ENA}}$ is asserted only when the transmit buffer is full, indicating that the slave is ready to begin another transfer. In five-pin mode, the $\overline{\text{SPIx_ENA}}$ is additionally qualified by $\overline{\text{SPIx_SCS}}$ being asserted. This allows a single handshake line to be shared by multiple slaves on the same SPI bus.

In master mode, the $\overline{\text{SPIx_ENA}}$ pin is an optional input and the master can be configured to delay the start of the next transfer until the slave asserts $\overline{\text{SPIx_ENA}}$. The addition of this handshake signal simplifies SPI communications and, on average, increases SPI bus throughput since the master does not need to delay each transfer long enough to allow for the worst-case latency of the slave device. Instead, each transfer can begin as soon as both the master and slave have actually serviced the previous SPI transfer.

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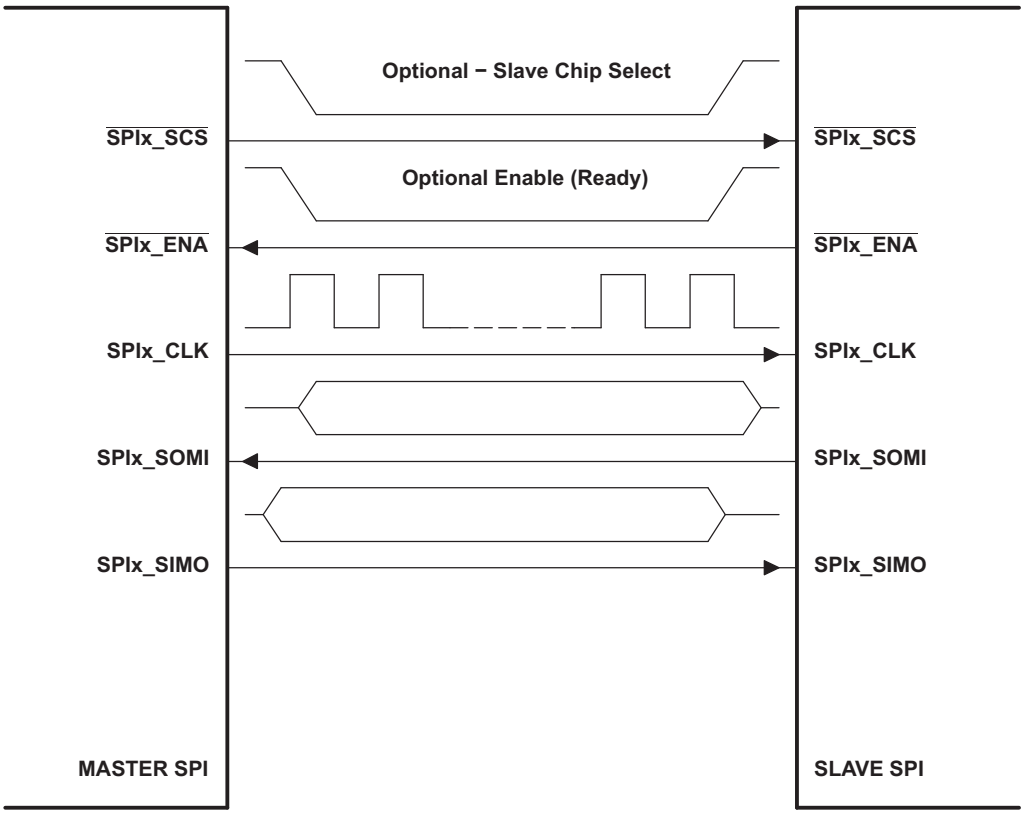

Figure 5-38. Illustration of SPI Master-to-SPI Slave Connection

5.16.1 SPI Peripheral Registers Description(s)

Table 5-51 is a list of the SPI registers. See the *TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.* – Literature Number SPRUFK9 for more details.

Table 5-51. SPIx Configuration Registers

SPI0 BYTE ADDRESS	SPI1 BYTE ADDRESS	REGISTER NAME	DESCRIPTION
0x01C4 1000	0x01E1 2000	SPIGCR0	Global Control Register 0
0x01C4 1004	0x01E1 2004	SPIGCR1	Global Control Register 1
0x01C4 1008	0x01E1 2008	SPIINT0	Interrupt Register
0x01C4 100C	0x01E1 200C	SPILVL	Interrupt Level Register
0x01C4 1010	0x01E1 2010	SPIFLG	Flag Register
0x01C4 1014	0x01E1 2014	SPIPC0	Pin Control Register 0 (Pin Function)
0x01C4 1018	0x01E1 2018	SPIPC1	Pin Control Register 1 (Pin Direction)
0x01C4 101C	0x01E1 201C	SPIPC2	Pin Control Register 2 (Pin Data In)
0x01C4 1020	0x01E1 2020	SPIPC3	Pin Control Register 3 (Pin Data Out)
0x01C4 1024	0x01E1 2024	SPIPC4	Pin Control Register 4 (Pin Data Set)
0x01C4 1028	0x01E1 2028	SPIPC5	Pin Control Register 5 (Pin Data Clear)
0x01C4 102C	0x01E1 202C	Reserved	Reserved - Do not write to this register
0x01C4 1030	0x01E1 2030	Reserved	Reserved - Do not write to this register
0x01C4 1034	0x01E1 2034	Reserved	Reserved - Do not write to this register
0x01C4 1038	0x01E1 2038	SPIDAT0	Shift Register 0 (without format select)
0x01C4 103C	0x01E1 203C	SPIDAT1	Shift Register 1 (with format select)
0x01C4 1040	0x01E1 2040	SPIBUF	Buffer Register
0x01C4 1044	0x01E1 2044	SPIEMU	Emulation Register
0x01C4 1048	0x01E1 2048	SPIDELAY	Delay Register
0x01C4 104C	0x01E1 204C	SPIDEF	Default Chip Select Register
0x01C4 1050	0x01E1 2050	SPIFMT0	Format Register 0
0x01C4 1054	0x01E1 2054	SPIFMT1	Format Register 1
0x01C4 1058	0x01E1 2058	SPIFMT2	Format Register 2
0x01C4 105C	0x01E1 205C	SPIFMT3	Format Register 3
0x01C4 1060	0x01E1 2060	Reserved	Reserved - Do not write to this register
0x01C4 1064	0x01E1 2064	INTVEC1	Interrupt Vector for SPI INT1

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5.16.2 SPI Electrical Data/Timing

5.16.2.1 Serial Peripheral Interface (SPI) Timing

Table 5-52 through Table 5-67 assume testing over recommended operating conditions (see Figure 5-39 through Figure 5-42).

Table 5-52. General Timing Requirements for SPI0 Master Modes(1)(2)

NO.				MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle Time, SPI0_CLK, All Master Modes		greater of 2P or 20 ns	256P	ns
2	$t_{w(SPCH)M}$	Pulse Width High, SPI0_CLK, All Master Modes		$0.5t_{c(SPC)M}$ - 1		ns
3	$t_{w(SPCL)M}$	Pulse Width Low, SPI0_CLK, All Master Modes		$0.5t_{c(SPC)M}$ - 1		ns
4	$t_{d(SIMO_SPC)M}$	Delay, initial data bit valid on SPI0_SIMO after initial edge on SPI0_CLK(3)	Polarity = 0, Phase = 0, to SPI0_CLK rising		5	ns
			Polarity = 0, Phase = 1, to SPI0_CLK rising		$-0.5t_{c(SPC)M}$ + 5	
			Polarity = 1, Phase = 0, to SPI0_CLK falling		5	
			Polarity = 1, Phase = 1, to SPI0_CLK falling		$-0.5t_{c(SPC)M}$ + 5	
5	$t_{d(SPC_SIMO)M}$	Delay, subsequent bits valid on SPI0_SIMO after transmit edge of SPI0_CLK	Polarity = 0, Phase = 0, from SPI0_CLK rising		5	ns
			Polarity = 0, Phase = 1, from SPI0_CLK falling		5	
			Polarity = 1, Phase = 0, from SPI0_CLK falling		5	
			Polarity = 1, Phase = 1, from SPI0_CLK rising		5	
6	$t_{oh(SPC_SIMO)M}$	Output hold time, SPI0_SIMO valid after receive edge of SPI0_CLK	Polarity = 0, Phase = 0, from SPI0_CLK falling	$0.5t_{c(SPC)M}$ -3		ns
			Polarity = 0, Phase = 1, from SPI0_CLK rising	$0.5t_{c(SPC)M}$ -3		
			Polarity = 1, Phase = 0, from SPI0_CLK rising	$0.5t_{c(SPC)M}$ -3		
			Polarity = 1, Phase = 1, from SPI0_CLK falling	$0.5t_{c(SPC)M}$ -3		
7	$t_{su(SOMI_SPC)M}$	Input Setup Time, SPI0_SOMI valid before receive edge of SPI0_CLK	Polarity = 0, Phase = 0, to SPI0_CLK falling	0		ns
			Polarity = 0, Phase = 1, to SPI0_CLK rising	0		
			Polarity = 1, Phase = 0, to SPI0_CLK rising	0		
			Polarity = 1, Phase = 1, to SPI0_CLK falling	0		
8	$t_{ih(SPC_SOMI)M}$	Input Hold Time, SPI0_SOMI valid after receive edge of SPI0_CLK	Polarity = 0, Phase = 0, from SPI0_CLK falling	5		ns
			Polarity = 0, Phase = 1, from SPI0_CLK rising	5		
			Polarity = 1, Phase = 0, from SPI0_CLK rising	5		
			Polarity = 1, Phase = 1, from SPI0_CLK falling	5		

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(2) P = SYSCLK2 period
(3) First bit may be MSB or LSB depending upon SPI configuration. MO(0) refers to first bit and MO(n) refers to last bit output on SPI0_SIMO. MI(0) refers to the first bit input and MI(n) refers to the last bit input on SPI0_SOMI.

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Table 5-53. General Timing Requirements for SPI0 Slave Modes[1][2]

NO.				MIN	MAX	UNIT
9	$t_{c(SPC)S}$	Cycle Time, SPI0_CLK, All Slave Modes		greater of 3P or 20 ns		ns
10	$t_{w(SPCH)S}$	Pulse Width High, SPI0_CLK, All Slave Modes		18		ns
11	$t_{w(SPCL)S}$	Pulse Width Low, SPI0_CLK, All Slave Modes		18		ns
12	$t_{su(SOMI_SPC)S}$	Setup time, transmit data written to SPI before initial clock edge from master.[3] [4]	Polarity = 0, Phase = 0, to SPI0_CLK rising	2P		ns
			Polarity = 0, Phase = 1, to SPI0_CLK rising	2P		
			Polarity = 1, Phase = 0, to SPI0_CLK falling	2P		
			Polarity = 1, Phase = 1, to SPI0_CLK falling	2P		
13	$t_{d(SPC_SOMI)S}$	Delay, subsequent bits valid on SPI0_SOMI after transmit edge of SPI0_CLK	Polarity = 0, Phase = 0, from SPI0_CLK rising		19	ns
			Polarity = 0, Phase = 1, from SPI0_CLK falling		19	
			Polarity = 1, Phase = 0, from SPI0_CLK falling		19	
			Polarity = 1, Phase = 1, from SPI0_CLK rising		19	
14	$t_{oh(SPC_SOMI)S}$	Output hold time, SPI0_SOMI valid after receive edge of SPI0_CLK	Polarity = 0, Phase = 0, from SPI0_CLK falling	$0.5t_{c(SPC)S}$ -3		ns
			Polarity = 0, Phase = 1, from SPI0_CLK rising	$0.5t_{c(SPC)S}$ -3		
			Polarity = 1, Phase = 0, from SPI0_CLK rising	$0.5t_{c(SPC)S}$ -3		
			Polarity = 1, Phase = 1, from SPI0_CLK falling	$0.5t_{c(SPC)S}$ -3		
15	$t_{su(SIMO_SPC)S}$	Input Setup Time, SPI0_SIMO valid before receive edge of SPI0_CLK	Polarity = 0, Phase = 0, to SPI0_CLK falling	0		ns
			Polarity = 0, Phase = 1, to SPI0_CLK rising	0		
			Polarity = 1, Phase = 0, to SPI0_CLK rising	0		
			Polarity = 1, Phase = 1, to SPI0_CLK falling	0		
16	$t_{ih(SPC_SIMO)S}$	Input Hold Time, SPI0_SIMO valid after receive edge of SPI0_CLK	Polarity = 0, Phase = 0, from SPI0_CLK falling	5		ns
			Polarity = 0, Phase = 1, from SPI0_CLK rising	5		
			Polarity = 1, Phase = 0, from SPI0_CLK rising	5		
			Polarity = 1, Phase = 1, from SPI0_CLK falling	5		

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(2) P = SYSCLK2 period
(3) First bit may be MSB or LSB depending upon SPI configuration. SO(0) refers to first bit and SO(n) refers to last bit output on SPI0_SOMI. SI(0) refers to the first bit input and SI(n) refers to the last bit input on SPI0_SIMO.
(4) Measured from the termination of the write of new data to the SPI module, In analyzing throughput requirements, additional internal bus cycles must be accounted for to allow data to be written to the SPI module by either the DSP CPU or the dMAX.

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Table 5-54. Additional[1] SPI0 Master Timings, 4-Pin Enable Option[2] [3]

NO.				MIN	MAX	UNIT
17	$t_{d(ENA_SPC)M}$	Delay from slave assertion of SPI0_ENA active to first SPI0_CLK from master.[4]	Polarity = 0, Phase = 0, to SPI0_CLK rising		3P + 3.6	ns
			Polarity = 0, Phase = 1, to SPI0_CLK rising		$0.5t_{c(SPC)M}$ + 3P + 3.6	
			Polarity = 1, Phase = 0, to SPI0_CLK falling		3P + 3.6	
			Polarity = 1, Phase = 1, to SPI0_CLK falling		$0.5t_{c(SPC)M}$ + 3P + 3.6	
18	$t_{d(SPC_ENA)M}$	Max delay for slave to deassert SPI0_ENA after final SPI0_CLK edge to ensure master does not begin the next transfer.[5]	Polarity = 0, Phase = 0, from SPI0_CLK falling		P+5	ns
			Polarity = 0, Phase = 1, from SPI0_CLK falling		$0.5t_{c(SPC)M}$+P+5	
			Polarity = 1, Phase = 0, from SPI0_CLK rising		P+5	
			Polarity = 1, Phase = 1, from SPI0_CLK rising		$0.5t_{c(SPC)M}$+P+5	

(1) These parameters are in addition to the general timings for SPI master modes (Table 5-52).
(2) P = SYSCLK2 period
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(4) In the case where the master SPI is ready with new data before SPI0_ENA assertion.
(5) In the case where the master SPI is ready with new data before SPI0_ENA deassertion.

Table 5-55. Additional[1] SPI0 Master Timings, 4-Pin Chip Select Option[2] [3] [4]

NO.				MIN	MAX	UNIT
19	$t_{d(SCS_SPC)M}$	Delay from SPI0_SCS active to first SPI0_CLK[5] [6]	Polarity = 0, Phase = 0, to SPI0_CLK rising	2P -5		ns
			Polarity = 0, Phase = 1, to SPI0_CLK rising	$0.5t_{c(SPC)M}$ + 2P -5		
			Polarity = 1, Phase = 0, to SPI0_CLK falling	2P -5		
			Polarity = 1, Phase = 1, to SPI0_CLK falling	$0.5t_{c(SPC)M}$ + 2P -5		
20	$t_{d(SPC_SCS)M}$	Delay from final SPI0_CLK edge to master deasserting SPI0_SCS[7] [8]	Polarity = 0, Phase = 0, from SPI0_CLK falling	$0.5t_{c(SPC)M}$ P-3		ns
			Polarity = 0, Phase = 1, from SPI0_CLK falling	P-3		
			Polarity = 1, Phase = 0, from SPI0_CLK rising	$0.5t_{c(SPC)M}$ P-3		
			Polarity = 1, Phase = 1, from SPI0_CLK rising	P-3		

(1) These parameters are in addition to the general timings for SPI master modes (Table 5-52).
(2) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(3) P = SYSCLK2 period
(4) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(5) In the case where the master SPI is ready with new data before SPI0_SCS assertion.
(6) This delay can be increased under software control by the register bit field SPIDELAY.C2TDELAY[4:0].
(7) Except for modes when SPIDAT1.CSHOLD is enabled and there is additional data to transmit. In this case, SPI0_SCS will remain asserted.
(8) This delay can be increased under software control by the register bit field SPIDELAY.T2CDELAY[4:0].

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Table 5-56. Additional[1] SPI0 Master Timings, 5-Pin Option[2][3] [4]

NO.				MIN	MAX	UNIT
18	$t_{d(SPC_ENA)M}$	Max delay for slave to deassert SPI0_ENA after final SPI0_CLK edge to ensure master does not begin the next transfer.[5]	Polarity = 0, Phase = 0, from SPI0_CLK falling		P+5	ns
			Polarity = 0, Phase = 1, from SPI0_CLK falling		$0.5t_{c(SPC)M}$+P+5	
			Polarity = 1, Phase = 0, from SPI0_CLK rising		P+5	
			Polarity = 1, Phase = 1, from SPI0_CLK rising		$0.5t_{c(SPC)M}$+P+5	
20	$t_{d(SPC_SCS)M}$	Delay from final SPI0_CLK edge to master deasserting SPI0_SCS [6] [7]	Polarity = 0, Phase = 0, from SPI0_CLK falling	$0.5t_{c(SPC)M}$+P-3		ns
			Polarity = 0, Phase = 1, from SPI0_CLK falling	P-3		
			Polarity = 1, Phase = 0, from SPI0_CLK rising	$0.5t_{c(SPC)M}$+P-3		
			Polarity = 1, Phase = 1, from SPI0_CLK rising	P-3		
21	$t_{d(SCSL_ENAL)M}$	Max delay for slave SPI to drive SPI0_ENA valid after master asserts SPI0_SCS to delay the master from beginning the next transfer,			C2TDELAY + P	ns
22	$t_{d(SCS_SPC)M}$	Delay from SPI0_SCS active to first SPI0_CLK[8] [9] [10]	Polarity = 0, Phase = 0, to SPI0_CLK rising	2P -5		ns
			Polarity = 0, Phase = 1, to SPI0_CLK rising	$0.5t_{c(SPC)M}$ + 2P -5		
			Polarity = 1, Phase = 0, to SPI0_CLK falling	2P -5		
			Polarity = 1, Phase = 1, to SPI0_CLK falling	$0.5t_{c(SPC)M}$ + 2P -5		
23	$t_{d(ENA_SPC)M}$	Delay from assertion of SPI0_ENA low to first SPI0_CLK edge.[11]	Polarity = 0, Phase = 0, to SPI0_CLK rising		3P + 3.6	ns
			Polarity = 0, Phase = 1, to SPI0_CLK rising		$0.5t_{c(SPC)M}$ + 3P + 3.6	
			Polarity = 1, Phase = 0, to SPI0_CLK falling		3P + 3.6	
			Polarity = 1, Phase = 1, to SPI0_CLK falling		$0.5t_{c(SPC)M}$ + 3P + 3.6	

(1) These parameters are in addition to the general timings for SPI master modes (Table 5-53).
(2) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(3) P = SYSCLK2 period
(4) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(5) In the case where the master SPI is ready with new data before SPI0_ENA deassertion.
(6) Except for modes when SPIDAT1.CSHOLD is enabled and there is additional data to transmit. In this case, SPI0_SCS will remain asserted.
(7) This delay can be increased under software control by the register bit field SPIDELAY.T2CDELAY[4:0].
(8) If SPI0_ENA is asserted immediately such that the transmission is not delayed by SPI0_ENA.
(9) In the case where the master SPI is ready with new data before SPI0_SCS assertion.
(10) This delay can be increased under software control by the register bit field SPIDELAY.C2TDELAY[4:0].
(11) If SPI0_ENA was initially deasserted high and SPI0_CLK is delayed.

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Table 5-57. Additional[1] SPI0 Slave Timings, 4-Pin Enable Option[2][3] [4]

NO.				MIN	MAX	UNIT
24	$t_{d(SPC_ENAH)S}$	Delay from final SPI0_CLK edge to slave deasserting $\overline{SPI0_ENA}$.	Polarity = 0, Phase = 0, from SPI0_CLK falling	1.5 P -3	2.5 P + 18.5	ns
			Polarity = 0, Phase = 1, from SPI0_CLK falling	$-0.5t_{c(SPC)M}$ + 1.5 P -3	$-0.5t_{c(SPC)M}$ + 2.5 P + 18.5	
			Polarity = 1, Phase = 0, from SPI0_CLK rising	1.5 P -3	2.5 P + 18.5	
			Polarity = 1, Phase = 1, from SPI0_CLK rising	$-0.5t_{c(SPC)M}$ + 1.5 P -3	$-0.5t_{c(SPC)M}$ + 2.5 P + 18.5	

(1) These parameters are in addition to the general timings for SPI slave modes (Table 5-53).
(2) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(3) P = SYSCLK2 period
(4) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.

Table 5-58. Additional[1] SPI0 Slave Timings, 4-Pin Chip Select Option[2][3] [4]

NO.				MIN	MAX	UNIT
25	$t_{d(SCSL_SPC)S}$	Required delay from $\overline{SPI0_SCS}$ asserted at slave to first SPI0_CLK edge at slave.		2P		ns
26	$t_{d(SPC_SCSH)S}$	Required delay from final SPI0_CLK edge before $\overline{SPI0_SCS}$ is deasserted.	Polarity = 0, Phase = 0, from SPI0_CLK falling	$0.5t_{c(SPC)M}$ + 2P+5		ns
			Polarity = 0, Phase = 1, from SPI0_CLK falling	2P+5		
			Polarity = 1, Phase = 0, from SPI0_CLK rising	$0.5t_{c(SPC)M}$ + 2P+5		
			Polarity = 1, Phase = 1, from SPI0_CLK rising	2P+5		
27	$t_{ena(SCSL_SOMI)S}$	Delay from master asserting $\overline{SPI0_SCS}$ to slave driving SPI0_SOMI valid			P + 18.5	ns
28	$t_{dis(SCSH_SOMI)S}$	Delay from master deasserting $\overline{SPI0_SCS}$ to slave 3-stating SPI0_SOMI			P + 18.5	ns

(1) These parameters are in addition to the general timings for SPI slave modes (Table 5-53).
(2) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(3) P = SYSCLK2 period
(4) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.

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Table 5-59. Additional[1] SPI0 Slave Timings, 5-Pin Option[2][3] [4]

NO.				MIN	MAX	UNIT
25	$t_{d(SCSL_SPC)S}$	Required delay from $\overline{SPI0_SCS}$ asserted at slave to first SPI0_CLK edge at slave.		2P		ns
26	$t_{d(SPC_SCSH)S}$	Required delay from final SPI0_CLK edge before $\overline{SPI0_SCS}$ is deasserted.	Polarity = 0, Phase = 0, from SPI0_CLK falling	$0.5t_{c(SPC)M}$ + 2P+5		ns
			Polarity = 0, Phase = 1, from SPI0_CLK falling	2P+5		
			Polarity = 1, Phase = 0, from SPI0_CLK rising	$0.5t_{c(SPC)M}$ + 2P+5		
			Polarity = 1, Phase = 1, from SPI0_CLK rising	2P+5		
27	$t_{ena(SCSL_SOMI)S}$	Delay from master asserting $\overline{SPI0_SCS}$ to slave driving SPI0_SOMI valid			P + 18.5	ns
28	$t_{dis(SCSH_SOMI)S}$	Delay from master deasserting $\overline{SPI0_SCS}$ to slave 3-stating SPI0_SOMI			P + 18.5	ns
29	$t_{ena(SCSL_ENA)S}$	Delay from master deasserting $\overline{SPI0_SCS}$ to slave driving $\overline{SPI0_ENA}$ valid			18.5	ns
30	$t_{dis(SPC_ENA)S}$	Delay from final clock receive edge on SPI0_CLK to slave 3-stating or driving high $\overline{SPI0_ENA}$.[5]	Polarity = 0, Phase = 0, from SPI0_CLK falling		2.5 P + 18.5	ns
			Polarity = 0, Phase = 1, from SPI0_CLK rising		2.5 P + 18.5	
			Polarity = 1, Phase = 0, from SPI0_CLK rising		2.5 P + 18.5	
			Polarity = 1, Phase = 1, from SPI0_CLK falling		2.5 P + 18.5	

(1) These parameters are in addition to the general timings for SPI slave modes (Table 5-53).
(2) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(3) P = SYSCLK2 period
(4) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.
(5) $\overline{SPI0_ENA}$ is driven low after the transmission completes if the SPIINT0.ENABLE_HIGHZ bit is programmed to 0. Otherwise it is tri-stated. If tri-stated, an external pullup resistor should be used to provide a valid level to the master. This option is useful when tying several SPI slave devices to a single master.

Table 5-60. General Timing Requirements for SPI1 Master Modes[1][2]

NO.				MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle Time, SPI1_CLK, All Master Modes		greater of 3P or 20 ns	256P	ns
2	$t_{w(SPCH)M}$	Pulse Width High, SPI1_CLK, All Master Modes		$0.5t_{c(SPC)M}$ - 1		ns
3	$t_{w(SPCL)M}$	Pulse Width Low, SPI1_CLK, All Master Modes		$0.5t_{c(SPC)M}$ - 1		ns
4	$t_{d(SIMO_SPC)M}$	Delay, initial data bit valid on SPI1_SIMO after initial edge on SPI1_CLK[3]	Polarity = 0, Phase = 0, to SPI1_CLK rising	5		ns
			Polarity = 0, Phase = 1, to SPI1_CLK rising	$-0.5t_{c(SPC)M}$ + 5		
			Polarity = 1, Phase = 0, to SPI1_CLK falling	5		
			Polarity = 1, Phase = 1, to SPI1_CLK falling	$-0.5t_{c(SPC)M}$ + 5		
5	$t_{d(SPC_SIMO)M}$	Delay, subsequent bits valid on SPI1_SIMO after transmit edge of SPI1_CLK	Polarity = 0, Phase = 0, from SPI1_CLK rising	5		ns
			Polarity = 0, Phase = 1, from SPI1_CLK falling	5		
			Polarity = 1, Phase = 0, from SPI1_CLK falling	5		
			Polarity = 1, Phase = 1, from SPI1_CLK rising	5		

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(2) P = SYSCLK2 period
(3) First bit may be MSB or LSB depending upon SPI configuration. MO(0) refers to first bit and MO(n) refers to last bit output on SPI1_SIMO. MI(0) refers to the first bit input and MI(n) refers to the last bit input on SPI1_SOMI.

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Table 5-60. General Timing Requirements for SPI1 Master Modes[1][2] (continued)

NO.				MIN	MAX	UNIT
6	$t_{oh(SPC_SIMO)M}$	Output hold time, SPI1_SIMO valid after receive edge of SPI1_CLK	Polarity = 0, Phase = 0, from SPI1_CLK falling	$0.5t_{c(SPC)M}$ -3		ns
			Polarity = 0, Phase = 1, from SPI1_CLK rising	$0.5t_{c(SPC)M}$ -3		
			Polarity = 1, Phase = 0, from SPI1_CLK rising	$0.5t_{c(SPC)M}$ -3		
			Polarity = 1, Phase = 1, from SPI1_CLK falling	$0.5t_{c(SPC)M}$ -3		
7	$t_{su(SOMI_SPC)M}$	Input Setup Time, SPI1_SOMI valid before receive edge of SPI1_CLK	Polarity = 0, Phase = 0, to SPI1_CLK falling	0		ns
			Polarity = 0, Phase = 1, to SPI1_CLK rising	0		
			Polarity = 1, Phase = 0, to SPI1_CLK rising	0		
			Polarity = 1, Phase = 1, to SPI1_CLK falling	0		
8	$t_{ih(SPC_SOMI)M}$	Input Hold Time, SPI1_SOMI valid after receive edge of SPI1_CLK	Polarity = 0, Phase = 0, from SPI1_CLK falling	5		ns
			Polarity = 0, Phase = 1, from SPI1_CLK rising	5		
			Polarity = 1, Phase = 0, from SPI1_CLK rising	5		
			Polarity = 1, Phase = 1, from SPI1_CLK falling	5		

Table 5-61. General Timing Requirements for SPI1 Slave Modes[1][2]

NO.				MIN	MAX	UNIT
9	$t_{c(SPC)S}$	Cycle Time, SPI1_CLK, All Slave Modes		greater of 3P or 40 ns		ns
10	$t_{w(SPCH)S}$	Pulse Width High, SPI1_CLK, All Slave Modes		18		ns
11	$t_{w(SPCL)S}$	Pulse Width Low, SPI1_CLK, All Slave Modes		18		ns
12	$t_{su(SOMI_SPC)S}$	Setup time, transmit data written to SPI before initial clock edge from master.[3] [4]	Polarity = 0, Phase = 0, to SPI1_CLK rising	2P		ns
			Polarity = 0, Phase = 1, to SPI1_CLK rising	2P		
			Polarity = 1, Phase = 0, to SPI1_CLK falling	2P		
			Polarity = 1, Phase = 1, to SPI1_CLK falling	2P		
13	$t_{d(SPC_SOMI)S}$	Delay, subsequent bits valid on SPI1_SOMI after transmit edge of SPI1_CLK	Polarity = 0, Phase = 0, from SPI1_CLK rising		19	ns
			Polarity = 0, Phase = 1, from SPI1_CLK falling		19	
			Polarity = 1, Phase = 0, from SPI1_CLK falling		19	
			Polarity = 1, Phase = 1, from SPI1_CLK rising		19	

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(2) P = SYSCLK2 period
(3) First bit may be MSB or LSB depending upon SPI configuration. SO(0) refers to first bit and SO(n) refers to last bit output on SPI1_SOMI. SI(0) refers to the first bit input and SI(n) refers to the last bit input on SPI1_SIMO.
(4) Measured from the termination of the write of new data to the SPI module, In analyzing throughput requirements, additional internal bus cycles must be accounted for to allow data to be written to the SPI module by either the DSP CPU or the dMAX.

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Table 5-61. General Timing Requirements for SPI1 Slave Modes[1][2] (continued)

NO.				MIN	MAX	UNIT
14	$t_{oh(SPC_SOMI)S}$	Output hold time, SPI1_SOMI valid after receive edge of SPI1_CLK	Polarity = 0, Phase = 0, from SPI1_CLK falling	$0.5t_{c(SPC)S}$ -3		ns
			Polarity = 0, Phase = 1, from SPI1_CLK rising	$0.5t_{c(SPC)S}$ -3		
			Polarity = 1, Phase = 0, from SPI1_CLK rising	$0.5t_{c(SPC)S}$ -3		
			Polarity = 1, Phase = 1, from SPI1_CLK falling	$0.5t_{c(SPC)S}$ -3		
15	$t_{su(SIMO_SPC)S}$	Input Setup Time, SPI1_SIMO valid before receive edge of SPI1_CLK	Polarity = 0, Phase = 0, to SPI1_CLK falling	0		ns
			Polarity = 0, Phase = 1, to SPI1_CLK rising	0		
			Polarity = 1, Phase = 0, to SPI1_CLK rising	0		
			Polarity = 1, Phase = 1, to SPI1_CLK falling	0		
16	$t_{ih(SPC_SIMO)S}$	Input Hold Time, SPI1_SIMO valid after receive edge of SPI1_CLK	Polarity = 0, Phase = 0, from SPI1_CLK falling	5		ns
			Polarity = 0, Phase = 1, from SPI1_CLK rising	5		
			Polarity = 1, Phase = 0, from SPI1_CLK rising	5		
			Polarity = 1, Phase = 1, from SPI1_CLK falling	5		

Table 5-62. Additional[1] SPI1 Master Timings, 4-Pin Enable Option[2][3] [4]

NO.				MIN	MAX	UNIT
17	$t_{d(ENA_SPC)M}$	Delay from slave assertion of SPI1_ENA active to first SPI1_CLK from master.[5]	Polarity = 0, Phase = 0, to SPI1_CLK rising	P + 3		ns
			Polarity = 0, Phase = 1, to SPI1_CLK rising	$0.5t_{c(SPC)M}$ + P + 3		
			Polarity = 1, Phase = 0, to SPI1_CLK falling	P + 3		
			Polarity = 1, Phase = 1, to SPI1_CLK falling	$0.5t_{c(SPC)M}$ + P + 3		
18	$t_{d(SPC_ENA)M}$	Max delay for slave to deassert SPI1_ENA after final SPI1_CLK edge to ensure master does not begin the next transfer.[6]	Polarity = 0, Phase = 0, from SPI1_CLK falling	P+5		ns
			Polarity = 0, Phase = 1, from SPI1_CLK falling	$0.5t_{c(SPC)M}$+P+5		
			Polarity = 1, Phase = 0, from SPI1_CLK rising	P+5		
			Polarity = 1, Phase = 1, from SPI1_CLK rising	$0.5t_{c(SPC)M}$+P+5		

(1) These parameters are in addition to the general timings for SPI master modes (Table 5-60).
(2) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(3) P = SYSCLK2 period
(4) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(5) In the case where the master SPI is ready with new data before SPI1_ENA assertion.
(6) In the case where the master SPI is ready with new data before SPI1_ENA deassertion.

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Table 5-63. Additional[1] SPI1 Master Timings, 4-Pin Chip Select Option[2][3] [4]

NO.				MIN	MAX	UNIT
19	$t_{d(SCS_SPC)M}$	Delay from SPI1_SCS active to first SPI1_CLK[5] [6]	Polarity = 0, Phase = 0, to SPI1_CLK rising	2P -5		ns
			Polarity = 0, Phase = 1, to SPI1_CLK rising	$0.5t_{c(SPC)M}$ + 2P -5		
			Polarity = 1, Phase = 0, to SPI1_CLK falling	2P -5		
			Polarity = 1, Phase = 1, to SPI1_CLK falling	$0.5t_{c(SPC)M}$ + 2P -5		
20	$t_{d(SPC_SCS)M}$	Delay from final SPI1_CLK edge to master deasserting SPI1_SCS [7] [8]	Polarity = 0, Phase = 0, from SPI1_CLK falling	$0.5t_{c(SPC)M}$-3		ns
			Polarity = 0, Phase = 1, from SPI1_CLK falling	-3		
			Polarity = 1, Phase = 0, from SPI1_CLK rising	$0.5t_{c(SPC)M}$-3		
			Polarity = 1, Phase = 1, from SPI1_CLK rising	-3		

(1) These parameters are in addition to the general timings for SPI master modes (Table 5-60).
(2) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(3) P = SYSCLK2 period
(4) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(5) In the case where the master SPI is ready with new data before SPI1_SCS assertion.
(6) This delay can be increased under software control by the register bit field SPIDELAY.C2TDELAY[4:0].
(7) Except for modes when SPIDAT1.CSHOLD is enabled and there is additional data to transmit. In this case, SPI1_SCS will remain asserted.
(8) This delay can be increased under software control by the register bit field SPIDELAY.T2CDELAY[4:0].

Table 5-64. Additional[1] SPI1 Master Timings, 5-Pin Option[2][3] [4]

NO.				MIN	MAX	UNIT
18	$t_{d(SPC_ENA)M}$	Max delay for slave to deassert SPI1_ENA after final SPI1_CLK edge to ensure master does not begin the next transfer.[5]	Polarity = 0, Phase = 0, from SPI1_CLK falling		P+3	ns
			Polarity = 0, Phase = 1, from SPI1_CLK falling		$0.5t_{c(SPC)M}$+P+3	
			Polarity = 1, Phase = 0, from SPI1_CLK rising		P+3	
			Polarity = 1, Phase = 1, from SPI1_CLK rising		$0.5t_{c(SPC)M}$+P+3	
20	$t_{d(SPC_SCS)M}$	Delay from final SPI1_CLK edge to master deasserting SPI1_SCS [6] [7]	Polarity = 0, Phase = 0, from SPI1_CLK falling	$0.5t_{c(SPC)M}$-3		ns
			Polarity = 0, Phase = 1, from SPI1_CLK falling	-3		
			Polarity = 1, Phase = 0, from SPI1_CLK rising	$0.5t_{c(SPC)M}$-3		
			Polarity = 1, Phase = 1, from SPI1_CLK rising	-3		
21	$t_{d(SCSL_ENAL)M}$	Max delay for slave SPI to drive SPI1_ENA valid after master asserts SPI1_SCS to delay the master from beginning the next transfer,			C2TDELAY + P	ns

(1) These parameters are in addition to the general timings for SPI master modes (Table 5-61).
(2) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(3) P = SYSCLK2 period
(4) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(5) In the case where the master SPI is ready with new data before SPI1_ENA deassertion.
(6) Except for modes when SPIDAT1.CSHOLD is enabled and there is additional data to transmit. In this case, SPI1_SCS will remain asserted.
(7) This delay can be increased under software control by the register bit field SPIDELAY.T2CDELAY[4:0].

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Table 5-64. Additional[1] SPI1 Master Timings, 5-Pin Option[2][3] [4] (continued)

NO.				MIN	MAX	UNIT
22	$t_{d(SCS_SPC)M}$	Delay from $\overline{SPI1_SCS}$ active to first SPI1_CLK[8] [9] [10]	Polarity = 0, Phase = 0, to SPI1_CLK rising	2P -5		ns
			Polarity = 0, Phase = 1, to SPI1_CLK rising	$0.5t_{c(SPC)M}$ + 2P -5		
			Polarity = 1, Phase = 0, to SPI1_CLK falling	2P -5		
			Polarity = 1, Phase = 1, to SPI1_CLK falling	$0.5t_{c(SPC)M}$ + 2P -5		
23	$t_{d(ENA_SPC)M}$	Delay from assertion of $\overline{SPI1_ENA}$ low to first SPI1_CLK edge.[11]	Polarity = 0, Phase = 0, to SPI1_CLK rising		P + 3	ns
			Polarity = 0, Phase = 1, to SPI1_CLK rising		$0.5t_{c(SPC)M}$ + P + 3	
			Polarity = 1, Phase = 0, to SPI1_CLK falling		P + 3	
			Polarity = 1, Phase = 1, to SPI1_CLK falling		$0.5t_{c(SPC)M}$ + P + 3	

(8) If $\overline{SPI1_ENA}$ is asserted immediately such that the transmission is not delayed by $\overline{SPI1_ENA}$.
(9) In the case where the master SPI is ready with new data before $\overline{SPI1_SCS}$ assertion.
(10) This delay can be increased under software control by the register bit field SPIDELAY.C2TDELAY[4:0].
(11) If $\overline{SPI1_ENA}$ was initially deasserted high and SPI1_CLK is delayed.

Table 5-65. Additional[1] SPI1 Slave Timings, 4-Pin Enable Option[2][3] [4]

NO.				MIN	MAX	UNIT
24	$t_{d(SPC_ENAH)S}$	Delay from final SPI1_CLK edge to slave deasserting $\overline{SPI1_ENA}$.	Polarity = 0, Phase = 0, from SPI1_CLK falling	1.5 P -3	2.5 P + 19	ns
			Polarity = 0, Phase = 1, from SPI1_CLK falling	$-0.5t_{c(SPC)M}$ + 1.5 P -3	$-0.5t_{c(SPC)M}$ + 2.5 P + 19	
			Polarity = 1, Phase = 0, from SPI1_CLK rising	1.5 P -3	2.5 P + 19	
			Polarity = 1, Phase = 1, from SPI1_CLK rising	$-0.5t_{c(SPC)M}$ + 1.5 P -3	$-0.5t_{c(SPC)M}$ + 2.5 P + 19	

(1) These parameters are in addition to the general timings for SPI slave modes (Table 5-61).
(2) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(3) P = SYSCLK2 period
(4) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.

Table 5-66. Additional[1] SPI1 Slave Timings, 4-Pin Chip Select Option[2][3] [4]

NO.				MIN	MAX	UNIT
25	$t_{d(SCSL_SPC)S}$	Required delay from $\overline{SPI1_SCS}$ asserted at slave to first SPI1_CLK edge at slave.		2P		ns
26	$t_{d(SPC_SCSH)S}$	Required delay from final SPI1_CLK edge before $\overline{SPI1_SCS}$ is deasserted.	Polarity = 0, Phase = 0, from SPI1_CLK falling	$0.5t_{c(SPC)M}$ + 2P+5		ns
			Polarity = 0, Phase = 1, from SPI1_CLK falling	2P+5		
			Polarity = 1, Phase = 0, from SPI1_CLK rising	$0.5t_{c(SPC)M}$ + 2P+5		
			Polarity = 1, Phase = 1, from SPI1_CLK rising	2P+5		
27	$t_{ena(SCSL_SOMI)S}$	Delay from master asserting $\overline{SPI1_SCS}$ to slave driving SPI1_SOMI valid			P + 19	ns
28	$t_{dis(SCSH_SOMI)S}$	Delay from master deasserting $\overline{SPI1_SCS}$ to slave 3-stating SPI1_SOMI			P + 19	ns

(1) These parameters are in addition to the general timings for SPI slave modes (Table 5-61).
(2) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(3) P = SYSCLK2 period
(4) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.

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Table 5-67. Additional[1] SPI1 Slave Timings, 5-Pin Option[2][3] [4]

NO.				MIN	MAX	UNIT
25	$t_{d(SCSL_SPC)S}$	Required delay from $\overline{SPI1_SCS}$ asserted at slave to first SPI1_CLK edge at slave.		2P		ns
26	$t_{d(SPC_SCSH)S}$	Required delay from final SPI1_CLK edge before $\overline{SPI1_SCS}$ is deasserted.	Polarity = 0, Phase = 0, from SPI1_CLK falling	$0.5t_{c(SPC)M}$ + 2P		ns
			Polarity = 0, Phase = 1, from SPI1_CLK falling	2P		
			Polarity = 1, Phase = 0, from SPI1_CLK rising	$0.5t_{c(SPC)M}$ + 2P		
			Polarity = 1, Phase = 1, from SPI1_CLK rising	2P		
27	$t_{ena(SCSL_SOMI)S}$	Delay from master asserting $\overline{SPI1_SCS}$ to slave driving SPI1_SOMI valid			P + 19	ns
28	$t_{dis(SCSH_SOMI)S}$	Delay from master deasserting $\overline{SPI1_SCS}$ to slave 3-stating SPI1_SOMI			P + 19	ns
29	$t_{ena(SCSL_ENA)S}$	Delay from master deasserting $\overline{SPI1_SCS}$ to slave driving $\overline{SPI1_ENA}$ valid			19	ns
30	$t_{dis(SPC_ENA)S}$	Delay from final clock receive edge on SPI1_CLK to slave 3-stating or driving high $\overline{SPI1_ENA}$.[5]	Polarity = 0, Phase = 0, from SPI1_CLK falling		2.5 P + 19	ns
			Polarity = 0, Phase = 1, from SPI1_CLK rising		2.5 P + 19	
			Polarity = 1, Phase = 0, from SPI1_CLK rising		2.5 P + 19	
			Polarity = 1, Phase = 1, from SPI1_CLK falling		2.5 P + 19	

(1) These parameters are in addition to the general timings for SPI slave modes (Table 5-61).
(2) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(3) P = SYSCLK2 period
(4) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.
(5) $\overline{SPI1_ENA}$ is driven low after the transmission completes if the SPIINT0.ENABLE_HIGHZ bit is programmed to 0. Otherwise it is tri-stated. If tri-stated, an external pullup resistor should be used to provide a valid level to the master. This option is useful when tying several SPI slave devices to a single master.

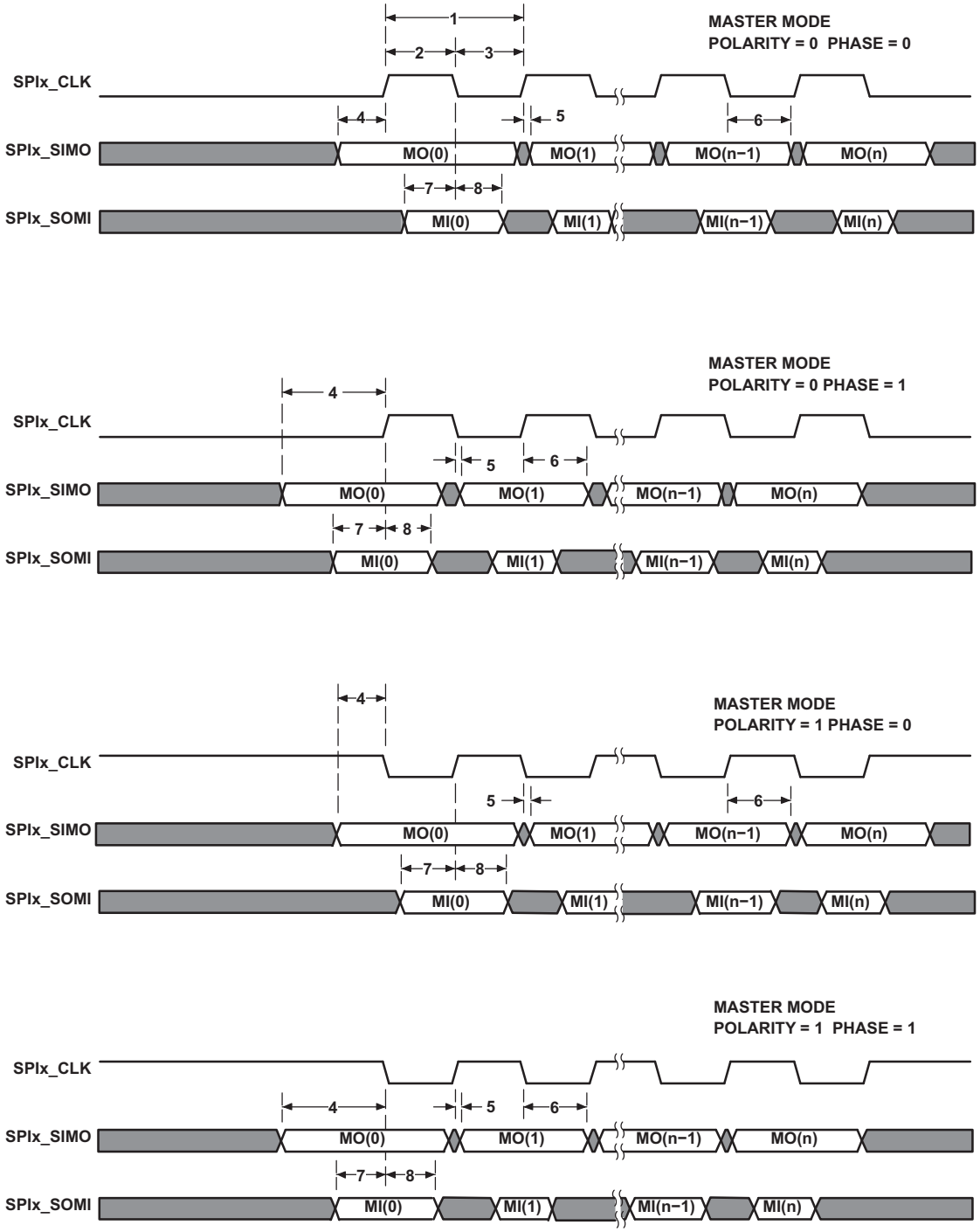

Figure 5-39. SPI Timings—Master Mode

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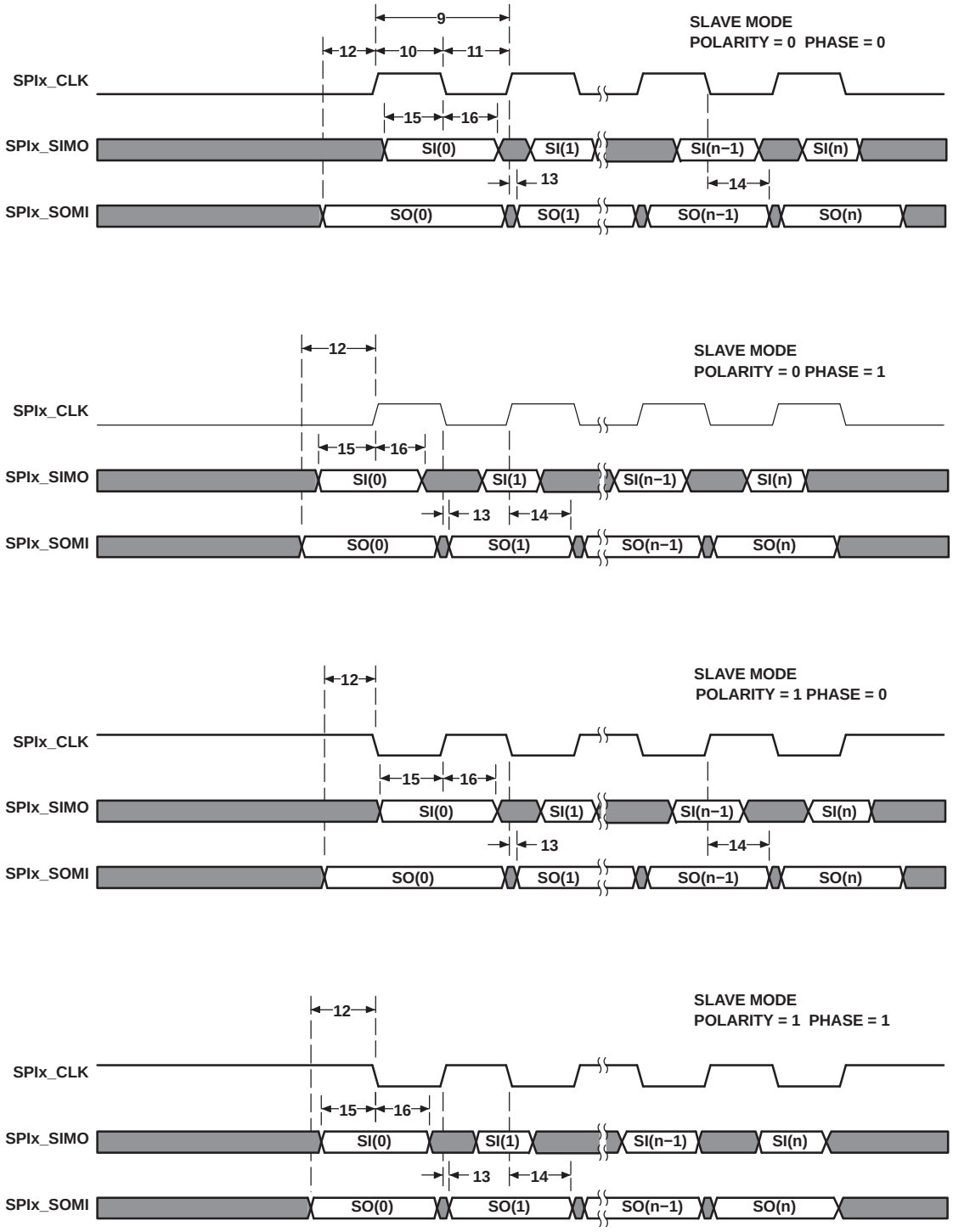

Figure 5-40. SPI Timings—Slave Mode

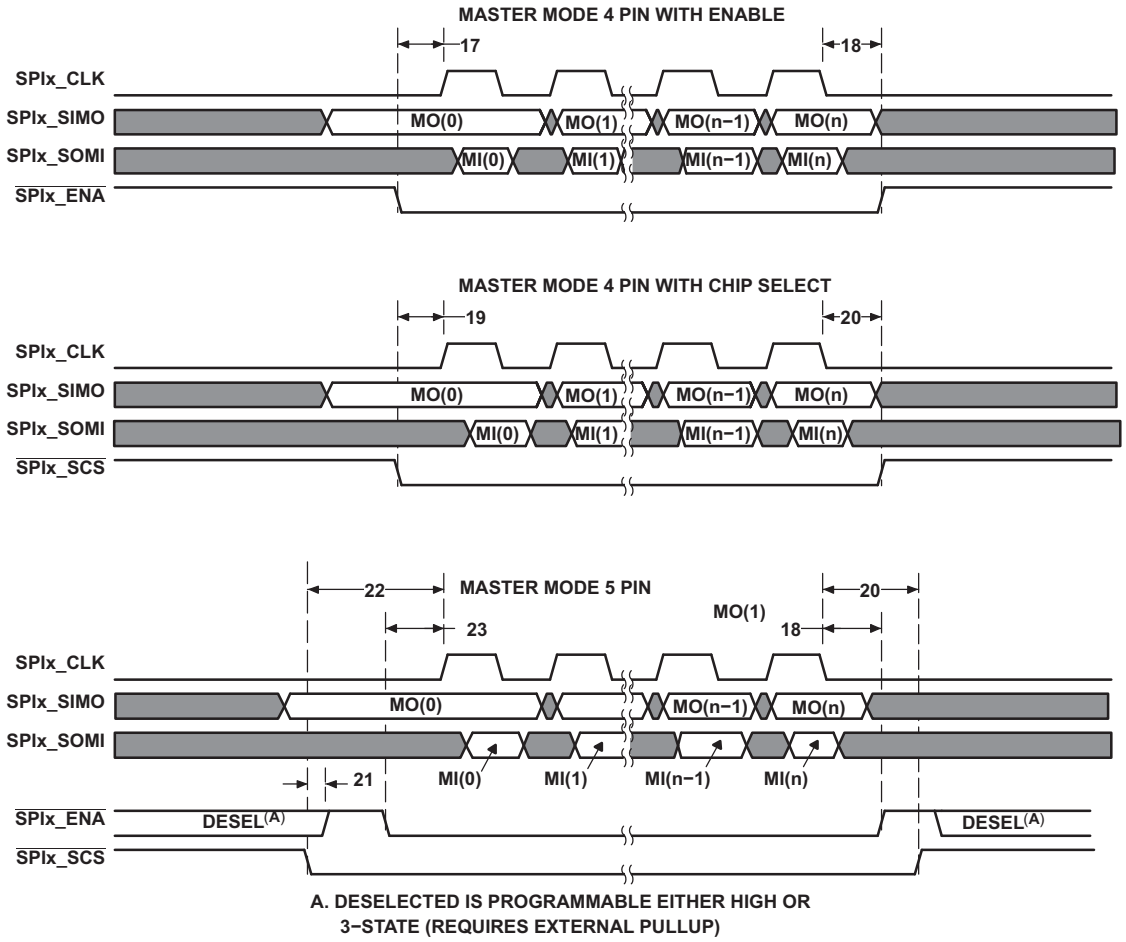

Figure 5-41. SPI Timings—Master Mode (4-Pin and 5-Pin)

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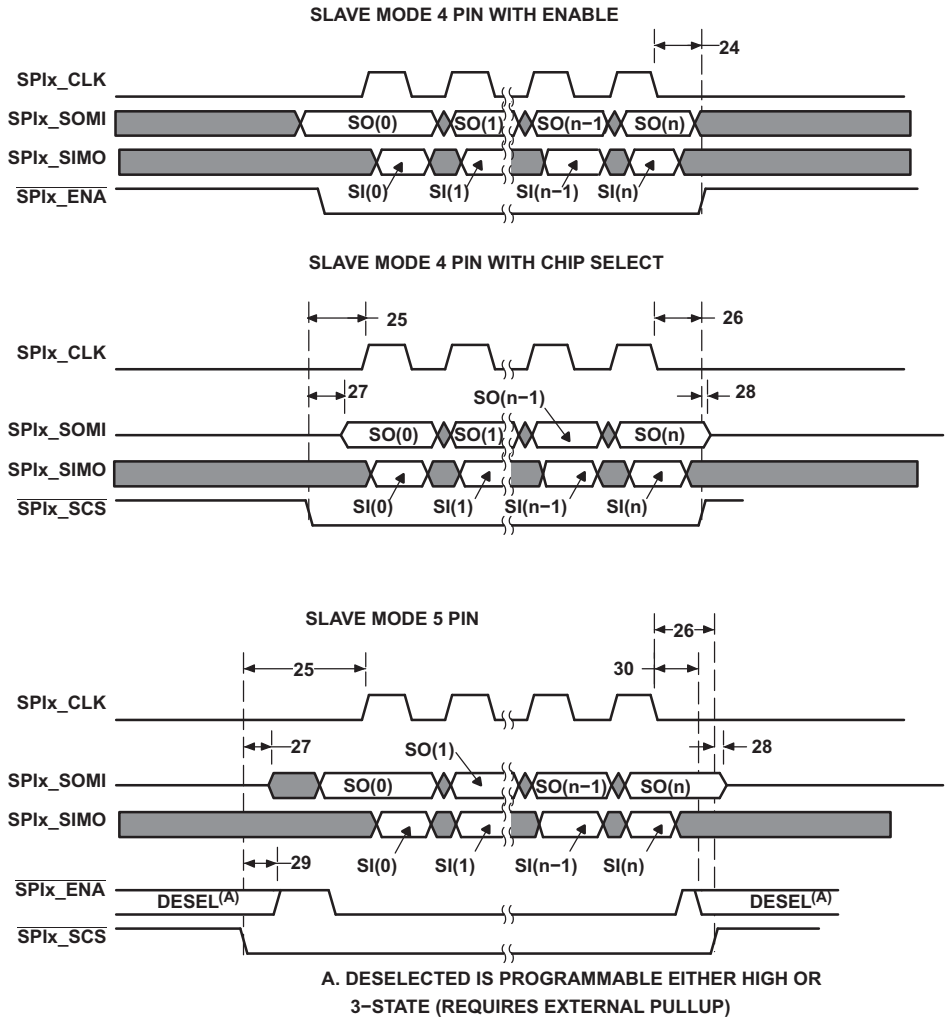

Figure 5-42. SPI Timings—Slave Mode (4-Pin and 5-Pin)

5.17 Enhanced Capture Module (eCAP)

The device contains up to three enhanced capture (eCAP) modules. Figure 5-43 shows a functional block diagram of a module.

Uses for ECAP include:

- Speed measurements of rotating machinery (e.g. toothed sprockets sensed via Hall sensors)
- Elapsed time measurements between position sensor triggers
- Period and duty cycle measurements of Pulse train signals
- Decoding current or voltage amplitude derived from cuty cycle encoded current/voltage sensors

The ECAP module described in this specification includes the following features:

- 32 bit time base
- 4 event time-stamp registers (each 32 bits)
- Edge polarity selection for up to 4 sequenced time-stamp capture events
- Interrupt on either of the 4 events
- Single shot capture of up to 4 event time-stamps
- Continuous mode capture of time-stamps in a 4 deep circular buffer
- Absolute time-stamp capture
- Difference mode time-stamp capture
- All the above resources are dedicated to a single input pin

The eCAP modules are clocked at the SYSCLK2 rate.

The clock enable bits (ECAP1/2/3/4ENCLK) in the PCLKCR1 register are used to turn off the eCAP modules individually (for low power operation). Upon reset, ECAP1ENCLK, ECAP2ENCLK, ECAP3ENCLK, and ECAP4EN CLK are set to low, indicating that the peripheral clock is off.

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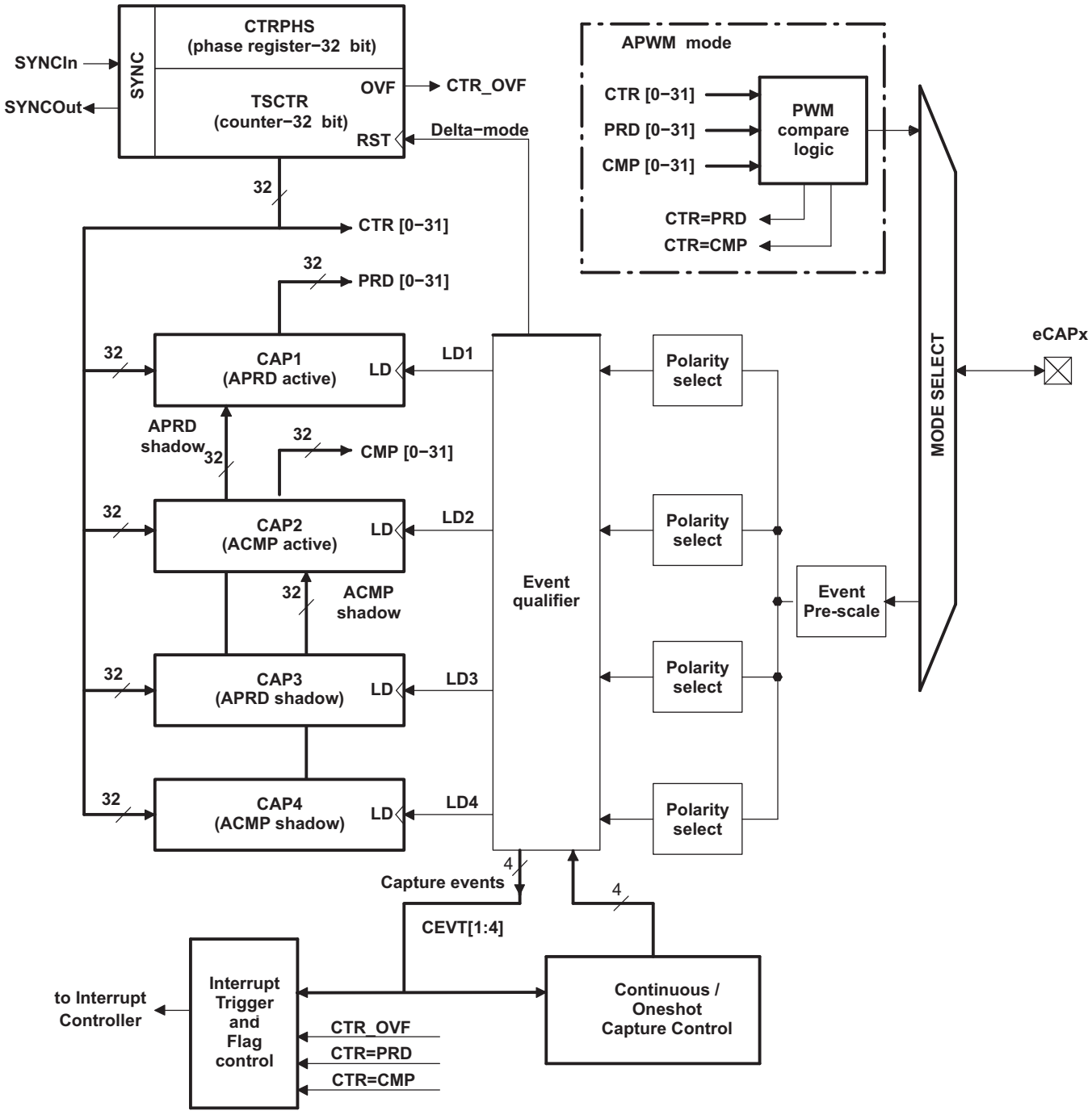

Figure 5-43. eCAP Functional Block Diagram

Table 5-68 is the list of the ECAP registers. See the *TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.* – Literature Number SPRUFK9 for more details.

Table 5-68. ECAPx Configuration Registers

ECAP0 BYTE ADDRESS	ECAP1 BYTE ADDRESS	ECAP2 BYTE ADDRESS	REGISTER NAME	DESCRIPTION
0x01F0 6000	0x01F0 7000	0x01F0 8000	TSCTR	Time-Stamp Counter
0x01F0 6004	0x01F0 7004	0x01F0 8004	CTRPHS	Counter Phase Offset Value Register
0x01F0 6008	0x01F0 7008	0x01F0 8008	CAP1	Capture 1 Register
0x01F0 600C	0x01F0 700C	0x01F0 800C	CAP2	Capture 2 Register
0x01F0 6010	0x01F0 7010	0x01F0 8010	CAP3	Capture 3 Register
0x01F0 6014	0x01F0 7014	0x01F0 8014	CAP4	Capture 4 Register
0x01F0 6028	0x01F0 7028	0x01F0 8028	ECCTL1	Capture Control Register 1
0x01F0 602A	0x01F0 702A	0x01F0 802A	ECCTL2	Capture Control Register 2
0x01F0 602C	0x01F0 702C	0x01F0 802C	ECEINT	Capture Interrupt Enable Register
0x01F0 602E	0x01F0 702E	0x01F0 802E	ECFLG	Capture Interrupt Flag Register
0x01F0 6030	0x01F0 7030	0x01F0 8030	ECCLR	Capture Interrupt Clear Register
0x01F0 6032	0x01F0 7032	0x01F0 8032	ECFRC	Capture Interrupt Force Register
0x01F0 605C	0x01F0 705C	0x01F0 805C	REVID	Revision ID

Table 5-69 shows the eCAP timing requirement and Table 5-70 shows the eCAP switching characteristics.

Table 5-69. Enhanced Capture (eCAP) Timing Requirement(1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(CAP)}$	Capture input pulse width	Asynchronous	$2t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		cycles

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.

Table 5-70. eCAP Switching Characteristics(1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(APWM)}$	Pulse duration, APWMx output high/low		20		ns

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.

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5.18 Enhanced Quadrature Encoder Module (eQEP)

The device contains up to two enhanced quadrature encoder (eQEP) modules.

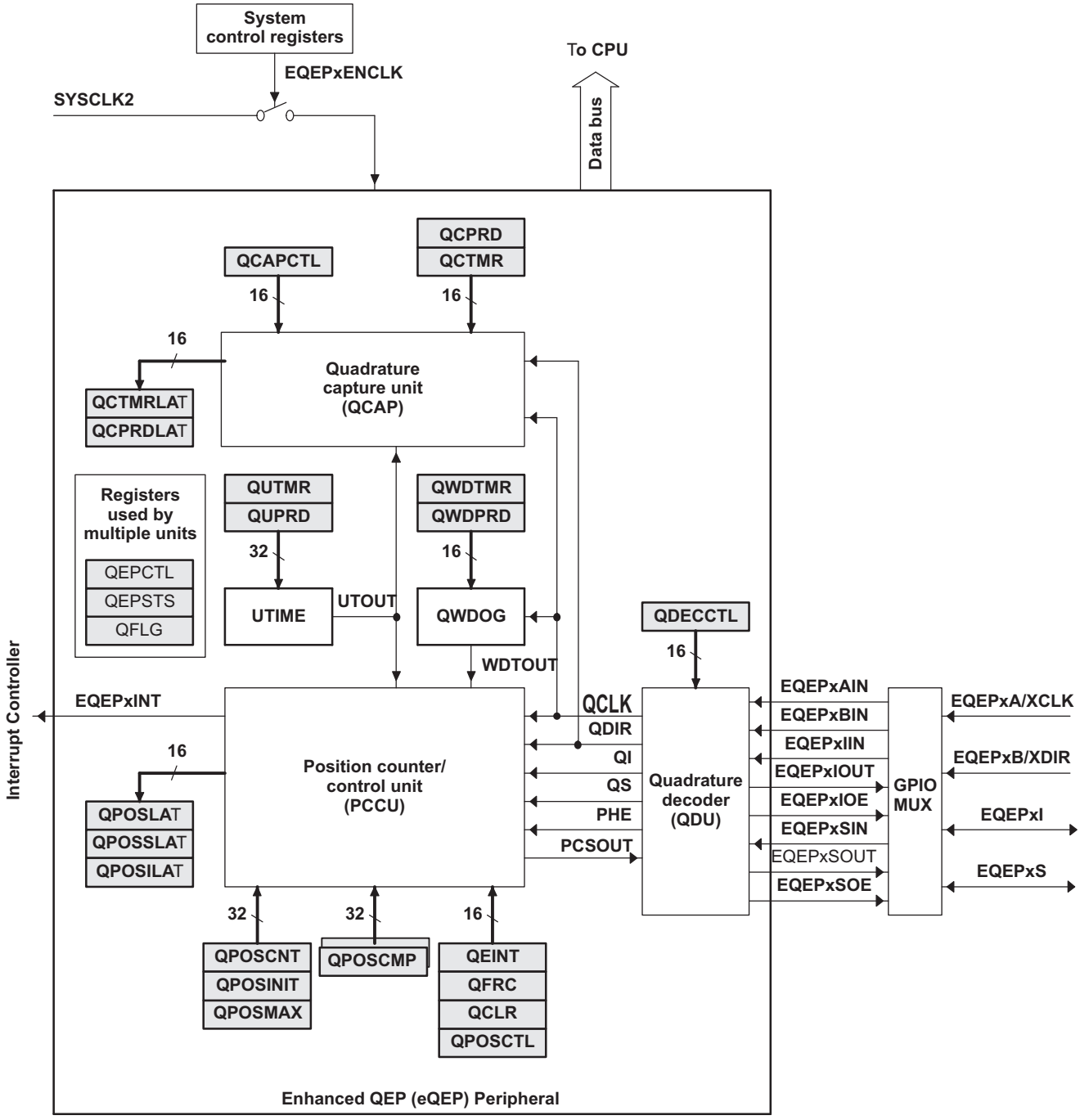

Figure 5-44. eQEP Functional Block Diagram

Table 5-71 is the list of the EQEP registers. See the *TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.* – Literature Number SPRUFK9 for more details.

Table 5-72 shows the eQEP timing requirement and Table 5-73 shows the eQEP switching characteristics.

Table 5-71. EQEP Registers

EQEP0 BYTE ADDRESS	EQEP1 BYTE ADDRESS	REGISTER NAME	DESCRIPTION
0x01F0 9000	0x01F0 A000	QPOSCNT	eQEP Position Counter
0x01F0 9004	0x01F0 A004	QPOSINIT	eQEP Initialization Position Count
0x01F0 9008	0x01F0 A008	QPOSMAX	eQEP Maximum Position Count
0x01F0 900C	0x01F0 A00C	QPOSCMP	eQEP Position-compare
0x01F0 9010	0x01F0 A010	QPOSILAT	eQEP Index Position Latch
0x01F0 9014	0x01F0 A014	QPOSSLAT	eQEP Strobe Position Latch
0x01F0 9018	0x01F0 A018	QPOSLAT	eQEP Position Latch
0x01F0 901C	0x01F0 A01C	QUTMR	eQEP Unit Timer
0x01F0 9020	0x01F0 A020	QUPRD	eQEP Unit Period Register
0x01F0 9024	0x01F0 A024	QWDTMR	eQEP Watchdog Timer
0x01F0 9026	0x01F0 A026	QWDPRD	eQEP Watchdog Period Register
0x01F0 9028	0x01F0 A028	QDECCTL	eQEP Decoder Control Register
0x01F0 902A	0x01F0 A02A	QEPCTL	eQEP Control Register
0x01F0 902C	0x01F0 A02C	QCAPCTL	eQEP Capture Control Register
0x01F0 902E	0x01F0 A02E	QPOSCTL	eQEP Position-compare Control Register
0x01F0 9030	0x01F0 A030	QEINT	eQEP Interrupt Enable Register
0x01F0 9032	0x01F0 A032	QFLG	eQEP Interrupt Flag Register
0x01F0 9034	0x01F0 A034	QCLR	eQEP Interrupt Clear Register
0x01F0 9036	0x01F0 A036	QFRC	eQEP Interrupt Force Register
0x01F0 9038	0x01F0 A038	QEPSTS	eQEP Status Register
0x01F0 903A	0x01F0 A03A	QCTMR	eQEP Capture Timer
0x01F0 903C	0x01F0 A03C	QCPRD	eQEP Capture Period Register
0x01F0 903E	0x01F0 A03E	QCTMRLAT	eQEP Capture Timer Latch
0x01F0 9040	0x01F0 A040	QCPRDLAT	eQEP Capture Period Latch
0x01F0 905C	0x01F0 A05C	REVID	eQEP Revision ID

Table 5-72. Enhanced Quadrature Encoder Pulse (eQEP) Timing Requirements(1)

		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(QEPP)}$	QEP input period	Asynchronous/synchronous	$2t_{c(SCO)}$		cycles
$t_{w(INDEXH)}$	QEP Index Input High time	Asynchronous/synchronous	$2t_{c(SCO)}$		cycles
$t_{w(INDEXL)}$	QEP Index Input Low time	Asynchronous/synchronous	$2t_{c(SCO)}$		cycles
$t_{w(STROBH)}$	QEP Strobe High time	Asynchronous/synchronous	$2t_{c(SCO)}$		cycles
$t_{w(STROBL)}$	QEP Strobe Input Low time	Asynchronous/synchronous	$2t_{c(SCO)}$		cycles

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.

Table 5-73. eQEP Switching Characteristics(1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(CNTR)xin}$	Delay time, external clock to counter increment			$4t_{c(SCO)}$	cycles
$t_{d(PCS-OUT)QEP}$	Delay time, QEP input edge to position compare sync output			$6t_{c(SCO)}$	cycles

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.

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5.19 Enhanced High-Resolution Pulse-Width Modulator (eHRPWM)

The device contains up to three enhanced PWM Modules (eHRPWM). Figure 5-45 shows a block diagram of multiple eHRPWM modules. Figure 4-4 shows the signal interconnections with the eHRPWM. See the *TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.* – Literature Number SPRUFK9 for more details.

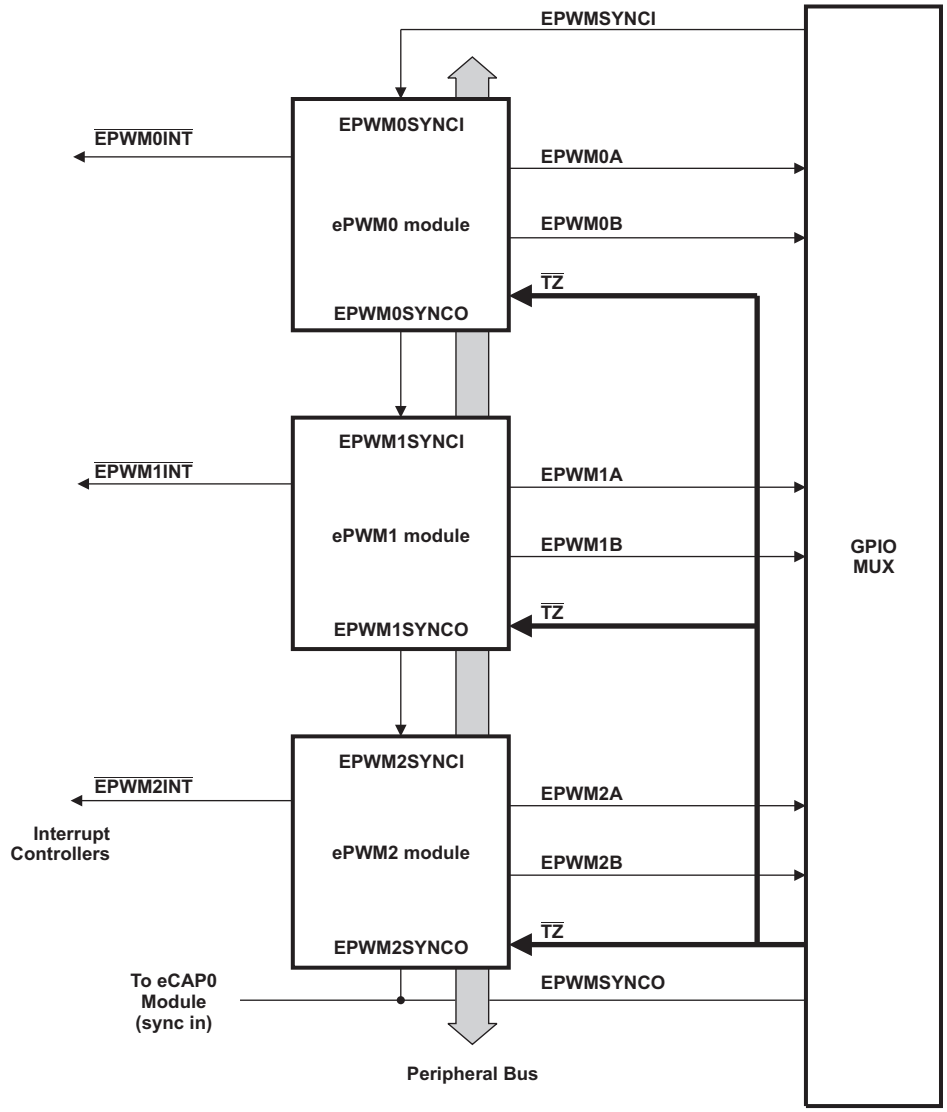

Figure 5-45. Multiple PWM Modules in the device

Table 5-74. eHRPWM Module Control and Status Registers Grouped by Submodule

eHRPWM0 BYTE ADDRESS	eHRPWM1 BYTE ADDRESS	eHRPWM2 BYTE ADDRESS	Acronym	Size (×16)	Shadow	Register Description
			Time-Base Submodule Registers			
0x01F0 0000	0x01F0 2000	0x01F0 4000	TBCTL	1	No	Time-Base Control Register
0x01F0 0002	0x01F0 2002	0x01F0 4002	TBSTS	1	No	Time-Base Status Register
0x01F0 0004	0x01F0 2004	0x01F0 4004	TBPHSHR	1	No	Extension for HRPWM Phase Register (1)
0x01F0 0006	0x01F0 2006	0x01F0 4006	TBPHS	1	No	Time-Base Phase Register
0x01F0 0008	0x01F0 2008	0x01F0 4008	TBCNT	1	No	Time-Base Counter Register
0x01F0 000A	0x01F0 200A	0x01F0 400A	TBPRD	1	Yes	Time-Base Period Register
			Counter-Compare Submodule Registers			
0x01F0 000E	0x01F0 200E	0x01F0 400E	CMPCTL	1	No	Counter-Compare Control Register
0x01F0 0010	0x01F0 2010	0x01F0 4010	CMPAHR	1	No	Extension for HRPWM Counter-Compare A Register (1)
0x01F0 0012	0x01F0 2012	0x01F0 4012	CMPA	1	Yes	Counter-Compare A Register
0x01F0 0014	0x01F0 2014	0x01F0 4014	CMPB	1	Yes	Counter-Compare B Register
			Action-Qualifier Submodule Registers			
0x01F0 0016	0x01F0 2016	0x01F0 4016	AQCTLA	1	No	Action-Qualifier Control Register for Output A (eHRPWMxA)
0x01F0 0018	0x01F0 2018	0x01F0 4018	AQCTLB	1	No	Action-Qualifier Control Register for Output B (eHRPWMxB)
0x01F0 001A	0x01F0 201A	0x01F0 401A	AQSFRC	1	No	Action-Qualifier Software Force Register
0x01F0 001C	0x01F0 201C	0x01F0 401C	AQCSFRC	1	Yes	Action-Qualifier Continuous S/W Force Register Set
			Dead-Band Generator Submodule Registers			
0x01F0 001E	0x01F0 201E	0x01F0 401E	DBCTL	1	No	Dead-Band Generator Control Register
0x01F0 0020	0x01F0 2020	0x01F0 4020	DBRED	1	No	Dead-Band Generator Rising Edge Delay Count Register
0x01F0 0022	0x01F0 2022	0x01F0 4022	DBFED	1	No	Dead-Band Generator Falling Edge Delay Count Register
			PWM-Chopper Submodule Registers			
0x01F0 003C	0x01F0 203C	0x01F0 403C	PCCTL	1	No	PWM-Chopper Control Register
			Trip-Zone Submodule Registers			
0x01F0 0024	0x01F0 2024	0x01F0 4024	TZSEL	1	No	Trip-Zone Select Register
0x01F0 0028	0x01F0 2028	0x01F0 4028	TZCTL	1	No	Trip-Zone Control Register
0x01F0 002A	0x01F0 202A	0x01F0 402A	TZEINT	1	No	Trip-Zone Enable Interrupt Register
0x01F0 002C	0x01F0 202C	0x01F0 402C	TZFLG	1	No	Trip-Zone Flag Register
0x01F0 002E	0x01F0 202E	0x01F0 402E	TZCLR	1	No	Trip-Zone Clear Register
0x01F0 0030	0x01F0 2030	0x01F0 4030	TZFRC	1	No	Trip-Zone Force Register
			Event-Trigger Submodule Registers			
0x01F0 0032	0x01F0 2032	0x01F0 4032	ETSEL	1	No	Event-Trigger Selection Register
0x01F0 0034	0x01F0 2034	0x01F0 4034	ETPS	1	No	Event-Trigger Pre-Scale Register
0x01F0 0036	0x01F0 2036	0x01F0 4036	ETFLG	1	No	Event-Trigger Flag Register
0x01F0 0038	0x01F0 2038	0x01F0 4038	ETCLR	1	No	Event-Trigger Clear Register
0x01F0 003A	0x01F0 203A	0x01F0 403A	ETFRC	1	No	Event-Trigger Force Register
			High-Resolution PWM (HRPWM) Submodule Registers			
0x01F0 1040	0x01F0 3040	0x01F0 5040	HRCNFG	1	No	HRPWM Configuration Register (1)

(1) These registers are only available on eHRPWM instances that include the high-resolution PWM (HRPWM) extension; otherwise, these locations are reserved.

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5.19.1 Enhanced Pulse Width Modulator (eHRPWM) Timing

PWM refers to PWM outputs on eHRPWM1-6. Table 5-75 shows the PWM timing requirements and Table 5-76, switching characteristics.

Table 5-75. eHRPWM Timing Requirements(1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(SYNCIN)}$	Sync input pulse width	Asynchronous	$2t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		cycles

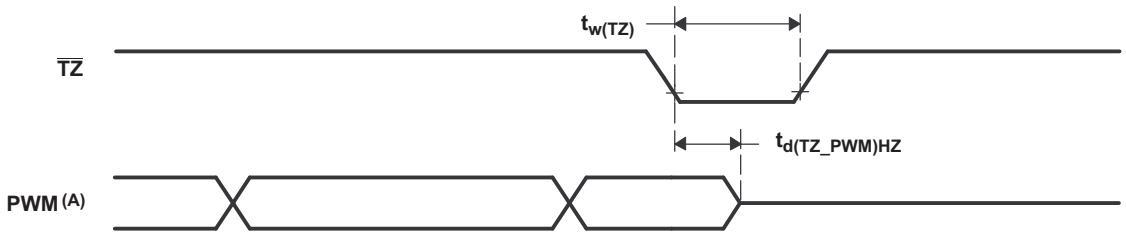
(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.

Table 5-76. eHRPWM Switching Characteristics(1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(PWM)}$	Pulse duration, PWMx output high/low		20		ns
$t_{w(SYNCOUT)}$	Sync output pulse width		$8t_{c(SCO)}$		cycles
$t_{d(PWM)TZA}$	Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low	no pin load		25	ns
$t_{d(TZ-PWM)HZ}$	Delay time, trip input active to PWM Hi-Z			20	ns

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.

5.19.2 Trip-Zone Input Timing



A. PWM refers to all the PWM pins in the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM recovery software.

Figure 5-46. PWM Hi-Z Characteristics

Table 5-77. Trip-Zone Input Timing Requirements(1)

			MIN	MAX	UNIT
$t_{w(TZ)}$	Pulse duration, $\overline{TZx}$ input low	Asynchronous	$1t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		cycles

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.

Table 5-78 shows the high-resolution PWM switching characteristics.

Table 5-78. High Resolution PWM Characteristics at SYSCLKOUT = (60 - 100 MHz)(1)

	MIN	TYP	MAX	UNIT
Micro Edge Positioning (MEP) step size(2)		200		ps

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(2) Maximum MEP step size is based on worst-case process, maximum temperature and maximum voltage. MEP step size will increase with low voltage and high temperature and decrease with voltage and cold temperature.
Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO function in end applications. SFO functions help to estimate the number of MEP steps per SYSCLKOUT period dynamically while the HRPWM is in operation.

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5.20 LCD Controller

Table 5-79 lists the LCD Controller registers. See the *TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.* – Literature Number SPRUFK9 for more details.

Table 5-79. LCD Controller (LCDC) Registers

Address Offset	Acronym	Register Description
0x01E1 3000	REVID	LCD Revision Identification Register
0x01E1 3004	LCD_CTRL	LCD Control Register
0x01E1 3008	LCD_STAT	LCD Status Register
0x01E1 300C	LIDD_CTRL	LCD LIDD Control Register
0x01E1 3010	LIDD_CS0_CONF	LCD LIDD CS0 Configuration Register
0x01E1 3014	LIDD_CS0_ADDR	LCD LIDD CS0 Address Read/Write Register
0x01E1 3018	LIDD_CS0_DATA	LCD LIDD CS0 Data Read/Write Register
0x01E1 301C	LIDD_CS1_CONF	LCD LIDD CS1 Configuration Register
0x01E1 3020	LIDD_CS1_ADDR	LCD LIDD CS1 Address Read/Write Register
0x01E1 3024	LIDD_CS1_DATA	LCD LIDD CS1 Data Read/Write Register
0x01E1 3028	RASTER_CTRL	LCD Raster Control Register
0x01E1 302C	RASTER_TIMING_0	LCD Raster Timing 0 Register
0x01E1 3030	RASTER_TIMING_1	LCD Raster Timing 1 Register
0x01E1 3034	RASTER_TIMING_2	LCD Raster Timing 2 Register
0x01E1 3038	RASTER_SUBPANEL	LCD Raster Subpanel Display Register
0x01E1 3040	LCDDMA_CTRL	LCD DMA Control Register
0x01E1 3044	LCDDMA_FB0_BASE	LCD DMA Frame Buffer 0 Base Address Register
0x01E1 3048	LCDDMA_FB0_CEILING	LCD DMA Frame Buffer 0 Ceiling Address Register
0x01E1 304C	LCDDMA_FB1_BASE	LCD DMA Frame Buffer 1 Base Address Register
0x01E1 3050	LCDDMA_FB1_CEILING	LCD DMA Frame Buffer 1 Ceiling Address Register

5.20.1 LCD Interface Display Driver (LIDD Mode)

Table 5-80. LCD LIDD Mode Timing Requirements(1)

NO	PARAMETER		MIN	MAX	UNIT
16	$t_{su(LCD_D)}$	Setup time, LCD_D[15:0] valid before LCD_CLK (SYSCLK2) ↑	7		ns
17	$t_{h(LCD_D)}$	Hold time, LCD_D[15:0] valid after LCD_CLK (SYSCLK2) ↑	0.5		ns

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.

Table 5-81. LCD LIDD Mode Timing Characteristics(1)

NO	PARAMETER		MIN	MAX	UNIT
4	$t_{d(LCD_D_V)}$	Delay time, LCD_CLK (SYSCLK2) ↑ to LCD_D[15:0] valid (write)	-0.5	10	ns
5	$t_{d(LCD_D_I)}$	Delay time, LCD_CLK (SYSCLK2) ↑ to LCD_D[15:0] invalid (write)	-0.5	10	ns
6	$t_{d(LCD_E_A)}$	Delay time, LCD_CLK (SYSCLK2) ↑ to $\overline{\text{LCD_AC_ENB_CS}}$↓	-0.5	7	ns
7	$t_{d(LCD_E_I)}$	Delay time, LCD_CLK (SYSCLK2) ↑ to $\overline{\text{LCD_AC_ENB_CS}}$↑	-0.5	7	ns
8	$t_{d(LCD_A_A)}$	Delay time, LCD_CLK (SYSCLK2) ↑ to LCD_VSYNC↓	-0.5	8	ns
9	$t_{d(LCD_A_I)}$	Delay time, LCD_CLK (SYSCLK2) ↑ to LCD_VSYNC↑	-0.5	8	ns

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.

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Table 5-81. LCD LIDD Mode Timing Characteristics[(1)] (continued)

NO	PARAMETER		MIN	MAX	UNIT
10	$t_{d(LCD_W_A)}$	Delay time, LCD_CLK (SYSCLK2) ↑ to LCD_HSYNC↓	-0.5	8	ns
11	$t_{d(LCD_W_I)}$	Delay time, LCD_CLK (SYSCLK2) ↑ to LCD_HSYNC↑	-0.5	8	ns
12	$t_{d(LCD_STRB_A)}$	Delay time, LCD_CLK (SYSCLK2) ↑ to LCD_PCLK↑	-0.5	12	ns
13	$t_{d(LCD_STRB_I)}$	Delay time, LCD_CLK (SYSCLK2) ↑ to LCD_PCLK↓	-0.5	12	ns
14	$t_{d(LCD_D_Z)}$	Delay time, LCD_CLK (SYSCLK2) ↑ to LCD_D[15:0] in 3-state	-0.5	12	ns
15	$t_{d(Z_LCD_D)}$	Delay time, LCD_CLK (SYSCLK2) ↑ to 15 td(Z_LCD_D) 3-state) LCD_D[15:0] (valid from 3-state)	-0.5	12	ns

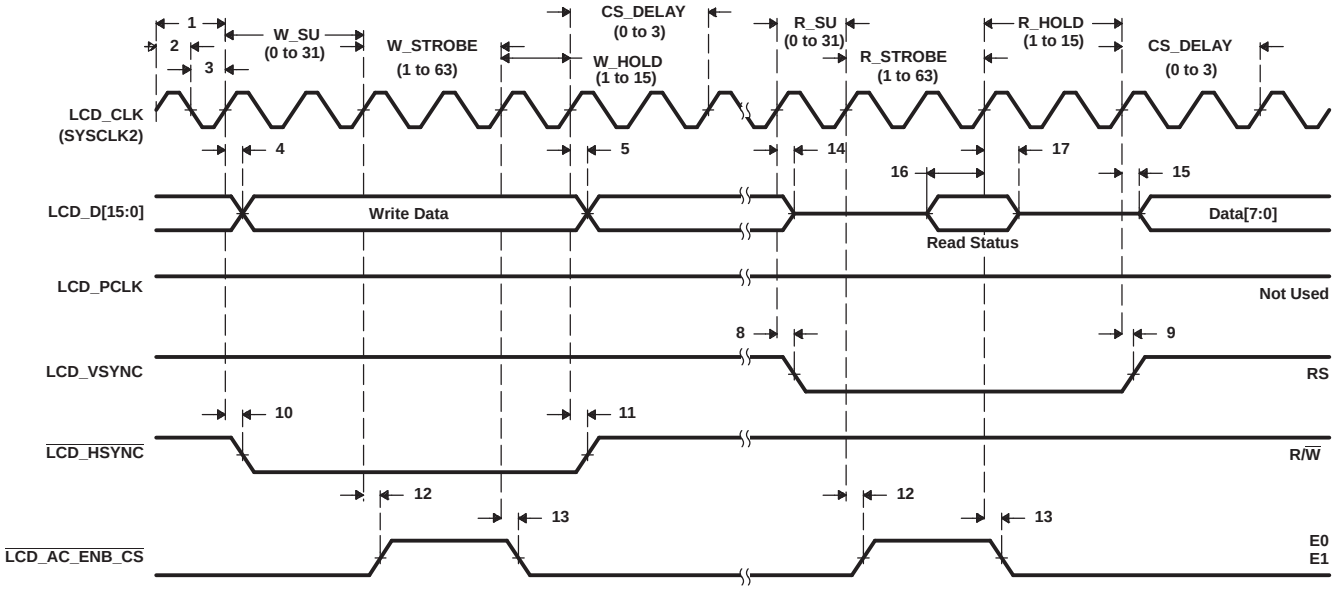

Figure 5-47. Character Display HD44780 Write

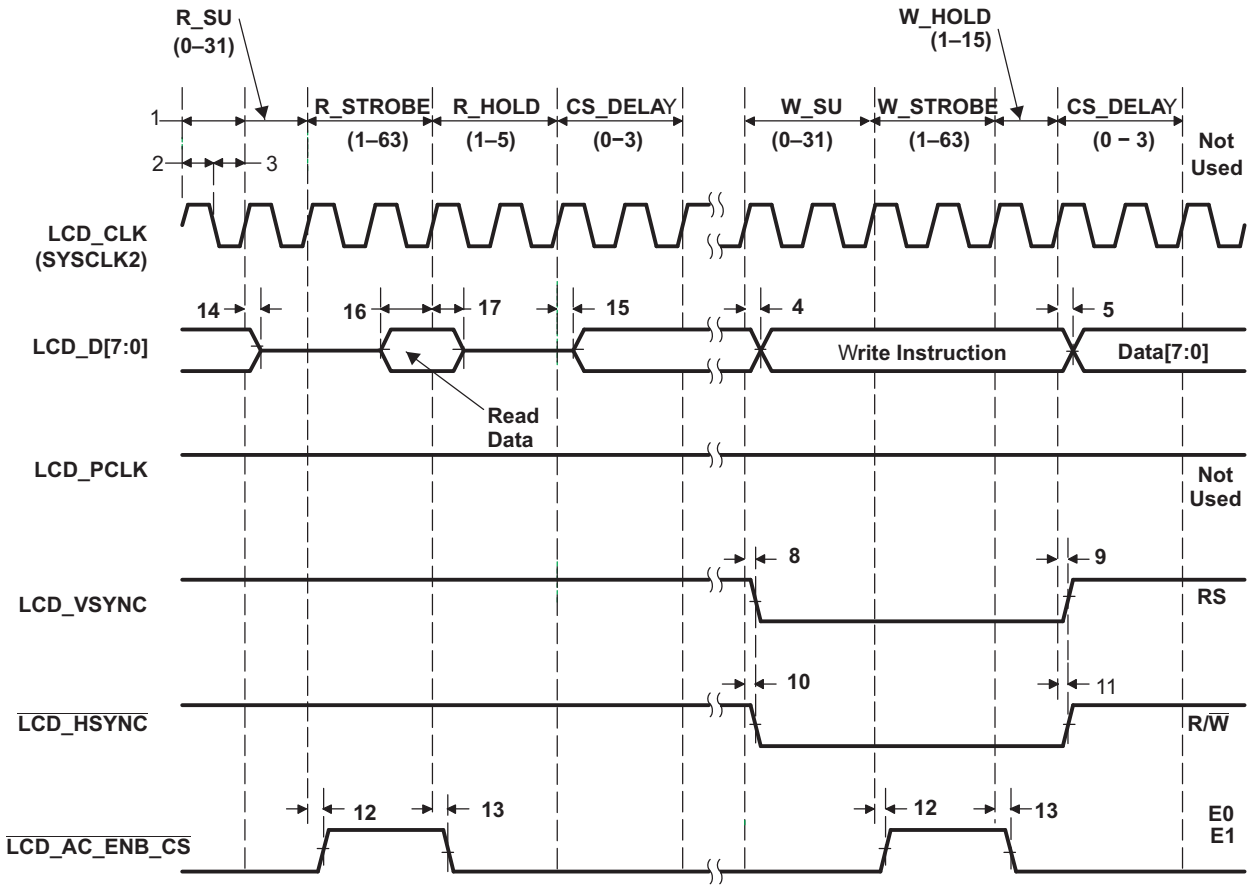

Figure 5-48. Character Display HD44780 Read

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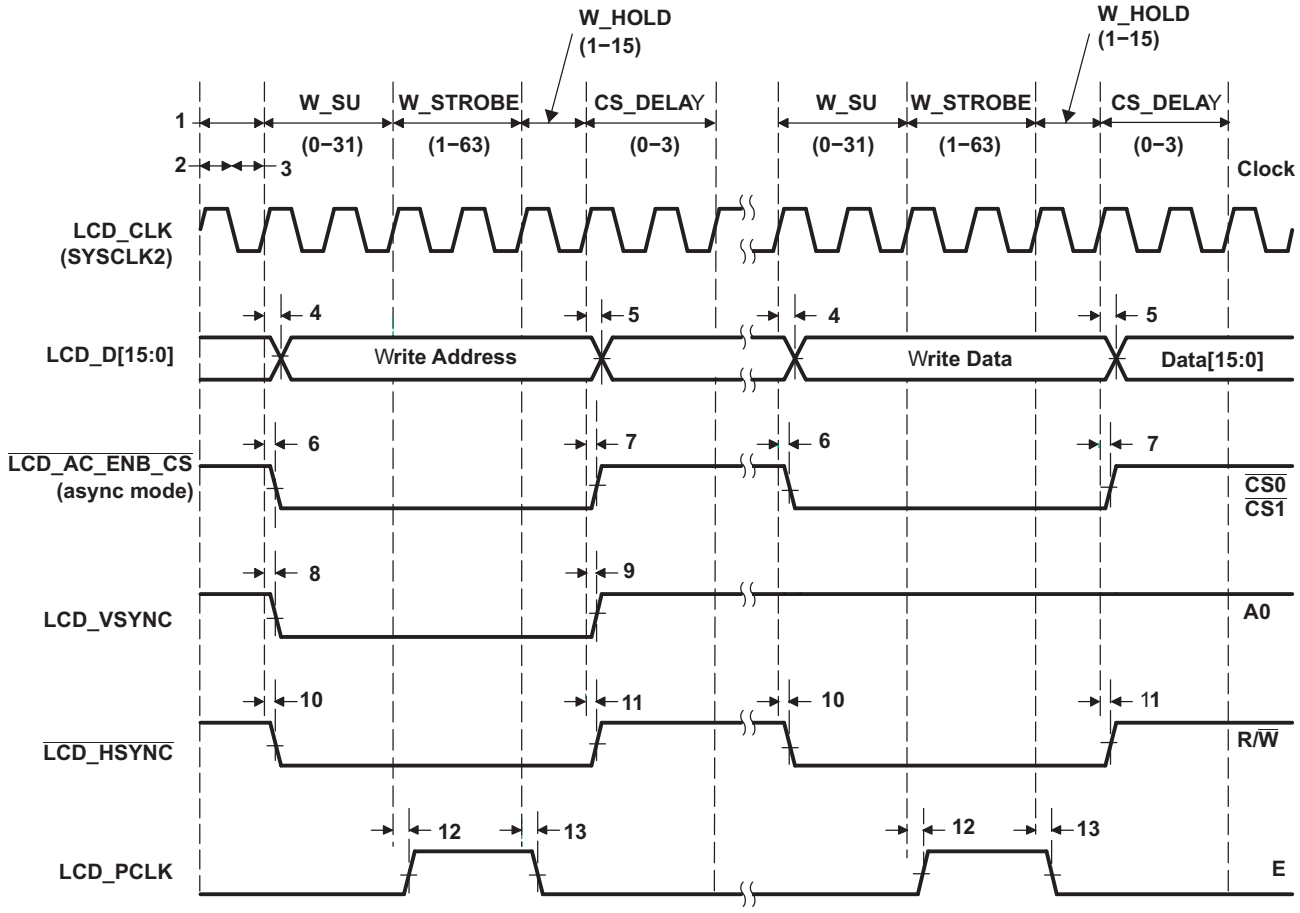

Figure 5-49. Micro-Interface Graphic Display 6800 Write

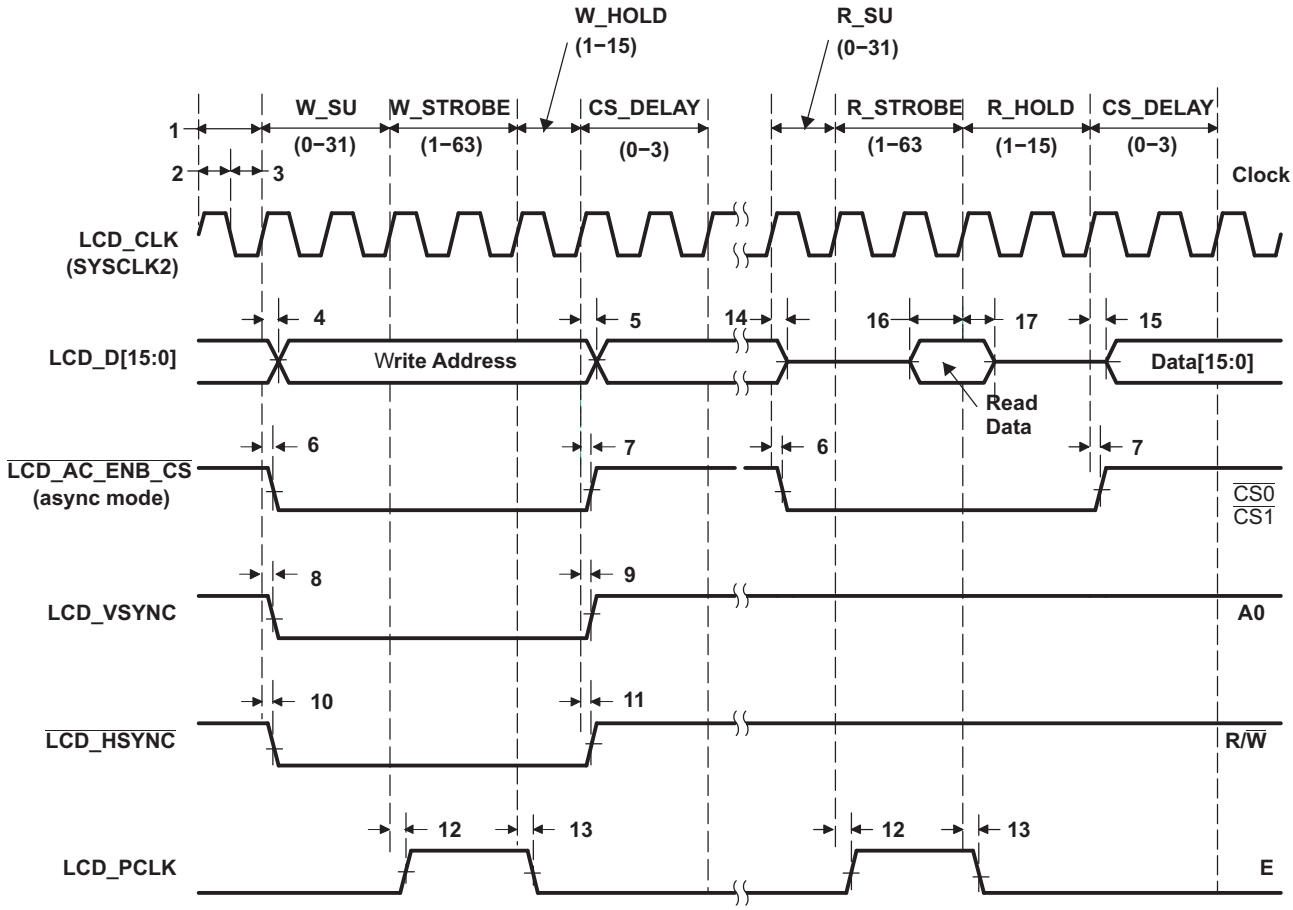

Figure 5-50. Micro-Interface Graphic Display 6800 Read

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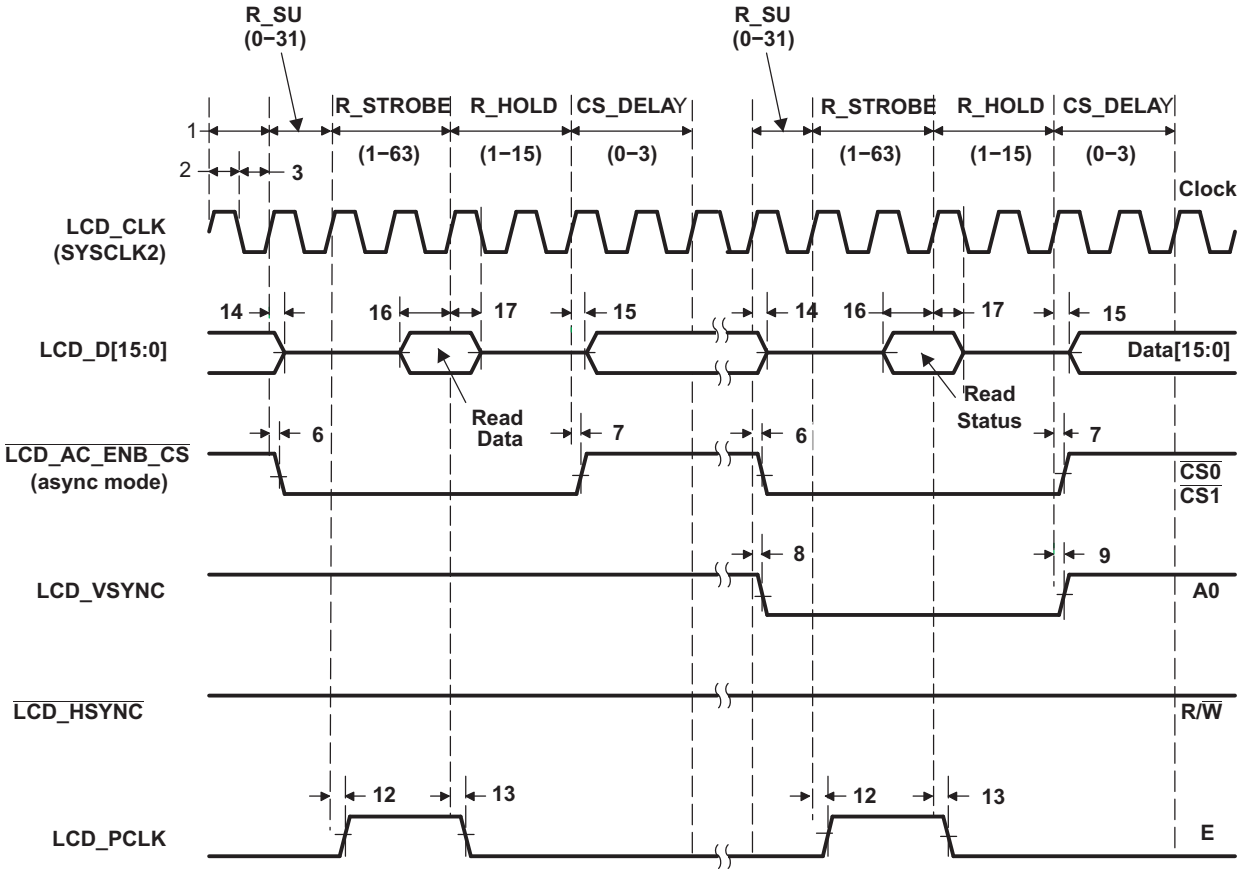

Figure 5-51. Micro-Interface Graphic Display 6800 Status

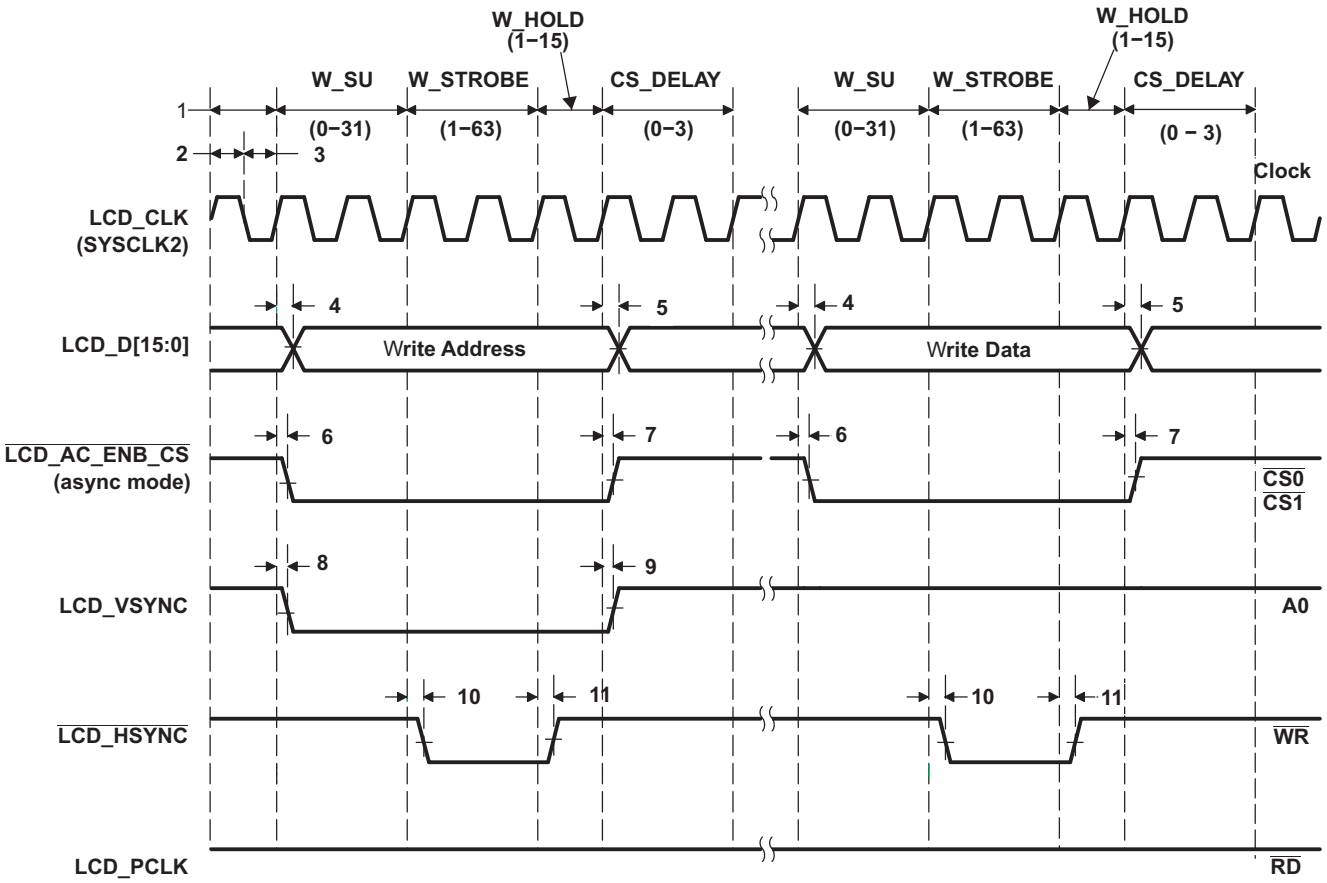

Figure 5-52. Micro-Interface Graphic Display 8080 Write

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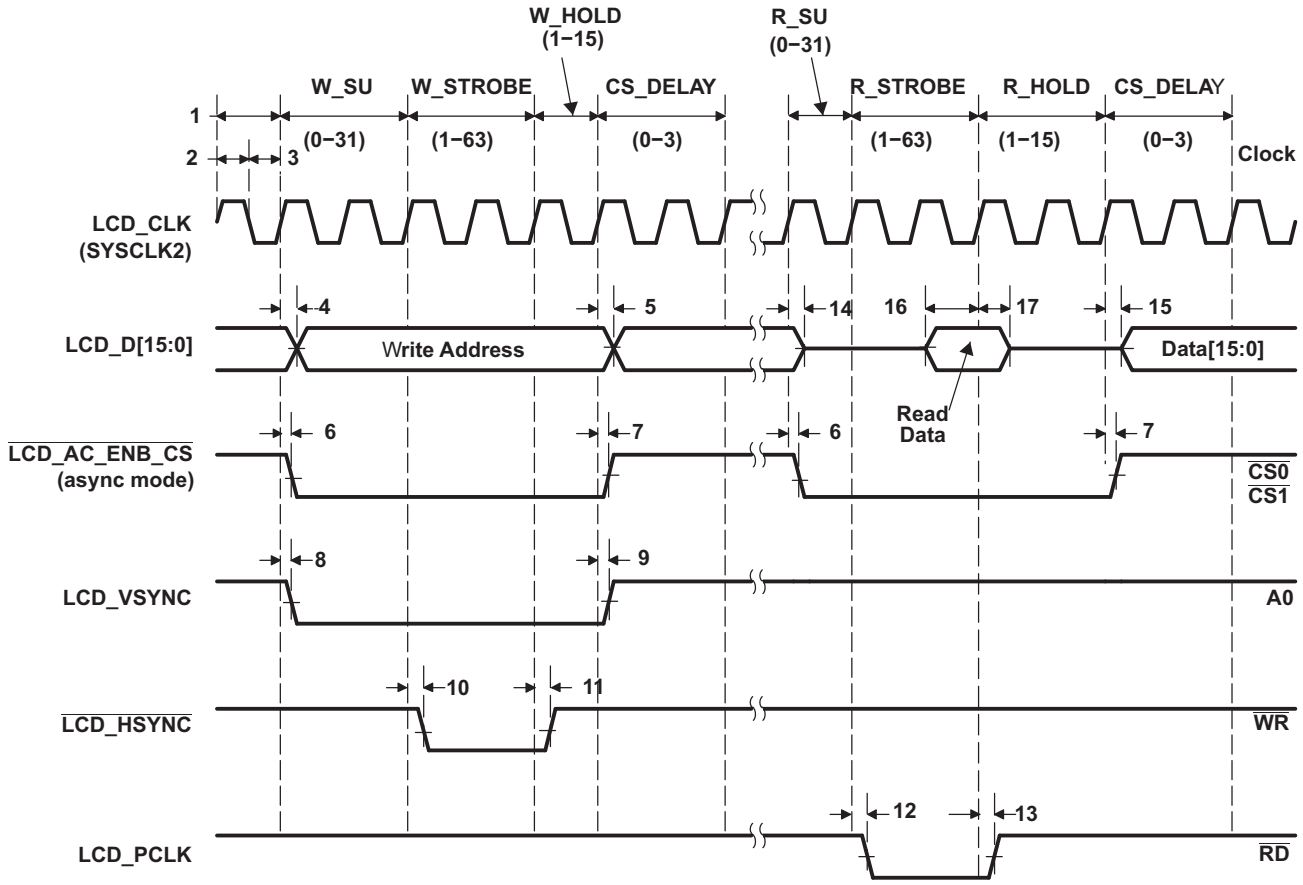

Figure 5-53. Micro-Interface Graphic Display 8080 Read

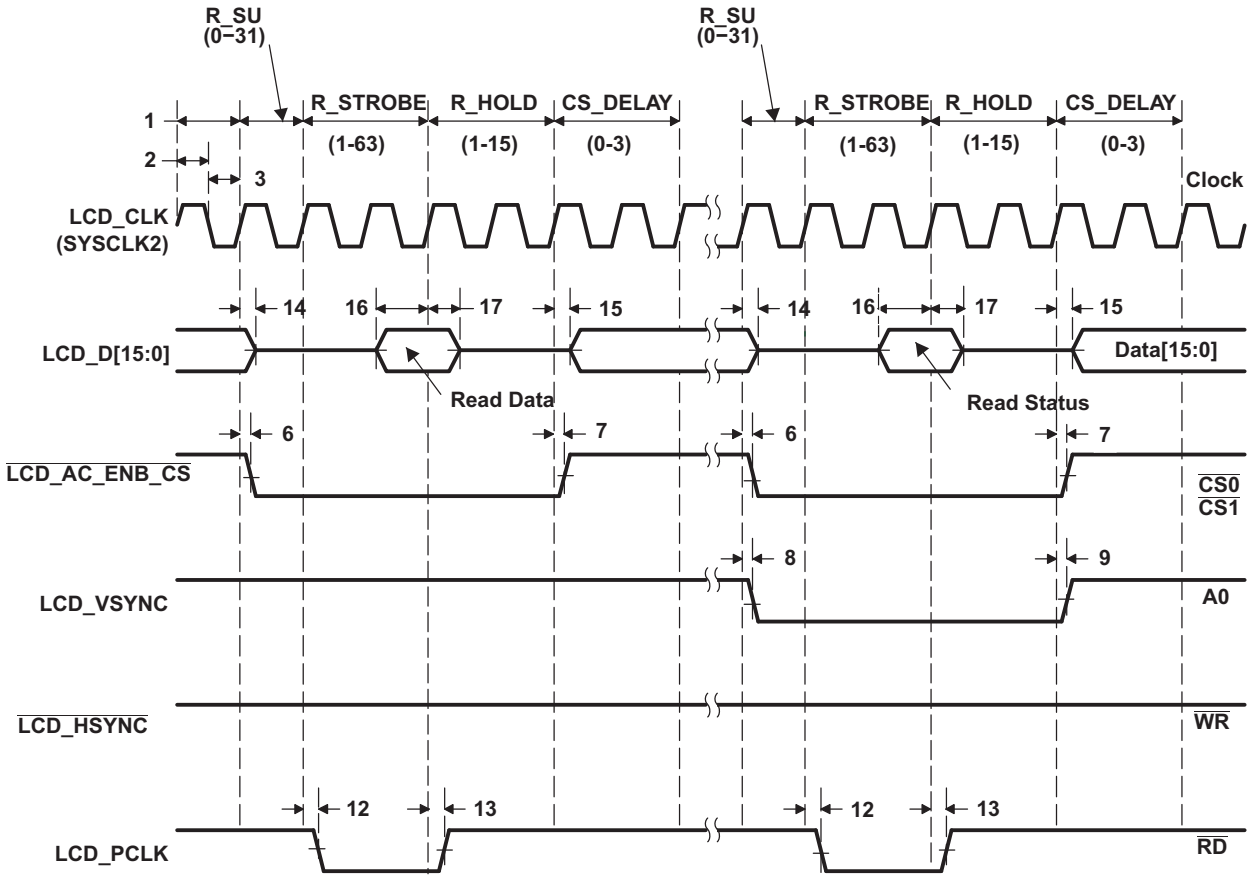

Figure 5-54. Micro-Interface Graphic Display 8080 Status

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5.20.2 LCD Raster Mode

Table 5-82. LCD Raster Mode Timing

See Figure 5-56 through Figure 5-54

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{clock(PIXEL_CLK)}$	Clock frequency, pixel clock		F/2 (1)	MHz
1 (2)	$t_{c(PIXEL_CLK)}$	Cycle time, pixel clock	26.6		ns
2 (2)	$t_{w(PIXEL_CLK_H)}$	Pulse duration, pixel clock high	10		ns
3 (2)	$t_{w(PIXEL_CLK_L)}$	Pulse duration, pixel clock low	10		ns
4	$t_{d(LCD_D_V)}$	Delay time, LCD_PCLK↑ to LCD_D[15:0] valid (write)	0	12.5	ns
5	$t_{d(LCD_D_IV)}$	Delay time, LCD_PCLK↑ to LCD_D[15:0] invalid (write)	0	12.5	ns
6	$t_{d(\overline{LCD_AC_ENB_CS_A})}$	Delay time, LCD_PCLK↓ to $\overline{LCD_AC_ENB_CS}$↑	S2+0 (3)	S2+12.5 (3)	ns
7	$t_{d(\overline{LCD_AC_ENB_CS_I})}$	Delay time, LCD_PCLK↓ to $\overline{LCD_AC_ENB_CS}$↓	S2+0 (3)	S2+12.5 (3)	ns
8	$t_{d(LCD_VSYNC_A)}$	Delay time, LCD_PCLK↓ to LCD_VSYNC↑	0	12.5	ns
9	$t_{d(LCD_VSYNC_I)}$	Delay time, LCD_PCLK↓ to LCD_VSYNC↓	0	12.5	ns
10	$t_{d(LCD_HSYNC_A)}$	Delay time, LCD_PCLK↑ to LCD_HSYNC↑	0	12.5	ns
11	$t_{d(LCD_HSYNC_I)}$	Delay time, LCD_PCLK↑ to LCD_HSYNC↓	0	12.5	ns

(1) F = frequency of LCD_PCLK in ns
(2) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(3) S2=SYSCLK2 cycle time in ns.

Frame-to-frame timing is derived through the following parameters in the LCD (RASTER_TIMING_1) register:

- Vertical front porch (VFP)
- Vertical sync pulse width (VSW)
- Vertical back porch (VBP)
- Lines per panel (LPP)

Line-to-line timing is derived through the following parameters in the LCD (RASTER_TIMING_0) register:

- Horizontal front porch (HFP)
- Horizontal sync pulse width (HSW)
- Horizontal back porch (HBP)
- Pixels per panel (PPL)

$\overline{LCD_AC_ENB_CS}$ timing is derived through the following parameter in the LCD (RASTER_TIMING_2) register:

- AC bias frequency (ACB)

The display format produced in raster mode is shown in Figure 5-55. An entire frame is delivered one line at a time. The first line delivered starts at data pixel (1, 1) and ends at data pixel (P, 1). The last line delivered starts at data pixel (1, L) and ends at data pixel (P, L). The beginning of each new frame is denoted by the activation of I/O signal LCD_VSYNC. The beginning of each new line is denoted by the activation of I/O signal LCD_HSYNC.

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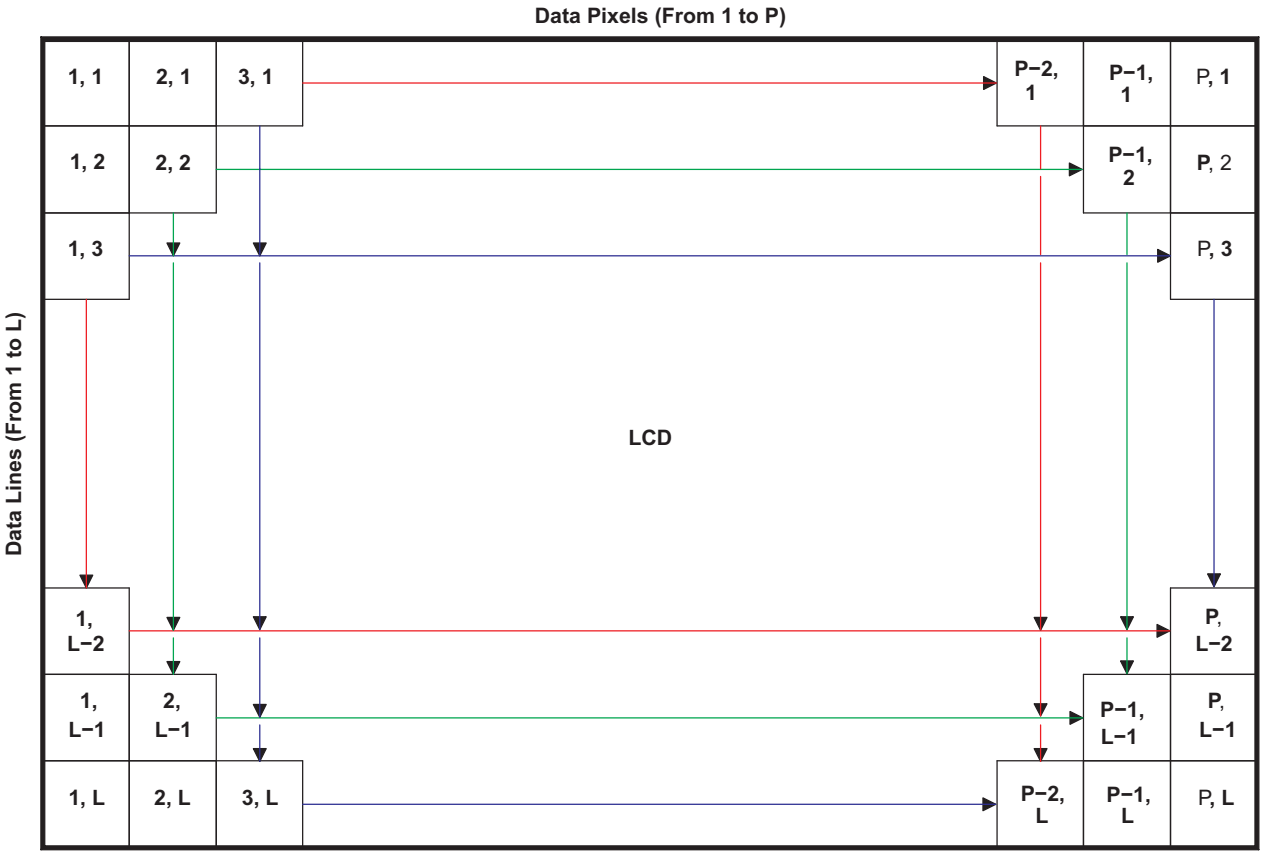

Figure 5-55. LCD Raster-Mode Display Format

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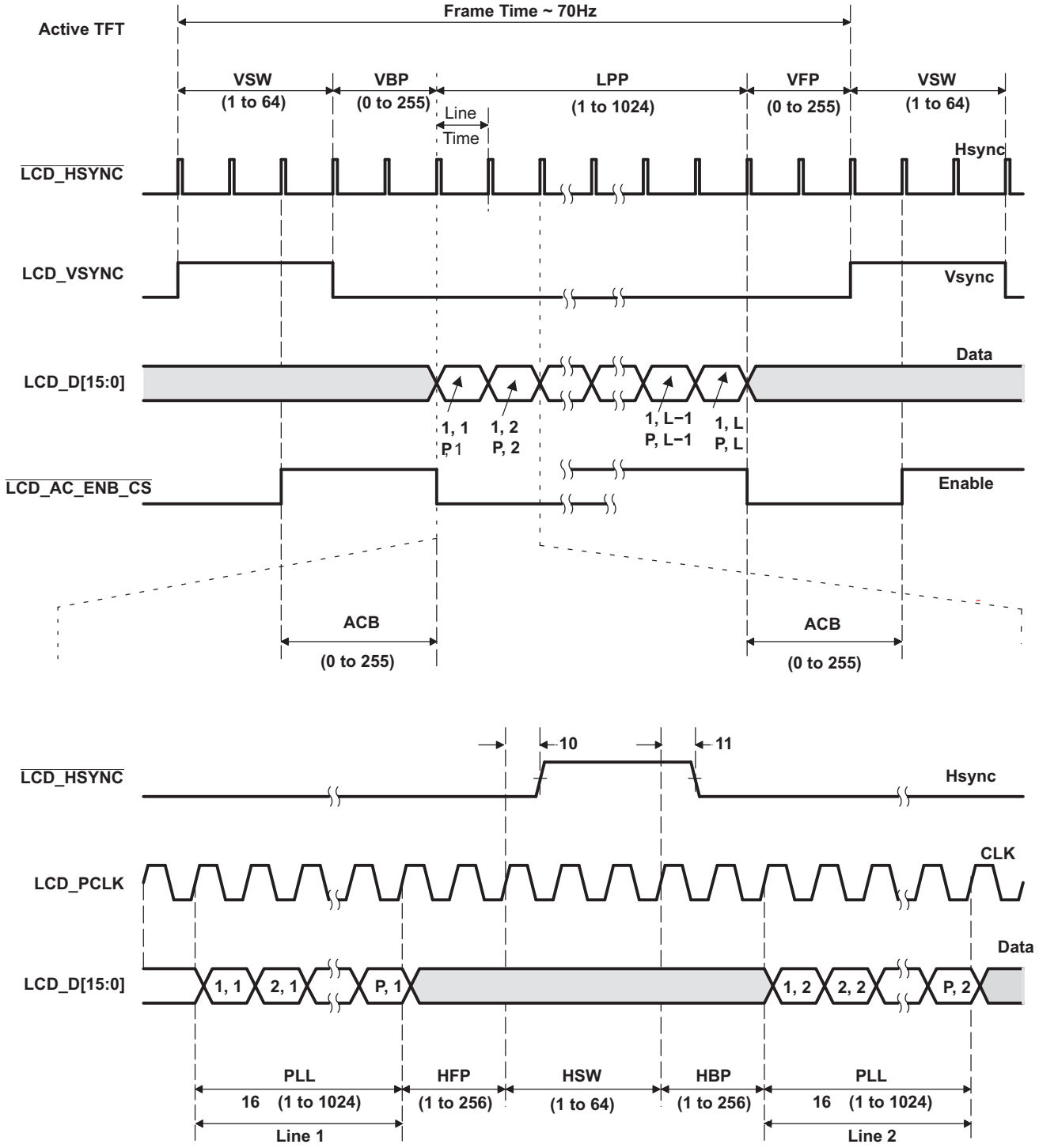

Figure 5-56. LCD Raster-Mode Active

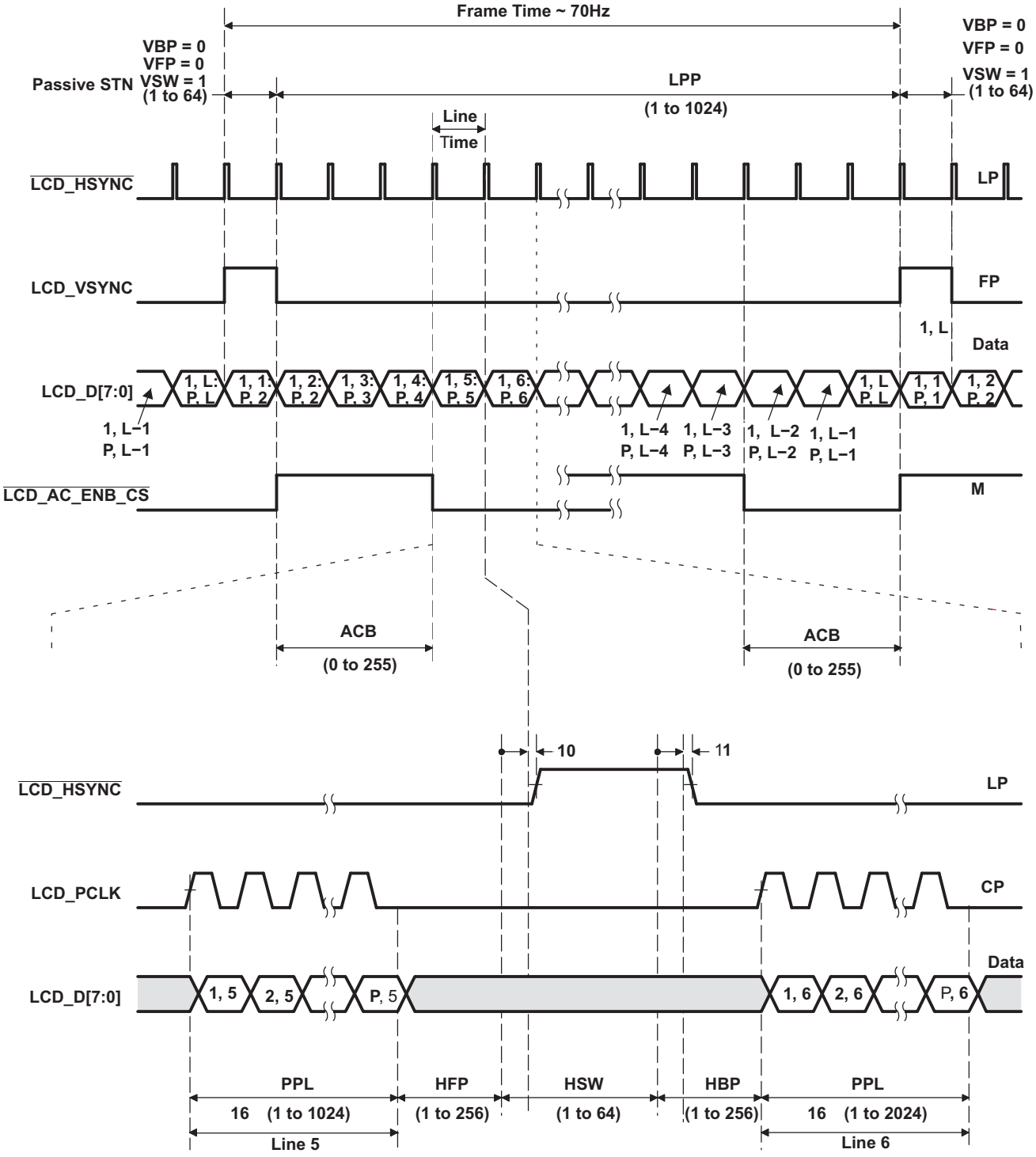

Figure 5-57. LCD Raster-Mode Passive

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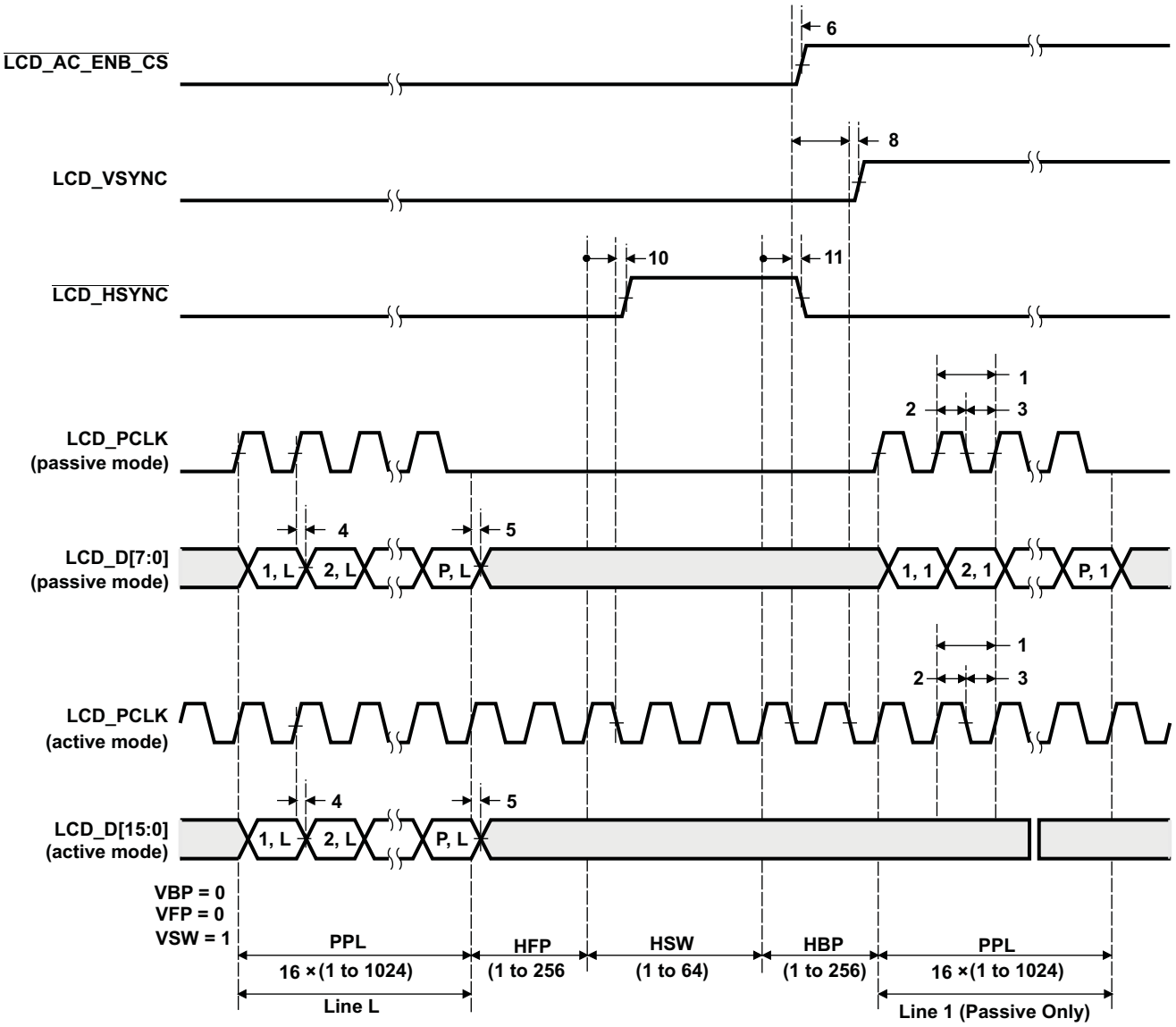

Figure 5-58. LCD Raster-Mode Control Signal Activation

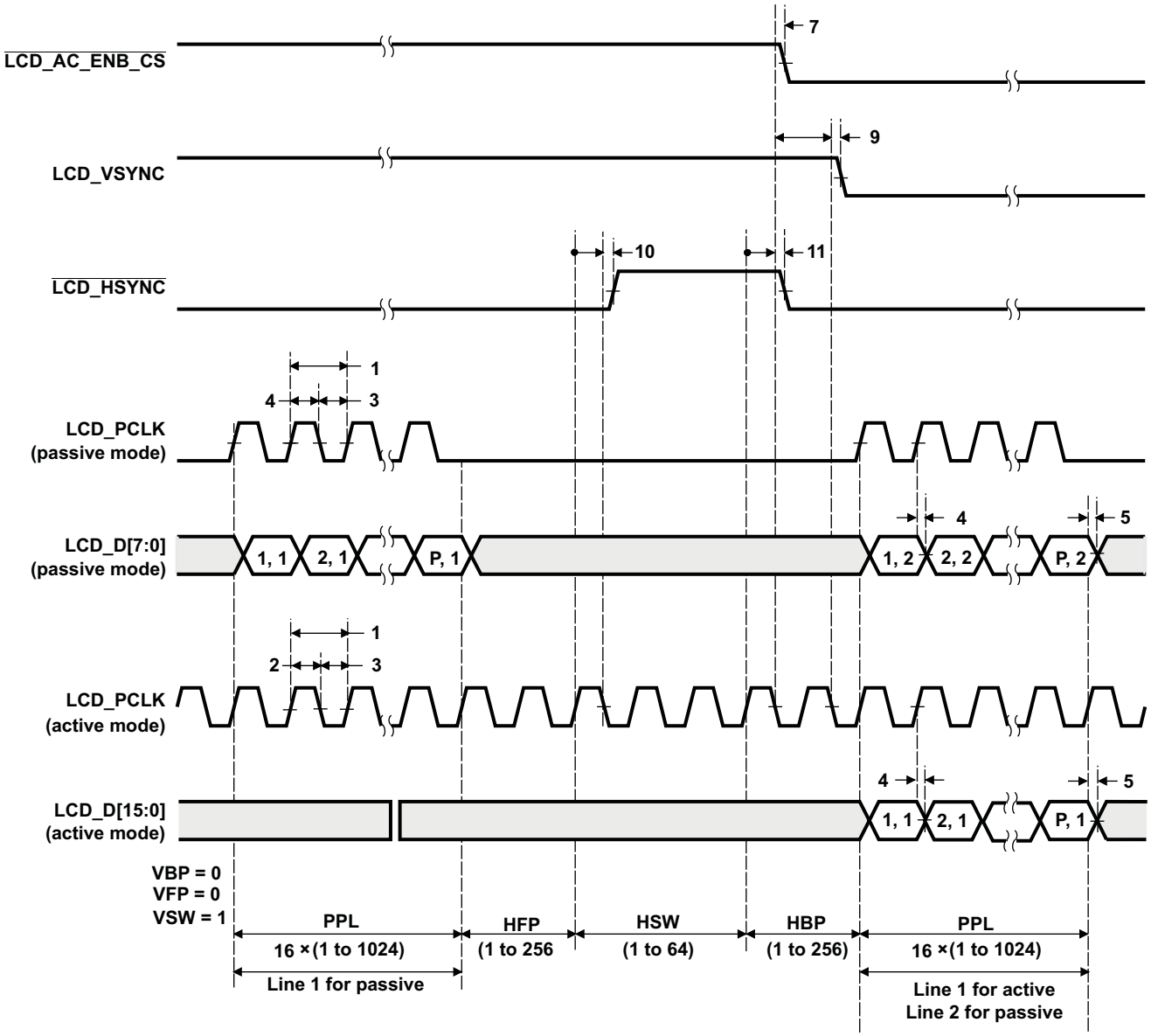

Figure 5-59. LCD Raster-Mode Control Signal Deactivation

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5.21 Timers

The timers support the following features:

- Configurable as single 64-bit timer or two 32-bit timers
- Period timeouts generate interrupts, DMA events or external pin events
- Eight 32-bit compare registers
- Compare matches generate interrupt events
- Capture capability
- 64-bit Watchdog capability (Timer64P1 only)

Table 5-83 lists the timer registers. See the *TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.* – Literature Number SPRUFK9 for more details.

Table 5-83. Timer Registers

Timer64P 0	Timer64P 1	Acronym	Register Description
0x01C2 0000	0x01C2 1000	REV	Revision Register
0x01C2 0004	0x01C2 1004	EMUMGT	Emulation Management Register
0x01C2 0008	0x01C2 1008	GPINTGPEN	GPIO Interrupt and GPIO Enable Register
0x01C2 000C	0x01C2 100C	GPDATGPDIR	GPIO Data and GPIO Direction Register
0x01C2 0010	0x01C2 1010	TIM12	Timer Counter Register 12
0x01C2 0014	0x01C2 1014	TIM34	Timer Counter Register 34
0x01C2 0018	0x01C2 1018	PRD12	Timer Period Register 12
0x01C2 001C	0x01C2 101C	PRD34	Timer Period Register 34
0x01C2 0020	0x01C2 1020	TCR	Timer Control Register
0x01C2 0024	0x01C2 1024	TGCR	Timer Global Control Register
0x01C2 0028	0x01C2 1028	WDTCR	Watchdog Timer Control Register
0x01C2 0034	0x01C2 1034	REL12	Timer Reload Register 12
0x01C2 0038	0x01C2 1038	REL34	Timer Reload Register 34
0x01C2 003C	0x01C2 103C	CAP12	Timer Capture Register 12
0x01C2 0040	0x01C2 1040	CAP34	Timer Capture Register 34
0x01C2 0044	0x01C2 1044	INTCTLSTAT	Timer Interrupt Control and Status Register
0x01C2 0060	0x01C2 1060	CMP0	Compare Register 0
0x01C2 0064	0x01C2 1064	CMP1	Compare Register 1
0x01C2 0068	0x01C2 1068	CMP2	Compare Register 2
0x01C2 006C	0x01C2 106C	CMP3	Compare Register 3
0x01C2 0070	0x01C2 1070	CMP4	Compare Register 4
0x01C2 0074	0x01C2 1074	CMP5	Compare Register 5
0x01C2 0078	0x01C2 1078	CMP6	Compare Register 6
0x01C2 007C	0x01C2 107C	CMP7	Compare Register 7

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5.21.1 Timer Electrical Data/Timing

Table 5-84. Timing Requirements for Timer Input(1)(2) (3) (see Figure 5-60)

NO.			MIN	MAX	UNIT
1	$t_{c(TIN)}$	Cycle time, TIM_IN	4P		ns
2	$t_{w(TINPH)}$	Pulse duration, TIM_IN high	0.45C	0.55C	ns
3	$t_{w(TINPL)}$	Pulse duration, TIM_IN low	0.45C	0.55C	ns
4	$t_{t(TIN)}$	Transition time, TIM_IN		0.05C	ns

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(2) P = OSCIN cycle time in ns. For example, when OSCIN frequency is 27 MHz, use P = 37.037 ns.
(3) C = TM64P0_IN12 cycle time in ns. For example, when TM64Px_IN12 frequency is 27 MHz, use C = 37.037 ns

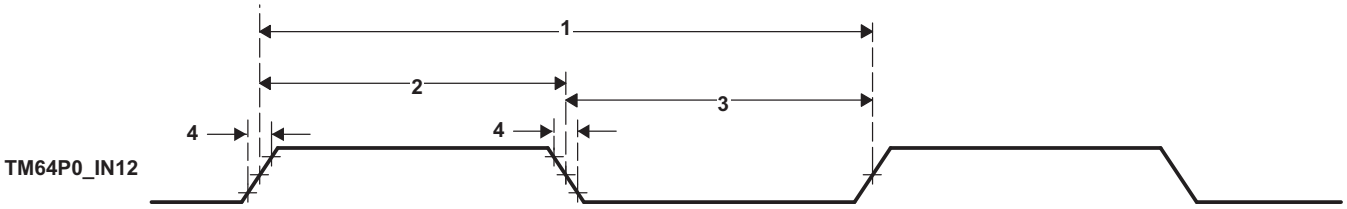

Figure 5-60. Timer Timing

Table 5-85. Switching Characteristics Over Recommended Operating Conditions for Timer Output(1) (2)

NO.			MIN	MAX	UNIT
5	$t_{w(TOUTH)}$	Pulse duration, TM64P0_OUT12 high	4P		ns
6	$t_{w(TOUTL)}$	Pulse duration, TM64P0_OUT12 low	4P		ns

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(2) P = OSCIN cycle time in ns. For example, when OSCIN frequency is 27 MHz, use P = 37.037 ns.

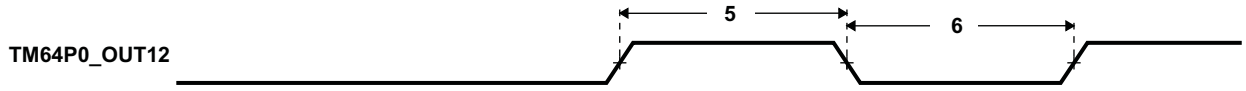

Figure 5-61. Timer Timing

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5.22 Inter-Integrated Circuit Serial Ports (I2C0, I2C1)

5.22.1 I2C Device-Specific Information

Having two I2C modules on the device simplifies system architecture, since one module may be used by the DSP to control local peripherals ICs (DACs, ADCs, etc.) while the other may be used to communicate with other controllers in a system or to implement a user interface. Figure Figure 5-62 is block diagram of the I2C Module.

Each I2C port supports:

- Compatible with Philips® I2C Specification Revision 2.1 (January 2000)
- Fast Mode up to 400 Kbps (no fail-safe I/O buffers)
- Noise Filter to Remove Noise 50 ns or less
- Seven- and Ten-Bit Device Addressing Modes
- Master (Transmit/Receive) and Slave (Transmit/Receive) Functionality
- Events: DMA, Interrupt, or Polling
- General-Purpose I/O Capability if not used as I2C

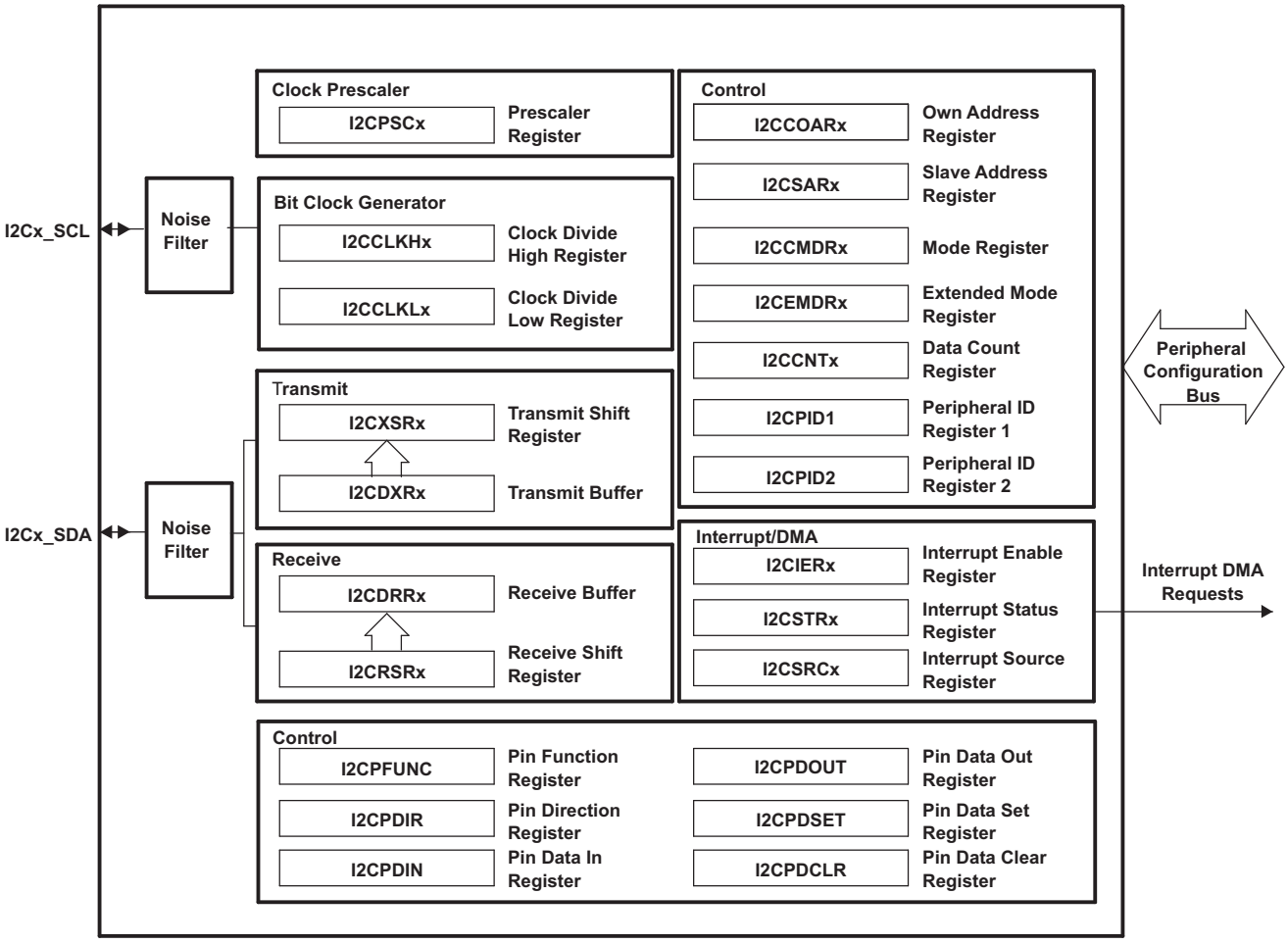

Figure 5-62. I2C Module Block Diagram

5.22.2 I2C Peripheral Registers Description(s)

Table 5-86 is the list of the I2C registers. See the *TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.* – Literature Number SPRUFK9 for more details.

Table 5-86. Inter-Integrated Circuit (I2C) Registers

I2C0 BYTE ADDRESS	I2C1 BYTE ADDRESS	Acronym	Register Description
0x01C2 2000	0x01E2 8000	ICOAR	I2C Own Address Register
0x01C2 2004	0x01E2 8004	ICIMR	I2C Interrupt Mask Register
0x01C2 2008	0x01E2 8008	ICSTR	I2C Interrupt Status Register
0x01C2 200C	0x01E2 800C	ICCLKL	I2C Clock Low-Time Divider Register
0x01C2 2010	0x01E2 8010	ICCLKH	I2C Clock High-Time Divider Register
0x01C2 2014	0x01E2 8014	ICCNT	I2C Data Count Register
0x01C2 2018	0x01E2 8018	ICDRR	I2C Data Receive Register
0x01C2 201C	0x01E2 801C	ICSAR	I2C Slave Address Register
0x01C2 2020	0x01E2 8020	ICDXR	I2C Data Transmit Register
0x01C2 2024	0x01E2 8024	ICMDR	I2C Mode Register
0x01C2 2028	0x01E2 8028	ICIVR	I2C Interrupt Vector Register
0x01C2 202C	0x01E2 802C	ICEMDR	I2C Extended Mode Register
0x01C2 2030	0x01E2 8030	ICPSC	I2C Prescaler Register
0x01C2 2034	0x01E2 8034	REVID1	I2C Revision Identification Register 1
0x01C2 2038	0x01E2 8038	REVID2	I2C Revision Identification Register 2
0x01C2 2048	0x01E2 8048	ICPFUNC	I2C Pin Function Register
0x01C2 204C	0x01E2 804C	ICPDIR	I2C Pin Direction Register
0x01C2 2050	0x01E2 8050	ICPDIN	I2C Pin Data In Register
0x01C2 2054	0x01E2 8054	ICPDOUT	I2C Pin Data Out Register
0x01C2 2058	0x01E2 8058	ICPDSET	I2C Pin Data Set Register
0x01C2 205C	0x01E2 805C	ICPDCLR	I2C Pin Data Clear Register

5.22.3 I2C Electrical Data/Timing

5.22.3.1 Inter-Integrated Circuit (I2C) Timing

Table 5-87 and Table 5-88 assume testing over recommended operating conditions (see Figure 5-63 and Figure 5-64).

Table 5-87. I2C Input Timing Requirements(1)

NO.				MIN	MAX	UNIT
1	$t_{c(SCL)}$	Cycle time, I2Cx_SCL	Standard Mode	10		µs
			Fast Mode	2.5		
2	$t_{su(SCLH-SDAL)}$	Setup time, I2Cx_SCL high before I2Cx_SDA low	Standard Mode	4.7		µs
			Fast Mode	0.6		
3	$t_{h(SCLL-SDAL)}$	Hold time, I2Cx_SCL low after I2Cx_SDA low	Standard Mode	4		µs
			Fast Mode	0.6		
4	$t_{w(SCLL)}$	Pulse duration, I2Cx_SCL low	Standard Mode	4.7		µs
			Fast Mode	1.3		
5	$t_{w(SCLH)}$	Pulse duration, I2Cx_SCL high	Standard Mode	4		µs
			Fast Mode	0.6		
6	$t_{su(SDA-SCLH)}$	Setup time, I2Cx_SDA before I2Cx_SCL high	Standard Mode	250		ns
			Fast Mode	100		

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.

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Table 5-87. I2C Input Timing Requirements[1] (continued)

NO.				MIN	MAX	UNIT
7	$t_{h(SDA-SCLL)}$	Hold time, I2Cx_SDA after I2Cx_SCL low	Standard Mode	0		µs
			Fast Mode	0	0.9	
8	$t_{w(SDAH)}$	Pulse duration, I2Cx_SDA high	Standard Mode	4.7		µs
			Fast Mode	1.3		
9	$t_{r(SDA)}$	Rise time, I2Cx_SDA	Standard Mode		1000	ns
			Fast Mode	$20 + 0.1C_b$	300	
10	$t_{r(SCL)}$	Rise time, I2Cx_SCL	Standard Mode		1000	ns
			Fast Mode	$20 + 0.1C_b$	300	
11	$t_{f(SDA)}$	Fall time, I2Cx_SDA	Standard Mode		300	ns
			Fast Mode	$20 + 0.1C_b$	300	
12	$t_{f(SCL)}$	Fall time, I2Cx_SCL	Standard Mode		300	ns
			Fast Mode	$20 + 0.1C_b$	300	
13	$t_{su(SCLH-SDAH)}$	Setup time, I2Cx_SCL high before I2Cx_SDA high	Standard Mode	4		µs
			Fast Mode	0.6		
14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)	Standard Mode	N/A		ns
			Fast Mode	0	50	
15	C_b	Capacitive load for each bus line	Standard Mode		400	pF
			Fast Mode		400	

Table 5-88. I2C Switching Characteristics[1][2]

NO.	PARAMETER			MIN	MAX	UNIT
16	$t_{c(SCL)}$	Cycle time, I2Cx_SCL	Standard Mode	10		µs
			Fast Mode	2.5		
17	$t_{su(SCLH-SDAL)}$	Setup time, I2Cx_SCL high before I2Cx_SDA low	Standard Mode	4.7		µs
			Fast Mode	0.6		
18	$t_{h(SDAL-SCLL)}$	Hold time, I2Cx_SCL low after I2Cx_SDA low	Standard Mode	4		µs
			Fast Mode	0.6		
19	$t_{w(SCLL)}$	Pulse duration, I2Cx_SCL low	Standard Mode	4.7		µs
			Fast Mode	1.3		
20	$t_{w(SCLH)}$	Pulse duration, I2Cx_SCL high	Standard Mode	4		µs
			Fast Mode	0.6		
21	$t_{su(SDAV-SCLH)}$	Setup time, I2Cx_SDA valid before I2Cx_SCL high	Standard Mode	250		ns
			Fast Mode	100		
22	$t_{h(SCLL-SDAV)}$	Hold time, I2Cx_SDA valid after I2Cx_SCL low	Standard Mode	0		µs
			Fast Mode	0	0.9	
23	$t_{w(SDAH)}$	Pulse duration, I2Cx_SDA high	Standard Mode	4.7		µs
			Fast Mode	1.3		
28	$t_{su(SCLH-SDAH)}$	Setup time, I2Cx_SCL high before I2Cx_SDA high	Standard Mode	4		µs
			Fast Mode	0.6		

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(2) I2C must be configured correctly to meet the timings in Table 5-88.

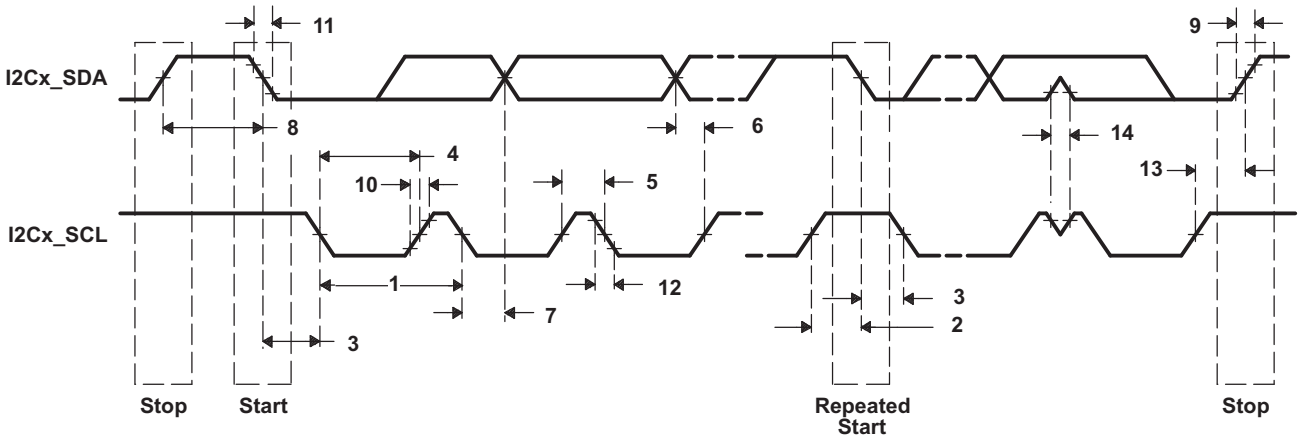

Figure 5-63. I2C Receive Timings

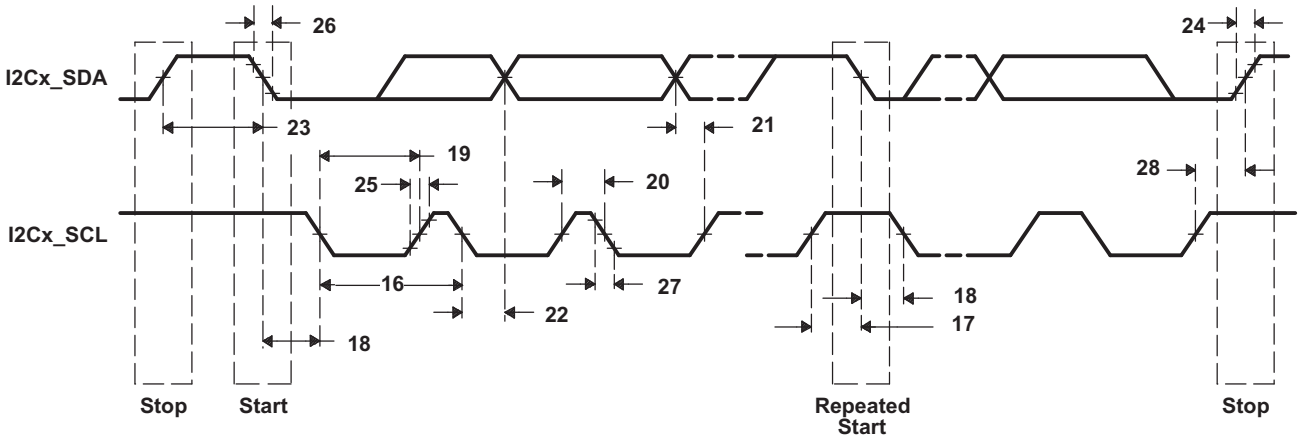

Figure 5-64. I2C Transmit Timings

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5.23 Universal Asynchronous Receiver/Transmitter (UART)

The device has 3 UART peripherals. Each UART has the following features:

- 16-byte storage space for both the transmitter and receiver FIFOs
- 1, 4, 8, or 14 byte selectable receiver FIFO trigger level for autoflow control and DMA
- DMA signaling capability for both received and transmitted data
- Programmable auto-rts and auto-cts for autoflow control
- Programmable Baud Rate up to 3MBaud
- Programmable Oversampling Options of x13 and x16
- Frequency pre-scale values from 1 to 65,535 to generate appropriate baud rates
- Prioritized interrupts
- Programmable serial data formats
  - 5, 6, 7, or 8-bit characters
  - Even, odd, or no parity bit generation and detection
  - 1, 1.5, or 2 stop bit generation
- False start bit detection
- Line break generation and detection
- Internal diagnostic capabilities
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, and framing error simulation
- Modem control functions (CTS, RTS) on ***UART0 only***.

The UART registers are listed in Section 5.23.1

5.23.1 UART Peripheral Registers Description(s)

Table 5-89 is the list of UART registers. See the *TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.* – Literature Number SPRUFK9 for more details.

Table 5-89. UART Registers

UART0 BYTE ADDRESS	UART1 BYTE ADDRESS	UART2 BYTE ADDRESS	REGISTER NAME	Register Description
0x01C4 2000	0x01D0 C000	0x01D0 D000	RBR	Receiver Buffer Register (read only)
0x01C4 2000	0x01D0 C000	0x01D0 D000	THR	Transmitter Holding Register (write only)
0x01C4 2004	0x01D0 C004	0x01D0 D004	IER	Interrupt Enable Register
0x01C4 2008	0x01D0 C008	0x01D0 D008	IIR	Interrupt Identification Register (read only)
0x01C4 2008	0x01D0 C008	0x01D0 D008	FCR	FIFO Control Register (write only)
0x01C4 200C	0x01D0 C00C	0x01D0 D00C	LCR	Line Control Register
0x01C4 2010	0x01D0 C010	0x01D0 D010	MCR	Modem Control Register
0x01C4 2014	0x01D0 C014	0x01D0 D014	LSR	Line Status Register
0x01C4 2018	0x01D0 C018	0x01D0 D018	MSR	Modem Status Register
0x01C4 201C	0x01D0 C01C	0x01D0 D01C	SCR	Scratchpad Register
0x01C4 2020	0x01D0 C020	0x01D0 D020	DLL	Divisor LSB Latch
0x01C4 2024	0x01D0 C024	0x01D0 D024	DLH	Divisor MSB Latch
0x01C4 2028	0x01D0 C028	0x01D0 D028	REVID1	Revision Identification Register 1
0x01C4 2030	0x01D0 C030	0x01D0 D030	PWREMU_MGMT	Power and Emulation Management Register
0x01C4 2034	0x01D0 C034	0x01D0 D034	MDR	Mode Definition Register

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5.23.2 UART Electrical Data/Timing

Table 5-90. Timing Requirements for UARTx Receive(1)(2) (see Figure 5-65)

NO.			MIN	MAX	UNIT
4	$t_{w(URXDB)}$	Pulse duration, receive data bit (RXDn)	0.96U	1.05U	ns
5	$t_{w(URXSB)}$	Pulse duration, receive start bit	0.96U	1.05U	ns

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(2) U = UART baud time = 1/programmed baud rate.

Table 5-91. Switching Characteristics Over Recommended Operating Conditions for UARTx Transmit(1)(2) (see Figure 5-65)

NO.	PARAMETER		MIN	MAX	UNIT
1	$f_{(baud)}$	Maximum programmable baud rate		3	MBaud
2	$t_{w(UTXDB)}$	Pulse duration, transmit data bit (TXDn)	U - 2	U + 2	ns
3	$t_{w(UTXSB)}$	Pulse duration, transmit start bit	U - 2	U + 2	ns

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(2) U = UART baud time = 1/programmed baud rate.

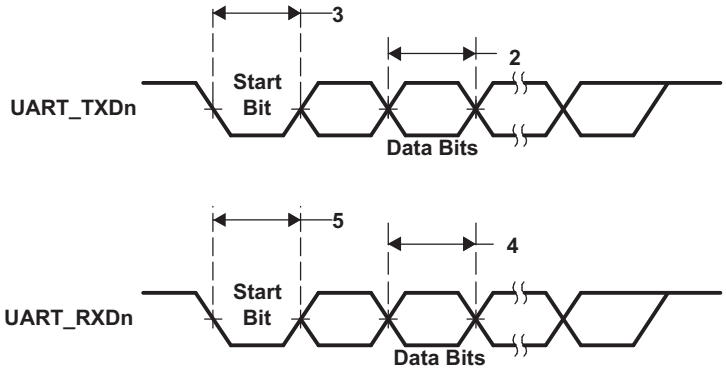

Figure 5-65. UART Transmit/Receive Timing

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5.24 USB1 Host Controller (USB1.1 OHCI)

All OMAPL137 USB interfaces are compliant with Universal Serial Bus Specifications, Revision 1.1.

Table 5-92 is the list of USB Host Controller registers. See the *TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.* – Literature Number SPRUFK9 for more details.

Table 5-92. USB Host Controller (USB1) Registers

USB BYTE ADDRESS	REGISTER NAME	Register Description
0x01E2 5000	HCREVISION	OHCI Revision Number Register
0x01E2 5004	HCCONTROL	HC Operating Mode Register
0x01E2 5008	HCCOMMANDSTATUS	HC Command and Status Register
0x01E2 500C	HCINTERRUPTSTATUS	HC Interrupt and Status Register
0x01E2 5010	HCINTERRUPTENABLE	HC Interrupt Enable Register
0x01E2 5014	HCINTERRUPTDISABLE	HC Interrupt Disable Register
0x01E2 5018	HCHCCA	HC HCAA Address Register(1)
0x01E2 501C	HCPERIODCURRENTED	HC Current Periodic Register(1)
0x01E2 5020	HCCONTROLHEADED	HC Head Control Register(1)
0x01E2 5024	HCCONTROLCURRENTED	HC Current Control Register(1)
0x01E2 5028	HCBULKHEADED	HC Head Bulk Register(1)
0x01E2 502C	HCBULKCURRENTED	HC Current Bulk Register(1)
0x01E2 5030	HCDONEHEAD	HC Head Done Register(1)
0x01E2 5034	HCFMINTERVAL	HC Frame Interval Register
0x01E2 5038	HCFMREMAINING	HC Frame Remaining Register
0x01E2 503C	HCFMNUMBER	HC Frame Number Register
0x01E2 5040	HCPERIODICSTART	HC Periodic Start Register
0x01E2 5044	HCLSTHRESHOLD	HC Low-Speed Threshold Register
0x01E2 5048	HCRHDESCRIPTORA	HC Root Hub A Register
0x01E2 504C	HCRHDESCRIPTORB	HC Root Hub B Register
0x01E2 5050	HCRHSTATUS	HC Root Hub Status Register
0x01E2 5054	HCRHPORTSTATUS1	HC Port 1 Status and Control Register(2)
0x01E2 5058	HCRHPORTSTATUS2	HC Port 2 Status and Control Register(3)

(1) Restrictions apply to the physical addresses used in these registers.
(2) Connected to the integrated USB1.1 phy pins (USB1_DM, USB1_DP).
(3) Although the controller implements two ports, the second port cannot be used.

Table 5-93. Switching Characteristics Over Recommended Operating Conditions for USB1(1)

NO.	PARAMETER		LOW SPEED		FULL SPEED		UNIT
			MIN	MAX	MAX	MAX	
U1	t_r	Rise time, USB.DP and USB.DM signals(2)	75(2)	300(2)	4(2)	20(2)	ns
U2	t_f	Fall time, USB.DP and USB.DM signals(2)	75(2)	300(2)	4(2)	20(2)	ns
U3	t_{RFM}	Rise/Fall time matching(3)	80(3)	120(3)	90(3)	110(3)	%
U4	V_{CRS}	Output signal cross-over voltage(2)	1.3(2)	2(2)	1.3(2)	2(2)	V
U5	t_j	Differential propagation jitter(4)	-25(4)	25(4)	-2(4)	2(4)	ns
U6	f_{op}	Operating frequency(5)		1.5		12	MHz

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(2) Low Speed: C_L = 200 pF. High Speed: C_L = 50pF
(3) t_{RFM} =(t_r/t_f) x 100
(4) $t_{jr} = t_{px(1)} - t_{px(0)}$
(5) $f_{op} = 1/t_{per}$

5.25 USB0 OTG (USB2.0 OTG)

The USB2.0 peripheral supports the following features:

- USB 2.0 peripheral at speeds high speed and full speed (FS: 12 Mb/s)
- USB 2.0 host at speeds FS, and low speed (LS: 1.5 Mb/s)
- All transfer modes (control, bulk, interrupt, and isochronous)
- 4 Transmit (TX) and 4 Receive (RX) endpoints in addition to endpoint 0
- FIFO RAM
  - 4K endpoint
  - Programmable size
- Integrated USB 2.0 High Speed PHY
- Connects to a standard Charge Pump for VBUS 5 V generation
- RNDIS mode for accelerating RNDIS type protocols using short packet termination over USB

Table 5-94 is the list of USB OTG registers. See the *TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.* – Literature Number SPRUFK9 for more details.

Table 5-94. Universal Serial Bus OTG (USB0) Registers

BYTE ADDRESS	Acronym	Register Description
0x01E0 0000		Revision Register
0x01E0 0004	CTRLR	Control Register
0x01E0 0008	STATR	Status Register
0x01E0 000C		Emulation Register
0x01E0 0010		Mode Register
0x01E0 0014	AUTOREQ	Autorequest Register
0x01E0 0018		SRP Fix Time Register
0x01E0 001C		RX Teardown Register
0x01E0 0020	INTSRCR	USB Interrupt Source Register
0x01E0 0024	INTSETR	USB Interrupt Source Set Register
0x01E0 0028	INTCLRR	USB Interrupt Source Clear Register
0x01E0 002C	INTMSKR	USB Interrupt Mask Register
0x01E0 0030	INTMSKSETR	USB Interrupt Mask Set Register
0x01E0 0034	INTMSKCLRR	USB Interrupt Mask Clear Register
0x01E0 0038	INTMASKEDR	USB Interrupt Source Masked Register
0x01E0 003C	EOIR	USB End of Interrupt Register
0x01E0 0040	INTVECTR	USB Interrupt Vector Register
0x01E0 0050	RNDISEP1	Generic RNDIS Size EP1
0x01E0 0054	RNDISEP2	Generic RNDIS Size EP2
0x01E0 0058	RNDISEP3	Generic RNDIS Size EP3
0x01E0 005C	RNDISEP4	Generic RNDIS Size EP4
0x01E0 0400	FADDR	Function Address Register
0x01E0 0401	POWER	Power Management Register
0x01E0 0402	INTRTX	Interrupt Register for Endpoint 0 plus Transmit Endpoints 1 to 4
0x01E0 0404	INTRRX	Interrupt Register for Receive Endpoints 1 to 4
0x01E0 0406	INTRTXE	Interrupt enable register for INTRTX
0x01E0 0408	INTRRXE	Interrupt Enable Register for INTRRX
0x01E0 040A	INTRUSB	Interrupt Register for Common USB Interrupts
0x01E0 040B	INTRUSBE	Interrupt Enable Register for INTRUSB
0x01E0 040C	FRAME	Frame Number Register
0x01E0 040E	INDEX	Index Register for Selecting the Endpoint Status and Control Registers

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Table 5-94. Universal Serial Bus OTG (USB0) Registers (continued)

BYTE ADDRESS	Acronym	Register Description
0x01E0 040F	TESTMODE	Register to Enable the USB 2.0 Test Modes
Indexed Registers These registers operate on the endpoint selected by the INDEX register		
0x01E0 0410	TXMAXP	Maximum Packet Size for Peripheral/Host Transmit Endpoint (Index register set to select Endpoints 1-4 only)
0x01E0 0412	PERI_CSR0	Control Status Register for Endpoint 0 in Peripheral Mode. (Index register set to select Endpoint 0)
	HOST_CSR0	Control Status Register for Endpoint 0 in Host Mode. (Index register set to select Endpoint 0)
	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint. (Index register set to select Endpoints 1-4)
	HOST_TXCSR	Control Status Register for Host Transmit Endpoint. (Index register set to select Endpoints 1-4)
0x01E0 0414	RXMAXP	Maximum Packet Size for Peripheral/Host Receive Endpoint (Index register set to select Endpoints 1-4 only)
0x01E0 0416	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint. (Index register set to select Endpoints 1-4)
	HOST_RXCSR	Control Status Register for Host Receive Endpoint. (Index register set to select Endpoints 1-4)
0x01E0 0418	COUNT0	Number of Received Bytes in Endpoint 0 FIFO. (Index register set to select Endpoint 0)
	RXCOUNT	Number of Bytes in Host Receive Endpoint FIFO. (Index register set to select Endpoints 1- 4)
0x01E0 041A	HOST_TYPE0	Defines the speed of Endpoint 0
0x01E0 041B	HOST_TXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host Transmit endpoint. (Index register set to select Endpoints 1-4 only)
	HOST_NAKLIMIT0	Sets the NAK response timeout on Endpoint 0. (Index register set to select Endpoint 0)
	HOST_TXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Transmit endpoint. (Index register set to select Endpoints 1-4 only)
0x01E0 041C	HOST_RXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host Receive endpoint. (Index register set to select Endpoints 1-4 only)
0x01E0 041D	HOST_RXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Receive endpoint. (Index register set to select Endpoints 1-4 only)
0x01E0 041F	CONFIGDATA	Returns details of core configuration. (Index register set to select Endpoint 0)
FIFO		
0x01E0 0420	FIFO0	Transmit and Receive FIFO Register for Endpoint 0
0x01E0 0424	FIFO1	Transmit and Receive FIFO Register for Endpoint 1
0x01E0 0428	FIFO2	Transmit and Receive FIFO Register for Endpoint 2
0x01E0 042C	FIFO3	Transmit and Receive FIFO Register for Endpoint 3
0x01E0 0430	FIFO4	Transmit and Receive FIFO Register for Endpoint 4
OTG Device Control		
0x01E0 0460	DEVCTL	Device Control Register
Dynamic FIFO Control		
0x01E0 0462	TXFIFOSZ	Transmit Endpoint FIFO Size (Index register set to select Endpoints 1-4 only)
0x01E0 0463	RXFIFOSZ	Receive Endpoint FIFO Size (Index register set to select Endpoints 1-4 only)
0x01E0 0464	TXFIFOADDR	Transmit Endpoint FIFO Address (Index register set to select Endpoints 1-4 only)

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Table 5-94. Universal Serial Bus OTG (USB0) Registers (continued)

BYTE ADDRESS	Acronym	Register Description
0x01E0 0466	RXFIFOADDR	Receive Endpoint FIFO Address (Index register set to select Endpoints 1-4 only)
Target Endpoint 0 Control Registers, Valid Only in Host Mode		
0x01E0 0480	TXFUNCADDR	Address of the target function that has to be accessed through the associated Transmit Endpoint.
0x01E0 0482	TXHUBADDR	Address of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 0483	TXHUBPORT	Port of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 0484	RXFUNCADDR	Address of the target function that has to be accessed through the associated Receive Endpoint.
0x01E0 0486	RXHUBADDR	Address of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 0487	RXHUBPORT	Port of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
Target Endpoint 1 Control Registers, Valid Only in Host Mode		
0x01E0 0488	TXFUNCADDR	Address of the target function that has to be accessed through the associated Transmit Endpoint.
0x01E0 048A	TXHUBADDR	Address of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 048B	TXHUBPORT	Port of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 048C	RXFUNCADDR	Address of the target function that has to be accessed through the associated Receive Endpoint.
0x01E0 048E	RXHUBADDR	Address of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 048F	RXHUBPORT	Port of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
Target Endpoint 2 Control Registers, Valid Only in Host Mode		
0x01E0 0490	TXFUNCADDR	Address of the target function that has to be accessed through the associated Transmit Endpoint.
0x01E0 0492	TXHUBADDR	Address of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 0493	TXHUBPORT	Port of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 0494	RXFUNCADDR	Address of the target function that has to be accessed through the associated Receive Endpoint.
0x01E0 0496	RXHUBADDR	Address of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 0497	RXHUBPORT	Port of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
Target Endpoint 3 Control Registers, Valid Only in Host Mode		
0x01E0 0498	TXFUNCADDR	Address of the target function that has to be accessed through the associated Transmit Endpoint.

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Table 5-94. Universal Serial Bus OTG (USB0) Registers (continued)

BYTE ADDRESS	Acronym	Register Description
0x01E0 049A	TXHUBADDR	Address of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 049B	TXHUBPORT	Port of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 049C	RXFUNCADDR	Address of the target function that has to be accessed through the associated Receive Endpoint.
0x01E0 049E	RXHUBADDR	Address of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 049F	RXHUBPORT	Port of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
Target Endpoint 4 Control Registers, Valid Only in Host Mode		
0x01E0 04A0	TXFUNCADDR	Address of the target function that has to be accessed through the associated Transmit Endpoint.
0x01E0 04A2	TXHUBADDR	Address of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 04A3	TXHUBPORT	Port of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 04A4	RXFUNCADDR	Address of the target function that has to be accessed through the associated Receive Endpoint.
0x01E0 04A6	RXHUBADDR	Address of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
0x01E0 04A7	RXHUBPORT	Port of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub.
Control and Status Register for Endpoint 0		
0x01E0 0502	PERI_CSR0	Control Status Register for Endpoint 0 in Peripheral Mode
	HOST_CSR0	Control Status Register for Endpoint 0 in Host Mode
0x01E0 0508	COUNT0	Number of Received Bytes in Endpoint 0 FIFO
0x01E0 050A	HOST_TYPE0	Defines the Speed of Endpoint 0
0x01E0 050B	HOST_NAKLIMIT0	Sets the NAK Response Timeout on Endpoint 0
0x01E0 050F	CONFIGDATA	Returns details of core configuration.
Control and Status Register for Endpoint 1		
0x01E0 0510	TXMAXP	Maximum Packet Size for Peripheral/Host Transmit Endpoint
0x01E0 0512	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
	HOST_TXCSR	Control Status Register for Host Transmit Endpoint (host mode)
0x01E0 0514	RXMAXP	Maximum Packet Size for Peripheral/Host Receive Endpoint
0x01E0 0516	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
	HOST_RXCSR	Control Status Register for Host Receive Endpoint (host mode)
0x01E0 0518	RXCOUNT	Number of Bytes in Host Receive endpoint FIFO
0x01E0 051A	HOST_TXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host Transmit endpoint.
0x01E0 051B	HOST_TXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Transmit endpoint.

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Table 5-94. Universal Serial Bus OTG (USB0) Registers (continued)

BYTE ADDRESS	Acronym	Register Description
0x01E0 051C	HOST_RXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host Receive endpoint.
0x01E0 051D	HOST_RXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Receive endpoint.
Control and Status Register for Endpoint 2		
0x01E0 0520	TXMAXP	Maximum Packet Size for Peripheral/Host Transmit Endpoint
0x01E0 0522	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
	HOST_TXCSR	Control Status Register for Host Transmit Endpoint (host mode)
0x01E0 0524	RXMAXP	Maximum Packet Size for Peripheral/Host Receive Endpoint
0x01E0 0526	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
	HOST_RXCSR	Control Status Register for Host Receive Endpoint (host mode)
0x01E0 0528	RXCOUNT	Number of Bytes in Host Receive endpoint FIFO
0x01E0 052A	HOST_TXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host Transmit endpoint.
0x01E0 052B	HOST_TXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Transmit endpoint.
0x01E0 052C	HOST_RXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host Receive endpoint.
0x01E0 052D	HOST_RXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Receive endpoint.
Control and Status Register for Endpoint 3		
0x01E0 0530	TXMAXP	Maximum Packet Size for Peripheral/Host Transmit Endpoint
0x01E0 0532	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
	HOST_TXCSR	Control Status Register for Host Transmit Endpoint (host mode)
0x01E0 0534	RXMAXP	Maximum Packet Size for Peripheral/Host Receive Endpoint
0x01E0 0536	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
	HOST_RXCSR	Control Status Register for Host Receive Endpoint (host mode)
0x01E0 0538	RXCOUNT	Number of Bytes in Host Receive endpoint FIFO
0x01E0 053A	HOST_TXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host Transmit endpoint.
0x01E0 053B	HOST_TXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Transmit endpoint.
0x01E0 053C	HOST_RXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host Receive endpoint.
0x01E0 053D	HOST_RXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Receive endpoint.
Control and Status Register for Endpoint 4		
0x01E0 0540	TXMAXP	Maximum Packet Size for Peripheral/Host Transmit Endpoint
0x01E0 0542	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
	HOST_TXCSR	Control Status Register for Host Transmit Endpoint (host mode)
0x01E0 0544	RXMAXP	Maximum Packet Size for Peripheral/Host Receive Endpoint

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Table 5-94. Universal Serial Bus OTG (USB0) Registers (continued)

BYTE ADDRESS	Acronym	Register Description
0x01E0 0546	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
	HOST_RXCSR	Control Status Register for Host Receive Endpoint (host mode)
0x01E0 0548	RXCOUNT	Number of Bytes in Host Receive endpoint FIFO
0x01E0 054A	HOST_TXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host Transmit endpoint.
0x01E0 054B	HOST_TXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Transmit endpoint.
0x01E0 054C	HOST_RXTYPE	Sets the operating speed, transaction protocol and peripheral endpoint number for the host Receive endpoint.
0x01E0 054D	HOST_RXINTERVAL	Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Receive endpoint.
DMA Registers		
0x01E0 1000	DMAREV	DMA Revision Register
0x01E0 1004	TDFDQ	DMA Teardown Free Descriptor Queue Control Register
0x01E0 1008	DMAEMU	DMA Emulation Control Register
0x01E0 1800	TGCR[0]	Transmit Channel 0 Global Configuration Register
0x01E0 1808	RXGCR[0]	Receive Channel 0 Global Configuration Register
0x01E0 180C	RXHPCRA[0]	Receive Channel 0 Host Packet Configuration Register A
0x01E0 1810	RXHPCRB[0]	Receive Channel 0 Host Packet Configuration Register B
0x01E0 1820	TGCR[1]	Transmit Channel 1 Global Configuration Register
0x01E0 1828	RXGCR[1]	Receive Channel 1 Global Configuration Register
0x01E0 182C	RXHPCRA[1]	Receive Channel 1 Host Packet Configuration Register A
0x01E0 1830	RXHPCRB[1]	Receive Channel 1 Host Packet Configuration Register B
0x01E0 1840	TGCR[2]	Transmit Channel 2 Global Configuration Register
0x01E0 1848	RXGCR[2]	Receive Channel 2 Global Configuration Register
0x01E0 184C	RXHPCRA[2]	Receive Channel 2 Host Packet Configuration Register A
0x01E0 1850	RXHPCRB[2]	Receive Channel 2 Host Packet Configuration Register B
0x01E0 1860	TGCR[3]	Transmit Channel 3 Global Configuration Register
0x01E0 1868	RXGCR[3]	Receive Channel 3 Global Configuration Register
0x01E0 186C	RXHPCRA[3]	Receive Channel 3 Host Packet Configuration Register A
0x01E0 1870	RXHPCRB[3]	Receive Channel 3 Host Packet Configuration Register B
0x01E0 2C00	DMA_SCHED_CTRL	DMA Scheduler Control Register
0x01E0 2D00	ENTRY[0]	DMA Scheduler Table Word 0
0x01E0 2D04	ENTRY[1]	DMA Scheduler Table Word 1
. . .	. . .	. . .
0x01E0 2DFC	ENTRY[63]	DMA Scheduler Table Word 63
Queue Manager Registers		
0x01E0 4000	QMGRREV	Queue Manager Revision Register
0x01E0 4008	DIVERSION	Queue Diversion Register
0x01E0 4020	FDBSC0	Free Descriptor/Buffer Starvation Count Register 0
0x01E0 4024	FDBSC1	Free Descriptor/Buffer Starvation Count Register 1
0x01E0 4028	FDBSC2	Free Descriptor/Buffer Starvation Count Register 2
0x01E0 402C	FDBSC3	Free Descriptor/Buffer Starvation Count Register 3
0x01E0 4080	LRAM0BASE	Linking RAM Region 0 Base Address Register
0x01E0 4084	LRAM0SIZE	Linking RAM Region 0 Size Register
0x01E0 4088	LRAM1BASE	Linking RAM Region 1 Base Address Register
0x01E0 4090	PEND0	Queue Pending Register 0

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Table 5-94. Universal Serial Bus OTG (USB0) Registers (continued)

BYTE ADDRESS	Acronym	Register Description
0x01E0 4094	PEND1	Queue Pending Register 1
0x01E0 5000	QMEMRBASE[0]	Memory Region 0 Base Address Register
0x01E0 5004	QMEMRCTRL[0]	Memory Region 0 Control Register
0x01E0 5010	QMEMRBASE[1]	Memory Region 1 Base Address Register
0x01E0 5014	QMEMRCTRL[1]	Memory Region 1 Control Register
. . .	. . .	. . .
0x01E0 5070	QMEMRBASE[7]	Memory Region 7 Base Address Register
0x01E0 5074	QMEMRCTRL[7]	Memory Region 7 Control Register
0x01E0 6000	QCTRL_CTRLA[0]	Queue Manager Queue 0 Control Register A
0x01E0 6004	QCTRL_CTRLB[0]	Queue Manager Queue 0 Control Register B
0x01E0 6008	QCTRL_CTRLC[0]	Queue Manager Queue 0 Control Register C
0x01E0 600C	QCTRL_CTRLD[0]	Queue Manager Queue 0 Control Register D
0x01E0 6010	QCTRL_CTRLA[1]	Queue Manager Queue 1 Control Register A
0x01E0 6014	QCTRL_CTRLB[1]	Queue Manager Queue 1 Control Register B
0x01E0 6018	QCTRL_CTRLC[1]	Queue Manager Queue 1 Control Register C
0x01E0 601C	QCTRL_CTRLD[1]	Queue Manager Queue 1 Control Register D
. . .	. . .	. . .
0x01E0 63F0	QCTRL_CTRLA[63]	Queue Manager Queue 63 Status Register A
0x01E0 63F4	QCTRL_CTRLB[63]	Queue Manager Queue 63 Status Register B
0x01E0 63F8	QCTRL_CTRLC[63]	Queue Manager Queue 63 Status Register C
0x01E0 63FC	QCTRL_CTRLD[63]	Queue Manager Queue 63 Status Register D
0x01E0 6800	QCTRL_STATA[0]	Queue Manager Queue 0 Status Register A
0x01E0 6804	QCTRL_STATB[0]	Queue Manager Queue 0 Status Register B
0x01E0 6808	QCTRL_STATC[0]	Queue Manager Queue 0 Status Register C
0x01E0 6810	QCTRL_STATA[1]	Queue Manager Queue 1 Status Register A
0x01E0 6814	QCTRL_STATB[1]	Queue Manager Queue 1 Status Register B
0x01E0 6818	QCTRL_STATC[1]	Queue Manager Queue 1 Status Register C
. . .	. . .	. . .
0x01E0 6BF0	QCTRL_STATA[63]	Queue Manager Queue 63 Status Register A
0x01E0 6BF4	QCTRL_STATB[63]	Queue Manager Queue 63 Status Register B
0x01E0 6BF8	QCTRL_STATC[63]	Queue Manager Queue 63 Status Register C

5.25.1 USB0 Electrical Data/Timing

Table 5-95. Switching Characteristics Over Recommended Operating Conditions for USB0(1) (see Figure 5-66)

NO.	PARAMETER		LOW SPEED 1.5 Mbps		FULL SPEED 12 Mbps		HIGH SPEED 480 Mbps		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{r(D)}$	Rise time, USB0_DP and USB0_DM signals(2)	75	300	4	20	0.5		ns
2	$t_{f(D)}$	Fall time, USB0_DP and USB0_DM signals(2)	75	300	4	20	0.5		ns
3	t_{rfM}	Rise/Fall time, matching(3)	80	120	90	111	–	–	%
4	V_{CRS}	Output signal cross-over voltage(2)	1.3	2	1.3	2	–	–	V
5	$t_{jr(source)NT}$	Source (Host) Driver jitter, next transition		2		2			(4)ns

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(2) Low Speed: C_L = 200 pF, Full Speed: C_L = 50 pF, High Speed: C_L = 50 pF
(3) $t_{RFM} = (t_r/t_f) \times 100$. [Excluding the first transaction from the Idle state.]
(4) For more detailed information, see the Universal Serial Bus Specification Revision 2.0, Chapter 7. Electrical.

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Table 5-95. Switching Characteristics Over Recommended Operating Conditions for USB0[(1)] (see Figure 5-66) (continued)

NO.	PARAMETER		LOW SPEED 1.5 Mbps		FULL SPEED 12 Mbps		HIGH SPEED 480 Mbps		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
	$t_{jr(FUNC)NT}$	Function Driver jitter, next transition		25		2		(4)	ns
6	$t_{jr(source)PT}$	Source (Host) Driver jitter, paired transition[(5)]		1		1		(4)	ns
	$t_{jr(FUNC)PT}$	Function Driver jitter, paired transition		10		1		(4)	ns
7	$t_{w(EOPT)}$	Pulse duration, EOP transmitter	1250	1500	160	175	–	–	ns
8	$t_{w(EOPR)}$	Pulse duration, EOP receiver	670		82		–		ns
9	$t_{(DRATE)}$	Data Rate		1.5		12		480	Mb/s
10	Z_{DRV}	Driver Output Resistance	–	–	40.5	49.5	40.5	49.5	Ω
11	Z_{INP}	Receiver Input Impedance	100k		100k		-	-	Ω

(5) $t_{jr} = t_{px(1)} - t_{px(0)}$

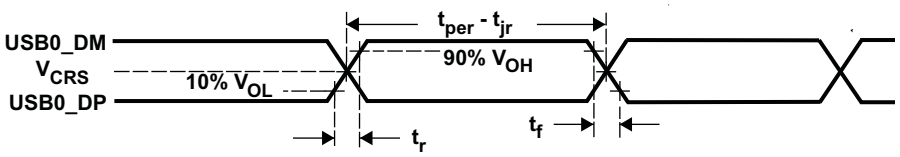

Figure 5-66. USB0 Integrated Transceiver Interface Timing

5.26 Universal Host-Port Interface (UHPI)

5.26.1 HPI Device-Specific Information

The device includes a user-configurable 16-bit Host-port interface (HPI16). See the *TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.* – Literature Number SPRUFK9 for more details.

5.26.2 HPI Peripheral Register Description(s)

Table 5-96. HPI Control Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
0x01E1 0000	PID	Peripheral Identification Register	
0x01E1 0004	PWREMU_MGMT	HPI power and emulation management register	The CPU has read/write access to the PWREMU_MGMT register.
0x01E1 0008	-	Reserved	
0x01E1 000C	GPIO_EN	General Purpose IO Enable Register	
0x01E1 0010	GPIO_DIR1	General Purpose IO Direction Register 1	
0x01E1 0014	GPIO_DAT1	General Purpose IO Data Register 1	
0x01E1 0018	GPIO_DIR2	General Purpose IO Direction Register 2	
0x01E1 001C	GPIO_DAT2	General Purpose IO Data Register 2	
0x01E1 0020	GPIO_DIR3	General Purpose IO Direction Register 3	
0x01E1 0024	GPIO_DAT3	General Purpose IO Data Register 3	
0x01E1 0028	-	Reserved	
0x01E1 002C	-	Reserved	
0x01E1 0030	HPIC	HPI control register	The Host and the CPU both have read/write access to the HPIC register.
0x01E1 0034	HPIA (HPIAW)(1)	HPI address register (Write)	The Host has read/write access to the HPIA registers. The CPU has only read access to the HPIA registers.
0x01E1 0038	HPIA (HPIAR)(1)	HPI address register (Read)	
0x01E1 000C - 0x01E1 07FF	-	Reserved	

(1) There are two 32-bit HPIA registers: HPIAR for read operations and HPIAW for write operations. The HPI can be configured such that HPIAR and HPIAW act as a single 32-bit HPIA (single-HPIA mode) or as two separate 32-bit HPIAs (dual-HPIA mode) from the perspective of the Host. The CPU can access HPIAW and HPIAR independently.

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5.26.3 HPI Electrical Data/Timing

Table 5-97. Timing Requirements for Host-Port Interface Cycles(1)(2) (3)

NO.			MIN	MAX	UNIT
1	$t_{su(SELV-HSTBL)}$	Setup time, select signals(4) valid before $\overline{\text{HSTROBE}}$ low	5		ns
2	$t_{h(HSTBL-SELV)}$	Hold time, select signals(4) valid after $\overline{\text{HSTROBE}}$ low	2		ns
3	$t_{w(HSTBL)}$	Pulse duration, $\overline{\text{HSTROBE}}$ active low	15		ns
4	$t_{w(HSTBH)}$	Pulse duration, $\overline{\text{HSTROBE}}$ inactive high between consecutive accesses	2M		ns
11	$t_{su(HDV-HSTBH)}$	Setup time, host data valid before $\overline{\text{HSTROBE}}$ high	5		ns
12	$t_{h(HSTBH-HDV)}$	Hold time, host data valid after $\overline{\text{HSTROBE}}$ high	1		ns
13	$t_{h(HRDYL-HSTBH)}$	Hold time, $\overline{\text{HSTROBE}}$ high after $\overline{\text{HRDY}}$ low. $\overline{\text{HSTROBE}}$ should not be inactivated until $\overline{\text{HRDY}}$ is active (low); otherwise, HPI writes will not complete properly.	0		ns

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(2) $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: [NOT($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{HCS}}$.
(3) M=SYSCLK2 period (CPU clock frequency)/2 in ns. For example, when running parts at 300 MHz, use M=6.67 ns.
(4) Select signals include: HCNTL[1:0], HR/$\overline{\text{W}}$ and HHWIL.

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Table 5-98. Switching Characteristics for Host-Port Interface Cycles(1)(2) (3) (4)

NO.	PARAMETER			MIN	MAX	UNIT
5	$t_{d(HSTBL-HRDYV)}$	Delay time, HSTROBE low to HRDY valid	For HPI Write, HRDY can go high (*not ready*) for these HPI Write conditions; otherwise, HRDY stays low (*ready*): *Case 1*: Back-to-back HPIA writes (can be either first or second half-word) *Case 2*: HPIA write following a PREFETCH command (can be either first or second half-word) *Case 3*: HPID write when FIFO is full or flushing (can be either first or second half-word) *Case 4*: HPIA write and Write FIFO not empty For HPI Read, HRDY can go high (*not ready*) for these HPI Read conditions: *Case 1*: HPID read (with auto-increment) and data not in Read FIFO (can only happen to first half-word of HPID access) *Case 2*: First half-word access of HPID Read without auto-increment For HPI Read, HRDY stays low (*ready*) for these HPI Read conditions: *Case 1*: HPID read with auto-increment and data is already in Read FIFO (applies to either half-word of HPID access) *Case 2*: HPID read without auto-increment and data is already in Read FIFO (always applies to second half-word of HPID access) *Case 3*: HPIC or HPIA read (applies to either half-word access)		12	ns
5a	$t_{d(HRSL-HRDYV)}$	Delay time HAS low to HRDY valid			13	
6	$t_{en(HSTBL-HD)}$	Enable time, HD driven from HSTROBE low		2		ns
7	$t_{d(HRDYL-HDV)}$	Delay time, HRDY low to HD valid			0	ns
8	$t_{oh(HSTBH-HDV)}$	Output hold time, HD valid after HSTROBE high		1.5		ns
14	$t_{dis(HSTBH-HDV)}$	Disable time, HD high-impedance from HSTROBE high			12	ns
15	$t_{d(HSTBL-HDV)}$	Delay time, HSTROBE low to HD valid	For HPI Read. Applies to conditions where data is already residing in HPID/FIFO: *Case 1*: HPIC or HPIA read *Case 2*: First half-word of HPID read with auto-increment and data is already in Read FIFO *Case 3*: Second half-word of HPID read with or without auto-increment		15	ns
18	$t_{d(HSTBH-HRDYV)}$	Delay time, HSTROBE high to HRDY valid	For HPI Write, HRDY can go high (*not ready*) for these HPI Write conditions; otherwise, HRDY stays low (*ready*): *Case 1*: HPID write when Write FIFO is full (can happen to either half-word) *Case 2*: HPIA write (can happen to either half-word) *Case 3*: HPID write without auto-increment (only happens to second half-word)		12	ns

(1) Parameters are characterized from -40°C to 125°C unless otherwise noted.
(2) M=SYSCLK2 period (CPU clock frequency)/2 in ns. For example, when running parts at 300 MHz, use M=6.67 ns.
(3) HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.
(4) By design, whenever HCS is driven inactive (high), HPI will drive HRDY active (low).

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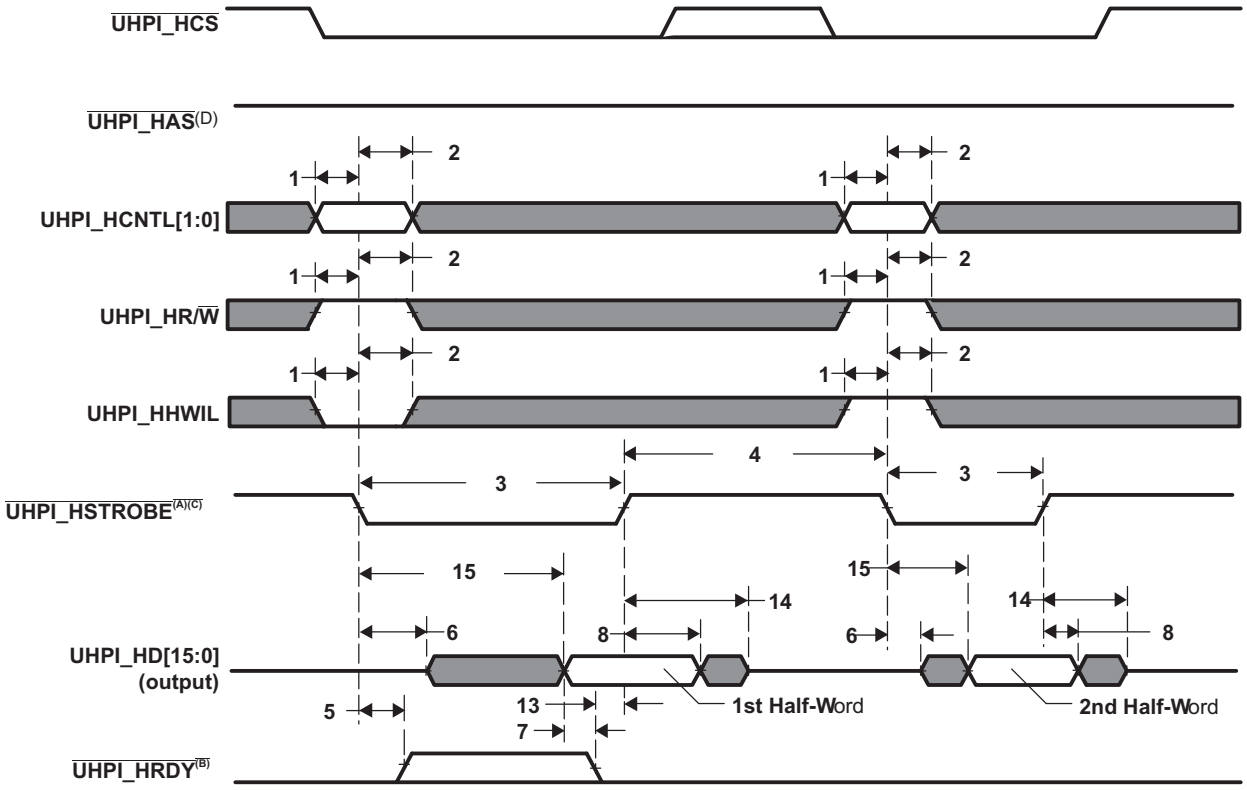


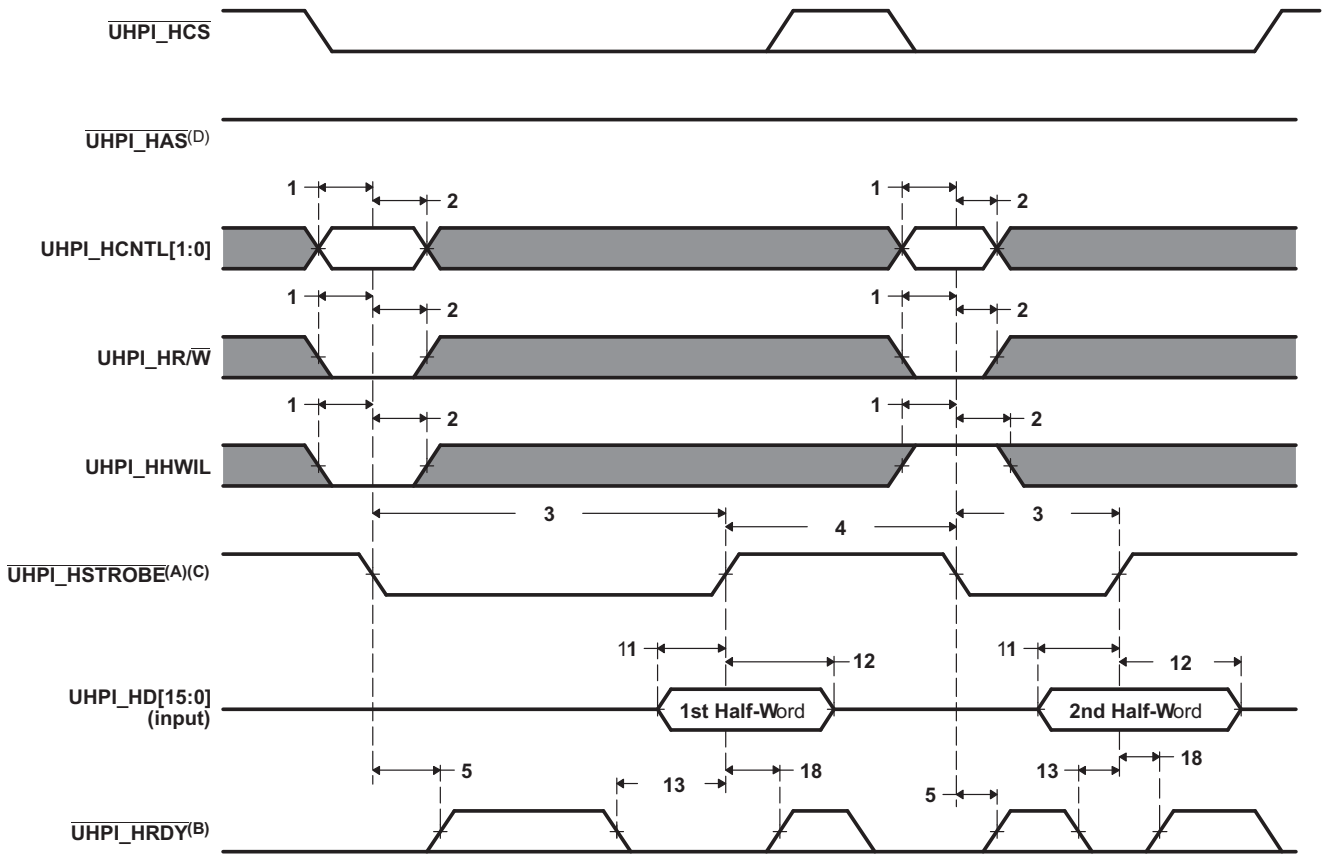
A. UHPI_HSTROBE refers to the following logical operation on UHPI_HCS, UHPI_HDS1, and UHPI_HDS2: [NOT(HDS1 XOR HDS2)] OR UHPI_HCS.

B. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on UHPI_HRDY may or may not occur.

C. UHPI_HCS reflects typical UHPI_HCS behavior when UHPI_HSTROBE assertion is caused by UHPI_HDS1 or UHPI_HDS2. UHPI_HCS timing requirements are reflected by parameters for UHPI_HSTROBE

D The diagram above assumes UHPI_HAS has been pulled high.

Figure 5-67. UHPI Read Timing (HAS Not Used, Tied High)



A. UHPI_HSTROBE refers to the following logical operation on UHPI_HCS, UHPI_HDS1, and UHPI_HDS2: [NOT(HDS1 XOR HDS2)] OR UHPI_HCS.

B. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on UHPI_HRDY may or may not occur.

C. UHPI_HCS reflects typical UHPI_HCS behavior when UHPI_HSTROBE assertion is caused by UHPI_HDS1 or UHPI_HDS2. UHPI_HCS timing requirements are reflected by parameters for UHPI_HSTROBE.

D The diagram above assumes UHPI_HAS has been pulled high.

Figure 5-68. UHPI Write Timing (HAS Not Used, Tied High)

5.27 Memory Protection Units (MPU)

The MPU performs memory protection checking. It inputs a VBUSM or VBUSP bus, checks the address against the fixed and programmable regions to see if the access is allowed. If allowed the transfer is passed unmodified to the output VBUSM or VBUSP bus. If the transfer is illegal (fails the protection check) then the MPU does not pass the transfer to the output bus but rather services the transfer internally back to the input bus (to prevent a hang) returning the fault status to the requestor as well as generating an interrupt about the fault. The following features are supported by the MPU:

- Provides memory protection for fixed and programmable address ranges.
- Supports multiple programmable address region.
- Supports secure and debug access privileges.
- Supports read, write, and execute access privileges.
- Supports privid(8) associations with ranges.
- Generates an interrupt when there is a protection violation, and saves violating transfer parameters.
- MMR access is also protected.

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Table 5-99. MPU Register Descriptions

MPU1 BYTE ADDRESS	MPU2 BYTE ADDRESS	REGISTER NAME	DESCRIPTION
0x01E1 4000	0x01E1 5000	REVISION	Revision
0x01E1 4004	0x01E1 5004	CONFIGURATION	Configuration
0x01E1 4008 - 0x01E1 4009	0x01E1 5008 - 0x01E1 5009	RSVD	Reserved
0x01E1 4010	0x01E1 5010	INTR_RAW_STATUS	Interrupt Raw Status/Set
0x01E1 4014	0x01E1 5014	INTR_ENABLED_STATUS	Interrupt Enabled Status/Clear
0x01E1 4018	0x01E1 5018	INTR_ENABLE	Interrupt Enable
0x01E1 401C	0x01E1 501C	INTR_ENABLE_CLR	Interrupt Enable Clear
0x01E1 4020	0x01E1 5020	RSVD	Reserved
0x01E1 4024	0x01E1 5024	RSVD	Reserved
0x01E1 4028 - 0x01E1 40FF	0x01E1 5028 - 0x01E1 50FF	RSVD	Reserved
0x01E1 4100	0x01E1 5100	FIXED_MPSAR	Fixed 1 Start Address
0x01E1 4104	0x01E1 5104	FIXED_MPEAR	Fixed 1 End Address
0x01E1 4108	0x01E1 5108	FIXED_MPPA	Fixed 1 MPPA
0x01E1 410C	0x01E1 510C	RSVD	Reserved
0x01E1 4110 - 0x01E1 41FF	0x01E1 5110 - 0x01E1 51FF	RSVD	Reserved
0x01E1 4200	0x01E1 5200	PROG0_MPSAR	Programmable 1 Start Address
0x01E1 4204	0x01E1 5204	PROG0_MPEAR	Programmable 1 End Address
0x01E1 4208	0x01E1 5208	PROG0_MPPA	Programmable 1 MPPA
0x01E1 420C	0x01E1 520C	RSVD	Reserved
0x01E1 4210	0x01E1 5210	PROG1_MPSAR	Additional Programmable Range MMRs
0x01E1 4214	0x01E1 5214	PROG1_MPEAR	
0x01E1 4218	0x01E1 5218	PROG1_MPPA	
0x01E1 421C	0x01E1 521C	RSVD	
0x01E1 4220	0x01E1 5220	PROG2_MPSAR	
0x01E1 4224	0x01E1 5224	PROG2_MPEAR	
0x01E1 4228	0x01E1 5228	PROG2_MPPA	
0x01E1 422C	0x01E1 522C	RSVD	
0x01E1 4230	0x01E1 5230	PROG3_MPSAR	
0x01E1 4234	0x01E1 5234	PROG3_MPEAR	
0x01E1 4238	0x01E1 5238	PROG3_MPPA	
0x01E1 423C	0x01E1 523C	RSVD	
0x01E1 4240	0x01E1 5240	PROG4_MPSAR	
0x01E1 4244	0x01E1 5244	PROG4_MPEAR	
0x01E1 4248	0x01E1 5248	PROG4_MPPA	
0x01E1 424C	0x01E1 524C	RSVD	
0x01E1 4250	0x01E1 5250	PROG5_MPSAR	
0x01E1 4254	0x01E1 5254	PROG5_MPEAR	
0x01E1 4258	0x01E1 5258	PROG5_MPPA	
0x01E1 425C - 0x01E1 42FF	0x01E1 525C	RSVD	
-	0x01E1 5260	PROG6_MPSAR	
-	0x01E1 5264	PROG6_MPEAR	

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Table 5-99. MPU Register Descriptions (continued)

MPU1 BYTE ADDRESS	MPU2 BYTE ADDRESS	REGISTER NAME	DESCRIPTION
-	0x01E1 5268	PROG6_MPPA	
-	0x01E1 526C	RSVD	
-	0x01E1 5270	PROG7_MPSAR	
-	0x01E1 5274	PROG7_MPEAR	
-	0x01E1 5278	PROG7_MPPA	
-	0x01E1 527C	RSVD	
-	0x01E1 5280	PROG8_MPSAR	
-	0x01E1 5284	PROG8_MPEAR	
-	0x01E1 5288	PROG8_MPPA	
-	0x01E1 528C	RSVD	
-	0x01E1 5290	PROG9_MPSAR	
-	0x01E1 5294	PROG9_MPEAR	
-	0x01E1 5298	PROG9_MPPA	
-	0x01E1 529C	RSVD	
-	0x01E1 52A0	PROG10_MPSAR	
-	0x01E1 52A4	PROG10_MPEAR	
-	0x01E1 52A8	PROG10_MPPA	
-	0x01E1 52AC	RSVD	
-	0x01E1 52B0	PROG11_MPSAR	
-	0x01E1 52B4	PROG11_MPEAR	
-	0x01E1 52B8	PROG11_MPPA	
-	0x01E1 52BC - 0x01E1 52FF	RSVD	
0x01E1 4300	0x01E1 5300	MPFAR	Fault 1 Address
0x01E1 4304	0x01E1 5304	MPFSR	Fault 1 Status
0x01E1 4308	0x01E1 5308	MPFCR	Fault 1 Clear

5.28 Power and Sleep Controller (PSC)

The Power and Sleep Controllers (PSC) are responsible for managing transitions of system power on/off, clock on/off, resets (device level and module level). It is used primarily to provide granular power control for on chip modules (peripherals and CPU). A PSC module consists of a Global PSC (GPSC) and a set of Local PSCs (LPSCs). The GPSC contains memory mapped registers, PSC interrupts, a state machine for each peripheral/module it controls. An LPSC is associated with every module that is controlled by the PSC and provides clock and reset control. See the *TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.* – Literature Number SPRUFK9 for more details.

The PSC includes the following features:

- Provides a software interface to:
  - Control module clock enable/disable
  - Control module reset
  - Control CPU local reset
- Supports ICEpick TAP Router power, clock and reset features. For details on ICEpick features see http://tiexpressdsp.com/wiki/index.php?title=ICEPICK.

Table 5-100. Power and Sleep Controller (PSC) Registers

PSC0	PSC1	Register	Description
0x01C1 0000	0x01E2 7000	REVID	Peripheral Revision and Class Information Register

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Table 5-100. Power and Sleep Controller (PSC) Registers (continued)

PSC0	PSC1	Register	Description
0x01C1 0018	0x01E2 7018	INTEVAL	Interrupt Evaluation Register
0x01C1 0040	0x01E2 7040	MERRPR0	Module Error Pending Register 0 (module 0-15) (PSC0) Module Error Pending Register 0 (module 0-31) (PSC1)
0x01C1 0050	0x01E2 7050	MERRCR0	Module Error Clear Register 0 (module 0-15) (PSC0) Module Error Clear Register 0 (module 0-31) (PSC1)
0x01C1 0060	0x01E2 7060	PERRPR	Power Error Pending Register
0x01C1 0068	0x01E2 7068	PERRCR	Power Error Clear Register
0x01C1 0120	0x01E2 7120	PTCMD	Power Domain Transition Command Register
0x01C1 0128	0x01E2 7128	PTSTAT	Power Domain Transition Status Register
0x01C1 0200	0x01E2 7200	PDSTAT0	Power Domain 0 Status Register
0x01C1 0204	0x01E2 7204	PDSTAT1	Power Domain 1 Status Register
0x01C1 0300	0x01E2 7300	PDCTL0	Power Domain 0 Control Register
0x01C1 0304	0x01E2 7304	PDCTL1	Power Domain 1 Control Register
0x01C1 0400	0x01E2 7400	PDCFG0	Power Domain 0 Configuration Register
0x01C1 0404	0x01E2 7404	PDCFG1	Power Domain 1 Configuration Register
0x01C1 0800 - 0x01C1 083C	0x01E2 7800 - 0x01E2 787C	MDSTAT0-MDSTAT15 MDSTAT0-MDSTAT31	Module Status *n* Register (modules 0-15) (PSC0) Module Status *n* Register (modules 0-31) (PSC1)
0x01C1 0A00 - 0x01C1 0A3C	0x01E2 7A00 - 0x01E2 7A7C	MDCTL0-MDCTL15 MDCTL0-MDCTL31	Module Control *n* Register (modules 0-15) (PSC0) Module Control *n* Register (modules 0-31) (PSC1)

5.28.1 Power Domain and Module Topology

The device includes two PSC modules. Each PSC module consists of an Always On power domain and an additional pseudo/internal power domain that manages the sleep modes for the RAMs present in the DSP subsystem and the L3 RAM, respectively.

Each PSC module controls clock states for several of the on chip modules, controllers and interconnect components. Table 5-101 and Table 5-102 lists the set of peripherals/modules that are controlled by the PSC, the power domain they are associated with, the LPSC assignment and the default (power-on reset) module states. See the device-specific data manual for the peripherals available on a given device. The module states and terminology are defined in Section 5.28.1.2.

Table 5-101. PSC0 Default Module Configuration

LPSC Number	Module Name	Power Domain	Default Module State	Auto Sleep/Wake Only
0	EDMA3 Channel Controller	AlwaysON (PD0)	SwRstDisable	—
1	EDMA Transfer Controller 0	AlwaysON (PD0)	SwRstDisable	—
2	EDMA Transfer Controller 1	AlwaysON (PD0)	SwRstDisable	—
3	EMIFA (BR7)	AlwaysON (PD0)	SwRstDisable	—
4	SPI 0	AlwaysON (PD0)	SwRstDisable	—
5	MMC/SD 0	AlwaysON (PD0)	SwRstDisable	—
6	Arm Interrupt Controller —	AlwaysON (PD0) —	SwRstDisable —	—
7	ARM RAM/ROM —	AlwaysON (PD0) —	Enable —	Yes —
8	-	-	-	—
9	UART 0	AlwaysON (PD0)	SwRstDisable	—

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Table 5-101. PSC0 Default Module Configuration (continued)

LPSC Number	Module Name	Power Domain	Default Module State	Auto Sleep/Wake Only
10	SCR0 (Br 0, Br 1, Br 2, Br 8)	AlwaysON (PD0)	Enable	Yes
11	SCR1 (Br 4)	AlwaysON (PD0)	Enable	Yes
12	SCR2 (Br 3, Br 5, Br 6)	AlwaysON (PD0)	Enable	Yes
13	dMAX	AlwaysON (PD0)	SwRstDisable	—
14	ARM —	AlwaysON (PD0) —	SwRstDisable —	—
15	DSP	PD_DSP (PD1)	Enable	—

Table 5-102. PSC1 Default Module Configuration

LPSC Number	Module Name	Power Domain	Module State	Auto Sleep/Wake Only
0	-	—	—	—
1	USB0 (USB2.0)	AlwaysON (PD0)	SwRstDisable	—
2	USB1 (USB1.1) —	AlwaysON (PD0) —	SwRstDisable —	—
3	GPIO	AlwaysON (PD0)	SwRstDisable	—
4	UHPI	AlwaysON (PD0)	SwRstDisable	—
5	EMAC —	AlwaysON (PD0) —	SwRstDisable —	—
6	EMIFB (Br 20)	AlwaysON (PD0)	SwRstDisable	—
7	McASP0 (+ McASP0 FIFO)	AlwaysON (PD0)	SwRstDisable	—
8	McASP1 (+ McASP1 FIFO)	AlwaysON (PD0)	SwRstDisable	—
9	McASP2(+ McASP2 FIFO)	AlwaysON (PD0)	SwRstDisable	—
10	SPI 1	AlwaysON (PD0)	SwRstDisable	—
11	I2C 1	AlwaysON (PD0)	SwRstDisable	—
12	UART 1	AlwaysON (PD0)	SwRstDisable	—
13	UART 2	AlwaysON (PD0)	SwRstDisable	—
14-15 16	—	—	—	—
16	LCDC —	AlwaysON (PD0) —	SwRstDisable —	—
17	eHRPWM0/1/2	AlwaysON (PD0)	SwRstDisable	—
18-19	Not Used	—	—	—
20	ECAP0/1/2	AlwaysON (PD0)	SwRstDisable	—
21	EQEP0/1	AlwaysON (PD0)	SwRstDisable	—
22-23	-	—	—	—
24	SCR8 (Br 15)	AlwaysON (PD0)	Enable	Yes
25	SCR7 (Br 12)	AlwaysON (PD0)	Enable	Yes
26	SCR12 (Br 18)	AlwaysON (PD0)	Enable	Yes
27-30	-	—	—	—
31	Shared RAM (Br 13)	PD_SHRAM (PD1)	Enable	Yes

5.28.1.1 Power Domain States

A power domain can only be in one of the two states: ON or OFF, defined as follows:

- ON: power to the domain is on
- OFF: power to the domain is off

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In the device, for both PSC0 and PSC1, the Always ON domain, or PD0 power domain, is always in the ON state when the chip is powered-on. This domain is not programmable to OFF state.

- On PSC0 PD1/PD_DSP Domain: Controls the sleep state for DSP L1 and L2 Memories
- On PSC1 PD1/PD_SHRAM Domain: Controls the sleep state for the 128K Shared RAM

5.28.1.2 Module States

The PSC defines several possible states for a module. This states are essentially a combination of the module reset asserted or de-asserted and module clock on/enabled or off/disabled. The module states are defined in Table 5-103.

Table 5-103. Module States

Module State	Module Reset	Module Clock	Module State Definition
Enable	De-asserted	On	A module in the enable state has its module reset de-asserted and it has its clock on. This is the normal operational state for a given module
SwRstDisable	Asserted	Off	A module in the SwResetDisable state has its module reset asserted and it has its clock disabled. After initial power-on, several modules come up in the SwRstDisable state. Generally, software is not expected to initiate this state

5.29 Emulation Logic

This section describes the steps to use a third party debugger. The debug capabilities and features for DSP and ARM are as shown below.

For TI's latest debug and emulation information see :

http://tiexpressdsp.com/wiki/index.php?title=Category:Emulation

DSP:

- Basic Debug
  - Execution Control
  - System Visibility
- Real-Time Debug
  - Interrupts serviced while halted
  - Low/non-intrusive system visibility while running
- Advanced Debug
  - Global Start
  - Global Stop
  - Specify targeted memory level(s) during memory accesses
  - HSRTDX (High Speed Real Time Data eXchange)
- Advanced System Control
  - Subsystem reset via debug
  - Peripheral notification of debug events
  - Cache-coherent debug accesses
- Security
  - Configurable levels of security and debug visibility
  - Halting on a security violation
  - Debug halts prevented during secure code execution
  - Memory accesses prevented to secure memory

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- Analysis Actions
  - Stop program execution
  - Generate debug interrupt
  - Benchmarking with counters
  - External trigger generation
  - Debug state machine state transition
  - Combinational and Sequential event generation
- Analysis Events
  - Program event detection
  - Data event detection
  - External trigger Detection
  - System event detection (i.e. cache miss)
  - Debug state machine state detection
- Analysis Configuration
  - Application access
  - Debugger access

Table 5-104. DSP Debug Features

Category	Hardware Feature	Availability
Basic Debug	Software breakpoint	Unlimited
	Hardware breakpoint	Up to 10 HWBPs, including: 4 precise (1) HWBPs inside DSP core and one of them is associated with a counter. 2 imprecise (1) HWBPs from AET. 4 imprecise (1) HWBPs from AET which are shared for watch point.
Analysis	Watch point	Up to 4 watch points, which are shared with HWBPs, and can also be used as 2 watch points with data (32 bits)
	Watch point with Data	Up to 2, Which can also be used as 4 watch points.
	Counters/timers	1x64-bits (cycle only) + 2x32-bits (water marke counters)
	External Event Trigger In	1
	External Event Trigger Out	1

(1) Precise hardware breakpoints will halt the processor immediately prior to the execution of the selected instruction. Imprecise breakpoints will halt the processor some number of cycles after the selected instruction depending on device conditions.

ARM:

- Basic Debug
  - Execution Control
  - System Visibility
- Advanced Debug
  - Global Start
  - Global Stop
- Advanced System Control
  - Subsystem reset via debug
  - Peripheral notification of debug events
  - Cache-coherent debug accesses

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- Security
  - Halting on a security violation (by cross-triggering via INTC)
  - Memory accesses prevented to secure memory (this is ensured by system level security mechanism)
- Program Trace
  - Program flow corruption
  - Code coverage
  - Path coverage
  - Thread/interrupt synchronization problems
- Data Trace
  - Memory corruption
- Timing Trace
  - Profiling
- Analysis Actions
  - Stop program execution
  - Control trace streams
  - Generate debug interrupt
  - Benchmarking with counters
  - External trigger generation
  - Debug state machine state transition
  - Combinational and Sequential event generation
- Analysis Events
  - Program event detection
  - Data event detection
  - External trigger Detection
  - System event detection (i.e. cache miss)
  - Debug state machine state detection
- Analysis Configuration
  - Application access
  - Debugger access

Table 5-105. ARM Debug Features

Category	Hardware Feature	Availability
Basic Debug	Software breakpoint	Unlimited
	Hardware breakpoint	Up to 14 HWBPs, including: 2 precise (1) HWBP inside ARM core which are shared with watch points. 8 imprecise (1) HWBPs from ETM's address comparators, which are shared with trace function, and can be used as watch point too. 4 imprecise (1) HWBPs from ICECrusher.

(1) Precise hardware breakpoints will halt the processor immediately prior to the execution of the selected instruction. Imprecise breakpoints will halt the processor some number of cycles after the selected instruction depending on device conditions.

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Table 5-105. ARM Debug Features (continued)

Category	Hardware Feature	Availability
Analysis	Watch point	Up to 6 watch points, including: 2 from ARM core which is shared with HWBPs and can be associated with a data. 8 from ETM's address comparators, which are shared with trace function, and HWBPs.
	Watch point with Data	2 from ARM core which is shared with HWBPs. 8 watch points from ETM can be associated with a data comparator, and ETM has total 4 data comparators.
	Counters/timers	3x32-bit (1 cycle ; 2 event)
	External Event Trigger In	1
	External Event Trigger Out	1
	Internal Cross-Triggering Signals	One between ARM and DSP
Trace Control	Address range for trace	4
	Data qualification for trace	2
	System events for trace control	20
	Counters/Timers for trace control	2x16-bit
	State Machines/Sequencers	1x3-State State Machine
	Context/Thread ID Comparator	1
	Independent trigger control units	12
On-chip Trace Capture	Capture depth PC	4k bytes ETB
	Capture depth PC + Timing	4k bytes ETB
	Application accessible	Y

5.29.1 JTAG Port Description

The target debug interface uses the five standard IEEE 1149.1(JTAG) signals ($\overline{\text{TRST}}$, TCK, TMS, TDI, and TDO), a return clock (RTCK) due to the clocking requirements of the ARM926EJ-S and EMU0.

$\overline{\text{TRST}}$ holds the debug and boundary scan logic in reset (normal DSP operation) when pulled low (its default state). Since $\overline{\text{TRST}}$ has an internal pull-down resistor, this ensures that at power up the device functions in its normal (non-test) operation mode if $\overline{\text{TRST}}$ is not connected. Otherwise, $\overline{\text{TRST}}$ should be driven inactive by the emulator or boundary scan controller. Boundary scan test cannot be performed while the $\overline{\text{TRST}}$ pin is pulled low.

Table 5-106. JTAG Port Description

PIN	TYPE	NAME	DESCRIPTION
$\overline{\text{TRST}}$	I	Test Logic Reset	When asserted (active low) causes all test and debug logic in OMAPL137 to be reset along with the IEEE 1149.1 interface
TCK	I	Test Clock	This is the test clock used to drive an IEEE 1149.1 TAP state machine and logic. Depending on the emulator attached to OMAPL137, this is a free running clock or a gated clock depending on RTCK monitoring.
RTCK	O	Returned Test Clock	Synchronized TCK. Depending on the emulator attached to OMAPL137, the JTAG signals are clocked from RTCK or RTCK is monitored by the emulator to gate TCK.
TMS	I	Test Mode Select	Directs the next state of the IEEE 1149.1 test access port state machine
TDI	I	Test Data Input	Scan data input to the device
TDO	O	Test Data Output	Scan data output of the device
EMU0	I/O	Emulation 0	Channel 0 trigger + HSRTDX

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5.29.2 Scan Chain Configuration Parameters

Table 5-107 shows the TAP configuration details required to configure the router/emulator for this device.

Table 5-107. JTAG Port Description

Router Port ID	Default TAP	TAP Name	Tap IR Length
17	No	C674x	38
18	No	ARM926	4
19	No	ETB	4

The router is ICEpick revision C and has a 6-bit IR length.

5.29.3 Initial Scan Chain Configuration

The first level of debug interface that sees the scan controller is the TAP router module. The debugger can configure the TAP router for serially linking up to 16 TAP controllers or individually scanning one of the TAP controllers without disrupting the IR state of the other TAPs.

5.29.3.1 Adding TAPS to the Scan Chain

A Power-On Reset (POR) or the JTAG Test-Logic Reset state configures the TAP router to contain only the router's TAP.

The TAP router must be programmed to add additional TAPs to the scan chain. The following JTAG scans must be completed to add the ARM926EJ-S to the scan chain.

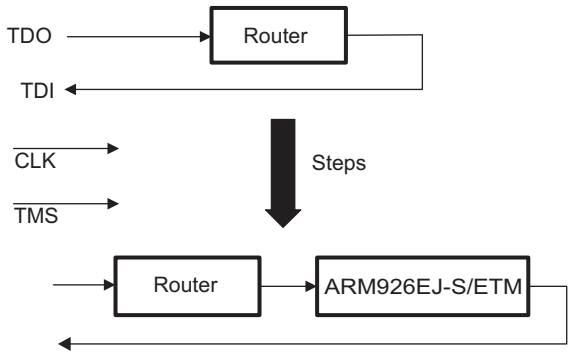

Figure 5-69. Adding ARM926EJ-S to the scan chain

Pre-amble: The device whose data reaches the emulator first is listed first in the board configuration file. This device is a pre-amble for all the other devices. This device has the lowest device ID.

Post-amble: The device whose data reaches the emulator last is listed last in the board configuration file. This device is a post-amble for all the other devices. This device has the highest device ID.

- Function : Update the JTAG preamble and post-amble counts.
  - Parameter : The IR pre-amble count is '0'.
  - Parameter : The IR post-amble count is '0'.
  - Parameter : The DR pre-amble count is '0'.
  - Parameter : The DR post-amble count is '0'.
  - Parameter : The IR main count is '6'.
  - Parameter : The DR main count is '1'.

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- Function : Do a send-only JTAG IR/DR scan.
  - Parameter : The route to JTAG shift state is 'shortest transition'.
  - Parameter : The JTAG shift state is 'shift-ir'.
  - Parameter : The JTAG destination state is 'pause-ir'.
  - Parameter : The bit length of the command is '6'.
  - Parameter : The send data value is '0x00000007'.
  - Parameter : The actual receive data is 'discarded'.
- Function : Do a send-only JTAG IR/DR scan.
  - Parameter : The route to JTAG shift state is 'shortest transition'.
  - Parameter : The JTAG shift state is 'shift-dr'.
  - Parameter : The JTAG destination state is 'pause-dr'.
  - Parameter : The bit length of the command is '8'.
  - Parameter : The send data value is '0x00000089'.
  - Parameter : The actual receive data is 'discarded'.
- Function : Do a send-only JTAG IR/DR scan.
  - Parameter : The route to JTAG shift state is 'shortest transition'.
  - Parameter : The JTAG shift state is 'shift-ir'.
  - Parameter : The JTAG destination state is 'pause-ir'.
  - Parameter : The bit length of the command is '6'.
  - Parameter : The send data value is '0x00000002'.
  - Parameter : The actual receive data is 'discarded'.
- Function : Embed the port address in next command.
  - Parameter : The port address field is '0x0f000000'.
  - Parameter : The port address value is '3'.
- Function : Do a send-only JTAG IR/DR scan.
  - Parameter : The route to JTAG shift state is 'shortest transition'.
  - Parameter : The JTAG shift state is 'shift-dr'.
  - Parameter : The JTAG destination state is 'pause-dr'.
  - Parameter : The bit length of the command is '32'.
  - Parameter : The send data value is '0xa2002108'.
  - Parameter : The actual receive data is 'discarded'.
- Function : Do a send-only all-ones JTAG IR/DR scan.
  - Parameter : The JTAG shift state is 'shift-ir'.
  - Parameter : The JTAG destination state is 'run-test/idle'.
  - Parameter : The bit length of the command is '6'.
  - Parameter : The send data value is 'all-ones'.
  - Parameter : The actual receive data is 'discarded'.
- Function : Wait for a minimum number of TCLK pulses.
  - Parameter : The count of TCLK pulses is '10'.
- Function : Update the JTAG preamble and post-amble counts.
  - Parameter : The IR pre-amble count is '0'.
  - Parameter : The IR post-amble count is '6'.
  - Parameter : The DR pre-amble count is '0'.
  - Parameter : The DR post-amble count is '1'.
  - Parameter : The IR main count is '4'.
  - Parameter : The DR main count is '1'.

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The initial scan chain contains only the TAP router module. The following steps must be completed in order to add ETB TAP to the scan chain.

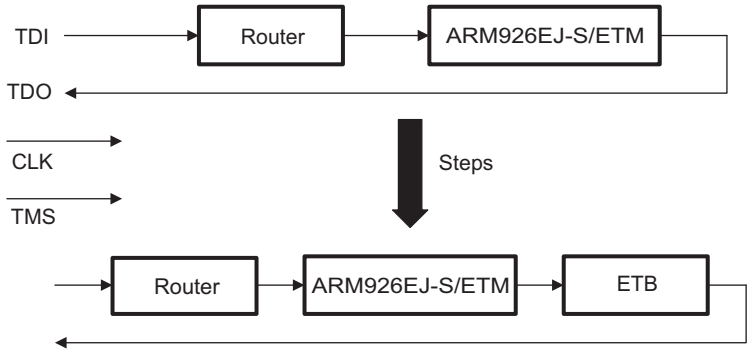

Figure 5-70. Adding ETB to the scan chain

- Function : Do a send-only JTAG IR/DR scan.
  - Parameter : The route to JTAG shift state is 'shortest transition'.
  - Parameter : The JTAG shift state is 'shift-ir'.
  - Parameter : The JTAG destination state is 'pause-ir'.
  - Parameter : The bit length of the command is '6'.
  - Parameter : The send data value is '0x00000007'.
  - Parameter : The actual receive data is 'discarded'.
- Function : Do a send-only JTAG IR/DR scan.
  - Parameter : The route to JTAG shift state is 'shortest transition'.
  - Parameter : The JTAG shift state is 'shift-dr'.
  - Parameter : The JTAG destination state is 'pause-dr'.
  - Parameter : The bit length of the command is '8'.
  - Parameter : The send data value is '0x00000089'.
  - Parameter : The actual receive data is 'discarded'.
- Function : Do a send-only JTAG IR/DR scan.
  - Parameter : The route to JTAG shift state is 'shortest transition'.
  - Parameter : The JTAG shift state is 'shift-ir'.
  - Parameter : The JTAG destination state is 'pause-ir'.
  - Parameter : The bit length of the command is '6'.
  - Parameter : The send data value is '0x00000002'.
  - Parameter : The actual receive data is 'discarded'.
- Function : Embed the port address in next command.
  - Parameter : The port address field is '0x0f000000'.
  - Parameter : The port address value is '3'.
- Function : Do a send-only JTAG IR/DR scan.
  - Parameter : The route to JTAG shift state is 'shortest transition'.
  - Parameter : The JTAG shift state is 'shift-dr'.
  - Parameter : The JTAG destination state is 'pause-dr'.
  - Parameter : The bit length of the command is '32'.
  - Parameter : The send data value is '0xa3302108'.
  - Parameter : The actual receive data is 'discarded'.

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- Function : Do a send-only all-ones JTAG IR/DR scan.
  - Parameter : The JTAG shift state is 'shift-ir'.
  - Parameter : The JTAG destination state is 'run-test/idle'.
  - Parameter : The bit length of the command is '6'.
  - Parameter : The send data value is 'all-ones'.
  - Parameter : The actual receive data is 'discarded'.
- Function : Wait for a minimum number of TCLK pulses.
  - Parameter : The count of TCLK pulses is '10'.
- Function : Update the JTAG preamble and post-amble counts.
  - Parameter : The IR pre-amble count is '0'.
  - Parameter : The IR post-amble count is '6 + 4'.
  - Parameter : The DR pre-amble count is '0'.
  - Parameter : The DR post-amble count is '1 + 1'.
  - Parameter : The IR main count is '4'.
  - Parameter : The DR main count is '1'.

5.29.4 JTAG 1149.1 Boundary Scan Considerations

To use boundary scan, the following sequence should be followed:

- Execute a valid reset sequence and exit reset
- Wait at least 6000 OSCIN clock cycles
- Enter boundary scan mode using the JTAG pins

No specific value is required on the EMU0 pin for boundary scan testing. If TRST is not driven by the boundary scan tool or tester, TRST should be externally pulled high during boundary scan testing.

5.30 Real Time Clock (RTC)

The RTC provides a time reference to an application running on the device. The current date and time is tracked in a set of counter registers that update once per second. The time can be represented in 12-hour or 24-hour mode. The calendar and time registers are buffered during reads and writes so that updates do not interfere with the accuracy of the time and date.

Alarms are available to interrupt the CPU at a particular time, or at periodic time intervals, such as once per minute or once per day. In addition, the RTC can interrupt the CPU every time the calendar and time registers are updated, or at programmable periodic intervals.

The real-time clock (RTC) provides the following features:

- 100-year calendar (xx00 to xx99)
- Counts seconds, minutes, hours, day of the week, date, month, and year with leap year compensation
- Binary-coded-decimal (BCD) representation of time, calendar, and alarm
- 12-hour clock mode (with AM and PM) or 24-hour clock mode
- Alarm interrupt
- Periodic interrupt
- Single interrupt to the CPU
- Supports external 32.768-kHz crystal or external clock source of the same frequency
- Separate isolated power supply

Figure 5-71 shows a block diagram of the RTC. See the *TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.* – Literature Number SPRUFK9 for more details.

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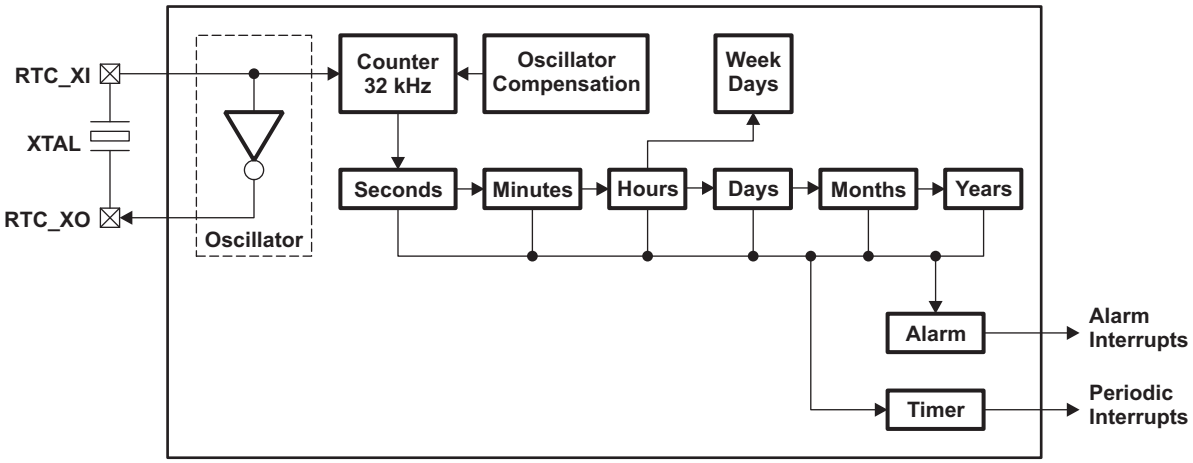


Figure 5-71. Real-Time Clock Block Diagram

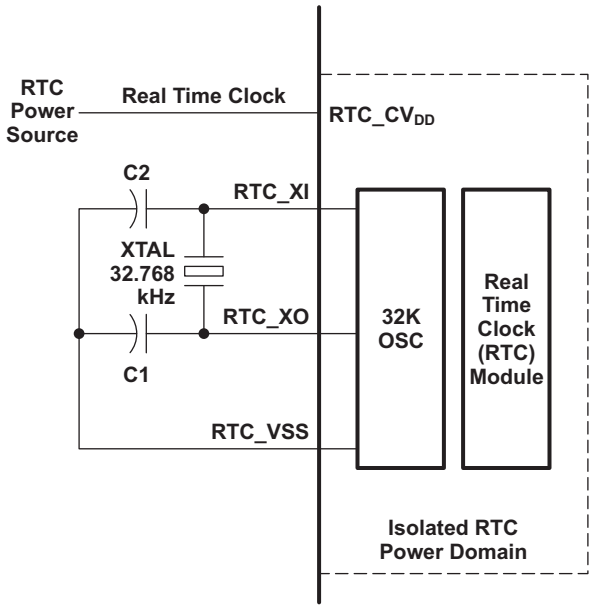
5.30.1 Clock Source

The clock reference for the RTC is an external 32.768-kHz crystal or an external clock source of the same frequency. The RTC also has a separate power supply that is isolated from the rest of the system. When the CPU and other peripherals are without power, the RTC can remain powered to preserve the current time and calendar information.

The source for the RTC reference clock may be provided by a crystal or by an external clock source. The RTC has an internal oscillator buffer to support direct operation with a crystal. The crystal is connected between pins RTC_XI and RTC_XO. RTC_XI is the input to the on-chip oscillator and RTC_XO is the output from the oscillator back to the crystal. A crystal with 70k-ohm max ESR is recommended. Typical C1, C2 values are 10-20 pF.

An external 32.768-kHz clock source may be used instead of a crystal. In such a case, the clock source is connected to RTC_XI, and RTC_XO is left unconnected.

If the RTC is not used, the RTC_XI pin should be held high and RTC_XO should be left unconnected.



The oscillator performance is validated up to 125°C, operating above 125°C is recommended to be driven with an external clock source.

Figure 5-72. Clock Source

5.30.2 Registers

Table 5-108 lists the memory-mapped registers for the RTC. See the device-specific data manual for the memory address of these registers.

Table 5-108. Real-Time Clock (RTC) Registers

BYTE ADDRESS	Acronym	Register Description
0x01C2 3000	SECOND	Seconds Register
0x01C2 3004	MINUTE	Minutes Register
0x01C2 3008	HOUR	Hours Register
0x01C2 300C	DAY	Day of the Month Register
0x01C2 3010	MONTH	Month Register
0x01C2 3014	YEAR	Year Register
0x01C2 3018	DOTW	Day of the Week Register
0x01C2 3020	ALARMSECOND	Alarm Seconds Register
0x01C2 3024	ALARMMINUTE	Alarm Minutes Register
0x01C2 3028	ALARMHOUR	Alarm Hours Register
0x01C2 302C	ALARMDAY	Alarm Days Register
0x01C2 3030	ALARMMONTH	Alarm Months Register
0x01C2 3034	ALARMYEAR	Alarm Years Register
0x01C2 3040	CTRL	Control Register
0x01C2 3044	STATUS	Status Register
0x01C2 3048	INTERRUPT	Interrupt Enable Register
0x01C2 304C	COMPLSB	Compensation (LSB) Register
0x01C2 3050	COMPMSB	Compensation (MSB) Register
0x01C2 3054	OSC	Oscillator Register
0x01C2 3060	SCRATCH0	Scratch 0 (General-Purpose) Register
0x01C2 3064	SCRATCH1	Scratch 1 (General-Purpose) Register
0x01C2 3068	SCRATCH2	Scratch 2 (General-Purpose) Register
0x01C2 306C	KICK0	Kick 0 (Write Protect) Register
0x01C2 3070	KICK1	Kick 1 (Write Protect) Register

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6 Device and Document Support

6.1 Device Support

TI offers an extensive line of development tools for the OMAPL137 platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of applications:

Software Development Tools:

Code Composer Studio™ Integrated Development Environment (IDE): including Editor

C/C++/Assembly Code Generation, and Debug plus additional development tools

Scalable, Real-Time Foundation Software (DSP/BIOS™), which provides the basic run-time target software needed to support any application.

Hardware Development Tools:

Extended Development System (XDS™) Emulator

For a complete listing of development-support tools for OMAPL137 , visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com uniform resource locator (URL). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

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6.2 Documentation Support

The following documents describe the Applications Processor. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

DSP Reference Guides

SPRUG82 ***TMS320C674x DSP Cache User's Guide.*** Explains the fundamentals of memory caches and describes how the two-level cache-based internal memory architecture in the TMS320C674x digital signal processor (DSP) can be efficiently used in DSP applications. Shows how to maintain coherence with external memory, how to use DMA to reduce memory latencies, and how to optimize your code to improve cache efficiency. The internal memory architecture in the C674x DSP is organized in a two-level hierarchy consisting of a dedicated program cache (L1P) and a dedicated data cache (L1D) on the first level. Accesses by the CPU to the these first level caches can complete without CPU pipeline stalls. If the data requested by the CPU is not contained in cache, it is fetched from the next lower memory level, L2 or external memory.

SPRUFE8 ***TMS320C674x DSP CPU and Instruction Set Reference Guide.*** Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C674x digital signal processors (DSPs). The C674x DSP is an enhancement of the C64x+ and C67x+ DSPs with added functionality and an expanded instruction set.

SPRU186 ***TMS320C6000 Assembly Language Tools User's Guide.***Describes the assembly language tools (assembler, linker, and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C6000 platform of devices (including the C64x+, C67x+, and C674x generations).

SPRU187 ***TMS320C6000 Optimizing Compiler User's Guide.*** Describes the TMS320C6000 C compiler and the assembly optimizer. This C compiler accepts ANSI standard C source code and produces assembly language source code for the TMS320C6000 platform of devices (including the C64x+, C67x+, and C674x generations). The assembly optimizer helps you optimize your assembly code.

SPRUG83 ***TMS320OMAPL137 Digital Audio Processor System Reference Guide***. Describes the ARM subsystem, DSP subsystem, system memory, device clocking, phase-locked loop controller (PLLC), power and sleep controller (PSC), power management, ARM interrupt controller (AINTC), and system configuration module.

SPRUFK5 ***TMS320C674x DSP Megamodule Reference Guide.*** Describes the TMS320C674x digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

SPRUFK9 ***TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.*** Provides an overview and briefly describes the peripherals available on the device.

SPRUG84 ***OMAP-L137 Applications Processor System Reference Guide*** System-on-Chip (SoC) including the ARM subsystem, DSP subsystem, system memory, device clocking, phase-locked loop controller (PLLC), power and sleep controller (PSC), power management, ARM interrupt controller (AINTC), and system configuration module.

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7 Mechanical Packaging and Orderable Information

This section describes the device orderable part numbers, packaging options, materials, thermal and mechanical parameters.

7.1 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., TMS320C6745). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: X, P or NULL (e.g., XOMAPL137). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications.

P Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

NULL Fully-qualified production device.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Null devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ZBK), the temperature range (for example, "Blank" is the commercial temperature range), and the device speed range in megahertz (for example, "Blank" is the default).

Figure 7-1 provides a legend for reading the complete device name for any OMAPL13x member.

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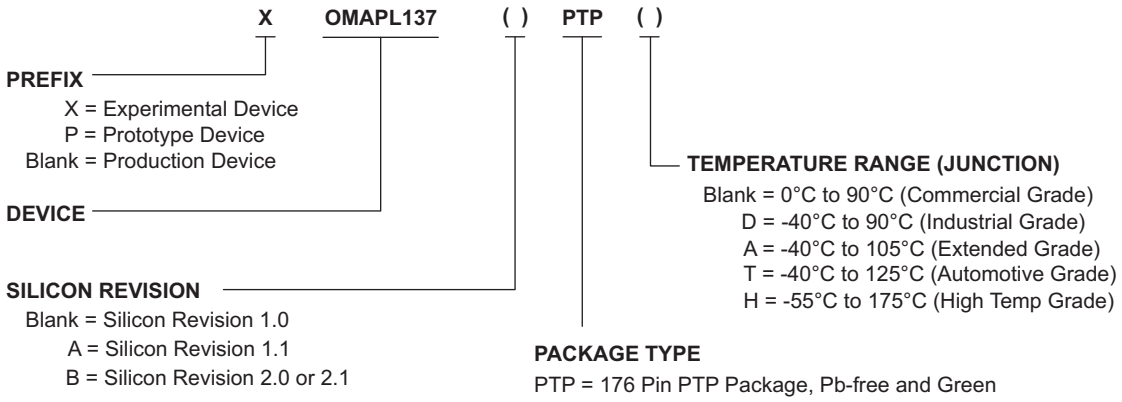

Figure 7-1. Device Nomenclature (PTP Package)

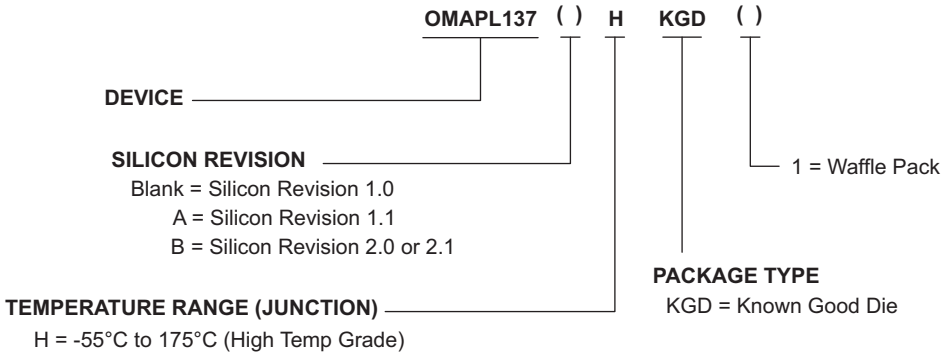

Figure 7-2. Device Nomenclature (KGD Package)

7.2 Packaging Materials Information

The 176-pin PTP package is lead-free (Pb-free) and green. "Lead-free" and "green" are defined as follows:

- **Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

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7.3 Thermal Data for PTP

The following table(s) show the thermal resistance characteristics for the PowerPAD™ PTP mechanical package.

Table 7-1. Thermal Resistance Characteristics (PowerPAD™ Package) [PTP]

NO.			°C/W
1	$R\Theta_{JCTOP}$	Junction-to-case top	9.3
2	$R\Theta_{JB}$	Junction-to-board	10.3
3	$R\Theta_{JA}$	Junction-to-free air	26.5
4	$R\Theta_{JCBOT}$	Junction-to-case bottom	0.2
5	Psi_{JT}	Junction-to-package top	0.4
6	Psi_{JB}	Junction-to-board	10.1

7.4 Supplementary Information About the 176-pin PTP PowerPAD™ Package

This section highlights a few important details about the 176-pin PTP PowerPAD™ package. Texas Instruments' PowerPAD Thermally Enhanced Package Technical Brief (literature number SLMA002) should be consulted when creating a PCB footprint for this device.

7.4.1 Standoff Height

As illustrated in Figure 7-3, the standoff height specification for this device (between 0.050 mm and 0.150 mm) is measured from the seating plane established by the three lowest package pins to the **lowest** point on the package body. Due to warpage, the lowest point on the package body is located in the center of the package at the exposed thermal pad.

Using this definition of standoff height provides the correct result for determining the correct solder paste thickness. According to TI's PowerPAD Thermally Enhanced Package Technical Brief (literature number SLMA002), the recommended range of solder paste thickness for this package is between 0.152 mm and 0.178 mm.

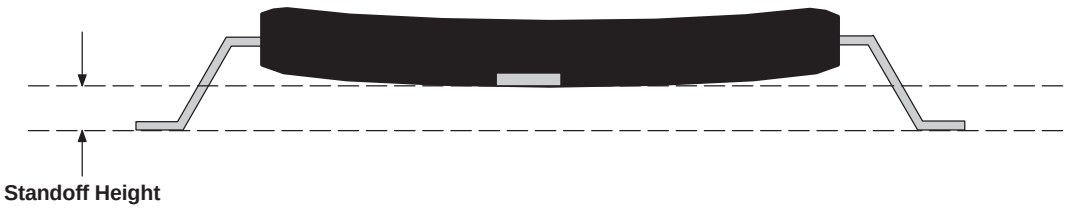

Figure 7-3. Standoff Height Measurement on 176-pin PTP Package

7.4.2 PowerPAD™ PCB Footprint

In general, for proper thermal performance, the thermal pad under the package body should be as large as possible. However, the soldermask opening for the PowerPAD™ should be sized to match the pad size on the 176-pin PTP package; as illustrated in Figure 7-4.

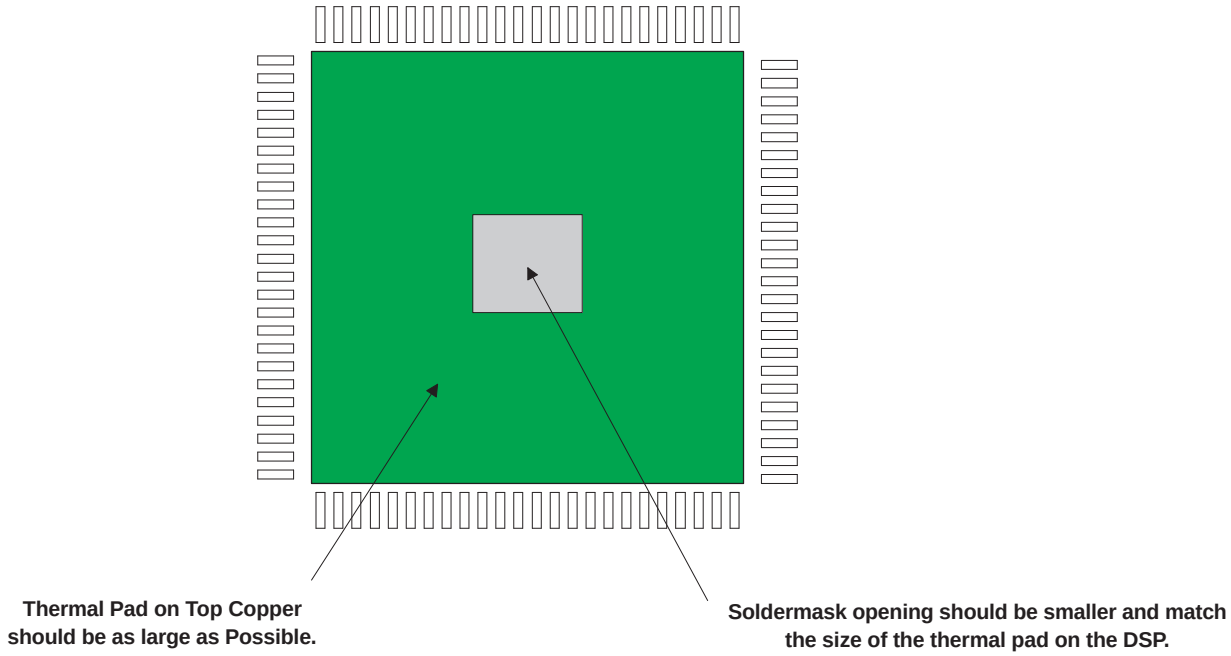

Figure 7-4. Soldermask Opening Should Match Size of DSP Thermal Pad

7.5 Packaging Information

Table 7-2. Orderable Part Numbers

ORDERABLE PART NUMBER	PACKAGE	CPU SPEED	EMIFB SDRAM SPEED	CORE SUPPLY	I/O SUPPLY	OPERATING JUNCTION TEMPERATURE RANGE
OMAPL137BPTPH	176 PTP	300 MHz	133 MHz	1.2 V	3.3 V	-55°C to 175°C
OMAPL137BHKGD1	KGD die	300 MHz	133 MHz	1.2 V	3.3 V	-55°C to 175°C

7.6 Mechanical Drawings

This section contains the detailed mechanical drawing for the PTP PowerPAD™ plastic quad flat pack package. Additionally, a detailed drawing of the actual thermal pad dimensions as well as a recommended PCB footprint are provided.

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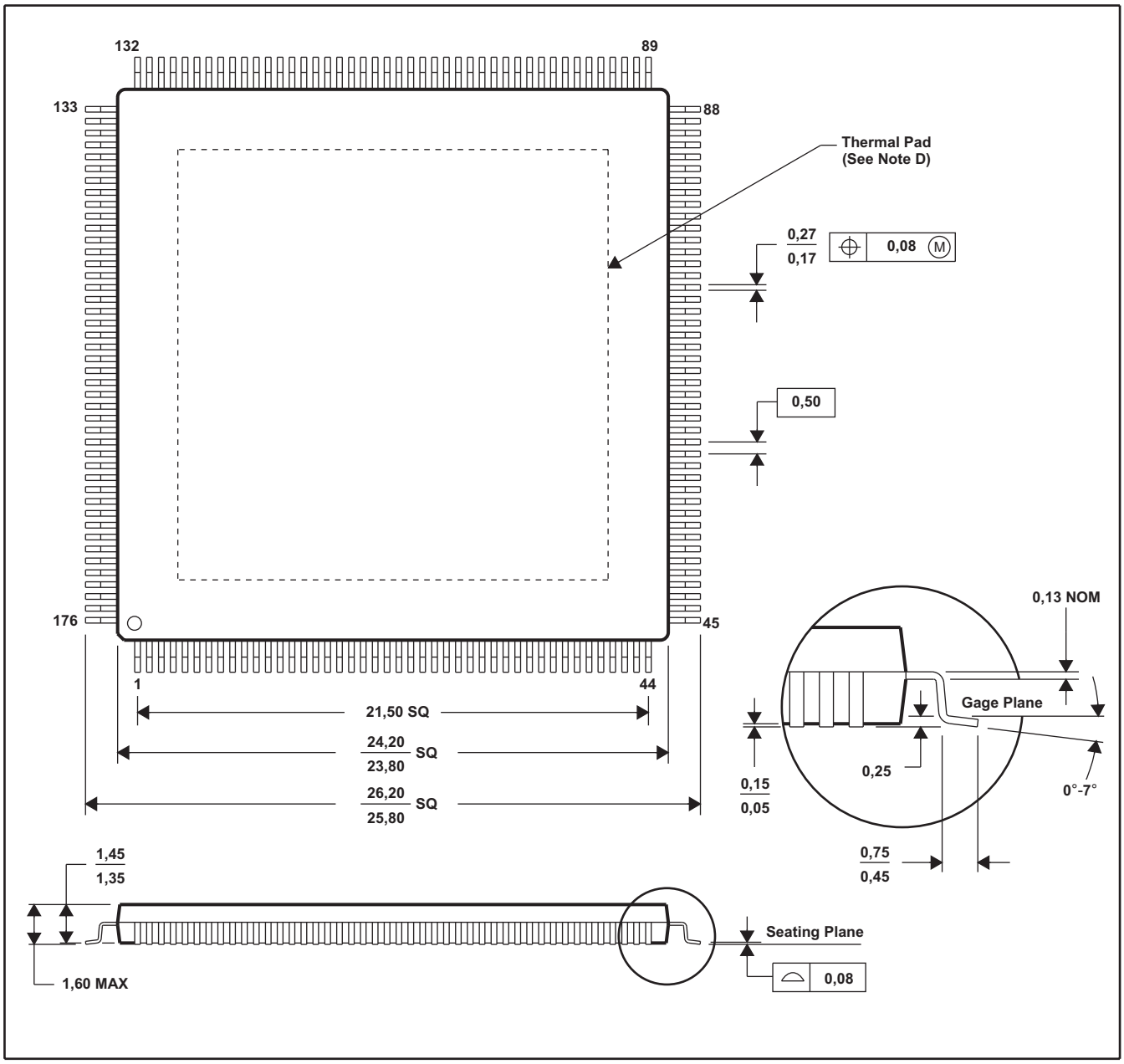
7.6.1 PTP (S-PQFP-G176)

PTP (S-PQFP-G176) PowerPAD™ PLASTIC QUAD



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package. Texas Instruments Literature No. SLMA002 for information regarding recommened board layout. This documrnt is available at <http://www.ti.com>.
E. Falls within JEDEC MS-026

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7.7 dMAX

Table 7-3 lists the dMAX control registers.

Table 7-3. dMAX Control Registers

Register Address		dMAX Register Name	Register Description
6000 0008h		DEPR	The dMAX event polarity register (DEPR) controls the polarity-rising edge (low to high) or falling edge (high to low)-that sets the flag in the EFR register.
6000 000Ch		DEER	The events can be enabled by writing a 1 to dMAX Event Enable Register (DEER).
6000 0010h		DEDR	The events can be disabled by writing a 1 to dMAX Event Disable Register (DEDR).
6000 0014h		DEHPR	An event is assigned to the high priority event group when the bit, which corresponds to the event, is set in the dMAX Event High Priority Register (DEHPR).
6000 0018h		DELPR	An event is assigned to the low priority event group when the bit, which corresponds to the event, is set in the dMAX Event Low Priority Register (DELPR).
6000 001Ch		DEFR	The dMAX Event Flag Register (DEFR) indicates that an appropriate transition edge (specified in the Event Polarity Register) has occurred on the event signals. All events are captured in the event flag register, even when the events are disabled.
6000 0034h		DER0	The dMAX event register (DER0) reflects current value of the event signals 7-0.
6000 0054h		DER1	The dMAX event register (DER1) reflects current value of the event signals 15-8.
6000 0074h		DER2	The dMAX event register (DER2) reflects current value of the event signals 23-16.
6000 0094h		DER3	The dMAX event register (DER3) reflects current value of the event signals 31-24.
6000 0040h		DFSR0	dMAX FIFO status register 0. Writing a 1 to the DFSR0 register clears the corresponding bit. Writing 0 has no effect.
6000 0060h		DFSR1	dMAX FIFO status register 1. Writing a 1 to the DFSR1 register clears the corresponding bit. Writing 0 has no effect.
6000 0080h		DTCR0	dMAX transfer completion register 0. Writing a 1 to the DTCR0 register clears the corresponding bit. Writing 0 has no effect.
6000 00A0h		DTCR1	dMAX transfer completion register 1. Writing a 1 to the DTCR1 register clears the corresponding bit. Writing 0 has no effect.
-		DETR	dMAX event trigger register. By toggling a bit in this register the CPU can trigger an event. To facilitate faster CPU access, the dMAX Event Trigger Register is not memory-mapped and is placed inside the CPU module.
-		DESR	dMAX event status register. To facilitate low CPU access overhead this register mirrors TCC bits from DTCR0 and DTCR1 registers. The register also keeps track of dMAX controller activity. To facilitate faster CPU access, the dMAX Event Status Register is not memory-mapped and is placed inside the CPU module.

7.8 Key Manager

The Key Manager provides the management of the security keys within the Security Architecture. Its goal as part of the architecture is to provide protection of keys / key information (known from this point on as Keys) against unintended users.The following features are supported by the Key Manager:

- Controls the system level security key information
- Supports a configurable number of 128-bit security keys and 16-bit key checksums (up to 16)
- EFUSE scan chain snooping capabilities
  - Device Type capture
  - Security Key checksum validation

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- Read only VBUSP slave port for register access
  - Access controls for security key information
    - Configurable mstid and privid filter
    - Support for CBA memory protection sideband signals (secure, priv, privid, emudbg)
  - Clock management interface
- Interaction with system level Security controller

Table 7-4. Key Manager Register Descriptions

BYTE ADDRESS	REGISTER NAME	DESCRIPTION
01xC1 2000	REVID	Revision Register
01xC1 2004	STAT	Key Manager Status
01xC1 2008	CHKSUMSTAT	Key Checksum Status
01xC1 200C	RSVD	Reserved
01xC1 2010 - 01xC1 201C	KEY1WRD1	Key 1
01xC1 2020 - 01xC1 202C	KEY1WRD1	Key 2
...	...	...
01xC1 20F0 - 01xC1 20FC	KEY1WRD1	Key 15
01xC1 2100 - 01xC1 210C	KEY1WRD1	Key 16
01xC1 2110 - 01xC1 23FF	RSVD	Reserved

7.9 SECCTRL

Table 7-5. SECCTRL Register Descriptions

BYTE ADDRESS	REGISTER NAME	DESCRIPTION
01xC1 3000	PID	
	RSVD	Reserved
	SYSSTATUS	
	SYSWR	
	RSVD	Reserved
	ARMWR	
	SYSCONTROL	
	SYSCONTROLPROTECT	
	SYSTAPEN	
	SECRESERVED	
	PSTATUS	
	PREADDEBUGDAT	
	PWRITEDEBUGDAT	

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2012) to Revision B	Page
• Added bare die information and bond pad coordinates for Known Good Die (KGD)	21
• Added N/C to blank descriptions in Table 2-4	22
• Deleted : Murata BLM31PG500SN1L or Equivalent from Figure 5-9	56
• Added device nomenclature for KGD	194
• Added orderable part number for KGD	196

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OMAPL137BHKGD1	ACTIVE	XCEPT	KGD	0	35	TBD	Call TI	N / A for Pkg Type			Samples
OMAPL137BPTPH	ACTIVE	HLQFP	PTP	176	1	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR		OMAPL137BPTPH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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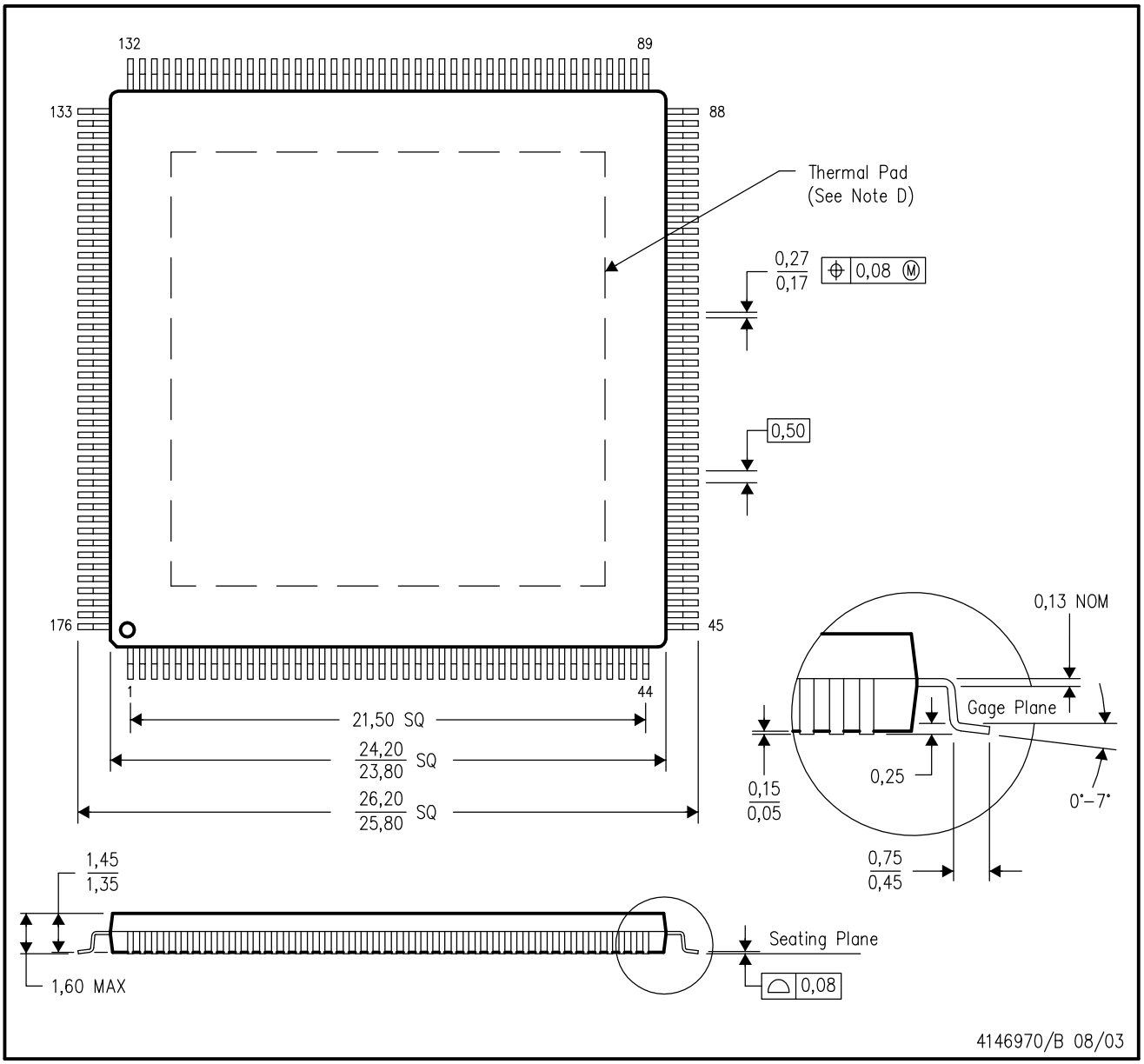
PTP (S–PQFP–G176) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–026

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THERMAL PAD MECHANICAL DATA

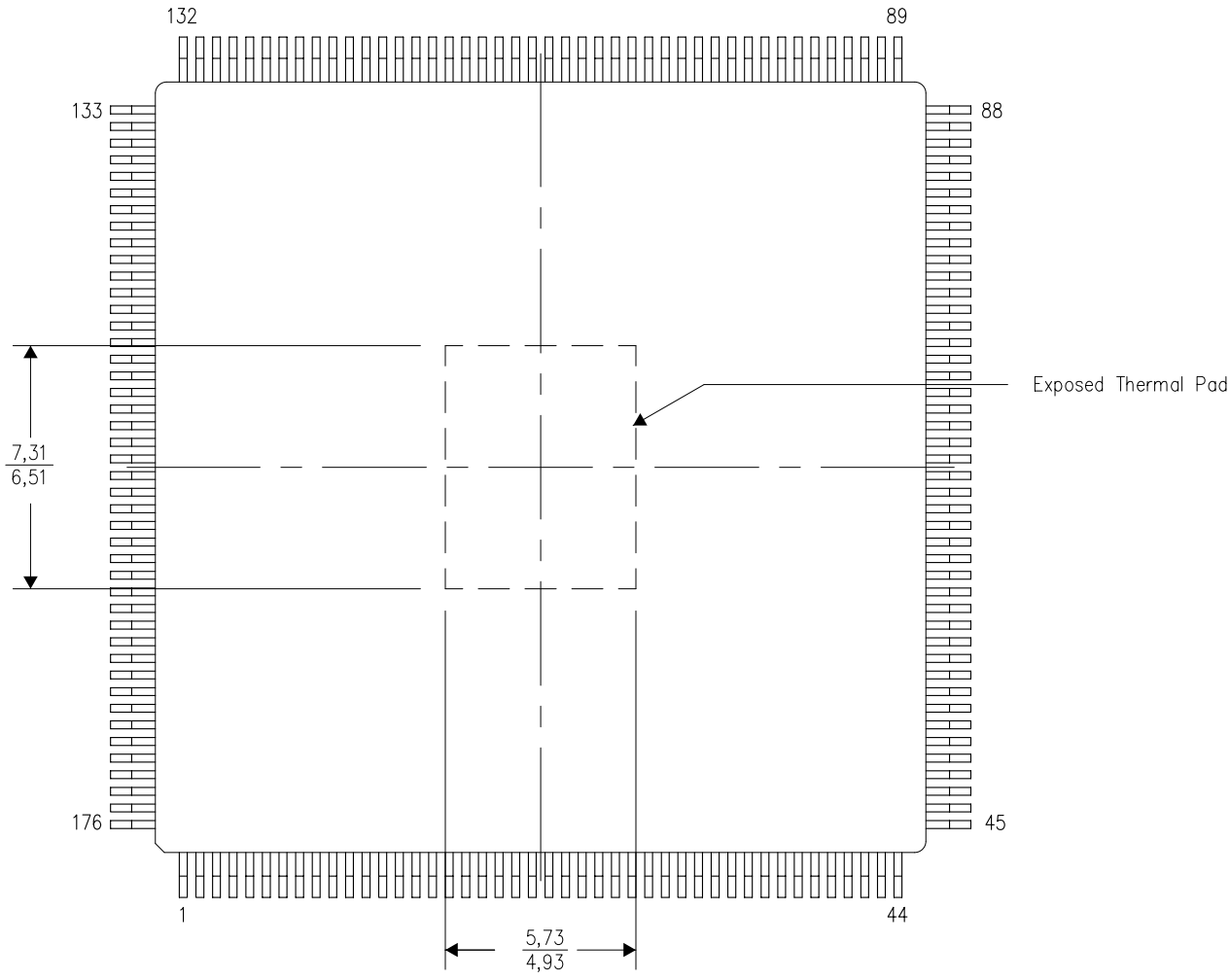
PTP (S–PQFP–G176)

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

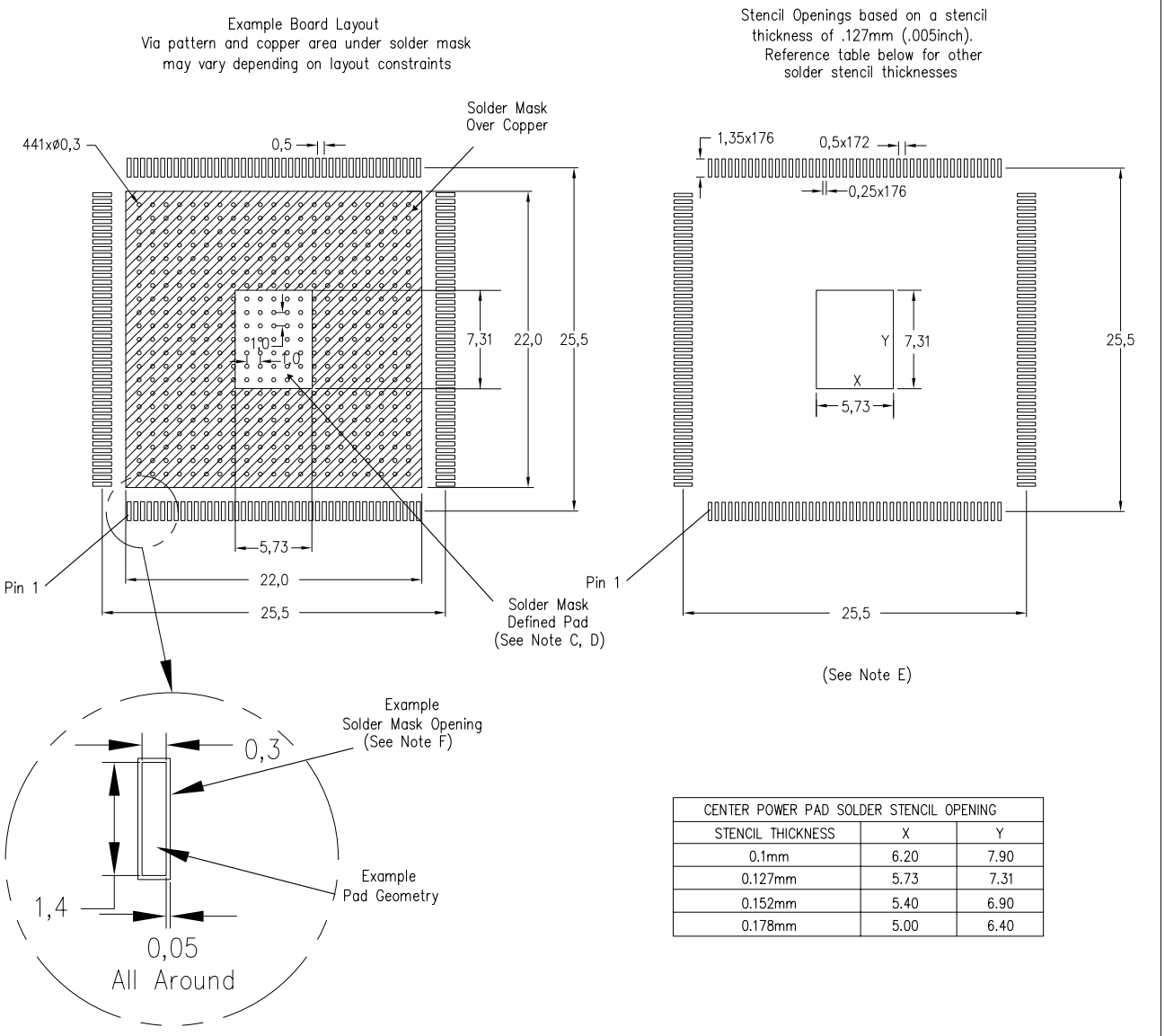


NOTE: All linear dimensions are in millimeters

Top View

Exposed Thermal Pad Dimensions

PTP (S–PQFP–G176) PowerPAD™ PLASTIC QUAD FLATPACK



CENTER POWER PAD SOLDER STENCIL OPENING		
STENCIL THICKNESS	X	Y
0.1mm	6.20	7.90
0.127mm	5.73	7.31
0.152mm	5.40	6.90
0.178mm	5.00	6.40

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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RFID	www.ti-rfid.com		
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