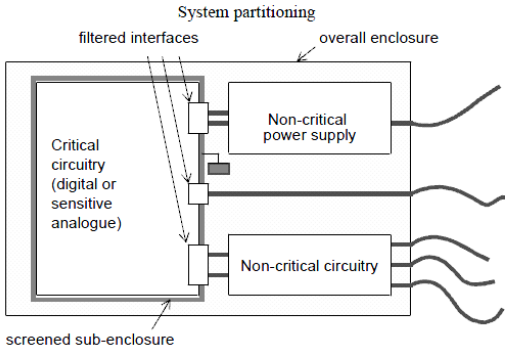
EMC Design Guideline

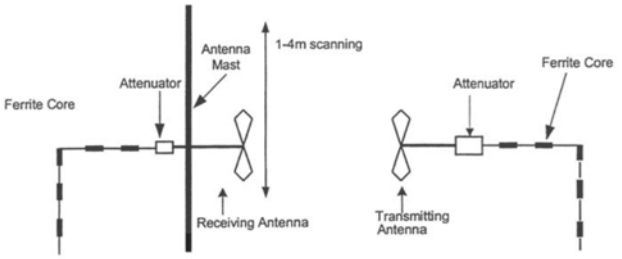
Partitioning separates the system into critical and non-critical sections from EMC point of view.



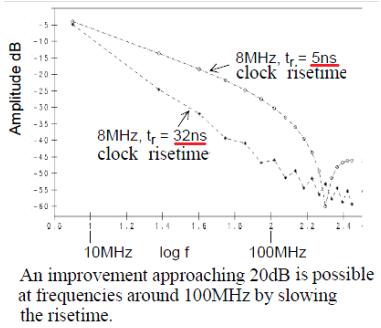
Long I/O and power cables usually act as good antennas, picking up noise from the outside world and conducting this into the system. For unshielded systems, long PCB tracks may also act as antennas. Once inside the system, the noise may be coupled into other, more sensitive signal lines. It is therefore vital that the amount of RF energy allowed into the system be kept as low as possible, even if the input lines themselves are not connected to any sensitive circuit. This can be done by adding one or more of the following:

- Series inductors or ferrite beads will reduce the amount of HF noise that reaches the microcontroller pin. They will have high impedance for HF, while having low impedance for low-frequency signals.
- Decoupling capacitors on the input lines will short the HF noise to ground. The capacitors should have low ESR (equivalent series resistance). This is more important than high capacitance values. In combination with resistors or inductors, the capacitors will form low-pass filters. If the system is shielded, the capacitors should be connected directly to the shield. This will prevent the noise from entering the system at all. Special feed-through capacitors are designed for this purpose, but these may be expensive.
- Special EMC filters combining inductors and capacitors in the same package are now delivered from many manufacturers in many different shapes and component values.

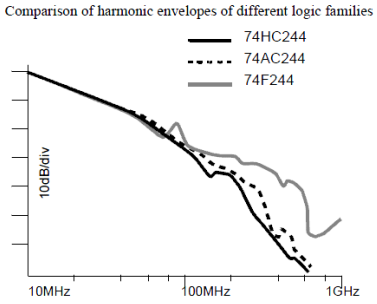
Ferrites with high insertion loss are applied in a wide frequency range. Common mode interferences are filtered with ferrite sleeves and differential mode interferences with ferrite beads. The ferrite beads have the disadvantage that they absorb also the information signal. In order to prevent this, there are ferrites with special frequency dependent impedance.
Current-compensated chokes are a special form of ferrite sleeves with more than a half turn. They have a large asymmetrical effective inductance, typically some mH, and a very small symmetrical inductance, also leakage inductance. The sum of all currents in this chokes should be zero. A small imbalance will cause the inductor partly going into saturation, which results in a decrease of effective inductance.
Using ferrite sleeves to lower any currents flowing on the cable shields:



Emissions: The most critical circuits for EMI emissions are the highly repetitive circuits, such as *clocks, address enables, and high speed data busses*. Even signals with low repetition rates, such as address bit 0, can cause problems with sensitive automotive radio receivers. Consider adding a ferrite bead or small resistor (10±33 ohms) in series with any clock or other high speed output, right at the driving pin. This will help damp any ringing, and also helps provide an impedance match.
Always use the slowest logic family that will do the job; don't use fast logic when it is unnecessary.

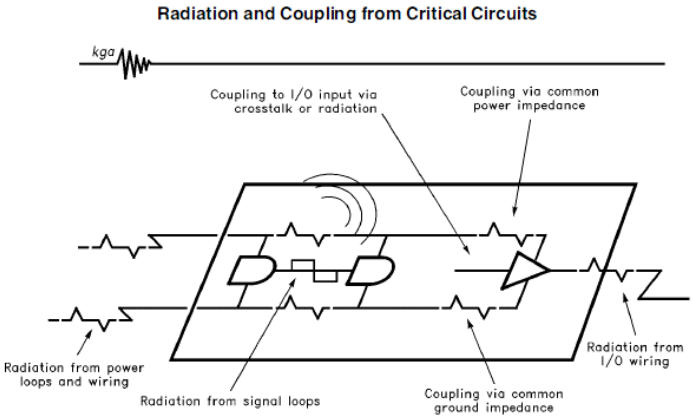


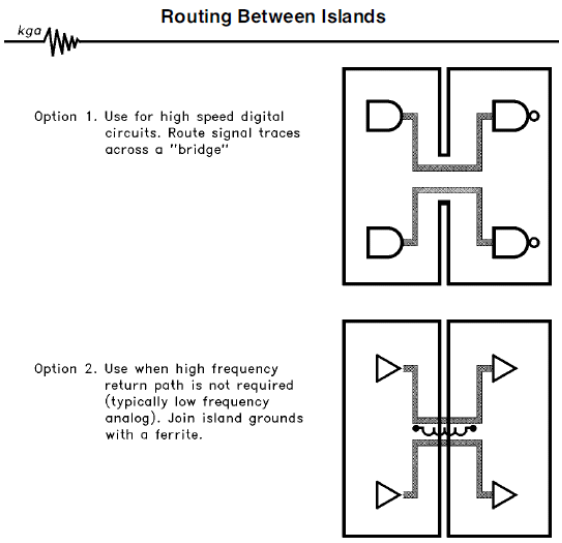
An improvement approaching 20dB is possible at frequencies around 100MHz by slowing the risetime.



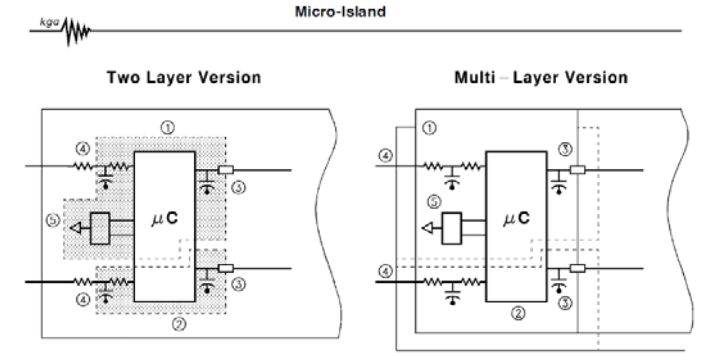
Susceptibility: The most critical circuits for EMI susceptibility are the *reset, interrupt, and control lines*. The entire system can be brought to a halt if one of these lines is corrupted by EMI. Even though these circuits may have slow (or even nonexistent) repetition rates, they are still vulnerable to transients and spikes which can result in false triggering. Use high frequency filtering, such as small capacitors (0.001 mf typical) and ferrite beads (or 100 ohm resistors) to protect these lines. These filtering components should be installed right at the input pins to the microcontroller.
Be especially careful with the reset circuitry, particularly when using external devices for watchdogs or detecting power loss. Any false triggering of these external circuits can cause a false reset, so these external circuits must be protected against EMI as well. Once again, small capacitors and ferrite beads or resistors are very effective as filters against spikes and transients.

EMC Design Guideline





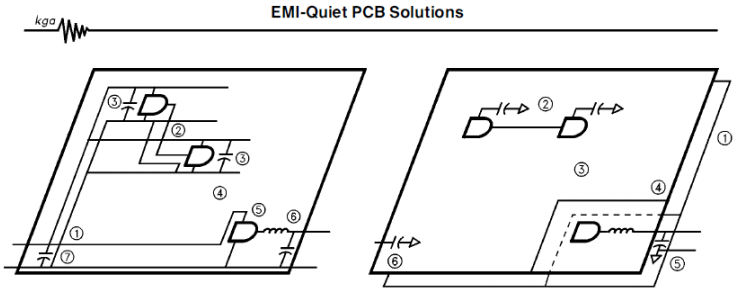
Define the boundaries of the island to encompass all high speed circuitry (microcontroller, crystal, RAM, ROM, etc.). Fill this area with a ground plane.
Isolate every signal entering or leaving the island with a T-filter (ferrite-capacitor or resistor-capacitor). The capacitors are connected to the ground plane through a short lead.
Isolate every power and ground trace with a series ferrite bead. Decouple the power and ground with a 0.01 mF capacitor at the capacitor energy point.
Any signal not starting or ending on Micro-Island must be routed around the island. Later in this application note, we'll share some test results of this technique.



- Use local power decoupling of every integrated circuit on the board.
- For devices with multiple power and ground pins, each pair of pins should be decoupled. High frequency capacitors in the 0.01±0.1 mf range should be installed as close as possible to the device.
- For multi-layer boards, run a short trace from the power pin to the capacitor, and then drop the other lead into the ground plane.
- For two layer boards, ``fat'' traces (with a length to width ratio of 5:1 or less) should be used on both the power and ground sides of the capacitor to minimize inductance.
- In both cases, keep the leads as short as possible.

EMC Design Guideline

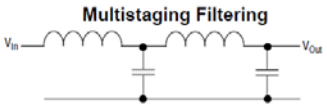
- Additional protection can be provided by *inserting a ferrite in series with the VCC line to the microcontroller*. This must be installed on the VCC side of the capacitor, not on the IC side. This small LC filter further isolates the VCC traces from current demands of the switched device. This technique is strongly recommended for two layer and Micro-Island designs; it's optional for multi-layer designs.
- Use high frequency decoupling at the power entry points. In addition to the standard 1±10 mf ``bulk'' capacitors, add a 0.01±0.1 mf high frequency capacitor in parallel at the power entry point. Due to internal resonances, the bulk capacitors are useless at frequencies above about 1 MHz. The high frequency capacitors are there to intercept any high frequency energy that tries to sneak out the power interface. For more protection, series ferrites can also be added. Be sure to keep the leads short on the decoupling capacitors. The self-inductance of wires and traces is about 8 nH/cm (20 nH/inch), so even a few millimeters of wire length can defeat the decoupling at high frequencies due to the inductance. Figure 13 gives several examples of how lead inductance defeats the decoupling capacitor. Note that once you are above the resonant frequency, using a larger capacitor provides no additional benefits, as the inductive reactance prevails.
- Add high frequency capacitors (0.001 mf typical) to the input and outputs of all on-board voltage regulators. This will protect these devices against high levels of RF energy (which can upset the feedback) and will also help suppress VHF parasitic oscillations from these devices. Keep the capacitors close to the devices, with very short leads.
- Don't overlook the ground leads in the signal interface, as these can provide sneak paths for common mode currents into and out of the system. Add a small ferrite bead in the ground lead, to complete the filtering of the interface.



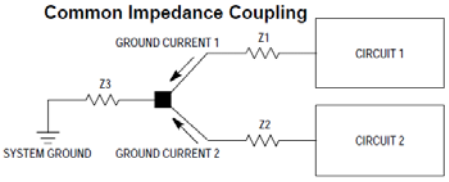
GOOD
- 1. Parallel Power/Ground Traces
- 2. Parallel Signal/Return Traces
- 3. Power Decoupling at Chip
- 4. Separation from I/O
- 5. Separate I/O Power
- 6. High Frequency Filter on I/O
- 7. High Frequency Capacitor on Power

BETTER
1. Multi-Layer Board
2. Power Decoupling at Chip
3. Separation from I/O
4. Isolated I/O Power/Ground Plane
5. High Frequency Filter on I/O
6. High Frequency Capacitor on Power

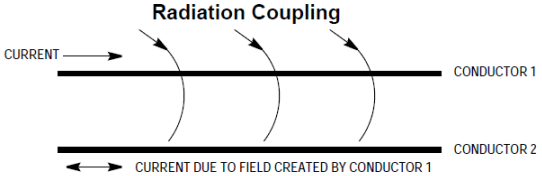
- Use ferrite beads at power entry points. Beads are an inexpensive and convenient way to attenuate frequencies above 1 MHz without causing power loss at low frequencies. They are small and can generally be slipped over component leads or conductors.
- Use multistage filtering to attenuate multiband power supply noise:



- *In high-speed digital circuits, the clock circuitry is usually the biggest generator of wide-band noise*. In faster MCUs, these circuits can produce harmonic distortions up to 300 MHz, which should be eliminated. In digital circuits, the most vulnerable elements are the *reset lines, interrupt lines, and control lines*.
- One of the most obvious, but often overlooked, ways to induce noise into a circuit is via a conductor. A wire run through a noisy environment can pick up noise and conduct it to another circuit, where it causes interference. The designer must either prevent the wire from picking up noise or remove noise by decoupling before it causes interference. The most common example is noise conducted into a circuit on the power supply leads. If the supply itself, or other circuits connected to the supply, are sources of interference, it becomes necessary to decouple before the power conductors enter the susceptible circuit. This type of coupling occurs when currents from two different circuits flow through a common impedance. The voltage drop across the impedance is influenced by both circuits.

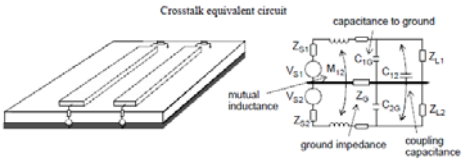


- Ground currents from both circuits flow through the common ground impedance. The ground potential of circuit 1 is modulated by ground current 2. A noise signal or a dc offset is coupled from circuit 2 to circuit 1 through the common ground impedance.



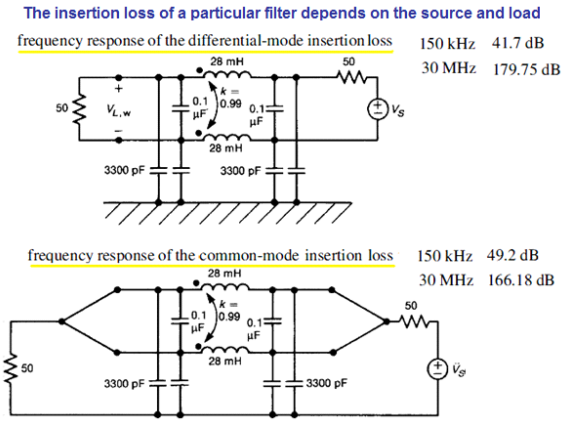
Coupling through radiation, commonly called crosstalk, occurs when a current flowing through a conductor creates an electromagnetic field which induces a transient current in another nearby conductor.

EMC Design Guideline



A ground plane is a useful tool to combat crosstalk. Crosstalk coupling between two tracks is mediated via inductive, capacitive and common ground impedance routes, usually a combination of all three.

The two basic types of radiated emission are differential mode (DM) and common mode (CM).



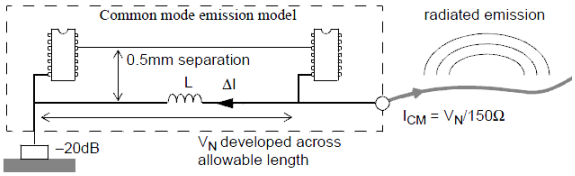
Common-mode radiation or monopole antenna radiation is caused by unintentional voltage drops that raise all the ground connections in a circuit above system ground potential. The electric field term for CM is: E = 4 (1) 10–7 (f L I_f/d) volts/meter

Where:

f = frequency in Hz
L = cable length in m
d = distance from cable in m
I_f = CM current in cable at frequency fA

Common mode radiation which is due mainly to cables and large metallic structures increases at a rate linearly proportional to frequency (ignoring resonances). There are two factors which make common mode coupling the major source of radiated emissions:

- cable radiation is much more effective than from a small loop, and so a smaller common mode current (of the order of microamps) is needed for the same field strength;
- cable resonance usually falls within the range 30-100MHz, and radiation is enhanced over that of the short cable model.



A great deal of interference propagates in ***common-mode***, and this can be attenuated using common-mode (CM) ferrite chokes.
Ferrite effectiveness increases with frequency. The impedance of a ferrite choke is typically around 50ohm at 30MHz, rising to hundreds of ohms above 100MHz (the actual value depends on shape, size and material composition). Usually a ferrite has little effect at frequencies lower than 30MHz, becomes most effective above 100MHz and falls off in performance as the frequency approaches 1GHz. A useful property of ferrites is that their impedance becomes resistive at the higher frequencies, so that interference energy tends to be absorbed rather than reflected.

Differential-mode radiation occurs when an alternating current passes through a small loop. The magnitude of the radiation from the loop varies in proportion to the current. The electric field term for DM is: E = 265 (10^{-16}) (A I_f f^2/d) volts/meter

Where:

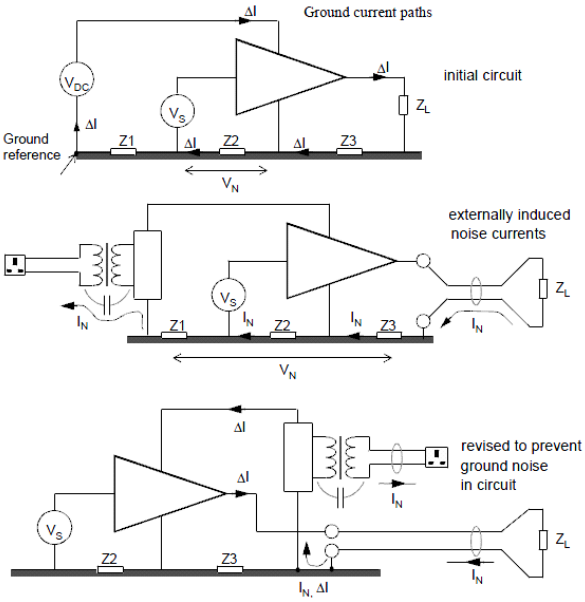
A = loop area in m/2
d = distance from loop center in m
I_f = current at frequency A in Hz
f = frequency (of harmonic) in Hz

Due to the magnitude of the electric field, *CM radiation is much more of an emission problem than DM radiation*. To minimize CM radiation, common current must be reduced to zero by means of a sensible grounding scheme.
Higher supply voltages mean greater voltage swings and more emissions. Lower supply voltages can affect susceptibility.
Higher frequency yields more emissions. Periodic signals generate more emissions. High-frequency digital systems create current spikes when transistors are switched on and off. Analog systems create current spikes when load currents change.

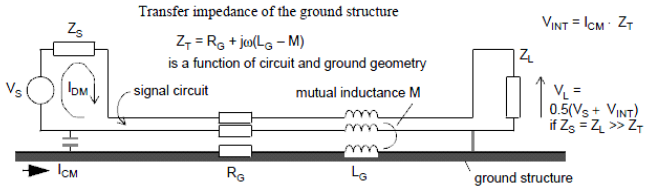
EMC Design Guideline

Grounding

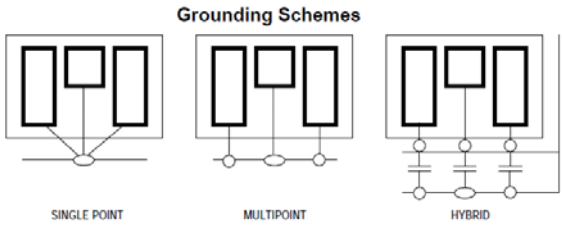
Nothing is more important to circuit design than a solid and complete power system. An overwhelming majority of all EMC problems, whether they are due to emissions, susceptibility, or self-compatibility, have inadequate grounding as a principal contributor. The most important EMC function of a ground system is to minimize interference voltages at critical points compared to the desired signal. To do this, it must present a low transfer impedance path at these critical locations.



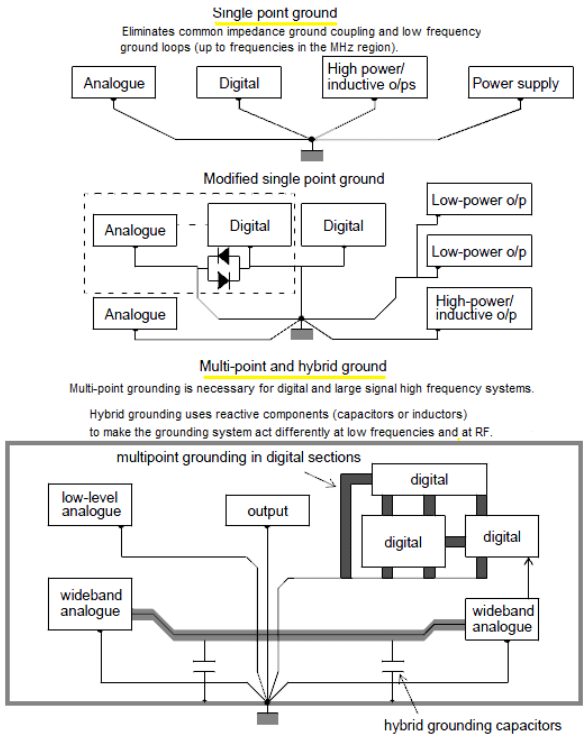
Interference voltages V_N which are developed across the impedances can create emission or susceptibility problems. At high frequencies (above a few kHz) or high rates of change of current the impedance of any linear connection is primarily inductive and increases with frequency ($V = - L \cdot di/dt$), hence *ground noise increases in seriousness as the frequency rises*.
Interference current I_N induced in, say, the output lead, flows through the ground system, passing through Z_2 again and therefore inducing a voltage in series with the input, before exiting via stray capacitance to the mains supply connection. To deal with the problem *ensure that the interfering currents are not allowed to flow through the sensitive part of the ground network*.



There are three types of ***signal grounding****: single point, multipoint and hybrid:*



EMC Design Guideline

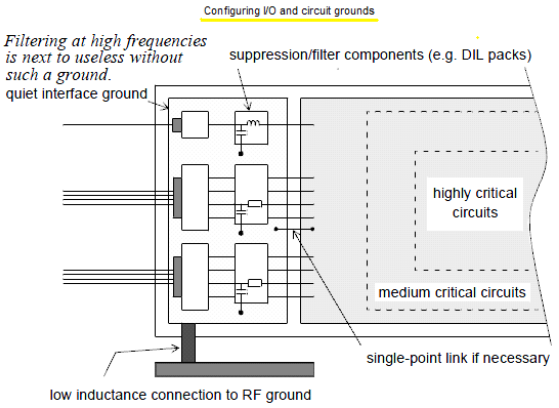


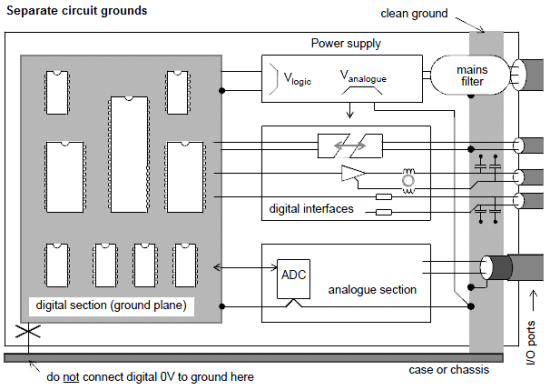
Grounding principles:

- All conductors have a finite impedance which increases with frequency
- Two physically separate ground points are not at the same potential unless no current flows between them
- At high frequencies there is no such thing as a single point ground

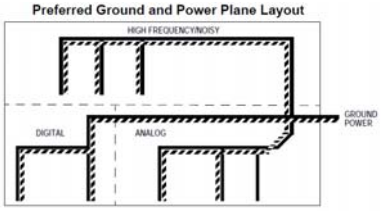
Grounding rules:

- identify the circuits of high di/dt (for emissions) - clocks, bus buffers/drivers, high-power oscillators
- identify sensitive circuits (for susceptibility) - low-level analogue, fast digital data
- minimize their ground inductance by - minimizing the length and enclosed area implementing a ground plane keeping critical circuits away from the edge of the plane
- ensure that internal and external ground noise cannot couple out of or into the system: *incorporate a clean interface ground*
- partition the system to control common mode current flow between sections
- create, maintain and enforce a ground map



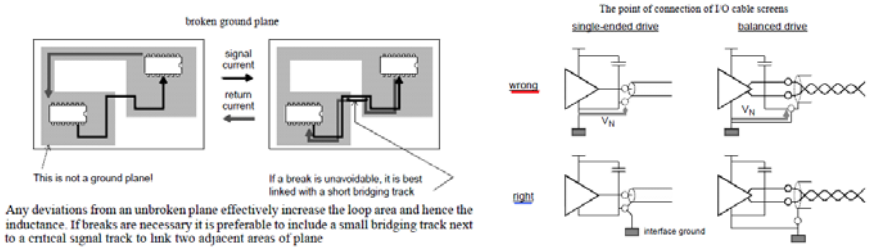


Ground layout is especially critical, *ground returns from high-frequency digital circuits and low-level analog circuits must not be mixed*.



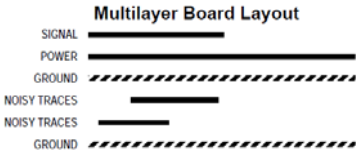
EMC Design Guideline

Proper printed circuit board (PCB) layout is essential to prevention of EMI.



Power Decoupling

When a logic gate switches, a transient current is produced on power supply lines. These transient currents must be damped and filtered out. *High-frequency ceramic capacitors with low-inductance* are ideal for this purpose.



Transient currents from high di/dt sources cause ground and trace "bounce" voltages. The high di/dt generates a broad range of high frequency currents that excite structures and cables to radiate.

A variation in current through a conductor with a certain inductance, L, results in a voltage drop of: $V = L.\ di/dt$

The voltage drop can be minimized by reducing either the inductance or the variation in current over time. Three ways to prevent interference are:

1. Suppress the emission at its source.
2. Make the coupling path as inefficient as possible.
3. Make the receptor less susceptible to emission.

Device-Level Techniques

- Use multiple power and ground pins
- Use fewer clocks
- Eliminate fights or race conditions
- Reduce output buffer drive
- Use low-power techniques
- Reduce internal power/ground trace impedance
- For long buses, keep high-speed traces separated from lowspeed traces. Add extra spacing between high-speed and lowspeed signals and run high-frequency signals next to a ground bus.
- Supply good ground imaging for long traces, high-speed signals
- Turn off clocks when not in use
- Eliminate charge pumps if possible
- Minimize loop area within chip

Board-Level Techniques

- Use ground and power planes
- Maximize plane areas to provide low impedance for power supply decoupling
- Minimize surface conductors
- Use narrow traces (4 to 8 mils) to increase high-frequency damping and reduce capacitive coupling
- Segment ground/power for digital, analog, receiver, transmitter,relays, etc.
- Separate circuits on PCB according to frequency and type
- Do not notch PCB; traces routed around notches can cause unwanted loops
- Use multilayer boards to enclose traces between power and ground planes
- Avoid large open-loop plane structures
- Border PCB with chassis ground; this provides a formidable shield (or field interceptor) to prevent radiation (or reduce susceptibility) at the circuit boundaries.
- Use multipoint grounding to keep ground impedance low at high frequencies
- Use single-point grounding only for low-frequency, low-level circuits
- Keep ground leads shorter than one-twentieth (1/20) of a wavelength to prevent radiation and to maintain low impedance

EMC Design Guideline

Routing noise-reduction techniques

- Use 45-degree, rather than 90-degree, trace turns. Ninety-degree turns add capacitance and cause change in the characteristic impedance of the transmission line.
- Keep spacing between adjacent active traces greater than trace width to minimize crosstalk.
- Keep clock signal loop areas as small as possible.
- Keep high-speed lines and clock-signal conductors short and direct.
- Do not run sensitive traces parallel to traces that carry highcurrent, fast-switching signals.
- Eliminate floating digital inputs to prevent unnecessary switching and noise generation:
  – Configure multipurpose device pins as outputs.
  – Set three-state pins to high impedance.
  – Use appropriate pull-up or pull-down circuitry.
- Avoid running traces under crystals and other inherently noisy circuits.
- Run corresponding power and ground and signal and return traces in parallel to cancel noise.
- Keep clock traces, buses, and chip-enable lines separate from input/output (I/O) lines and connectors.
- To protect critical traces:
  – Use 4-mil to 8-mil traces to minimize inductance.
  – Route close to ground plane.
  – Sandwich between planes.
  – Guard-band with a ground on each side.
- Use orthogonal crossovers for traces and intersperse ground traces to minimize crosstalk, especially when analog and digital signals are routed together.
- Route clock signals perpendicular to I/O signals.

Filter techniques

- Filter the power line and all signals entering a board.
- Use high-frequency, low-inductance ceramic capacitors for integrated circuit (IC) decoupling at each power pin (0.1 µF for up to 15 MHz, 0.01 µF over 15 MHz).
- Use tantalum electrolytic capacitors as bulk decoupling capacitors at headers and connectors. Bulk decoupling capacitors recharge the IC decoupling capacitors.
- Bypass all power feed and reference voltage pins for analog circuits.
- Bypass fast switching transistors.
- Decouple locally whenever possible.
- Decouple power/ground at device leads.
- Use ferrite beads at power entry points. Beads are an inexpensive and convenient way to attenuate frequencies above 1 MHz without causing power loss at low frequencies. They are small and can generally be slipped over component leads or conductors.
- Use multistage filtering to attenuate multiband power supply noise

Other design techniques

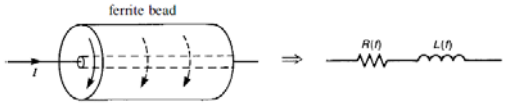
- Mount crystals flush to board and ground them.
- Use shielding where appropriate.
- Use the lowest frequency and slowest rise time clock that will do the job.
- Use series termination to minimize resonance and transmission reflection. Impedance mismatch between load and line causes a portion of the signal to reflect. Reflections induce ringing and overshoot, producing significant EMI. Termination is needed when line length, L, (inches) exceeds 3 t_r (ns). The value of the termination resistor is given by:$R_L = Z_0/(1 + C_L/C_{Line})1/2$

  Where:

  Z = Characteristic impedance of the line without the load(s)
  C_L = Total load distributed along the line
  C_{Line} = Total capacitance of the line without the load(s)
- Route adjacent ground traces closer to signal traces than other signal traces for more effective interception of emerging fields.
- Place properly decoupled line drivers and receivers as close as practical to the physical I/O interface. This reduces coupling to other PCB circuitry and lowers both radiation and susceptibility.
- Shield and twist noisy leads together to cancel mutual coupling out of the PCB.
- Use clamping diodes for relay coils and other inductive loads.
- For emission diagnostics use clamp ferrites on harnesses to eliminate effect of conducted energy.

Capacitors, inductors, and ferrites characteristically are used to filter narrow frequency bands.

Ferrites are a ceramic material having very poor conductivity. *Ferrites act as a combination inductor and frequency-dependent resistor whose resistance is proportional to frequency.* For this reason ferrite beads are great for eliminating high-frequency noise on (low-current) power supplies and digital clock signals. Ferrite beads are used to provide high impedance at the frequencies of the unwanted noise.



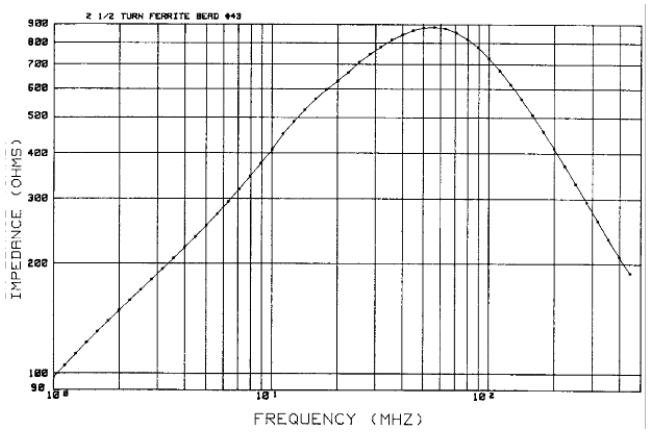
$L_{bead} = \mu_0 \mu_r K$ K is some constant depending on the bead dimensions

$\mu_r = \mu_r'(f) - j\mu_r''(f)$

μ_r' is related to the stored magnetic energy in the bead material

μ_r'' is related to the losses in the bead material

EMC Design Guideline



Digital circuit designers like to think of signals in terms of their voltage. *Signal integrity and EMC engineers must think of signals in terms of their current.*
There are two things that every good circuit designer should know about signal currents.

1. Signal currents always return to their source (i.e. current paths are always loops)
2. Signal currents take the path(s) of least impedance.

At megahertz frequencies and higher, signal current paths are relatively easy to identify. This is because the path of least impedance at high frequencies is generally the path of least inductance, which is generally the path that minimizes the loop area. Currents return as close as possible to the path of the outgoing current.

At low frequencies (generally kHz frequencies and below), the path of least impedance tends to be the path(s) of least resistance. Low frequency currents are more difficult to trace, since they will spread out significant current return paths may be relatively distance from the outgoing current path.

There are some situations where a well-placed gap in the return plane is called for. However, these are relatively rare and always involve a need to control the flow of low-frequency currents. The safest rule-of-thumb is to *provide one solid plane for returning all signal currents*. In situations where you expect that a particular low-frequency signal is susceptible or is capable of interfering with the circuitry on your board, *use a trace on a separate layer to return that current to its source*.

In general, *never split, gap or cut your board's signal return plane*. If you are convinced that a gap is necessary to prevent a low-frequency coupling problem, seek advice from an expert. Don't rely on design guidelines or application notes and don't try to implement a scheme that "worked" in someone else's "similar" design.

Many times simple board designs that should have had no trouble at all meeting EMC requirements at no additional cost or effort, wind up being heavily shielded and filtered because they violated this simple rule.

Why is the location of connectors so important? At frequencies below a few hundred megahertz, wavelengths are on the order of a meter or longer. Any possible antennas on the printed circuit board itself tend to be electrically small and therefore inefficient. However, *cables or other devices connected to a board can serve as relatively efficient antennas*. Signal currents flowing on traces and returning through solid planes result in small voltage differences between any two points on the plane. These voltage differences are generally proportional to the current flowing in the plane. When all connectors are placed along one edge of a board, the voltage between them tends to be negligible. However, high-speed circuitry located between connectors can easily develop potential differences of a few millivolts or greater between the connectors. These voltages can drive currents onto attached cables causing a product to exceed radiated emissions requirements.

A board operating with a clock speed of 100 MHz should never fail to meet a radiated emissions requirement at 2 GHz. A *well-formed digital signal* will have a significant amount of power in the lower harmonic frequencies, but not so much power in the upper harmonics*. Power in the upper harmonic frequencies is best controlled by controlling the transition times in digital signals. Longer transition times are preferred for EMC*. Excessively long transition times can cause signal integrity and thermal problems. An engineering compromise must be reached between these competing requirements. *A transition time that is approximately 20% of a bit period result in a reasonably good-looking waveform, while minimizing problems due to crosstalk and radiated emissions.* Depending on the application, transitions times may need to be more or less than 20% of the bit period; however transitions times should not be left to chance.

There are three common methods for controlling rise and fall times in digital logic:

1. Use a logic family that is only as fast as the application requires.
2. *Put a resistor or a ferrite in series with a device's output.*
3. Put a capacitor in parallel with a device's output.

The first choice is often the easiest and most effective option. However, the use of a resistor or ferrite gives the designer more control and is less affected by changes that occur in logic families over time. Capacitors can actually increase the amount of high-frequency current drawn by the source device and in most cases are not appropriate choices.

Note that it is never a good idea to try to slow down or filter a single-ended signal by impeding the flow of current in the return path. For example, one should never intentionally route a low-speed trace over a gap in a return plane in an attempt to filter out the high-frequency noise.

Ferrite beads tend to be effective in blocking noise currents in power supplies and typically have maximum values of impedance of the order of a few hundred ohms. Therefore, in order for them to be effective, they must be *in series with impedances that are no larger than the bead impedance*, since otherwise the bead impedance would be overshadowed by this larger impedance. The intent is to use the bead to *block noise currents by adding significant impedance to the path*. Circuit impedances tend to be small in power supplies as opposed to other electronic circuits. Therefore insertion of a bead tends to provide a significant increase in the circuit impedance in power supply circuits.

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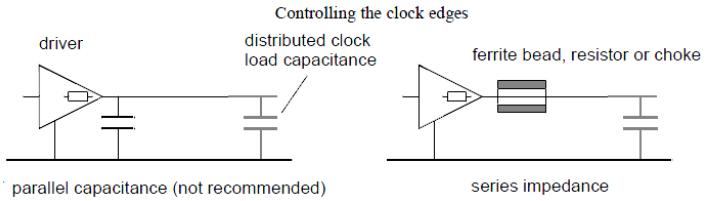
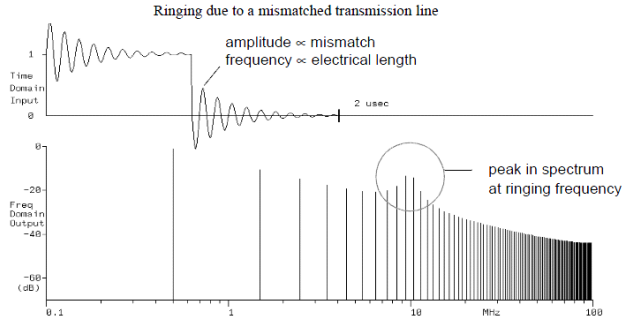
The main source of radiation in digital circuits is the processor clock (or clocks) and its harmonics.

- The *narrowband emissions* should be minimized first, by proper layout, grounding and buffering of clock lines.
- Where circuit constraints allow it, is recommended to slow clock edges to minimize harmonic generation. This can be done in three ways: series impedance, parallel capacitance or by using a low-performance buffer. Generally, slugging the clock output with a parallel capacitor is undesirable because although it has the desired effect of reducing the dv/dt feeding into the clock line, it increases the capacitive loading on the driver and hence increases the di/dt drawn from its supply pins; the overall effect may be to worsen the emissions rather than improve them.
- *It is preferable to increase the series impedance of the driver output at the harmonic frequencies*, and this can best be done with a *small ferrite impeder in series with the output.*
- A low-value resistor is often an acceptable substitute; low-loss inductors are less helpful as they tend to introduce ringing.



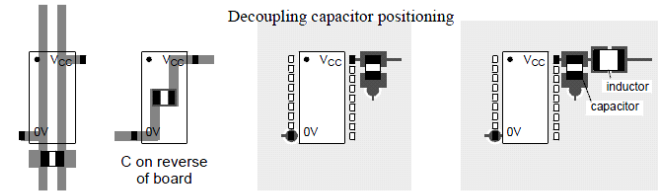
Ringing on transmission lines

If you transmit data or clocks down long lines, these must be terminated to prevent ringing. Ringing is generated on the transitions of digital signals when a portion of the signal is reflected back down the line due to a mismatch between the line impedance and the terminating impedance. A similar mismatch at the driving end will re-reflect a further portion towards the receiver, and so on. Severe ringing will affect the data transfer, by causing spurious transitions, if it exceeds the device's input noise margin. Aside from its effect on noise margins, ringing may also be a source of radiated interference in its own right. The amplitude of the ringing depends on the degree of mismatch at either end of the line while the frequency depends on the electrical length of the line. A digital driver/receiver combination should be analysed in terms of its transmission line behaviour if: 2 x t_{PD} x line length > transition time (where t_{PD} is the line propagation delay in ns per unit length).



Digital circuit decoupling

No matter how good the VCC and ground connections are, they will introduce impedance which will create switching noise from the transient switching currents taken from the VCC pins. The purpose of a decoupling capacitor is to maintain low dynamic impedance from the individual IC supply voltage to ground. This minimizes the local supply voltage droop when a fast current pulse is taken from it, and more importantly it minimizes the lengths of track which carry high di/dt currents. Placement is critical; the capacitor must be tracked close to the circuit it is decoupling.



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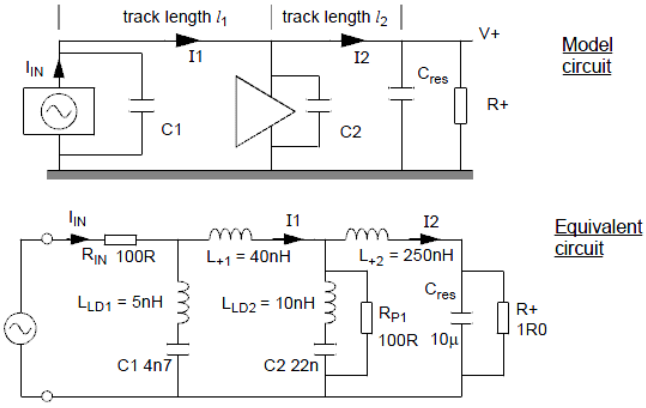
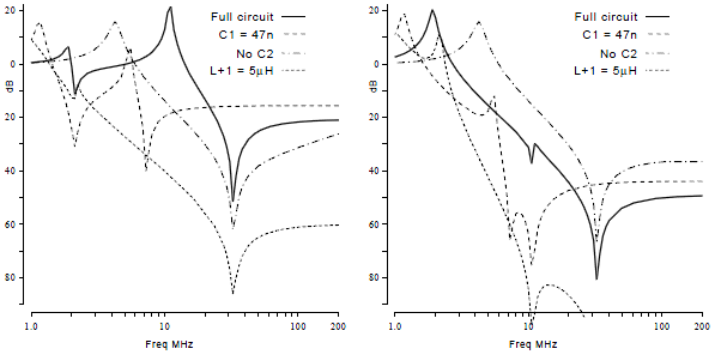
Component selection

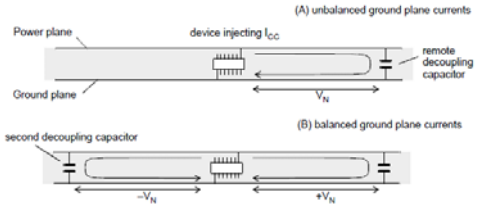
The crucial factor when selecting capacitor type *for high-speed logic decoupling is lead inductance* rather than absolute value. Minimum lead inductance offers low impedance to fast pulses. Small disk or multilayer ceramics, or polyester film types (lead pitch 2.5 or 5mm), are preferred; chip capacitors are even better. The overall inductance of each connection is the sum of both lead and track inductances. Flat ceramic capacitors, matched to the common dual-in-line pinouts, and intended for mounting directly beneath the IC package, *minimize the pin-to-pin inductance* and offer superior performance above about 50MHz.





$I1/I_{IN}$ Decoupling effect $I2/I_{IN}$

distributing many capacitors across the board, particularly close to high-noise devices, will control the resulting currents as far as possible.



EMC Design Guideline

Multiple Returns in Ribbon Cable

Why "multiple returns in a ribbon cable" are an important rule for good design practice?

RIBBON CABLES EMC DISADVANTAGES:

1) CROSSTALK

a. Occurs between the various conductors and the radiation from and susceptibility of the cable. This crosstalk occurs between not only adjacent conductors but between all of the conductors to various degrees.

b. If only one of the conductors in the cable is used as the return or ground line for all of the other signal conductors (e.g. signals "a" and "g" in the figure below) will generate a current loop.

c. Note that conductor "g" surrounds the loop generated by conductor "a". Therefore, *the time-varying field generated by current i_g will easily induce a current in conductor a.*

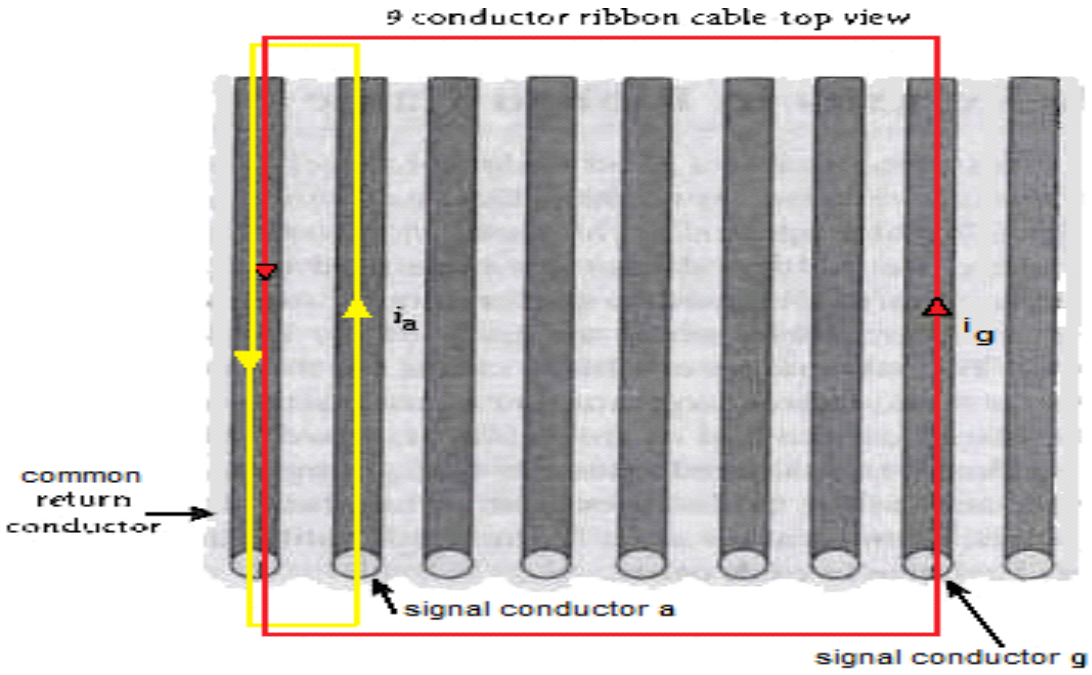
d. Similarly, the field generated by a time-varying current in will induce a current in conductor g. The actual induced currents (and voltages) are a complicated function of the mutual capacitance and inductance between each of the conductors and the source and load impedances between each conductor and the return conductor. It has been shown that to predict accurately the crosstalk between each of the wires,

2) COMMON-MODE IMPEDANCE COUPLING

a. At lower frequencies, common-impedance coupling is an issue.

b. The impedance of the return conductor (i.e., its resistance and inductive reactance) becomes important.

c. The *voltage drop* along the return conductor is a function of all of the currents returning along it. Therefore, *the voltage of the return conductor will vary with the signal currents*. This variation of the voltage across or current through a common conductor is referred to as *common-impedance coupling*.



3) EMISSIONS/RADIATIONS FROM RIBBON & SUSCEPTIBILITY OF RIBBON CABLE TO EXTERNAL NOISE

- For electrically-short cables, both the emissions and susceptibility increase with the length of the cable and with the loop area generated by each conductor and its return
- For *single return conductor* scenario, the loop area generated by the conductors that are not adjacent or near to the return conductor can generate significant emissions and be quite susceptible to external noise.

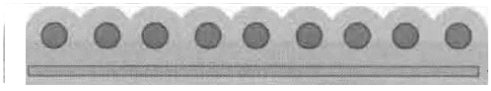
4) RIBBON CABLE CAPACITANCE

Ribbon cables capacitance is somewhat larger than many other cables (and larger than an unbundled set of wires). Distortion and signal source loading that can occur with excessive capacitance but it is more likely that crosstalk will limit the useful length of the ribbon cable. The suggested maximum length is 10 ft but increasing the rise and fall time of the signals on the conductors, can extend this length.

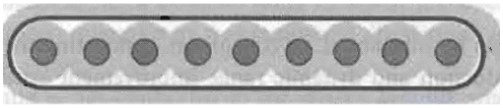
EMC Design Guideline

METHODS TO IMPROVE RIBBON CABLE EMC PERFORMANCE

1) Use every other conductor or more than one conductor as a return or ground GSGSGS ... or GSSGSSG ... where S and G represent signal and ground conductors, respectively. These schemes essentially reduce the loop area for the signal and its return, reducing emissions, susceptibility, and crosstalk. Although a percentage of the current for a signal can pass through returns that are not nearby, most of the current will return through the path of least impedance. In this case, the path of the least impedance is generally where the loop area and, hence, inductance is the smallest. Common impedance coupling is also reduced when multiple returns are used. It is not always necessary to use a separate or nearby return for every signal conductor. A nearby return should be used for critical lines such as enabling or strobing signals.
2) Use balanced differential sources and receivers. As opposed to unbalanced single-ended sources (where one side of the supply is grounded and, therefore, the return for the signal is also grounded), when balanced sources (and receivers) are used, neither side is connected directly to the ground or signal reference. To maintain the balance of the sources, two conductors are required for each source.
3) Use ribbon cables with flat conducting returns. If a return has to be shared among several signals, then the impedance of the return should be as small as possible. The addition of this large return conductor can substantially reduce the mutual capacitance and inductance between the signal conductors. It also reduces the loop area generated by the signal and its return current. The return current for each signal will be concentrated directly under the wire in the ground plane. It is necessary, however, to terminate properly the ground plane at both ends of this type of ribbon cable with a full-width connection to the system ground.
4) Use shielded ribbon cables require a full 360^0 connection for effectiveness; otherwise, pigtail-related problems can arise. It is important to restate that the link between the shield and return plane of the cable and the equipment should be as complete and continuous as possible. A single pigtail or drain wire is normally inadequate, especially at higher frequencies.



RIBBON CABLE WITH GROUNDPLANE



SHIELDED RIBBON CABLE

5) Use multiple sets of twisted pair in a flat package (referred to as "Twist-'nflat" or "Varl-Twist"). By twisting the pairs, the differential radiation (radiation from the currents in the signal and return that are in opposite directions) from the wires is substantially reduced. The radiation from the common-mode signal (radiation from the currents in the signal and return that are in the same direction) is not affected (much) by the twisting of the wires. Unfortunately, these twisted-pair multi-conductor cables can have flat termination areas spaced along the cable for termination or mounting. In these untwisted areas of the cable, the EMC advantages of twisted lines are lost.
6) Use flat cables with multiple, miniature parallel coaxial cables, each with its own inner conductor, concentric outer conductor, and drain wire(s).This ribbon coaxial cable was designed for high-speed computer applications.
7) When flat cables are stacked, coupling does occur between the different cable layers. Increasing the distance between the layers, using individually shielded flat cables, or inserting a shield between the layers can reduce the crosstalk between cables.