HW ASSIGNMENT 1 REPORT

pushpraj , kartik

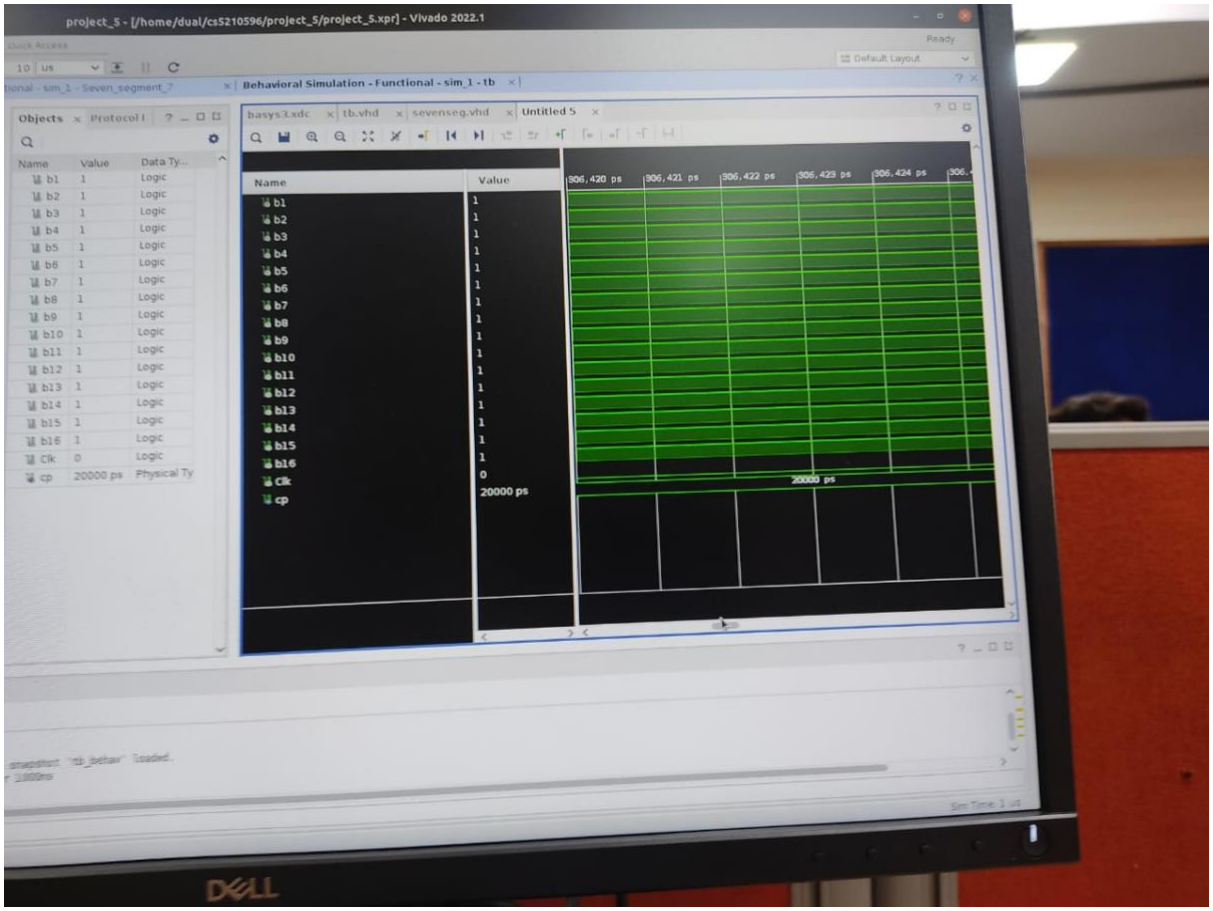
DESIGN DECISIONS:

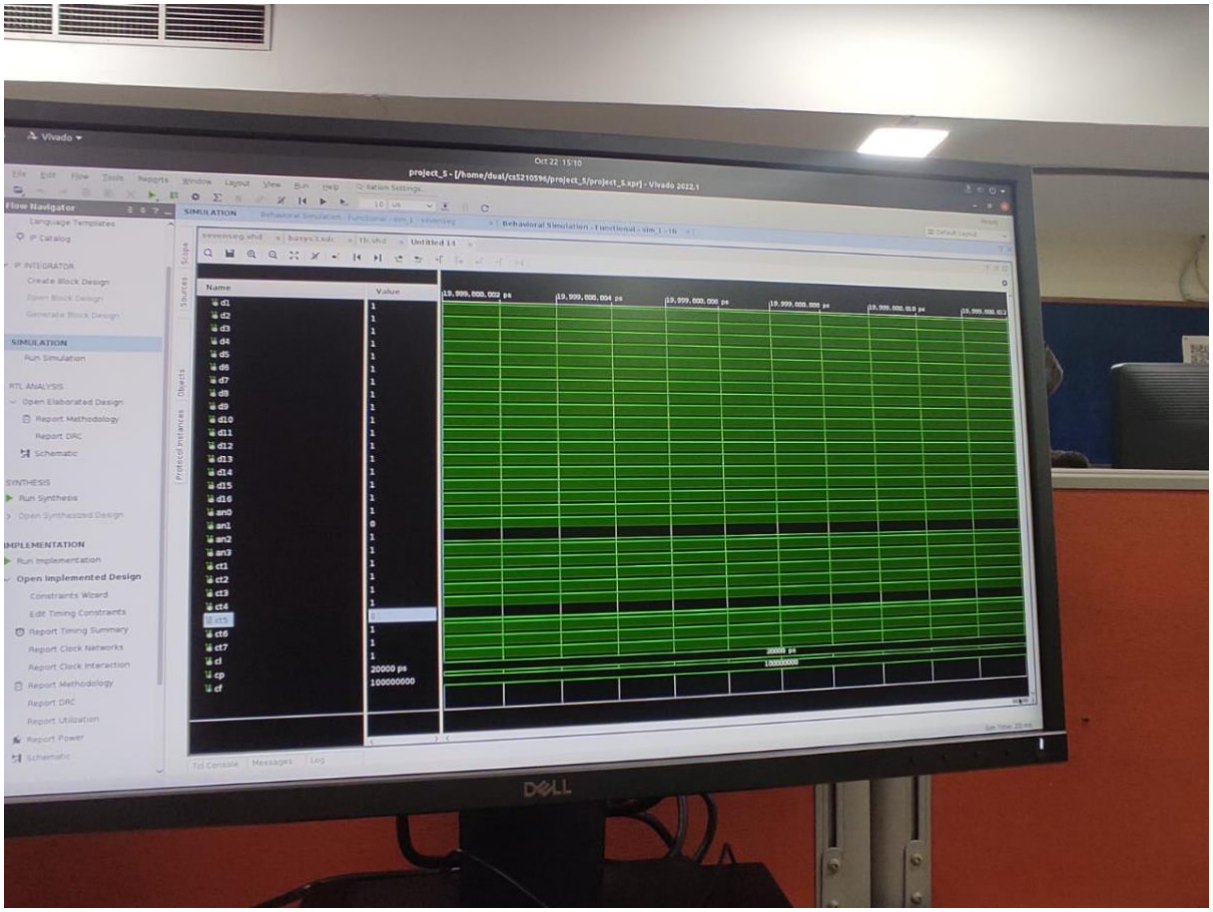
• We designed the 7 segment display by first minimising the minterms using kmaps. Given 4 bit number we have to set some cathodes equal to 0 while others 1 which are not to be illuminated, also the corresponding anode must be 0. We minimised the terms by introducing dont cares for the terms whose value is more then 9.

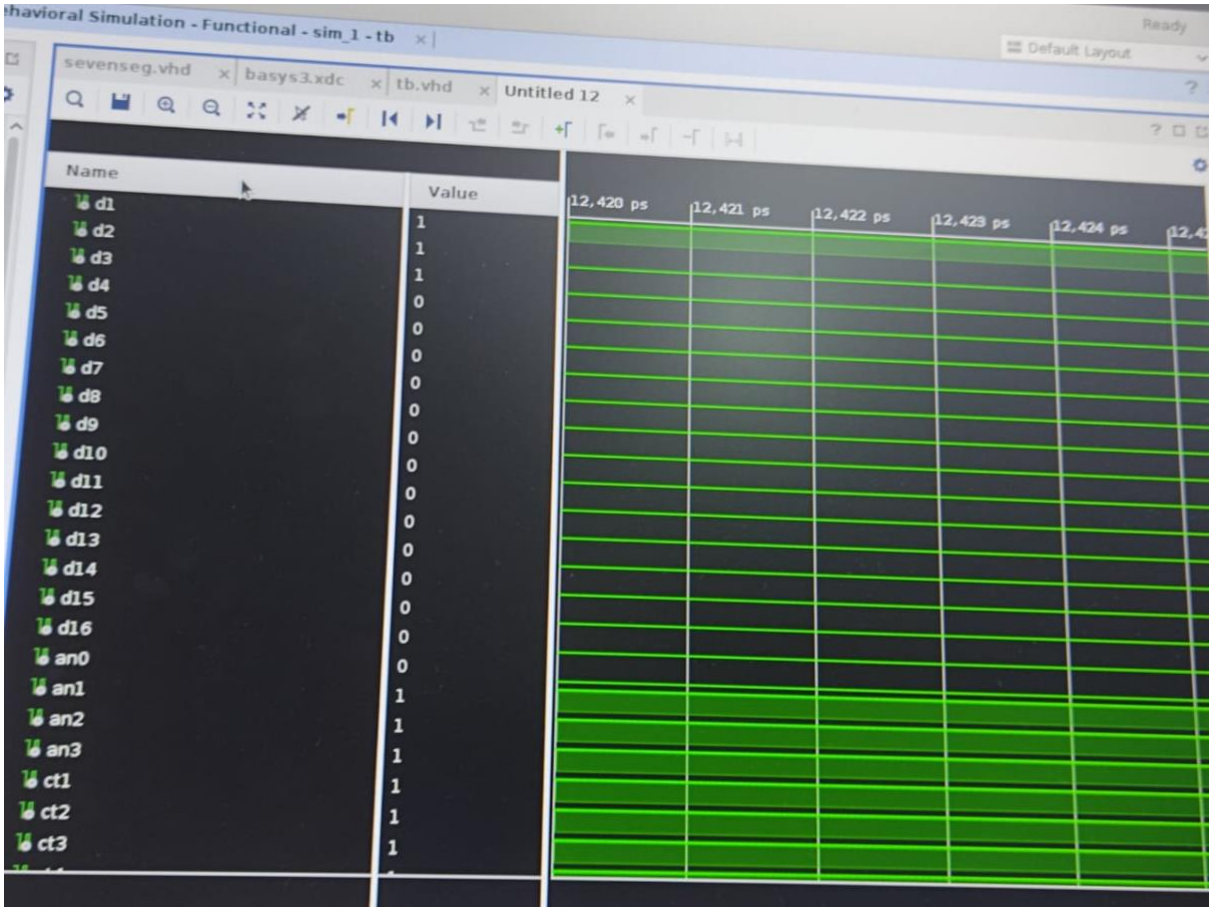
LAB WORK:

• It was easy to implement the some function , but building the clock was main challenge , but after reading instructions carefully we realised , basys board has an inbuilt oscillator which we can use to drive the clock and implement the required functions. • For the purpose of test bench , we made a signal named cl that changes its value i.e. from 0 to 1 or vice-versa every 5 ns , and time interval between two rising edges becomes 10ns , so for every 10ns , we increase a counter. When the counter becomes 100000(1 lakh) , the time elapsed becomes 1ms. So we run such 4 cycles to get 4ms and in that range a particular anode is set to 0 rest all 1. This way we get the required refresh rate. We tested the code by creating a test bench and it gave expected results. The basys board too reflected the expected results on varying inputs.

Simulation Snapshots


project_5 - [/home/dual/cs5210596/project_5/project_5.xpr] - Vivado 2022.1
Behavioral Simulation - Functional - sim_1 - tb
basys3.xdc
tb.vhd
sevenseg.vhd
Untitled 5
Objects
Protocol I
Name
Value
Data Ty...
b1
b2
b3
b4
b5
b6
b7
b8
b9
b10
b11
b12
b13
b14
b15
b16
Clk
cp
20000 ps
Logic
Physical Ty
306,420 ps
306,421 ps
306,422 ps
306,423 ps
306,424 ps
DELL


Vivado
project_5 - [/home/dual/cs5210596/project_5/project_5.xpr] - Vivado 2022.1
Flow Navigator
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
IMPLEMENTATION
Run Implementation
Open Implemented Design
Name
Value
d1
d2
d3
d4
d5
d6
d7
d8
d9
d10
d11
d12
d13
d14
d15
d16
an0
an1
an2
an3
ct1
ct2
ct3
ct4
ct5
ct6
ct7
cl
cp
cf
20000 ps
100000000
DELL


havioral Simulation - Functional - sim_1 - tb
Ready
Default Layout
sevenseg.vhd
basys3.xdc
tb.vhd
Untitled 12
Name
Value
d1 1
d2 1
d3 1
d4 0
d5 0
d6 0
d7 0
d8 0
d9 0
d10 0
d11 0
d12 0
d13 0
d14 0
d15 0
d16 0
an0 0
an1 1
an2 1
an3 1
ct1 1
ct2 1
ct3 1
12,420 ps
12,421 ps
12,422 ps
12,423 ps
12,424 ps