

EEE 313 Term Project
Bilkent University
Department of Electrical and Electronics Engineering



Audio Amplifier With Gain and Power Stages

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Introduction and Purpose

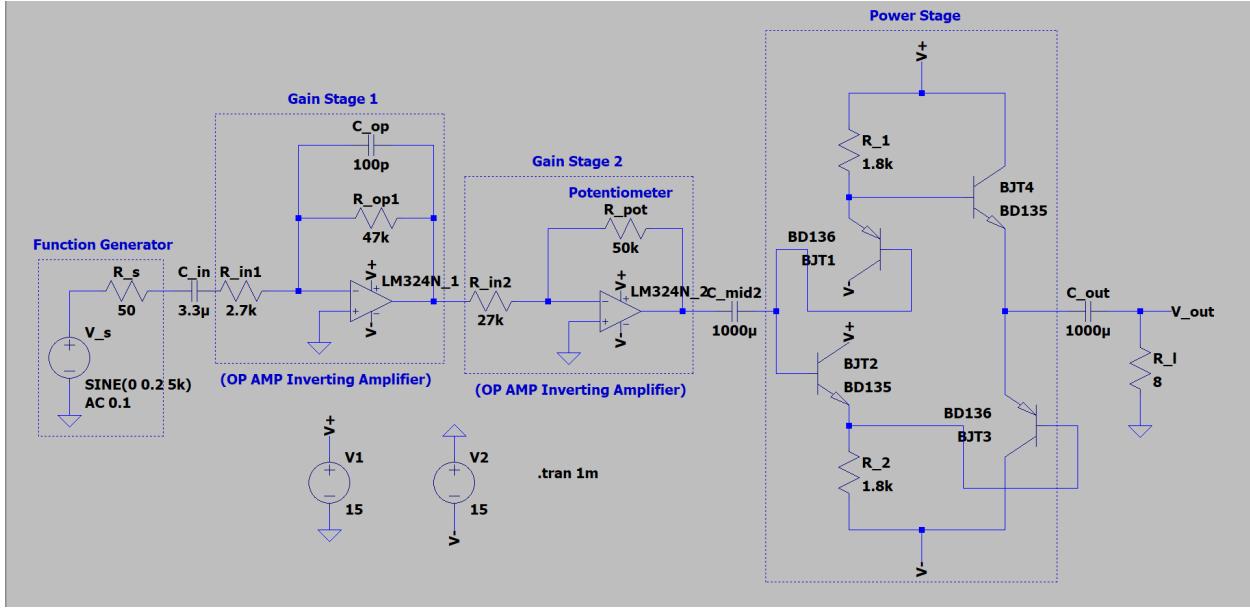


Figure 1: Overview of the entire circuit.

In this term project, the objective was to design and implement a circuit capable of driving an 8Ω speaker from the output of a Samsung S10+ smartphone. This was accomplished using two gain stages and one power stage.

In the first gain stage, an OP AMP in the inverting amplifier configuration was used. A coupling capacitor and a capacitor parallel to the feedback resistor were utilized for high-pass and low-pass filtering respectively. The aim of this stage is to provide constant voltage gain and get rid of unwanted frequencies.

In the second gain stage, again, an OP AMP in the inverting amplifier configuration was utilized. Differences from the first gain stage are, there being no capacitors, and a potentiometer being used in variable resistor configuration in the place of the constant feedback resistor. The aim of this stage is to provide volume adjustment and additional voltage gain. Since the potentiometer is used to change the gain of an OP AMP, no additional energy is wasted if the volume is turned down. The potentiometer cannot be implemented in the first gain stage because C_{OP} and R_{OP1} together determine the upper cutoff frequency of the amplifier, which should not change with the volume.

In the power stage, a class-AB output stage with input buffer transistors was used. The aim of this stage is to provide the current needed to power the speaker while resulting in minimal voltage loss. While the two transistors and two resistors on the left provide quiescent bias, the two transistors on the right accomplish the current amplification. Half of the sine wave goes through the top transistor, while the other half goes through the bottom transistor, increasing efficiency compared to the class-A output stage. Each transistor stays “on” slightly longer than

half of the cycle to diminish crossover distortion. The two coupling capacitors connecting this stage to the rest of the circuit isolate the constant component of the voltage from escaping. Since any impedance resulting from these capacitors are unwanted, a **large capacitance value** was chosen.

Methods

After the general circuit topology was established, the particular component values were determined by circuit analysis. First, the first and second gain stage resistance values.

The formula for the gain of the inverting amplifier configuration used in both the first and second gain stages is the following.

$$A_V = \frac{-R_{feedback}}{R_{in}}$$

Since the gain is determined by a ratio, the absolute values of the chosen resistors are not important in this regard. However, this issue has significant repercussions in other areas. Choosing the resistance values to be too small increases the current draw. Since OP AMPs can provide a limited amount of current, this is undesirable. Choosing the resistance values to be too large, on the other hand, magnify the non-ideal behaviors of the OP AMP and adds noise. Keeping these factors in mind, resistors in the tens of kilohms were chosen. Considering the gain bandwidth product specification of the OP AMP, the following resistance values were chosen. **2.7kΩ** and **47kΩ** for the first gain stage and **27kΩ** and **50kΩ** (max potentiometer value) for the second gain stage resulting in voltage gain values of **17.4** and **1.85** respectively. The maximum calculated voltage gain at the output of these two stages is **32.2**.

For the capacitors, the formula for both high and low-pass filters is:

$$f_C = \frac{1}{2\pi RC}$$

Choosing the 3-dB frequency cutoff values to be 20Hz and 20kHz and plugging the appropriate values into the formula, the following values are achieved. **2.95μF** for C_{IN} and **169pF** for C_{OP} . For the implementation, Components valued **3.3μF** and **100pF** were chosen respectively.

For the power stage, the relevant formulas are as follows. ($R_1 = R_2 = R$)

$$v_{out} \approx v_{in}$$

$$i_{in} = \frac{2v_{in}}{(1+\beta)R}$$

$$i_{out} = \frac{v_{out}}{R_L} \simeq \frac{v_{in}}{R_L}$$

$$A_i = \frac{(1+\beta)R}{2R_L}$$

Referring to the formulas above, $R_1 = R_2 = R$ value was chosen to be **1.8kΩ**.

After determining the values of the components, the circuit was simulated in LTSpice and the results were checked against the calculations. Observing that the results were satisfactory, the circuit was prototyped on a breadboard. Finally, using the software EasyEDA, a PCB was designed. This PCB was later manufactured and the circuit was implemented on the PCB for the final time.

Results

In this section, the results of simulation, breadboard prototyping, PCB development, and final PCB implementation will be presented.

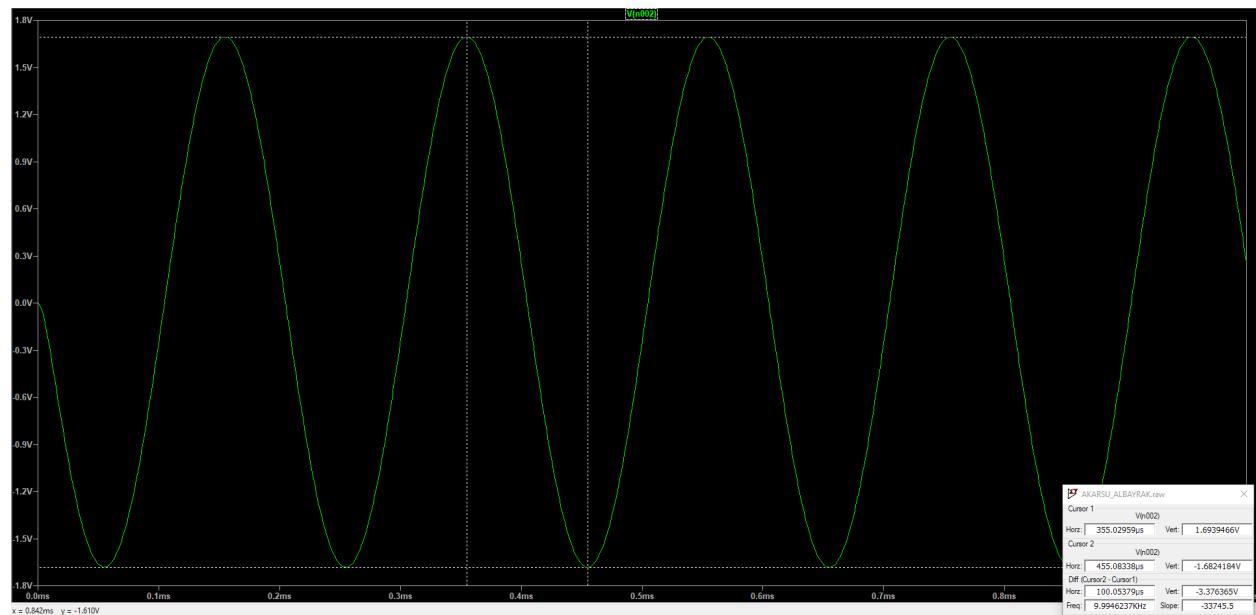


Figure 2: First gain stage output. ($3376 / 200 = 16.88$)

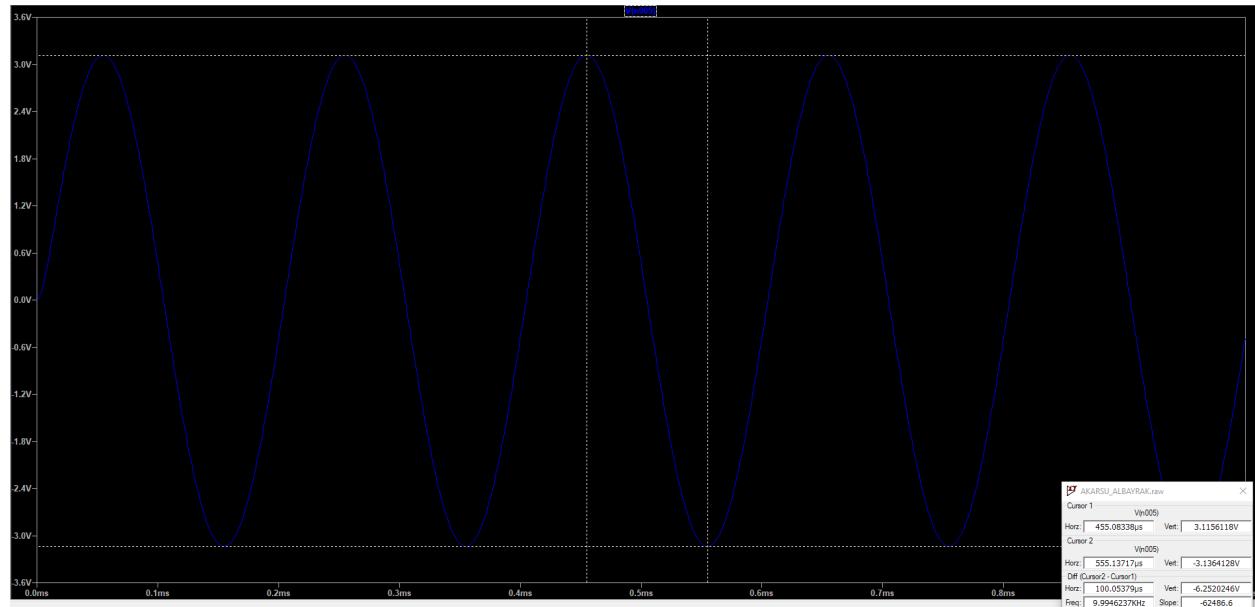


Figure 3: Second gain stage output. ($6252 / 200 = 31.26$)

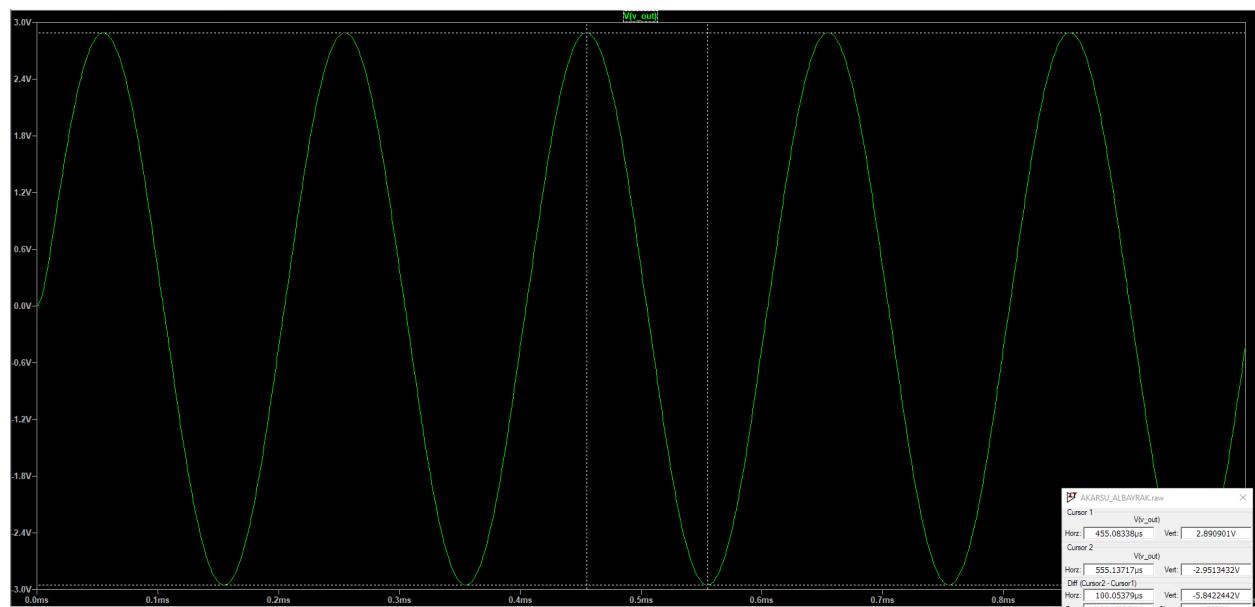
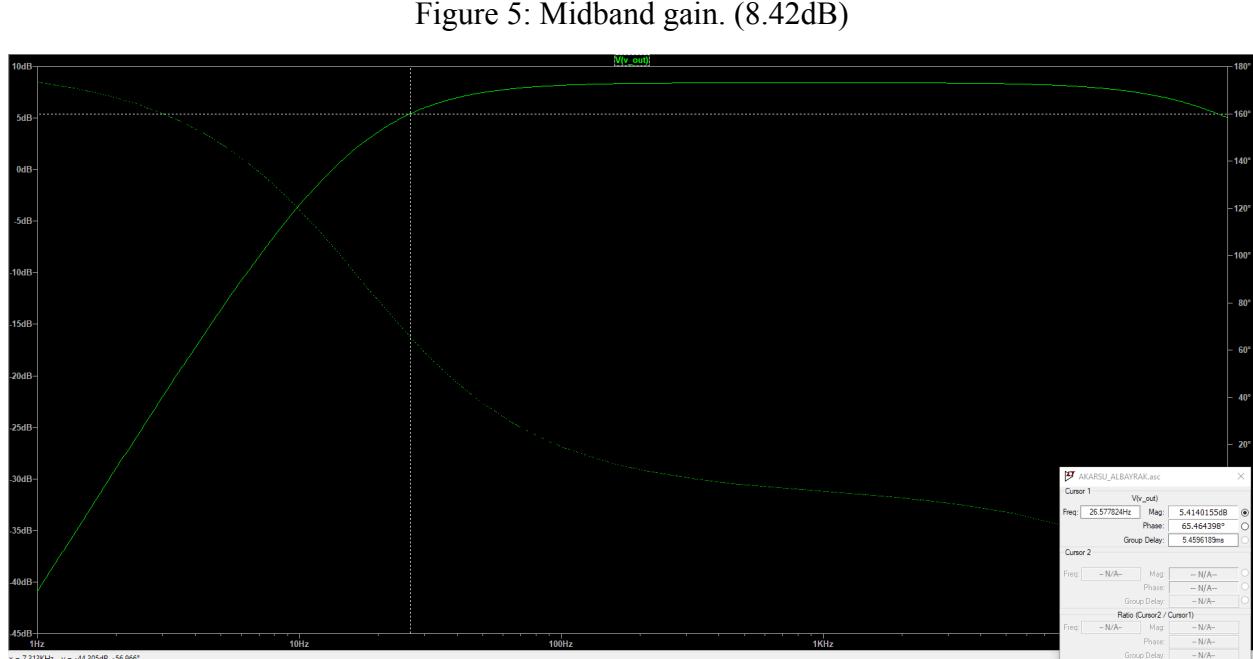
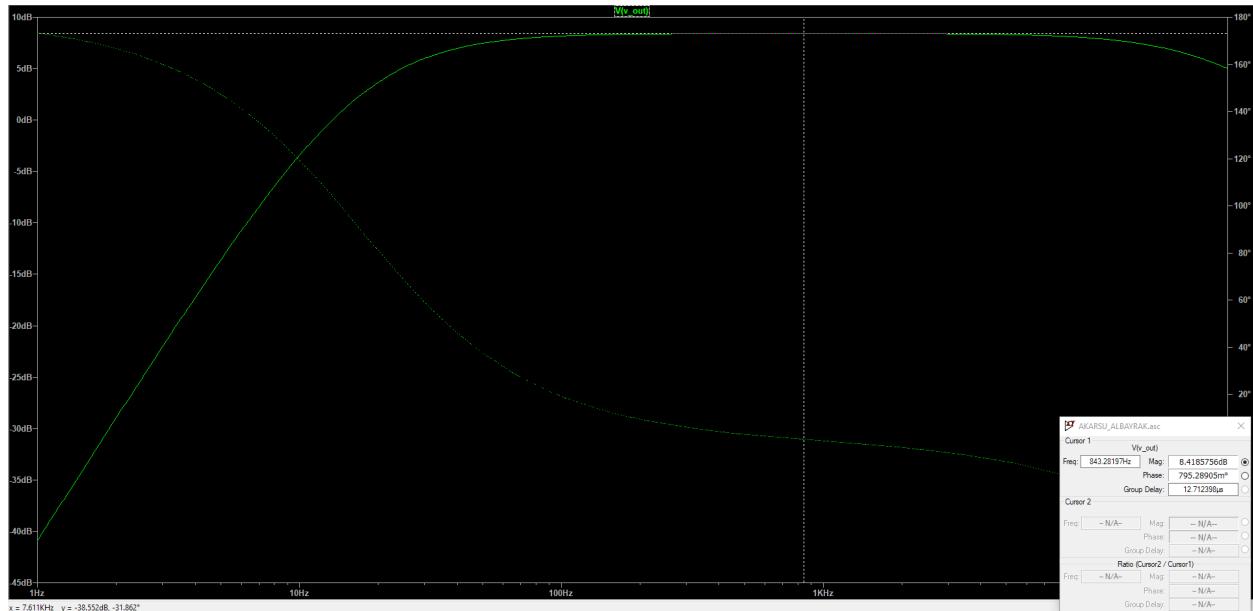


Figure 4: Power stage output. ($6252 / 200 = 29.21$)



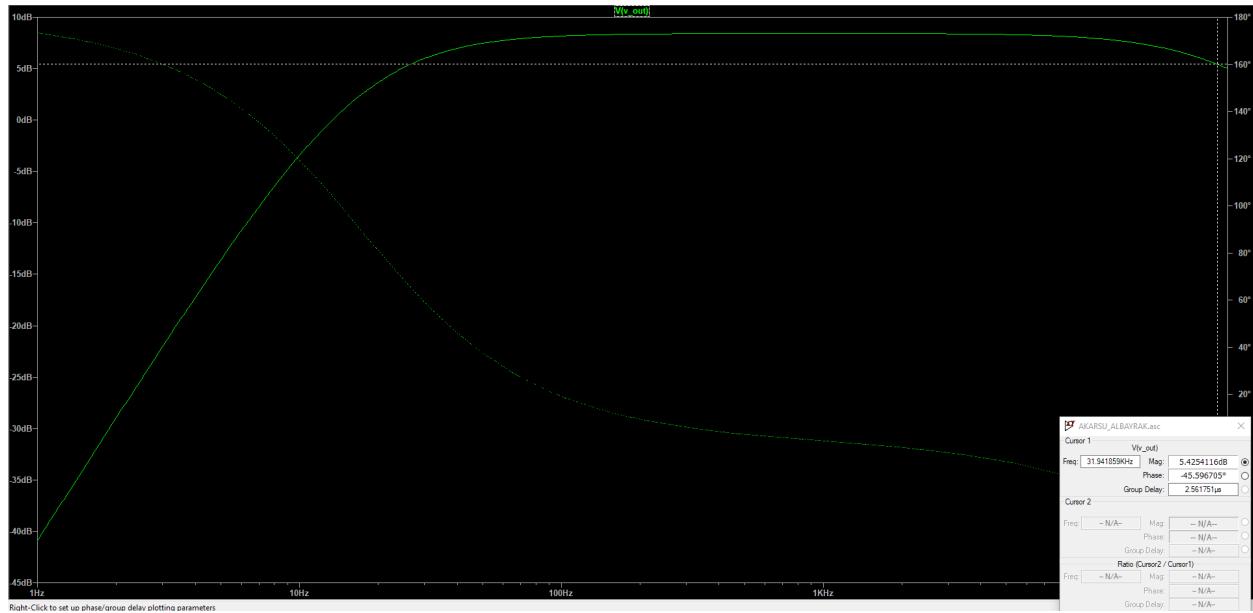


Figure 7: -3dB upper-cutoff frequency. (31.94kHz)

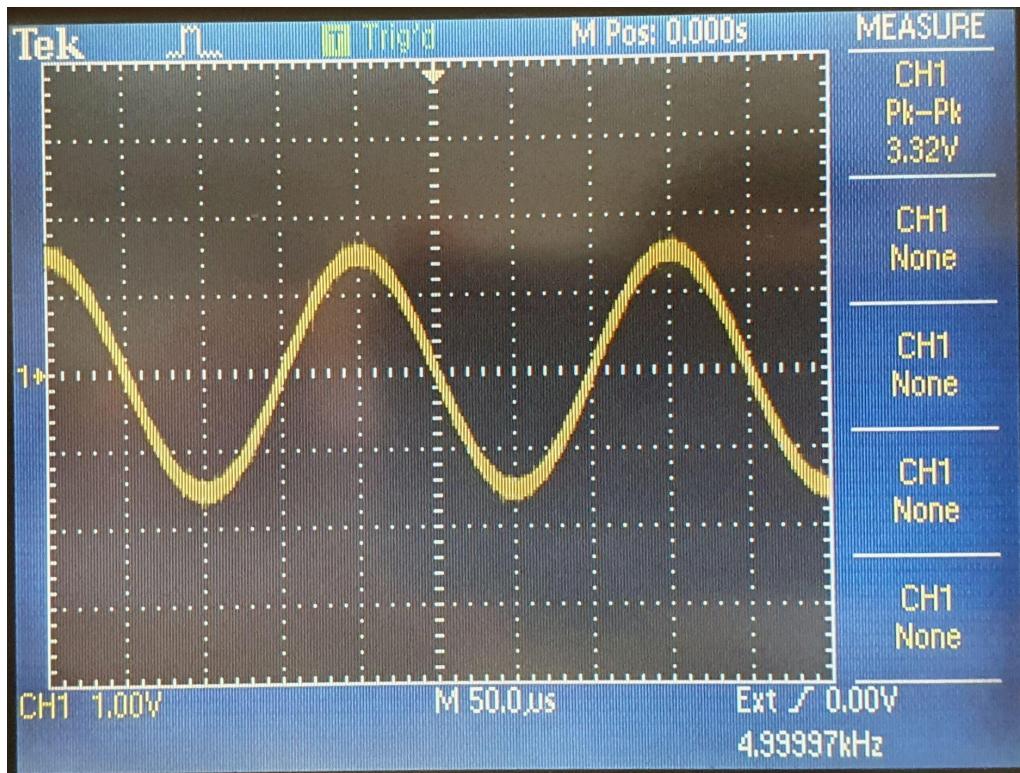


Figure 8: Breadboard first gain stage output. (3320 / 200 = 16.6)

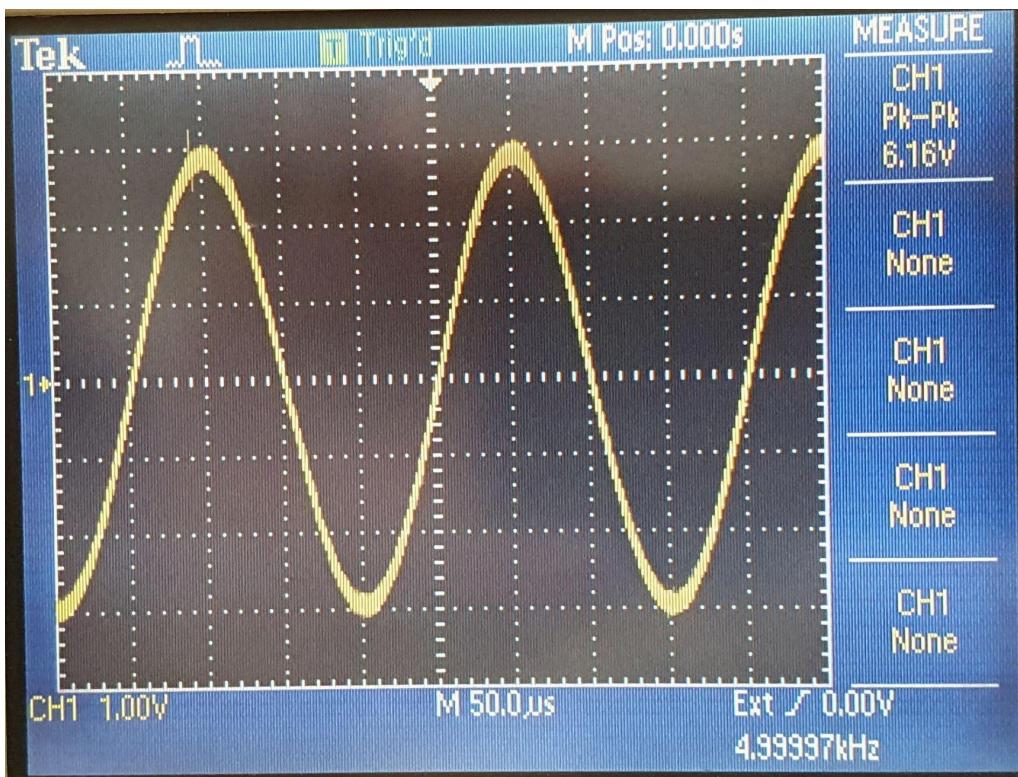


Figure 9: Breadboard second gain stage output. ($3320 / 200 = 30.8$)

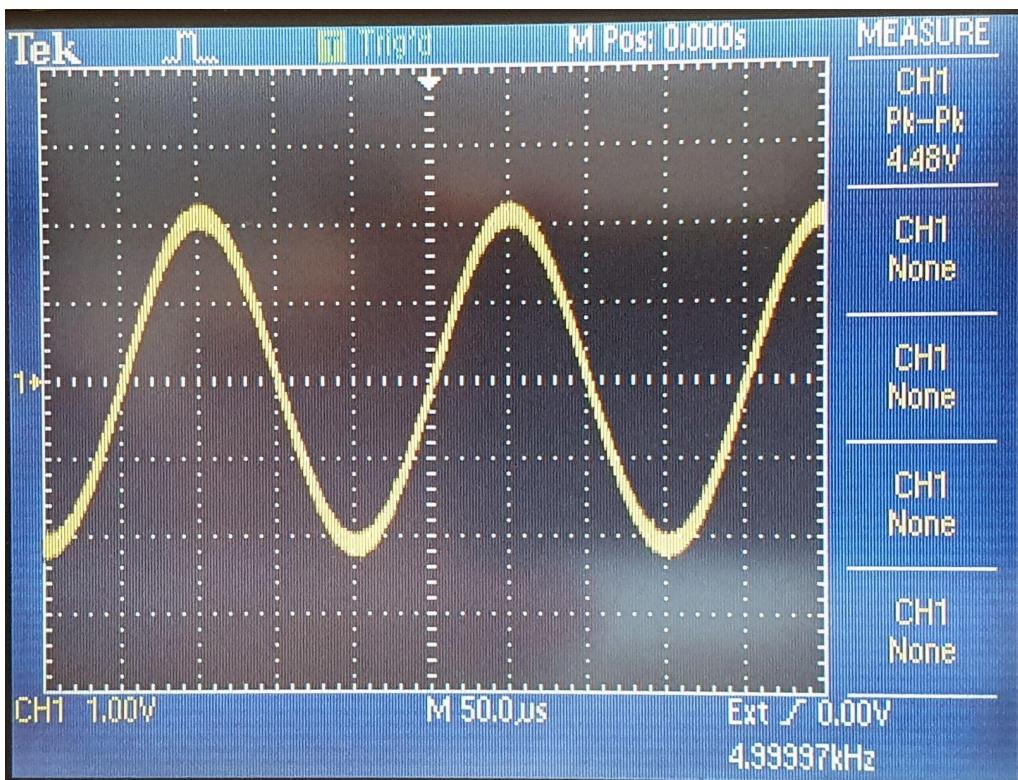


Figure 10: Breadboard power stage output. ($3320 / 200 = 22.4$)

The measurements for the figures 8, 9, and 10 are identical in the PCB implementation.

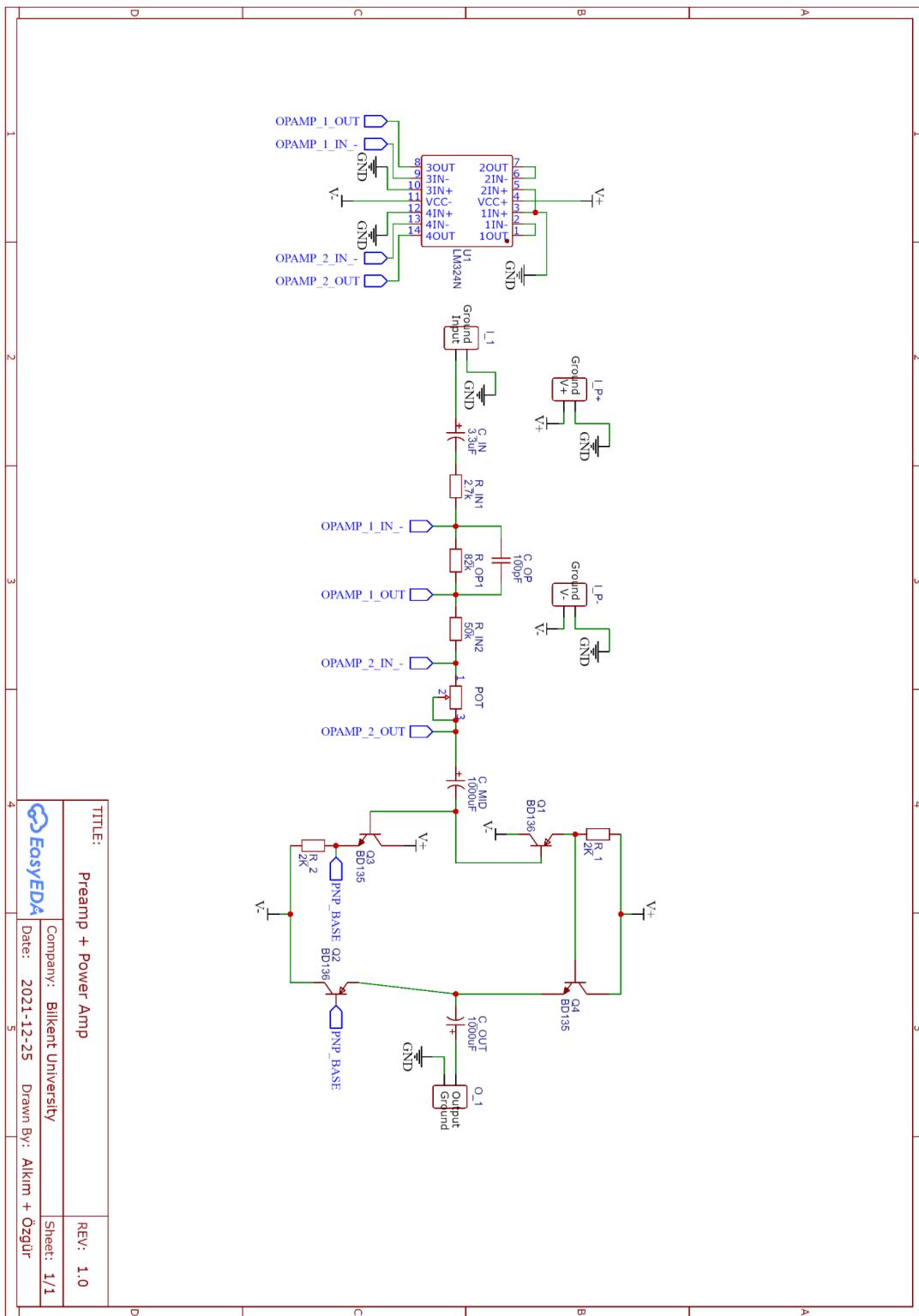


Figure 11: EasyEDA Schematic.

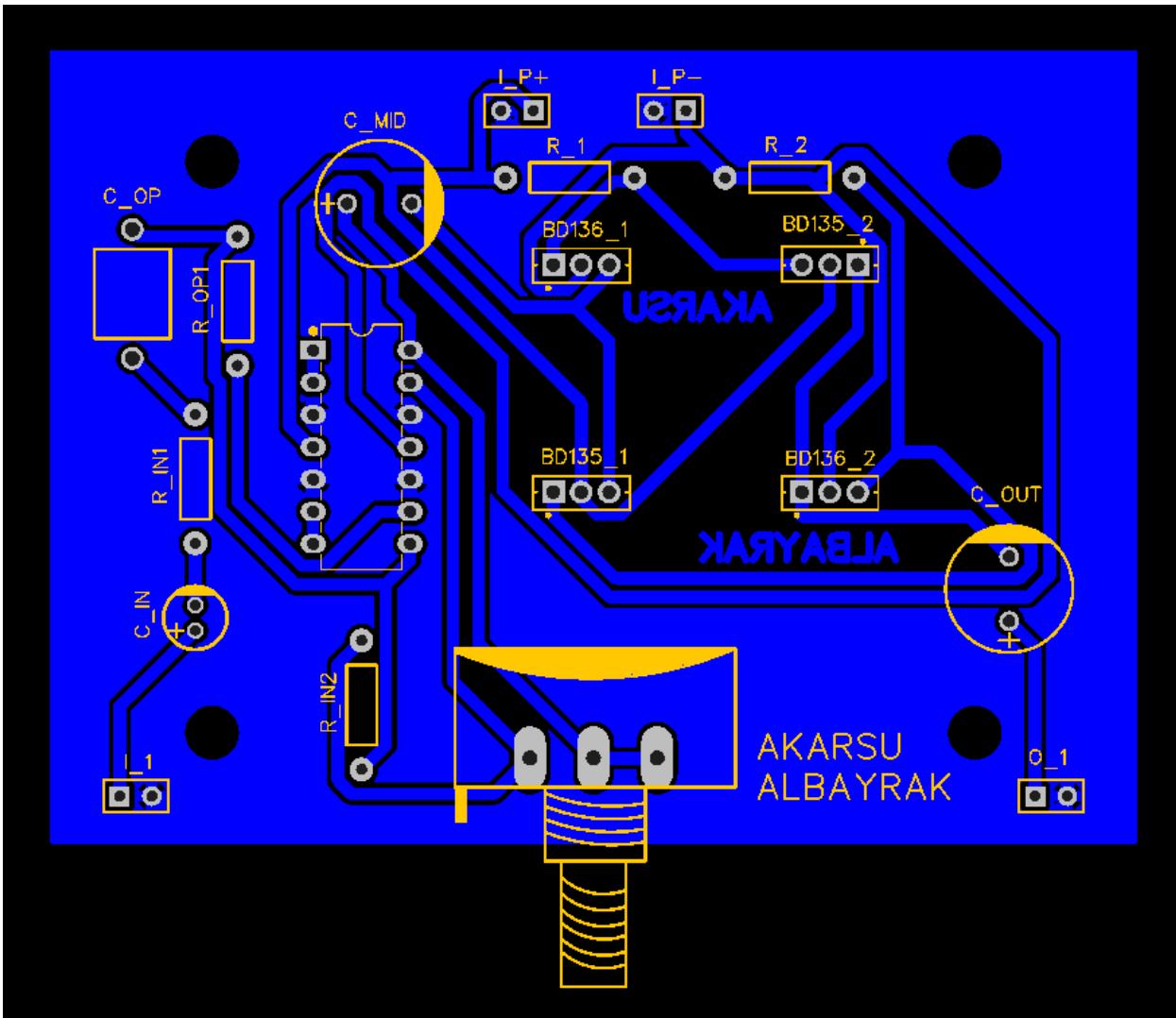


Figure 12: EasyEDA PCB design.

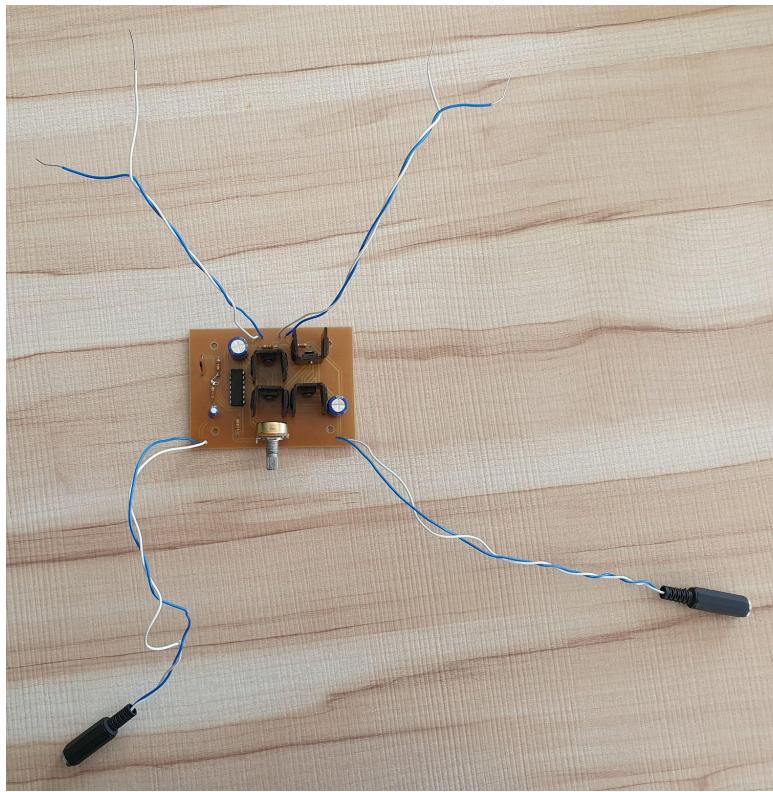


Figure 13: General view of the finished product.

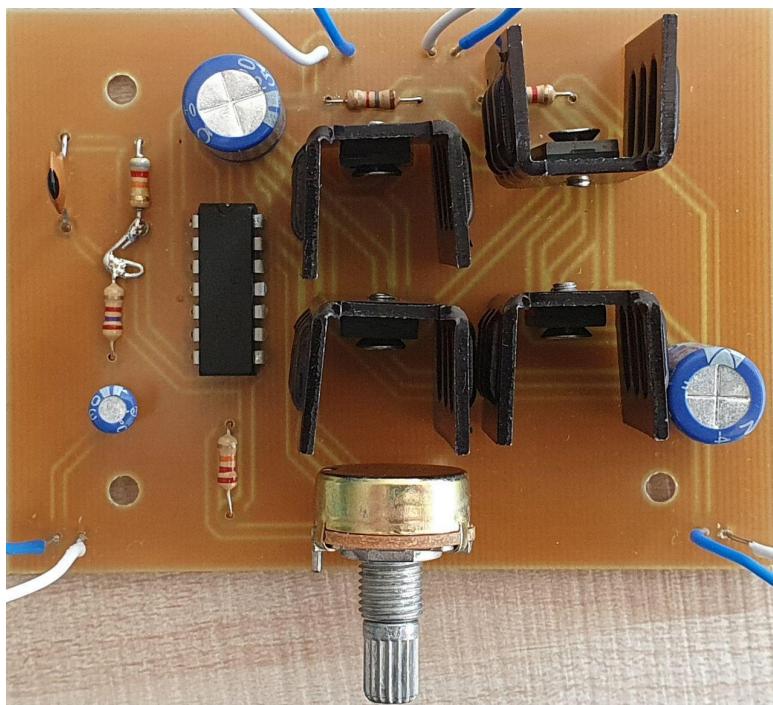


Figure 14: Close-up view of the PCB.

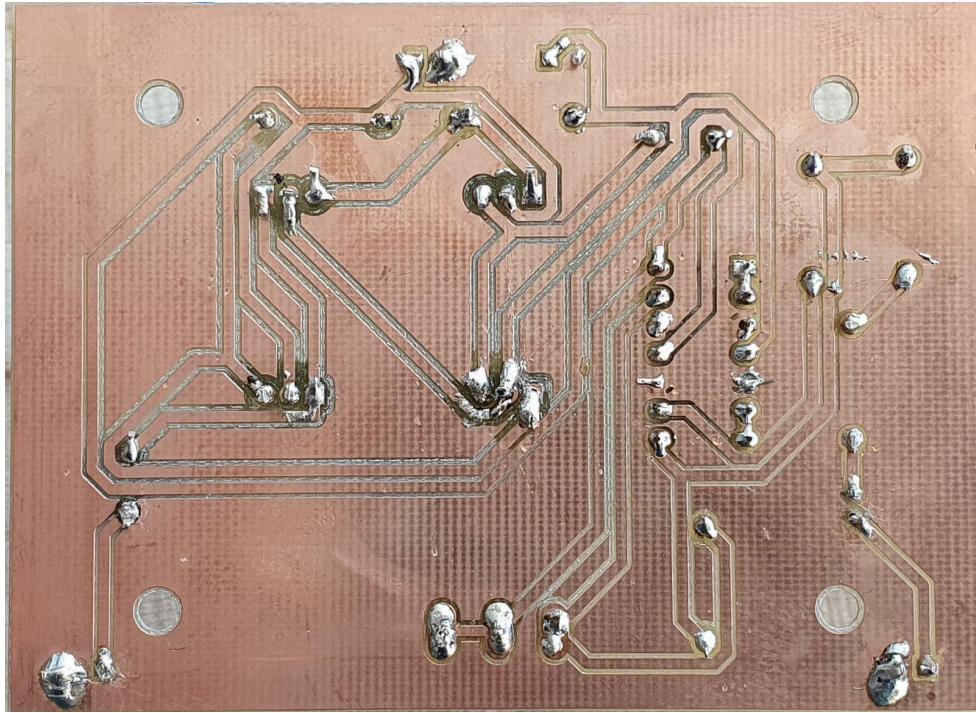


Figure 15: Close-up view of the back of the PCB.

Last names of the group members are present on the EasyEDA PCB design. However, they did not appear on the finished product. Figures 12 and 15 can be easily compared and understood as identical.



Figure 16: -3dB lower-cutoff frequency. (25Hz)



Figure 17: -3dB upper-cutoff frequency. (17kHz)



Figure 18: Harmonic content at 0.1Vpp input.



Figure 19: Harmonic content at 0.2Vpp input.



Figure 20: Harmonic content at 0.3Vpp input.



Figure 21: Harmonic content at 0.4Vpp input.



Figure 22: Harmonic content at 0.5Vpp input.

Conclusion

Some distortion can be observed in some of the figures. These distortions can be caused by transistor malfunction, overheating or other non-ideal factors. While working on the project, I gained experience about a wide variety of topics, especially practical implementation of amplifiers. The most enjoyable part of the project was the PCB design part. Listening to music via the amplifier I made was also very rewarding. I can definitely say that the final implementation of the amplifier worked as expected and performed very well. Although the pictures of the breadboard circuit is not available, it was seen - and given a check - by the TA responsible from this group. Also, the final check was given on the PCB and in a box.