Boost Integrated High Frequency Isolated Half-Bridge DC-DC Converter: Analysis, Design, Simulation and Experimental Results

by

Hossein Tahmasebi

B.Sc. in Electrical Engineering, University of Tehran, Iran, 1989

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ABSTRACT

Recently, there has been a growing interest in alternative energy sources because world energy crisis intensified and the growing demand of energy globally. Among the various alternative source of energy, solar power stands apart as it is a clean, abundant and unlimited source of energy. Photovoltaic (PV) systems generally use DC-DC boost converter structure to step-up the low voltage to a higher voltage level. This DC-DC converter will form the front-end of utility interfaced PV array converter system.

The performance of DC-DC converter has a direct impact on the conversion efficiency of PV system. This project report presents design, analysis, simulation and experimental results for a step-up dc-to-dc converter with high-frequency transformer isolation for use with photovoltaic array output.

After reviewing the literature and discussing pros and cons of the existing topologies we select a configuration that has maximum efficiency, minimum number of switches and simple structure. This converter has the advantages such as high-voltage conversion ratio, low input current ripple and soft switching for all switches. Then we analyze the selected converter and design it for the required specifications (rated power 400 Watts, 40 to 80 V input, 200 V output). In the next step we simulate the designed converter with PSIM simulation package. An experimental circuit is also built to verify the analysis and simulation. The simulation and experimental results show that for the whole input voltage range the converter works in ZVS from full load to light load.

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List of Symbols

C_1 and C_2	DC bus capacitors
C_3 and C_4	Output filter capacitors
C_{oss}	POWER MOSFET output capacitance
C_{S1} and C_{S2}	Snubber capacitors
D	Duty ratio
D_1 and D_2	Anti-parallel diodes of POWER MOSFET
D_3 and D_4	Output rectifier diodes
D_{max}	Maximum duty ratio
D_{min}	Minimum duty ratio
f_s	Switching frequency
i_{C3}, i_{C4}	Capacitor currents
i_{D1}, i_{D2}	POWER MOSFET antiparallel diode currents
i_{D3}, i_{D4}	Output rectifier diode currents
$I_D(max)$	Maximum drain current of POWER MOSFET
I_{in}	DC input current
i_{in}	Instantaneous input current
$i_{in}(av)$	Average input current
$i_{in(\max)}$	Maximum input current
$I_{in}(max)$	Maximum DC input current
$i_{in(\min)}$	Minimum input current
$I_{in}(min)$	Minimum DC input current
i_{lk}	Leakage inductance current
$i_{LK}(+pk)$	Positive peak value of leakage inductance current
$i_{LK}(-pk)$	Negative peak value of leakage inductance current
I_o	Output current
i_{S1}, i_{S2}	MOSFET drain current
L_{in}	Input boost inductor
L_k	Leakage inductance of HF transformer

n	Transformer secondary to primary turns ratio
N_p	Transformer primary turns
N_s	Transformer secondary turns
P_{in}	Input power
P_{loss}	Converter power loss
P_o	Output power
$R_{DS(on)}$	Static drain-source ON resistance of POWER MOSFET
S_1 and S_2	Power switches
T	Switching period
Tr	Transformer
V_{C1}, V_{C2}, V_{C3} and V_{C4}	Capacitor voltages
$V_{DS}(max)$	Maximum drain source voltage of POWER MOSFET
v_{gs1}, v_{gs2}	Gating signals
V_{in}	Input voltage
v_{Lin}	Input boost inductor voltage
V_o	Output voltage
v_p	Transformer primary voltage
v_s	Transformer secondary voltage
v_{S1}, v_{S2}	Voltage across POWER MOSFET switches
Δi_{in}	Input ripple current
η	Efficiency

List of Abbreviations

AC	Alternating Current
CFMRC	Current Fed Multi-Resonant Converter
DC	Direct Current
EMC	Electro-Magnetic Compatibility
HF	High Frequency
LC	Inductor Capacitor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPPT	Maximum Power Point Tracking
PV	Photovoltaic
PWM	Pulse Width Modulation
SPRC	Series-Parallel Resonant Converter
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

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I would like to express my honest gratitude to my supervisor Dr. Ashoka K. S. Bhat for supporting towards my Masters of Engineering project. His assistance directed me in research, design and implementation of my project.

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Dedication

This work is dedicated to my wife and sons.

Chapter 1

Introduction

Review of high efficiency high step-up isolated DC/DC converters for photo voltaic applications

This project report presents design, analysis, simulation and experimental results for a step-up dc-to-dc converter with high-frequency transformer isolation for use with photovoltaic (PV) module output. This dc-to-dc converter will form the front-end of utility interfaced PV array converter system.

Layout of this Chapter is as follows: Section 1.1 gives an introduction to this chapter. In Section 1.2 we review some configurations of step up dc-to-dc converters with transformer isolation. In Section 1.3 we summarize the various topologies that are discussed in 1.2 and in Sections 1.4 and 1.5 the selected converter and its specifications are given. Objectives and chapter layout of the project report are given in Sections 1.6 and 1.7, respectively. Finally a conclusion of this chapter is presented in Section 1.8.

1.1 Introduction

High gain DC/DC converters are the key part of renewable energy systems (Figs.1.1, 1.2). The designing of high gain DC/DC converters is imposed by severe demands. Designers face contradictory constraints such as low cost and high reliability. First of all the inverters must be safe in terms of further maintenance as well as in relation to the environment. Since the renewable sources can be utilized for many years the converter designers cope with long time reliability issues. The main problem for the operator is to maximize the energy yield and to minimize the maintenance. For these reasons the converters must be distinguished by high efficiency over wide input power and voltage range. High voltage gain (usually tenfold) is required to produce sufficient DC bus voltage level. Additionally they should operate at wide temperature range expressing low EMC emission and be immune to environmental conditions. Such demands create severe constraints for DC/DC boost converter designing which are key

parts in terms of efficiency of overall renewable energy systems. The majority of commonly used renewable energy sources deliver electric power at the output voltage range of 20 VDC to 70 VDC. To adjust it to the electric grid standards that voltage should be boosted to the system DC Bus voltage of around 200 VDC or 400 VDC depending on the grid requirements (Fig. 1.2). Power conditioning can be accomplished by high efficiency high voltage gain step-up DC/DC converters. In this chapter major topology types of step-up DC/DC converters will be reviewed.

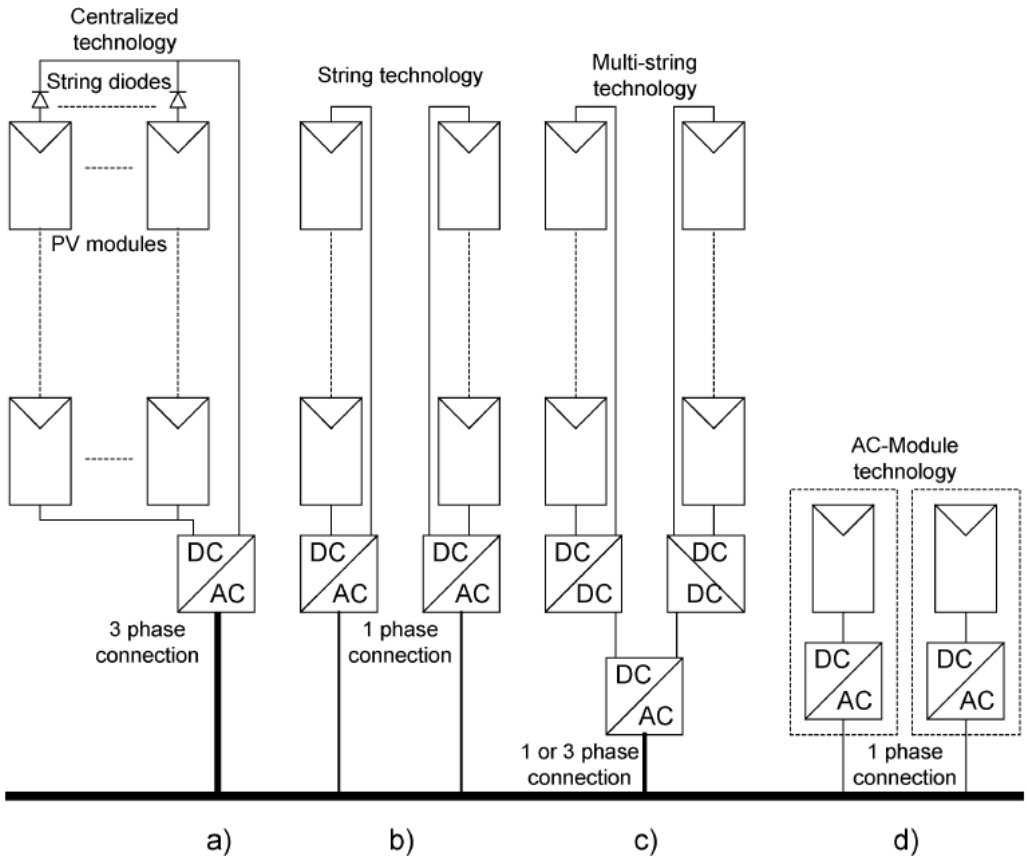


Fig. 1.1 Historical overview of PV inverters (Copied from Fig. 3 of [1]). (a) Past centralized technology. (b) Present string technology. (c) Present and future multi-string technology. (d) Present and future ac-module and ac cell technologies.

In the past one centralized inverter was responsible for connecting several modules or other renewable energy sources into the grid. The PV modules were divided into series connections, so called strings. Each module was generating high voltage sufficient to avoid further amplification (Fig. 1.1a). At the moment, string technology is dominating. Centralized technology has been replaced and two standards are currently used. The first technology comprises separate strings attached to one DC/AC inverter connected directly to the grid (Fig. 1.1b). The sub-type of string

technology is called multistring technology (Fig. 1.1c) with separate DC/DC converter that supports a panel or panel structure. Then DC/DC converter is attached to the DC/AC inverter which is coupled to the grid (1-or 3-phase). The string inverter is nothing but the reduced version of the technology seen on (Fig. 1.1a) – one string corresponds to a single inverter. While technologies (1.1b), (1.1c) and (1.1d) are currently used, a better choice seems to be a multi-string (1.1c). Since every string can be controlled individually thus the solar panels can be utilized more efficiently. This provides greater flexibility and facilitates the control and occasional replacement of individual panels. On Fig. 1.1d we can see the synthesis of the inverter and PV module into one electrical device. This technology has only one PV module so individual Maximum Power Point Tracking (MPPT) system for each inverter is needed [2]. Expandability of the system and opportunity to become a "plug-and-play" device is undoubtedly part of the benefits. There are no bypass or string diodes necessary. Each panel in this structure has its own MPPT controller which maximizes the power production.

Module structure Fig. 1.1d has one major disadvantage which is low efficiency due to high voltage amplification, so the price per watt is the largest of the four topologies discussed.

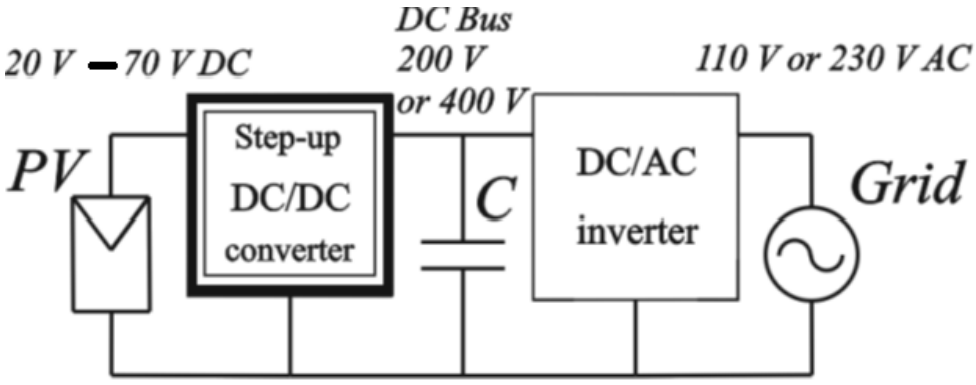


Fig. 1.2 The example of PV inverter with integrated DC/DC step-up converter (Copied from Fig.5 of [1]).

1.2 Review of Some DC-DC Step-Up Converters with Transformer Isolation

Transformers have significant influence on efficiency of whole energy conditioning system and hence on the quality of energy supplied to the network. The absence of transformer in the

system may result in injecting DC currents into AC current, which may disturb the operation of electric grid distribution transformers due to saturation of magnetic cores. Moreover the absence of active elimination of unwanted DC currents injected to the grid can lead to distribution transformers damage and whole electric grid failure. According to the electrical regulations and standards which are in place in some countries the galvanic isolation of the PV system may be necessary or not. It is performed by the transformers of high or low frequency. Galvanic isolation can be accomplished by either line frequency transformer or a high frequency one. Both are shown in Fig. 1.3. The grid frequency transformer (50/60 Hz) is not often used because of high price, high volume, high weight and low power efficiency.

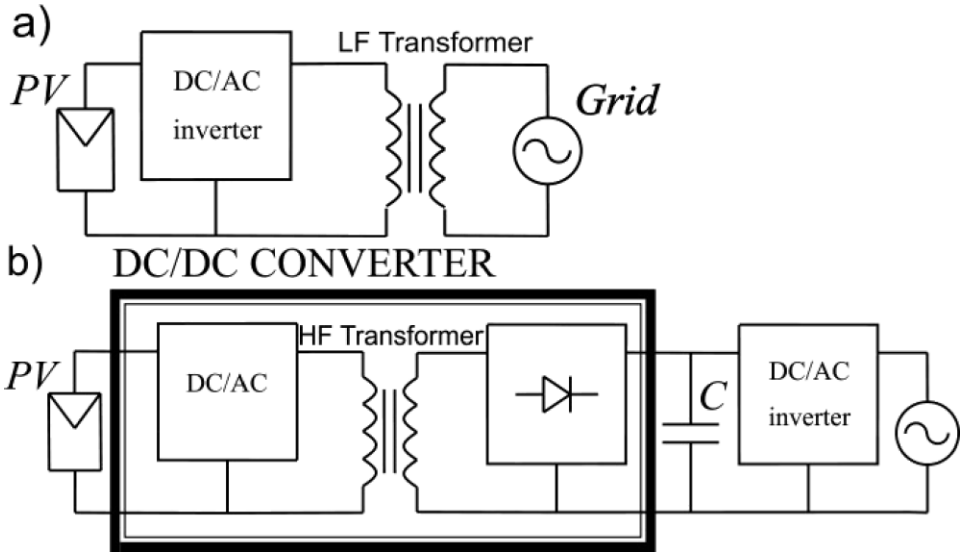


Fig. 1.3 Types of transformer isolation (Copied from Fig. 3 of [3]) (a) Low frequency transformer. (b) High frequency transformer.

For the reasons listed above the focus of this project report is on the topologies using high frequency transformers. These topologies can be divided into two main groups: hard switched and soft switched converters.

1.2.1 Isolated Step-Up Hard Switched Converter Topologies

Among power electronics converters with galvanic isolation there are several hard switched topologies, which are the starting point for further investigations and designing more advanced systems. Topologies such as flyback, forward or push-pull, and their variants have been described in detail in the literature [3]. The voltage step-up obtained in these systems is high,

unfortunately, does not go hand in hand with efficiency. Only by applying ZVS, ZCS soft switching techniques, these systems can achieve a satisfactory efficiency.

1.2.2 Isolated Step-up Soft Switched Converter Topologies

Unfortunately due to switching losses the efficiency of hard switched converters is low. That is why in this section we consider soft switching converters. Some of the selected converter configurations are discussed in the following paragraphs.

(a) Active clamp step-up converter:

The active clamp step-up DC/DC converter [4], (Fig. 1.4) has the advantages of both flyback and forward converters. It regulates the DC link voltage providing high voltage conversion ratio. The active clamp high step-up DC/DC converter unlike the conventional flyback and forward DC/DC converters uses the active-clamp circuit both in ON-state and OFF state so the input power is delivered to the output in both these states.

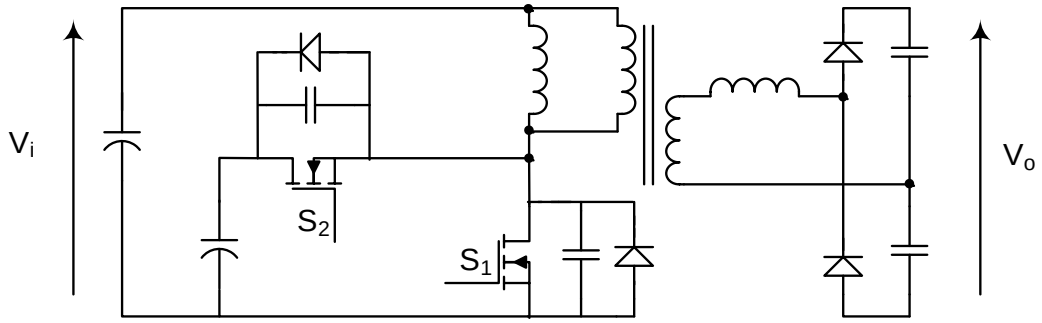


Fig. 1.4 Active clamp step-up converter [4].

Both positive and negative input voltages are injected to the resonant tank and thanks to the voltage doubler the transformer's winding ratio can be decreased. This feature allows providing only half of the distribution line voltage on the transformer's secondary winding. Thanks to the resonance of leakage inductance of the transformer and capacitors paralleled with the rectifier diodes the reverse-recovery loss of these diodes can be eliminated which, combined with an active-clamp circuit for soft switching of the MOSFET transistors ensures high system efficiency.

(b) Resonant push-pull current fed converter:

The high step-up resonant push-pull current fed converter [5] depicted in Fig.1.5 has advantages of a conventional current-fed push-pull converter such as low input current stress, high voltage conversion ratio and low conduction loss of switches. Thanks to LC resonance output diodes can commutate softly without the reverse recovery problem. Mentioned features together with high efficiency and low current ripples of the inductor make that converter appropriate to use in photovoltaic systems.

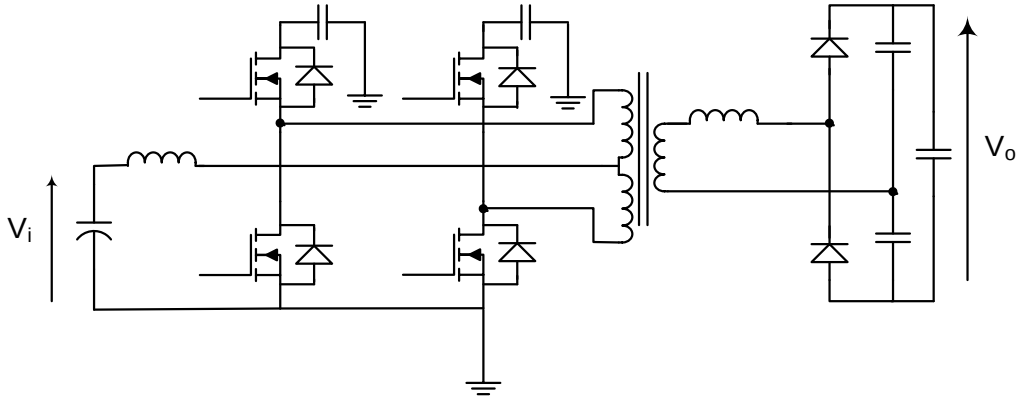


Fig. 1.5 Resonant push-pull current fed converter using active clamp circuit [5].

(c) High step-up zero-voltage switching current-fed converter:

Although the efficiency of the system seems to be the most important parameter distinguishing the converter in many cases, the designers also strive to simplify the control system. Example of this is high step-up ZVS current-fed DC/DC converter [6] shown in Fig. 1.6. Apart from ZVS condition of the main and auxiliary active switches (snubber) only one PWM control signal is connected to the pair of transistor gates. The pairs consisting of a main transistor in bridge leg and the auxiliary one from other leg are alternated in conduction during one switching period.

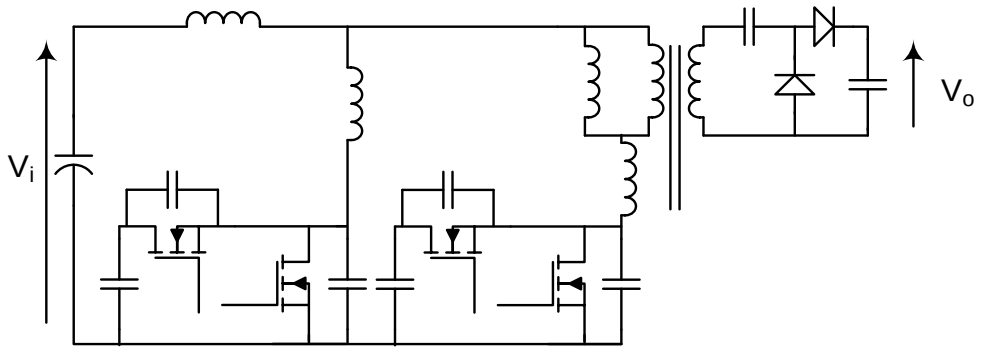


Fig. 1.6 High step-up zero-voltage switching current-fed converter [6].

(d) Series resonant half-bridge converter:

ZVS condition in half-bridge resonant converter [7] seen in Fig. 1.7 is achieved by connecting capacitor C_r in series with transformer leakage inductance and external inductor forming a resonant tank which can be tuned to the switching frequency by choosing appropriate capacitance. Apart from that high efficiency is achieved by the use of capacitive snubbers connected in parallel with the MOSFET switches, they can be switched in zero voltage (provided that switching frequency is greater than resonance frequency). The diodes of the rectifier are switched at zero current. As the switching losses are negligible only the conduction losses dominate.

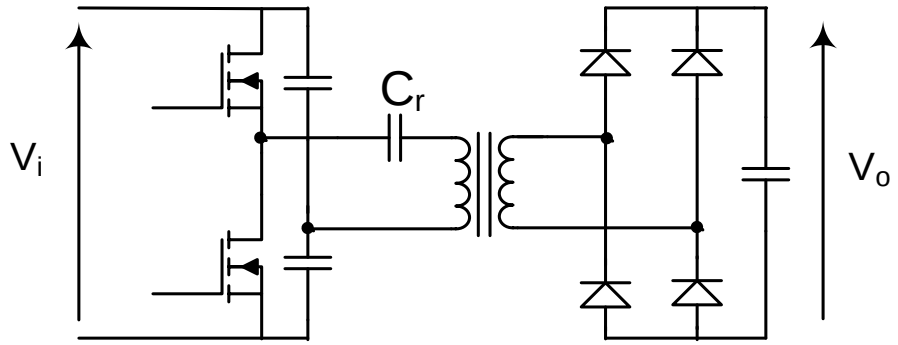


Fig. 1.7 Series Resonant half-bridge converter [7].

(e) Current fed dual half-bridge resonant converter:

Figure 1.8 shows ZVS two-inductor boost converter [8] for low voltage, high current DC to DC conversion. During turn off of the transistor the parallel capacitor C_1, C_2 resonates with inductor L_r thus turning on of the transistor occurs when voltage of the capacitor equals zero. Interesting is the fact that the resonant inductance L_r and capacitors C_1, C_2 may be physical or they can be replaced by the transformer leakage inductance and the MOSFET switch parasitic capacitances. Despite the high voltage gain, system efficiency is still high. Consequence of this topology is its multi-resonance variant with voltage doubler.

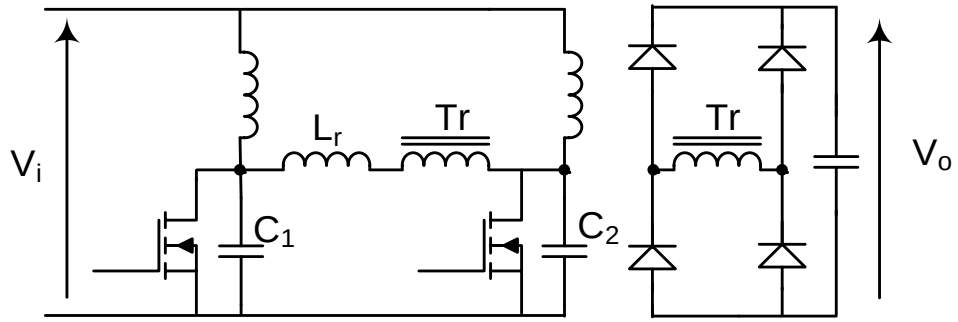


Fig. 1.8 Current fed dual half-bridge resonant converter [8].

(f) Current fed multi-resonant converter (CFMRC):

Figure 1.9 consists of a current fed two inductor half-bridge structure [9] followed by transformer with multi resonant tank and an output full bridge rectifier. However the secondary winding losses of the transformer which go together with high turns-ratio may limit the efficiency. Even though that converter demonstrates the number of advantages such as high voltage gain, low input ripple current and ZCS of bridge diodes the improved CFMRC topology was further developed [10]. In this converter voltage doubler was implemented to reduce the turns-ratio of the transformer. Therefore the cost of the transformer can be reduced (Fig. 1.10).

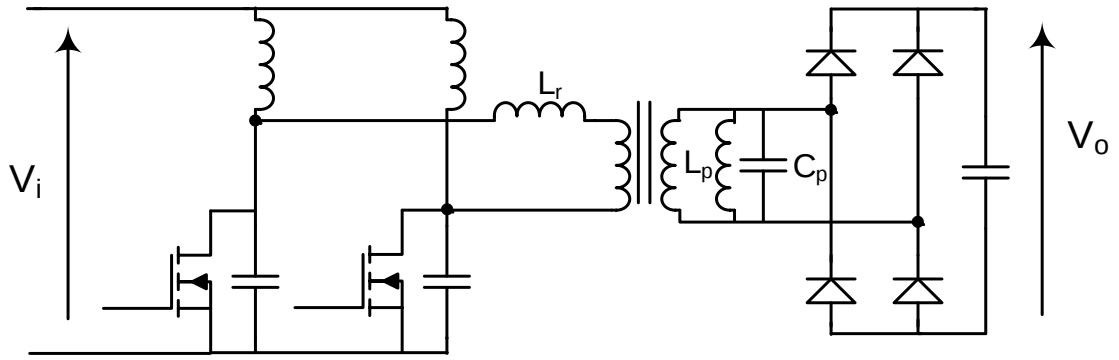


Fig. 1.9 Current fed multi-resonant converter with full-bridge rectifier [9].

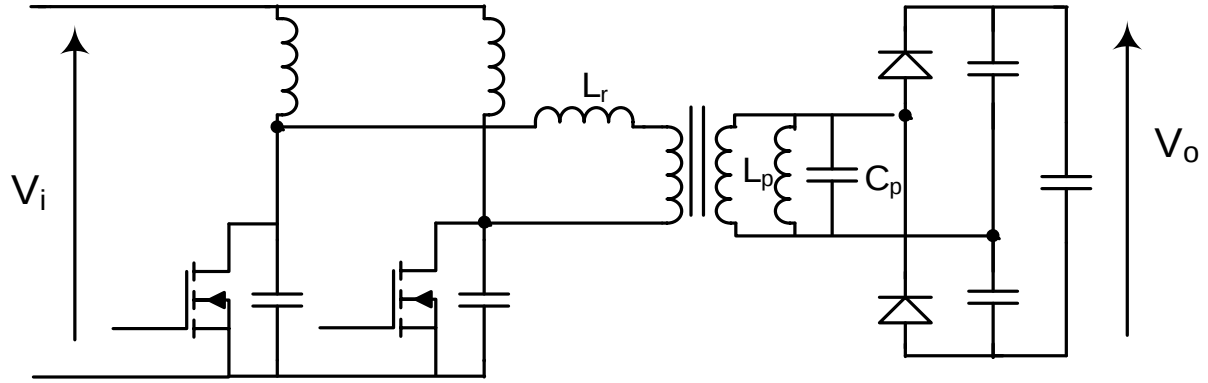


Fig. 1.10 Current fed multi-resonant converter with voltage doubler [10].

During switching period the overlapping of the signals driving two main switches is present resulting in resonance between leakage inductor L_r and resonant capacitor C_p . The ZVS condition of the half-bridge transistors is achieved and voltage spikes within converter are reduced. The power losses in semiconductor components are reduced also by ZCS of voltage doubler diodes. They are turned off at zero current in full load condition and during lighter load the primary current is limited. The common ground gate driving is also undoubted advantage of half-bridge current-fed converters.

(g) Series-parallel resonant converter (SPRC) or LCLC-type:

This converter [11] is depicted in Fig. 1.11. In this topology square wave generator (full bridge inverter) is linked with half bridge rectifier by high step-up high-frequency transformer.

Due to resonance bridge MOSFET transistors are zero voltage-switched and voltage doubler diodes are turned off at zero current. Mentioned features as well as half-bridge diode snubbers contribute to high efficiency of the system. There is a possibility to use series-parallel resonance feature both in single as well as in the three-phase converters through variable number of inverter and rectifier legs.

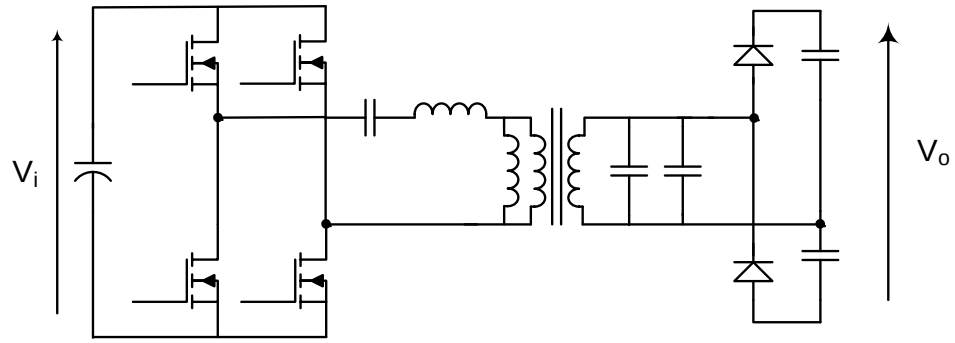


Fig. 1.11 Series-Parallel (LCLC-type) Full-bridge Resonant Converter [11].

(h) Soft-switching boost integrated half-bridge converter:

Figure 1.12 shows the soft switching boost integrated half bridge converter [12]. This topology is a combination of boost and half bridge converters. The converter is obtained by integrating a boost converter with a half-bridge dc-dc converter. The circuit composed of a boost inductor, two active power switches S_1 and S_2, divided capacitors C_1 and C_2, two winding high frequency step up transformer and voltage-doubler rectifying circuit. Switch S_1 is shared by the boost stage and the half-bridge converter.

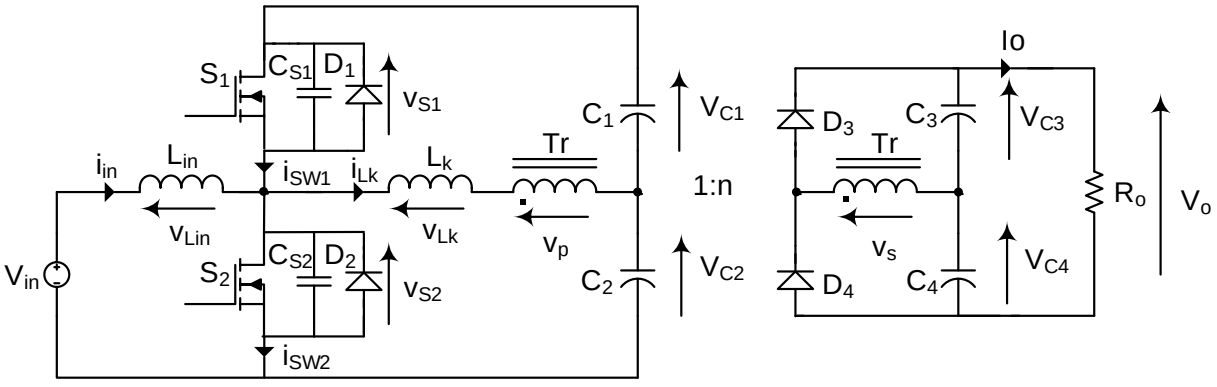


Fig.1.12 Integrated boost half bridge DC-DC converter [12].

This converter has the advantages of high voltage gain and high efficiency using a relatively small number of semiconductor components.

(i) Two transformer converter:

In topologies presented so far the isolation was provided by one transformer, which simultaneously ensures the voltage gain. In high step-up converter seen in Fig. 1.13 two transformers are utilized to double the voltage conversion ratio [13]. Distributed magnetic components not only lower the power losses and thermal stresses of the converter but also reduce transformer turns ratio. Resonance of the leakage inductances of the transformers and series connected capacitors in the voltage doubler makes the output diodes to be turned off at zero-current. This two series-resonant circuits and active clamping of the switching transistor ensure high efficiency.

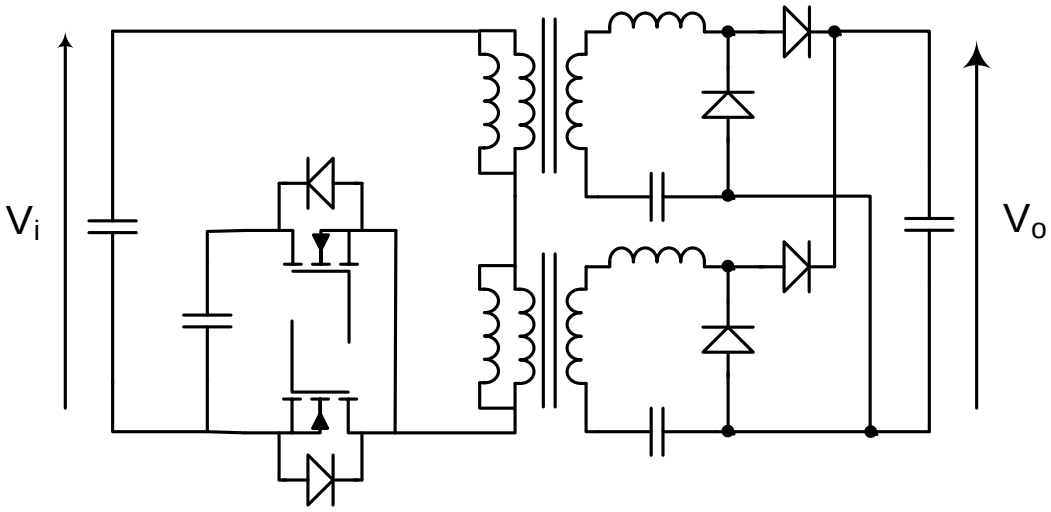


Fig. 1.13 High step-up two transformer converter [13].

1.2.3 Summary of Transformer Isolated Converters

Table 1.1 presents the summary of high-frequency transformer based step-up converters discussed above.

Table 1.1 Summary of DC/DC converters with high-frequency transformer isolation

Fig.	Ref.	η_{max} (%)	P_{max}(W)	f_s(kHz)	V_i(V_{dc})	V_o(V_{dc})	No. of Switches	No. of Diodes
4	4	96	1000	50	30-60	350	2	2
5	5	97	1500	70	35-60	350	4	2
6	6	92	400	100	45	200	4	2
7	7	---	250	100	36	430	2	4
8	8	90	85	1000	20	360	2	4
9	9	95	150	255	20-33	350	2	4
10	10	96	150	255	23	350	2	2
11	11	97	190	215	20-35	700	4	2
12	12	98	210	---	30-50	----	2	2
13	13	97	260	---	36	----	2	4

1.3 Summary

Different step-up DC/DC topologies have been presented in previous section. However the solution chosen by the designer depends on particular design constraints which are a need to determine the most robust and best performance topology. High efficiency of step-up DC/DC converters can be achieved by decreasing duty cycle (lower conduction losses) and reducing voltage stress on switches (cheaper and lower $R_{DS(on)}$ switches) applying soft switching technique (minimizing switching losses) and utilizing active clamp circuits (recycling the energy stored in parasitic inductances). Below there are a few distinguishing solutions presented. Half-bridge and full-bridge step-up topologies based on low $R_{DS(on)}$ MOSFET transistors with soft switching technique implemented demonstrate the highest efficiency. LLCC converter [11] is a good example of converters that merges the requirements of high efficiency and voltage gain. CFMRC is another distinguishing high performance topology [10] where a multi-resonant circuit eliminates parasitic parameters of transformer assuring high voltage gain. The presence of voltage doubler allows using lower turns-ratio transformers thus reduces overall cost of the system. Other advantage of that topology is that both switches work on low-side. In [13] even

though two transformers are in use the voltage gain and efficiency are still excellent. Basic topology such as push-pull converter with additional snubbers and voltage doubler [5] can be competitive solution among the other more advanced topologies.

1.4 Selected Converter

The selected converter is shown in Fig.1.14. This selection is based on maximum efficiency, minimum number of switches and simplicity of the configuration. This converter has the advantages such as high-voltage conversion ratio, low input current ripple and low conduction loss of switches. In the next chapter we will analyze the converter and find the design equations.

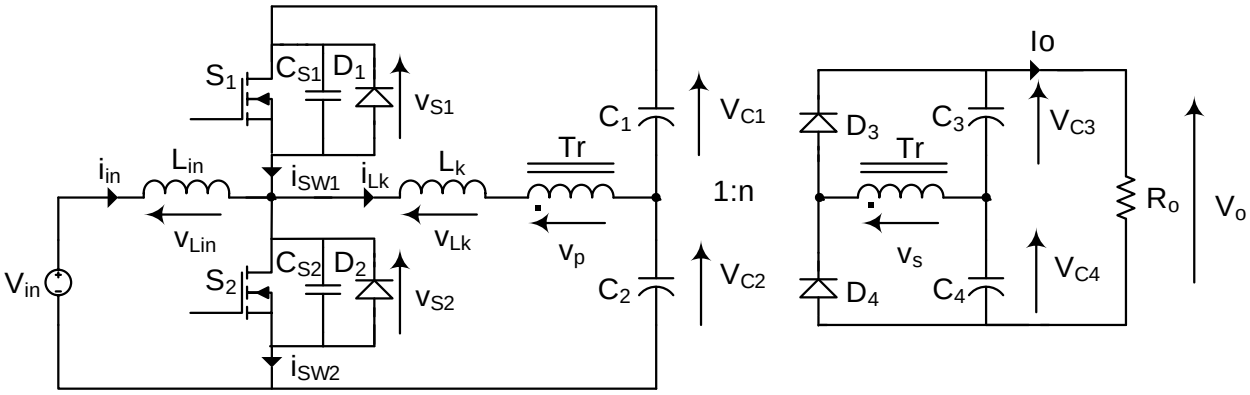


Fig. 1.14 Boost Half Bridge DC-DC Converter [12].

1.5 Specifications

The specifications of the converter to be designed are:

V_{in} = 40 to 80 V_{dc}

V_o = 200 V_{dc}

P_o = 400 W

f_s = 50 KHz

Output voltage ripple = 5%

Output voltage variation = 5%

Load Variation 10%---100%

High frequency isolation between input and output

Load is 120V 60Hz PWM Inverter

Solar Module Specification is given in the Appendix 2.

1.6 Objectives

The objectives of this project are to present the operation, analysis, design, simulate and build an experimental prototype of a dc to dc converter for photovoltaic application.

1.7 Chapter Layout

The layout of the project report is as follows: in the first chapter we reviewed some configurations of step up dc to dc converters with transformer isolation and selected the best configuration. In the second chapter we will analyze and design the selected configuration. In the third chapter the simulation and experimental results will be given and in the last chapter we will give conclusions and suggestions for future work.

1.8 Conclusion

In this chapter we reviewed and summarized some configurations of step up dc to dc converters with transformer isolation and based on our discussion and the specifications of the converter we selected the best configuration.

Chapter 2

Analysis and Design of the Converter

In this chapter we analyze and design a step-up dc-to-dc converter with high-frequency transformer isolation for use with photovoltaic (PV) module output.

2.1 Introduction

A step-up converter (Fig. 2.1) obtained by combining a boost converter with a half-bridge high-frequency (HF) transformer isolated dc-dc converter was realized in [12,14,15] for PV array to utility interface application. However, detailed operation, a systematic analysis and design equations for this converter are not available in the literature. We will refer to this converter as boost integrated HF isolated half-bridge dc-dc converter. Therefore in this chapter we analyze this converter and find the design equations.

Layout of this chapter is as follows. In section 2.2 we describe in detail the circuit operation and in section 2.3 we analyze the converter and will find the design equations based on our analysis. In section 2.4 we design the converter for the required specifications.

2.2 Circuit Details and Operation of Selected Converter

Figure 2.1 shows the selected boost integrated HF isolated half-bridge dc-dc converter [12]. As can be seen this converter is a combination of boost and half-bridge converters with an output voltage-doubler rectifier.

The circuit consists of a boost inductor L_{in}, two active power switches S_1 and S_2, anti-parallel diodes D_1 and D_2, dc bus capacitors C_1 and C_2, two winding high frequency step up transformer Tr (of ratio 1:n) and voltage-doubler rectifying circuit that uses diodes D_3 and D_4 together with output filter capacitors C_3 and C_4. Switch S_2 and diode D_1 are shared by the boost converter and the half-bridge converter. Inductance L_k is used for soft-switching and represents sum of leakage inductance of HF transformer and an external inductance.

The following assumptions are made in the operation and analysis of the converter:

(1) All the switches, diodes and passive components are ideal.

(2) Magnetizing inductance of HF transformer is neglected and its leakage inductance is used as part of L_k.

(3) V_{C1}, V_{C2}, V_{C3} and V_{C4} are assumed constant.

(4) Input current i_{in} and primary current i_{LK} are assumed to be constant during charging and discharging of snubber capacitors C_{S1} and C_{S2}.

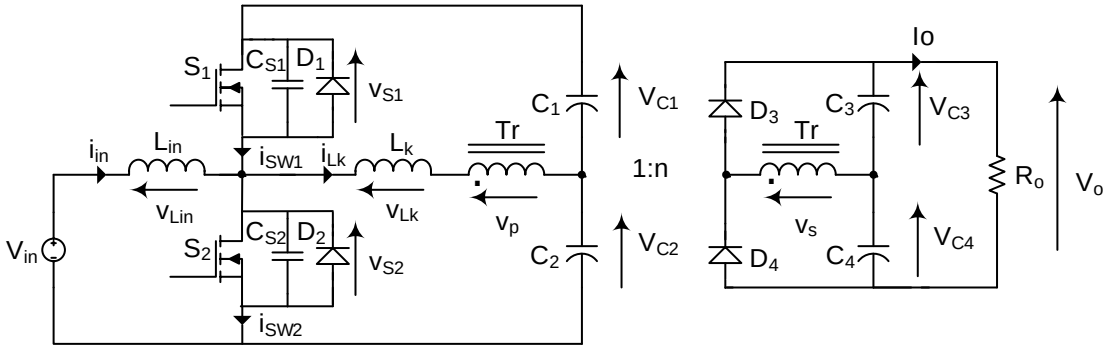


Fig. 2.1 boost integrated HF isolated half-bridge dc-dc converter.

Fig. 2.2 presents the voltage and current waveforms of the converter shown in Fig. 2.1. The lower and upper switches S_2 and S_1 are gated with gating signals of width DT and $(1 - D)T$, respectively. A small dead-gap is given between the gating signals to avoid short circuit due to simultaneous conduction of the switches. When S_2 is on input voltage is applied to L_{in} and its current increases. At the same time C_2 is connected across the series combination of L_k and primary winding of the transformer and the current through L_k decreases. During the conduction of S_1, the difference between V_{in} and $V_{C1} + V_{C2}$ is applied to L_{in} and since this voltage is negative the current through L_{in} decreases. At the same timeV_{C1} is applied to the series combination of L_k and primary winding of the transformer and therefore i_{Lk} increases. When primary current is positive D_3 is on and when it is negative D_4 is on. During each operation cycle, the switching events result in six operating states. The corresponding equivalent circuit and conduction paths of each state are demonstrated in the next section.

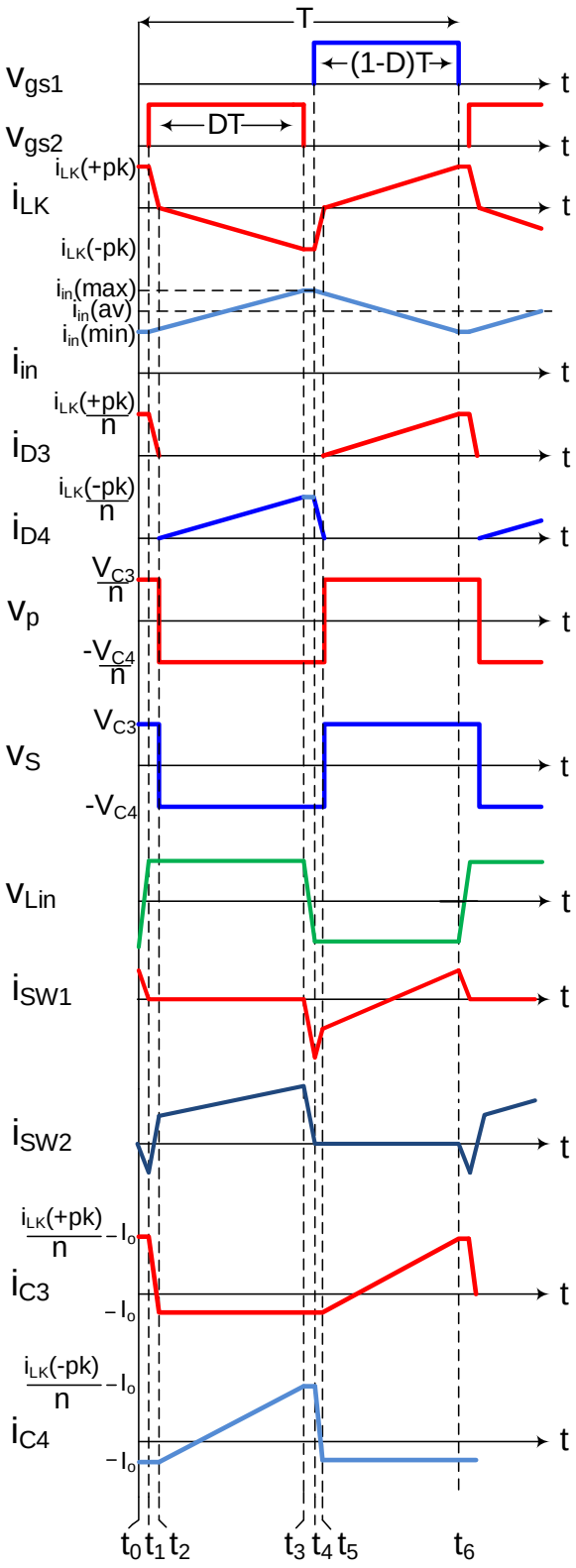


Fig. 2.2 Voltage and current waveforms.

2.2.1 Interval 1 (t_0-t_1) (Fig. 2.3):

Prior to this interval S_1 was on. This interval begins when S_1 is turned off at $t = t_0$. Therefore i_{in} and i_{Lk} start charging C_{S1} and discharging C_{S2}. At the end of this interval C_{S1} will charge to $V_{C1} + V_{C2}$ and v_{S2} will be zero. At the output, D_3 is conducting. Since this interval is very short, input current i_{in} and i_{LK} are assumed to be constant and i_{in} is at its minimum ($i_{in(\min)}$) and i_{LK} is at its maximum positive value ($i_{LK}(+pk)$) during this interval. Therefore we have:

$$v_S = V_{C3} \quad , \qquad v_P = \frac{V_{C3}}{n} \tag{2.1}$$

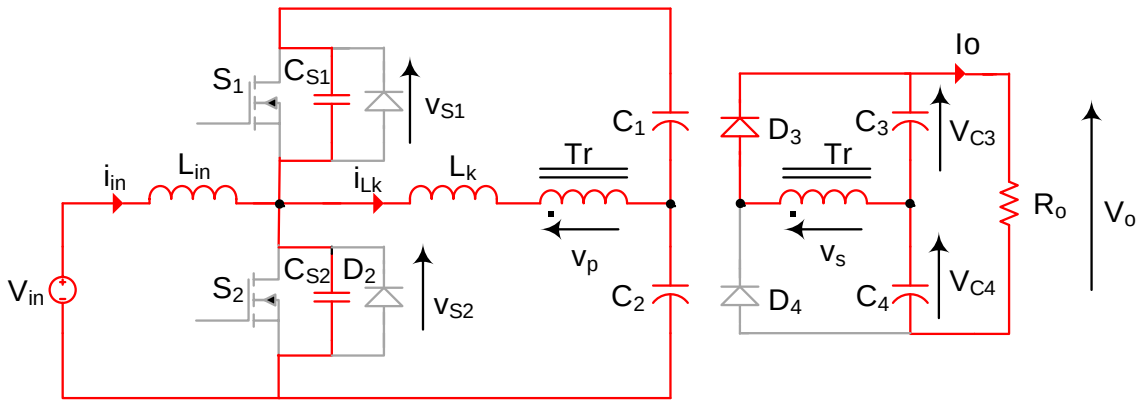


Fig. 2.3 Equivalent circuit for interval 1 (t_0-t_1).

2.2.2 Interval 2 (t_1-t_2) (Fig. 2.4):

At $t=t_1$ diode D_2 (antiparallel diode of S_2) starts to conduct and gating signal can be applied to S_2 to turn it on with ZVS when current through D2 reaches zero. i_{Lk} starts to decrease to zero and D_3 is still on and equation (2.1) is still valid. When D_2 is on, input voltage is across L_{in} and i_{in} starts increasing from $i_{in}(min)$. At the end of this interval i_{Lk} reaches zero. Therefore we can write:

$$V_{in} = L_{in}\frac{di_{in}}{dt} \tag{2.2a}$$

$$i_{in}(t_1) = i_{in}(min) \tag{2.2b}$$

$$i_{in} = i_{in}(min) + \frac{V_{in}}{L_{in}}(t - t_1) \tag{2.2c}$$

$$v_{Lk} = -\left(\frac{V_{C3}}{n} + V_{C2}\right) = L_k \frac{di_{Lk}}{dt} \tag{2.3a}$$

$$i_{Lk}(t_1) = i_{Lk}(+pk) \tag{2.3b}$$

$$i_{Lk} = i_{Lk}(+pk) - \frac{1}{L_k}\left(\frac{V_{C3}}{n} + V_{C2}\right)(t - t_1) \tag{2.3c}$$

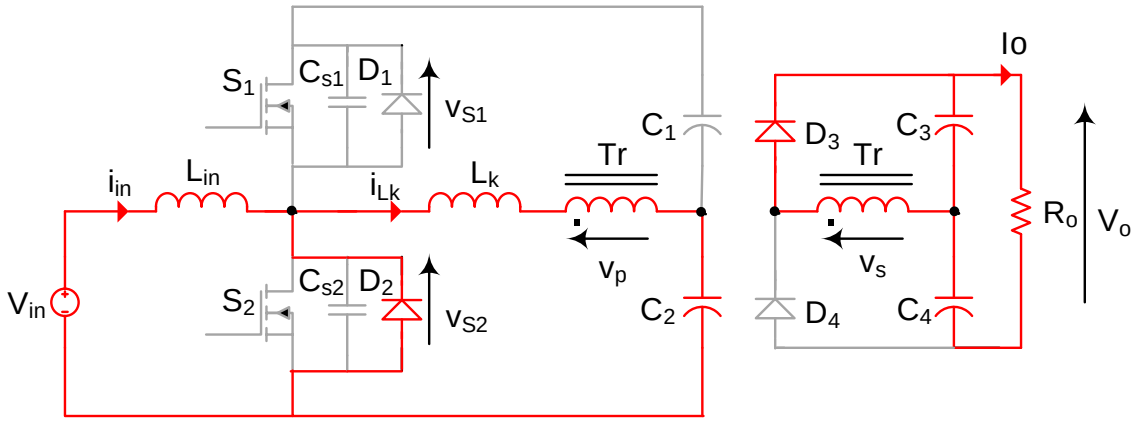


Fig. 2.4 Equivalent circuit for interval 2 (t_1-t_2).

2.2.3 Interval 3 (t_2-t_3) (Fig. 2.5):

This interval begins when i_{Lk} reaches zero. In this interval S_2 is on and V_{C2} is applied to the series connection of L_k and primary winding of Tr. Therefore v_p and v_s are negative and D_4 is conducting. At the same time input voltage is applied to L_{in} and its current continues to increase:

$$\left(\frac{V_{C4}}{n} - V_{C2}\right) = L_K \frac{di_{Lk}}{dt} \tag{2.4}$$

$$V_{in} = L_{in} \frac{di_{in}}{dt} \tag{2.5}$$

$$i_{Lk}(t_2) = 0 \tag{2.6a}$$

$$i_{Lk} = \frac{1}{L_k}\left(\frac{V_{C4}}{n} - V_{C2}\right)(t - t_2) \tag{2.6b}$$

Equation for i_{in} is the same as (2.2c) given in interval 2.

Therefore i_{in} continues to increase and reaches its maximum value at $t = t_3$. At the same time i_{Lk} starts from zero at $t = t_2$ to decrease to its negative peak $i_{Lk}(-pk)$ at $t = t_3$.

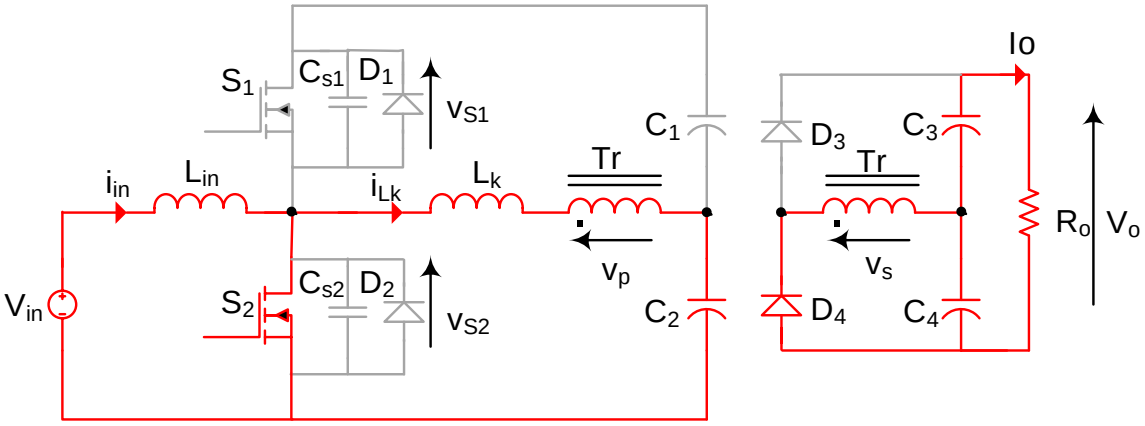


Fig. 2.5 Equivalent circuit for Interval 3 (t_2-t_3).

2.2.4 Interval 4 (t_3-t_4) (Fig. 2.6):

At $t=t_3$ S_2 is turned off and C_{S2} starts to charge to $V_{C1}+V_{C2}$ and C_{S1} starts to discharge to zero. Input current i_{in} is assumed to be constant at i_{in}(max) and i_{LK} is assumed to be constant at $i_{Lk}(-pk)$ during this interval. D_4 continues to conduct. When C_{S1} is completely discharged, D_1 begins to conduct and next interval starts.

$$v_S = V_{C4} \tag{2.7}$$

$$v_P = \frac{V_{C4}}{n} \tag{2.8}$$

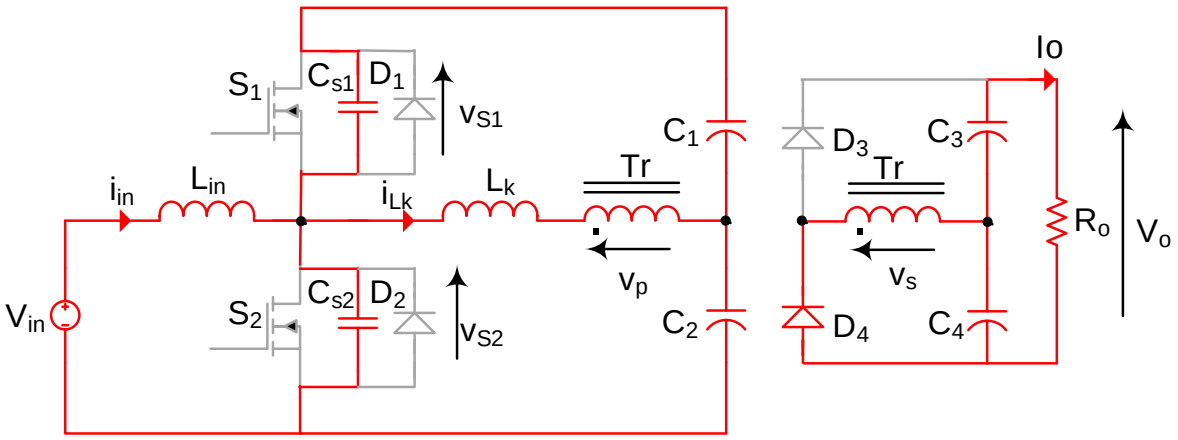


Fig. 2.6 Equivalent circuit for interval 4 (t_3-t_4).

2.2.5 Interval 5 (t_4-t_5) (Fig. 2.7):

At $t=t_4$ diode D_1 (antiparallel diode of S_1) starts to conduct and gating signal can be applied to S_1 to turn it on with ZVS. i_{Lk} starts to increase towards zero and i_{in} starts to decrease from its maximum value and D_4 is on. Equations (2.8) and (2.9) are still valid and we can write:

$$\left(\frac{V_{C4}}{n}+V_{C1}\right)=L_K\frac{di_{Lk}}{dt} \tag{2.9}$$

$$V_{in}-(V_{C1}+V_{C2})=L_{in}\frac{di_{in}}{dt} \tag{2.10}$$

$$i_{Lk}(t_4)=i_{Lk}(-pk) \tag{2.11}$$

$$i_{Lk}=i_{Lk}(-pk)+\frac{1}{L_K}\left(\frac{V_{C4}}{n}+V_{C1}\right)(t-t_4) \tag{2.12}$$

$$i_{in}(t_4)=i_{in}(max) \tag{2.13a}$$

$$i_{in}=i_{in}(max)+\frac{V_{in}-(V_{C1}+V_{C2})}{L_{in}}(t-t_4) \tag{2.13b}$$

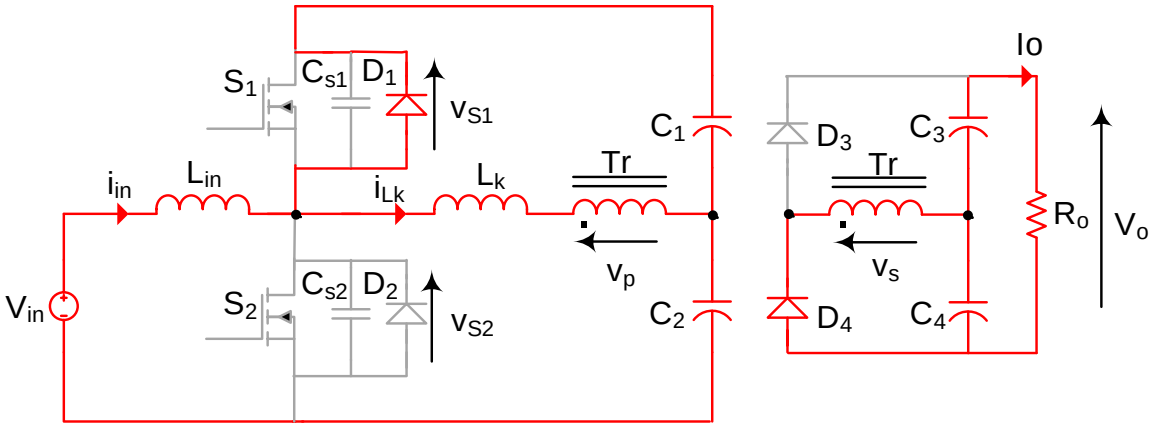


Fig. 2.7 Equivalent circuit for Interval 5 (t_4-t_5).

i_{Lk} reaches zero at the end of this interval.

2.2.6 Interval 6 (t_5-t_6) (Fig. 2.8):

During this interval S_1 is on and i_{Lk} starts to increase from zero at $t = t_5$ to reach its maximum value $i_{Lk}(+pk)$ at $t = t_6$. At the same time i_{in} decreases and reaches its minimum value at t_6. D_3 is conducting during this interval:

$$\left(V_{C1} - \frac{V_{C3}}{n}\right) = L_K \frac{di_{Lk}}{dt} \tag{2.14}$$

$$V_{in} - (V_{C1} + V_{C2}) = L_{in} \frac{di_{in}}{dt} \tag{2.15}$$

$$i_{Lk}(t_5) = 0$$

$$i_{Lk} = \frac{1}{L_K}\left(V_{C1} - \frac{V_{C3}}{n}\right)(t - t_5) \tag{2.16}$$

Equation for i_{in} is the same as (2.13b) given in interval-5.

At the end of this interval S_1 is turned off to complete the full switching cycle.

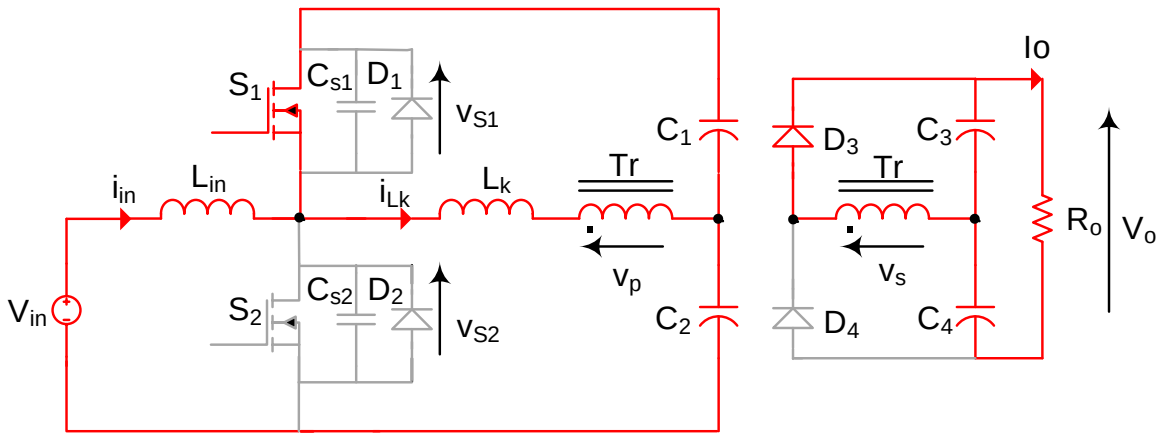


Fig. 2.8 Equivalent circuit for Interval 6 (t_5-t_6).

2.3 Steady state Analysis

In this section we find the design equations for steady-state operation of the converter. As assumed earlier in Section 2.2, the snubber charging/discharging intervals are very small and their effects are neglected.

2.3.1 Input/output voltage ratio

To determine the input output voltage ratio V_{C1} ,V_{C2} ,V_{C3} and V_{C4} are assumed constant during one switching period. The volt second balance equations for L_{in} , L_k and primary winding of T_1 in one switching period lead to:

S_1 off, D_2 or S_2 on:

$$V_{in} = \frac{L_{in}\Delta i_{in}}{DT} \tag{2.17}$$

S_1 on, S_2 off:

$$V_{in} - (V_{c1} + V_{c2}) = \frac{-L_{in}\Delta i_{in}}{(1-D)T} \tag{2.18}$$

Substituting (2.17) in (2.18):

$$V_{c1} + V_{c2} = \frac{V_{in}}{1-D} \tag{2.19}$$

Neglecting small voltage drop across the inductor L_k we can write equations (2.20) and (2.21) for voltage across the primary and secondary windings:

D_1 or S_1 on, *S_2* off:

$$v_p = V_{c1}\ , v_s = nV_{c1}\ , V_{c3} = \ nV_{c1} \tag{2.20}$$

S_1 off, *D_2* or *S_2* on:

$$v_p = -V_{c2}\ , v_s = -nV_{c2}\ ,\ V_{c4} = \ nV_{c2} \tag{2.21}$$

Using volt-second balance for transformer primary:

$$V_{c1}(1 - D) = V_{c2}D \tag{2.22}$$

$$\frac{V_{c1}}{V_{c2}} = \frac{D}{1 - D} \tag{2.23}$$

Since average voltage across L_{in} and L_k and primary winding is zero,

$$V_{c2} = V_{in} \tag{2.24}$$

Then using (2.23):

$$V_{c1} = \frac{D}{1 - D}V_{in} \tag{2.25}$$

Output voltage is given by:

$$V_o = V_{c3} + V_{c4} \tag{2.26}$$

Substituting for Vc3 and Vc4 from (2.20) and (2.21), we get:

$$V_o = n(V_{c1} + V_{c2}) \tag{2.27a}$$

Using (2.19):

$$V_o = \frac{nV_{in}}{1 - D} \tag{2.27b}$$

2.3.2 ZVS characteristics of switches

During interval 1 the difference value of i_{Lk} and i_{in} is used to charge C_{S1} and discharge C_{S2} to turn on S_2 under ZVS condition. Therefore we can write:

$$\frac{1}{2}L_k[i_{Lk}\,(+pk) - i_{in}\,(min)]^2 > \frac{1}{2}(C_{s1} + C_{s2})(V_{c1} + V_{c2})^2 \quad (2.28)$$

$$i_{in}(min) = i_{in}(av) - \frac{\Delta i_{in}}{2} \quad (2.29)$$

$$i_{in}(av) = \frac{P_i}{V_{in}} = \frac{P_o}{\eta V_{in}} = \frac{V_o I_o}{\eta V_{in}} = \frac{n}{1-D}\left(\frac{V_o}{\eta R_o}\right) \quad (2.30)$$

$$\Delta i_{in} = \frac{V_{in} D}{Lf} \quad (2.31)$$

Where switching frequency $f = 1/T$. During interval 4 the sum of $|i_{Lk}|$ and i_{in} is used to charge C_{S2} and discharge $C_{S1}$to turn on S_1 under ZVS condition. Therefore we can write:

$$\frac{1}{2}L_k[|i_{Lk}\,(-pk)| + i_{in}\,(max)]^2 > \frac{1}{2}(C_{s1} + C_{s2})(V_{c1} + V_{c2})^2 \quad (2.32)$$

$$i_{in}(max) = i_{in}(av) + \frac{\Delta i_{in}}{2} \quad (2.33)$$

We see that ZVS operation of S_1 is easier than S_2 .

2.3.3 Calculating peak values of primary current

In order to find $i_{Lk}(+pk)$ and $i_{Lk}(-pk)$ we just consider intervals 3 and 6. As mentioned earlier during interval 3, S_2 and D_4 are on and S_1 and D_3 are off. The primary current of T_1 decreases from zero to its negative peak value $i_{Lk}(-pk)$. Since the output current is the average current in D_4 we can write Io in terms of D:

$$I_o = \frac{|i_{Lk}\,(-pk)|}{n}\,\frac{D}{2} \quad (2.34)$$

$$|i_{Lk}\,(-pk)| = \frac{2nI_o}{D} \quad (2.35)$$

$$|i_{Lk}\,(-pk)| = \frac{2nP_o}{V_o D} \quad (2.36)$$

Similarly during interval 6, S_1 and D_3 are on and S_2 and D_4 are off and the output current is the average current in D_3 therefore we can write:

$$I_o = \frac{i_{Lk}\,(+pk)}{n}\,\frac{(1-D)}{2} \tag{2.37}$$

$$i_{Lk}\,(+pk) = \frac{2nI_o}{1-D} \tag{2.38}$$

$$i_{Lk}\,(+pk) = \frac{2nP_o}{V_o(1-D)} \tag{2.39}$$

2.4 Design

In this section we design the converter for the following specification:

$40\text{ V} < V_{in} < 80\text{ V}$, $P_o = 400\text{ W}$, $V_o = 200\text{ V}$, $f = 50\text{ kHz}$, assume an efficieny, $\eta = 0.9$

2.4.1 Calculation of transformer turns ratio and variation in duty cycle:

In order to utilize both switches optimally we consider $D = 0.5$ at mid-range of input voltage:

$$V_{in} = 60V, D = 0.5$$

Using (2.27),

$$V_o = \frac{nV_{in}}{1-D}\ , \qquad 200 = \frac{60n}{1-0.5}\ , \qquad n = 1.67$$

Therefore, transformer turns ratio is $n = 1.67$.

Therefore, using (2.27), D will vary between 0.33 and 0.67 for variation in V_{in} from 80 V to 40V.

2.4.2 Calculation of input inductor value:

Calculating the value of input inductor:

$$P_{in} = \frac{P_o}{\eta}$$

$$P_{in} = \frac{400}{0.9} = 444\text{ W}$$

Therefore:

$$I_{in}(min) = \frac{444}{80} = 5.55A$$

$$I_{in}(max) = \frac{444}{40} = 11.1A$$

Considering 20% ripple for maximum average input current:

$$\Delta i_{in} = 0.2 I_{in}(max) = 2.22A$$

$$L_{in} = \frac{V_{in}D}{f\Delta i_{in}} = \frac{40 \times 0.67}{50000 \times 2.22} = 241\ \mu H$$

2.4.3 Calculation of switch ratings:

Maximum voltage across the switches is given by:

$$V_{S1}\,(max) = V_{S2}\,(max) = V_{C1} + V_{C2} = \frac{V_{in}}{1-D} = \frac{80}{1-0.33} = 119\ V$$

Peak current through the switches and diodes are calculated below.

$$i_{S1}(max) = i_{Lk}\,(+pk) - i_{in}(min)$$

$$i_{Lk}\,(+pk) = \frac{2nP_o}{V_o(1-D_{max})} = \frac{2 \times 1.67 \times 400}{200(1-0.67)} = 20.2\ A$$

$$i_{in}(min) = i_{in}(av) - \frac{\Delta i_{in}}{2} = 11.1 - \frac{2.22}{2} = 10\ A$$

$$i_{S1}(max) = 10.2\ A$$

$$i_{S2}(max) = i_{in}(max) + |i_{Lk}\,(-pk)|$$

$$i_{in}(max) = i_{in}(av) + \frac{\Delta i_{in}}{2}$$

i_{in} is maximum when input voltage is minimum:

$$i_{in}(max) = I_{in}(max) + \frac{\Delta i_{in}}{2}$$

$$i_{in}(max) = 11.1 + \frac{2.22}{2} = 12.2A$$

$$|i_{Lk}(-pk)| = \frac{2nP_o}{V_o D}$$

$$|i_{Lk}(-pk)|(max) = \frac{2 \times 1.67 \times 400}{200 \times 0.33} = 20.2 \text{ A}$$

$$i_{S2}(max) = 12.2 + 20.2 = 32.4 \text{ A}$$

With small error we can say that:

$$i_{D2}(max) = i_{Lk}(+pk) - i_{in}(min)$$

$$i_{D2}(max) = 20.2 - 10 = 10.2 \text{ A}$$

$$i_{D1}(max) = |i_{Lk}(-pk)| + i_{in}(max)$$

$$i_{D1}(max) = 20.2 + 12.2 = 32.4 \text{ A}$$

Considering the maximum values for switch voltage and current and for low conduction loss we select IFP4228 for the transistors with following specifications:

$$V_{DS}(max) = 150V, I_D(max) = 78 \text{ A}, C_{oss} = 480\ pF$$

2.4.4 Calculation of inductor value L_k for ZVS:

Since the available stored energy in L_k is minimum for ZVS operation of S_2, therefore we consider this case in calculating the value of L_k. According to (2.28) to ensure ZVS operation for S_2 the following condition should be satisfied:

$$\frac{1}{2}L_k[i_{Lk}(+pk) - i_{in}(min)]^2 > \frac{1}{2}(C_{s1} + C_{s2})(V_{c1} + V_{c2})^2$$

Our goal is to have ZVS in the range of 20% -100% of full load current:

$$P_o = 0.2 \times 400 = 80W$$

$$i_{Lk}(+pk)_{min} = \frac{2nP_o}{V_o(1 - D_{min})} = \frac{2 \times 1.67 \times 80}{200 \times (1 - 0.33)} = 2 \text{ A}$$

D is minimum when input voltage is maximum:

$$i_{in}(av) = \frac{P_i}{V_{in}} = \frac{P_o}{\eta V_{in}} = \frac{80}{0.9 \times 80} = 1.11A$$

$$\Delta i_{in} = \frac{V_{in}D}{L_{in}f} = \frac{80 \times 0.33}{241 \times 10^{-6} \times 50 \times 10^{3}} = 2.2A$$

$$i_{in}(min) = i_{in}(av) - \frac{\Delta i_{in}}{2} = 1.11 - \frac{2.2}{2} \cong 0A$$

$$\frac{1}{2}L_k[i_{Lk}\,(+pk) - i_{in}\,(min)]^2 > \frac{1}{2}(C_{s1} + C_{s2})(V_{c1} + V_{c2})^2$$

$$\frac{1}{2}\,L_k \times 2^2 > \frac{1}{2}(2 \times 480 \times 10^{-12}) \times 119^2$$

$$L_k\ > 3.4\mu H$$

2.4.5 Calculation of dc bus filter capacitor values:

In order to calculate the value of C_1 and C_2 we can use the ripple formula for boost converter:

$$\frac{\Delta V}{V} = \frac{D}{RCf}$$

C is the equivalent capacitance of C_1 and C_2 and *R* is the equivalent resistance across the series combination of C_1 and C_2:

$$R = \frac{(V_{C1} + V_{C2}\,)^2}{P_o} = \frac{119^2}{400} = 35.4\ \Omega$$

Assuming two present for ripple ratio:

$$C = \frac{D}{Rf\frac{\Delta V}{V}} = \frac{0.67}{35.4 \times 50 \times 10^{3}\ \times 0.02} = 18.9\mu F$$

$$C_1\ = C_2\ = 47\mu F, 100V$$

2.4.6 Ratings of output rectifier diodes:

In order to choose output diodes we need to know maximum reverse voltage and forward current:

$$V_{D_3}(max) = V_{D_4}(max) = V_o = 200V$$

$$I_{D_3}(max) = \frac{i_{Lk}\,(+pk)_{max}}{n} = \frac{2I_o}{1 - D_{max}}$$

$$I_{D_4}(max) = \frac{|i_{Lk}\,(-pk)|_{max}}{n} = \frac{2I_o}{D_{min}}$$

$$I_o = \frac{400W}{200V} = 2A$$

$$I_{D_3}(max) = \frac{2 \times 2}{1 - 0.67} = 12.1A$$

$$I_{D_4}(max) = \frac{2 \times 2}{0.33} = 12.1A$$

2.4.7 Calculation of output filter capacitor values:

We can use same formula for calculating the values of C_3 and C_4:

$$C = \frac{D}{R_o f \frac{\Delta V}{V}}$$

$$R_o = \frac{V_o}{I_o} = \frac{200V}{2A} = 100\Omega\,, \frac{\Delta V}{V} = 0.02\,, \mathrm{D} = D_{max} = 0.67$$

$$C = \frac{0.67}{100 \times 50 \times 10^3 \times 0.02} = 6.7\mu\mathrm{F}$$

$$C_3 = C_4 = 15\mu\mathrm{F}, 200\mathrm{V}$$

Chapter 3

Simulation and Experimental Results

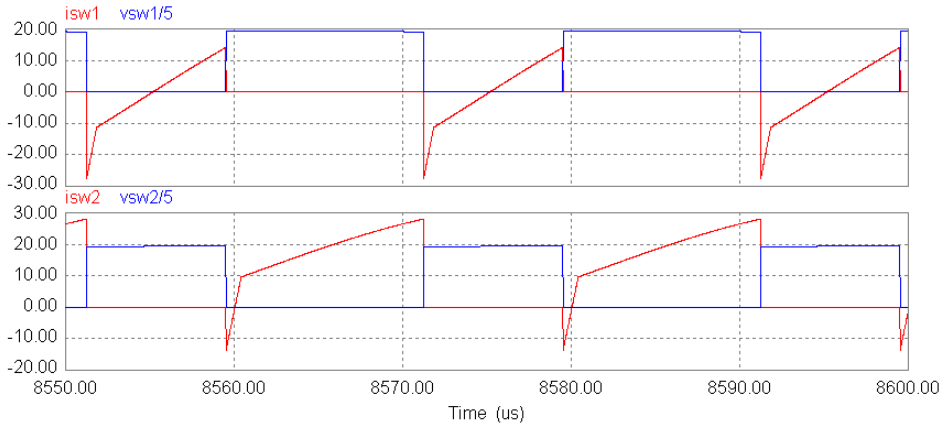
In this chapter simulation and experimental results for the converter designed in Chapter 2 are presented. Layout of this chapter is as follows: Section 3.1 presents the simulation results obtained using PSIM simulation program. Experimental results are given in Section 3.2. Section 3.3 gives the conclusions.

3.1 Simulation Results

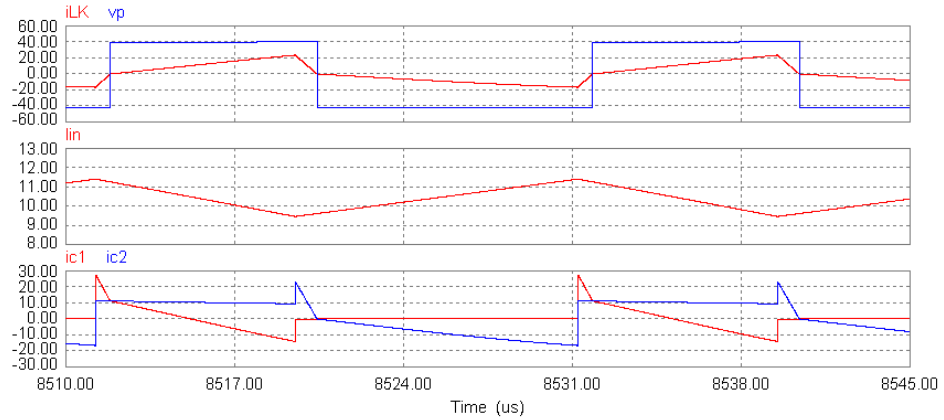
The component values obtained from the design section of previous chapter are used for simulation of 400 W, 200 V output 50 kHz boost integrated HF isolated half-bridge dc-dc converter with an input voltage of 40 to 80 V. The behavior of the converter for variation in load and input voltage has been evaluated with PSIM simulation software. The simulation sample waveforms obtained for the converter at full-load, half-load and 20%-load conditions with minimum input voltage ($V_{in(min)}$ = 40 V) are shown in Fig. 3.1 to Fig. 3.3.

The simulation sample waveforms of the converter at V_{in} = 60 V for full-load, half-load and 20%-load are given in Fig. 3.4 to Fig. 3.6. And finally the simulation sample waveforms of the converter at maximum input voltage ($V_{in(max)}$ = 80 V) for full-load, half-load and 20%-load are given in Fig. 3.7 to Fig. 3.9.

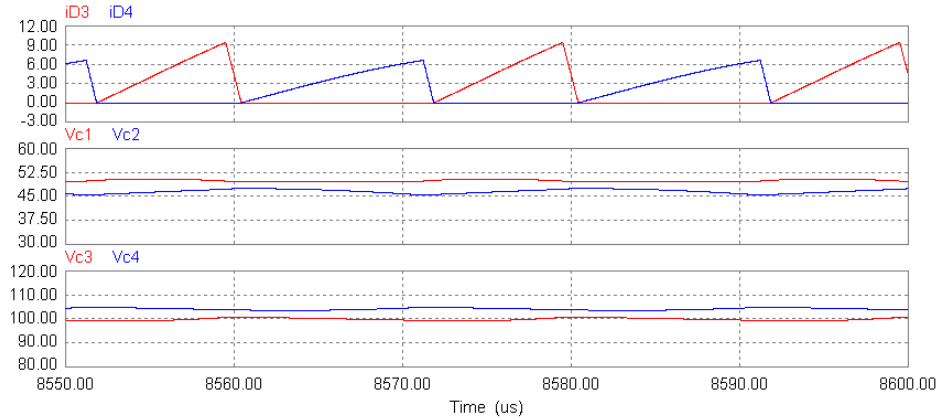
Figs. 3.1(a) to 3.7(a) show voltages and currents of switches for various load conditions. They show that for the whole input voltage range the converter works in ZVS from full-load to light-load since the anti-parallel diodes across the switches conduct first before the switches start conducting. Fig 3.1(b) to 3.7(b) show transformer primary voltage and current, input inductor current and boost capacitors currents for various load conditions. Figs. 3.1(c) to 3.7(c) show output diodes currents, boost capacitors voltages and output capacitors voltages for various load conditions. It is observed that beside the many advantages of this configuration the only disadvantage is that the current stress on the switches and boost capacitors and output diodes is not the same. Therefore power loss in S_2 is more than S_1 and we expect that in experiment ESR power loss in C_2 is more than C_1. For $V_{in(min)}$ = 40 V the peak current in D_3 is more than D_4 but for V_{in} = 60 V and $V_{in(max)}$ = 80 V the peak current in D_4 is more than D_3.



(a) Switch voltages and currents.

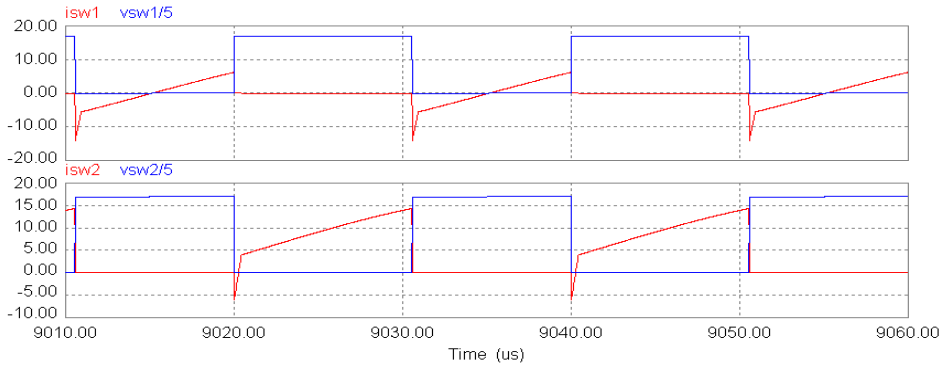


(b)Transformer primary voltage and current, input boost inductor current, boost capacitors (C_1 and C_2) currents.

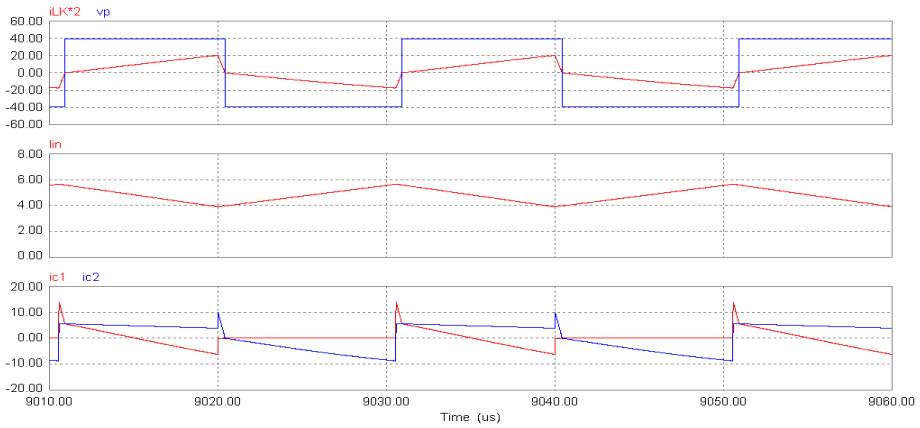


(c) Output diodes (D_3 and D_4) currents, boost capacitors (C_1 and C_2) voltages, output capacitors (C_3 and C_4) voltages.

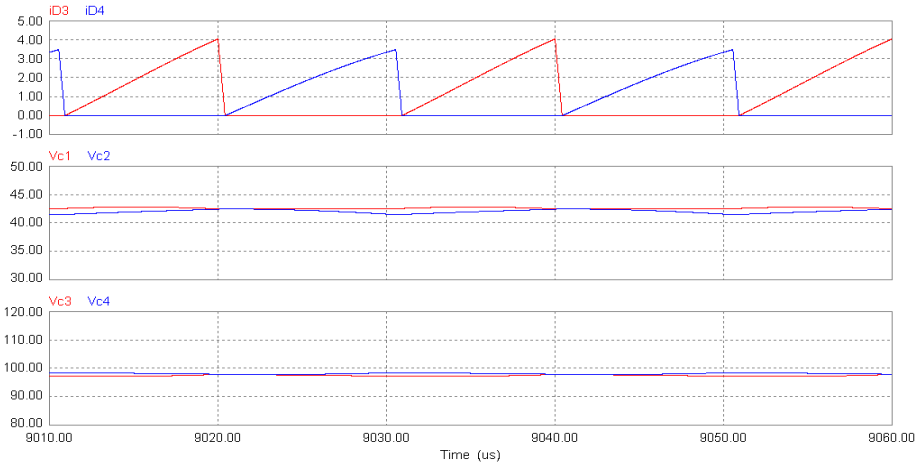
Fig. 3.1 PSIM simulation results with $V_{in(min)}$ = 40 V at full load.



(a) Switch voltages and currents.

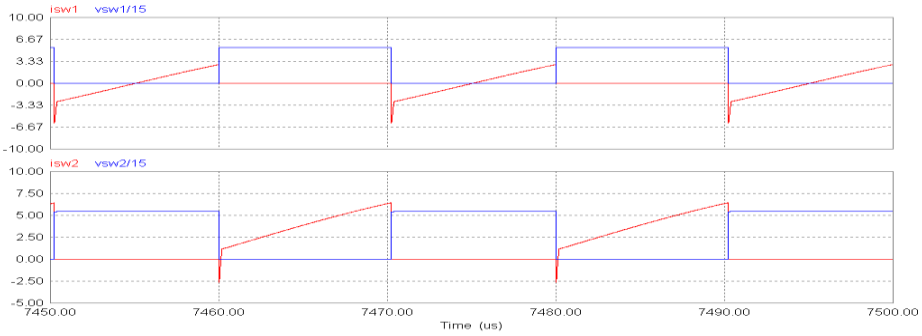


(b)Transformer primary voltage and current, input boost inductor current, boost capacitors (C_1 and C_2) currents.

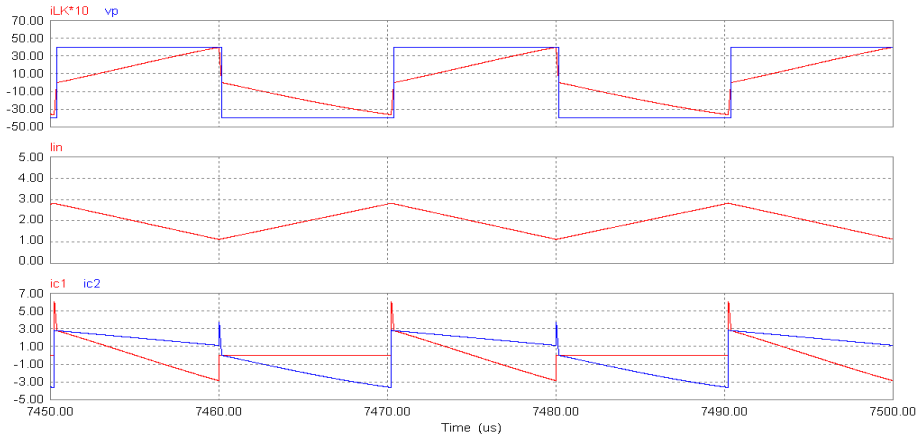


(c) Output diodes (D_3 and D_4) currents, boost capacitors (C_1 and C_2) voltages, output capacitors (C_3 and C_4) voltages

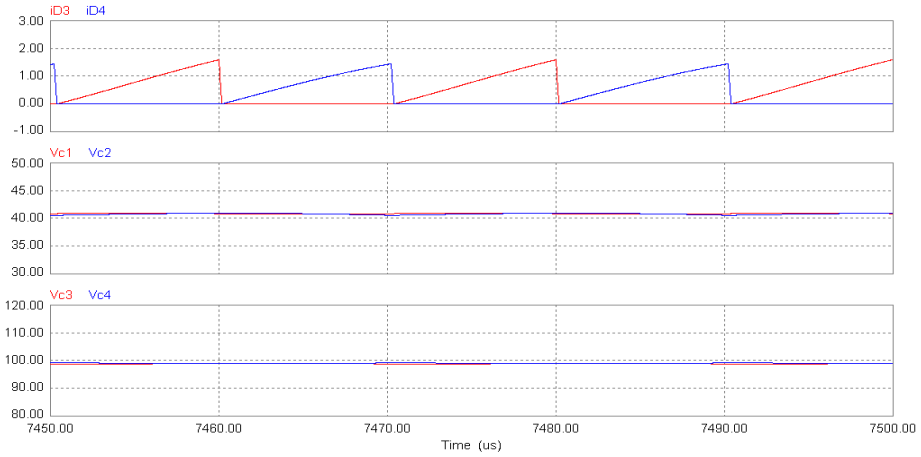
Fig. 3.2 PSIM simulation results with $V_{in(min)}$ = 40 V at half-load.



(a) Switch voltages and currents.

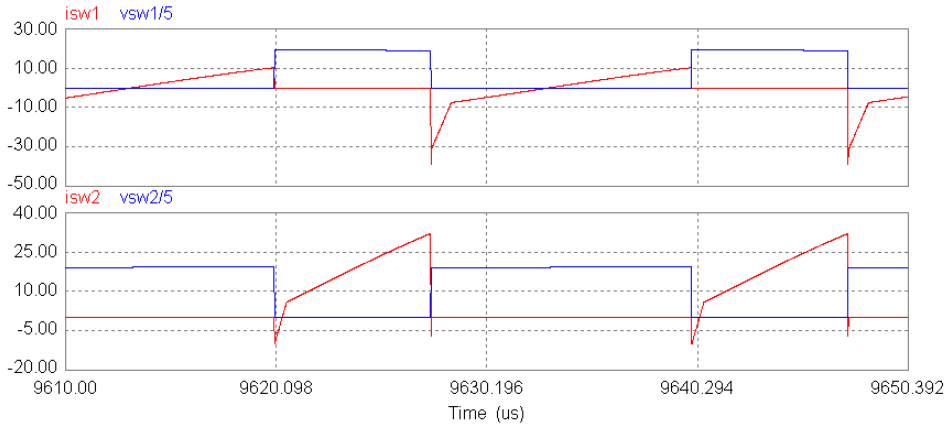


(b)Transformer primary voltage and current, input boost inductor current, boost capacitors (C_1 and C_2) currents.

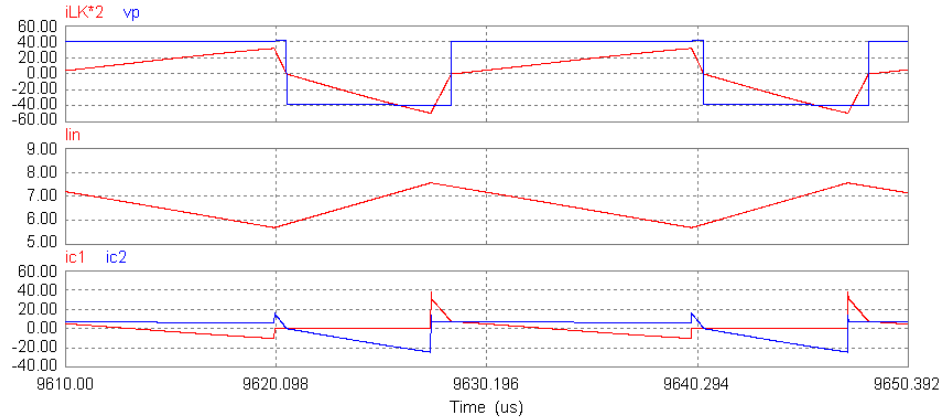


(c) Output diodes (D_3 and D_4) currents, boost capacitors (C_1 and C_2) voltages, output capacitors (C_3 and C_4) voltages.

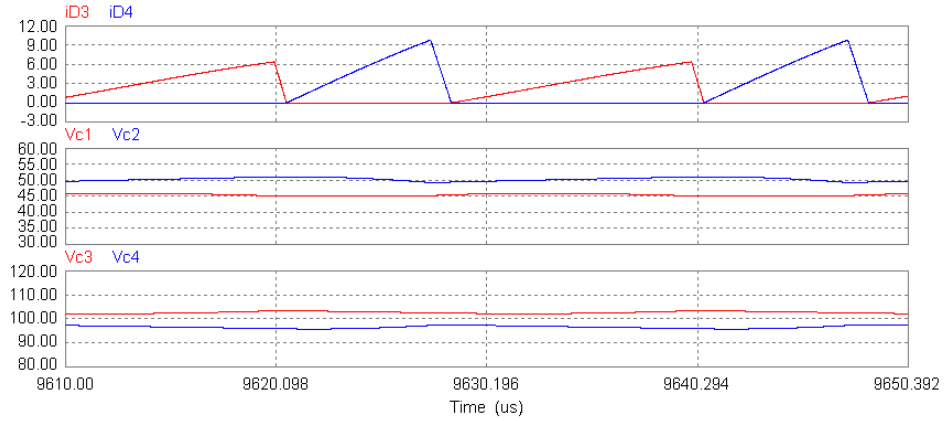
Fig.3.3 PSIM simulation results with $V_{in(min)}$ = 40 V at 20% load.



(a) Switch voltages and currents.

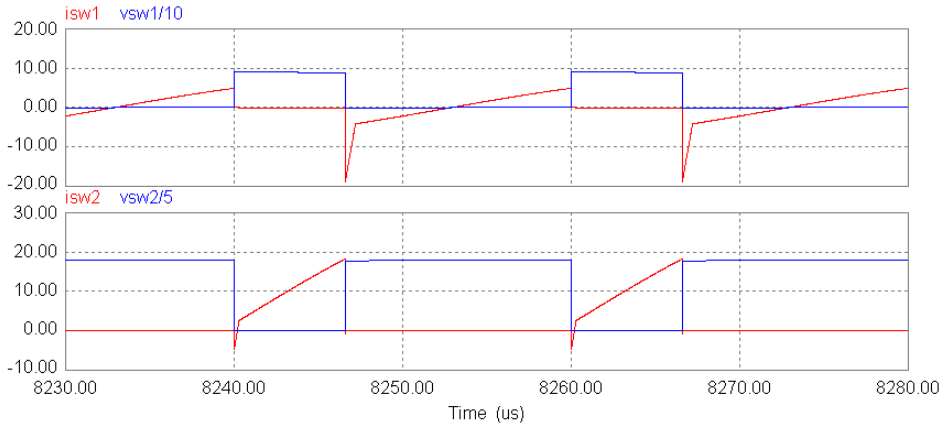


(b)Transformer primary voltage and current, input boost inductor current, boost capacitors (C_1 and C_2) currents.

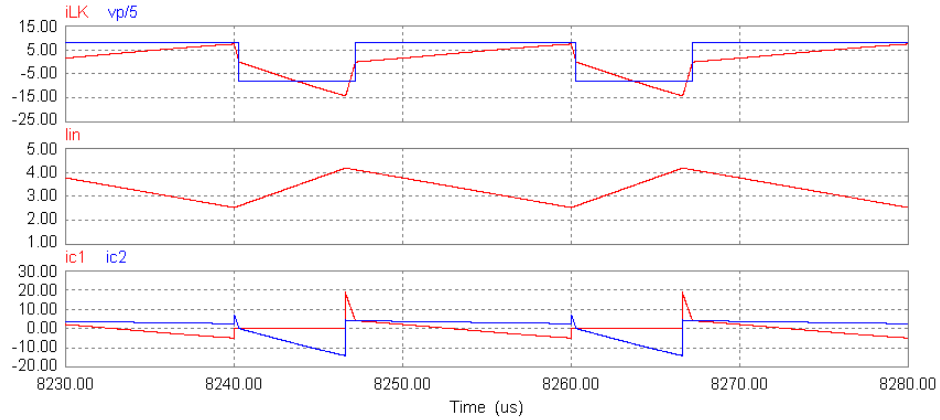


(c) Output diodes (D_3 and D_4) currents, boost capacitors (C_1 and C_2) voltages, output capacitors (C_3 and C_4) voltages.

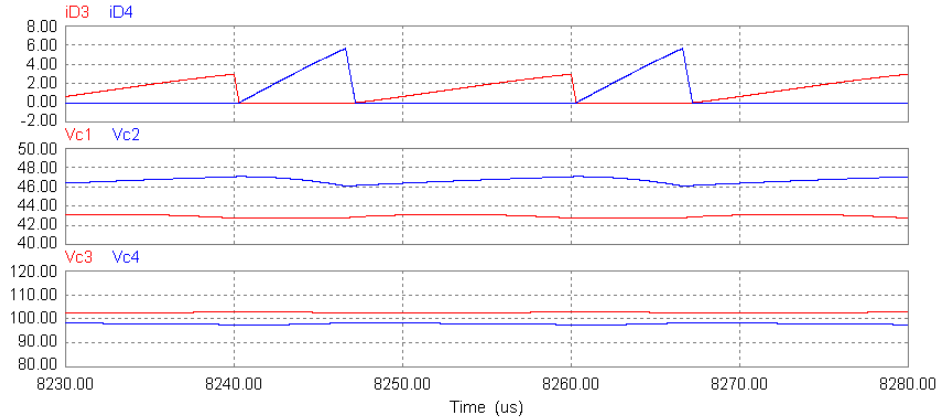
Fig. 3.4 PSIM simulation results with V_{in} = 60 V at full-load.



(a) Switch voltages and currents.

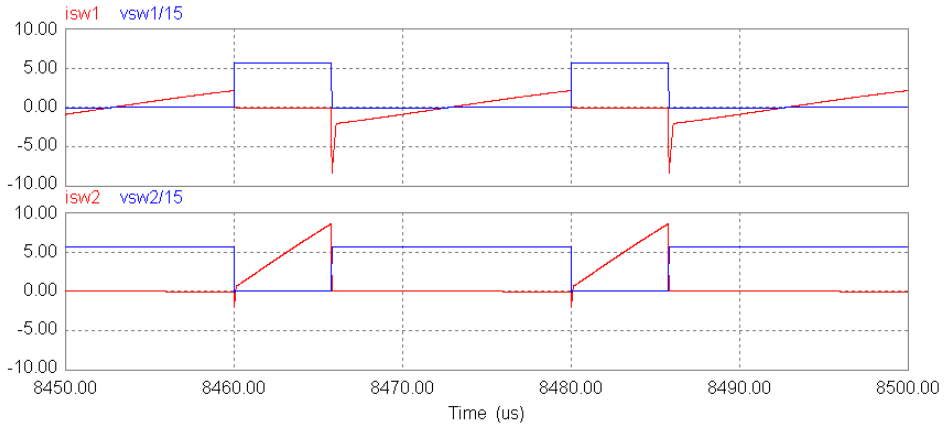


(b)Transformer primary voltage and current, input boost inductor current, boost capacitors (C_1 and C_2) currents.

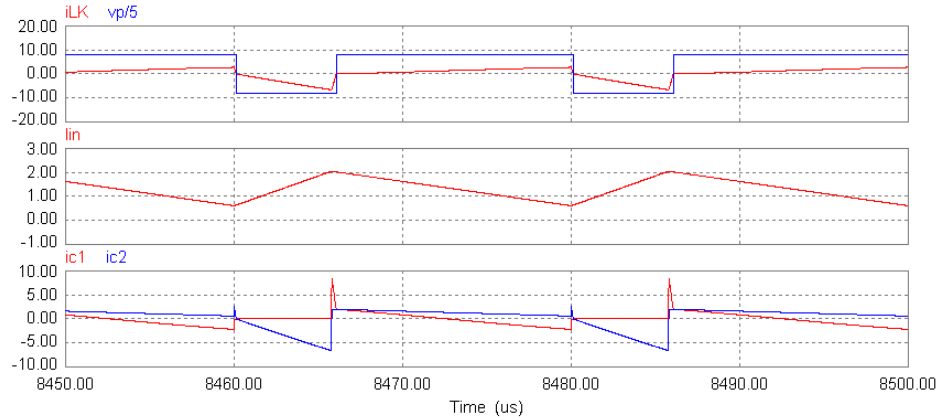


(c) Output diodes (D_3 and D_4) currents, boost capacitors (C_1 and C_2) voltages, output capacitors (C_3 and C_4) voltages.

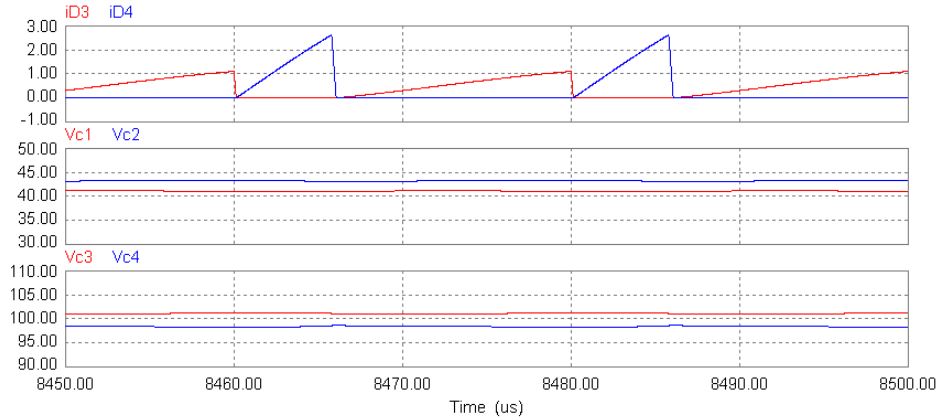
Fig. 3.5 PSIM simulation results with V_{in} = 60 V at half-load.



(a) Switch voltages and currents.

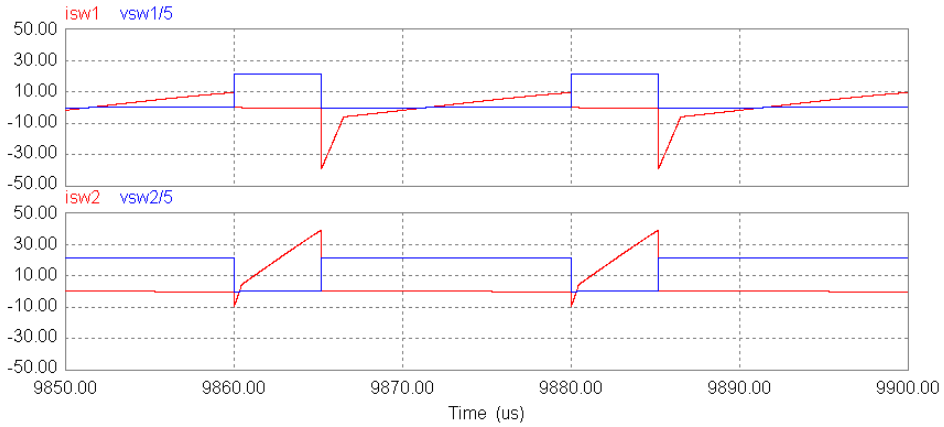


(b)Transformer primary voltage and current, input boost inductor current, boost capacitors (C_1 and C_2) currents.

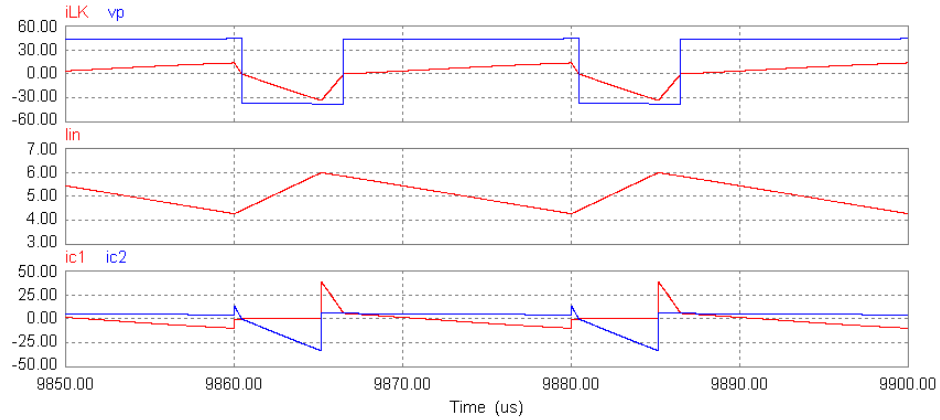


(c) Output diodes (D_3 and D_4) currents, boost capacitors (C_1 and C_2) voltages, output capacitors (C_3 and C_4) voltages.

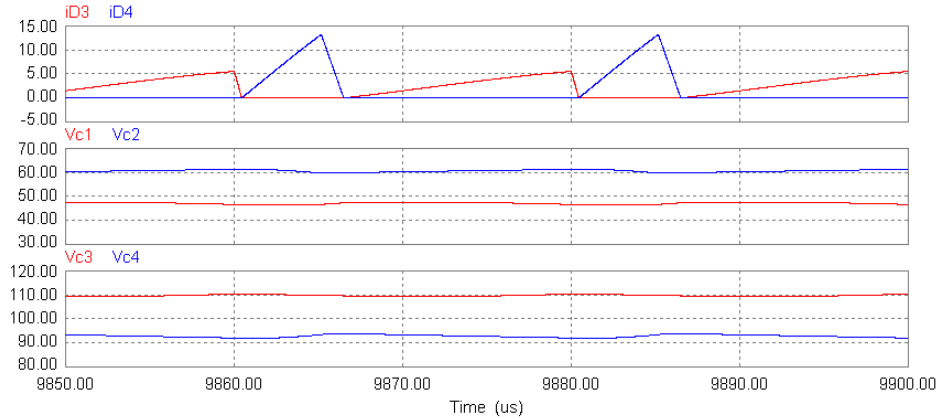
Fig. 3.6 PSIM simulation results with V_{in} = 60 V at 20% load.



(a) Switch voltages and currents.

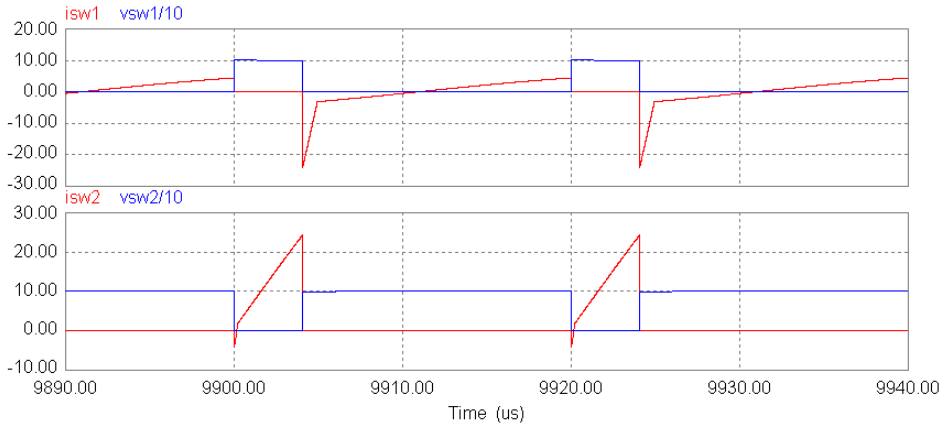


(b)Transformer primary voltage and current, input boost inductor current, boost capacitors (C_1 and C_2) currents.

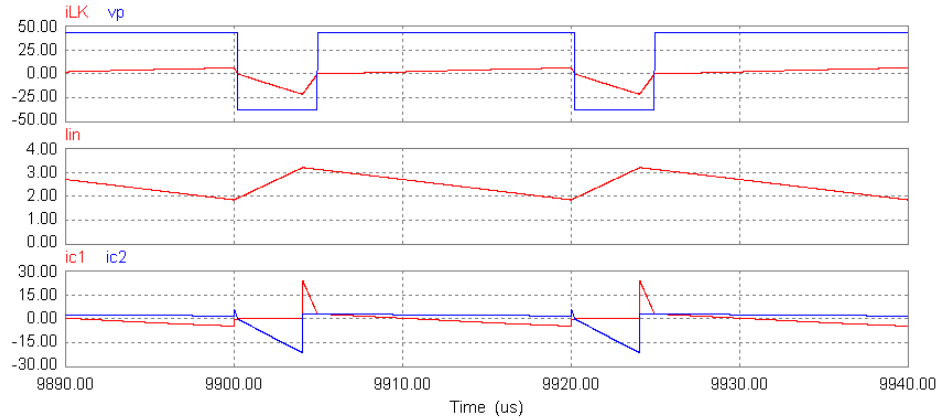


(c) Output diodes (D_3 and D_4) currents, boost capacitors (C_1 and C_2) voltages, output capacitors (C_3 and C_4) voltages.

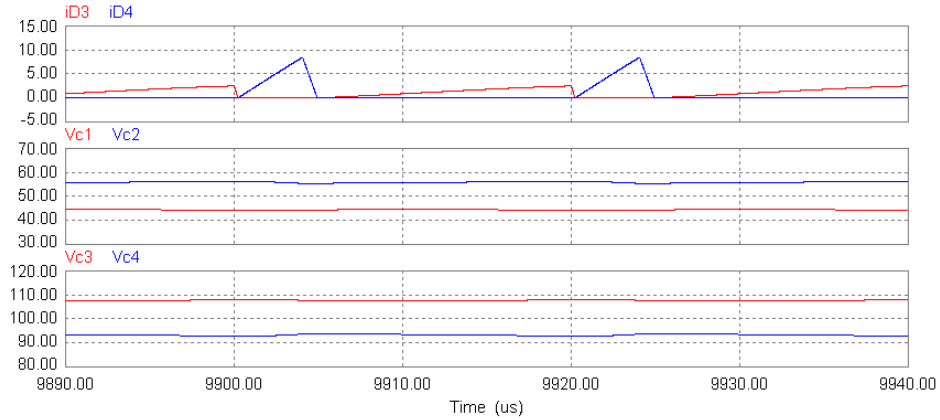
Fig. 3.7 PSIM simulation results with $V_{in(max)}$ = 80 V at full-load.



(a) Switch voltages and currents.

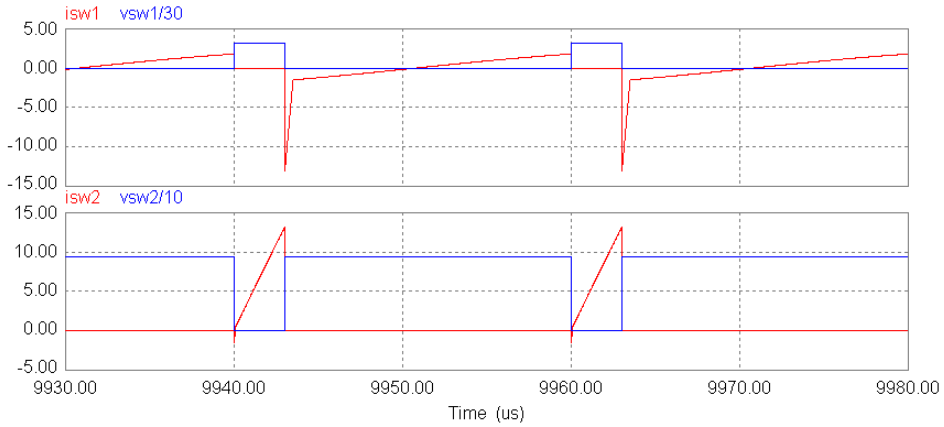


(b)Transformer primary voltage and current, input boost inductor current, boost capacitors (C_1 and C_2) currents.

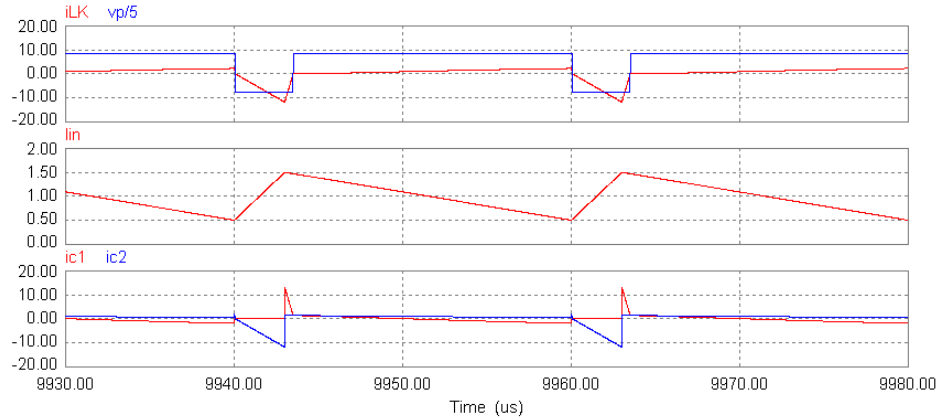


(c) Output diodes (D_3 and D_4) currents, boost capacitors (C_1 and C_2) voltages, output capacitors (C_3 and C_4) voltages.

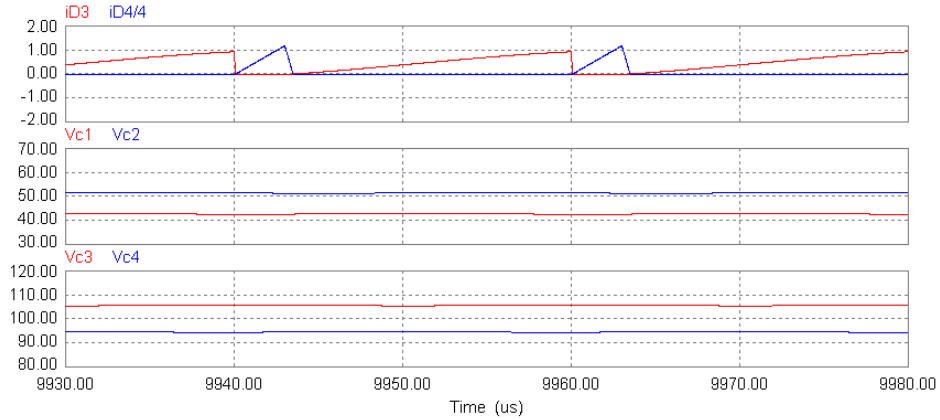
Fig. 3.8 PSIM simulation results with $V_{in(max)}$ = 80 V at half-load.



(a) Switch voltages and currents.



(b)Transformer primary voltage and current, input boost inductor current, boost capacitors (C_1 and C_2) currents.



(c) Output diodes (D_3 and D_4) currents, boost capacitors (C_1 and C_2) voltages, output capacitors (C_3 and C_4) voltages.

Fig. 3.9 PSIM simulation results with $V_{in(max)}$ = 80 V at 20%-load.

3.2 Experimental results

A 400 W 200 V output switching at 50 kHz converter designed in Chapter 2 was built in the power electronics lab to verify the operation and performance of the selected converter. Appendix 1 gives the circuit details built in the lab.

The detailed values of components are listed in Table 3.1:

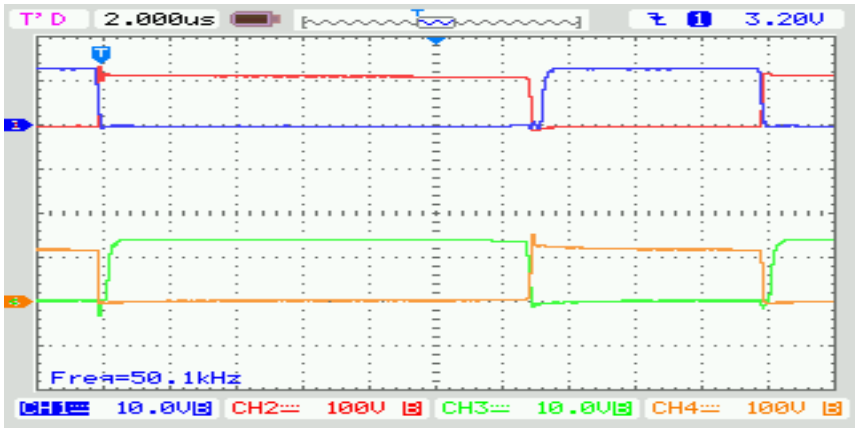
Table 3.1 Components used in experiment

S1,S2	IRFP4228 (150V,78A,12mΩ)
C1, C2	470μF, 200V, Electrolytic
C3,C4	2.2 μF, 630 V Metalized Polypropylene.
D3,D4	C3D02060E, 600 V, 4A, Silicon Carbide Schottky Diode
L_{in}	200 μH (A-759135-2(stack of two), number of turns =28)
L_k	3 μH (A-071065-2, number of turns =6)
HF Transformer	EI60 N_p = 6, N_s = 15 Core material - 2500B2, Leakage inductance = 0.7 μH
PWM Controller	UC3824
RC snubber	in parallel of series connection of L_k and primary winding of transformer (R = 100 ohm, C_s = 1 nF)

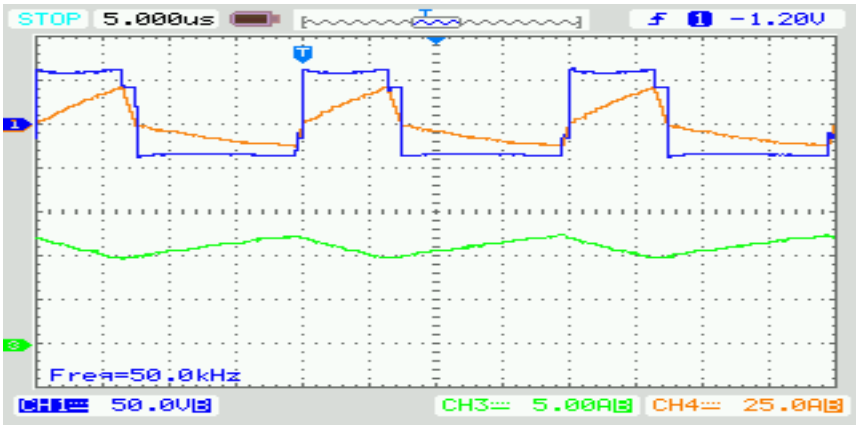
In order to tolerate quite large ripple currents in C_1 and C_2 we had to use ten times the designed value for them. Also the turns ratio of transformer is higher for duty cycle loss.

The converter was operated in open-loop control for 3 input voltages of V_{in} = 40 V, 60 V and 80 V and for 3 different loads (80 W, 200 W and 400 W). Figures 3.10 to 3.18 show the experimental results for different input voltages and loads.

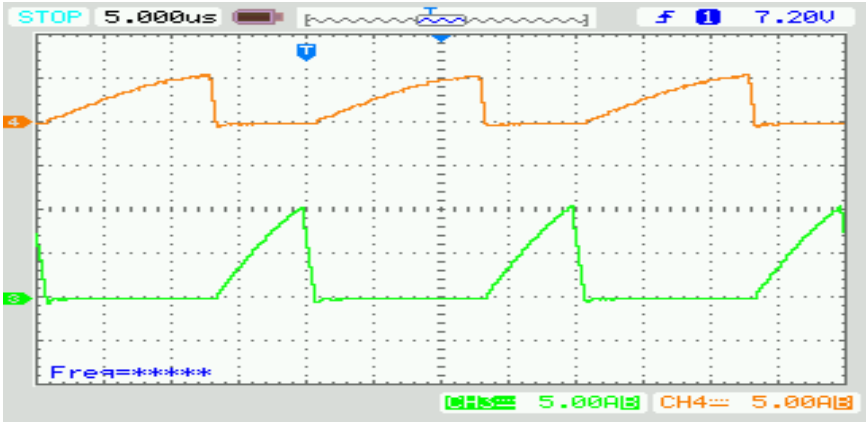
Fig. 3.10(a) - 3.18(a) show gate to source and drain to source voltages of switches. These waveforms show that almost in all operating conditions the gating signals are applied after the anti-parallel diode across the switch is turned on to ensure ZVS. Fig. 3.10(b) - 3.18(b) show input inductor current and primary voltage and current of transformer. Fig. 3.10(c) - 3.18(c) show output diodes currents. It can be seen that due to losses the diodes currents are non-linear. As we predicted through simulations the current stress on the switches and boost capacitors and output diodes is not same.



(a) v_{gs1} (CH1-10V/div), v_{ds1} (CH2-100V/div), v_{gs2} (CH3-10V/div), v_{ds2} (CH4-100V/div)

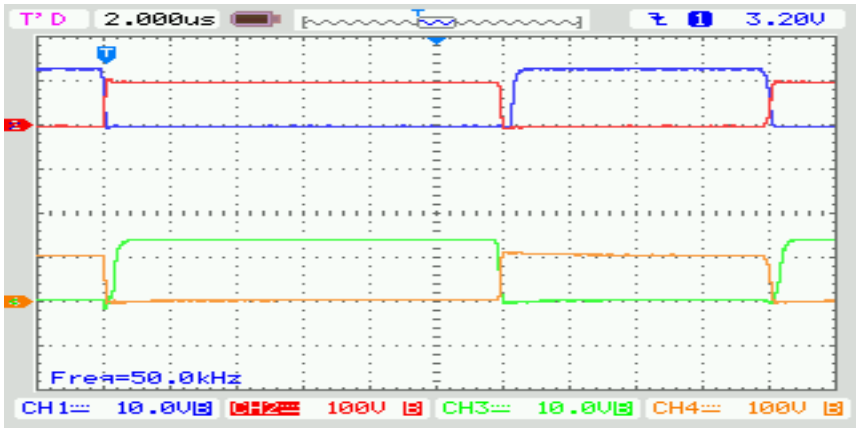


(b) v_p (CH1-50V/div), i_{in} (CH3-5A/div), i_{LK} (CH4-25A/div)

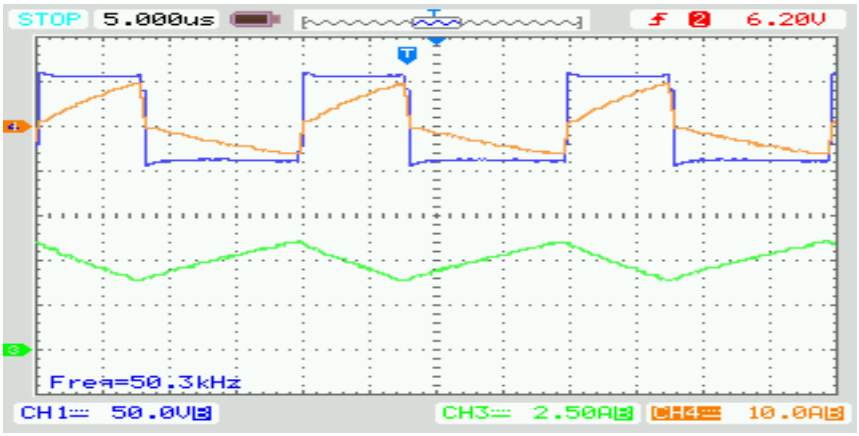


(c) i_{D3} (CH3-5A/div), i_{D4} (CH4-5A/div)

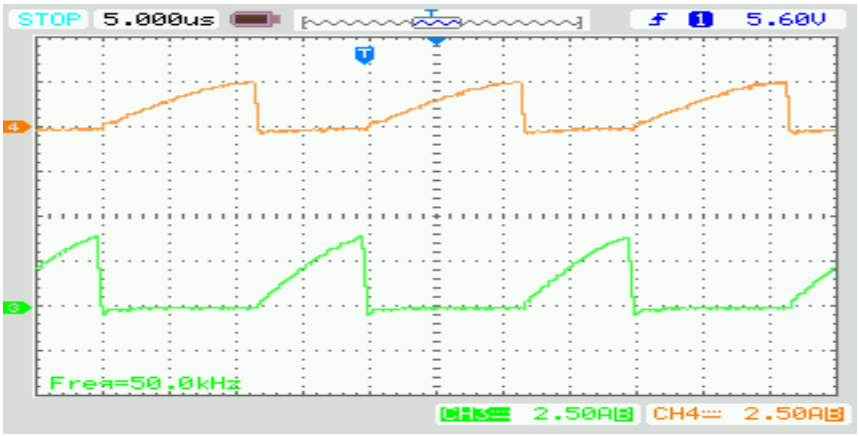
Fig. 3.10 Experimental results for V_{in} = 40 V at full-load.



(a) v_{gs1} (CH1-10V/div), v_{ds1} (CH2-100V/div), v_{gs2} (CH3-10V/div), v_{ds2} (CH4-100V/div)



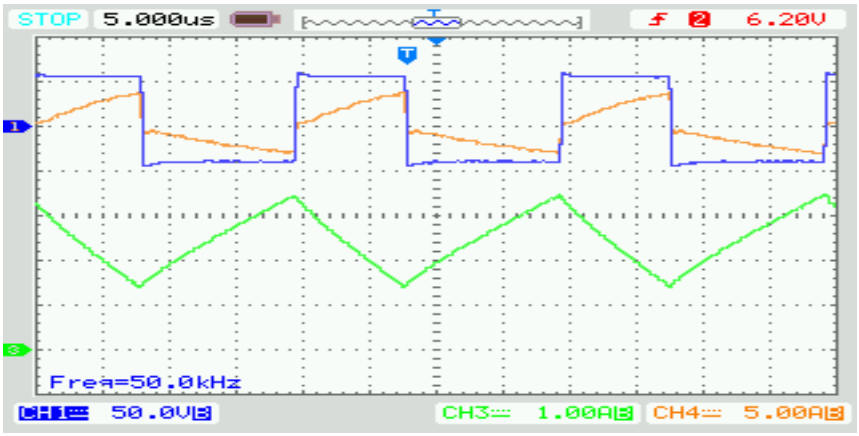
(b) v_p (CH1-50V/div), i_{in} (CH3-2.5A/div), i_{LK} (CH4-10A/div)



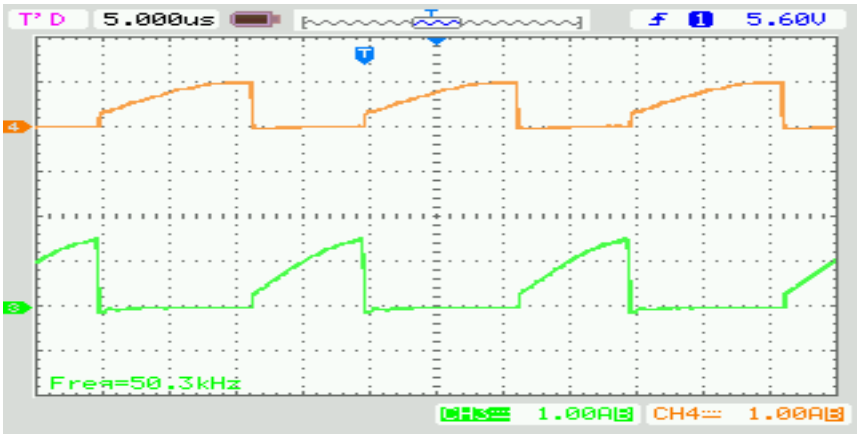
(c) i_{D3} (CH3-2.5A/div), i_{D4} (CH4-2.5A/div)

Fig.3.11 Experimental results for V_{in} = 40 V at half load.

(a) v_{gs1} (CH1-10V/div), v_{ds1} (CH2-100V/div), v_{gs2} (CH3-10V/div), v_{ds2} (CH4-100V/div)

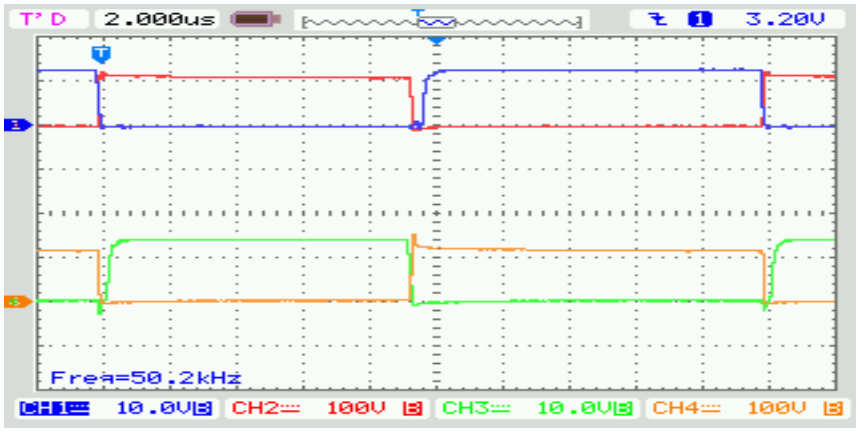


(b) v_p (CH1-50V/div), i_{in} (CH3-1A/div), i_{LK} (CH4-5A/div)

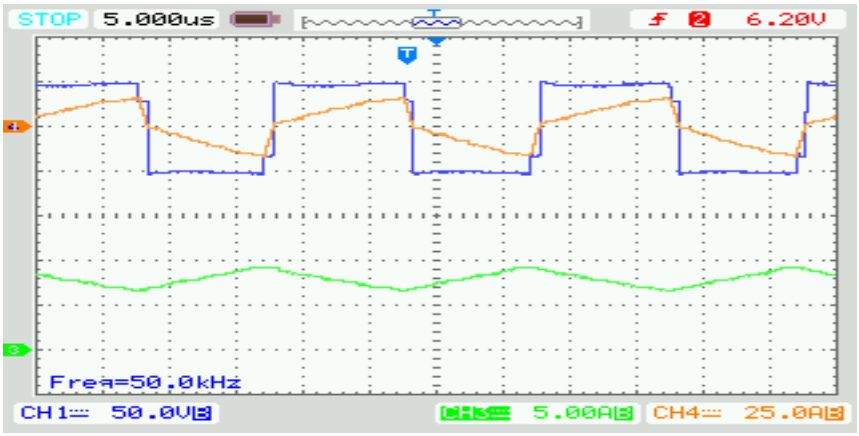


(c) i_{D3} (CH3-1A/div), i_{D4} (CH4-1A/div)

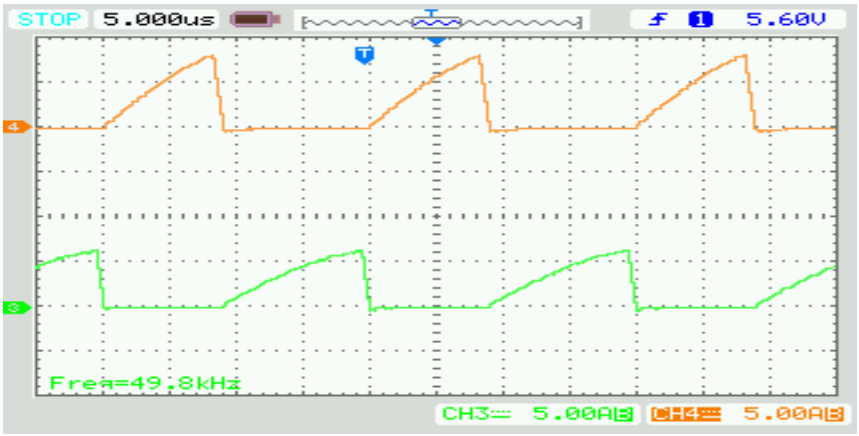
Fig. 3.12. Experimental results for V_{in} = 40V 20% load.



(a) v_{gs1} (CH1-10V/div), v_{ds1} (CH2-100V/div),v_{gs2} (CH3-10V/div), v_{ds2} (CH4-100V/div)

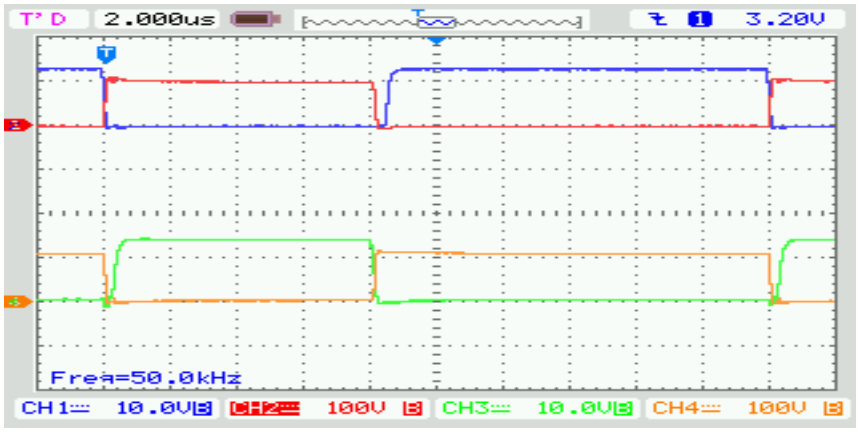


(b) v_p (CH1-50V/div), i_{in} (CH3-5A/div), i_{LK} (CH4-25A/div)

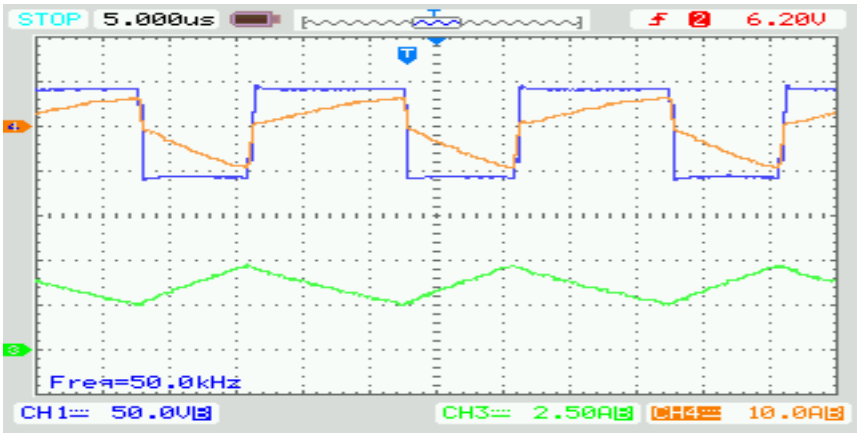


(c) i_{D3} (CH3-5A/div), i_{D4} (CH4-5A/div)

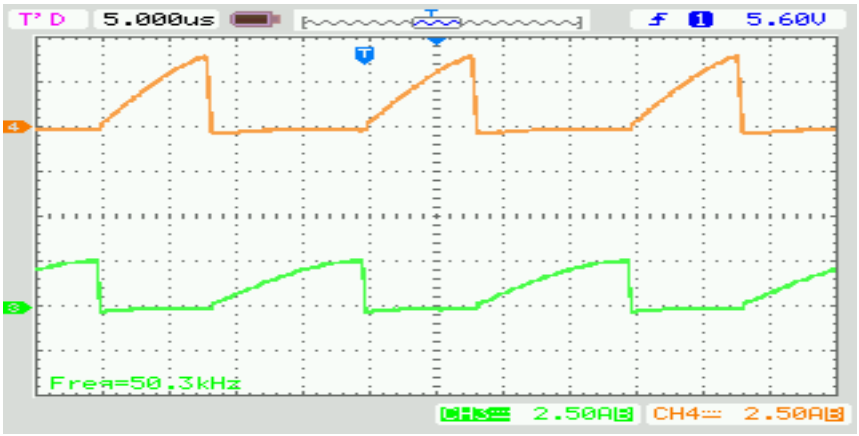
Fig. 3.13. Experimental results for V_{in} = 60 V at full-load.



(a) v_{gs1} (CH1-10V/div), v_{ds1} (CH2-100V/div), v_{gs2} (CH3-10V/div), v_{ds2} (CH4-100V/div)

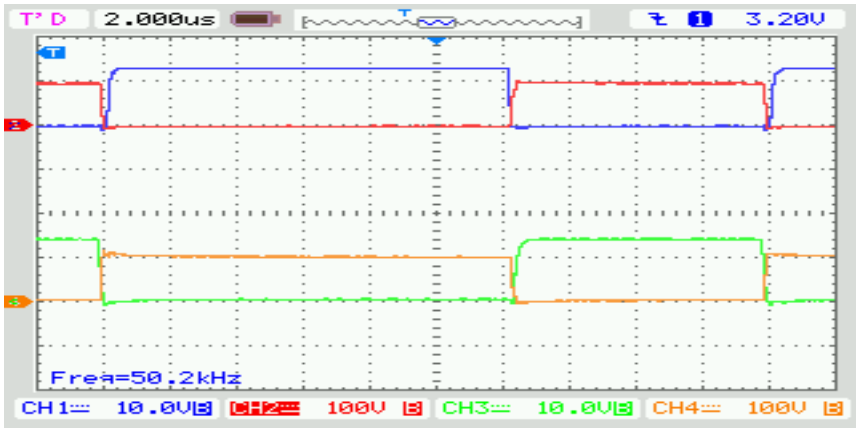


(b) v_p (CH1-50V/div), i_{in} (CH3-2.5A/div), i_{LK} (CH4-10A/div)

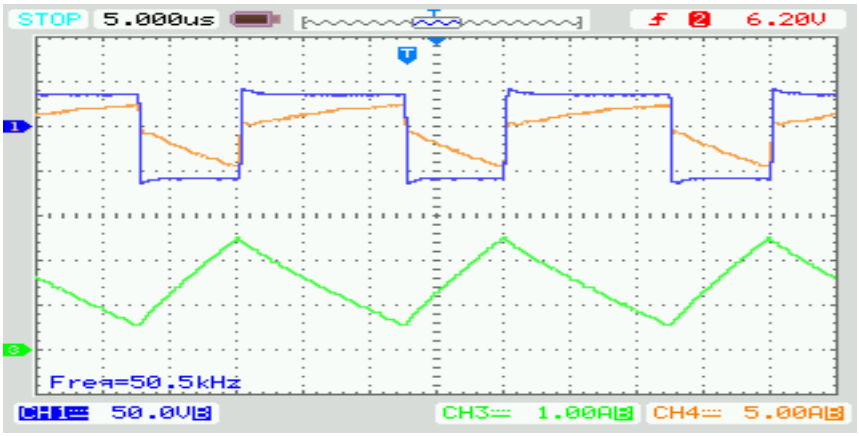


(c) i_{D3} (CH3-2.5A/div), i_{D4} (CH4-2.5A/div)

Fig. 3.14. Experimental results for V_{in} = 60 V at half-load.



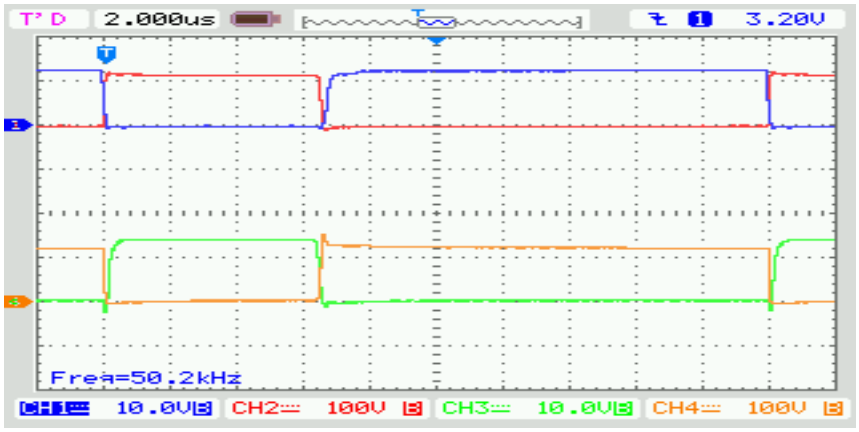
(a) v_{gs1} (CH1-10V/div), v_{ds1} (CH2-100V/div), v_{gs2} (CH3-10V/div), v_{ds2} (CH4-100V/div)



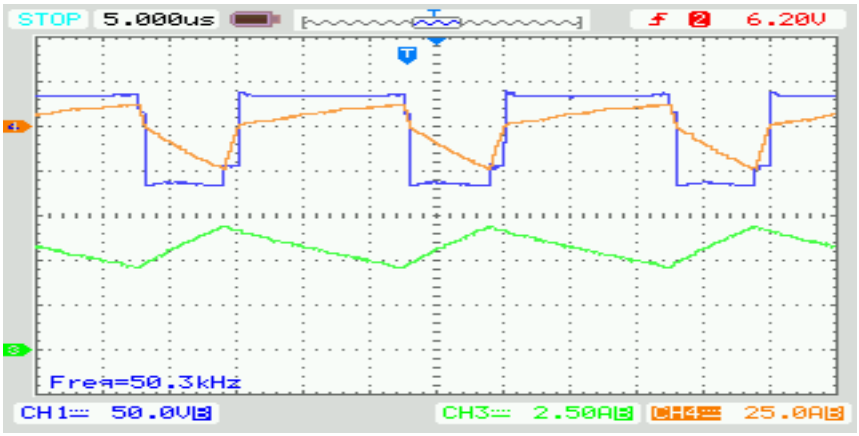
(b) v_p (CH1-50V/div), i_{in} (CH3-1A/div), i_{LK} (CH4-5A/div)

(c) i_{D3} (CH3-1A/div), i_{D4} (CH4-1A/div)

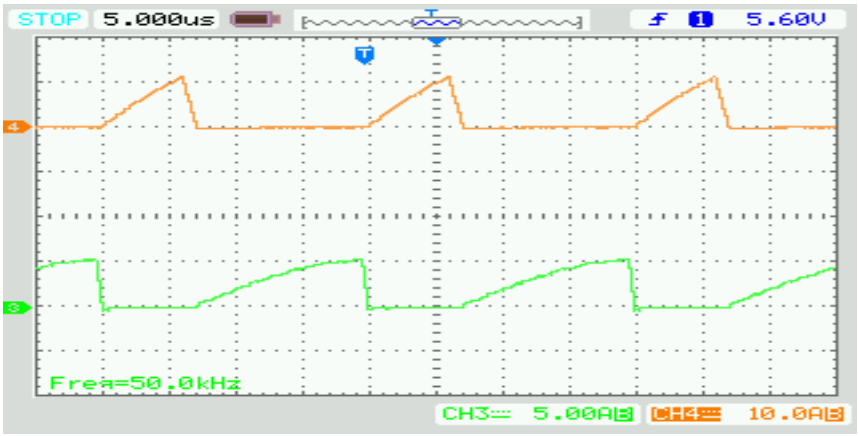
Fig. 3.15. Experimental results for V_{in} = 60 V at 20% load.



(a) v_{gs1} (CH1-10V/div), v_{ds1} (CH2-100V/div), v_{gs2} (CH3-10V/div), v_{ds2} (CH4-100V/div)

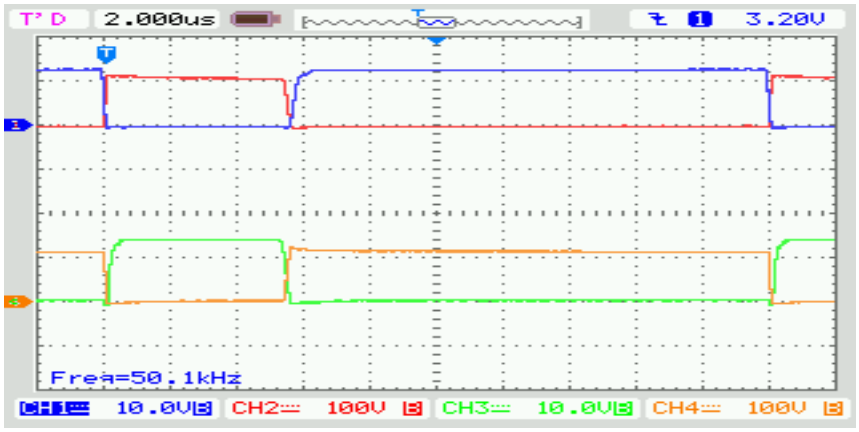


(b) v_p (CH1-50V/div), i_{in} (CH3-2.5A/div), i_{LK} (CH4-25A/div)

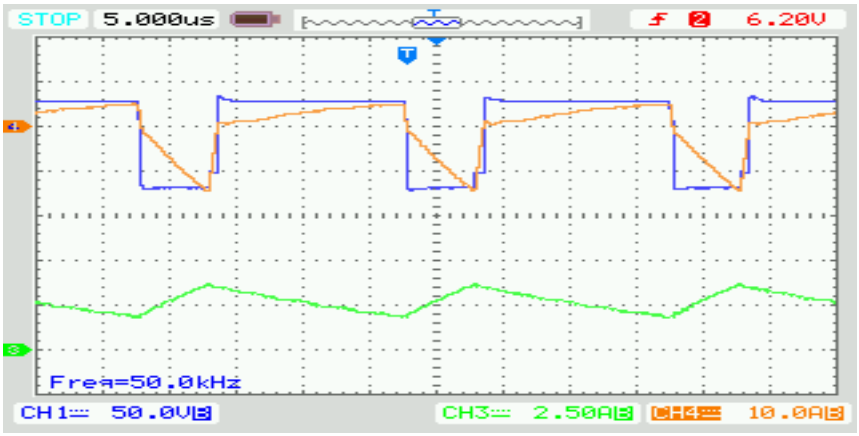


(c) i_{D3} (CH3-5A/div), i_{D4} (CH4-10A/div)

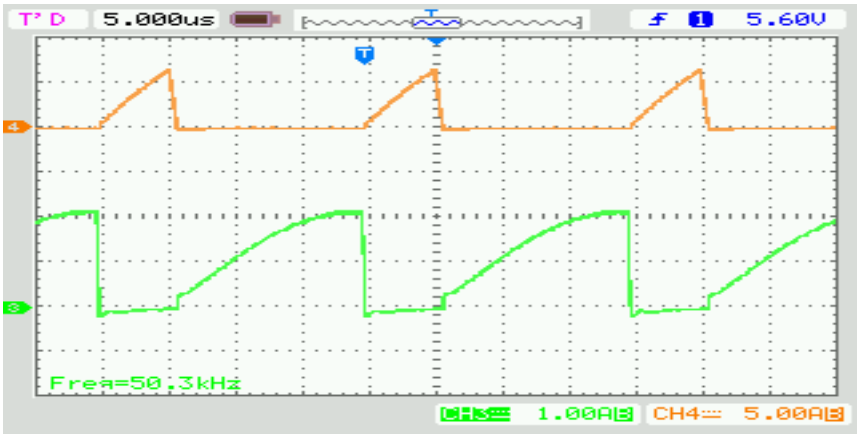
Fig. 3.16. Experimental results for V_{in} = 80 V at full-load.



(a) v_{gs1} (CH1-10V/div), v_{ds1} (CH2-100V/div), v_{gs2} (CH3-10V/div), v_{ds2} (CH4-100V/div)



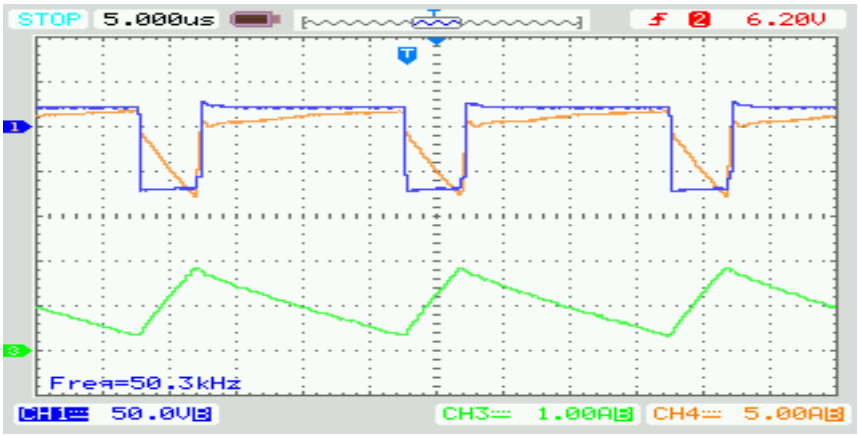
(b) v_p (CH1-50V/div), i_{in} (CH3-2.5A/div), i_{LK} (CH4-10A/div)



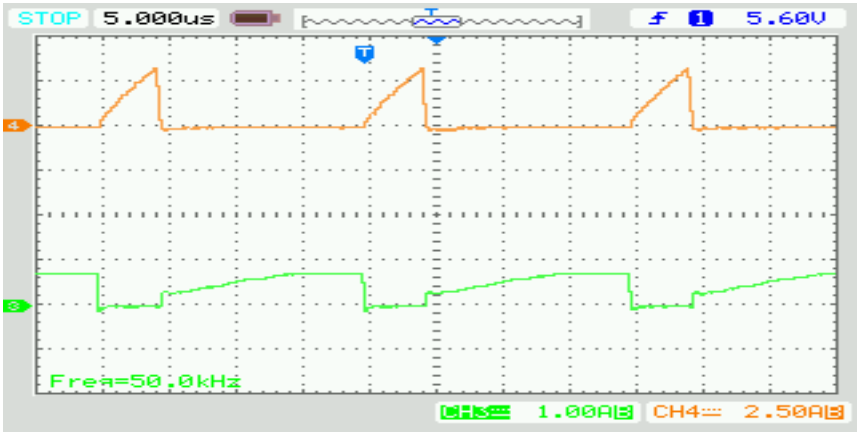
(c) i_{D3} (CH3-1A/div), i_{D4} (CH4-5A/div)

Fig. 3.17. Experimental results for V_{in} = 80 V at half-load.

(a) v_{gs1} (CH1-10V/div), v_{ds1} (CH2-100V/div), v_{gs2} (CH3-10V/div), v_{ds2} (CH4-100V/div)



(b) v_p (CH1-50V/div), i_{in} (CH3-1A/div), i_{LK} (CH4-5A/div)



(c) i_{D3} (CH3-1A/div), i_{D4} (CH4-2.5A/div)

Fig. 3.18. Experimental results for V_{in} = 80 V at 20% load.

Table 3.2 shows the results of experiment for full load and various input voltages.

Table 3.2 Experimental results for full load and various input voltages

V_{in}(V)	I_{in}(A)	P_{in}(W)	V_o(V)	I_o(A)	P_o(W)	P_{loss}(W)	Efficiency, η	Duty ratio, D
40.5	11.15	451	202	2	404	47	89.6%	0.64
60.7	7.37	447	202	2	404	43	90.4%	0.45
79.3	5.65	448	201	2	402	46	89.7%	0.33

Table 3.3 shows the results of experiment for half load and various input voltages.

Table 3.3 Experimental results for half-load and various input voltages

V_{in}(V)	I_{in}(A)	P_{in}(W)	V_o(V)	I_o(A)	P_o(W)	P_{loss}(W)	Efficiency, η	Duty ratio, D
40	5.35	214	201	1	201	13	93.9%	0.58
60	3.54	212	200	0.98	196	14	92.4%	0.4
80.2	2.7	216	201	1	201	15	93%	0.27

Table 3.4 shows the results of experiment for 20% load and various input voltages.

Table 3.4 Experimental results for 20% load and various input voltages

V_{in}(V)	I_{in}(A)	P_{in}(W)	V_o(V)	I_o(A)	P_o(W)	P_{loss}(W)	Efficiency, η	Duty ratio, D
40.1	2.29	91.8	201	0.41	82.4	9.4	89.8%	0.58
60	1.53	91.8	202	0.42	84.8	7	92.4%	0.38
80.1	1.15	92.1	202	0.42	84.8	7.3	92 %	0.2

The comparison of theoretical, simulation and experimental results for V_{in} = 40 V is given in Table 3.5 and for V_{in} = 60V and V_{in} = 80V are given in Tables 3.6 and 3.7, respectively. The differences between theoretical, simulation and experimental results are due to the fact that approximations were made in the theoretical analysis (i.e. neglecting magnetizing inductance of HF transformer, considering ideal diodes and switches and neglecting snubber effects) while in the simulation, losses were ignored. These losses include switching and conduction losses.

Table 3.5 Comparison of theoretical, simulation and experimental results for $V_{in} = V_{in(\min)} = 40$ V and different load conditions

	Full Load			Half Load			20% Load		
Parameter	Theory	Sim.	Exp.	Theory	Sim.	Exp.	Theory	Sim.	Exp.
V_o(V)	200	203	202	200	196	201	200	198	201
P_o(W)	400	412	404	200	192	201	80	78	82.4
D	0.67	0.56	0.64	0.67	0.53	0.58	0.67	0.51	0.58
$i_{in}(max)$(A)	12.2	11.4	12	6.67	6	6	3.33	2.8	3.4
$i_{in}(min)$ (A)	10	9.4	10	4.45	4.2	4	1.11	1.1	1.4
$i_{S1}(max)$(A)	10.2	14	10	5.65	6.6	6	2.94	2.8	2.6
$i_{S2}(max)$(A)	22.2	28	24	11.67	15	12	5.33	6.4	6.4
$i_{Lk}(+pk)$(A)	20.2	23	20	10.1	11	10	4.05	4	4
$i_{Lk}(-pk)$ (A)	10	16	12	5	8.6	6	2	3.6	3
$i_{D3}(max)$(A)	12.1	9.3	10	6.06	4.3	4	2.42	1.6	1.5
$i_{D4}(max)$(A)	6	6.6	5	3	3.4	2.5	1.2	1.4	1

Table 3.6 Comparison of theoretical, simulation and experimental results for $V_{in} = 60$V and different load conditions

	Full Load			Half Load			20% Load		
Parameter	Theory	Sim.	Exp.	Theory	Sim.	Exp.	Theory	Sim.	Exp.
V_o(V)	200	200	202	200	200	200	200	199	202
P_o(W)	400	400	404	200	200	196	80	79	84.8
D	0.5	0.38	0.45	0.5	0.33	0.4	0.5	0.29	0.38
$i_{in}(max)$(A)	8.65	7.6	9	4.95	4.2	4.5	2.73	2	2.5
$i_{in}(min)$ (A)	6.15	5.7	6.5	2.45	2.5	2.5	0.23	0.6	0.6
$i_{S1}(max)$(A)	7.21	10	8.5	4.23	4.9	3.5	2.44	2.2	1.9
$i_{S2}(max)$(A)	22	32	29	11.6	18	14.5	5.4	8.6	7
$i_{Lk}(+pk)$(A)	13.36	16	15	6.68	7.5	6	2.67	2.8	2.5
$i_{Lk}(-pk)$ (A)	13.36	24	20	6.68	14	10	2.67	6.5	4.5
$i_{D3}(max)$(A)	8	6.4	6	4	3	2.5	1.6	1.1	0.9
$i_{D4}(max)$(A)	8	9.7	8	4	5.6	4	1.6	2.6	1.7

Table 3.7 Comparison of theoretical, simulation and experimental results for $V_{in} = V_{in(\max)} = 80$ V and different load conditions

	Full Load			Half Load			20% Load		
Parameter	Theory	Sim.	Exp.	Theory	Sim.	Exp.	Theory	Sim.	Exp.
V_o(V)	200	202	201	200	201	201	200	200	202
P_o(W)	400	408	402	200	202	201	80	80	84.8
D	0.33	0.26	0.33	0.33	0.2	0.27	0.33	0.15	0.2
$i_{in}(max)$(A)	6.66	6	7	3.88	3.2	3.7	2.21	1.5	1.8
$i_{in}(min)$ (A)	4.46	4.3	4.5	1.68	1.9	1.8	0	0.5	0.4
$i_{S1}(max)$(A)	5.54	9.6	7.5	3.32	4.4	3.2	2	1.8	1.6
$i_{S2}(max)$(A)	26.9	38.6	32	14	24	17.7	6.26	13	9.8
$i_{Lk}(+pk)$(A)	10	13.9	12	5	6.3	5	2	2.3	2
$i_{Lk}(-pk)$ (A)	20.2	32.6	25	10.1	21	14	4.05	11.5	8
$i_{D3}(max)$(A)	6	5.6	5	3	2.5	2.2	1.2	0.93	0.7
$i_{D4}(max)$(A)	12.1	13.2	11	6.06	8.4	6	2.42	4.6	3.2

Fig. 3.19 shows the photograph of the experimental set-up built and used in the lab.

Fig. 3.19 Photograph of the experimental setup of boost integrated HF isolated half-bridge dc-dc converter.

3.3 Conclusions

In this chapter simulation and experimental results for the converter designed in Chapter 2 are presented. The experimental results show close agreement with the theoretical analysis. Major advantages of the converter are: simple structure with only two switches and soft-switching for the switches and diodes from full load to light load. The disadvantages are that the current stress on the switches and output diodes is not the same and peak currents are high.

Chapter 4

Conclusion

4.1 Summary of Work Done

In this report a boost integrated half bridge HF transformer isolated DC-DC converter for use in photovoltaic applications was discussed.

In the first chapter we reviewed and compared some DC-DC step-up converters with transformer isolation. Based on our comparison we selected a configuration that has maximum efficiency, minimum number of switches and simple structure. This converter has the advantages such as high-voltage conversion ratio, low input current ripple and soft switching for all switches. In Chapter 2 we analyzed the selected converter and the equivalent circuits for different time intervals were given. Then we found the design equations for steady-state operation of the converter and in the last section of Chapter 2 we designed the converter for the required specifications.

Simulation and experimental results for the converter were presented in Chapter 3. These results showed that for the whole input voltage range the converter works in ZVS from full load to light load. It was observed that besides the many advantages of this configuration the disadvantages are that the current stress on the switches and output diodes is not the same and peak currents are high.

4.2 Suggestions for future work

Some suggestions for future work are summarized below:

1) As mentioned before the only disadvantage of the selected converter is that the current stress on the switches and output diodes is not the same. So the configuration needs some changes to solve this issue.
2) The output voltage of the converter is currently regulated by using open loop control. In the future a closed loop control system has to be built that incorporates peak power point tracking for the PV array to obtain maximum output power.
3) In order to complete the PV system, a dc-ac inverter is required for the grid connection purpose.

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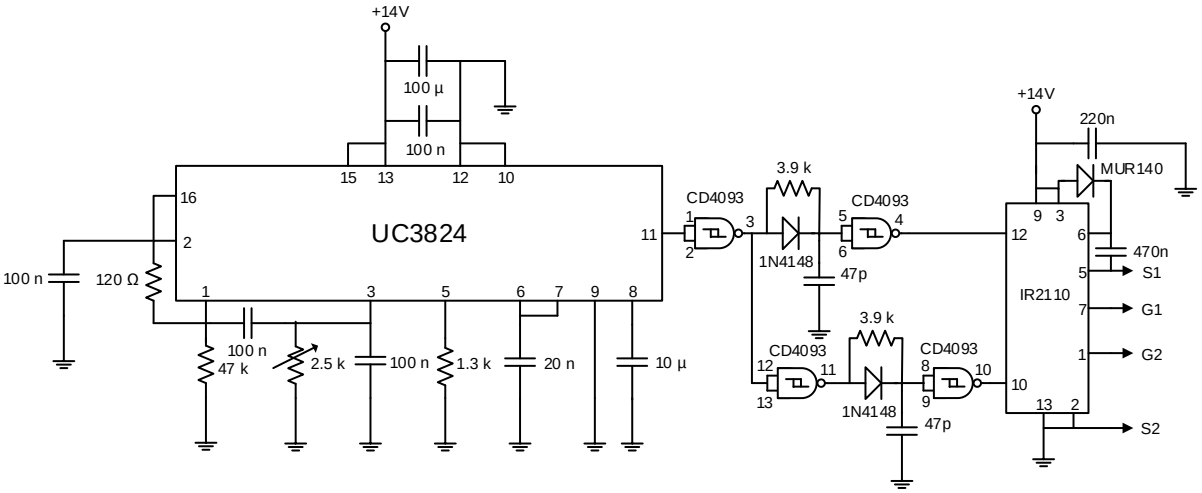
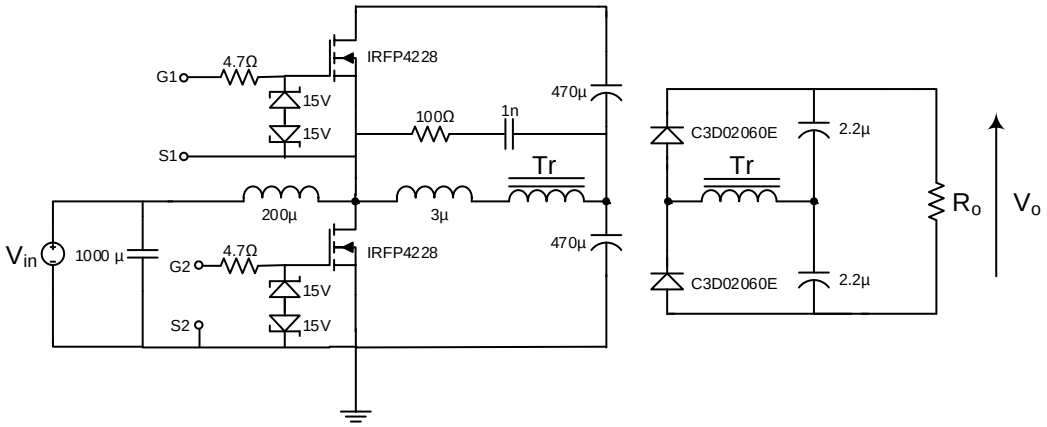
Appendix 1

Schematic Diagram of the Experimental Converter

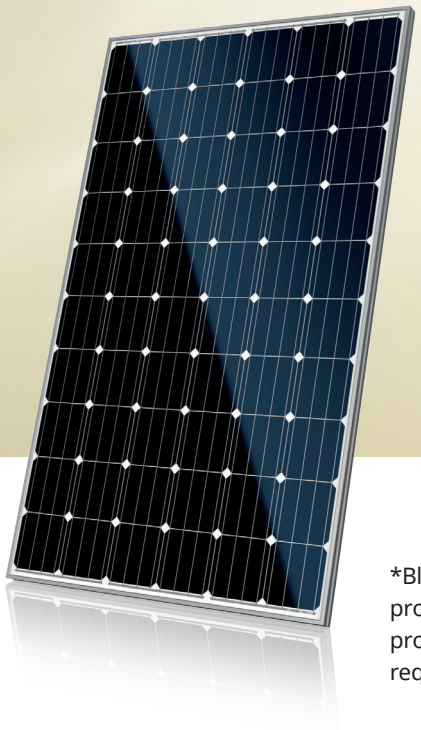




Appendix 2

Photo Voltaic Module Specifications

CanadianSolar



CS6P-260|265|270M

*Black frame product can be provided upon request.

High quality and reliability in all Canadian Solar modules is ensured by 13 years' experience in module manufacturing, well-engineered module design, stringent BOM quality testing, an automated manufacturing process and 100 % EL testing.

KEY FEATURES

- Excellent module efficiency up to 16.79 %
- Outstanding low irradiance performance > 96.5 %
- +5Wp — Positive power tolerance up to 5 W
- No. 1 PTC — High PTC rating up to 91.36 %
- IP67 junction box for long-term weather endurance
- Heavy snow load up to 5400 Pa wind load up to 2400 Pa
- Salt mist, ammonia and blown sand resistance, for seaside, farm and desert environments

25 years — **insurance-backed warranty**
non-cancellable, immediate warranty insurance
linear power output warranty

10 years — **product warranty on materials and workmanship**

MANAGEMENT SYSTEM CERTIFICATES

ISO 9001: 2008 / Quality management system
ISO/TS 16949:2009 / The automotive industry quality management system
ISO 14001:2004 / Standards for environmental management system
OHSAS 18001:2007 / International standards for occupational health & safety

PRODUCT CERTIFICATES

IEC 61215 / IEC 61730: VDE / MCS / CE / CEC AU / CQC
UL 1703 / IEC 61215 performance: CEC listed (US) / FSEC (US Florida)
UL 1703: CSA / IEC 61701 ED2: VDE / IEC 62716: TUV / IEC 60068-2-68: SGS
PV CYCLE (EU) / UNI 9177 Reaction to Fire: Class 1

CANADIAN SOLAR INC. is committed to providing high quality solar products, solar system solutions and services to customers around the world. As a leading manufacturer of solar modules and PV project developer with about 8 GW of premium quality modules deployed around the world since 2001, Canadian Solar Inc. (NASDAQ: CSIQ) is one of the most bankable solar companies worldwide.

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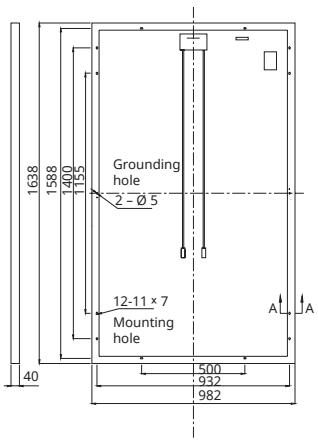
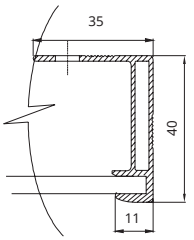
545 Speedvale Avenue West, Guelph, Ontario N1K 1E6, Canada, www.canadiansolar.com, support@canadiansolar.com

MODULE / ENGINEERING DRAWING (mm)

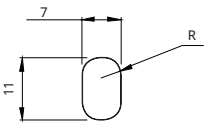
Rear View



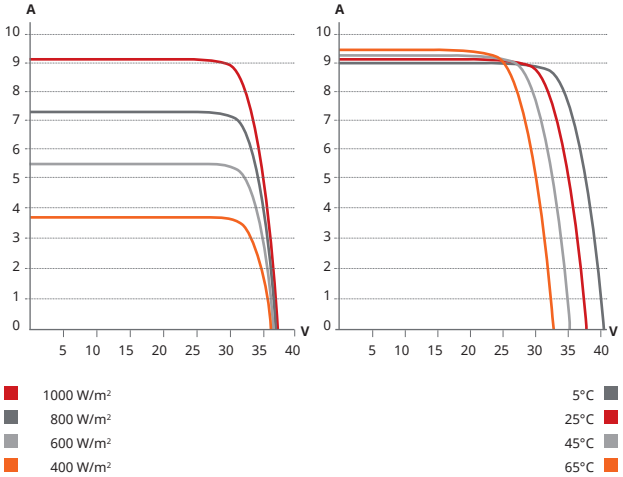
Frame Cross Section A-A



Mounting Hole



CS6P-265M / I-V CURVES



ELECTRICAL DATA / STC*

Electrical Data CS6P	260M	265M	270M
Nominal Max. Power (Pmax)	260 W	265 W	270 W
Opt. Operating Voltage (Vmp)	30.7 V	30.9 V	31.1 V
Opt. Operating Current (Imp)	8.48 A	8.61 V	8.67 A
Open Circuit Voltage (Voc)	37.8 V	37.9 V	38.2 V
Short Circuit Current (Isc)	8.99 A	9.11 A	9.19 A
Module Efficiency	16.16%	16.47%	16.79%
Operating Temperature	-40°C ~ +85°C		
Max. System Voltage	1000 V (IEC) or 1000 V (UL) or 600 V (UL)		
Module Fire Performance	TYPE 1 (UL 1703) or CLASS C (IEC61730)		
Max. Series Fuse Rating	15 A		
Application Classification	Class A		
Power Tolerance	0 ~ + 5 W		

* Under Standard Test Conditions (STC) of irradiance of 1000 W/m², spectrum AM 1.5 and cell temperature of 25°C.

ELECTRICAL DATA / NOCT*

Electrical Data CS6P	260M	265M	270M
Nominal Max. Power (Pmax)	188 W	191 W	195 W
Opt. Operating Voltage (Vmp)	28.0 V	28.2 V	28.4 V
Opt. Operating Current (Imp)	66.70 A	6.79 A	6.87 A
Open Circuit Voltage (Voc)	34.7 V	34.8 V	35.0 V
Short Circuit Current (Isc)	7.28 A	7.37 A	7.44 A

* Under Nominal Operating Cell Temperature (NOCT), irradiance of 800 W/m², spectrum AM 1.5, ambient temperature 20°C, wind speed 1 m/s.

PERFORMANCE AT LOW IRRADIANCE

Industry leading performance at low irradiation, +96.5 % module efficiency from an irradiance of 1000 W/m² to 200 W/m² (AM 1.5, 25°C).

As there are different certification requirements in different markets, please contact your sales representative for the specific certificates applicable to your products. The specification and key features described in this Datasheet may deviate slightly and are not guaranteed. Due to on-going innovation, research and product enhancement, Canadian Solar Inc. reserves the right to make any adjustment to the information described herein at any time without notice. Please always obtain the most recent version of the datasheet which shall be duly incorporated into the binding contract made by the parties governing all transactions related to the purchase and sale of the products described herein.

MODULE / MECHANICAL DATA

Specification	Data
Cell Type	Mono-crystalline, 6 inch
Cell Arrangement	60 (6 × 10)
Dimensions	1638×982×40 mm (64.5×38.7×1.57 in)
Weight	18 kg (39.7 lbs)
Front Cover	3.2 mm tempered glass
Frame Material	Anodized aluminium alloy
J-BOX	IP67, 3 diodes
Cable	4 mm² (IEC) or 4 mm² & 12 AWG 1000 V (UL1000 V) or 12 AWG (UL600V), 1000 mm
Connectors	MC4 or MC4 comparable
Stand. Packaging	24 pcs, 480 kg (quantity & weight per pallet)
Module Pieces per Container	672 pcs (40'HQ)

TEMPERATURE CHARACTERISTICS

Specification	Data
Temperature Coefficient (Pmax)	-0.45% / °C
Temperature Coefficient (Voc)	-0.35% / °C
Temperature Coefficient (Isc)	0.060% / °C
Nominal Operating Cell Temperature	45±2°C

PARTNER SECTION

Caution: Please read safety and installation instructions before using the product.