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-- Company:

-- Engineer:

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-- Create Date: 26.10.2015 21:08:08

-- Design Name:

-- Module Name: exe1\_b - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity exe1\_b is

Port (

input\_w : in std\_logic;

a\_data : in std\_logic\_vector(7 downto 0);

b\_data : in std\_logic\_vector(7 downto 0);

clk : in std\_logic;

dat\_4 : out std\_logic\_vector(7 downto 0);

dat\_5 : out std\_logic\_vector(2 downto 0)

);

end exe1\_b;

architecture Behavioral of exe1\_b is

begin

end Behavioral;