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-- Company:

-- Engineer:

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-- Create Date: 26.10.2015 22:02:15

-- Design Name:

-- Module Name: exe3 - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.numeric\_std.all;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity exe3 is

end exe3;

architecture Behavioral of exe3 is

signal slv : std\_logic\_vector(7 downto 0);

signal s : signed(7 downto 0);

signal us : unsigned(7 downto 0);

signal i : integer range 0 to 12;

begin

-- Signed

slv <= std\_logic\_vector(s);

us <= unsigned(std\_logic\_vector(s));

i <= to\_integer(s);

-- std\_logic\_vector

s <= signed(slv);

us <= unsigned(slv);

i <= to\_integer(signed(slv));

-- unsigned

slv <= std\_logic\_vector(us);

s <= signed(std\_logic\_vector(us));

i <= to\_integer(us);

-- integer

slv <= std\_logic\_vector(to\_signed(i,8));

s <= to\_signed(i,8);

us <= to\_unsigned(i,8);

end Behavioral;