----------------------------------------------------------------------------------

-- Company:

-- Engineer:

--

-- Create Date: 26.10.2015 21:39:12

-- Design Name:

-- Module Name: exe2 - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

--

-- Dependencies:

--

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity exe2 is

Port (

a : in std\_logic;

b : in std\_logic;

c : in std\_logic;

d : in std\_logic;

s1 : out std\_logic;

s2 : out std\_logic;

s3 : out std\_logic;

s4 : out std\_logic

);

end exe2;

architecture Behavioral of exe2 is

begin

s1 <= a or (not b);

s2 <= a or ((not b) and c) or d;

s3 <= (a or (not b)) and (c or d);

s4 <= (a or (not b)) and (not(c or (a and d)));

end Behavioral;