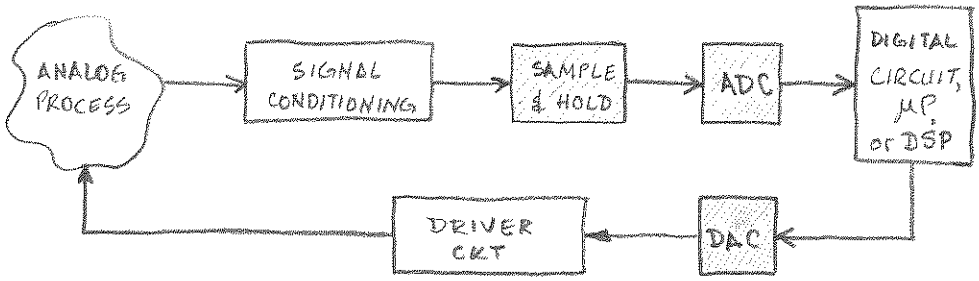
DATA CONVERSION CIRCUITS

Typical process control configuration

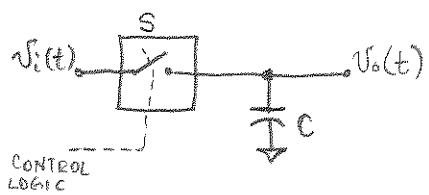


Sample & Hold Circuits (S/H)

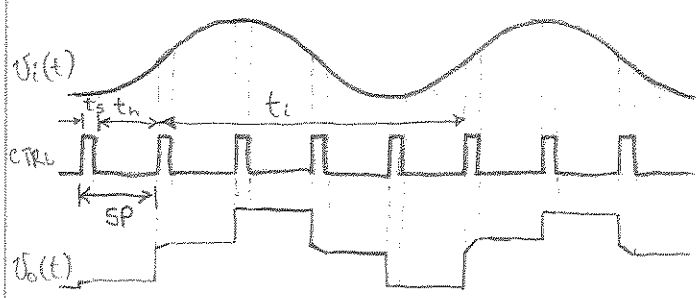
- Provide a stable DC signal for the conversion time of an ADC.
- Should operate at the required sampling rate required by application:
  - Nyquist criterion: The minimum rate at which a signal can be sampled to allow its unique reproduction is twice the maximum frequency component of the input signal.

$$f_s \geq 2 \times f_{i\,max}$$

  - Violating the Nyquist criterion produces a spectral folding in the reproduced signal calle aliasing.
- Idealized S/H circuit:



- Switch S is closed during sample period.
- When S is opened after sampling, capacitor C holds the last value of v_i during sampling



SP = Sampling period

t_s = Sample time

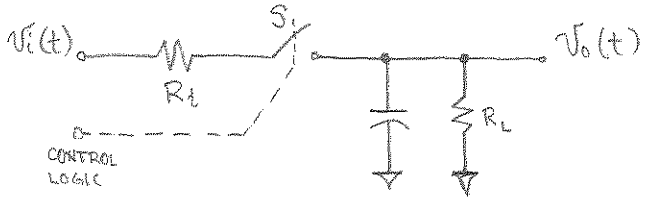
t_h = holding

t_i = Period of $v_i(t)$

Usually $t_s \ll SP \ll t_i$

Idealized behavior (assumes $R_i = 0$ and $R_L = \infty$)

• A more realistic representation of a S/H circuit

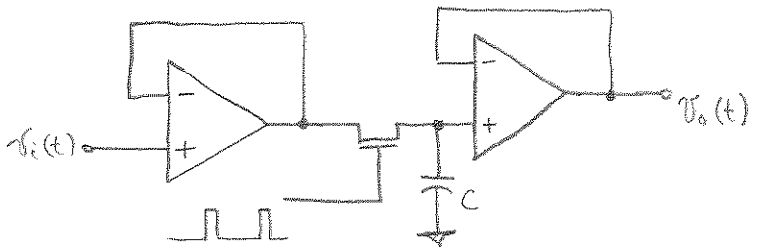


R_i = Output impedance of $V_i(t)$ & switch resist.

R_L = Input impedance of $V_o(t)$ & capacitor leak

• Implementations try to make $R_i \to 0$ and $R_L \to \infty$

• Basic Open-Loop S/H circuit



• NMOS used as switch

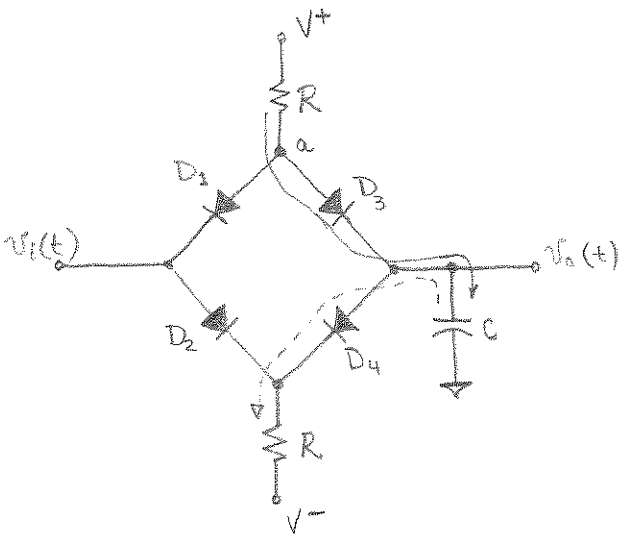
• Voltage follower provide
- Low R_o
- High R_i

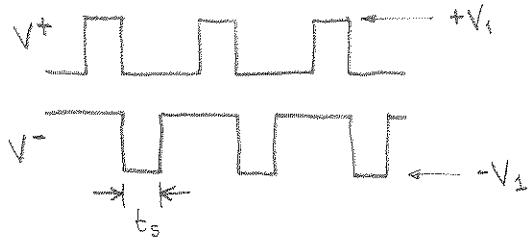
• Charging time constant

$\tau_a = R_a C = (R_o + r_{ds_{on}})C \to$ small

• Discharging time constant $\tau_b = R_b C = (R_i + r_{leak})C \to$ large

• Diode Bridge S/H circuit





• When $|V_i(t)| < V_1 - V_f$, C charges to V_i through R. $V_o(t) = V_i(t)$

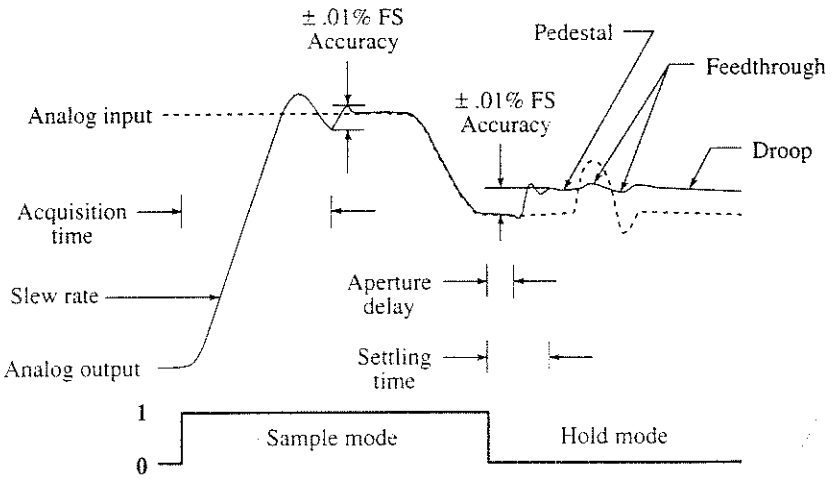
• When $V_i(t) < V_o(t-1)$, C discharges through R, $V_o(t) = V_i(t)$

• Usually S/H circuit should be phisically close to ADC

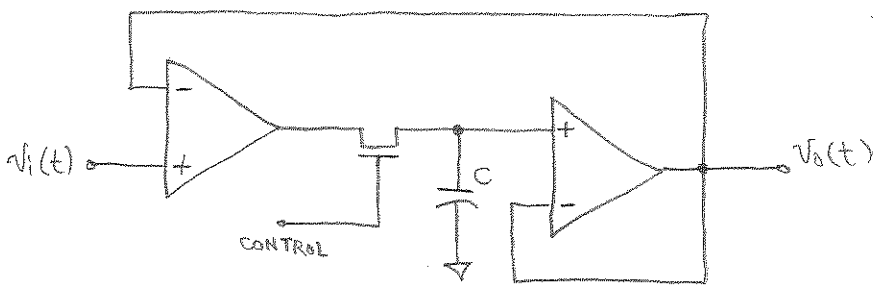
• Capacitors of polycarbonate, polyethylene, or polystyrene are recommended for C. DO NOT USE TANTALUM CAPACITORS

- This to reduce the effect of dielectric absorbtion

S/H Parameters



- Acquisition time: Time required for C to charge to a specific percentage of $V_i(t)$
  - Typical specs call for ± 0.01% i.e. $t_{ACQ} = 9RaC$
  - For small Ra values, critical factor is opamp slew rate ($I_{O\,max}$)
- Aperture delay: Time between hold command and switch aperture
- Droop Rate: Rate of decay of stored voltage
- Setting time: Time for output to settle after a hold command
- Slew Rate: Maximum rate of change of the stored voltage.
- Other: Pedestal error, Feedthrough
- Closed-loop S/H circuit



- Hi-Rq accuracy low-frequency tracking
- Feedback loop forces output to track input

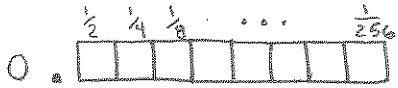
- Provides fast acquisition and settling times.
- More strict settling time requirements than open-loop S/H

DAC Input and ADC Output

- Commonly in NATURAL BINARY

$$N = a_{-1}2^{-1} + a_{-2}2^{-2} + \cdots + a_{-n}2^{-n} = \sum_{i=1}^{n} (a_{-i}2^{-i})$$

$$a_i \in \{0, 1\}$$



← Left Justified format

↑ Implied binary point

A voltage value is obtained as $V_o = N V_{FS}$

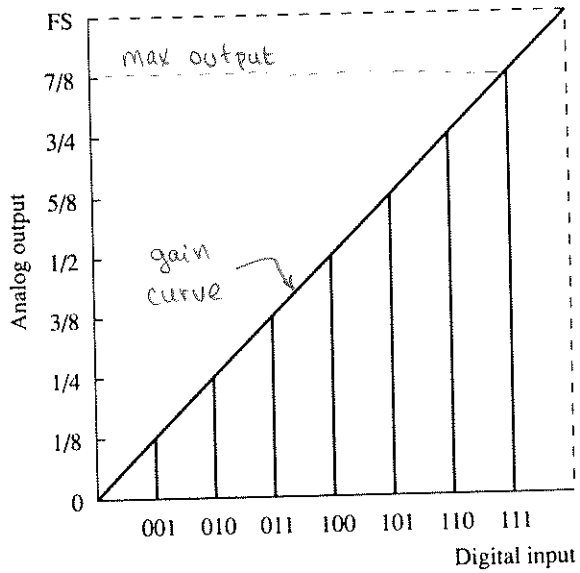
V_{FS} = Full scale voltage (maximum value)

$V_{o(FS)} = (1 - 2^{-n}) V_{FS}$

LSB change $V_{LSB} = \frac{V_{FS}}{2^n}$: Defines converter resolution

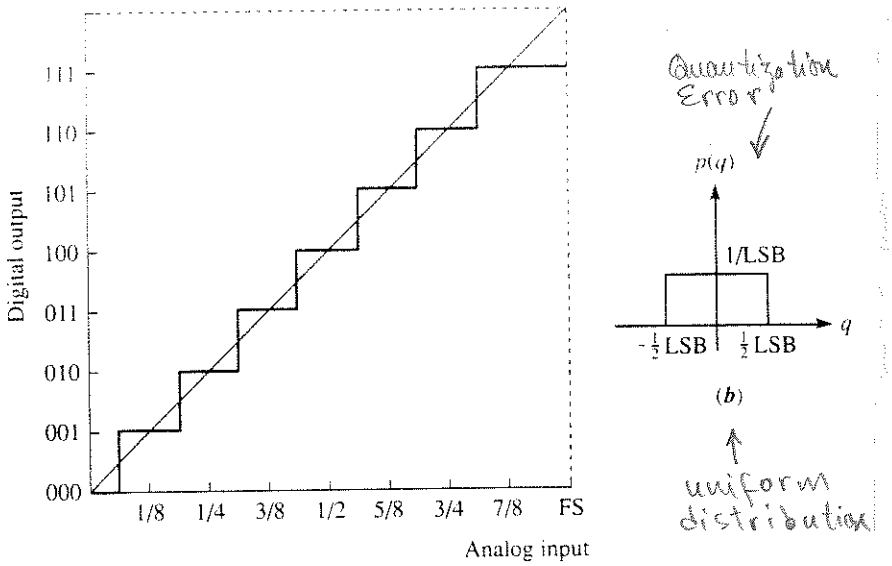
- An n-bit DAC has 2^n coded levels.

Example: A 3-bit DAC, Transfer function



- Note the maximum output value $V_{o(FS)} < V_{FS}$ by 1 LSB
- This example is an unipolar output DAC : Only positive voltage values

- Transfer Function of an unipolar ADC with $-\frac{1}{2}$LSB offset at zero scale



- Quantization: Process of digitizing ADC samples into discrete ranges
- Quantization Error: Introduced by quantization process.
- Transfer function offset: shifts transfer function to reduce quantization error

Offset: $-\frac{1}{2}$ LSB → Q.E. = $\pm$LSB/2

Offset = 0 → Q.E. = 1 LSB

- Signal-to-noise ratio (SNR) of an ADC: Measures proportion of noise introduced by quantization process

$$SNR = 10 \log(\text{Signal}/\text{Noise})$$

$$\text{Signal} = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} s^2(t)\,dt$$

$$\text{Noise} = \int_{-\infty}^{\infty} q^2 p(q)\,dq$$

$p(q)$ ← Probability density function of error.

For an ADC with $-\frac{1}{2}$LSB offset $\quad \text{Noise} = \dfrac{V_{FS}^2}{3 \times 2^{2(n+1)}}$

- Increasing number of bits increases SNR

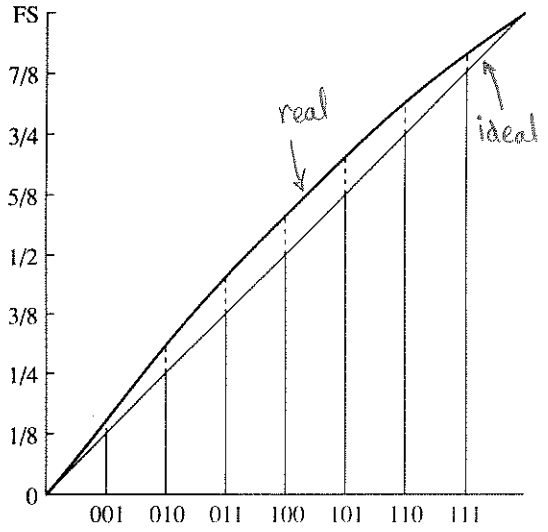
• Converter Specifications

- Resolution: Smallest incremental change in
  - Input (detection) in an ADC
  - Output (resolved) in DAC

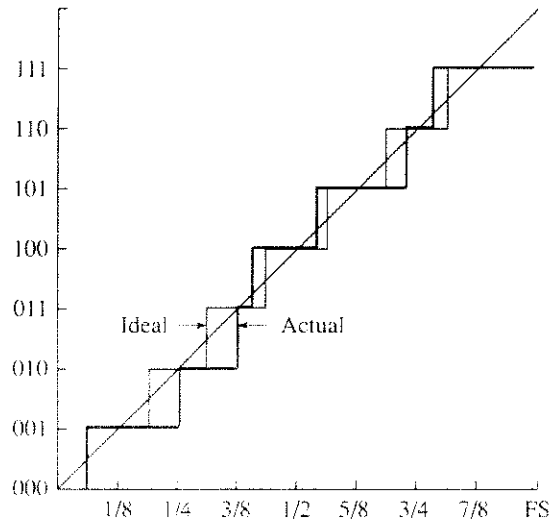
$$\text{Resolution} = \frac{1}{2^n} \times 100\ \%$$

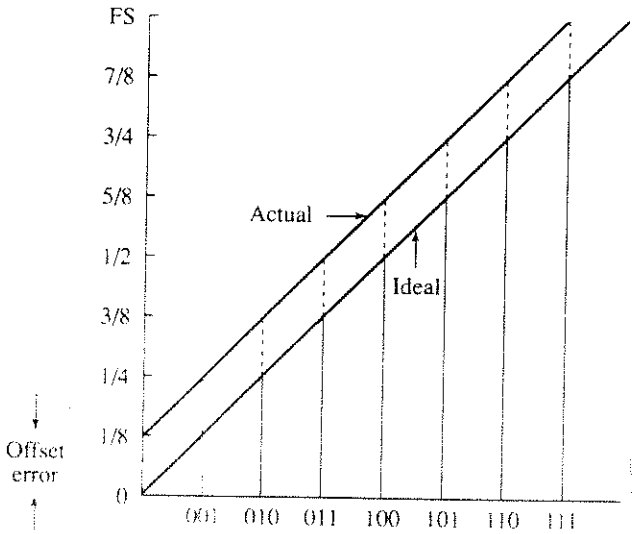
- Accuracy: Worst case deviation of output with respect to actual input value. Includes errors from:
  - Quantization
  - System noise
  - Non-linearity
  - Offset error

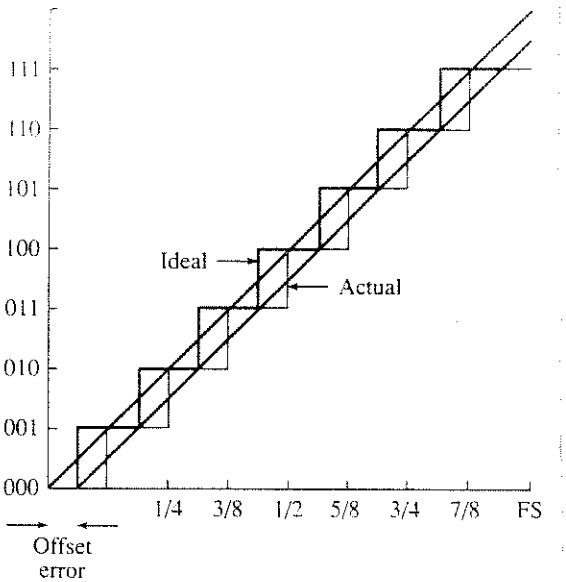
DAC nonlinearity



ADC nonlinearity

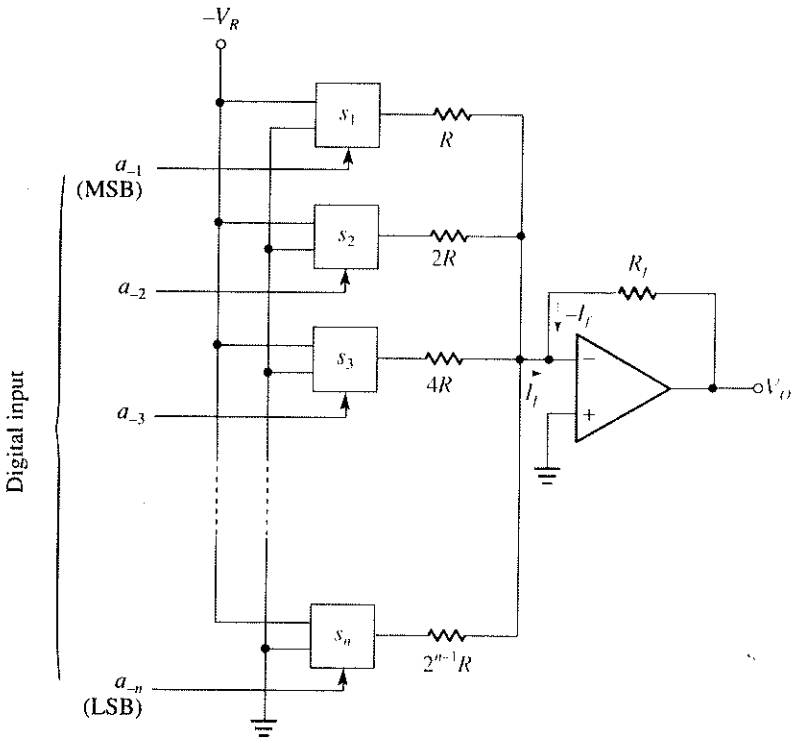






Digital-to-Analog Conversion

- Simplest circuit: Using binary-weighted resistors



$i = 1, 2, \ldots, n$

$R_i = 2^{i-1} R$

$I_f = \sum_i I_i$

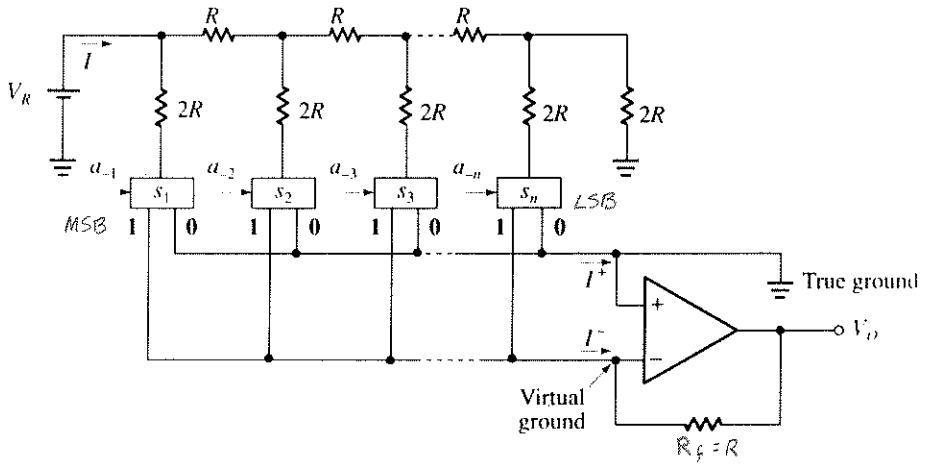
$I_f = \frac{-2 V_R N}{R}$

So $V_o = -I_f R_f$

$$V_o = \frac{2R_f}{R} V_R N$$

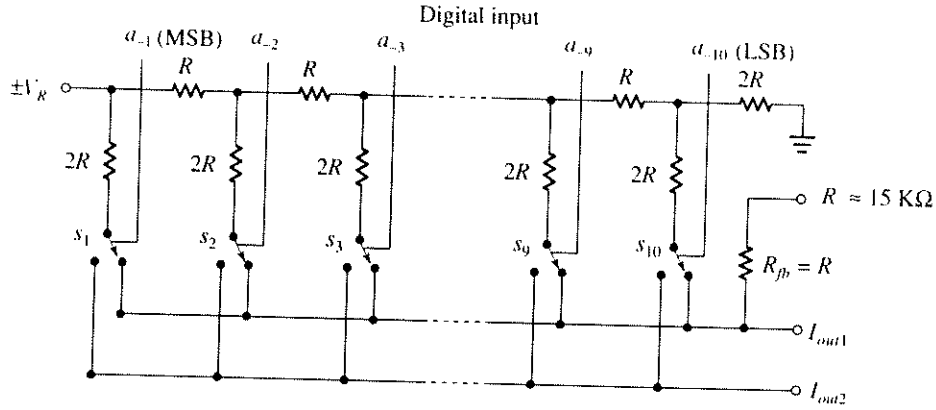
* Impractical because of values of Resistors.

- Ladder type DAC



- $I = V_R / R$
- Binary weighted currents on each branch
- Easy to implement because only two different resistors: R & $2R$

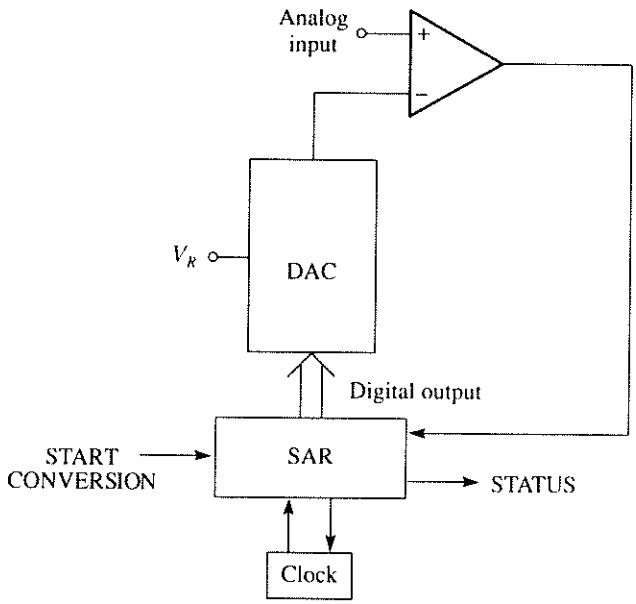
Multiplying DAC : Uses a variable V_R



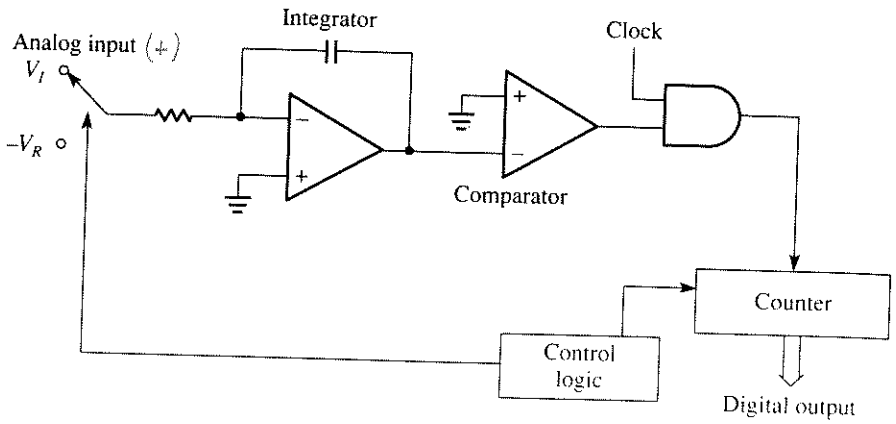
Requires external current-to-voltage converter to provide voltage output

Analog-to-Digital Converters

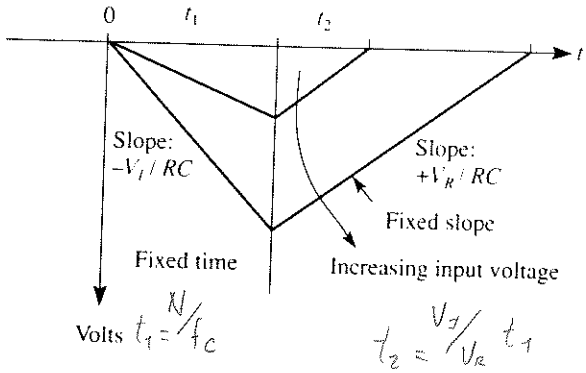
- Successive approximation ADC :
  - Bit are sequentially set from MSB to LSB until conversion is complete.
  - Only the bits making $V_c < V_i$ are left on in each step
  - Take n clock cycles to complete a conversion



- Dual-slope ADC :
  - Converts analog input to a time function
  - Time function controls counting time of of a counter which provides a digital output



(a)



$t_1 = N/f_c$

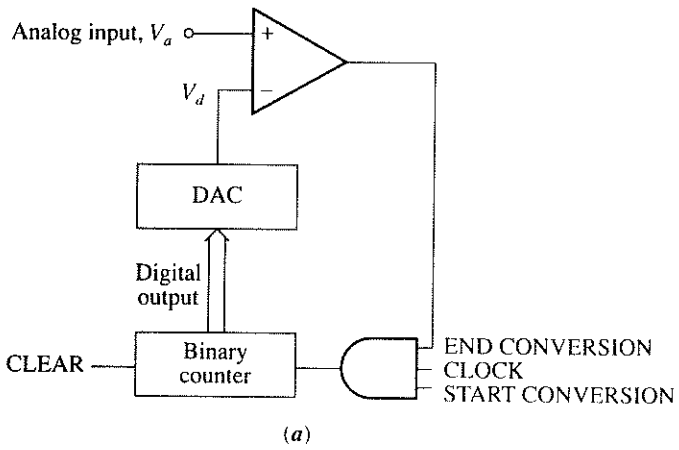
$t_2 = \frac{V_I}{V_R} t_1$

$n = \frac{N}{V_{FS}} V_I$

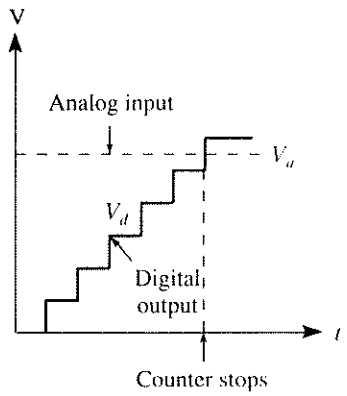
$t_1 \propto f_c$

(b)

- Counting ADC : Replaces SAR by counter



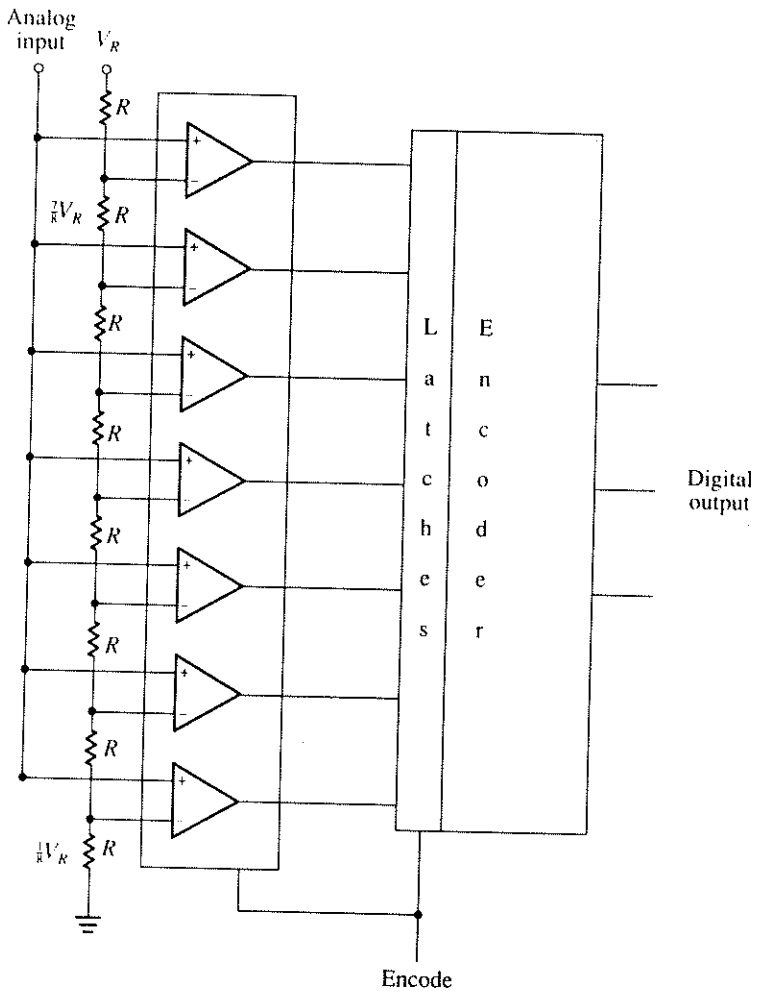
(a)



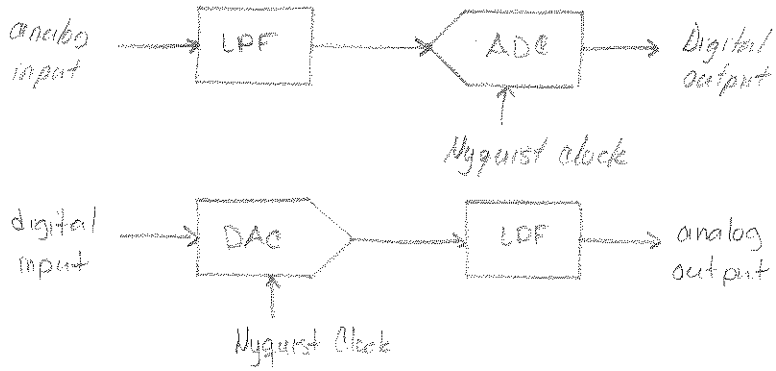
(b)

Flash ADC: Simplest and fastest. Also the largest in terms of hardware. Requires 2^n comparators for an n-bit conversion

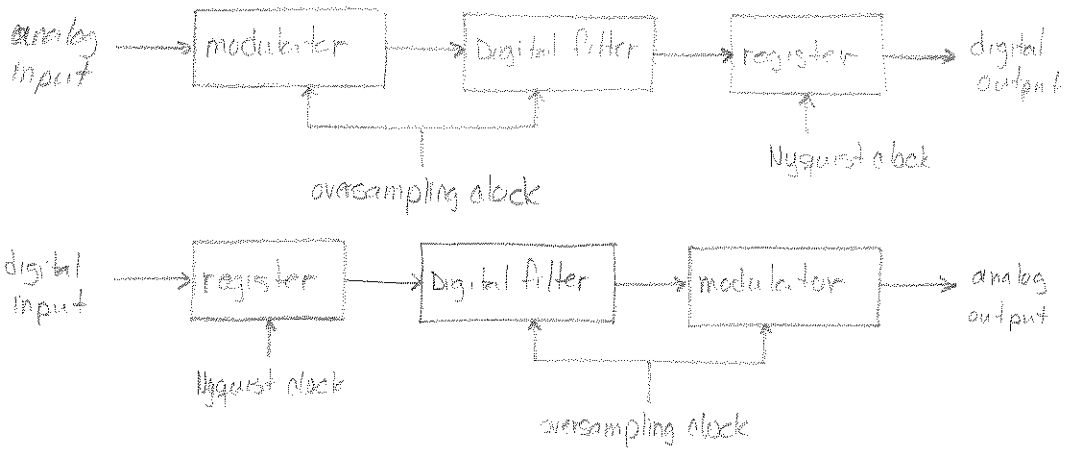
Encode = 0 ⇒ Sample mode
Encode = 1 ⇒ Freeze mode and output encoded into binary



Conventional Data Conversion



Oversampling Data Conversion



Virtues of oversampling converters:

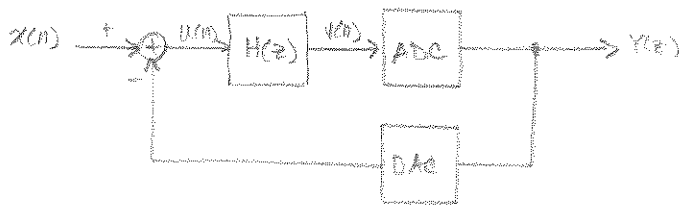
- High tolerance analog components
- Trade resolution in time for resolution in amplitude
- Eliminates the need for abrupt cut off in the analog filters.
- Extensive use of DSP

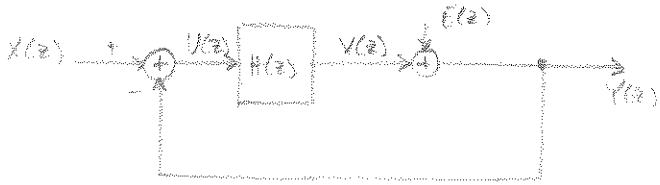
An important remark is that there is NO one-to-one correspondence between the input and output signal, and hence no classical methods of characterization can be used. Instead techniques of communications are used to describe the performance of oversampled data converters.

Sigma - Delta Modulator Structure

ΣΔM: Sigma - Delta Modulator

I. Basic Principles:



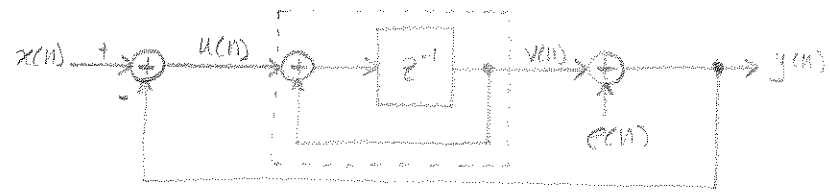


E(z): quantization noise

STF: $H_S(z) = \frac{H(z)}{1+H(z)}$ (LPF)

NTF: $H_N(z) = \frac{1}{1+H(z)}$ (HPF)

II. 1st Order ΣΔM



STF: $H_S(z) = z^{-1}$

NTF: $H_N(z) = 1 - z^{-1}$

$H(z) = \frac{z^{-1}}{1-z^{-1}}$ (integrator)

Time domain:

$$y(n) = x(n-1) + e(n) - e(n-1)$$

x(n)	U(n)	V(n)	Y(n)	
		0	0	
2/8	2/8	2/8	+1	} average 2/8
2/8	-6/8	-4/8	-1	
2/8	10/8	6/8	+1	
2/8	-6/8	0	-1	
2/8	10/8	10/8	+1	
2/8	-6/8	4/8	+1	
2/8	-6/8	-2/8	-1	
2/8	10/8	8/8	+1	

III. 1st Order ΣΔM Implementation