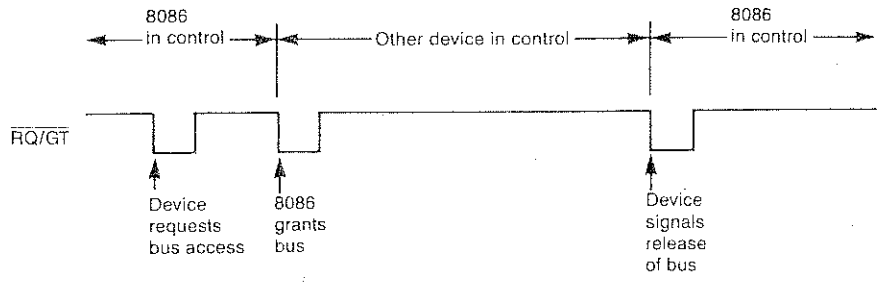
Figure 3.28. The 8086 bus request/bus grant operation.



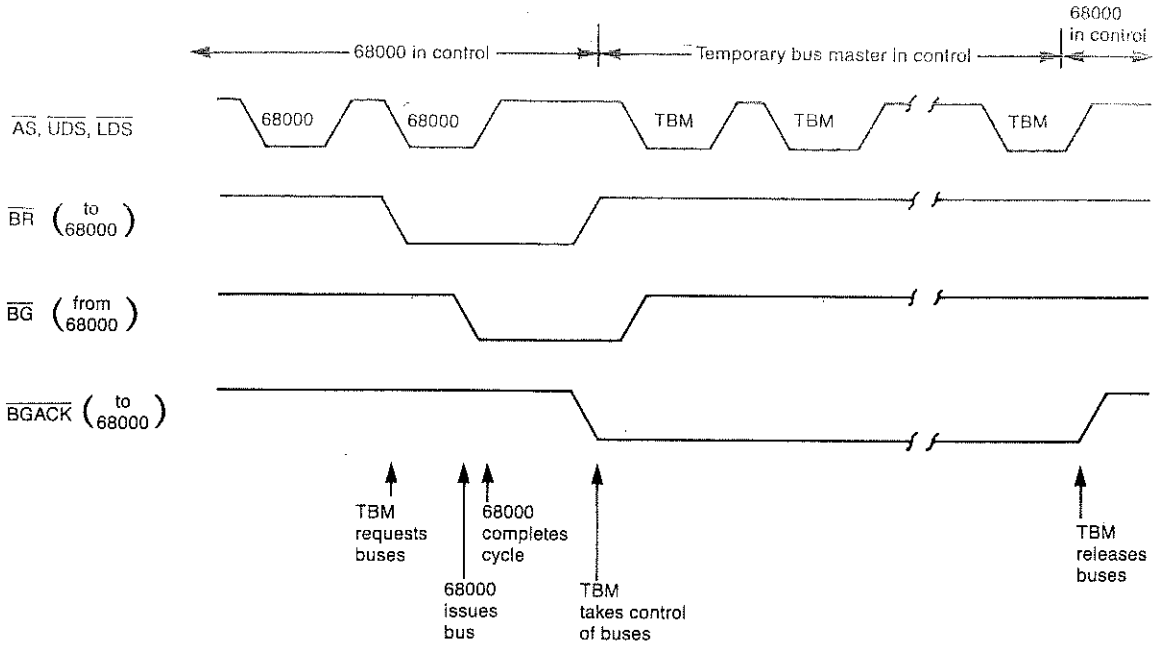
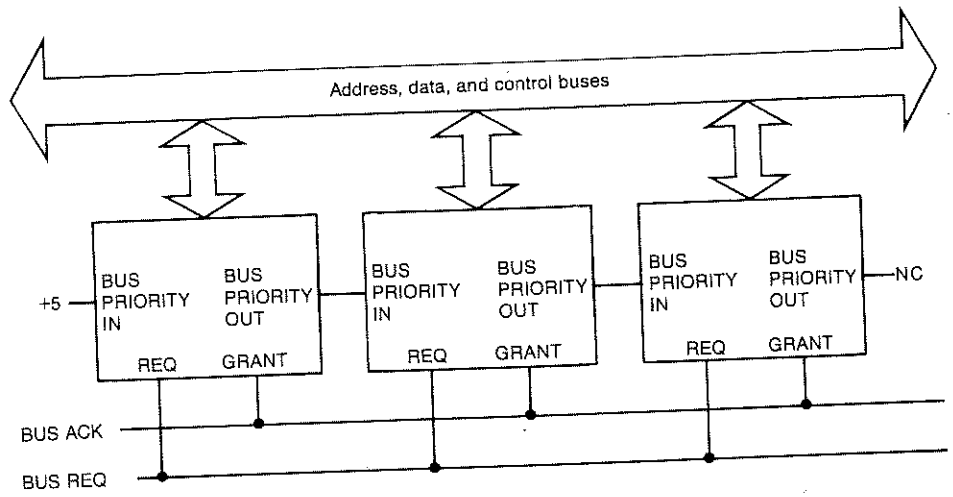


Figure 3.29. The 68000 bus request/bus grant operation.

Figure 3.30. Serial bus arbitration using priority daisy chain.



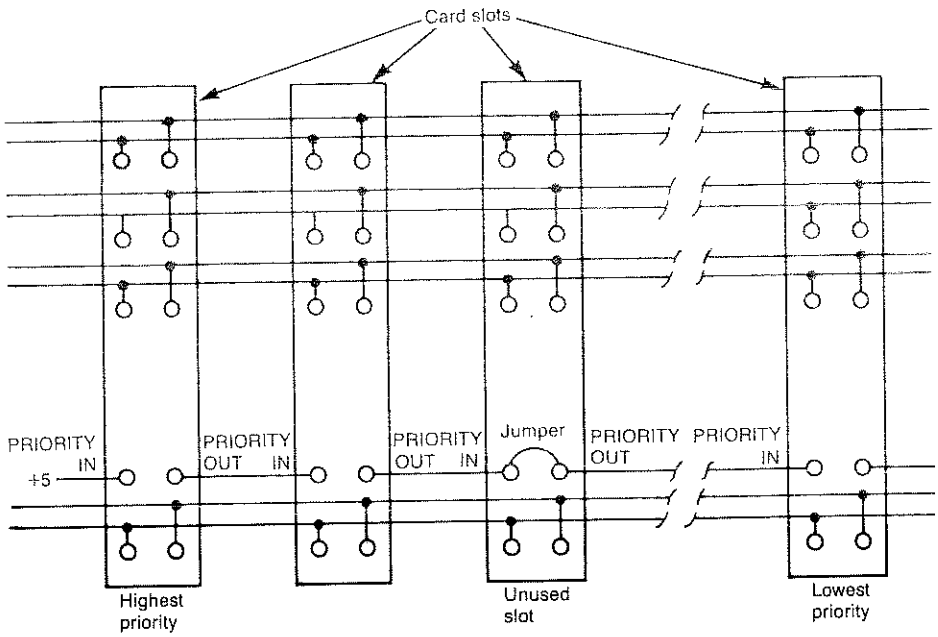


Figure 3.31. Daisy-chained priority signals on backplane.

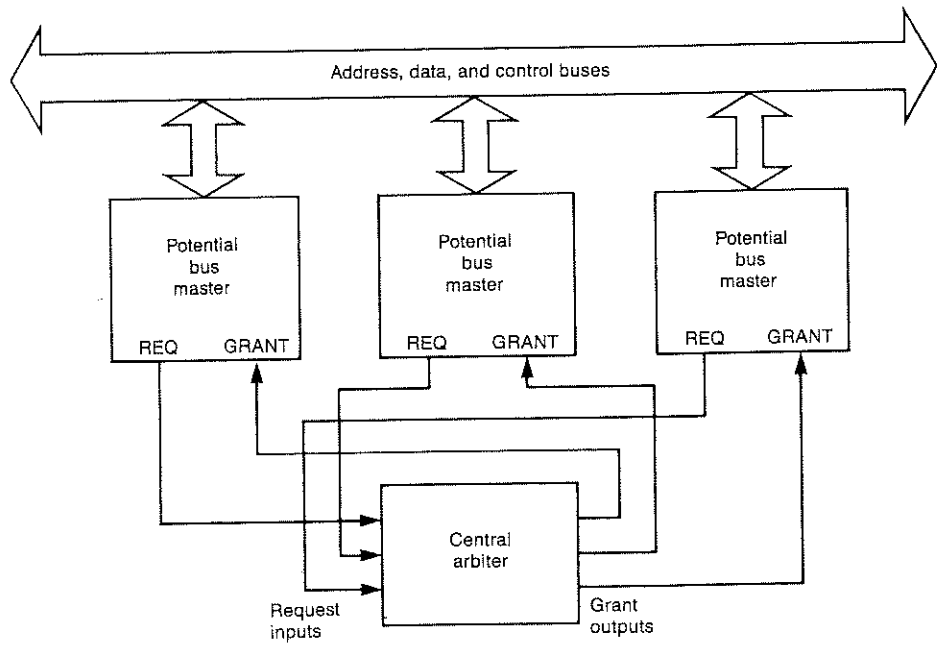


Figure 3.32. Parallel bus arbitration using central arbiter.

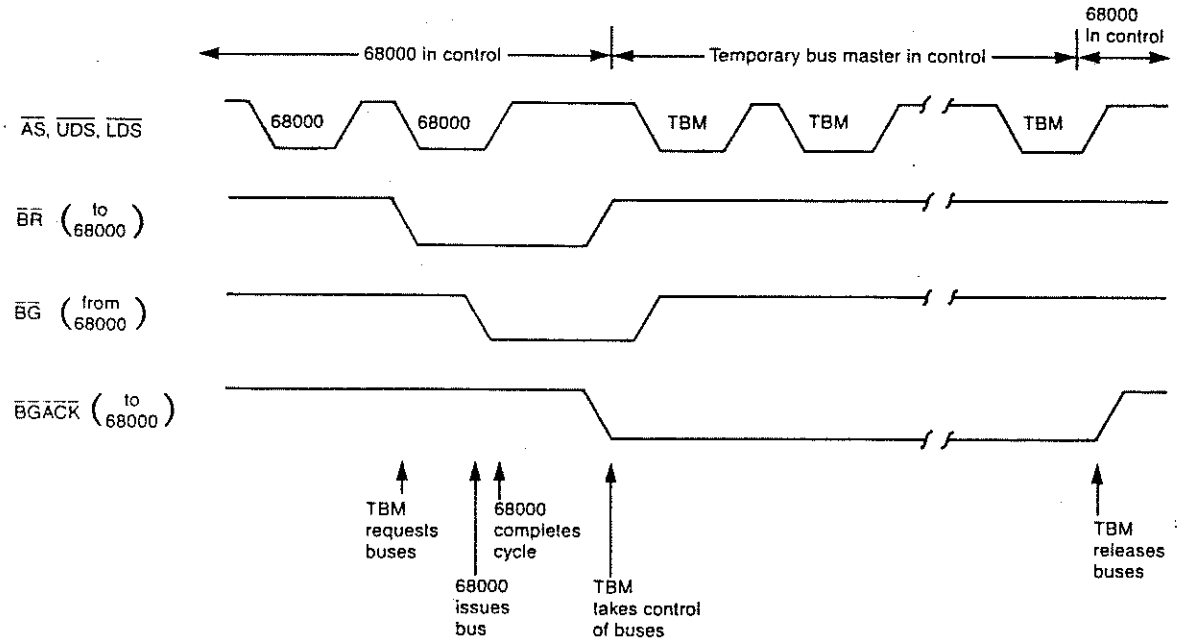


Figure 3.29. The 68000 bus request/bus grant operation.

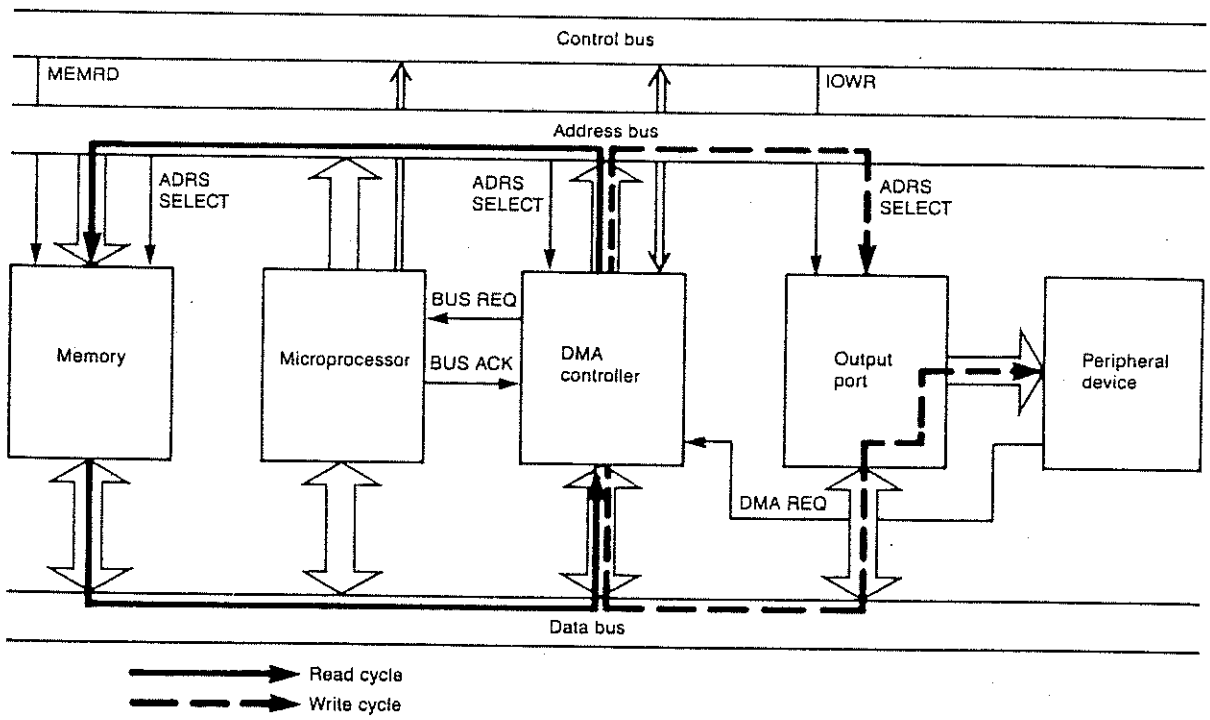


Figure 5.17. Two-cycle DMA transfer from memory to output port. The solid paths indicate the read cycle; the dashed paths indicate the write cycle.

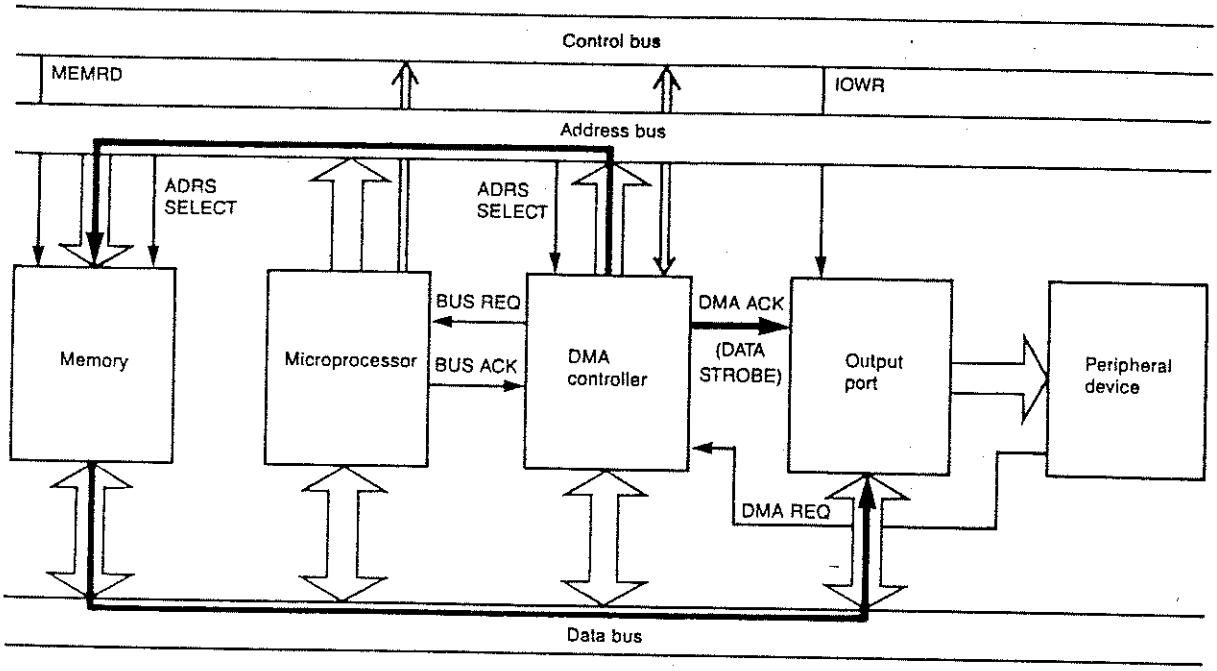


Figure 5.18. One-cycle DMA transfer from memory to output port.

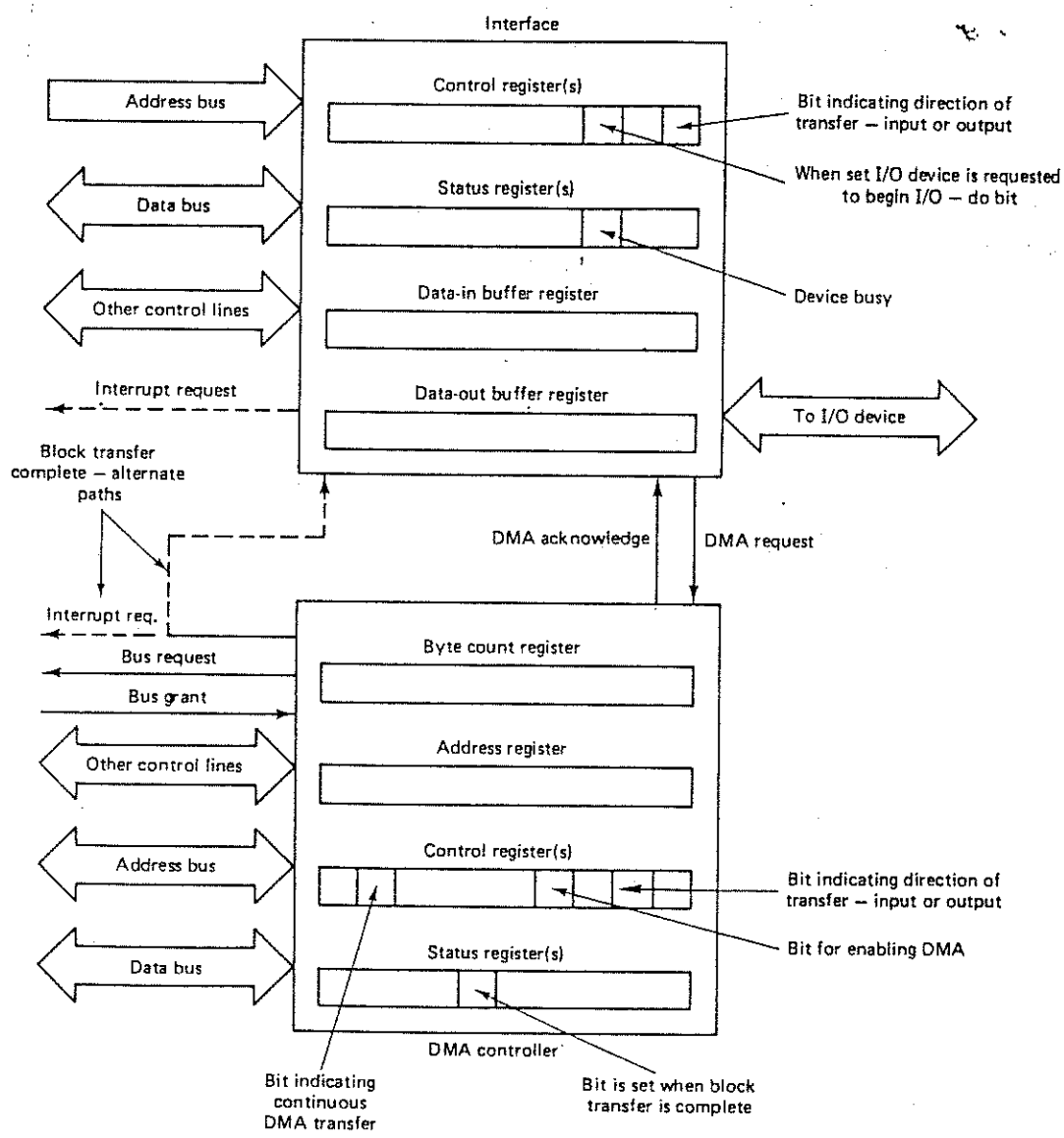


Figure 6-17 Minimal DMA controller/interface configuration.

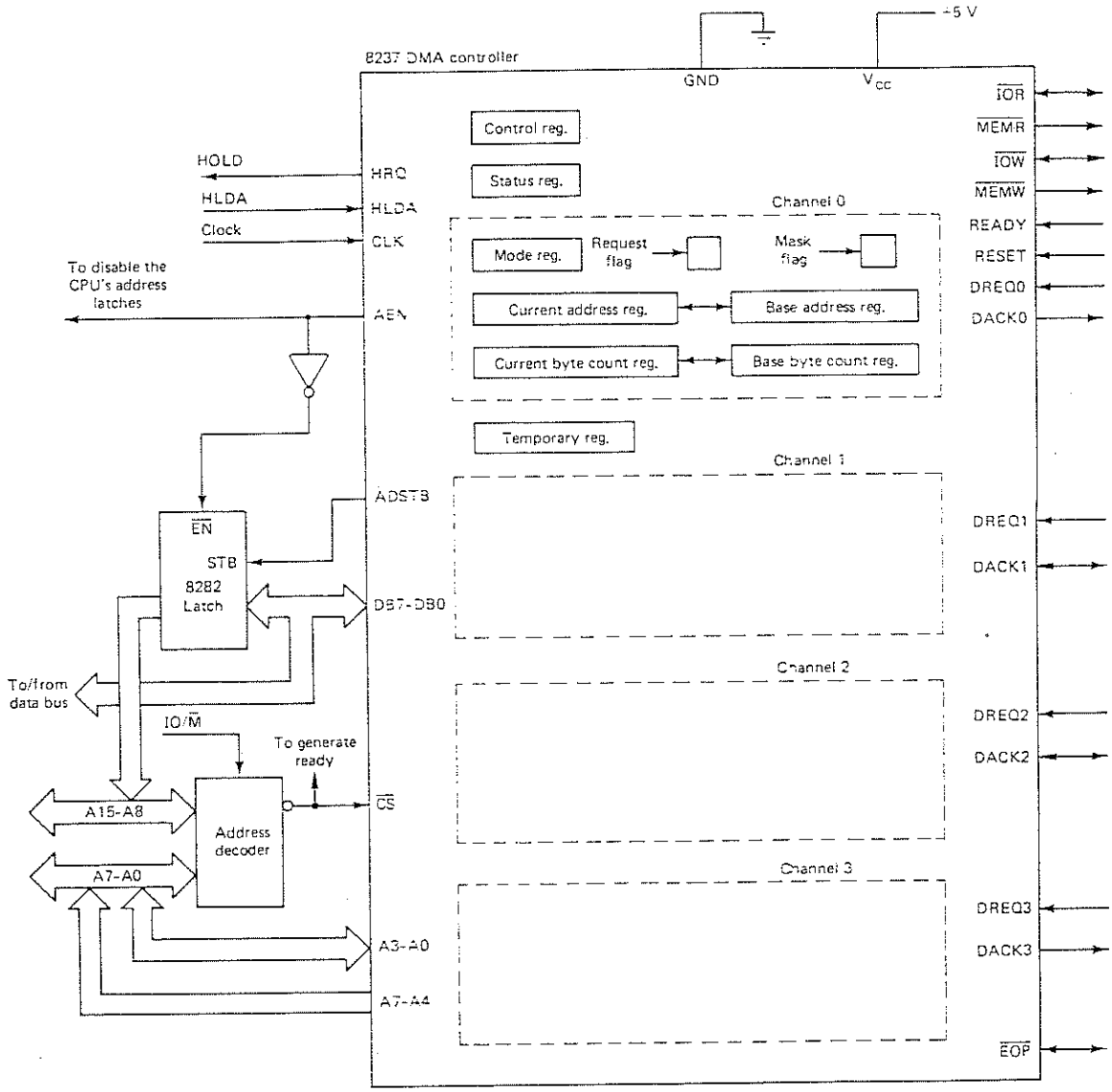


Figure 9-37 Organization of an 8237 and its associated logic.

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Register	4 bits	1
Request Register	4 bits	1

Figure 3. 8237A Internal Registers

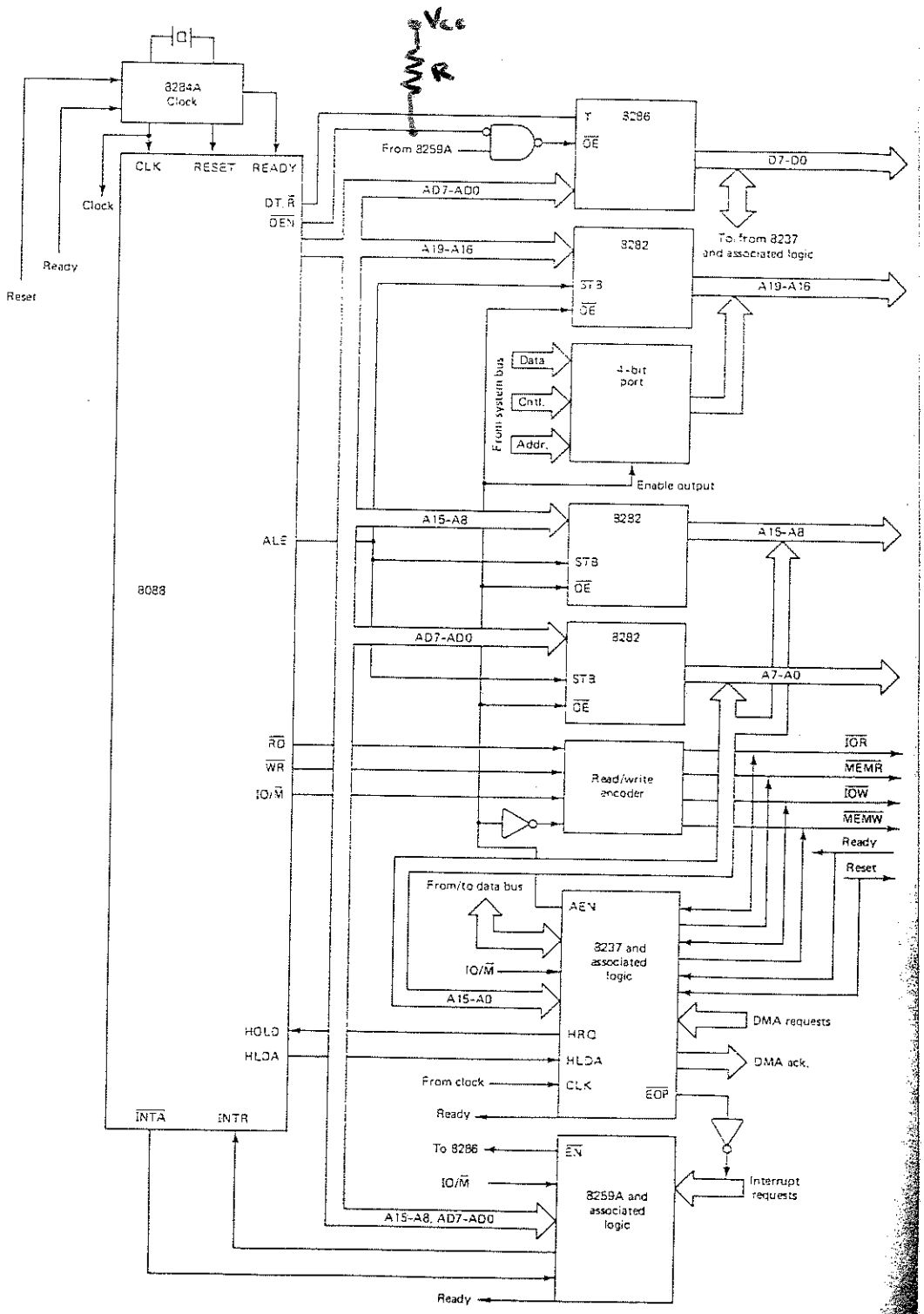


Figure 9-38 Minimum mode 8088 configuration that includes an 8237.

WAVEFORMS

SLAVE MODE WRITE TIMING

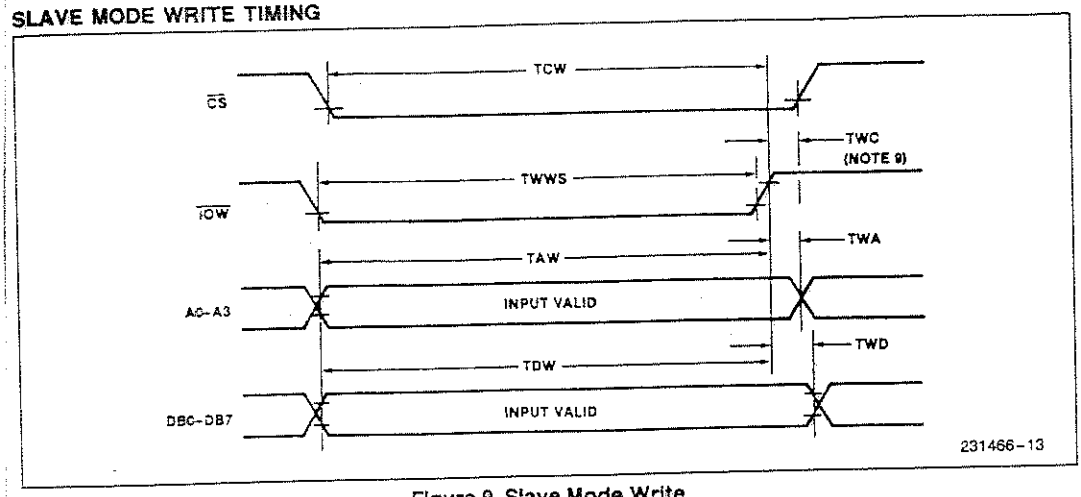


Figure 9. Slave Mode Write

SLAVE MODE READ TIMING

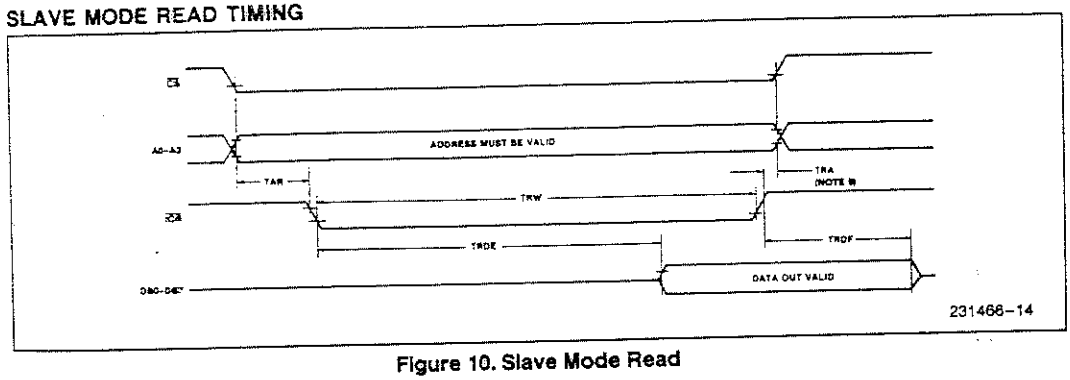


Figure 10. Slave Mode Read

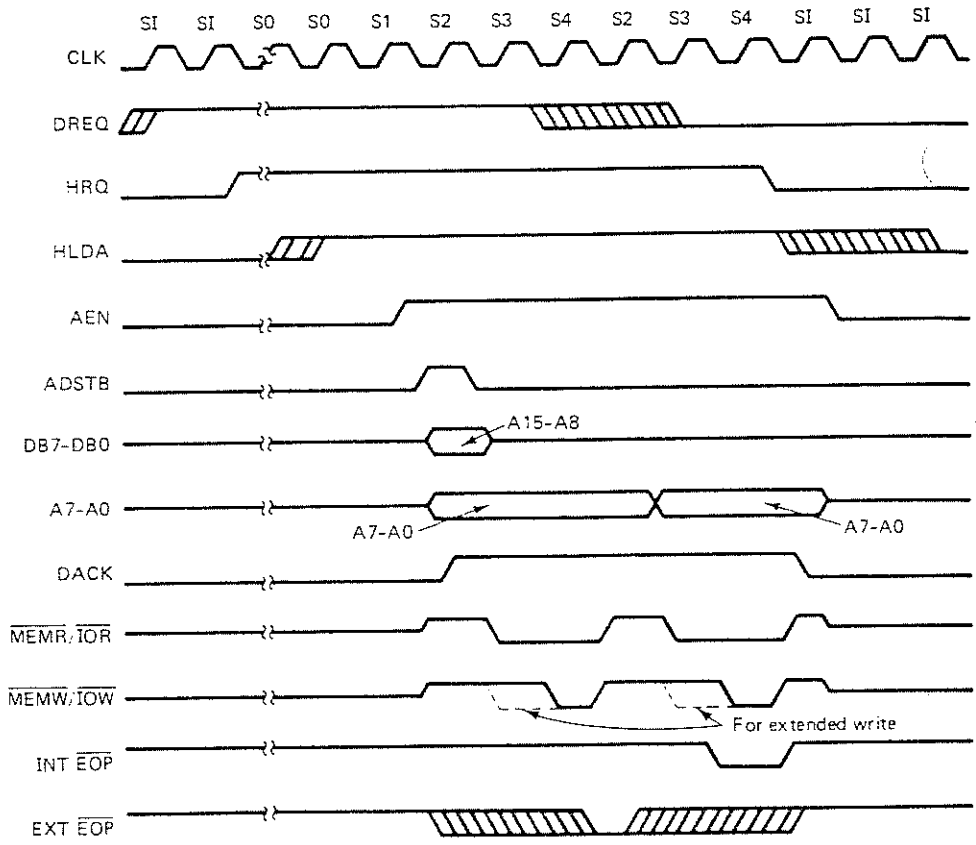
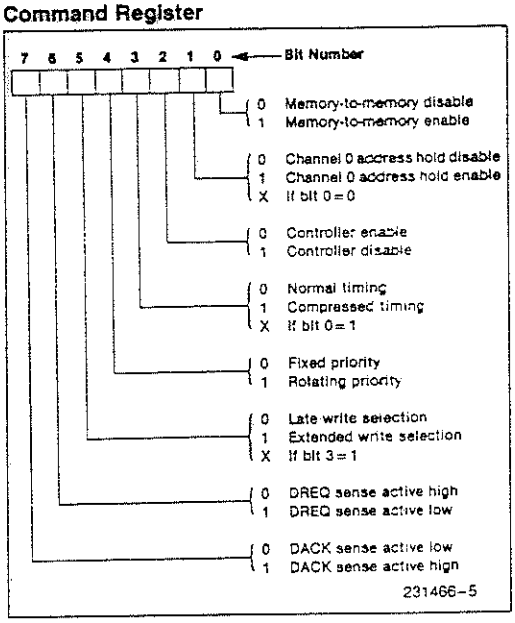
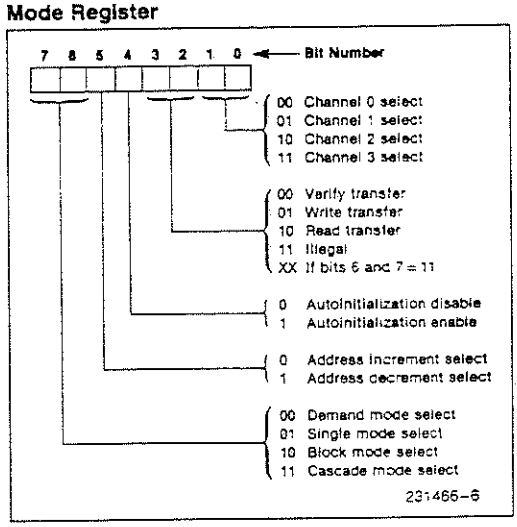


Figure 9-41 Typical timing diagram for an 8237.

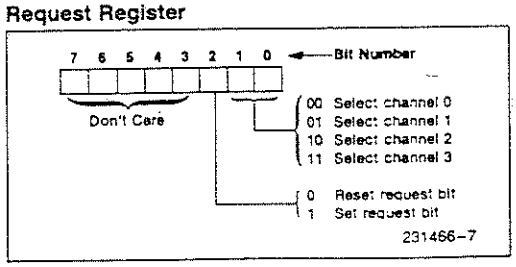
Command Register

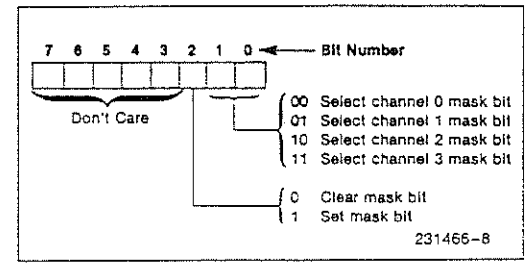


Mode Register

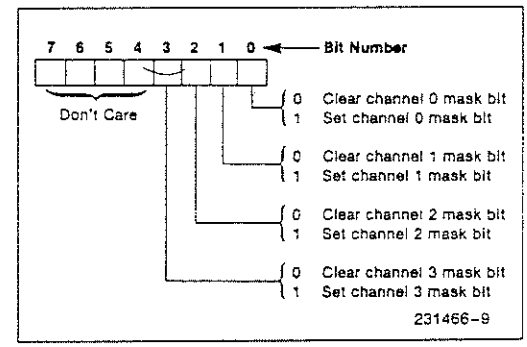


Request Register



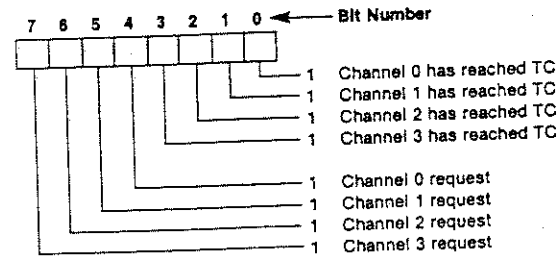


All four bits of the Mask register may also be written with a single command.



Register	Operation	Signals						
		$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0
Command	Write	0	1	0	1	0	0	0
Mode	Write	0	1	0	1	0	1	1
Request	Write	0	1	0	1	0	0	1
Mask	Set/Reset	0	1	0	1	0	1	0
Mask	Write	0	1	0	1	1	1	1
Temporary	Read	0	0	1	1	1	0	1
Status	Read	0	0	1	1	0	0	0

Figure 5. Definition of Register Codes

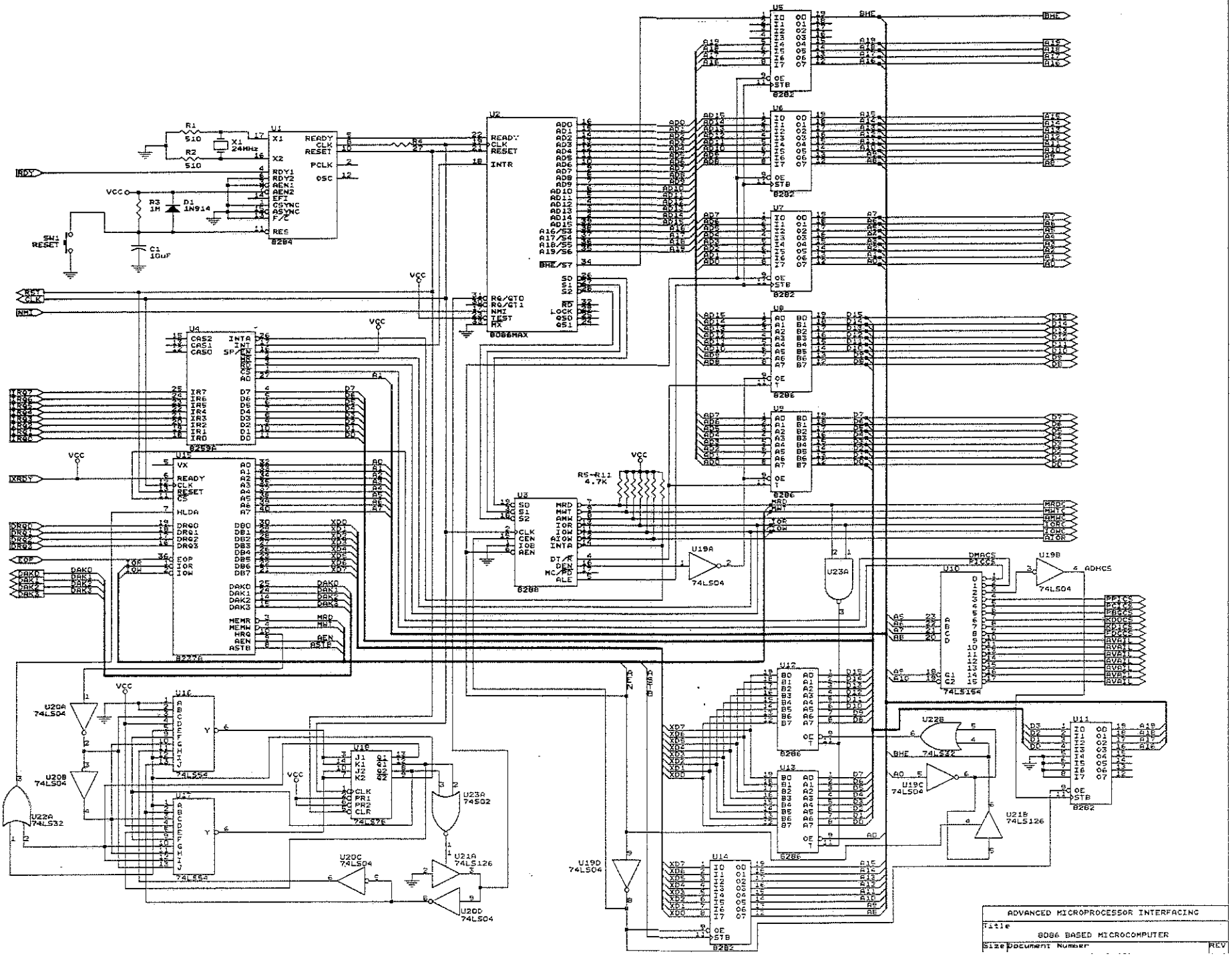


Signals						Operation
A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$	
1	0	0	0	0	1	Read Status Register
1	0	0	0	1	0	Write Command Register
1	0	0	1	0	1	Illegal
1	0	0	1	1	0	Write Request Register
1	0	1	0	0	1	Illegal
1	0	1	0	1	0	Write Single Mask Register Bit
1	0	1	1	0	1	Illegal
1	0	1	1	1	0	Write Mode Register
1	1	0	0	0	1	Illegal
1	1	0	0	1	0	Clear Byte Pointer Flip/Flop
1	1	0	1	0	1	Read Temporary Register
1	1	0	1	1	0	Master Clear
1	1	1	0	0	1	Illegal
1	1	1	0	1	0	Clear Mask Register
1	1	1	1	0	1	Illegal
1	1	1	1	1	0	Write All Mask Register Bits

Figure 6. Software Command Codes

Channel	Register	Operation	Signals							Internal Flip-Flop	Data Bus DB0–DB7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0		
0	Base and Current Address	Write	0	1	0	0	0	0	0	0	A0–A7
			0	1	0	0	0	0	0	1	A8–A15
	Current Address	Read	0	0	1	0	0	0	0	0	A0–A7
			0	0	1	0	0	0	0	1	A8–A15
	Base and Current Word Count	Write	0	1	0	0	0	0	1	0	W0–W7
			0	1	0	0	0	0	1	1	W8–W15
	Current Word Count	Read	0	0	1	0	0	0	1	0	W0–W7
			0	0	1	0	0	0	1	1	W8–W15
1	Base and Current Address	Write	0	1	0	0	0	1	0	0	A0–A7
			0	1	0	0	0	1	0	1	A8–A15
	Current Address	Read	0	0	1	0	0	1	0	0	A0–A7
			0	0	1	0	0	1	0	1	A8–A15
	Base and Current Word Count	Write	0	1	0	0	0	1	1	0	W0–W7
			0	1	0	0	0	1	1	1	W8–W15
	Current Word Count	Read	0	0	1	0	0	1	1	0	W0–W7
			0	0	1	0	0	1	1	1	W8–W15
2	Base and Current Address	Write	0	1	0	0	1	0	0	0	A0–A7
			0	1	0	0	1	0	0	1	A8–A15
	Current Address	Read	0	0	1	0	1	0	0	0	A0–A7
			0	0	1	0	1	0	0	1	A8–A15
	Base and Current Word Count	Write	0	1	0	0	1	0	1	0	W0–W7
			0	1	0	0	1	0	1	1	W8–W15
	Current Word Count	Read	0	0	1	0	1	0	1	0	W0–W7
			0	0	1	0	1	0	1	1	W8–W15
3	Base and Current Address	Write	0	1	0	0	1	1	0	0	A0–A7
			0	1	0	0	1	1	0	1	A8–A15
	Current Address	Read	0	0	1	0	1	1	0	0	A0–A7
			0	0	1	0	1	1	0	1	A8–A15
	Base and Current Word Count	Write	0	1	0	0	1	1	1	0	W0–W7
			0	1	0	0	1	1	1	1	W8–W15
	Current Word Count	Read	0	0	1	0	1	1	1	0	W0–W7
			0	0	1	0	1	1	1	1	W8–W15

Figure 7. Word Count and Address Register Command Codes


ADVANCED MICROPROCESSOR INTERFACING
Title
8086 BASED MICROCOMPUTER
Size
Document Number
REV

```
;*************************************************************
; Programs 8237A (address 020H) for:
;*************************************************************
;                - DMA channel 0 assigned to read FDC-write memory
;                - Block mode without autoinitialization
;                - Normal timing
;                - Fixed priority
;                - DREQ sense active high, DACK active low
;                - Location to place data given by DS:BX
;                - Block size given by CX

ReadFDC proc far

        push ax          ; Save registers
        push bx
        push cx

        mov ax,ds                ; Bits to program A16-A19 latch
        mov cl,0ch
        shr ax,cl
        out 040h,al      ; 4 bits to latch ADHCS

        out 02Ch,al      ; Reset first/last F/F

        mov ax,bx                ; Destination address in memory
        out 020h,al
        mov al,ah
        out 020h,al

        pop cx           ; count value
        mov ax,cx
        dec ax           ; adjust count
        out 021h,al
        mov al,ah
        out 021h,al

        mov al,10000100b ; Program mode for CH 00
        out 02bh,al

; To write to floppy change mode for channel 0
; to 10001000b and iclude the following two instruction
; to begin transfer
;       mov al,00000100  ; Program request register
;    out 029h,al

        mov al,00000000b ; Program control (enable DMA)
        out 028h,al

        mov al,00000001b ; Program mask register
        out 02fh,al

Chk:    in al,020h       ; Read status register
        test al,00000001b ; Checks CH 0 tc
        jz chk
        ret

eadFDC endp
```