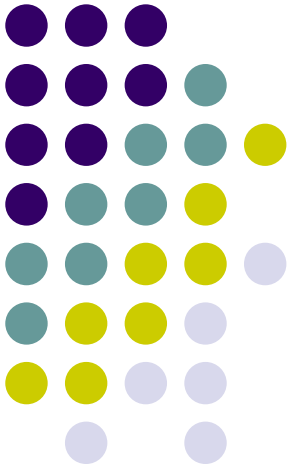
Chapter 6: EMBEDDED HARDWARE FUNDAMENTALS (2/3)



Manuel Jiménez

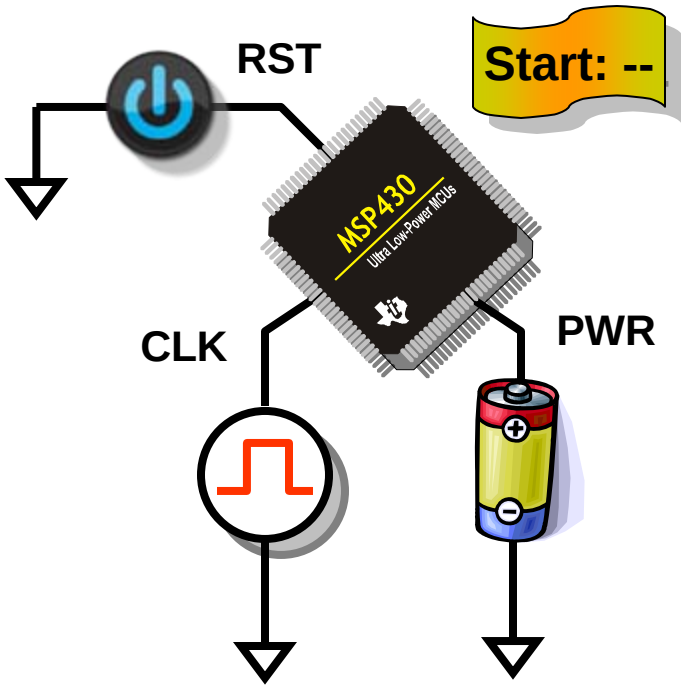
EMBEDDED SYSTEMS:

Theory and Applications Using the MSP430

UPRM - Spring 2010

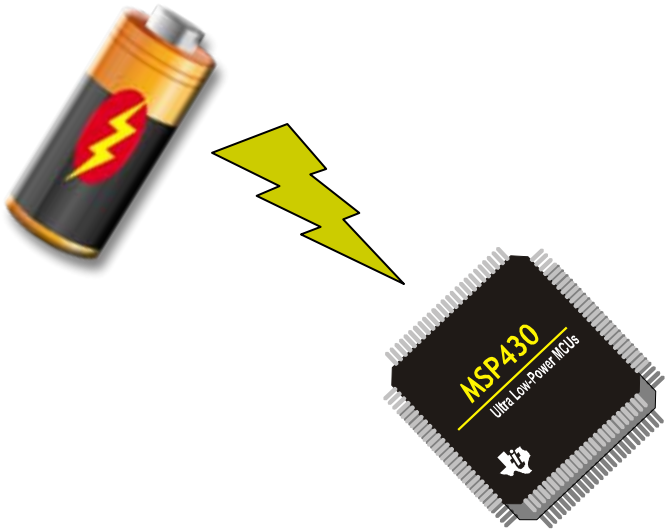
Part 2: The Basic Interface

- MCU and System Power Sources
  - Selecting a Power source
- Clock Oscillators
  - Choosing a Clock Source
- Power-on Reset
  - Reset Hardware
  - Initialization Software
- Memory Map: Programs & Data
  - Partitioning Programs and Data
  - Reserved Locations
- Interfacing Considerations
  - Bus Loading Considerations
  - Electrical Compatibility Issues
  - Noise and Signal Integrity Issues



Supplying Power to MCUs

- Provides Power to CPU and on-chip electronics
- Basic Criteria
  - Voltage Level
  - Supply Current
  - Regulation
  - Signal Compatibility
  - Power Ports:
    - Analog Vs. Digital Power



Where and How Much?

- Identify Voltage Level & Supply Ports
  - Most modern micros require a single supply voltage
  - Identify ports, polarity, and levels
  - Estimate supply current (CPU + Peripherals) to assign power supply

MSP430x13x, MSP430x14x

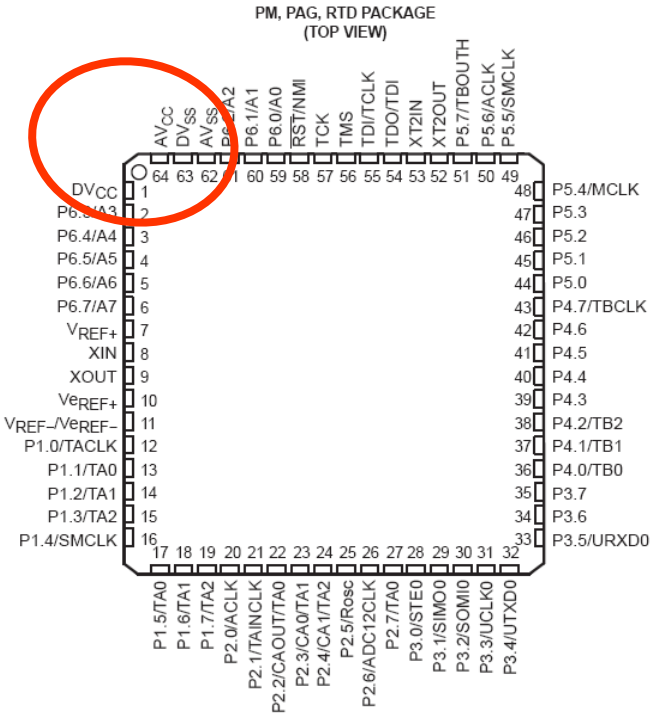
TERMINAL NAME	NO.	I/O	DESCRIPTION
AV_{CC}	64		Analog supply voltage, positive terminal. Supplies the analog portion of the analog-to-digital converter.
AV_{SS}	62		Analog supply voltage, negative terminal. Supplies the analog portion of the analog-to-digital converter.
DV_{CC}	1		Digital supply voltage, positive terminal. Supplies all digital parts.
DV_{SS}	63		Digital supply voltage, negative terminal. Supplies all digital parts.

recommended operating conditions

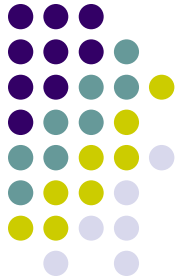
PARAMETER		MIN	NOM	MAX	UNITS
Supply voltage during program execution, V_{CC} (AV_{CC} = DV_{CC} = V_{CC})	MSP430F13x, MSP430F14x(1)	1.8		3.6	V
Supply voltage during flash memory programming, V_{CC} (AV_{CC} = DV_{CC} = V_{CC})	MSP430F13x, MSP430F14x(1)	2.7		3.6	V
Supply voltage, V_{SS} (AV_{SS} = DV_{SS} = V_{SS})		0.0		0.0	V

supply current into AV_{CC} + DV_{CC} excluding external current

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{(AM)}$	Active mode, (see Note 1) $f_{(MCLK)}$ = $f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz XTS=0, SELM=(0,1)	T_A = −40°C to 85°C	V_{CC} = 2.2 V		280	350	µA
			V_{CC} = 3 V		420	560	
$I_{(AM)}$	Active mode, (see Note 1) $f_{(MCLK)}$ = $f_{(SMCLK)}$ = 4 096 Hz, $f_{(ACLK)}$ = 4,096 Hz XTS=0, SELM=(0,1) XTS=0, SELM=3	T_A = −40°C to 85°C	V_{CC} = 2.2 V		2.5	7	µA
			V_{CC} = 3 V		9	20	



A Word About Regulation



- Most MCUs feature internal regulators
  - Accept a range of values for Vdd
  - Flexible power supply options
  - Main concerns
    - Signal Compatibility: V_{OH} depends on V_{DD}
    - Maximum Speed: f_{CLKmax} depends on V_{DD}
- MPUs might include on-chip DC-to-DC converters
  - Typically, only one fixed input V_{DD} value
    - Though, some MCUs might need more than one V_{DD} level
  - Voltage source requires stable supply
    - Common requirement calls for 5% regulation
  - Ensure current headroom in I_{DD} supply (at least 15%)

Some Examples

Table 3.1. Global DC Electrical Characteristics

–40 to +85 °C, 25 MHz System Clock unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Digital Supply Voltage[1]		VRST	3.3	3.6	V

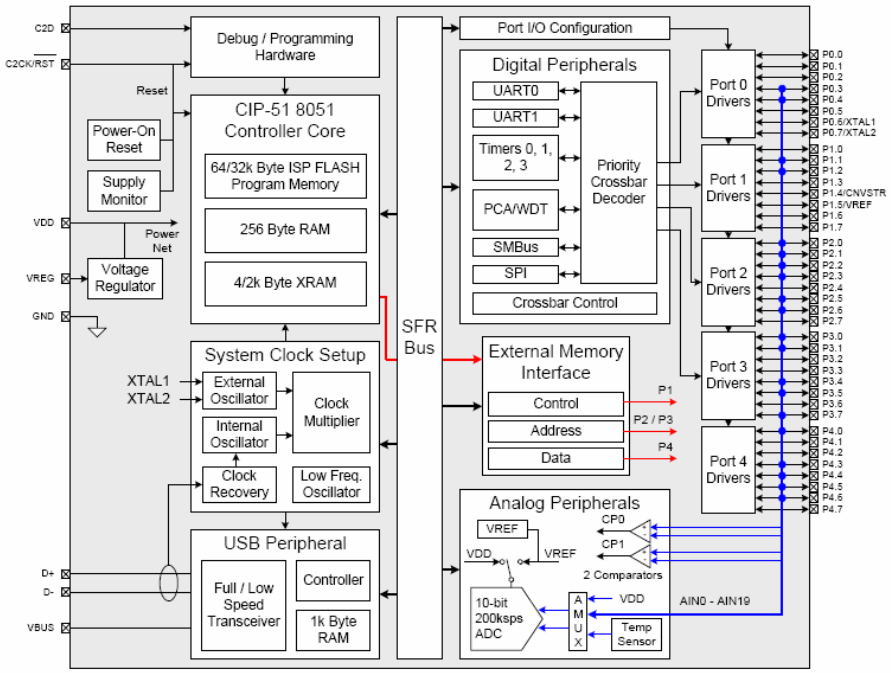


Figure 1.1. C8051F340/1/4/5 Block Diagram

PIC18LFXX2 (Industrial)

PIC18LFXX2 (Industrial)	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial
PIC18FXX2 (Industrial, Extended)	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
	VDD	**Supply Voltage**					
D001		PIC18LFXX2	2.0	—	5.5	V	HS, XT, RC and LP Osc mode
D001		PIC18FXX2	4.2	—	5.5	V	

Stellaris® LM3S1968 Microcontroller

Table 22-2. Recommended DC Operating Conditions

Parameter	Parameter Name	Min	Nom	Max	Unit
V_{DD}	I/O supply voltage	3.0	3.3	3.6	V
V_{DD25}	Core supply voltage	2.25	2.5	2.75	V
V_{DDA}	Analog supply voltage	3.0	3.3	3.6	V
V_{BAT}	Battery supply voltage	2.3	3.0	3.6	V

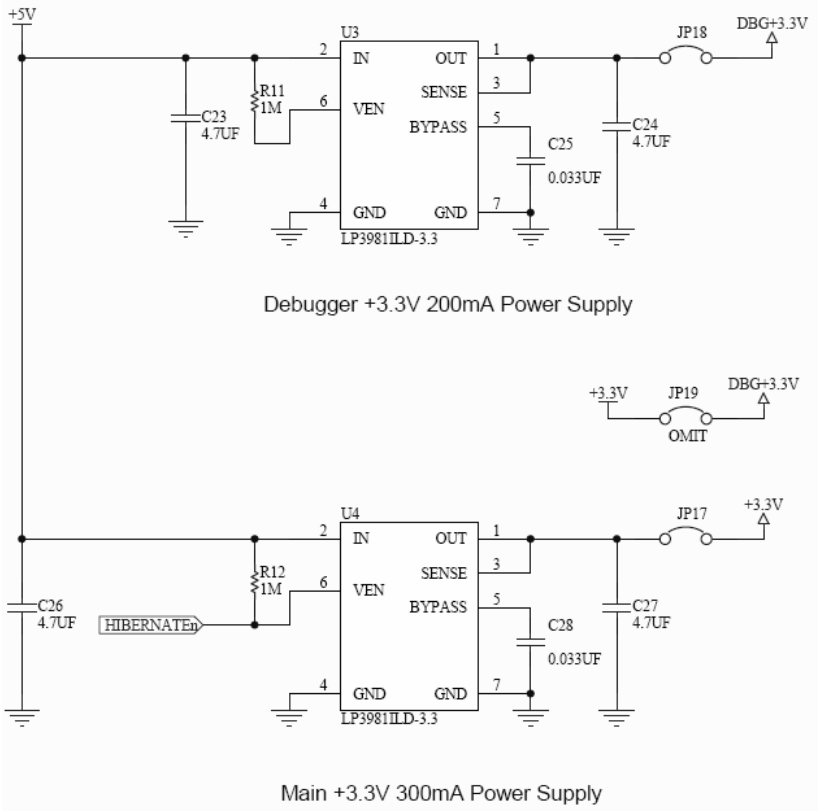
MOTOROLA **MCF5206e USER'S MANUAL**

Table 17-5. DC ELECTRICAL SPECIFICATIONS

CHARACTERISTIC	SYMBOL	MIN	MAX	UNIT
Operation voltage range	V_{DD}	3.0	3.6	V
Input high voltage	V_{IH}	2	55	V
Input low voltage	V_{IL}	GND	0.8	V

Providing Regulated Supply Voltages

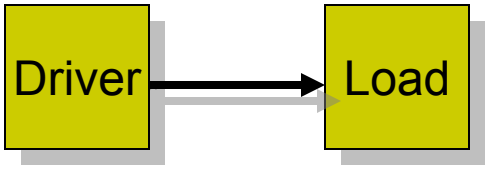
- Use separate voltage regulators for each supply level
- Use the main, unregulated input for each source
- Route separately the analog and digital supplies
  - Join them at a single point next to the power supply ground
- Provide bypassing caps at the power ports
- Include decoupling capacitors
  - One per digital IC
- Compute I_{DD} requirements for each regulator

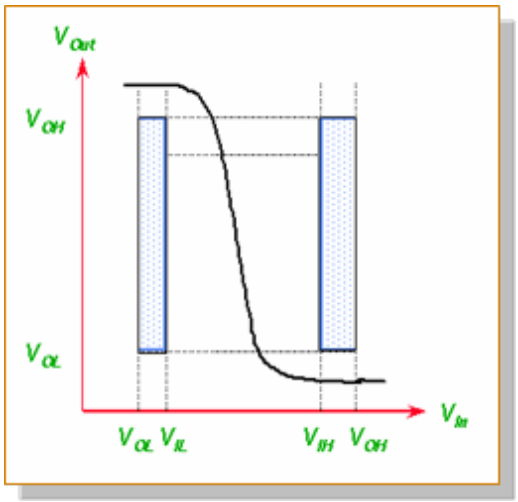


Signal Compatibility & V_{DD}

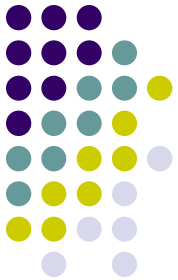
- Choose ICs that can operate at the same V_{DD} level
  - Maximizes the chances of good signal compatibility
- MCU and off-chip peripherals could operate at different voltage levels
  - Make sure logic levels are compatible
- Logic Interfacing Rule
  - $V_{OHdriver} > V_{IHload}$
  - $V_{OLdriver} < V_{ILload}$

  No Interface Needed
- Otherwise an interface needed!
  - Pull-up resistors increase V_{OH}
  - Pull down resistors reduce V_{OL}.
  - Some cases might need logic translation



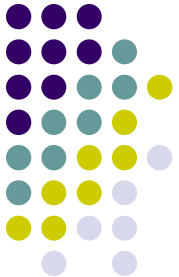


Clock Sources



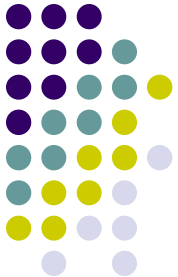
- Provide synchronization to CPU operation
- Define the system clock base
  - Time base for bus cycles, timers, baud rates
- Requirements
  - Source Type
    - Internal Vs. External
  - Minimum and maximum frequency values
    - Function of supply voltage V_{DD}
  - Clock stability
    - Maximum drift & jitter

Internal Sources



- Typically based on RC oscillators
  - Preferred in MCUs
- Pros:
  - Reduce external component count
  - Less expensive
  - Induce lower power consumption
- Cons:
  - Least stability
  - Least flexibility
  - Slowest frequency values

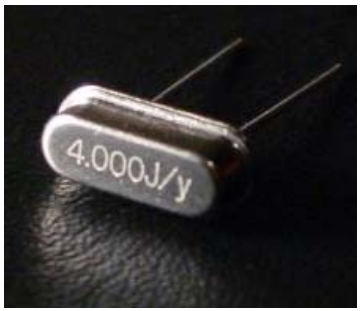
External Sources



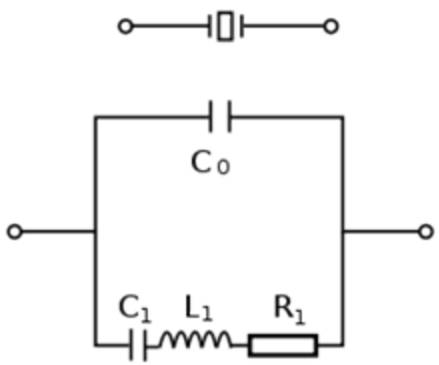
- Allow using diverse oscillator types
  - Crystal type
  - RC-based
  - External digital clocks
- Pros
  - Wider choice of frequency values
  - More design flexibility
- Cons
  - Increment the external component count
  - Higher clock speeds induce higher power consumption

Crystal Oscillators

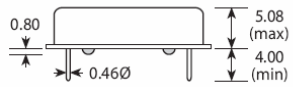
- Based on mechanical resonance of a vibrating piezoelectric crystal
  - Shape and size determine frequency
- Create an electrical signal with a very precise frequency
  - Require squaring circuit to get f_{CLK}
- Commercial crystal oscillator ICs provide squared signal output

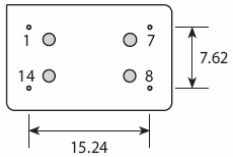


Symbol



Equivalent Circuit

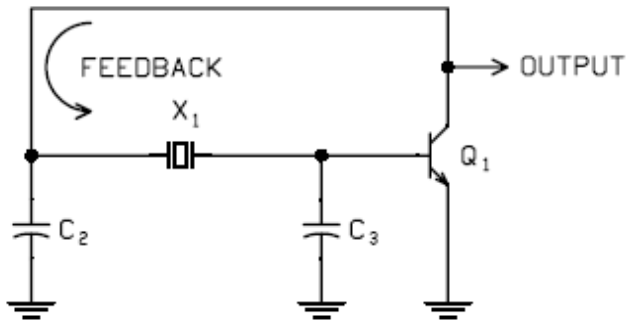


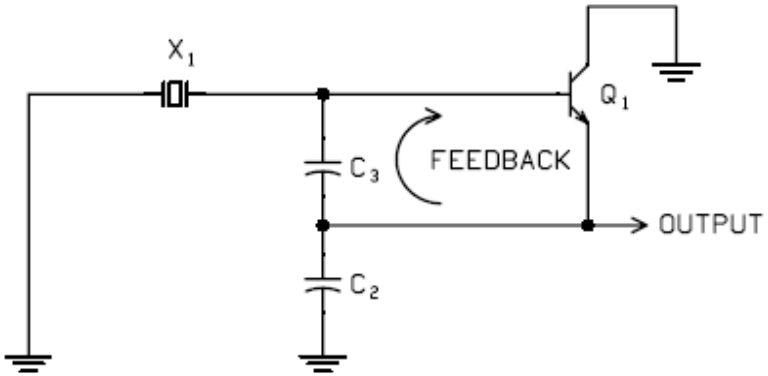


PIN	CONNECTION
1	Not connected
7	Ground
8	Output
14	Supply

Common Crystal Oscillators

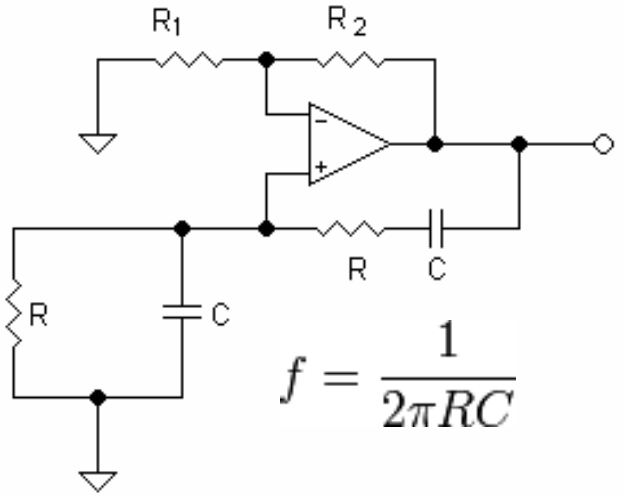
- Pierce Crystal Osc.
  - Series resonant
  - Insensitive to discrete component variations
- Colpittz Crystal Osc.
  - Parallel resonant





RC Oscillators

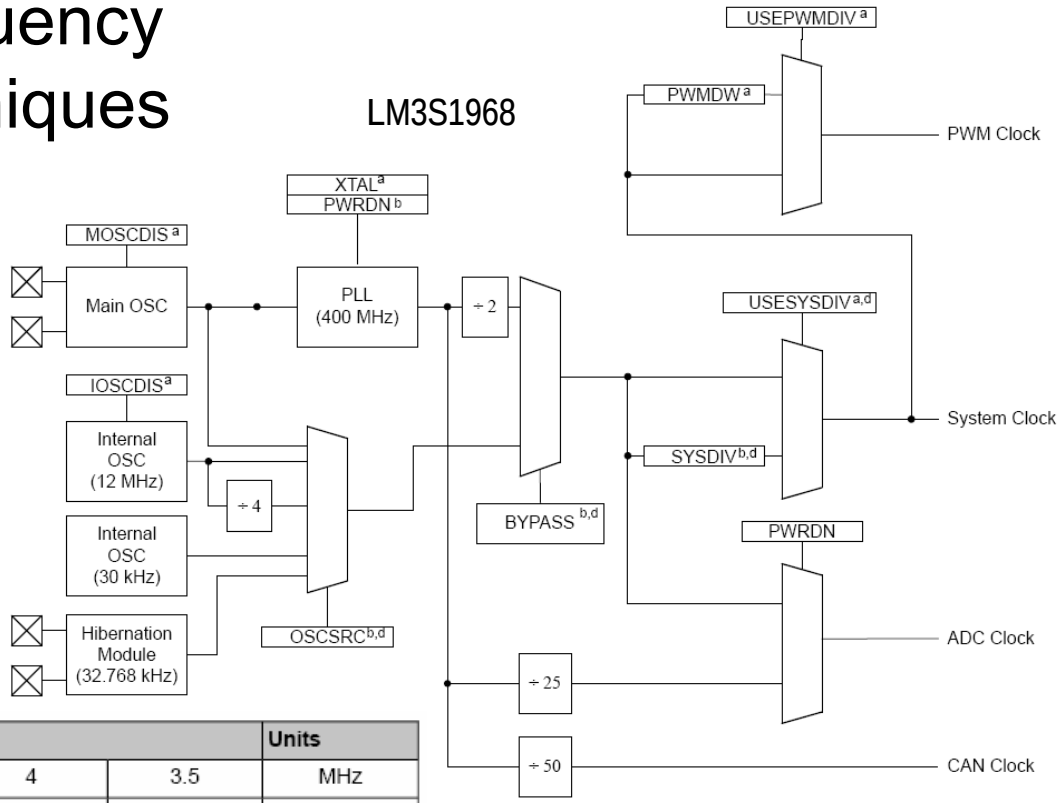
- Based on RC phase shift circuit
  - Commonly a Wien Bridge
  - Frequency determined by τ=RC
- Frequency stability affected by tolerance of R & C components
  - R values affected by temperature
  - C values can vary with V_{DD}
- Limited to low frequency values
- Preferred internal source for MCUs
  - Some allow external C to set f_{CLK}



Wien Bridge Oscillator

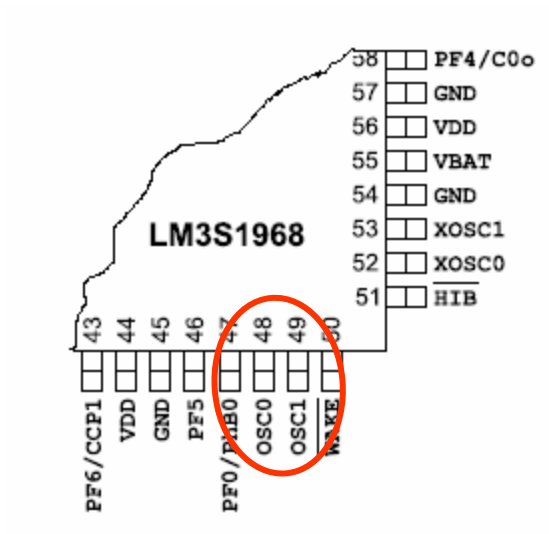
High Frequency Clock Sources

- Obtained with frequency multiplication techniques
  - Common in MPUs
  - Chipset-based or embedded



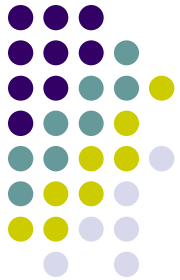
Parameter Name	Value				Units
Frequency	8	6	4	3.5	MHz
Frequency tolerance	±50	±50	±50	±50	ppm
Aging	±5	±5	±5	±5	ppm/yr
Oscillation mode	Parallel	Parallel	Parallel	Parallel	-
Temperature stability (-40°C to 85°C)	±25	±25	±25	±25	ppm

LM3S1968



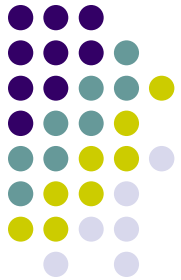
Function	Pin Name	Pin Number	Pin Type	Buffer Type[a]	Description
System Control & Clocks	CMOD0	65	I/O	TTL	CPU Mode bit 0. Input must be set to logic 0 (grounded); other encodings reserved.
	CMOD1	76	I/O	TTL	CPU Mode bit 1. Input must be set to logic 0 (grounded); other encodings reserved.
	OSC0	48	I	Analog	Main oscillator crystal input or an external clock reference input.
	OSC1	49	O	Analog	Main oscillator crystal output.
	$\overline{RST}$	64	I	TTL	System reset input.

Quartz Crystal Aging



- A systematic change in frequency over time caused by internal changes in the oscillator
  - Internal contamination, excessive drive level, crystal surface change, thermal effects, wire fatigue, and frictional wear
- Aging deviation measured in parts-per-million (ppm)
  - 1ppm in a 12MHz crystal = 12Hz

Drift and Jitter

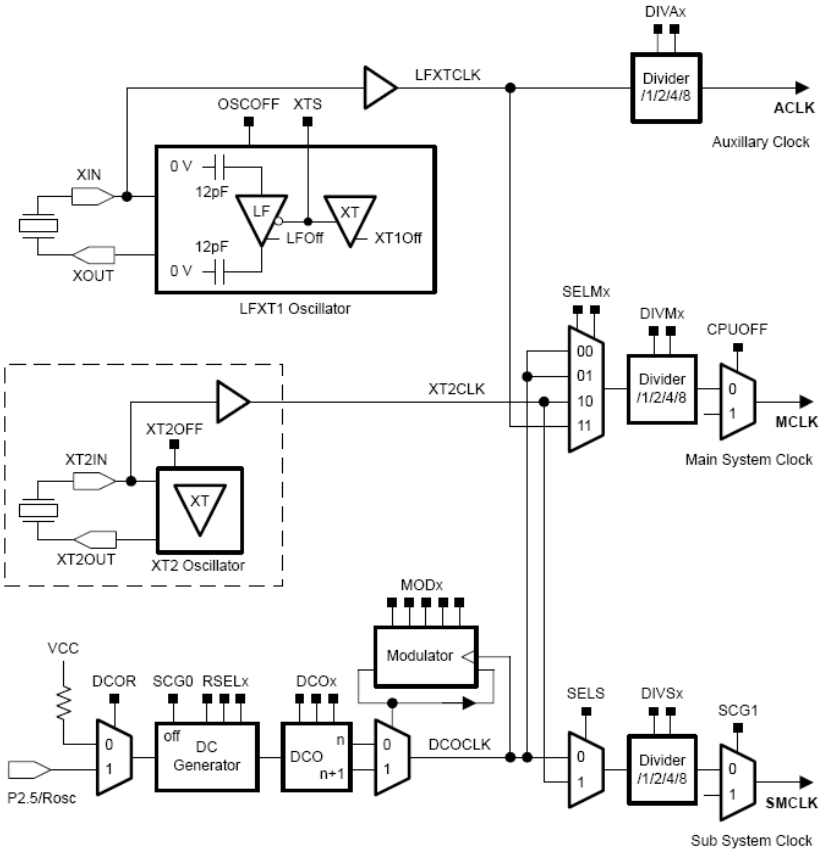


- **Drift**: The linear (first-order) component of a systematic change in frequency of an oscillator over time
  - Caused by aging, environment changes, and other factors external to the oscillator
- **Jitter**: The time variation of a periodic signal in relation to a reference clock source
  - A deviation from the ideal timing of an event

Some Typical f_{CLK} Values

Freq. (MHz)	Typical Applications
0.032768	Real-time clocks, quartz watches and clocks; allows binary division to 1 Hz signal (215×1 Hz)
1.843200	UART clock; allows integer division to baud rates. (213×32×52; 16×115,200 baud or 96×16×1,200 baud)
2.457600	UART clock; allows integer division to baud rates up to 38,400. (215×31×52; 64×38,400 baud or 2048×1,200 baud)
3.276800	Allows binary division to 100 Hz (32,768×100 Hz, or 215×100 Hz)
3.575611	PAL M color subcarrier
3.579545	NTSC M color subcarrier and DTMF generators
3.582056	PAL N color subcarrier
3.686400	UART clock (2×1.8432 MHz); allows integer division to common baud rates
4.096000	Allows binary division to 1 kHz (212×1 kHz)
4.194304	Real-time clocks, divides to 1 Hz signal (222×1 Hz)
4.433619	PAL B/D/G/H/I and NTSC M4.43 color subcarrier
6.144000	UART baud rates up to 38,400.
6.553600	Allows binary division to 100 Hz (65,536×100 Hz, or 216×100 Hz); used also in red boxes
7.372800	UART clock (4×1.8432 MHz); allows integer division to common baud rates
9.216000	Allows integer division to 1024 kHz and binary division to lower frequencies that are whole multiples of 1 Hz.
11.059200	UART clock (6×1.8432 MHz); allows integer division to common baud rates
12.000000	USB systems reference clock for full-speed PHY rate of 12 Mbit/s, or PLL multiplied up for speed PHYs at 480 Mbit/s

Ex. 1: TI MSP430F149



- The basic clock module includes two or three clock sources:
  - LFXT1CLK: Low-/high-frequency oscillator
    - Low-frequency 32,768-Hz watch standard crystals
    - External clock sources in the 450-kHz to 8-MHz range
  - XT2CLK: Optional high-frequency oscillator
    - Standard crystals, resonators
    - External clock sources in the 450-kHz to 8-MHz range
  - DCOCLK: Internal digitally controlled oscillator (DCO) with RC-type characteristics
    - SW adjustable frequency

Ex. 2: MC68HC08BD24

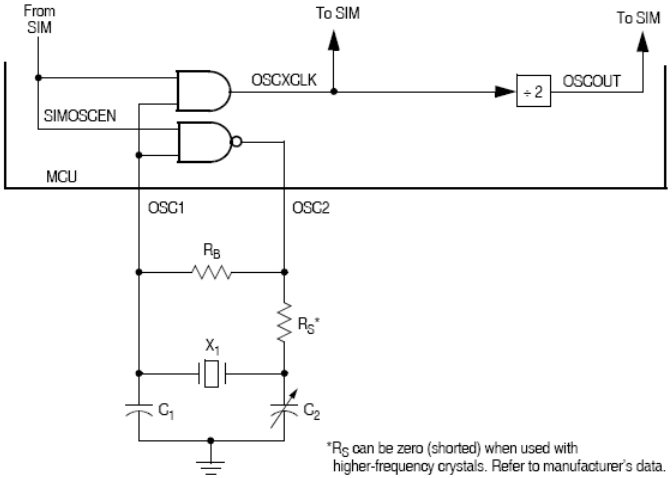


Figure 8-1. Oscillator External Connections

- OSC1: Input to the crystal amplifier oscillator (3.3V)
  - Can also be driven by an externally generated clock, leaving the OSC2 pin float.
- OSC2: Crystal oscillator inverting amplifier output (3.3V)

19.8 Oscillator Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Crystal Frequency[1]	$f_{OSCXCLK}$	—	24	—	MHz
External Clock Reference Frequency[1], [2]	$f_{OSCXCLK}$	dc	—	24	MHz
Crystal Load Capacitance[3]	C_L	—	15	—	pF
Crystal Fixed Capacitance[3]	C_1	—	$2 \times C_L$	—	
Crystal Tuning Capacitance[3]	C_2	—	$2 \times C_L$	—	
Feedback Bias Resistor	R_B	—	10	—	MΩ
Series Resistor[3], [4]	R_S	—	—	—	

NOTES:

1. The sync processor module is designed to function at $f_{OSCXCLK}$ = 24 MHz. The values given here are oscillator specifications.
2. No more than 10% duty cycle deviation from 50%
3. Consult crystal vendor data sheet
4. Not Required for high frequency crystals

Ex. 3: Freescale MCF5206e

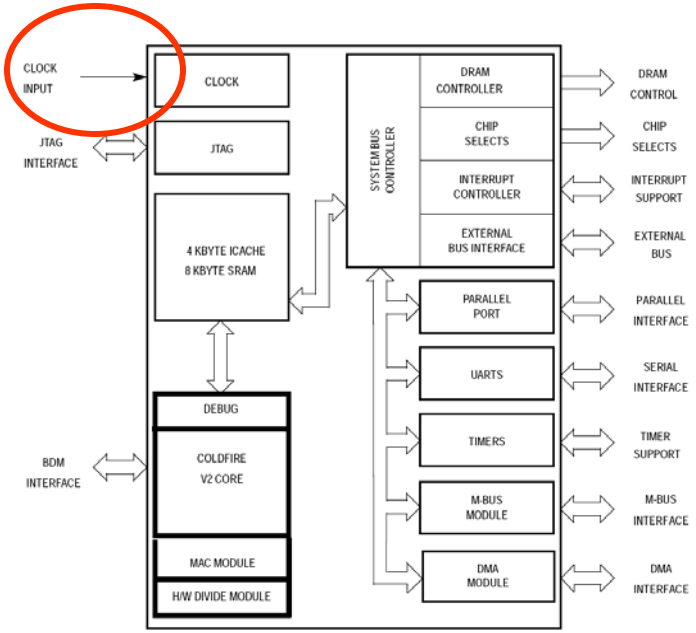


Figure 1-1. MCF5206e Block Diagram

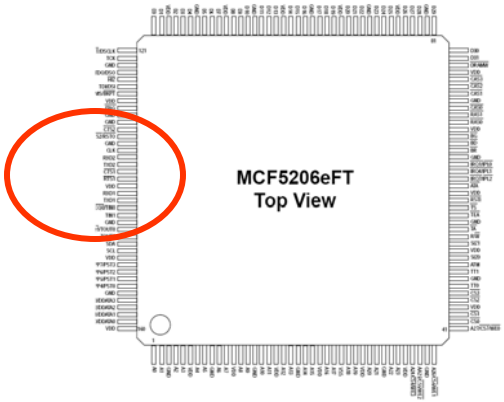


Table 17-6. Clock Input Timing Specifications

NAME	CHARACTERISTIC	40 MHz		54 MHz		UNIT
		MIN	MAX	MIN	MAX	
	Frequency of Operation[1]	0	40.00	0	54.00	MHz
C1	CLK cycle time	25	—	18.5	—	ns
C2[2]	CLK fall time(from V_h = 2.4V to V_l = 0.5V)	—	2	—	2	ns
C3[2]	CLK rise time (from V_l = 0.5V to V_h = 2.4V)	—	2	—	2	ns
C4	CLK duty cycle (measured at 1.5 V)	45	55	45	55	%
C4a[3]	CLK pulse width high (measured at 1.5 V)	11.25	13.75	8.33	10.19	ns
C4b[3]	CLK pulse width low (measured at 1.5 V)	11.25	13.75	8.33	10.19	ns

[1] CLK may be stopped to conserve power.
[2] Specification values are not tested.
[3] Specification values listed are for maximum frequency of operation.

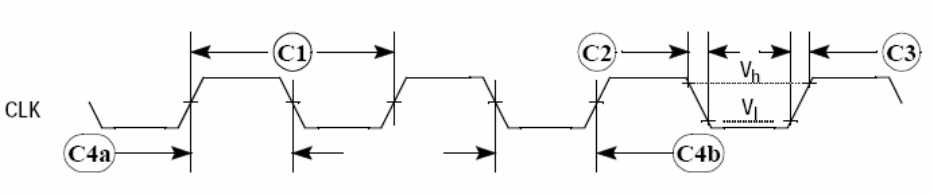


Figure 17-1. Clock Input Timing

Ex. 4: OMAP3530 Clock Specs

- The clock system accepts three input sources:
  - 32-kHz digital CMOS clock
  - Crystal oscillator or CMOS digital clock (12, 13, 16.8, 19.2, 26, or 38.4 MHz)
  - Alternate clock (48 or 54 MHz, or other up to 59 MHz)
- Internal PLL frequency multipliers produce f_{CLK} up to 700MHz

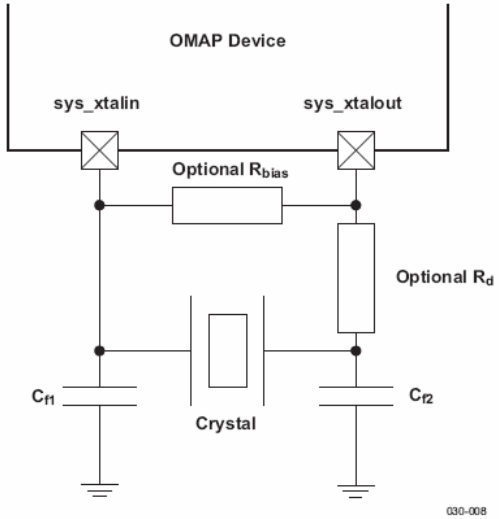


Figure 4-2. Crystal Implementation(1)(2)(3)(4)

Table 4-1. Clock Source Requirements

PAD	CLOCK FREQUENCY		STABILITY	DUTY CYCLE	JITTER	TRANSITION
sys_xtalout sys_xtalin	12, 13, 16.8, or 19.2 MHz	Crystal	± 25 ppm	na	na	na
	12, 13, 16.8, 19.2, 26, or 38.4 MHz	Square	± 50 ppm	45% to 55%	< 1%	< 3.6 ns
sys_altclk	48,54 or up to 59 MHz		± 50 ppm	40% to 60%	< 1%	< 5 ns

OMAP3530 Clock Specs (Cont)

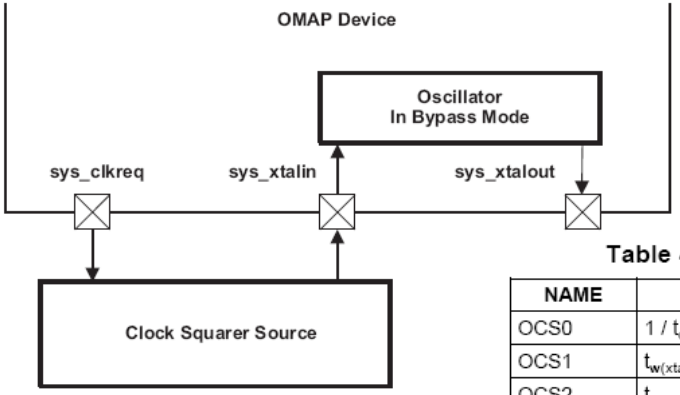


Table 4-5. 12-, 13-, 16.8-, 19.2-, 26-, or 38.4-MHz Input Clock Squarer Timing Requirements

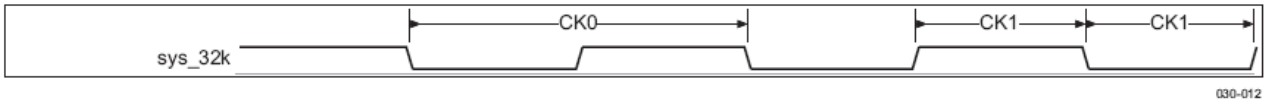
NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
OCS0	$1 / t_{c(xtalin)}$	Frequency, sys_xtalin	12, 13, 16.8, 19.2, 26, or 38.4			MHz
OCS1	$t_{w(xtalin)}$	Pulse duration, sys_xtalin low or high	0.45 * $t_{c(xtalin)}$		0.55 * $t_{c(xtalin)}$	ns
OCS2	$t_{J(xtalin)}$	Peak-to-peak jitter(1), sys_xtalin	–1%		1%	
OCS3	$t_{R(xtalin)}$	Rise time, sys_xtalin			3.6	ns
OCS4	$t_{F(xtalin)}$	Fall time, sys_xtalin			3.6	ns
OCS5	$t_{J(xtalin)}$	Frequency stability, sys_xtalin			±25	ppm

(1) Peak-to-peak jitter is defined as the difference between the maximum and the minimum output periods on a statistical population of 300 period samples. The sinusoidal noise is added on top of the vdds supply voltage.

Table 4-7. 32-kHz Input Clock Source Timing Requirements(1)

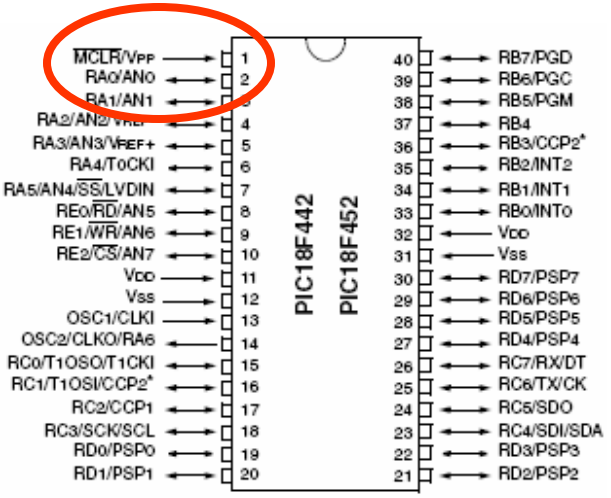
NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
CK0	$1 / t_{c(32k)}$	Frequency, sys_32k		32.768		kHz
CK3	$t_{R(32k)}$	Rise time, sys_32k			20	ns
CK4	$t_{F(32k)}$	Fall time, sys_32k			20	ns
CK5	$t_{J(32k)}$	Frequency stability, sys_32k			±200	ppm

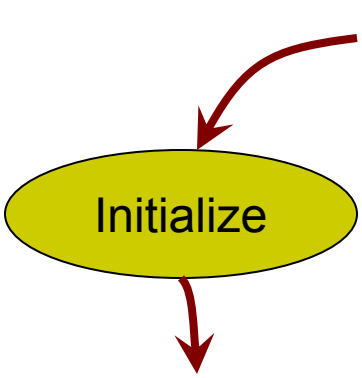
(1) See Table 3-4, *Electrical Characteristics*, Standard LVCMOS IOs part for sys_32k V_{IH}/V_{IL} parameters.

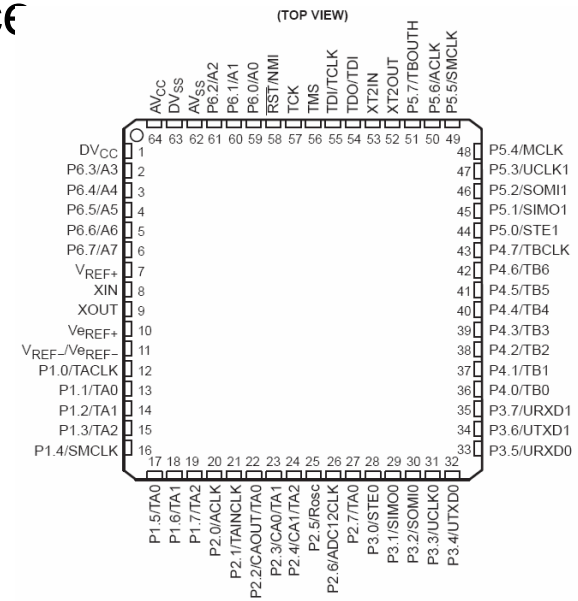


Power-on Reset (POR)

- Provides the start-up signal for the CPU
  - Fed through RESET pin
  - Brings the CPU FSM to its initial state
    - PC = Reset address
    - SR = Clear
    - IF = Disabled
- Makes CPU execute boot sequence

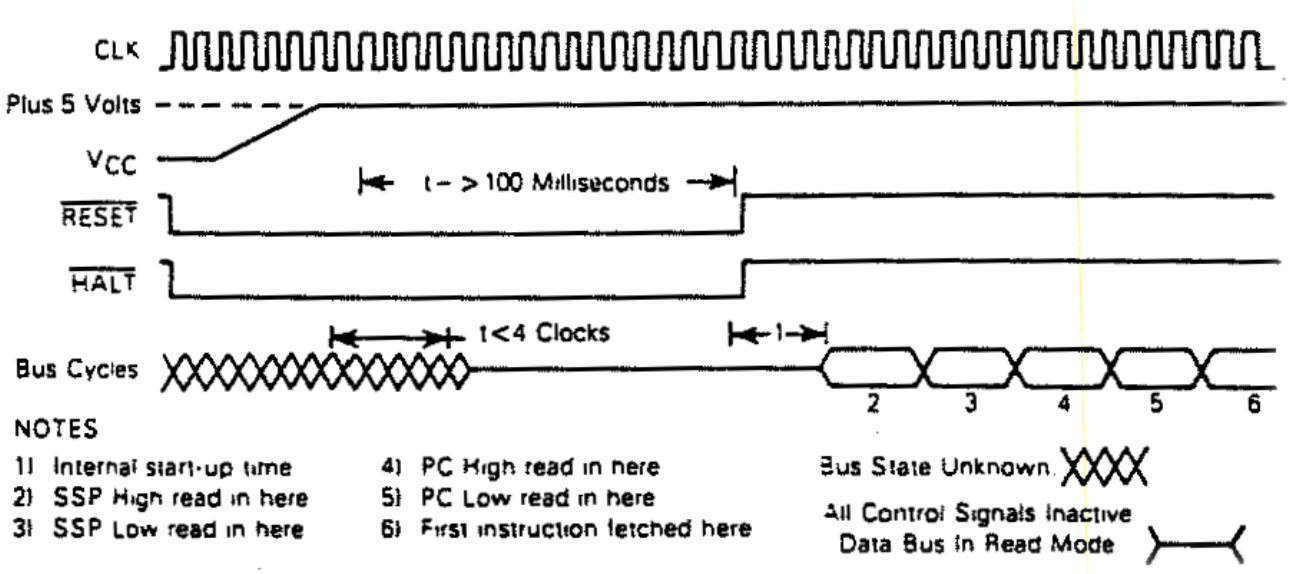






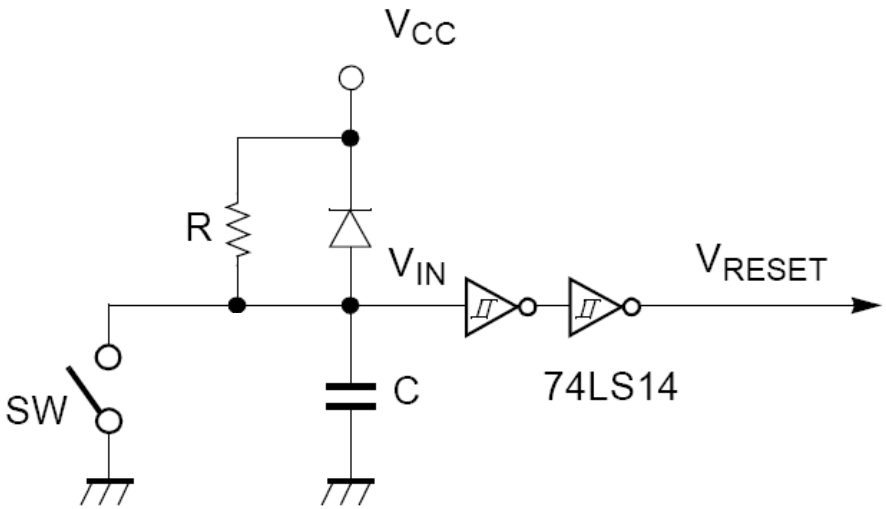
POR Signal Requirements

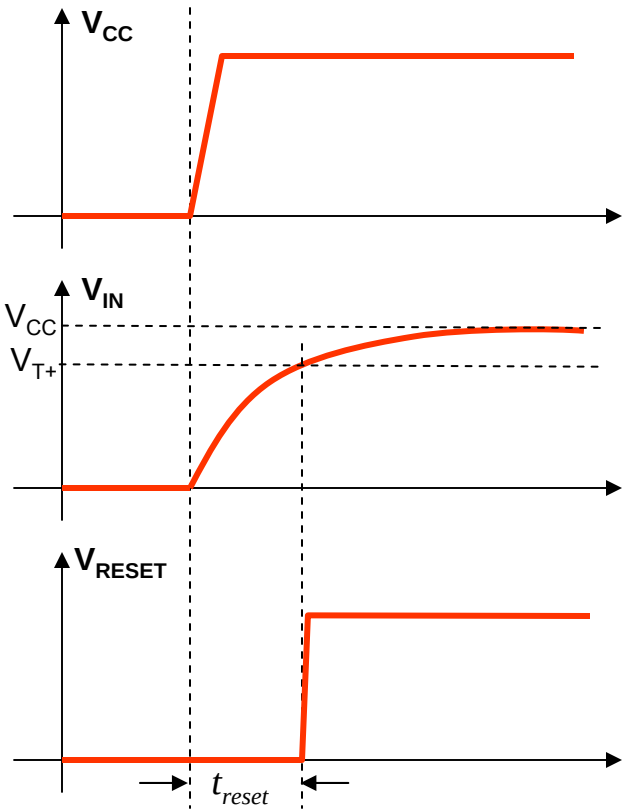
- Assertion level
  - High or Low: depends on specific CPU
- Synchronization
  - Minimum pulse width after V_{DD} stabilization
  - Usually measured in No. of f_{CLK} cycles
  - Requires a Power-on Reset (POR) circuit



A Simple POR Circuit

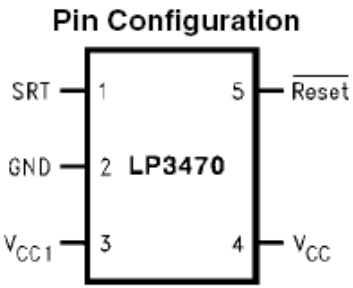
- One-shot with Manual Override

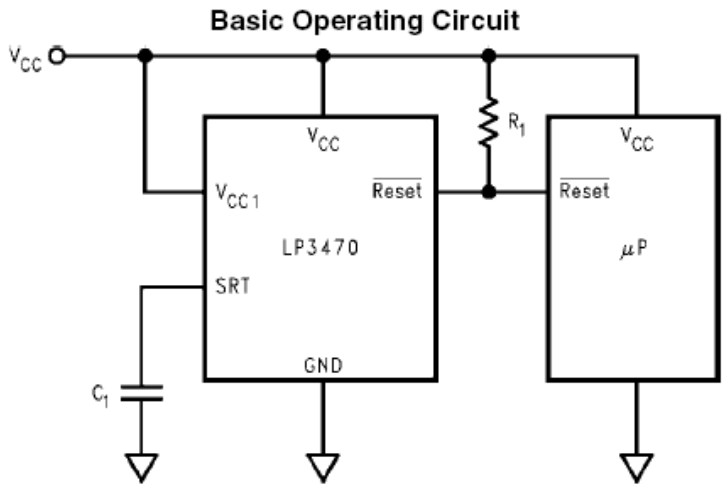


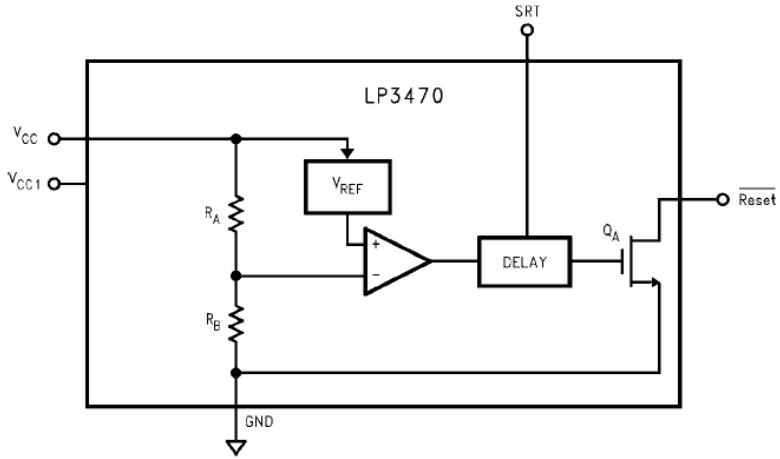


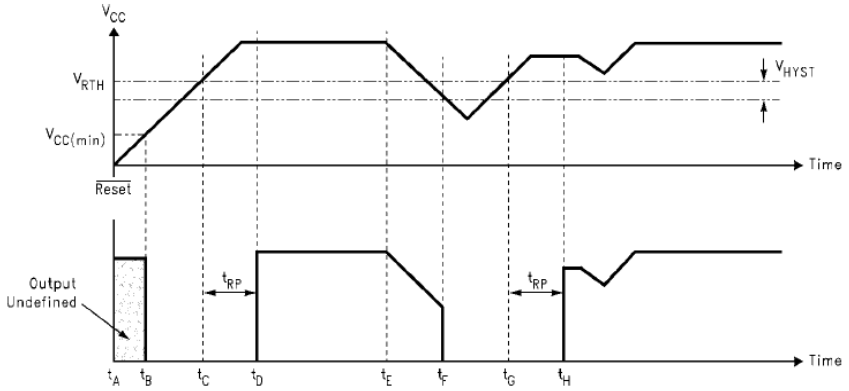
$$t_{reset} = RC \ln\left(\frac{Vcc}{V_{CC} - V_T^+}\right)$$

Dedicated Reset Supervisor

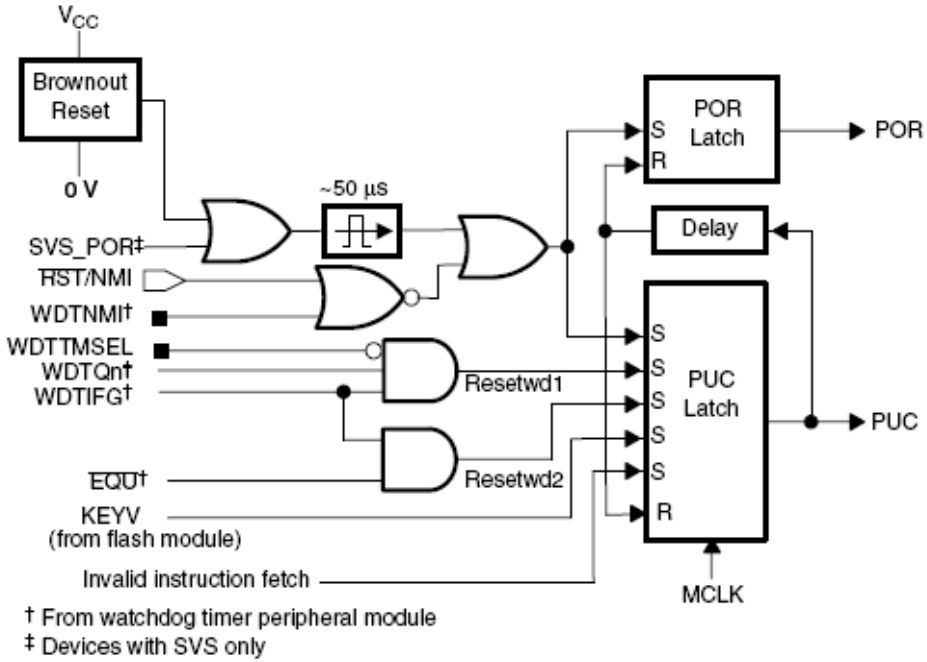








MSP430 POR Structure



MSP430 POR and PUC Schematic

A POR is a device reset. It is generated by one of the following events:

- Powering up the device
- A low signal on the RST/NMI pin when configured in the reset mode
- An SVS low condition when PORON = 1.

A PUC is always generated by a POR. A PUC does not generate a POR. The following events trigger a PUC:

- A POR signal
- Watchdog timer expiration when in watchdog mode only
- Watchdog timer security key violation
- A Flash memory security key violation
- A CPU instruction fetch from the peripheral address range 0h − 01FFh

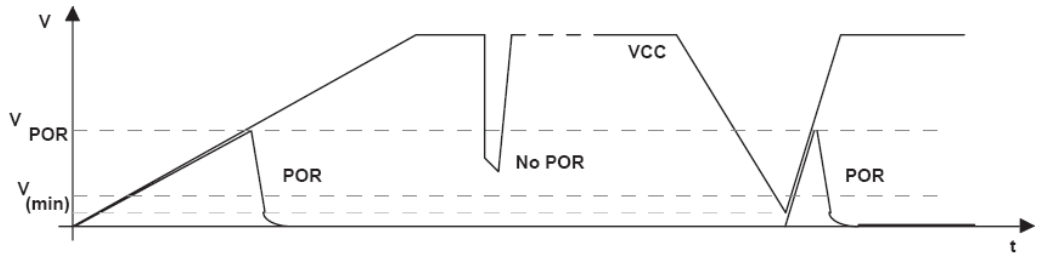
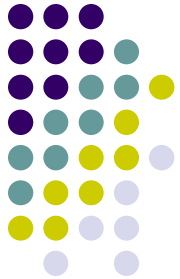


Figure 10. Power-On Reset (POR) vs Supply Voltage

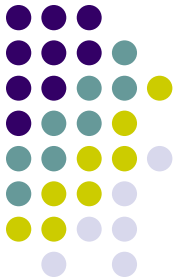
Boot Strap Loader



- Service routine executed upon RESET
  - Address programmed in the RESET entry
- Must initialize the system:
  - Configure I/O ports
  - Program peripherals (Timers, UARTs, ADCs, DMAs, Display devices, etc.)
  - Set-up stack
  - Enable Interrupts (local & global)
  - Initialize variables and status
- Activate operating mode
  - Low-power modes
  - Supervisory modes, etc
- Reachable only upon reset

```
        ORG RESET
        JMP Init
        ----
        ----
        ----
Init:   Set port mode
        Set time base
        ----
```

Summary



- Handling Precautions for Electronic Circuits
  - Electrostatic Discharge
- Understanding Data Sheets
  - Hardware and software components
  - Scope and consideration for diverse target applications
- Basic Interface for uP-based Systems
  - Power requirements
  - Clock sources
  - Hardware reset
  - Software initialization
  - Interfacing Considerations