INEL 4206. EXAM. FEBRUARY 27, 2012

Problem 1. Answer the following questions.

a. List four attributes of an embedded system.

   (a) Contains tightly coupled hardware and software componentes to perform a single function.

   (b) Is part of a larger system

   (c) Is not intended to be independently programmable by the user.

   (d) Is expected to work with minimal or no human intervention.

   (e) Reactive operation and heavily constrained.

b. What are the two major components of an embedded system?

   (a) Hardware components including a central processing unit usually in the form of a microcontroller.

   (b) Software components typically as firmware.

c. The 7-bit word $b_6b_5b_4b_3b_2b_1b_0$ is used to encode numbers in normal binary convention. What is the polynomial expression to decode decimal equivalent?
$b_6 * 2^6 + b_5 * 2^5 + b_4 * 2^4 + b_3 * 2^3 + b_2 * 2^2 + b_1 * 2^1 + b_0 * 2^0$

d. The 7-bit word $b_6b_5b_4b_3b_2b_1b_0$ is used to encode numbers in two's complement convention. What is the polynomial expression to decode the decimal equivalent?
$-b_6 * 2^6 + b_5 * 2^5 + b_4 * 2^4 + b_3 * 2^3 + b_2 * 2^2 + b_1 * 2^1 + b_0 * 2^0$

e. How many different items can be differentiated using N-bit words?
Up to 2^N *different items.*

f. What is the interval of integers for unsigned numbers encoded in normal binary convention using N-bit words?
From 0 *to* $2^N - 1$

g. What is the interval of integers for signed numbers encoded in two's complement convention using N-bit words?
From -2^{N-1} *to* $+2^{N-1} - 1$

h. Apply sign extension to the following 7-bit words expressed in hex notation to transform them into 12-bit words in hex notation: 53h, 3Ah.
Since the most significant bit of 53h is a 1, 53h is a negative number which must be sign extended by adding 1's, whereas the most significant bit of 3Ah is a 0 indicating it is a positive number which is sign extended by adding 0's. Thus

53h = 1010011B sign extends to 111111010011B = FD3h
and
3Ah = 0111010B sign extends to 000000111010B = 03Ah.

i. What is the interval of integers for unsigned numbers encoded in BCD convention using 16-bit words?
00 to 99, if using unpacked BCD and 0000 to 9999, if using packed BCD.

j. Name the main components of a microcomputer system.
The main components of a microcomputer system are the central processing unit or CPU, the memory unit, the system buses, and the input/output subsystem.

k. What is a bus?
A set of lines carrying similar signals grouped and treated as a unit.

l. What is the difference between a microprocessor and a microcontroller.
A microprocessor is one of the components of a microcontroller. A microcontroller usually includes several peripheral, which are not included in a microprocessor, such as timers, digital to analog DAC and analog to digital ADC converters, communication interfaces, etc.

m. The width of an address bus is N. What is the largest size of memory that can be accessed by the CPU?
Up to 2^N locations.

n. The width of the data bus is M. What does this mean with respect to the data size that the CPU can process?
The CPU can process operands of M bits each.

o. Write the difference between data memory and program memory.
Data memory is typically where the data used by a program is stored. Program memory refers to the memory locations where the program instructions are stored.

p. The architecture of a microcomputer system which has the data and program in the same memory system is called _____. *Von Neumann architecture.*

q. The architecture of a microcomputer system which has the data and program in different memory subsystems is called _____. *Harvard architecture.*

r. What is the difference between a physical memory address and a data memory address?
Physical memory address is the address of the memory location itself. Data memory address refers to way data is stored in physical memory, i.e. beginning with the least significant byte stored in the first (lowest numbered) memory location or beginning with the most significant byte stored in the first memory location.

s. If the data address of the double word 2AF30456h is 0402h, what are the physical addresses of the individual bytes in a little endian memory system?
Little endian system: [0402h]=56h, [0403h]=04h, [0404h]=F3h, [0405h]=2Ah

t. Repeat the previous question for a big endian system.
Big endian system: [0402h]=2Ah, [0403h]=F3h, [0404h]=04h, [0405h]=56h

u. A memory segment of 512 bytes starts at address 0400h. What is the last address in the segment?
512 = 0200h, thus the last address in the system is 0400h + 0200h - 1 or 0400h + 01FFh = 05FFh.

Problem 2. Take X = 914h and Y= 624h. What decimal numbers are represented if

a. they are encoded in normal binary unsigned convention?
X=$(9 * 16^2 + 1 * 16^1 + 4 * 16^0 = 2324$ *and* $Y = 6 * 16^2 + 2 * 16^1 + 4 * 16^0 = 1572$

b. they are encoded in two's complement signed convention?
Since 914h=100100010100 and 624h=011000100100 then ($X = -1 * 2^1 1 + 1 * 2^8 + 1 * 2^4 + 4 * 2^0 = -1772$ *and* $Y = 6 * 16^2 + 2 * 16^1 + 4 * 16^0 = 1572$

c. they are encoded in BCD?
914 and 624

d. they are encoded with bias 1620?
X: 2324 - 1620 = 704 and Y: 1572 - 1620 = -48

Do the following operations with these numbers:

e. Sign extend to 14 bits and express the result in hex notation and octal notation.

914h to 3914h = 34424Q and 624h to 0624h = 03044Q

f. Realize de operation X+y and X-Y in BCD convention.
X + Y = 914h + 624h = F38h then F38h + 600h = 1538h and
X - Y = 914h - 624h = 2F0h then 2F0h - 060h = 290h

g. Assuming they represent numbers in two's complement convention, realize Y-X using two's complement addition and tell if there is an overflow or not, Justify your answer.
X' (2's complement) = FFF - 914 + 1 = 6EC and thus Y - X = Y + X' = 624 + 6EC = D10.

If treated as signed numbers, then there is an overflow since the addition of 2 numbers of the same sign, positive, yielded a different sign number, negative.

If treated as unsigned numbers, then there is not an overflow since the carry out of the most significant position is zero.

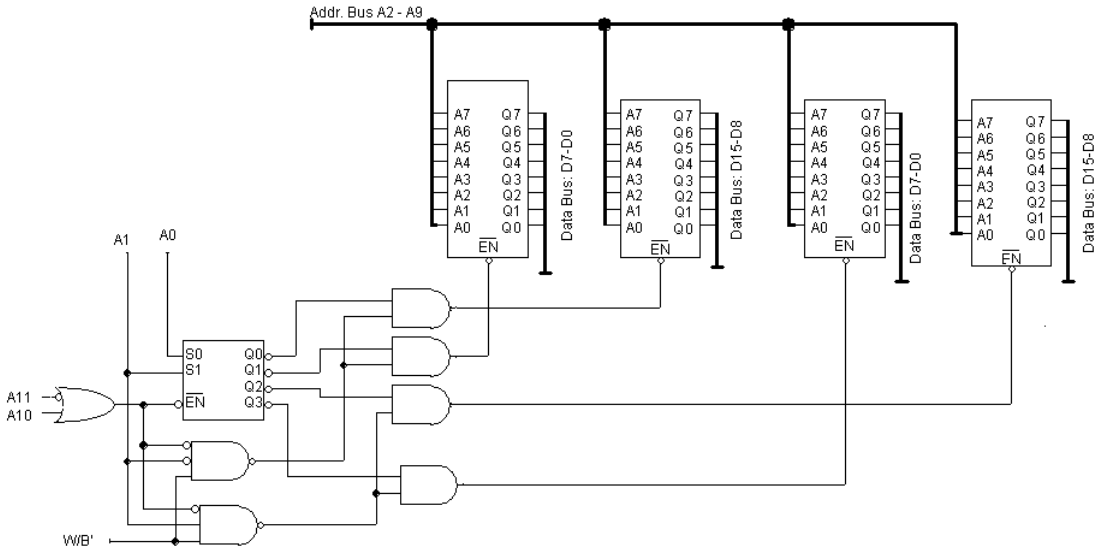
Problem 3. The following figure represents a 1KB memory segment space for a microcontroller with a 16-bit data bus, and a 12-bit address bus.

a. How many address locations are possible for this microcontroller and what is the total address space range? (Express the initial and final addresses in hex notation) *Ans.* 2^{12}*=4K, 000h to FFFh*

b. What is the range of addresses covered by the connection of the figure? *Ans. 800h to BFFh.*

c. What is the range covered by each memory module? *Ans. See explanation*

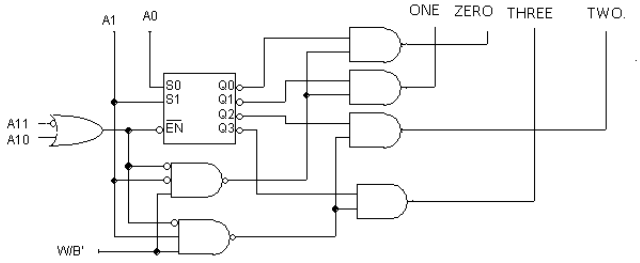
d. Does this connection corresponds to a big endian or a little endian type storage? *Ans. Big endian*



Solution

a. There are $2^{12} = 4K = 4096$ possible memory locations for the microcontroller, with addresses 000h to FFFh.

b. To simplify discussion, the address decoder is isolated in the following figure. From left to write, let us call the modules ONE, ZERO, THREE and TWO, which are enabled when the respective output from the address decoder is 0.



Any combination of address bus bits with A11=0 or A10=1 will yield a 1 at every output of the address decoder logic circuit. Hence, A11=1 and A10 = 0 is the only combination that will allow access to the modules. Therefore, the lowest

address is 1000 0000 0000B = 800h and the largest address 1011 1111 1111B = BFFh. These correspond, respectively, to the cases when all other bits are zero, and when all other bits are one.

c. To find the individual addresses, only A11=0 and A10 = 1 yield possible activations. We need to consider also the signal W/B'= 1. An analysis of the address decoder yields the following table:

A11	A10	W/B'	A1	A0	ONE	ZERO	THREE	TWO
1	0	0	0	0	1	0	1	1
1	0	0	0	1	0	1	1	1
1	0	0	1	0	1	1	1	0
1	0	0	1	1	1	1	0	1
1	0	1	0	X	0	0	1	1
1	0	1	1	X	1	1	0	0
0	X	X	X	X	1	1	1	1
X	1	X	X	X	1	1	1	1

Therefore, when W/B'=0, only bytes are considered since only one module is activated:

Module ZERO takes all addresses ending with 00 in the range 0100 0000 0000 to 0111 1111 1100. (800h to BFCh).
Module ONE takes all addresses ending with 01 in the range 0100 0000 0001 to 1011 1111 1101. (801h to BFDh).

Module TWO takes all addresses ending with 10 in the range 1000 0000 0010 to 1011 1111 1110. (802h to BFEh).
Module THREE takes all addresses ending with 11 in the range 0100 0000 0011 to 0111 1111 1111. (803h to BFFh).

In table form, for W/B'=0:

MODULE	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
ZERO	1	0	X	X	X	X	X	X	X	X	0	0
ONE	1	0	X	X	X	X	X	X	X	X	0	1
TWO	1	0	X	X	X	X	X	X	X	X	1	0
THREE	1	0	X	X	X	X	X	X	X	X	1	1

When W/B'=1, modules are activated by pairs, generating word-size data.
ZERO and ONE on one hand if A1=0, covering word-size data addresses ending with 00;
THREE and TWO if A1=1, covering word-size data addresses ending with 10.

d. When W/B'=1, working with word-size data. For A=0, module ONE takes the highest address (ending with 01) and module ZERO the lowest (ending with 00). They are connected, respectively, to the least significant and most significant bytes of the Data bus word.

The same reasoning is applied for A=1, with modules THREE and TWO holding the highest and lowest addresses. Therefore, this connection is an example of a **big endian** type.

Problem 4. The following sequence of operations with memory contents refer to 16-bit data in each case. Numbers without suffix are decimal.

Step 1: (0304h)← 14657

Step 2: (0306h)← 8932

Step 3: (0308h)← (0304h)

Step 4: (0308h)← (0308h) + (0304h)

Step 5: (0306h)← (0306h) + (0306h)

Step 6: (0308h)← (0308h) - (0306h)

a. In the table below, write the memory contents at each physical addresses after the step indicated, assuming little endian convention. For those cells with unknown contents, write XX.

b. Among the set of expressions { 3X+2Y, 2X + 3Y, 3X-2Y, 2X - 3Y}, which one represents the goal of the sequence? Justify your answer showing the numerical operation and verifying that the contents at the end reflects the numerical answer.

Step 1

Address	Cell
030Ah	
0309h	
0308h	
0307h	
0306h	
0305h	
0304h	
0303h	

Step 2

Address	Cell
030Ah	
0309h	
0308h	
0307h	
0306h	
0305h	
0304h	
0303h	

Step 3

Address	Cell
030Ah	
0309h	
0308h	
0307h	
0306h	
0305h	
0304h	
0303h	

Step 4

Address	Cell
030Ah	
0309h	
0308h	
0307h	
0306h	
0305h	
0304h	
0303h	

Step 5

Address	Cell
030Ah	
0309h	
0308h	
0307h	
0306h	
0305h	
0304h	
0303h	

Step 6

Address	Cell
030Ah	
0309h	
0308h	
0307h	
0306h	
0305h	
0304h	
0303h	

Solution

a. 14657 = 3941h and 8932 = 22E4h. With this information and considering the little endian convention, the table is filled as follows. Here, for sake of clarity, the

addresses in the source side have been substituted with the value to be considered.

Step 1: (0304h)← 3941h

Address	Cell
030Ah	XX
0309h	XX
0308h	XX
0307h	XX
0306h	XX
0305h	39
0304h	41
0303h	XX

Step 2:(0306h)← 22E4h

Address	Cell
030Ah	XX
0309h	XX
0308h	XX
0307h	22
0306h	E4
0305h	39
0304h	41
0303h	XX

Step 3: (0308h)← 3941h

Address	Cell
030Ah	XX
0309h	39
0308h	41
0307h	22
0306h	E4
0305h	39
0304h	41
0303h	XX

Step 4: (0308h)← 3941h+3941h

Address	Cell
030Ah	XX
0309h	72
0308h	82
0307h	22
0306h	E4
0305h	39
0304h	41
0303h	XX

Step 5: (0306h)← 22E4h+22E4h

Address	Cell
030Ah	XX
0309h	72
0308h	82
0307h	45
0306h	C8
0305h	39
0304h	41
0303h	XX

Step 5: (0308h)← 7282h-45C8h

Address	Cell
030Ah	XX
0309h	2C
0308h	BA
0307h	45
0306h	C8
0305h	39
0304h	41
0303h	XX

b. The program does not realize any of the operations in the set. It realizes an operation of the form 2X - 2Y, with X = 14,657 and Y = 8,932. The operation yields 11,450, whose hex equivalent is 2CBAh, stored at address 0308.