Microprocessor Interfacing INEL-4217
First Partial Exam

Name Clave ID# _____ Sec. _____

Part One: Theory (40%)

NOTE: *This part of the exam **must** be completed **without** any aid material.*

1.1 Discuss the difference between semi-synchronous and asynchronous buses. Point out advantages and disadvantages of each. (20%)

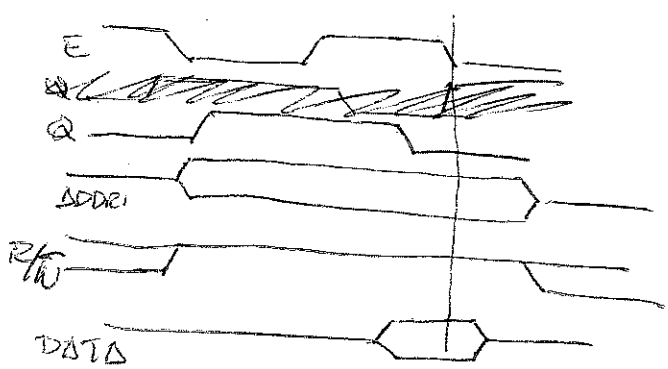
1.2 Explain the style used by **Motorola** in the design of its basic control bus. Use a simplified timing diagram to clarify your explanations. (20%)

1.1 Semi synch: All devices spected to finish on time. If any requires more time, assert $\overline{RDY}$ or WAIT signal.
Asynch: No device is spected to finish on time. When over, device must assert $\overline{DTACK}$ signal.

Semi synch: Requires less hardware, since only slow devices need to drive WAIT signal. However data is prone to be garbled in invalid address accesses.

Asynch: Data confidence is high since watch-dog ckt can be included to detect errors and avoid invalid lectures. However more hardware is required since ACK signal must be given by all devices. (also watchdog) ACK is required from all devices.

1.2 The MOTO style uses separated signals for providing access time and transfer direction. Address & Data buses are demux.



E → Indicates access time end with H→L transition

R/W → Transfer direction. Carries no timing info

Q → asserted for valid address

Access time: address valid to H→L transition of E

INEL 4217 First Partial Exam

Name _____ ID# _____ Sec. _____

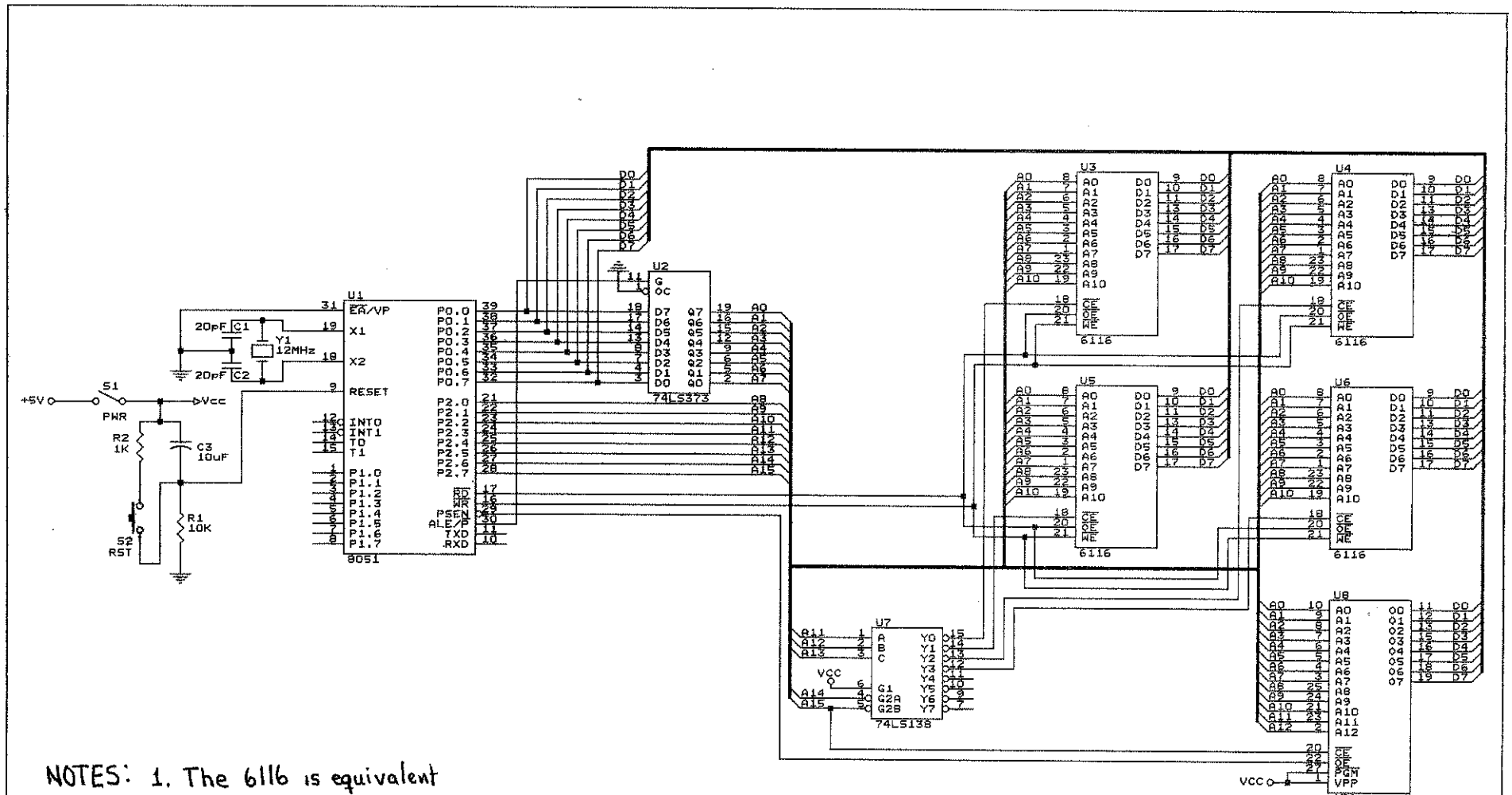
Part Two: Problems (60%)

NOTE: *The usage of aid materials is allowed for completing this part.*

Given the schematic in Figure 1, perform the following analyses using information extracted from the attached data sheets:

2.1 Perform a complete DC bus loading analysis for all devices in the schematics. Based on your analysis, give your recommendations about line interconnections (i.e. where might be drivers needed, if any). Also indicate how much supply current will require this circuit to operate. (35%)
NOTE: Make sure of showing all the computations you made to perform your analysis. Recommendations without support computations will not be considered.

2.2 Perform a timing analysis for [redacted] all accesses in the system. To simplify your computations, assume that all propagation delays, set-up, and hold times are negligible. Based on the results of your analysis, give your timing recommendations about the circuit. (25%)
NOTE: Here again, only recommendations based on your computations will be considered.



NOTES: 1. The 6116 is equivalent to a 5116S-12

2. The 2764 is actually a 2764A-25

Part II First Partial Exam		
Title	8051 BOARD	
Size	Document Number	
B	INEL42175081-091	
Date:	March 1, [illegible]	Sheet 1 of

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on $\overline{EA}$/V_{PP} Pin to V_{SS} . . . −0.5V to +21.5V
Voltage on Any Other Pin to V_{SS} . . . . −0.5V to +7V
Power Dissipation 1.5W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Operating Conditions: T_A (Under Bias) = 0°C to +70°C; V_{CC} = 5V ±10%; V_{SS} = 0V

D.C. CHARACTERISTICS (Under Operating Conditions)

Symbol	Parameter		Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (Except $\overline{EA}$ Pin of 8751H & 8751H-8)		−0.5	0.8	V	
V_{IL1}	Input Low Voltage to $\overline{EA}$ Pin of 8751H & 8751H-8		0	0.7	V	
V_{IH}	Input High Voltage (Except XTAL2, RST)		2.0	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage to XTAL2, RST		2.5	V_{CC} + 0.5	V	XTAL1 = V_{SS}
V_{OL}	Output Low Voltage (Ports 1, 2, 3)*			0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$)*					
		8751H, 8751H-8		0.60 0.45	V V	I_{OL} = 3.2 mA I_{OL} = 2.4 mA
		All Others		0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, $\overline{PSEN}$)		2.4		V	I_{OH} = −80 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)		2.4		V	I_{OH} = −400 μA
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3, RST) 8032AH, 8052AH All Others			−800 −500	μA μA	V_{IN} = 0.45V V_{IN} = 0.45V
I_{IL1}	Logical 0 Input Current to $\overline{EA}$ Pin of 8751H & 8751H-8 Only			−15	mA	V_{IN} = 0.45V
I_{IL2}	Logical 0 Input Current (XTAL2)			−3.2	mA	V_{IN} = 0.45V
I_{LI}	Input Leakage Current (Port 0) 8751H & 8751H-8 All Others			±100 ±10	μA μA	0.45 ≤ V_{IN} ≤ V_{CC} 0.45 ≤ V_{IN} ≤ V_{CC}
I_{IH}	Logical 1 Input Current to $\overline{EA}$ Pin of 8751H & 8751H-8			500	μA	V_{IN} = 2.4V
I_{IH1}	Input Current to RST to Activate Reset			500	μA	V_{IN} < (V_{CC} − 1.5V)
I_{CC}	Power Supply Current: 8031/8051 8031AH/8051AH 8032AH/8052AH 8751H/8751H-8			 160 125 175 250	 mA mA mA mA	 All Outputs Disconnected; $\overline{EA}$ = V_{CC}
C_{IO}	Pin Capacitance			10	pF	Test freq = 1 MHz

***NOTE:**
Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.

intel MCS®-51

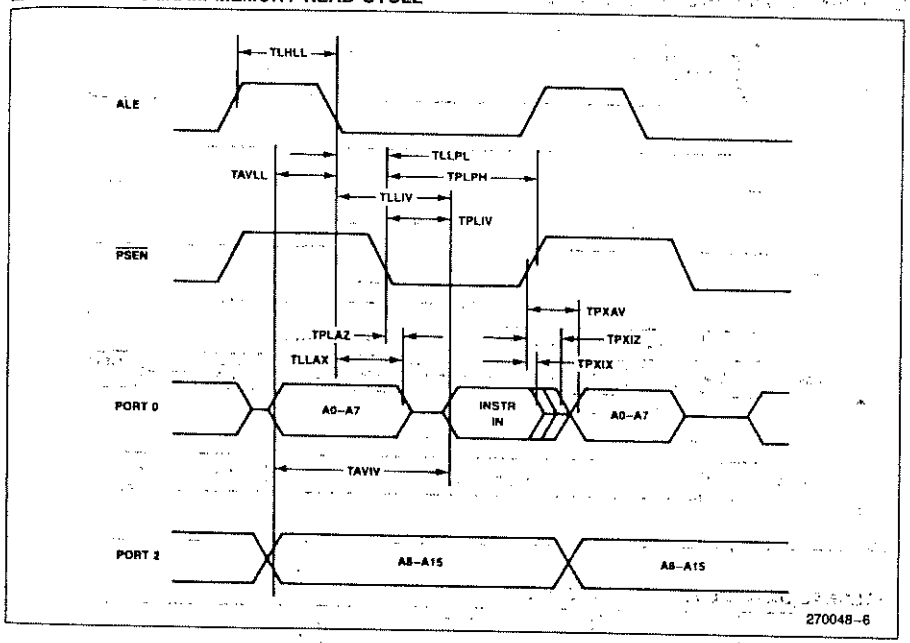
A.C. CHARACTERISTICS Under Operating Conditions;

Load Capacitance for Port 0, ALE, and PSEN = 100 pF;
Load Capacitance for All Other Outputs = 80 pF

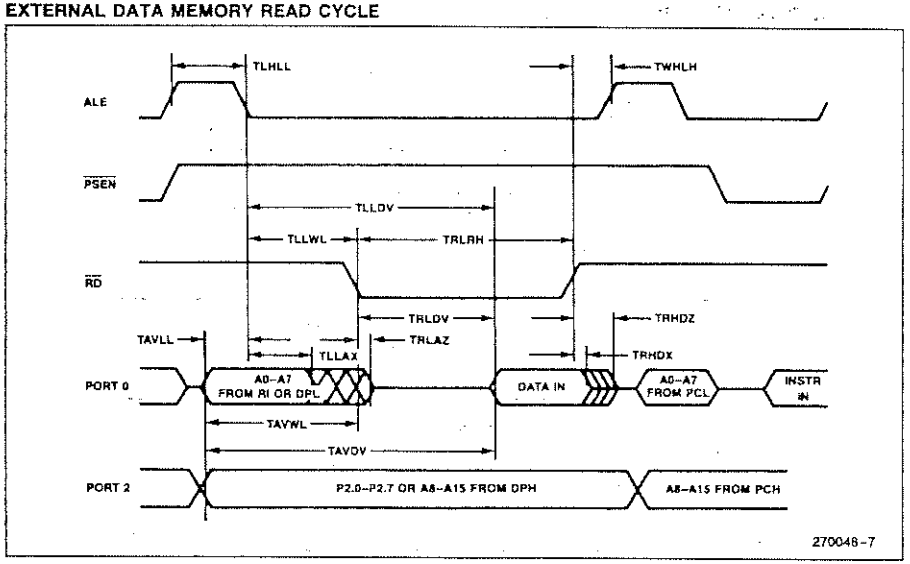
Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	12.0	MHz
TLHLL	ALE Pulse Width	127		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	43		TCLCL−40		ns
TLLAX	Address Hold after ALE Low	48		TCLCL−35		ns
TLLIV	ALE Low to Valid Instr In 8751H All Others		 183 233		 4TCLCL−150 4TCLCL−100	 ns ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	58		TCLCL−25		ns
TPLPH	$\overline{PSEN}$ Pulse Width 8751H All Others	 190 215		 3TCLCL−60 3TCLCL−35		 ns ns
TPLIV	$\overline{PSEN}$ Low to Valid Instr In 8751H All Others		 100 125		 3TCLCL−150 3TCLCL−125	 ns ns
TPXIX	Input Instr Hold after $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instr Float after $\overline{PSEN}$		63		TCLCL−20	ns
TPXAV	$\overline{PSEN}$ to Address Valid	75		TCLCL−8		ns
TAVIV	Address to Valid Instr In 8751H All Others		 267 302		 5TCLCL−150 5TCLCL−115	 ns ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		20		20	ns
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6TCLCL−100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		252		5TCLCL−165	ns
TRHDX	Data Hold after $\overline{RD}$	0		0		ns
TRHDZ	Data Float after $\overline{RD}$		97		2TCLCL−70	ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL−150	ns
TAVDV	Address to Valid Data In		585		9TCLCL−165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		4TCLCL−130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition 8751H All Others	 13 23		 TCLCL−70 TCLCL−60		 ns ns
TQVWH	Data Valid to $\overline{WR}$ High	433		7TCLCL−150		ns
TWHQX	Data Hold after $\overline{WR}$	33		TCLCL−50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		20		20	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High 8751H All Others	 33 43	 133 123	 TCLCL−50 TCLCL−40	 TCLCL+50 TCLCL+40	 ns ns

NOTE:
*This table does not include the 8751-8 A.C. characteristics (see next page).

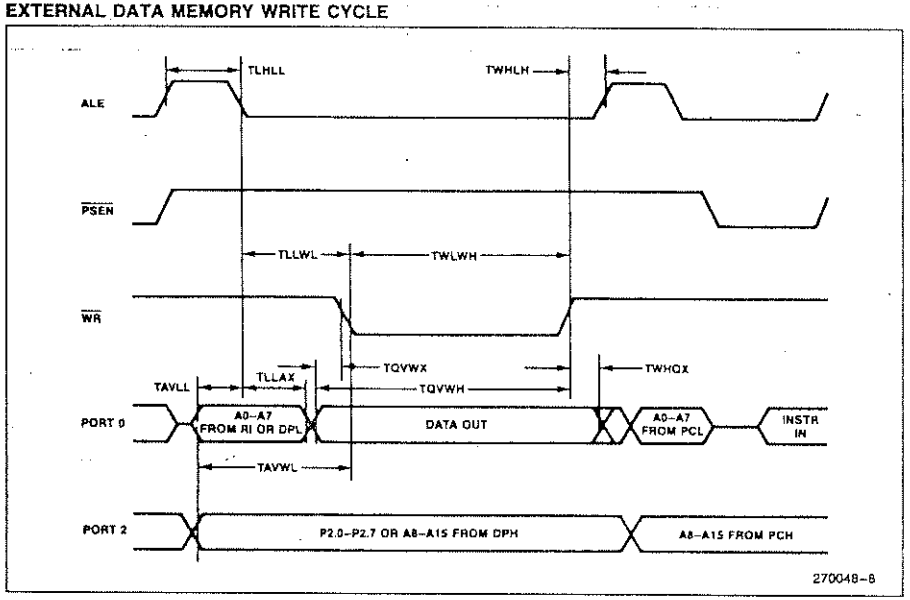
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read ..... 0°C to +70°C
Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +125°C
All Inputs or Output Voltages with
Respect to Ground ..... −0.6V to +6.25V
Voltage on Pin 24 with
Respect to Ground ..... −0.6V to +13.5V
V_{PP} Supply Voltage with
Respect to Ground
During Programming ..... −0.6V to +14.0V
V_{CC} Supply Voltage with Respect
to Ground ..... −0.6V to +7.0V

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READ OPERATION

D.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Symbol	Parameter	Limits			Conditions
		Min	Max	Unit	
I_{LI}	Input Load Current		10	µA	$V_{IN} = 0V$ to V_{CC}
I_{LO}	Output Leakage Current		10	µA	$V_{OUT} = 0V$ to V_{CC}
I_{PP}[2]	V_{PP} Current Read		5	mA	$V_{PP} = 5.5V$
I_{SB}	V_{CC} Current Standby		35	mA	$\overline{CE} = V_{IH}$
I_{CC}[2]	V_{CC} Current Active		75	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 1	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400$ µA
V_{PP}[2]	V_{PP} Read Voltage	3.8	V_{CC}	V	$V_{CC} = 5.0V \pm 0.25V$

A.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Versions[4]	$V_{CC} \pm 5\%$	2764A-1		2764A-2		2764A		Unit	Test Conditions
	$V_{CC} \pm 10\%$			2764A-20		2764A-25			
Symbol	Parameter	Min	Max	Min	Max	Min	Max		
t_{ACC}	Address to Output Delay		180		200		250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		180		200		250	ns	$\overline{OE} = V_{IL}$
t_{OE}	$\overline{OE}$ to Output Delay		65		75		100	ns	$\overline{CE} = V_{IL}$
t_{DF}[3]	$\overline{OE}$ High to Output Float	0	55	0	55	0	60	ns	$\overline{CE} = V_{IL}$
t_{OH}[3]	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

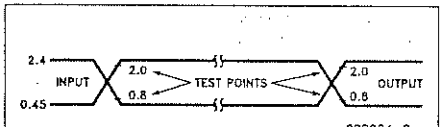
NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP}. The maximum current value is with outputs O_0 to O_7 unloaded.
3. This parameter is only sampled and is not 100% tested. Output Data Float is defined as the point where data is no longer driven—see timing diagram on the following page.
4. Model Number Prefixes: No prefix = CERDIP.

intel 2764A

CAPACITANCE[2] ($T_A = 25°C$, f = 1 MHz)

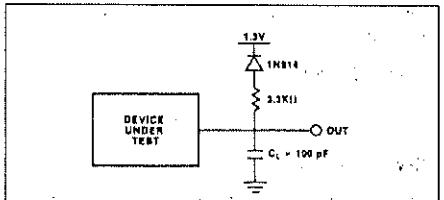
Symbol	Parameter	Typ[1]	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

A.C. TESTING INPUT/OUTPUT WAVEFORM



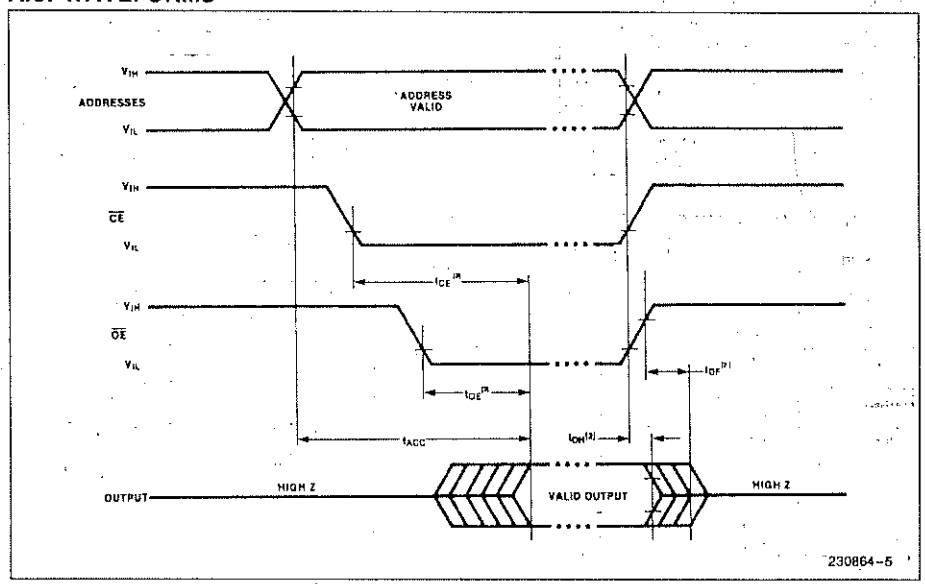
A.C. Testing: Inputs are Driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L Includes Jig Capacitance

A.C. WAVEFORMS



NOTES:
1. Typical values are for $T_A = 25°C$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground (V_{IN}, V_{OUT}) ..... −0.3V to +7V
Storage Temperature (T_{stg}) ..... −55°C to +150°C
Power Dissipation (P_D) 1.0W
DC Continuous Output Current (I_{OS}) ..... 50 mA

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RECOMMENDED OPERATING CONDITIONS Voltage referenced to V_{SS}, T_A = 0°C to 70°C

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2		V_{CC}+0.3	V
V_{IL}	Input Low Voltage	−0.3		0.8	V

NOTE:
1. During transitions, the inputs may undershoot to −3.5V for periods less than 20 ns.

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Min	Max	Unit
C_{IN1}	Input Capacitance (V_{IN} = 0V)		6	pF
C_{OUT}	Output Capacitance (V_{OUT} = 0V)		8	pF

NOTE:
This parameter is sampled and not 100% tested.

D.C. AND OPERATING CHARACTERISTICS

Recommended Operating Conditions unless otherwise noted

Symbol	Parameter		Min	Typ	Max	Units	Test Conditions
I_{CC1}	Operating Current			30	40	mA	V_{CC} = Max, $\overline{CS}$ = V_{IL}, Outputs open
I_{CC2}	Dynamic Current			30	60	mA	T_{cyc} = Min, V_{CC} = Max, Outputs open
I_{SB}	Standby Current				3	mA	$\overline{CS}$ = V_{IH}
I_{SB1}		STD		4	50	µA	$\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} = GND to V_{CC}
		L		0.2*	2		
I_{LI}	Input Load Current		−1		1	µA	V_{CC} = Max, V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage		−1		1	µA	$\overline{CS}$ = V_{IH}, V_{CC} = Max, V_{OUT} = GND to V_{CC}
V_{OH}	Output High Voltage		2.4			V	I_{OH} = −1.0 mA
V_{OL}	Output Low Voltage				0.4	V	I_{OL} = 2.1 mA

*T_A = 25°C

A.C. TEST CONDITIONS

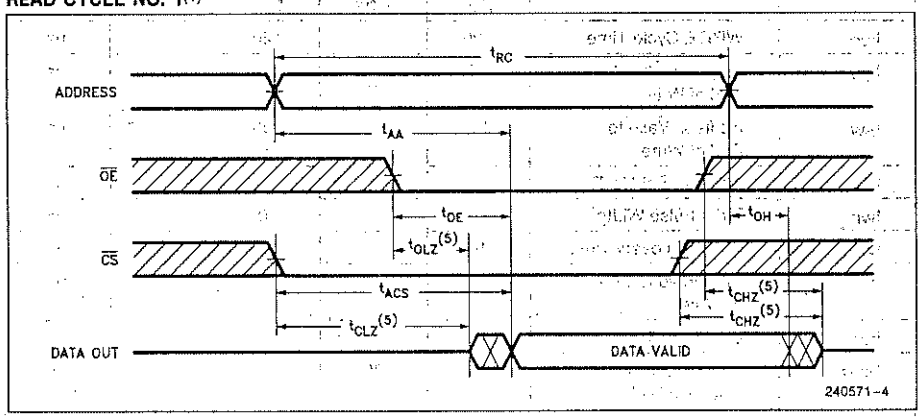
Input Pulse Levels ..... 0.8V to 2.4V
Input Rise and Fall Times ..... 10 ns
Timing Reference Level 1.5V
Output Load ..... 1 TTL Load + 100 pF

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10%

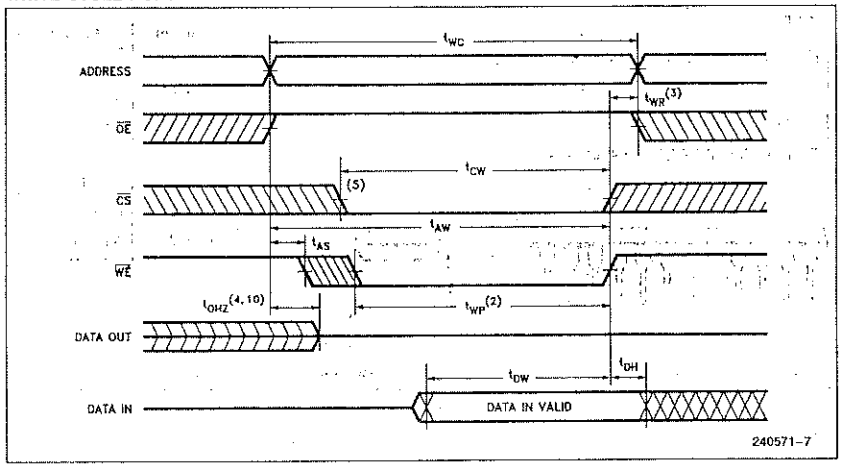
READ CYCLE

Symbol	Parameter	5116S-10		5116S-12		Unit
		Min	Max	Min	Max	
t_{RC}	READ Cycle Time	100		120		ns
t_{AA}	Address Access Time		100		120	ns
t_{ACS}	Chip Select Access Time		100		120	ns
t_{OH}	Output Hold from Address Change	10		10		ns
t_{CLZ}	Chip Selection to Output in Low Z	10		10		ns
t_{CHZ}	Chip Deselection to Output in High Z	0	40	0	40	ns
t_{OE}	Output Enable Access Time	40		50		ns
t_{OLZ}	Output Enable to Output in Low Z	10		10		ns
t_{OHZ}	Output Enable to Output in High Z	0	40	0	40	ns

READ CYCLE NO. 1(1)



WRITE CYCLE NO. 1[1]



WRITE CYCLE

Symbol	Parameter	5116S-10		5116S-12		Unit
		Min	Max	Min	Max	
t_{WC}	WRITE Cycle Time	100		120		ns
t_{CW}	Chip Selection to End of Write	65		70		ns
t_{AW}	Address Valid to End of Write	80		105		ns
t_{AS}	Address Set-Up Time	0		0		ns
t_{WP}	Write Pulse Width	60		70		ns
t_{WR}	Write Recovery Time	10		10		ns
t_{DW}	Data Valid to End of Write	30		35		ns
t_{DH}	Data Hold Time	10		10		ns
t_{WHZ}	Write Enable to Output in High Z	0	30	0	35	ns
t_{OW}	Output Active from End of Write	10		10		ns
t_{OHZ}	Output Disable to Output in High Z	0	40	0	40	ns

NOTES:
1. $\overline{WE}$ must be high during address transitions.
2. A Write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
4. During this period, I/O pins are in tri-state.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in tri-state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data on this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in output state.
10. Transition is measured at ±500 mV from steady state voltage.

Device Operation

The 5116S has two control inputs: Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$). $\overline{CS}$ is the power control pin and should be used for device operation. $\overline{WE}$ is the data control pin and should be used to gate data at the I/O pins.

Standby Power

The 5116S is placed in a standby or reduced power consumption mode by applying a high (V_{IH}) to the $\overline{CS}$ input. When in standby mode, the device is deselected and the outputs are in a high impedance state, independent of the $\overline{WE}$ input.

Table 1. Mode Selection Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	Standby	High Z	Standby
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	Active
L	X	H	Read	High Z	Active

Write Mode

Write Cycles may be controlled by either $\overline{WE}$ or $\overline{CS}$. In either case, both $\overline{WE}$ and $\overline{CS}$ must be high (V_{IH}) during address transitions. During a $\overline{WE}$ Controlled write cycle, $\overline{CS}$ must be held low (V_{IL}) while $\overline{WE}$ is low. Address transfers occur on the falling edge of $\overline{WE}$ and the data transfers on rising edge of $\overline{WE}$. During a $\overline{CS}$ controlled cycle, $\overline{WE}$ must be held low (V_{IL}) while $\overline{CS}$ is low. The addresses are then transferred on the falling edge of $\overline{CS}$ and data on the rising edge of $\overline{CS}$. Data, in both cases, must be valid for a time t_{DW} before the controlling input is brought high (V_{IH}) and remain valid for a time t_{DH} after the controlling input is high.

Read Mode

$\overline{CS}$ must be low (V_{IL}) and $\overline{WE}$ must be high (V_{IH}) to activate a read cycle and obtain data at the outputs. Given stable addresses, valid data is available after a time t_{AA}.

OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS — 54/74 SERIES "373"

54LS/74LS373

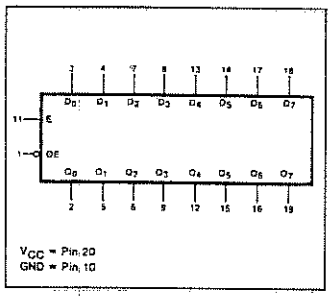
DESCRIPTION

The "373" is an 8-Bit Transparent Latch with 3-state buffered outputs. The latch outputs follow the data inputs when the latch Enable is HIGH, and they are stable when the Enable is LOW. The 3-state output buffers are controlled by an active LOW Output Enable ($\overline{OE}$) input. A HIGH on the $\overline{OE}$ input forces the eight outputs to the high impedance "off" state. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs.

FEATURES

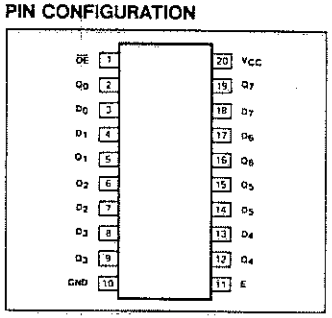
- **8-Bit transparent latch**
- **3-State output buffers**
- **Common Latch Enable input with hysteresis**
- **Common 3-state Output Enable control**
- **Independent latch and 3-state buffer operation**
- **See "363" for MOS compatible output version**

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V_{CC}=5V ± 5%; T_A=0°C to +70°C	MILITARY RANGES V_{CC}=5V ± 10%; T_A=−55°C to +125°C
Plastic DIP	N74LS373N	
Ceramic DIP	N74LS373F	S54LS373F
Flatpak		

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE[a]

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
E	Latch Enable (active HIGH) input	I_{IH} (μA) I_{IL} (mA)			20 −0.4
D_0-D_7	Parallel Data inputs	I_{IH} (μA) I_{IL} (mA)			20 −0.4
$\overline{OE}$	Output Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)			20 −0.4
Q_0-Q_7	3-State outputs	I_{OH} (mA) I_{OL} (mA)			−1/−2.6(a) 12/24(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "373" is Octal Transparent Latch coupled to eight 3-state output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition. The enable gate has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

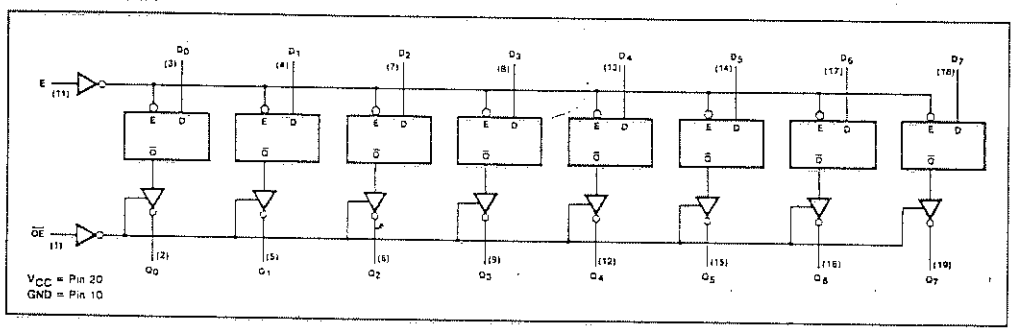
The 3-state output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-state buffers independent of the latch operation. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the high impedance "off" state, which means they will neither drive nor load the bus.

MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS				OUTPUTS
	$\overline{OE}$	E	D_n	INTERNAL REGISTER	Q_0-Q_7
Enable & read register	L L	H H	L H	L H	L H
Latch & read register	L L	L L	l h	L H	L H
Latch register & disable outputs	H H	L L	l h	L H	(Z) (Z)

H = HIGH voltage level
h = HIGH voltage one setup time prior to the HIGH-to-LOW enable transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the HIGH-to-LOW enable transition
(Z) = High impedance "off" state

LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE[b]

PARAMETER		TEST CONDITIONS		54/74 Min	54/74 Max	54S/74S Min	54S/74S Max	54LS/74LS Min	54LS/74LS Max	UNIT
V_{OL}	Output LOW voltage	V_{CC} Min	I_{OL} = 12mA						0.4	V
		$V_{\overline{OE}} = V_{IL}$	I_{OL} = 24mA						0.5(c)	V
V_{OH}	Output HIGH voltage	V_{CC} = Min, $V_{\overline{OE}} = V_{IL}$ I_{OH} = See Fan Out Table						2.4		V
I_{OS}	Output short circuit current	V_{CC} = Max, V_{OUT} = 0V						−30	−100	mA
I_{CC}	Supply current	V_{CC} = Max	Mil						44	mA
			Com						40	mA

NOTES

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

c. This parameter for Commercial Range only.

1-OF-8 DECODER/DEMULTIPLEXER 54/74 SERIES "138"

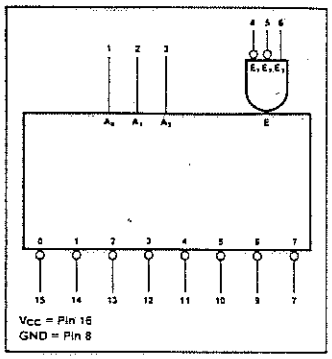
DESCRIPTION

The "138" is a HIGH speed 1-of-8 Decoder/Demultiplexer. The "138" is ideal for HIGH speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using only three "138" devices; or to a 1-of-32 decoder using four "138" devices and one inverter.

FEATURES

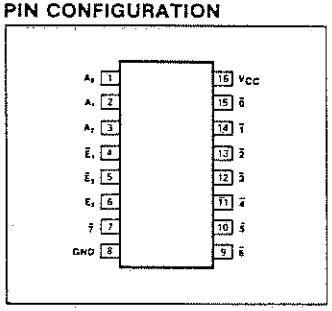
- **Demultiplexing capability**
- **Multiple input enable for easy expansion**
- **Ideal for memory chip select decoding**
- **Direct replacement for Intel 3205**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to 70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = -55°C to +125°C
Plastic DIP	N74S138N • N74LS138N	
Ceramic DIP	N74S138F • N74LS138F	S54S138F • S54LS138F
Flatpak		S54S138W • S54LS138W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE [a]

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
A_0-A_2	Address inputs	I_{IH} (μA) I_{IL} (mA)		50 -2.0	20 -0.36
$\overline{E}_1$, $\overline{E}_2$	Enable (Active LOW) inputs	I_{IH} (μA) I_{IL} (mA)		50 -2.0	20 -0.36
E_3	Enable (Active HIGH) input	I_{IH} (μA) I_{IL} (mA)		50 -2.0	20 -0.36
$\overline{0}$-$\overline{7}$	Decoder ouputs	I_{OH} (μA) I_{OL} (mA)		-1000 20	-400 4/8 [a]

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "138" decoder accepts three binary weighted inputs (A_0,A_1,A_2) and when enabled provides eight mutually exclusive active LOW outputs ($\overline{0}$-$\overline{7}$). The device features three Enable inputs: two active LOW ($\overline{E}_1$,$\overline{E}_2$) and one active HIGH (E_3). Every output will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple Enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four "138's" and one inverter.

The device can be used as an eight output demultiplexer by using one of the active LOW Enable inputs as the data input and the remaining Enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active HIGH or active LOW state.

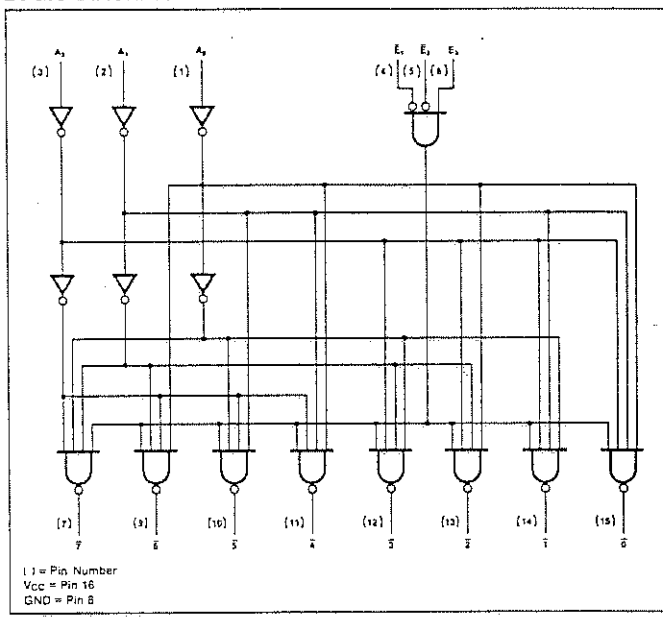
TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

NOTES

H = HIGH voltage level
L = LOW voltage level
X = Don't care

LOGIC DIAGRAM



( ) = Pin Number
VCC = Pin 16
GND = Pin 8

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE [b]

PARAMETER		TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
			Min	Max	Min	Max	Min	Max	
I_{CC}	Supply current	V_{CC} = Max				74		10	mA

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

8051 Note: Standby current is Icc when CS=H

	I_{OL}	I_{OH}	I_{IL}	I_{IH}	I_I	Icc
8051 P123	1.6m	80µ	500µ	10µ	10µ	160mA
* 8051 P0 ALE PSEN	3.2m	400µ	10µ	10µ	10µ	—
* 51165	2.1m	1m	1µ	1µ	1µ	60m
* 2764A	2.1m	400µ	10µ	10µ	10µ	75m
74LS138	DEC_OUT 8m	DEC_OUT 400µ	0.36m	20µ	—	10m
74LS373	24m	2.6m	0.1m	20µ	—	40m

ADDRESS AN. = 10
DATA AN. = 10
OTHER LINES = 5
SUPPLY CUR. = 5
30
Recomm = 5
35

Address bus loading:

- A0-A7: Driver 74LS373
  - LOAD RAM & ROM
  - $\Sigma I_{IL} = 4\mu + 10\mu = 14\mu A < 24mA$
  - $\Sigma I_{IH} = 4\mu A + 10\mu = 14\mu A < 2.6mA$
  - } No problem
- A8-A15:
  - Driver P2 µC
  - LOAD RAM, ROM → A8-A10
  - 138 → A13-A14
  - 138 + ROM → A11, A12, A15 ← Worst
  - $\Sigma I_{IL} = 360\mu + 10\mu = 370\mu A < 1.6m$
  - $\Sigma I_{IH} = 20\mu + 10\mu = 30\mu A < 80\mu A$
  - } No Problem

Data bus loading:

Weakest driver in low: Memory $I_{OL} = 2.1m$
Weakest driver in high: µP $I_{OH} = 400m$

Low state analysis:

Ram drives:	Loads	
	3 RAM INACT.	3µA
	1 ROM INAC	10µA
	1 µC ACT.	10µA
	1 373 In	400µA
		423µA

423µA < 2.1mA } no problem

High state analysis:

µP drives:	LOADS	
ALE & PSEN → Single load	4 RAM	4µA
	1 ROM	10µA
RD & WR lines	1 373	20µA
P3		34µA < 400µA } No problem

$\Sigma I_{IH} = \Sigma I_{IL} = 14\mu A < 80\mu A$ No problem

$\Sigma I_{cc} = {}^{8051}160 + 4*{}^{6116}60 + {}^{2764}75 + {}^{74}10 + {}^{74}40 = 525mA$

Rec. Psuk supply = 750mA @ 5V (minimum)

Timing Analysis:

O_{sc}. freq = 12 MHz $T_{CLCL} = \frac{1}{12} \times 10^{-6}$

Program Read $T_{acc} = T_{PLPH} + T_{LLPL} + T_{AVLL}$

$T_{acc_{MP}} = 215 + 58 + 43 = 316\,nS$

Data Read $T_{acc} = T_{RLRH} + T_{LLWL} + T_{AVLL}$

$T_{acc_{MP}} = 400 + 200 + 43 = 643\,nS$

Data Write $T_{acc} = T_{WLWH} + T_{LLWL} + T_{AVLL} =$

$T_{acc} = 400 + 200 + 43 = 643\,nS$

Z-80A-CTC

ROM Access time

Read = 250 nS

RAM Access time 5116G-12

Read = 120 nS

Write = 105 nS

$T_{chip} < T_{MC}$ } No problem wi read wi write