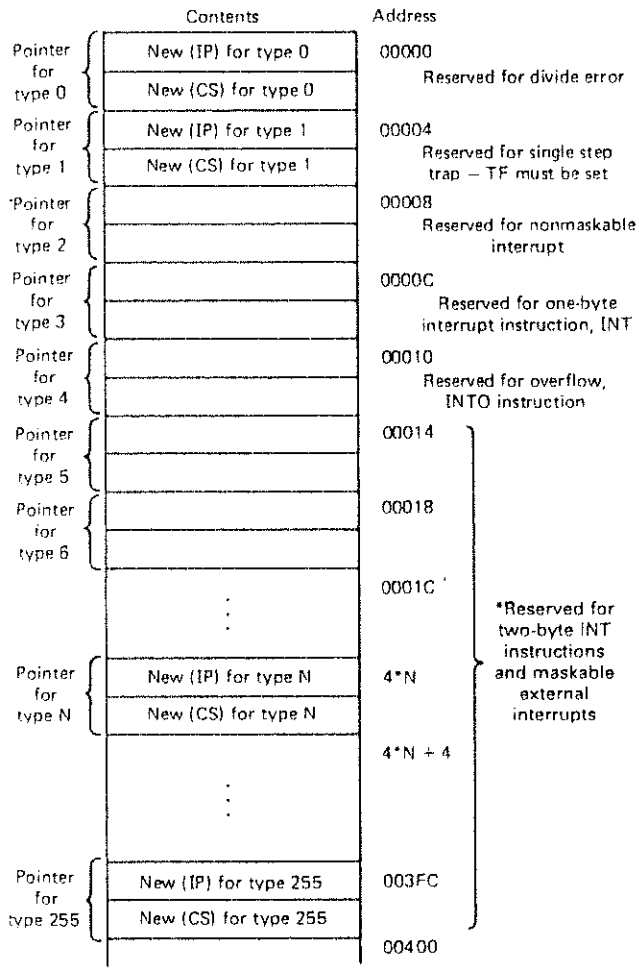


*For the two-byte INT instruction the type is specified by the second byte and for an external interrupt the type is sent to the CPU over 8 of the data lines.

Figure 4-26 Layout of interrupt pointers.

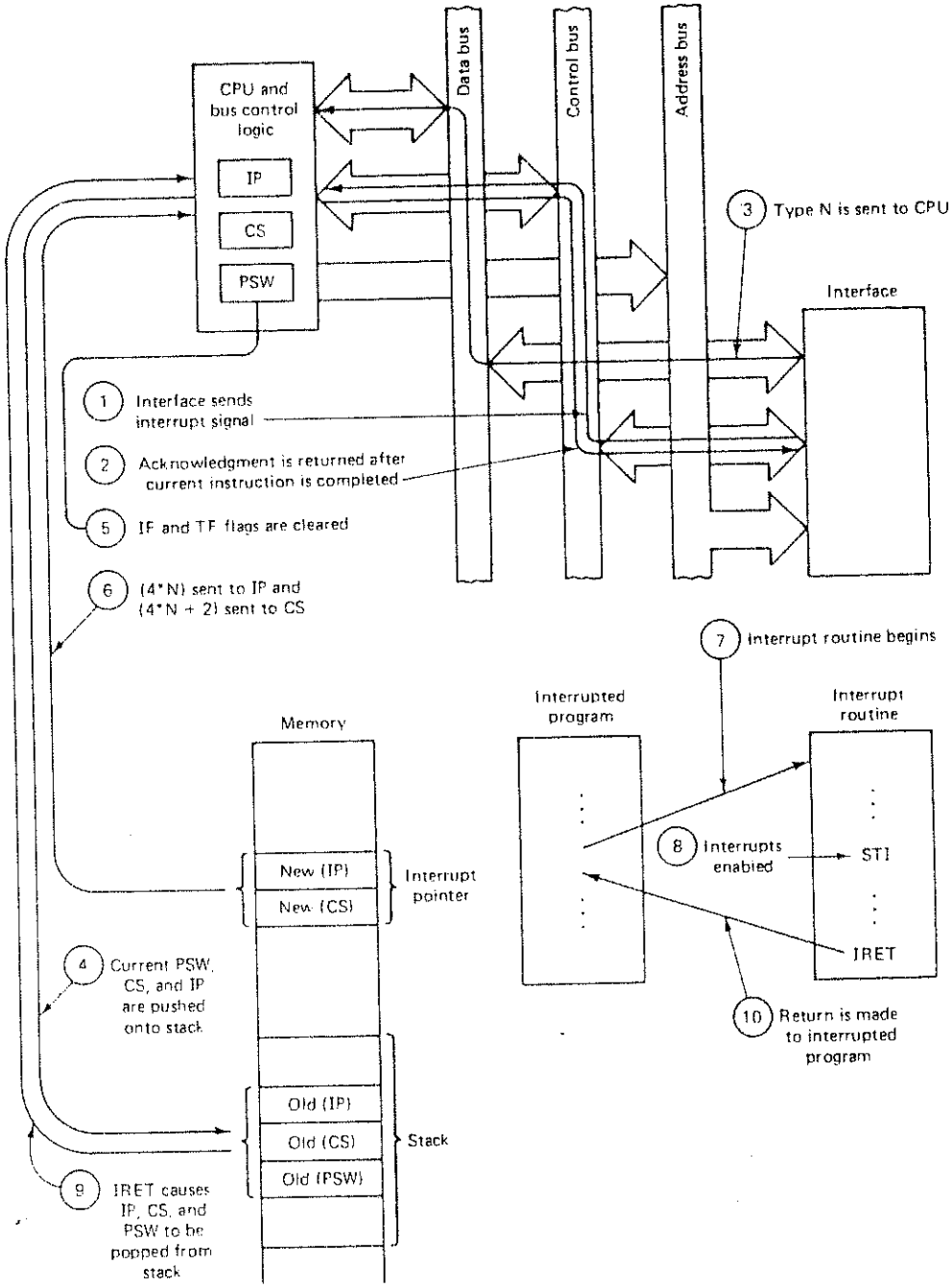
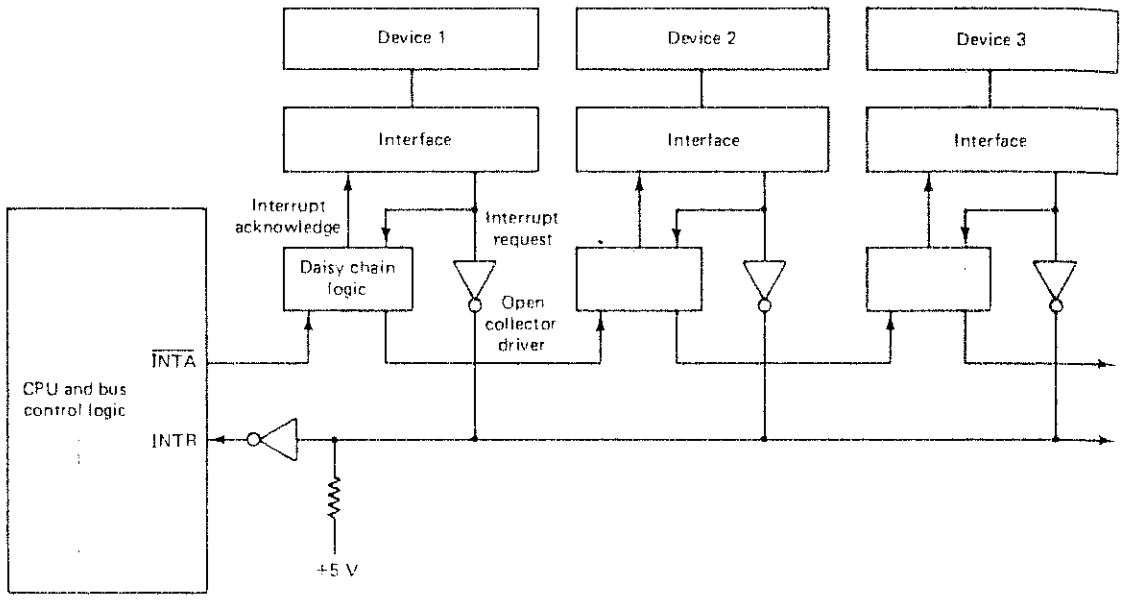
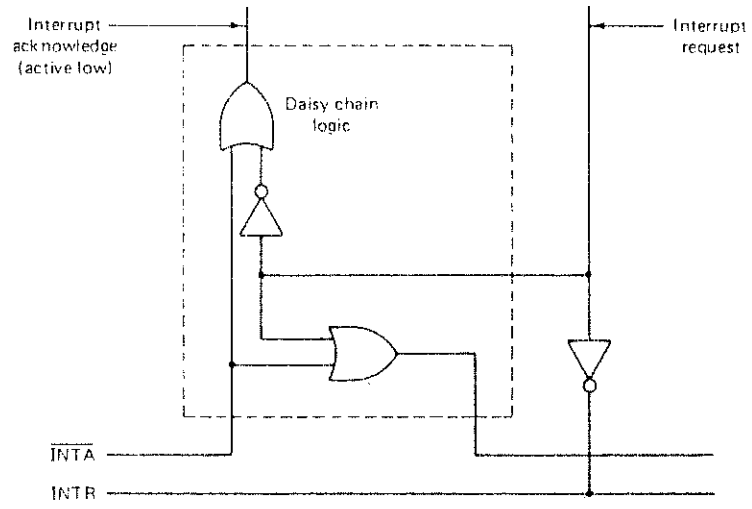


Figure 6-9 Sequence of events during a maskable interrupt and subsequent return.



(a) Daisy chain



(b) Logic

Figure 6-14 Daisy chain arrangement.

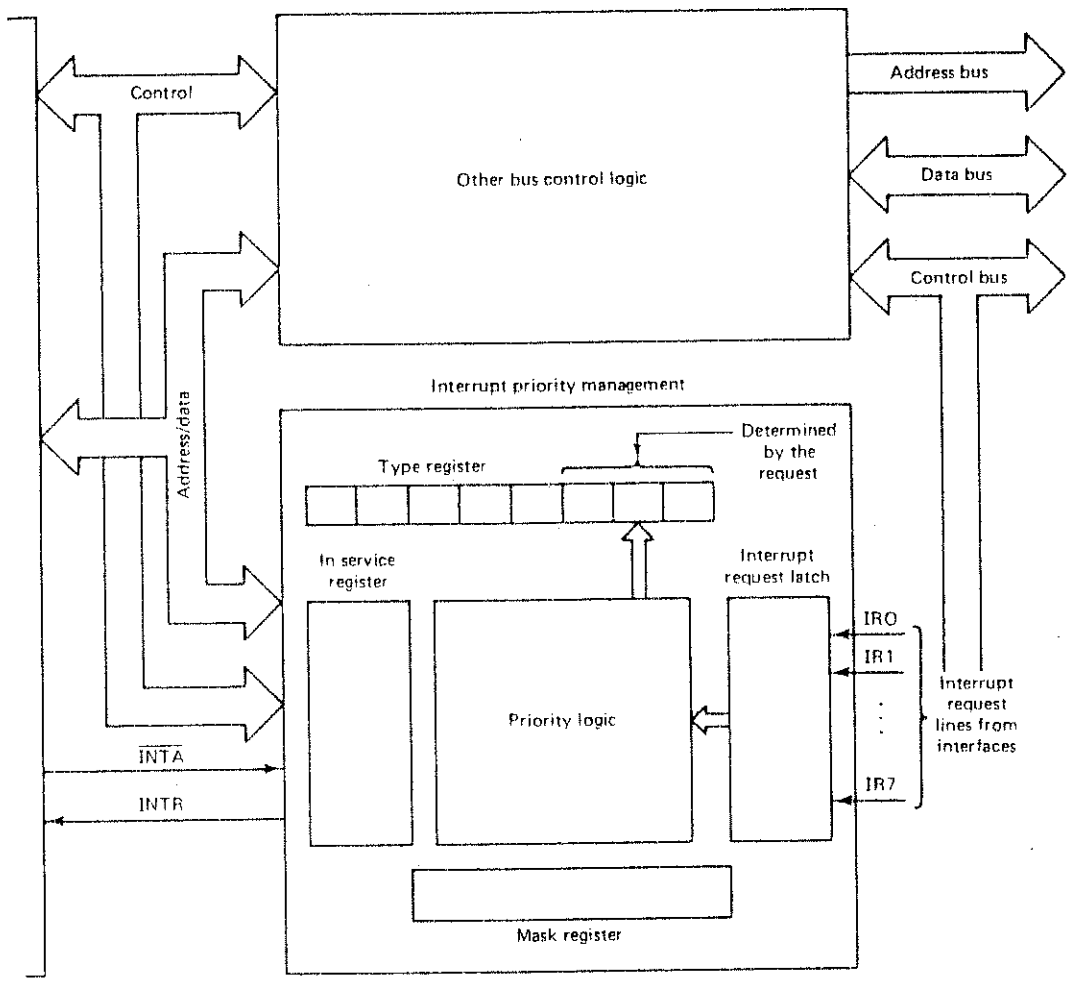
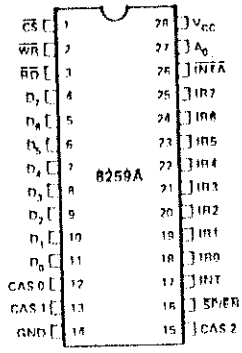


Figure 6-15 Representative interrupt priority management design.

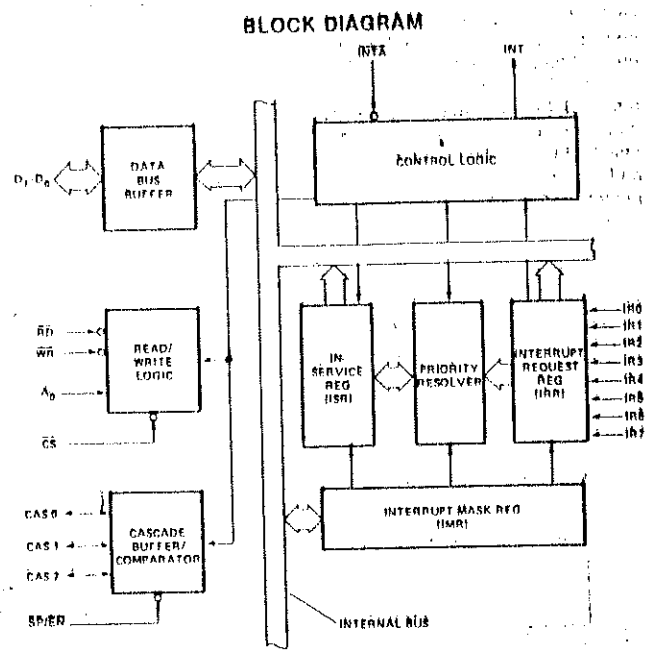
PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (BI-DIRECTIONAL)
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A_0	COMMAND SELECT ADDRESS
$\overline{CS}$	CHIP SELECT
CAS1-CAS0	CASCADE LINES
$\overline{SP/EN}$	SLAVE PROGRAM/ENABLE BUFFER
INT	INTERRUPT OUTPUT
$\overline{INTA}$	INTERRUPT ACKNOWLEDGE INPUT
IR0-IR7	INTERRUPT REQUEST INPUTS

BLOCK DIAGRAM



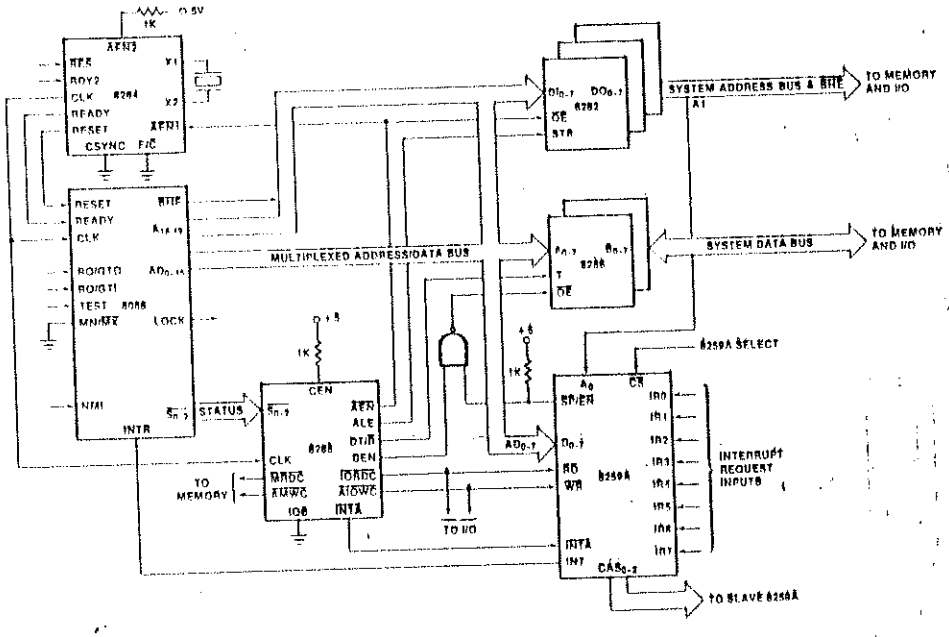
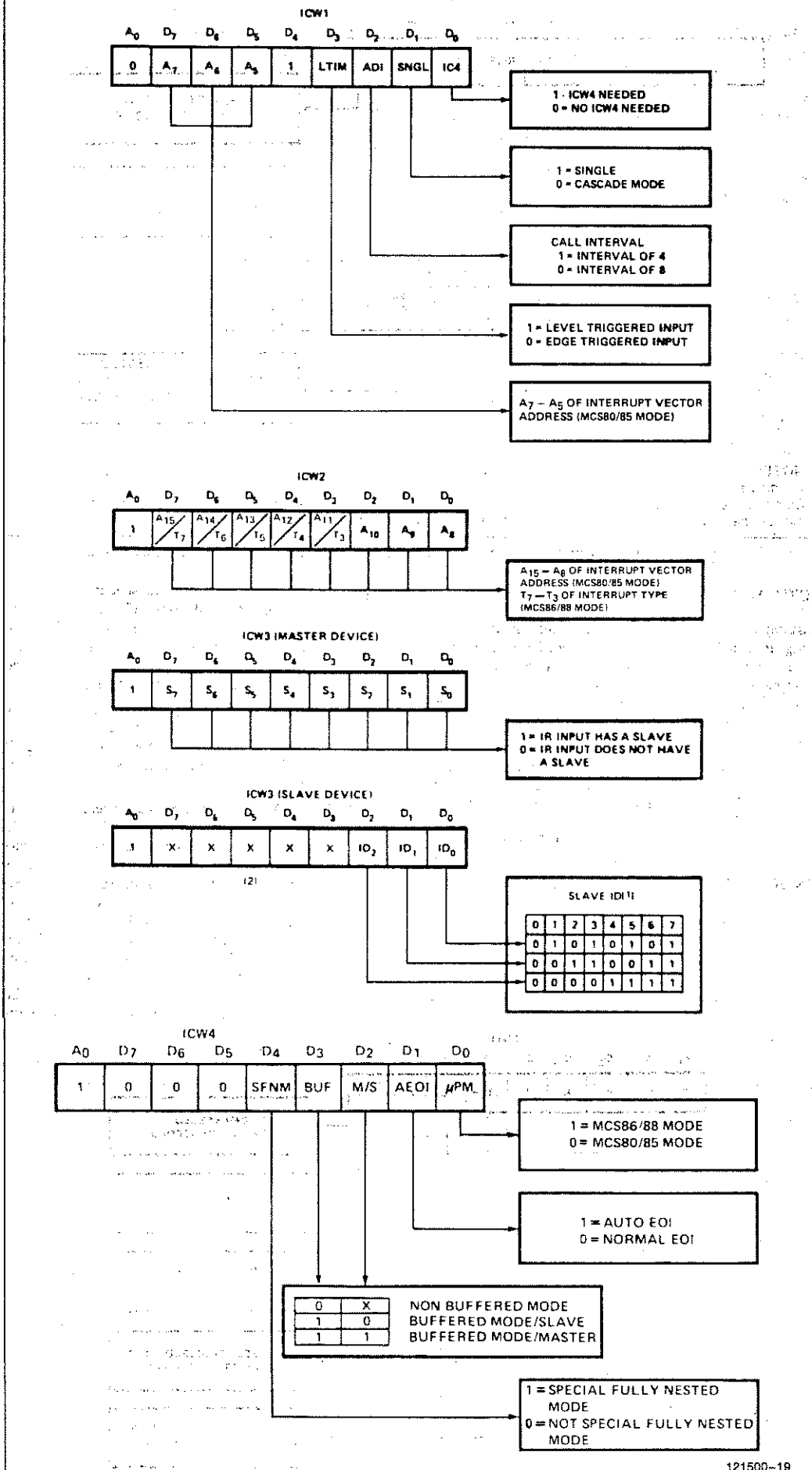
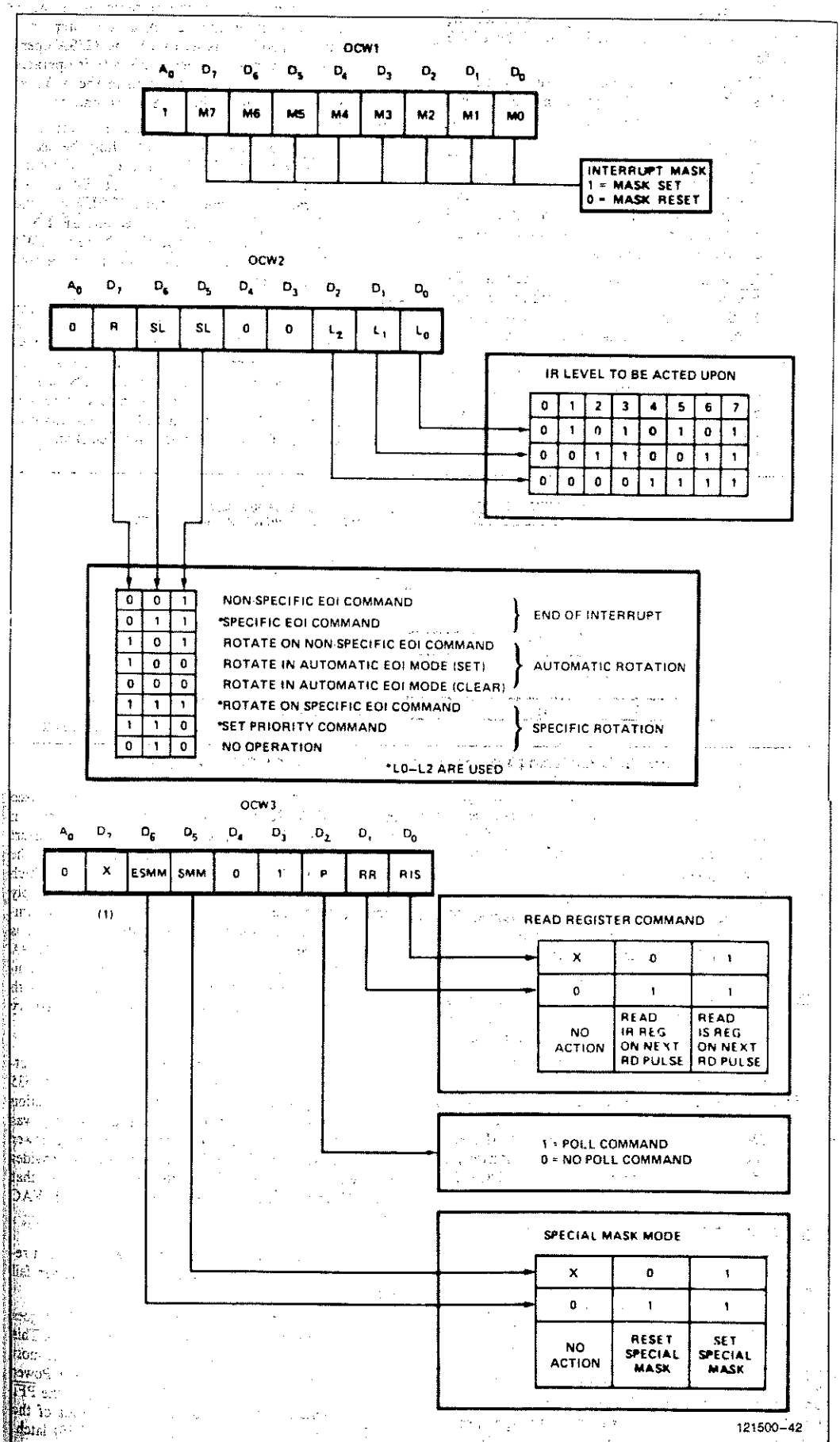


Figure 4. MSC-86 8259A Basic Configuration Example (8086 in Max. Mode)



NOTE:
X indicates "Don't Care".
Some of the terminology used may differ slightly from existing 8259A data sheets. This is done to better clarify and explain the programming of the 8259A, the operational results remain the same.

Figure 21. Initialization Command Words (ICWs) Programming Format (Continued)



NOTE:
X indicates "Don't Care".
Some of the terminology used may differ slightly from existing 8259A data sheets. This is done to better clarify and explain the programming of the 8259A, the operational results remain the same.

Figure 23. Operational Command Words (OCWs) Programming Format (Continued)

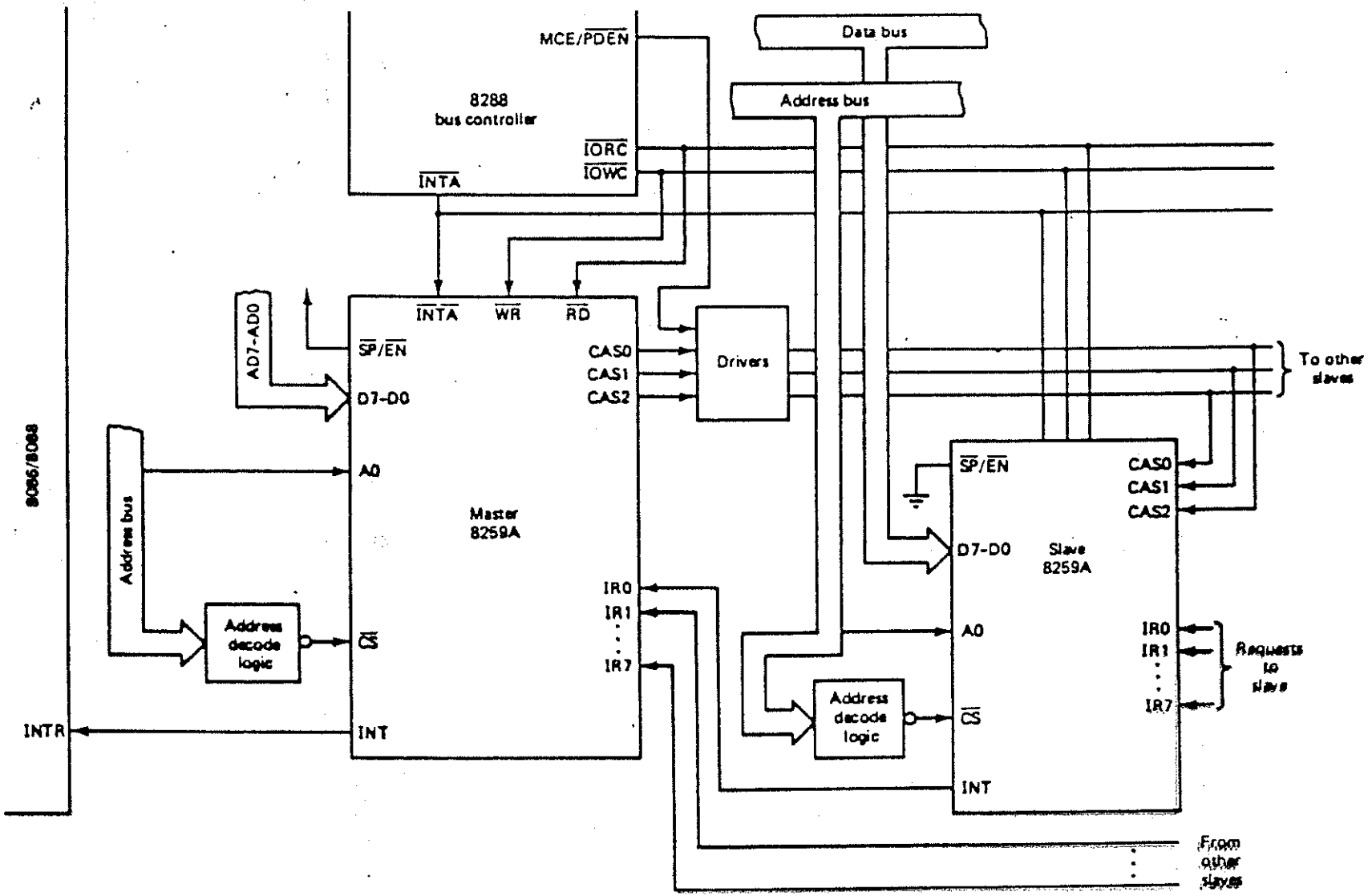


Figure 8-19 Multiple 8259A-based interrupt system.