

	Contents	Address
Pointer for type 0	New (IP) for type 0	00000
	New (CS) for type 0	Reserved for divide error
Pointer for type 1	New (IP) for type 1	00004
	New (CS) for type 1	Reserved for single step trap — TF must be set
Pointer for type 2		00008
		Reserved for nonmaskable interrupt
Pointer for type 3		0000C
		Reserved for one-byte interrupt instruction, INT
Pointer for type 4		00010
		Reserved for overflow, INTO instruction
Pointer for type 5		00014
		} *Reserved for two-byte INT instructions and maskable external interrupts
Pointer for type 6		00018
		0001C
Pointer for type N	New (IP) for type N	4*N
	New (CS) for type N	4*N + 4
Pointer for type 255	New (IP) for type 255	003FC
	New (CS) for type 255	00400

\*For the two-byte INT instruction the type is specified by the second byte and for an external interrupt the type is sent to the CPU over 8 of the data lines.

Figure 4-26 Layout of interrupt pointers.

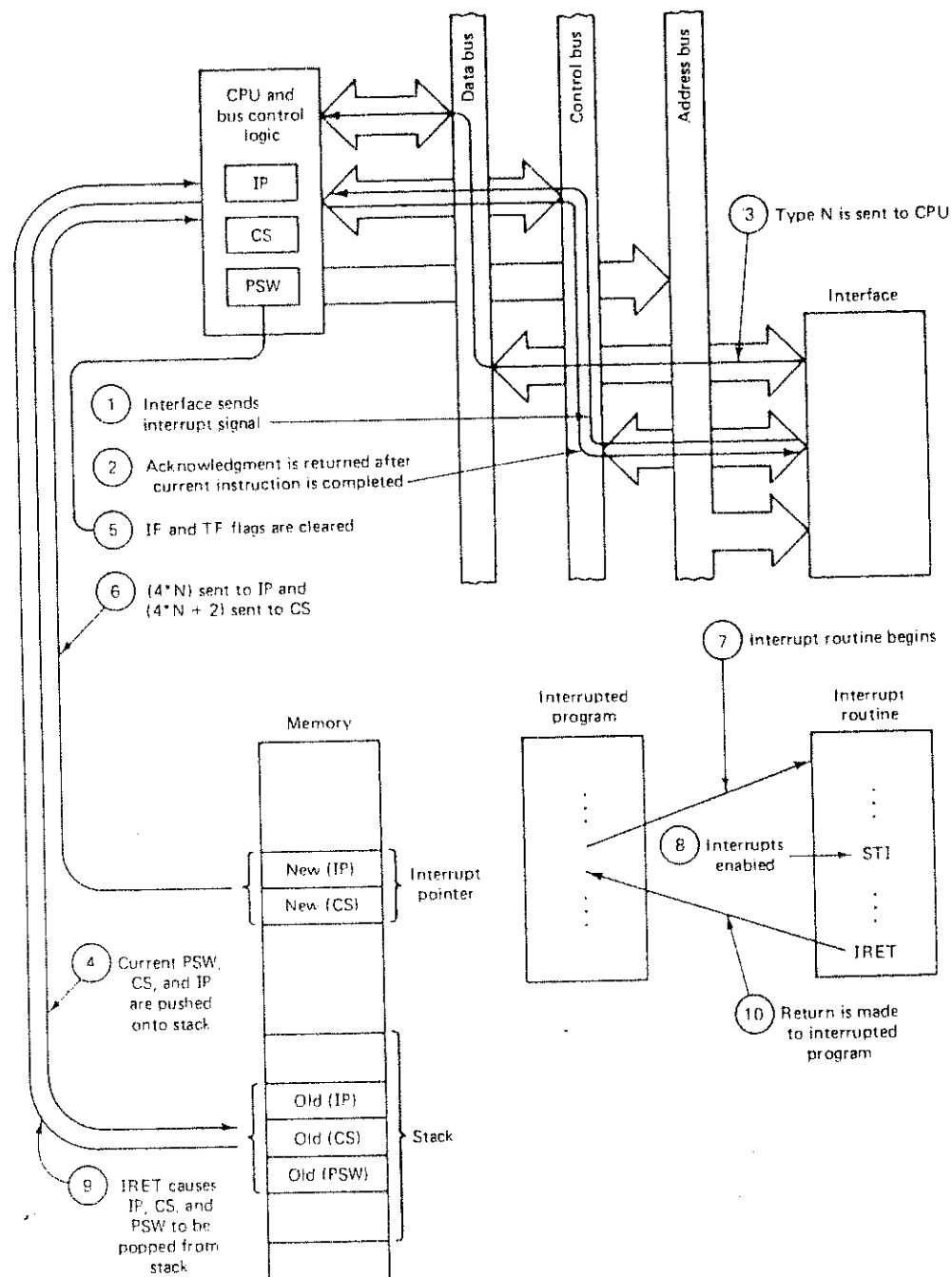
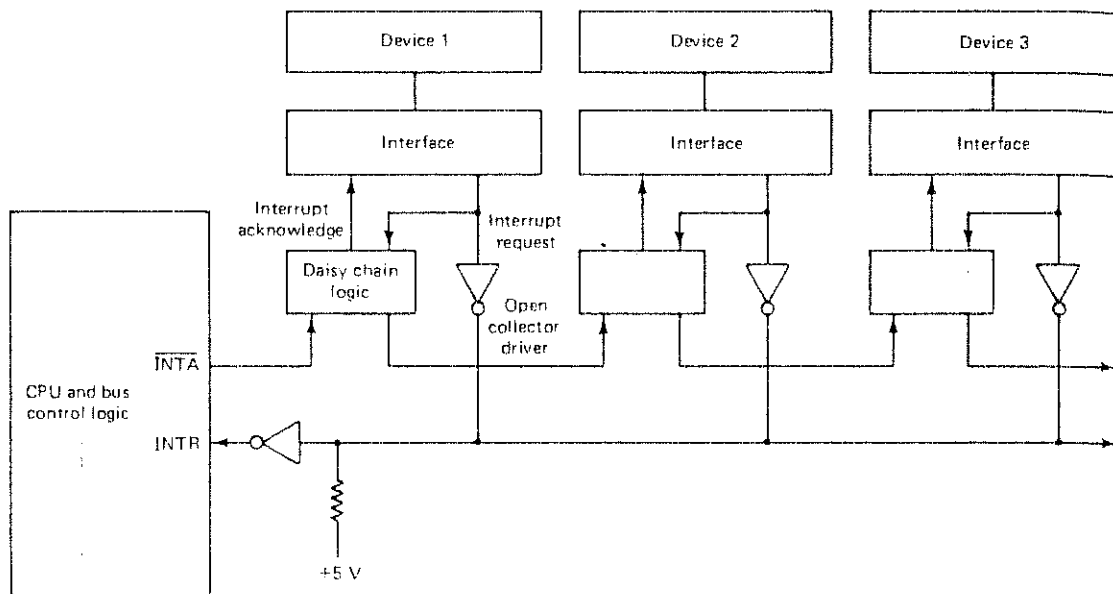
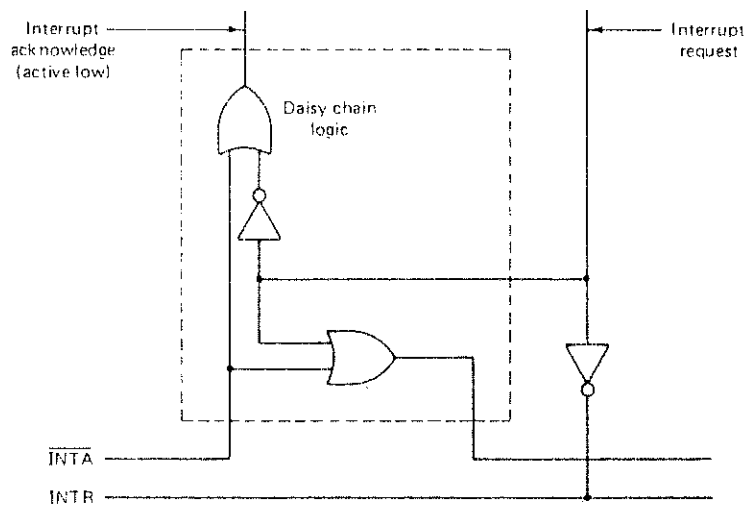


Figure 6-9 Sequence of events during a maskable interrupt and subsequent return.



(a) Daisy chain



(b) Logic

Figure 6-14 Daisy chain arrangement.

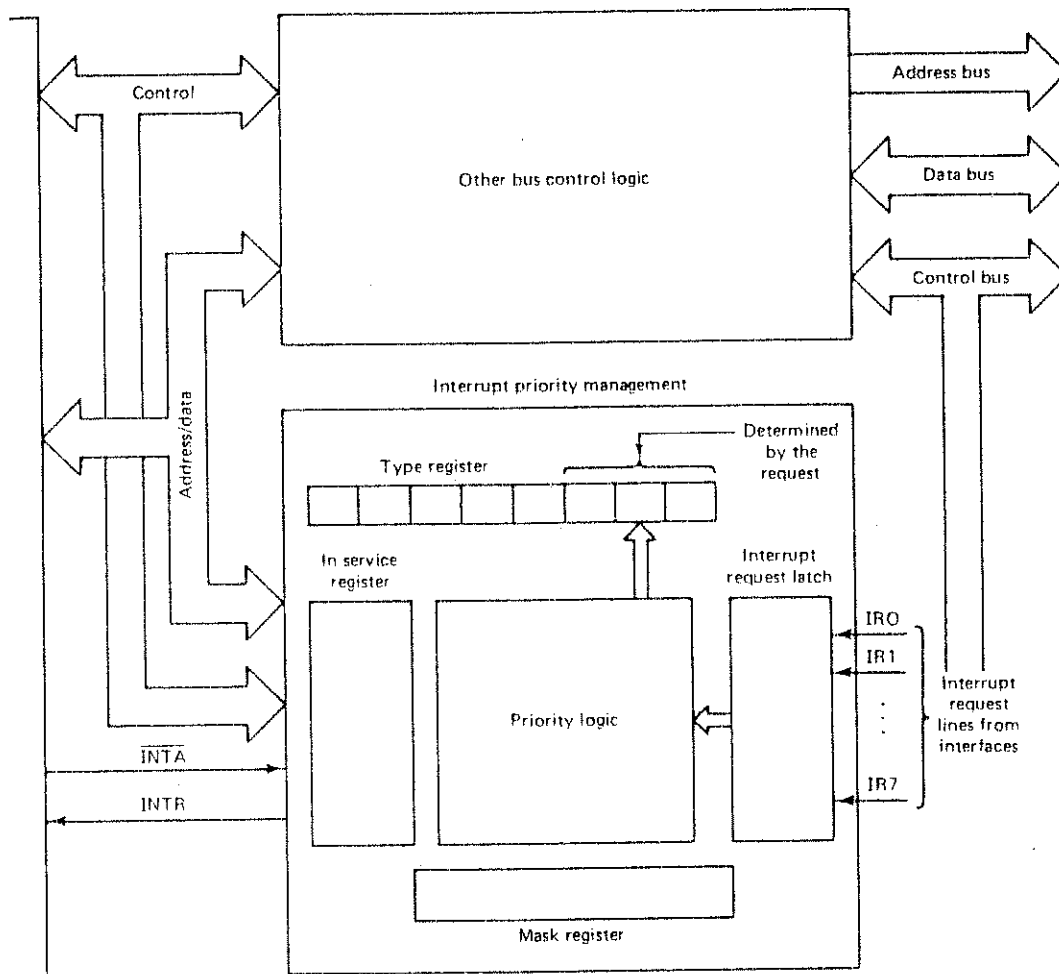


Figure 6-15 Representative interrupt priority management design.

$\overline{CS}$	1	28	$V_{CC}$
$\overline{WR}$	2	27	$A_0$
$\overline{RD}$	3	26	$\overline{INTA}$
$D_7$	4	25	$\overline{IR7}$
$D_6$	5	24	$\overline{IR6}$
$D_5$	6	23	$\overline{IR5}$
$D_4$	7	22	$\overline{IR4}$
$D_3$	8	21	$\overline{IR3}$
$D_2$	9	20	$\overline{IR2}$
$D_1$	10	19	$\overline{IR1}$
$D_0$	11	18	$\overline{IR0}$
CAS 0	12	17	$\overline{IR7}$
CAS 1	13	16	$\overline{SPEN}$
$\overline{RNB}$	14	15	CAS 2

D <sub>7</sub> D <sub>0</sub>	DATA BUS (BIDIRECTIONAL)
RD	READ INPUT
WR	WRITE INPUT
A <sub>9</sub>	COMMAND SELECT ADDRESS
CS	CHIP SELECT
CAS1 CAS0	CASCADE LINES
SPEN	SLAVE PROGRAMMABLE BUFFER
INT	INTERRUPT OUTPUT
INTA	INTERRUPT ACKNOWLEDGE INPUT
IRQ-IR7	INTERRUPT REQUEST INPUTS

The block diagram illustrates the internal architecture of the 68000 microprocessor, centered around a horizontal **INTERNAL BUS**. Key components and their connections are as follows:

- Control Logic:** Receives **NVA** and **INT** signals. It is connected to the internal bus and the **DATA BUS BUFFER**.
- DATA BUS BUFFER:** Manages data flow between the internal bus and external data buses **D<sub>1</sub>** and **D<sub>0</sub>**.
- READ/WRITE LOGIC:** Receives control signals **R<sub>0</sub>**, **W<sub>0</sub>**, and **A<sub>0</sub>**. It is connected to the internal bus and the **CASCADE BUFFER/COMPARATOR**.
- CASCADE BUFFER/COMPARATOR:** Receives external signals **CAS0**, **CAS1**, and **CAS2**. It is connected to the internal bus and the **INTERRUPT MASK REG (IMR)**.
- IN-SERVICE REG (ISR):** Connected to the internal bus and the **PRIORITY RESOLVER**.
- PRIORITY RESOLVER:** Receives signals from the **ISR** and the **INTERRUPT REQUEST REG (IRR)**.
- INTERRUPT REQUEST REG (IRR):** Receives external interrupt signals **IR0** through **IR7**. It is connected to the internal bus and the **PRIORITY RESOLVER**.
- INTERRUPT MASK REG (IMR):** Receives signals from the **CASCADE BUFFER/COMPARATOR** and the **PRIORITY RESOLVER**. It is connected to the internal bus.

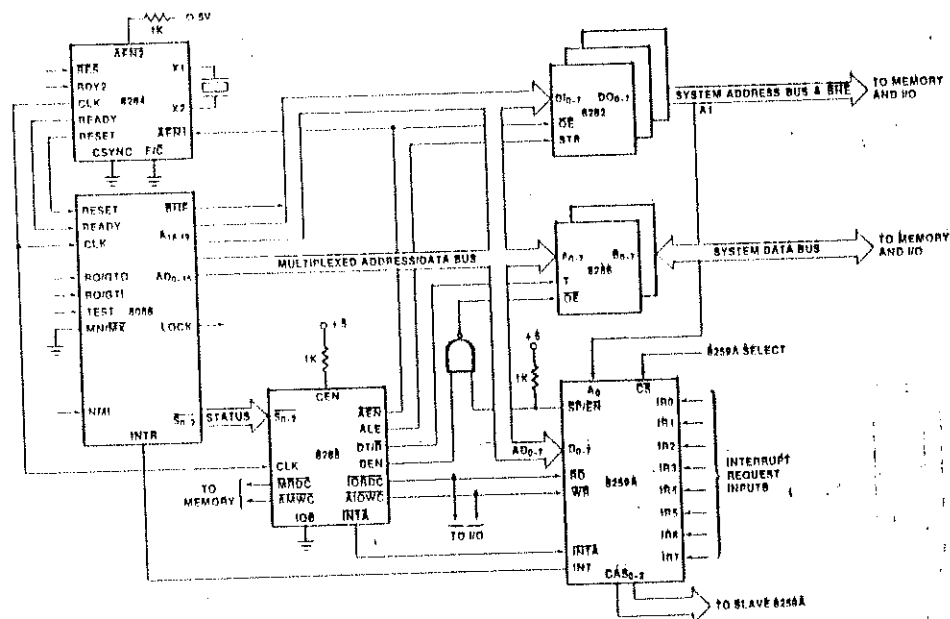
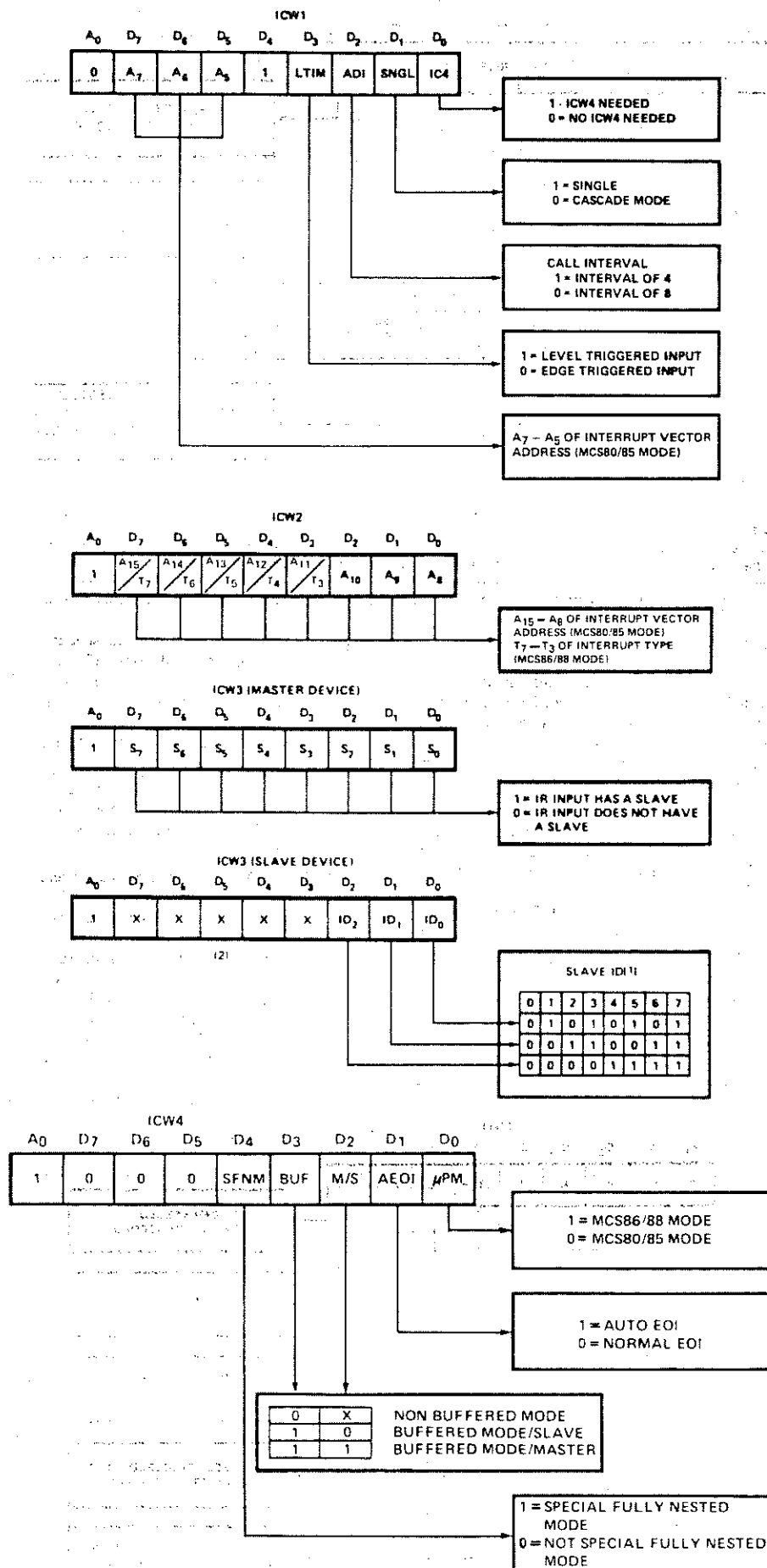


Figure 4. MSC-86: 8259A Basic Configuration Example (8086 in Max. Model)



121500-19

**NOTE:**

X indicates "Don't Care".

Some of the terminology used may differ slightly from existing 8259A data sheets. This is done to better clarify and explain the programming of the 8259A, the operational results remain the same.

**Figure 21. Initialization Command Words (ICWs) Programming Format (Continued)**

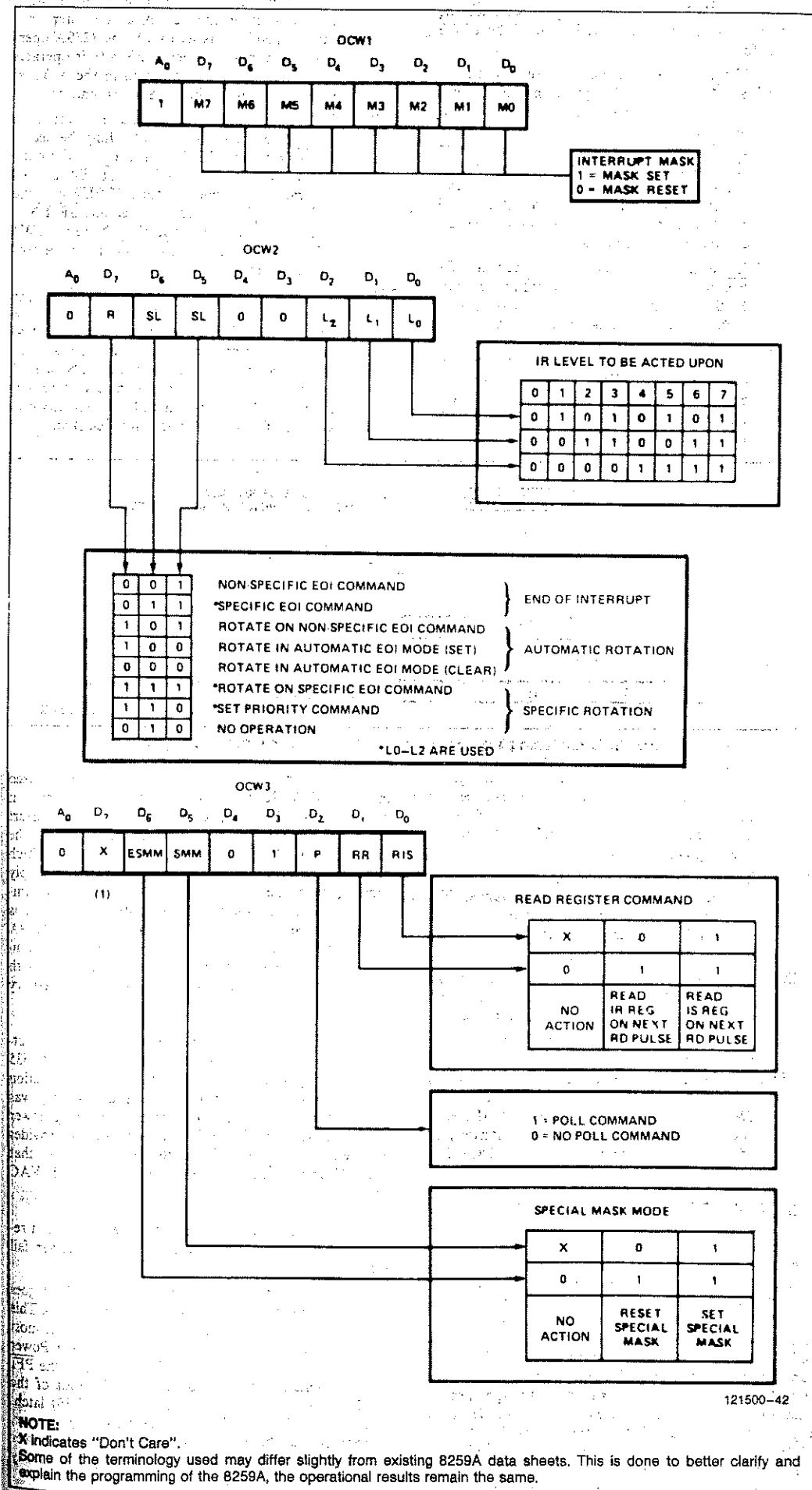


Figure 23. Operational Command Words (OCWs) Programming Format (Continued)

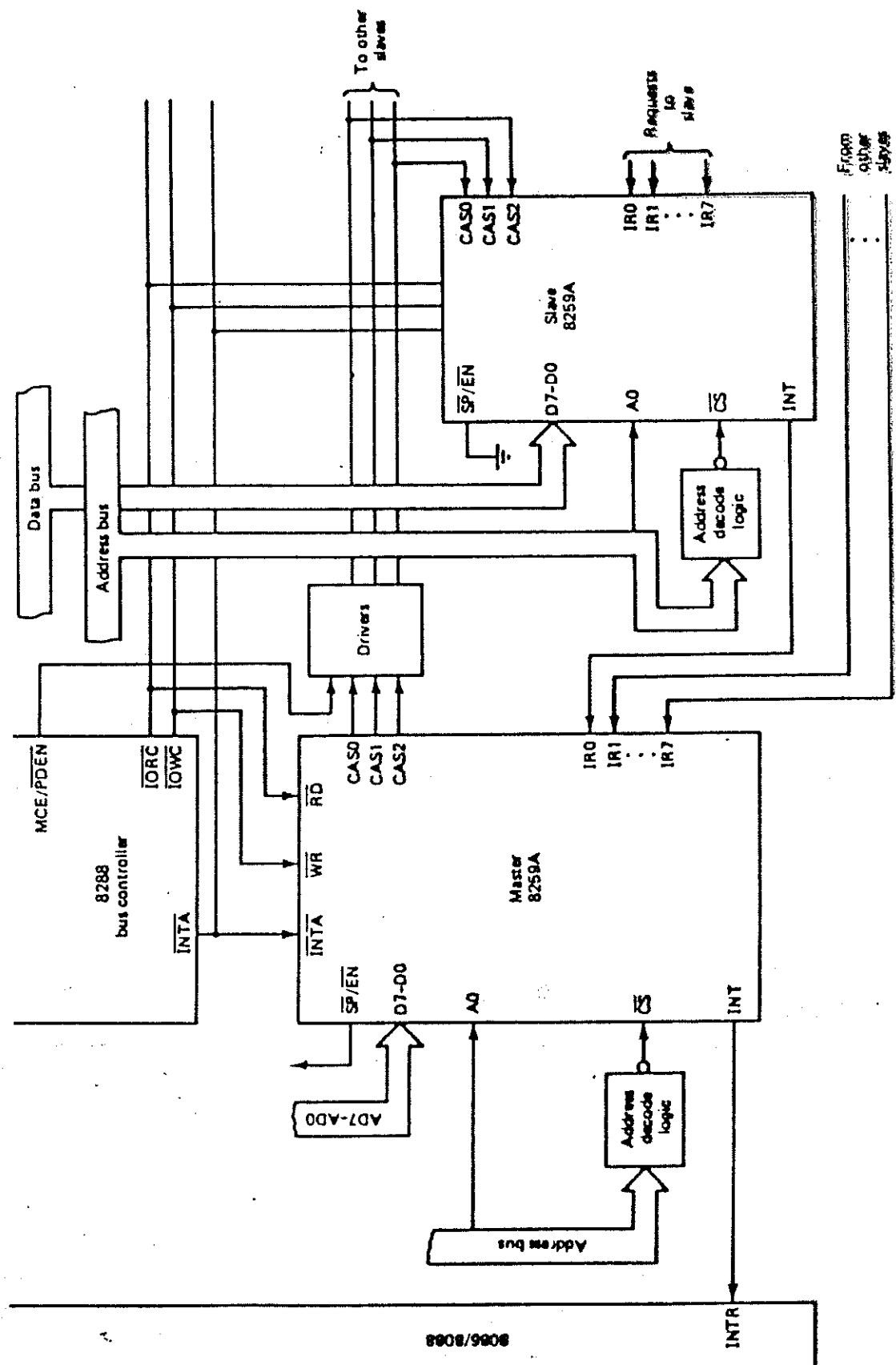


Figure 8-19 Multiple 8259A-based interrupt system.