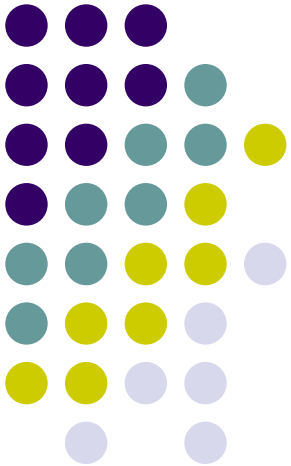
Chapter 6: EMBEDDED HARDWARE FUNDAMENTALS



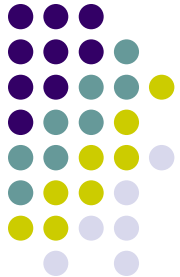
Manuel Jiménez

EMBEDDED SYSTEMS:

Theory and Applications Using the MSP430

UPRM - Fall 2008

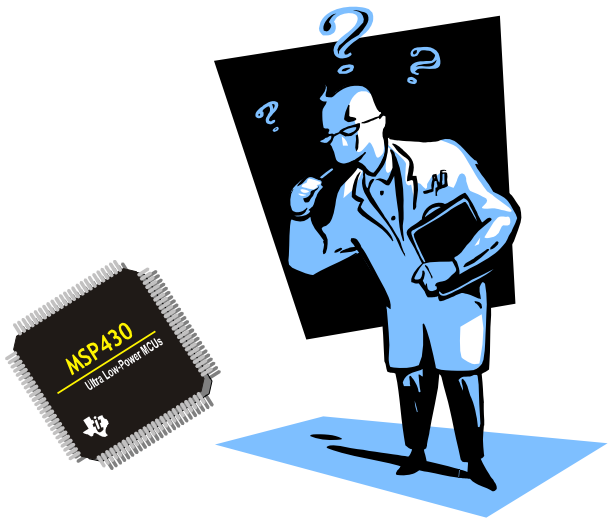
Chapter Outline



- Practical MCU Considerations
  - ESD Handling Precautions
  - Understanding MCU Data Sheets
- MCU and System Power Sources
  - Selecting a Power source
- Clock Oscillators
  - Choosing a Clock Source
- Power-on Reset
  - Reset Hardware
  - Initialization Software
- Memory Map: Programs & Data
  - Partitioning Programs and Data
  - Reserved Locations
- Interfacing Considerations
  - Bus Loading Considerations
  - Electrical Compatibility Issues
  - Noise and Signal Integrity Issues
- Basic Interface: The MSP430F2012 Case
  - Power Supply Requirements
  - Base Clock Module
  - Limits in Low-power Modes
  - System Reset and Initialization
  - Brownout Reset (BOR)
  - Software Initialization
  - Electrical Considerations
- Planning the Hardware Design
  - Defining the System Requirements
  - Selecting the MCU
  - Partitioning the Hardware and Defining the Parts
- A Practical Exercise
- Summary

Practical MCU Considerations

- What to do once you got a shiny, brand-new MCU chip?
  - Handling Precautions
    - ESD = ElectroStatic Discharge
  - Understanding Data Sheets
    - Main Parameters
  - Basic Interface
    - Minimum Interconnections
  - Interfacing Considerations
    - Adding Peripherals
    - Loads and Signals

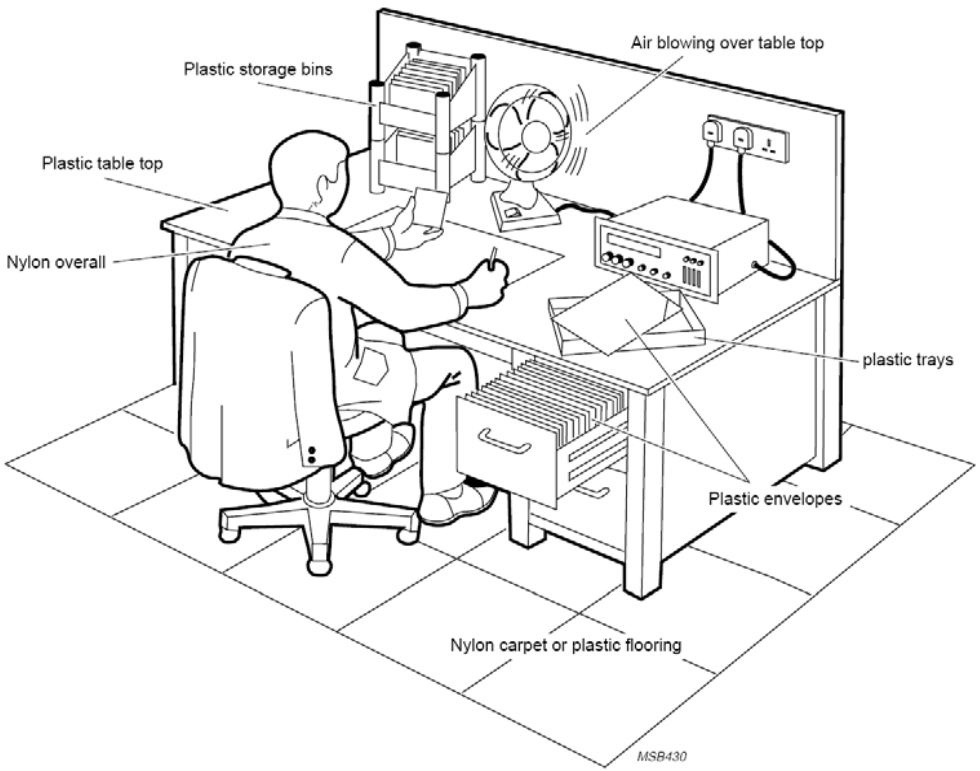


Electrostatic Discharge (ESD)

- Electrostatic Discharge (ESD)
  - Energy transfer between two objects at different electrostatic potential
  - Can occur by direct contact or via an ionized ambient discharge
- ES charges are generated by the separation or friction of two non-conducting surfaces
  - Caused by “Triboelectric Effect”
- Common ESD-generating Activities:
  - Walking on untreated vinyl floor: 250 - 12 KVolts
  - Rubbing plastic bag on workbench: 1.2 - 20 KVolts
  - Removing plexiglass plastic cover: 3.0 – 30 KVolts
- Lightning is a Natural Manifestation of ESD
  - About 1 GVolt “static” discharge

Factors Affecting ESD Events

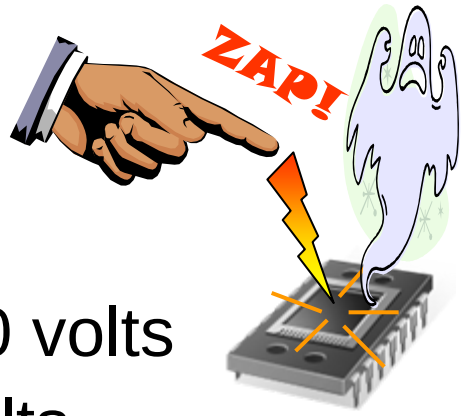
- Material Type
  - Insulators accumulate large amounts of static charge
- Contact Area
  - The larger the area, the larger the generated ES potential
- Speed of removal or brush
  - The faster the removal or brush event, the higher the accumulation
- Humidity
  - ES potential increases in dry environments



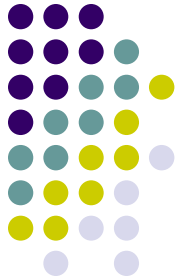
Working environment with potential ESD hazards
Courtesy of Philips Semiconductors

ESD and Electronics

- Electronic Components and ICs are Very Sensitive to Electrostatic Discharges (ESD)
- Voltages required to damage common electronic devices:
  - MOSFET 100 to 200 volts
  - JFET 140 to 10,000 volts
  - CMOS 250 to 2,000 volts
  - Schottky diodes & TTL 300 to 2,500 volts
  - Bipolar transistors 380 to 10,000 volts
  - SCR 680 to 1000 volts



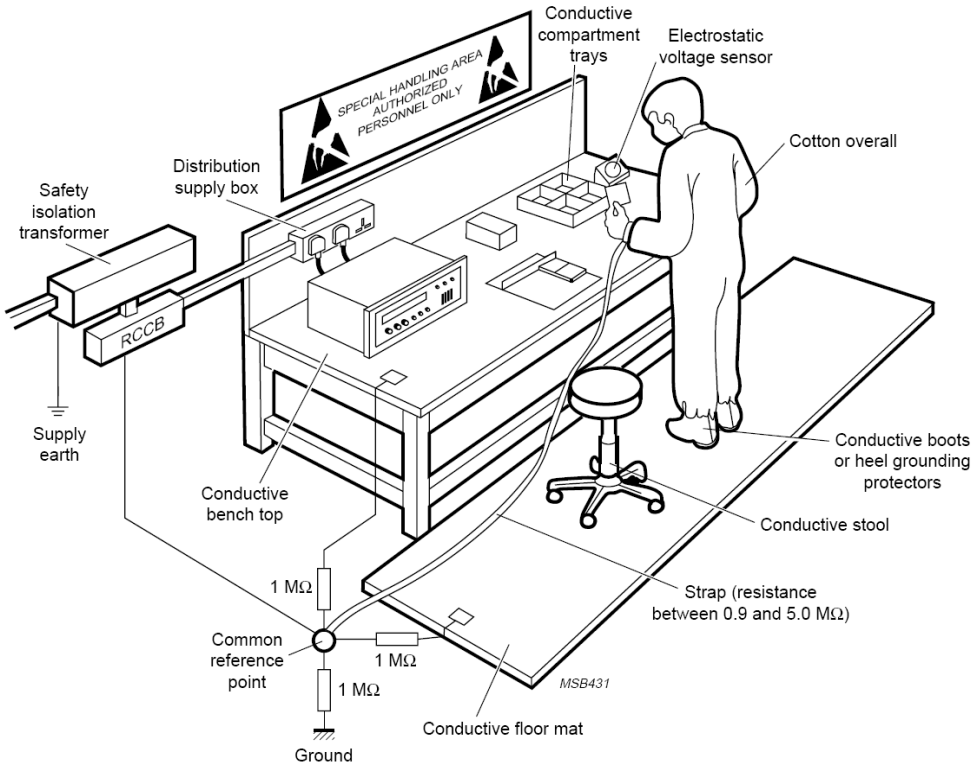
Types of ESD-induced Damage



- Catastrophic Failure
  - May cause a metal melt, junction breakdown, or oxide failure
  - Permanently damages the circuitry, causing the device to fail
  - Failures are usually identified before the device is shipped
  - Represent approximately 10% of ESD failures
- Latent Failure
  - Device is partially degraded after ESD event
    - Remains operable, but with compromised performance
  - Devices with latent defects may experience intermittent or premature failure
  - Detecting cause of failure may be difficult or hazardous
  - Latent failures increase warranty and replacement costs

ESD Handling Precautions

- Persons should be earthed via wrist strap-resistor or heel grounding
- Equipment cases should be grounded
- Relative humidity should be between 40% and 50%.
- Use ionizer to neutralize objects with static charges
- Keep static materials away from the workbench
  - No plastic envelopes
  - No plastic trays, etc.
- Keep stored components in anti-static containers
- Mount ESD sensitive devices last
- Handle completed PCBs with same care as components



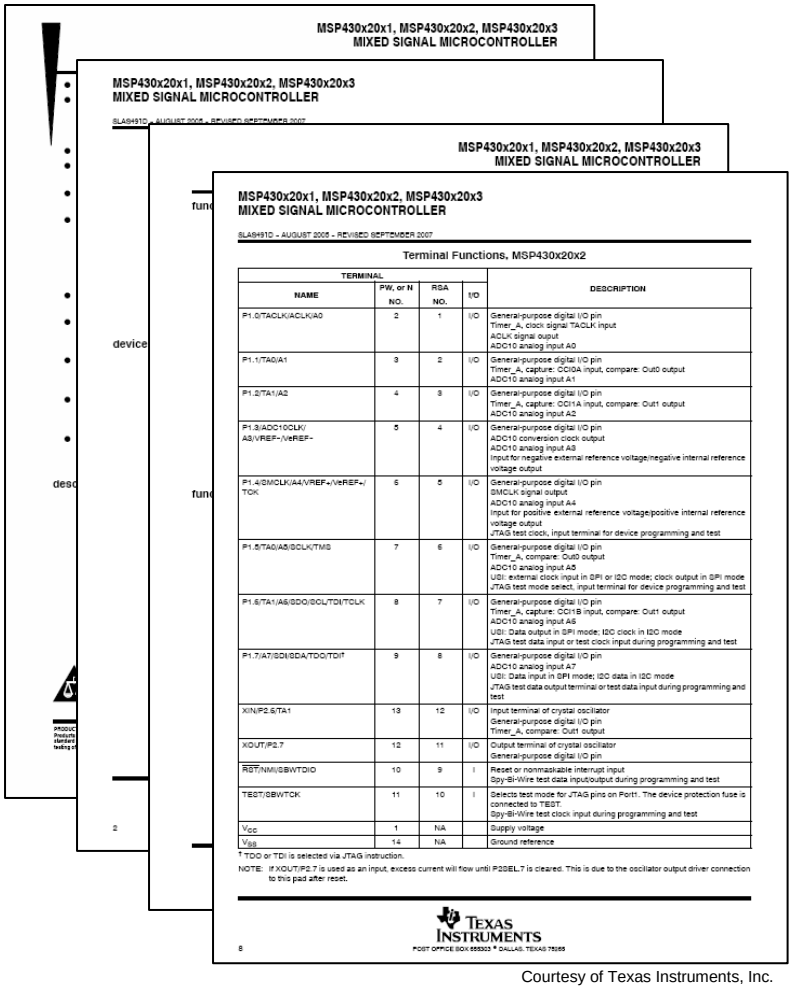
Working environment with proper ESD protection
Courtesy of Philips Semiconductors

Understanding Data Sheets

- Most Important Data
  - Summary Device Description
    - General device information: function and features
  - Absolute Maximum Ratings
    - Values that cause irreversible damage to the part
  - Recommended Operating Conditions
    - Practical use ranges
  - Electrical or DC Characteristics
    - Static DC parameters in ICs: Currents and voltages
  - Timing or AC Characteristics
    - Dynamic values: Timing, delays, capacitances
- Other Data
  - Noise Characteristics
  - Operating Characteristics
  - Parameter Measurement

Summary Device Description

- Family & Part Number
  - Similar devices
- Device Features
  - Highlights
- Device Description
  - Summarized
- Package
  - Pin-out and variations
- Functional Diagram
  - Internal configuration
- Pin Functions


MSP430x20x1, MSP430x20x2, MSP430x20x3
MIXED SIGNAL MICROCONTROLLER

MSP430x20x1, MSP430x20x2, MSP430x20x3
MIXED SIGNAL MICROCONTROLLER

MSP430x20x1, MSP430x20x2, MSP430x20x3
MIXED SIGNAL MICROCONTROLLER

MSP430x20x1, MSP430x20x2, MSP430x20x3
MIXED SIGNAL MICROCONTROLLER

SLAS491D – AUGUST 2005 – REVISED SEPTEMBER 2007

Terminal Functions, MSP430x20x2

TERMINAL NAME	PW, or N NO.	RSA NO.	I/O	DESCRIPTION
P1.0/TACLK/ACLK/A0	2	1	I/O	General-purpose digital I/O pin Timer_A, clock signal TACLK input ACLK signal ouput ADC10 analog input A0
P1.1/TA0/A1	3	2	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: Out0 output ADC10 analog input A1
P1.2/TA1/A2	4	3	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare: Out1 output ADC10 analog input A2
P1.3/ADC10CLK/ A3/VREF-/VeREF-	5	4	I/O	General-purpose digital I/O pin ADC10 conversion clock output ADC10 analog input A3 Input for negative external reference voltage/negative internal reference voltage output
P1.4/SMCLK/A4/VREF+/VeREF+/ TCK	6	5	I/O	General-purpose digital I/O pin SMCLK signal output ADC10 analog input A4 Input for positive external reference voltage/positive internal reference voltage output JTAG test clock, input terminal for device programming and test
P1.5/TA0/A5/SCLK/TMS	7	6	I/O	General-purpose digital I/O pin Timer_A, compare: Out0 output ADC10 analog input A5 USI: external clock input in SPI or I2C mode; clock output in SPI mode JTAG test mode select, input terminal for device programming and test
P1.6/TA1/A6/SDO/SCL/TDI/TCLK	8	7	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1B input, compare: Out1 output ADC10 analog input A6 USI: Data output in SPI mode; I2C clock in I2C mode JTAG test data input or test clock input during programming and test
P1.7/A7/SDI/SDA/TDO/TDI†	9	8	I/O	General-purpose digital I/O pin ADC10 analog input A7 USI: Data input in SPI mode; I2C data in I2C mode JTAG test data output terminal or test data input during programming and test
XIN/P2.6/TA1	13	12	I/O	Input terminal of crystal oscillator General-purpose digital I/O pin Timer_A, compare: Out1 output
XOUT/P2.7	12	11	I/O	Output terminal of crystal oscillator General-purpose digital I/O pin
RST/NMI/SBWTDIO	10	9	I	Reset or nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/SBWTCK	11	10	I	Selects test mode for JTAG pins on Port1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test
V_{CC}	1	NA		Supply voltage
V_{SS}	14	NA		Ground reference

† TDO or TDI is selected via JTAG instruction.

NOTE: If XOUT/P2.7 is used as an input, excess current will flow until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

8

Courtesy of Texas Instruments, Inc.

Absolute Maximum Ratings

- Stress levels that, if exceeded, may cause permanent device damage
- Exposure for extended periods may affect device reliability
  - Voltage Levels
  - Terminal Current
  - Temperature

8.1. Absolute Maximum Ratings*

Ambiant Temperature Under Bias :

C = commercial	0°C to 70°C
I = industrial	–40°C to 85°C
Storage Temperature	–65°C to + 150°C
Voltage on VCC to VSS	–0.5 V to + 7 V
Voltage on Any Pin to VSS	–0.5 V to V_{CC} + 0.5 V
Power Dissipation	1 W

* This value is based on the maximum allowable die temperature and the thermal resistance of the package

Courtesy of Temic Semiconductors

22.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

Ambient temperature under bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to VSS (except VDD, MCLR, and RA4)	-0.3V to (VDD + 0.3V)
Voltage on VDD with respect to VSS	-0.3V to +7.5V
Voltage on MCLR with respect to VSS **(Note 2)**	0V to +13.25V
Voltage on RA4 with respect to Vss	0V to +8.5V
Total power dissipation **(Note 1)**	1.0W
Maximum current out of VSS pin	300 mA
Maximum current into VDD pin	250 mA
Input clamp current, IIK (VI < 0 or VI > VDD)	±20 mA
Output clamp current, IOK (VO < 0 or VO > VDD)	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by PORTA, PORTB, and PORTE **(Note 3)** (combined)	200 mA
Maximum current sourced by PORTA, PORTB, and PORTE **(Note 3)** (combined)	200 mA
Maximum current sunk by PORTC and PORTD **(Note 3)** (combined)	200 mA
Maximum current sourced by PORTC and PORTD **(Note 3)** (combined)	200 mA

calculated as follows:
Σ IOH} + Σ {(VDD-VOH) x IOH} + Σ(VOl x IOL)

Courtesy of Microchip Corporation

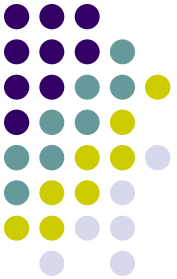
absolute maximum ratings†

Voltage applied at V_{CC} to V_{SS}	–0.3 V to 4.1 V
Voltage applied to any pin (see Note 2)	–0.3 V to V_{CC}+0.3 V
Diode current at any device terminal	±2 mA
Storage temperature, T_{stg} (unprogrammed device, see Note 3)	–55°C to 150°C
Storage temperature, T_{stg} (programmed device, see Note 3)	–40°C to 85°C

NOTES:
1. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
3. Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Courtesy of Texas Instruments, Inc.

Recommended Operating Conditions



- Conditions that should be provided by the application circuit for correct device functionality
- These values are used as test conditions for the limits in:
  - *Electrical characteristics*
  - *Timing requirements*
  - *Switching characteristics*
  - *Operating conditions*

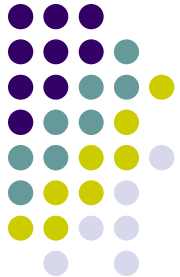
recommended operating conditions

		MIN	NOM	MAX	UNITS
Supply voltage during program execution, V_{CC}		1.8		3.6	V
Supply voltage during program/erase flash memory, V_{CC}		2.2		3.6	V
Supply voltage, V_{SS}			0		V
Operating free-air temperature range, T_A	I Version	–40		85	°C
	T Version	–40		105	°C
Processor frequency f_{SYSTEM} (Maximum MCLK frequency)	V_{CC} = 1.8 V, Duty Cycle = 50% ±10%	dc		6	MHz
	V_{CC} = 2.7 V, Duty Cycle = 50% ±10%	dc		12	
	V_{CC} ≥ 3.3 V, Duty Cycle = 50% ±10%	dc		16	

NOTES: 1. The MSP430 CPU is clocked directly with MCLK.
Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
2. Modules might have a different maximum input clock specification. Refer to the specification of the respective module in this data sheet.

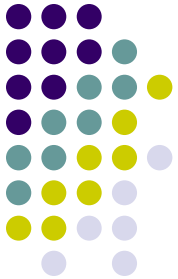
Courtesy of Texas Instruments, Inc.

Electrical Characteristics (1/4)



- Electrical-characteristic limits of the device when tested under the conditions in the recommended operating conditions table
  - Measured over recommended free-air temperature range table
  - Also known as the "*DC Characteristics*"
- Typical Parameters
  - Supply Current under different conditions (I_{DD})
  - Output Voltage Levels (V_{OL}, V_{OH})
  - Input Threshold Levels (V_{IL}, V_{IH})
  - Pin currents (I_{OL}, I_{OH}, I_{IL}, I_{IH}, I_Z)

Electrical Characteristics (2/4)



electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

active mode supply current (into V_{CC}) excluding external current (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	T_A	VCC	MIN	TYP	MAX	UNIT
$I_{AM,\ 1MHz}$	Active mode (AM) current (1MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 1MHz$, $f_{ACLK} = 32,768Hz$, Program executes in flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		220	270	µA
				3 V		300	370	
$I_{AM,\ 1MHz}$	Active mode (AM) current (1MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 1MHz$, $f_{ACLK} = 32,768Hz$, Program executes in RAM, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0,						

Courtesy of Texas Instruments, Inc.

leakage current

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{lkg(Px.x)}$	High-impedance leakage current	Port P1: P1.x, $0 \le x \le 7$ (see Notes 1, 2)	V_{CC} = 2.2 V/3 V,			±50	nA
		Port P2: P2.x, $0 \le x \le 5$ (see Notes 1, 2)	V_{CC} = 2.2 V/3 V,			±50	

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The leakage of the digital port pins is measured individually. The port pin must be selected for input and there must be no optional pullup or pulldown resistor.

electrical characteristics over recommended ranges of supply voltage and temperature (unless otherwise noted) (continued)

Schmitt-trigger inputs – Ports P1 and P2; (P1.0 to P1.7, P2.0 to P2.5)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 2.2 V	1.1		1.5
		V_{CC} = 3 V	1.5		1.9
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 2.2 V	0.4		0.9
		V_{CC} = 3 V	0.9		1.3
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)	V_{CC} = 2.2 V	0.3		1.1
		V_{CC} = 3 V	0.5		1

standard inputs – $\overline{RST}$/NMI, JTAG: TCK, TMS, TDI/TCLK

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX
V_{IL}	Low-level input voltage	V_{CC} = 2.2 V / 3 V	V_{SS}		V_{SS}+0.6
V_{IH}	High-level input voltage		0.8×V_{CC}		V_{CC}

outputs – Ports P1 and P2; (P1.0 to P1.7, P2.0 to P2.5)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage Port 1 and Port 2 (C11x1) Port 1 (F11x1A)	$I_{(OHmax)}$ = −1.5 mA	V_{CC} = 2.2 V	See Note 1	V_{CC}−0.25		V_{CC}	V
		$I_{(OHmax)}$ = −6 mA		See Note 2	V_{CC}−0.6		V_{CC}	
		$I_{(OHmax)}$ = −1.5 mA	V_{CC} = 3 V	See Note 1	V_{CC}−0.25		V_{CC}	
		$I_{(OHmax)}$ = −6 mA		See Note 2	V_{CC}−0.6		V_{CC}	
V_{OH}	High-level output voltage Port 2 (F11x1A)	$I_{(OHmax)}$ = −1 mA	V_{CC} = 2.2 V	See Note 3	V_{CC}−0.25		V_{CC}	V
		$I_{(OHmax)}$ = −3.4 mA		See Note 3	V_{CC}−0.6		V_{CC}	
		$I_{(OHmax)}$ = −1 mA	V_{CC} = 3 V	See Note 3	V_{CC}−0.25		V_{CC}	
		$I_{(OHmax)}$ = −3.4 mA		See Note 3	V_{CC}−0.6		V_{CC}	
V_{OL}	Low-level output voltage Port 1 and Port 2 (C11x1, F11x1A)	$I_{(OLmax)}$ = 1.5 mA	V_{CC} = 2.2 V	See Note 1	V_{SS}		V_{SS}+0.25	V
		$I_{(OLmax)}$ = 6 mA		See Note 2	V_{SS}		V_{SS}+0.6	
		$I_{(OLmax)}$ = 1.5 mA	V_{CC} = 3 V	See Note 1	V_{SS}		V_{SS}+0.25	
		$I_{(OLmax)}$ = 6 mA		See Note 2	V_{SS}		V_{SS}+0.6	

NOTES: 1. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.

Electrical Characteristics (3/4)

- Tabular Form for Important Parameters (intel 80C32 by Temic)
  - Input thresholds
    - (V_{IL}, V_{IH})
  - Output Thresholds
    - (V_{OL}, V_{OH})
  - Current Sinking
    - (I_{IL}, I_{IH}, I_Z=I_{PD})
  - Current Sourcing (as test conditions)
    - (I_{OL}, I_{OH})
  - Supply Current
    - (I_{CC}, I_{DD})

Courtesy of Temic Semiconductors

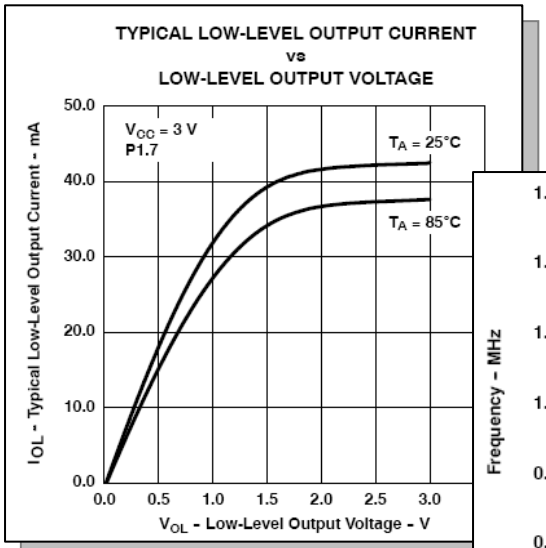
Table 3: DC Parameters

TA = 0°C to 70°C ; VSS = 0 V ; VCC = 5 V ± 10 % ; F = 0 to 44 MHz
TA = –40°C + 85°C ; VSS = 0 V ; VCC = 5 V ± 10 % ; F = 0 to 36 MHz

Symbol	Parameter	Min	Max	Unit	Test Conditions
VIL	Input Low Voltage	– 0.5	0.2 Vcc – 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 Vcc + 1.4	Vcc + 0.5	V	
VIH1	Input High Voltage (for XTAL and RST)	0.7 Vcc	Vcc + 0.5	V	
VOL	Output Low Voltage (Port 1, 2 and 3)		0.3 0.45 1.0	V V V	IOL = 100 µA IOL = 1.6 mA (note 2) IOL = 3.5 mA
VOL1	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$)		0.3 0.45 1.0	V V V	IOL = 200 µA IOL = 3.2 mA (note 2) IOL = 7.0 mA
VOH	Output High Voltage Port 1, 2, 3	Vcc – 0.3		V	IOH = – 10 µA
		Vcc – 0.7		V	IOH = – 30 µA
		Vcc – 1.5		V	IOH = – 60 µA VCC = 5 V ± 10 %
VOH1	Output High Voltage (Port 0, ALE, $\overline{PSEN}$)	Vcc – 0.3		V	IOH = – 200 µA
		Vcc – 0.7		V	IOH = – 3.2 mA
		Vcc – 1.5		V	IOH = – 7.0 mA VCC = 5 V ± 10 %
IIL	Logical 0 Input Current (Ports 1, 2 and 3)		– 50	µA	Vin = 0.45 V
ILI	Input leakage Current		± 10	µA	0.45 < Vin < Vcc
ITL	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)		– 650	µA	Vin = 2.0 V
IPD	Power Down Current		50	µA	Vcc = 2.0 V to 5.5 V (note 1)
RRST	RST Pulldown Resistor	50	200	KOhm	
CIO	Capacitance of I/O Buffer		10	pF	fc = 1 MHz, Ta = 25°C
ICC	Power Supply Current Freq = 1 MHz Icc op Icc idle Freq = 6 MHz Icc op Icc idle Freq ≥ 12 MHz Icc op = 1.25 Freq (MHz) + 5 mA Icc idle = 0.36 Freq (MHz) + 2.7 mA		 1.8 1 10 4	 mA mA mA mA	Vcc = 5.5 V

Electrical Characteristics (4/4)

- Parametric Plots: Allow estimating non-tabulated parameter values
  - $I_O = f(Vo)$, $f_{CLK} = f(V_{DD})$



Courtesy of Texas Instruments, Inc.

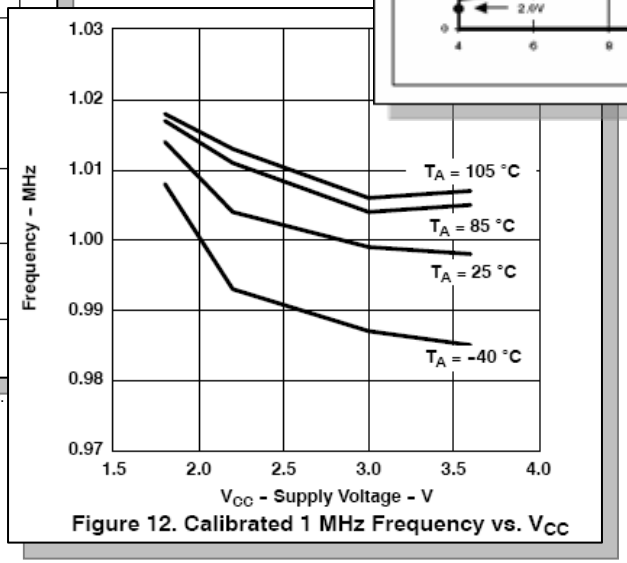
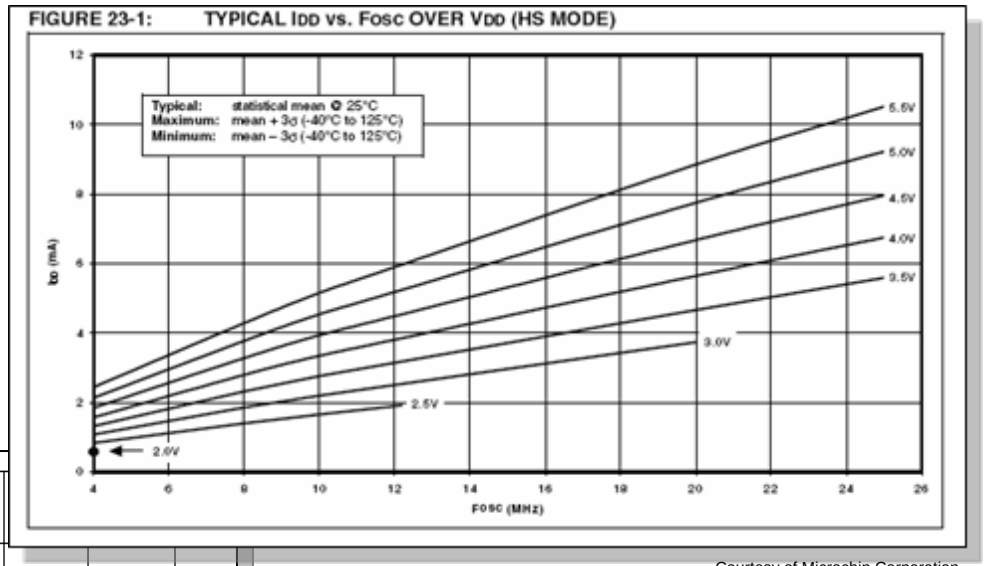


Figure 12. Calibrated 1 MHz Frequency vs. V_{CC}



Courtesy of Microchip Corporation

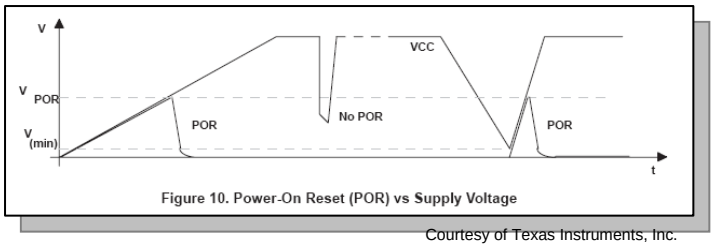
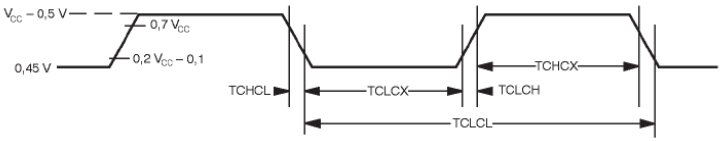


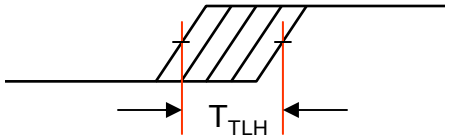
Figure 10. Power-On Reset (POR) vs Supply Voltage

Courtesy of Texas Instruments, Inc.

Understanding Timing Diagrams

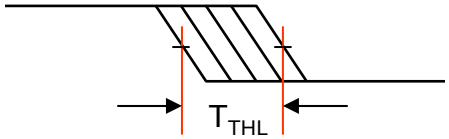


Single Line Transitions

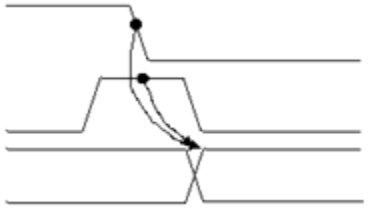


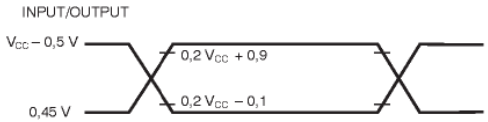
Low-to-high Signal


Signal edge triggered bus transition

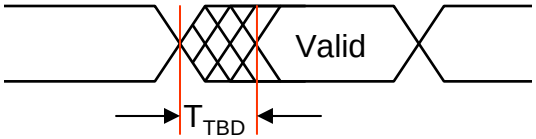


High-to-low Signal

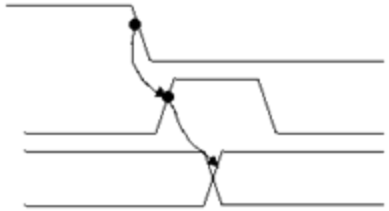

Edge AND level triggered bus transition

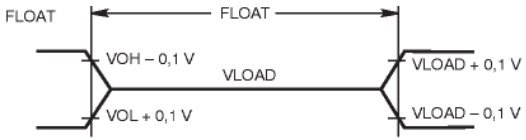


Bus Transitions

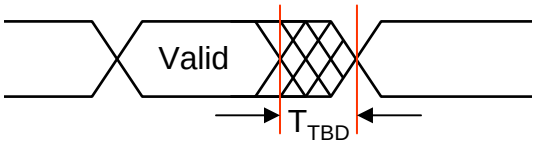


Begin of Valid Bus Signal


Double edge triggered bus transition



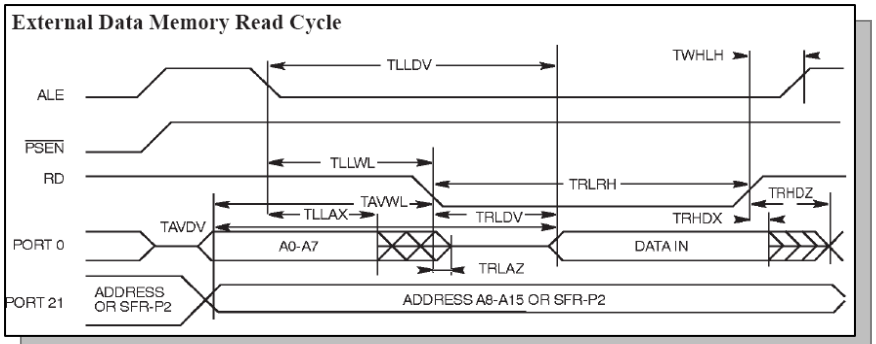
Tri-state Bus



End of Valid Bus Signal

Sample μP Timing Diagrams

- Format changes among manufacturers
  - Examples show an 80c32 and i8086

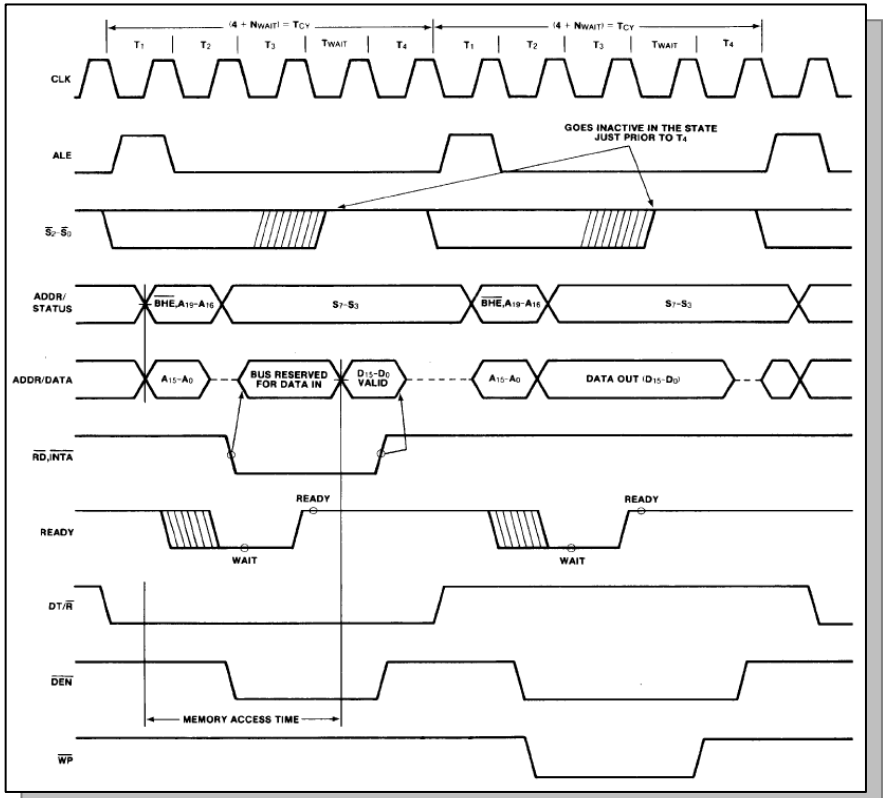


Courtesy of Temic Semiconductors

Table 9: External Data Memory Characteristics (values in ns)

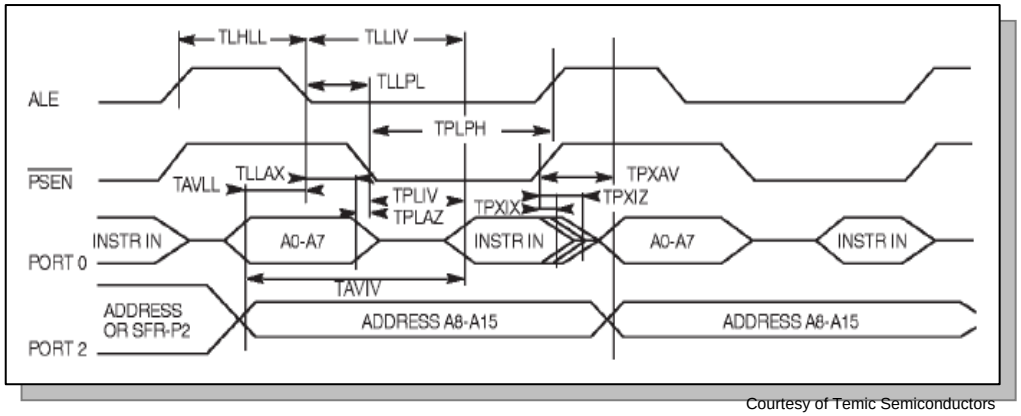
		16 MHz		20 MHz		25 MHz		30 MHz		36 MHz		40 MHz		42 MHz		44 MHz	
Symbol	Parameter	min	max	min	max	min	max	min	max	min	max	min	max	min	max	min	max
TRLRH	RD pulse Width	340		270		210		180		120		100		90		80	
TWLWH	WR pulse Width	340		270		210		180		120		100		90		80	
TLLAX	Address Hold After ALE	85		85		70		55		35		30		25		25	
TRLDV	RD to Valid Data in		240		210		175		135		110		90		80		70
TRHDX	Data hold after RD	0		0		0		0		0		0		0		0	
TRHDZ	Data float after RD		90		90		80		70		50		45		40		35
TLLDV	ALE to Valid Data In		435		370		290		235		170		150		140		130
TAVDV	Address to Valid Data IN		480		400		320		260		190		180		175		170
TLLWL	ALE to WR or RD	150	250	135	170	120	130	90	115	70	100	60	95	55	90	50	85

Courtesy of Temic Semiconductors



Courtesy of Intel Corporation

AC Characteristics



Courtesy of Temic Semiconductors

8.6. AC Parameters

TA = 0 to + 70°C ; Vss = 0 V ; Vcc = 5 V ± 10 % ; F = 0 to 44 MHz
TA = 0 to +70°C ; Vss = 0 V ; 2.7 V < Vcc < 5.5 V ; F = 0 to 16 MHz
TA = –40° to + 85°C ; Vss = 0 V ; 2.7 V < Vcc < 5.5 V ; F = 0 to 16 MHz
TA = –55° + 125°C ; Vss = 0 V ; Vcc = 5 V ± 10 % ; F = 0 to 36 MHz
(Load Capacitance for PORT 0, ALE and PSEN = 100 pF ; Load Capacitance for all other outputs = 80 pF)

Courtesy of Temic Semiconductors

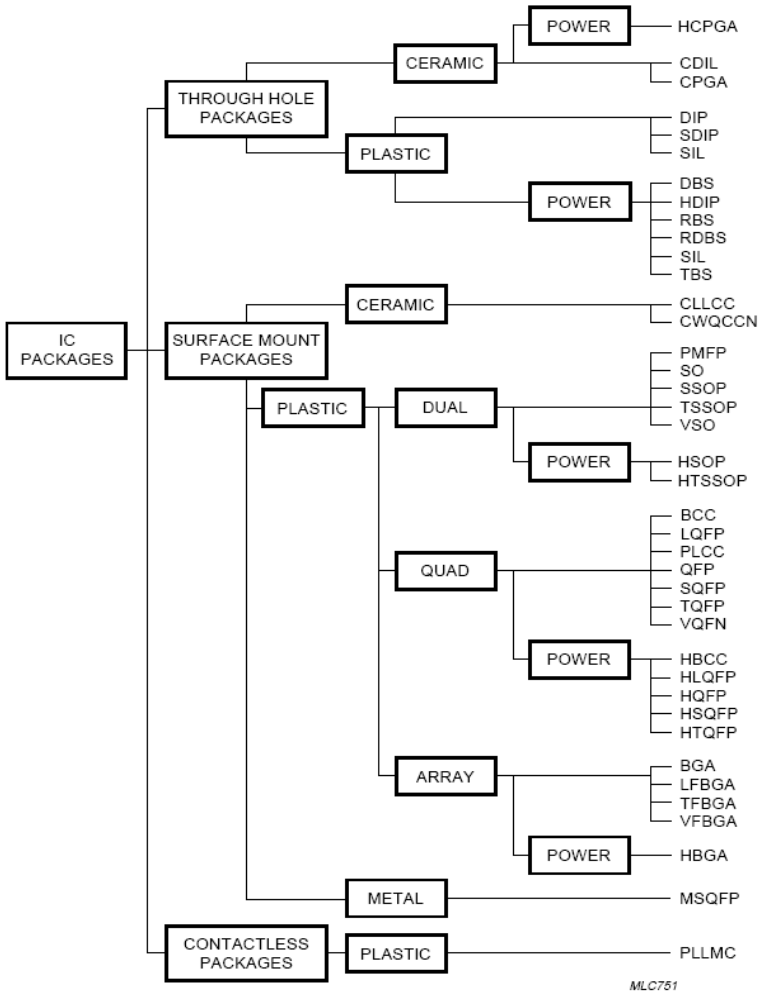
Table 8: External Program Memory Characteristics (values in ns)

		16 MHz		20 MHz		25 MHz		30 MHz		36 MHz		40 MHz		42 MHz		44 MHz	
Symbol	Parameter	min	max	min	max	min	max	min	max	min	max	min	max	min	max	min	max
TLHLL	ALE Pulse Width	110		90		70		60		50		40		35		30	
TAVLL	Address valid to ALE	40		30		20		15		10		9		8		7	
TLLAX	Address Hold After ALE	35		35		35		35		35		30		25		17	
TLLIV	ALE to valid instr in		185		170		130		100		80		70		65		65
TLLPL	ALE to PSEN	45		40		30		25		20		15		13		12	
TPLPH	PSEN pulse Width	165		130		100		80		75		65		60		54	
TPLIV	PSEN to valid instr in		125		110		85		65		50		45		40		35
TPXIX	Input instr Hold After PSEN	0		0		0		0		0		0		0		0	
TPXIZ	Input instr Float After PSEN		50		45		35		30		25		20		15		10
TPXAV	PSEN to Address Valid	55		50		40		35		30		25		20		15	
TAVIV	Address to Valid instr in		230		210		170		130		90		80		75		70
TPLAZ	PSEN low to Address Float		10		10		8		6		5		5		5		5

Courtesy of Temic Semiconductors

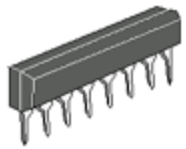
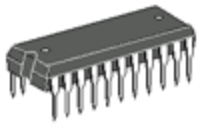
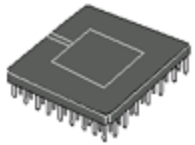
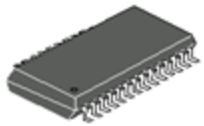
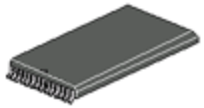
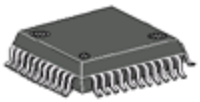
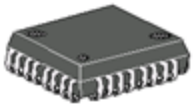
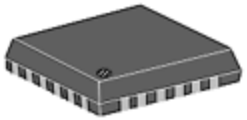
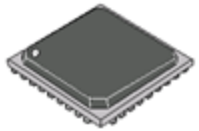
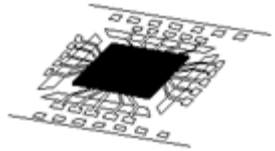
IC Packages

- Through-hole Mount
  - Low pin density
  - Easy hand prototyping
    - SIP
    - DIP
- Surface Mount
  - Medium to high density
  - Require adapter for hand prototyping
    - DIP
    - Quad
    - Array
- Contactless Mount
  - Not clear yet
  - Need to find out



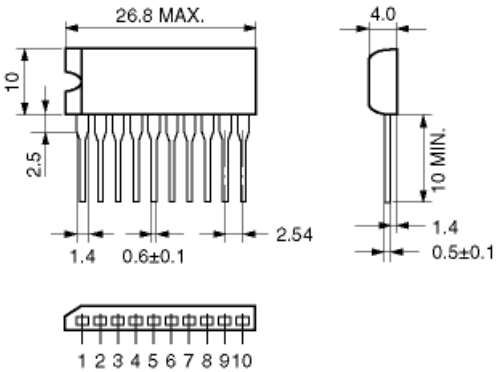
Courtesy of Philips Semiconductors

Review of IC Packages

					
SIP: Single In-line Package	**DIP**: Dual In-line Package	**SOJ**: Small Outline J-leaded	**PGA**: Pin Grid Array	**SOP**: Small Outline Package	**TSOP**: Thin Small Outline Package
					
QFP: Quad Flat Package	**PLCC**: Plastic Leaded Chip Carrier	**LCC**: Leadless Chip Carrier	**BGA**: Ball Grid Array	**LGA**: Land Grid Array	**TCP**: Tape Carrier Package

Courtesy of NEC Electronics

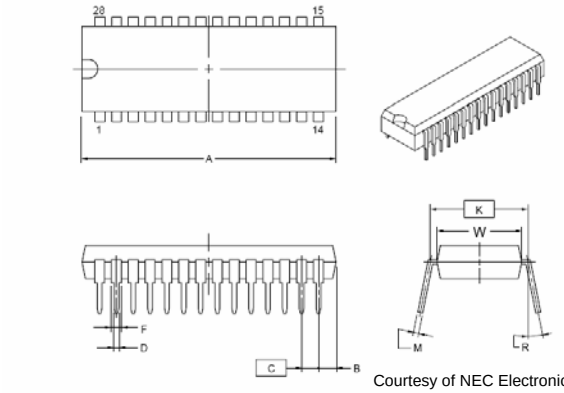
Single In-line Package (SIP)



Courtesy of NEC Electronics

- **Description**
  - Leads extending directly from one longer edge of the package are vertically mounted on the printed circuit board. The consequent reduction in mounting area allows many devices to be packed into a small area (high-density mounting).
- **Package Variations**
  - LBS
  - DBS
- **Package Attributes**
  - Pin Count and Lead Pattern

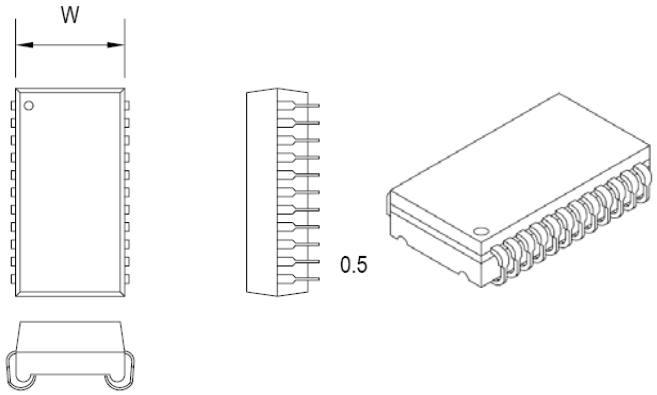
Dual In-line Package (DIP)



Courtesy of NEC Electronics

- **Description**
  - The most basic, first generation IC package
  - Leads are thru-hole, with a typical spacing of 0.100“, and extend on the long sides of the package body
  - Body width varies: 0.300", 0.400", 0.600" and 0.900".
- **Package Variations**
  - Shrink DIP (SDIP): have higher pin counts (i.e., 48 or 64 lead) with a lead pitch of 0.70" and a body size of either 0.600" or 0.750".
- **Package Attributes**
  - Pin Count and Body Width (W)

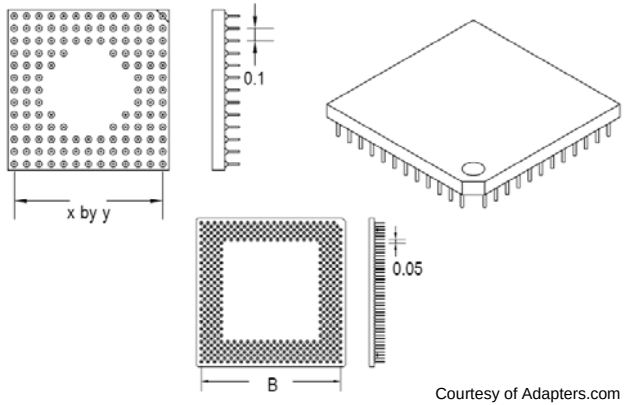
Small Outline J-leaded (SOJ)



Courtesy of Adapters.com

- **Description**
  - Originated as a surface-mount DIP equivalent with lead pitch reduced to 50 mil.
  - Pins protrude on two sides of the plastic package body and curl under it in a shape similar to the letter "J".
  - This package is sometimes referred to as a J-leaded package
  - Early versions were very common in SIMM memory modules
- **Package Variations**
  - N/A
- **Package Attributes**
  - Pin Count and Body Width (W)

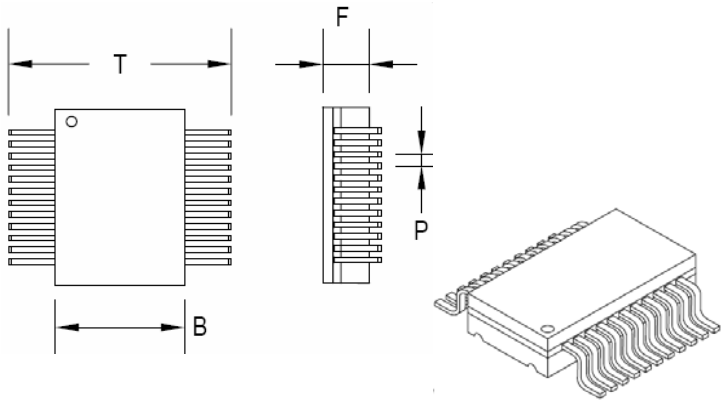
Pin Grid Array (PGA)



Courtesy of Adapters.com

- **Description**
  - Second generation package. Thru-hole leads placed in the underside of the packag in a grid pattern. Pins are located on a 0.1" grid in various patterns. The grids is called out by the pins in the x direction and the pins in the y direction. Commonly used in PC CPUs.
- **Package Variations**
  - Interstitial package (IPGA): carries additional pins on a 0.5" offset pattern in between the pins of a regular PGA pattern. It almost doubles the available pins on the same package size as a standard PGA.
- **Package Attributes**
  - Pin Count, Grid Size (x by y), and Grid Pattern

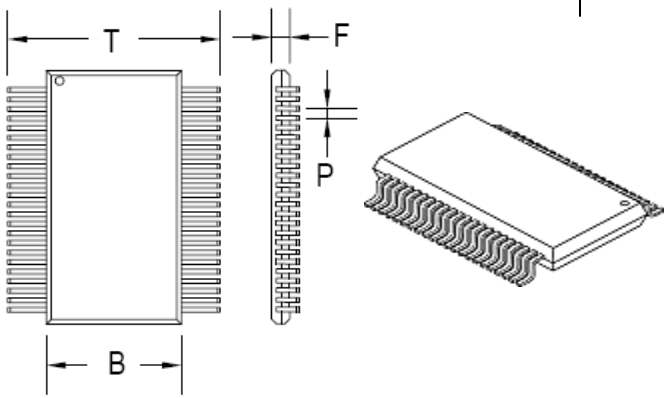
Small Outline Package (SOP)



Courtesy of Adapters.com

- **Description**
  - First surface-mount package to replace 8-16 DIP packages
  - Alternate names: "Gull Wing" pins shape or SOIC
  - Commonly used parts with up to 64 pins
  - Mostly used in memory ICs
- **Package Variations**
  - SOP -- Pitch = 1.27mm
  - SSOP -- Pitch = 0.4, 0.5 or 0.65mm
- **Package Attributes**
  - Pin Count, Pitch (P), Body Width (B), Body Thickness (F), and Tip-to-Tip Width (T)

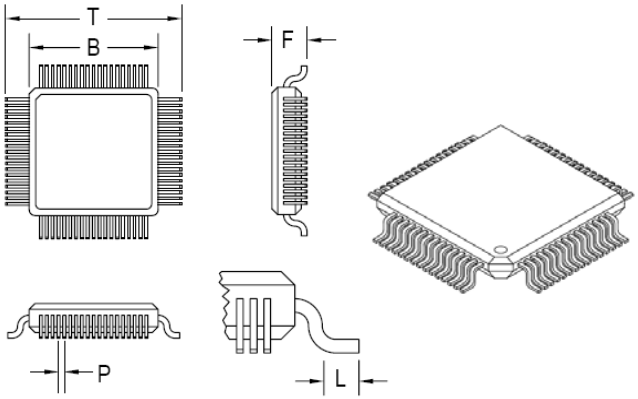
Thin SOP (TSOP)



Courtesy of Adapters.com

- **Description**
  - A variation of SOP with thinner body and larger pin count
  - TSOP I has the pins on the WIDE edge
  - The TSOP II has leads on NARROW side
- **Package Variations**
  - TSOP I -- Pitch 0.5 or 0.55mm
  - TSOP II -- Pitch: 0.65, 0.8 or 1.25mm
  - TSSOP -- Pitch: 0.4, 0.5 or 0.65mm
- **Package Attributes**
  - Pin Count, Pitch (P), Body Width (B), Body Thickness (F), Tip to Tip Width (T)

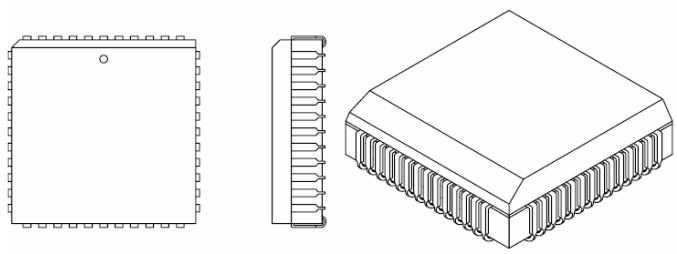
Quad Flat Pack (QFP)



Courtesy of Adapters.com

- **Description**
  - A high-density, surface-mount, evolved SOP with leads protruding on all four sides of the package.
  - Mostly built with plastic body (PQFP)
- **Package Variations**
  - Ceramic Quad Flat Pack (CQFP)
  - Metal Quad Flat Pack (MQFP)
  - Thin QFP (TQFP) -- 2mm body thickness
  - Very (small) QFP (VQFP): Same as TQFP.
- **Package Attributes**
  - Pin Count, Pitch (P), Body Width (B), Body Thickness (F), Tip-to-Tip Width (T), and Foot Length (L)

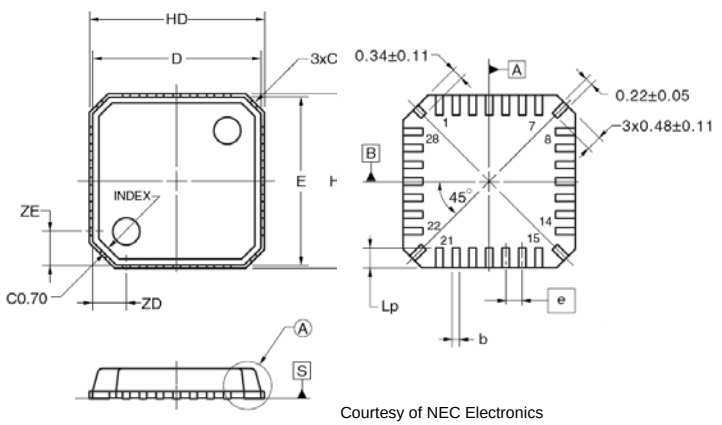
Plastic Leaded Chip Carrier (PLCC)



Courtesy of Adapters.com

- **Description**
  - Third generation packaging and the first true surface-mount package. An evolved and more popular version of the SOJ with leads on all four sides. Pitch and body sizes are fairly standard. Also called QFJ.
- **Package Variations**
  - Leadless Chip Carrier (LCC): Ceramic body with no physical leads. Pads on the bottom of the IC around the edges.
  - J-Leaded Chip Carrier (JLCC): Ceramic body material with leads similar to PLCC package.
- **Package Attributes**
  - Pin Count

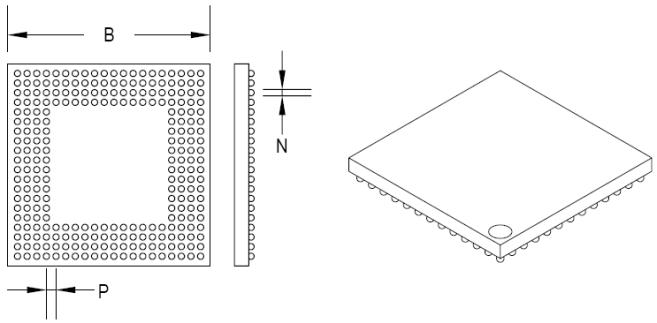
Leadless Chip Carrier (LCC)



Courtesy of NEC Electronics

- **Description**
  - This is similar to the PLCC package, however the leads located at four edges of the back of the package. LCC packages can be made in thinner and high-density models.
- **Package Variations**
  - Quad Flat Non-Leaded (QFN)
  - Very-thin QFN (VQFN)
- **Package Attributes**
  - Pin Count, Lead Pitch (P), and Body Size (B),

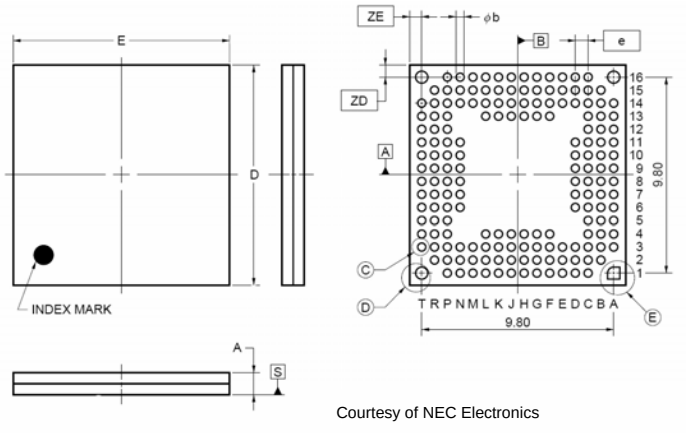
Ball Grid Array (BGA)



Courtesy of Adapters.com

- **Description**
  - A high-density, surface-mount package similar to PGA. In BGA pin connections are solder balls in a grid pattern, on the bottom side.
- **Package Variations**
  - MicroBGA and XBGA: Same as BGA, with finer grids. Pitch sizes: 0.65, 0.75 and 0.8mm.
  - Interstitial BGA: (IBGA) A package with denser pin count, in an offset pattern in-between the balls of a regular BGA pattern.
  - Flip-chip BGA (FCBGA): Die directly attached to substrate using solder bumps.
- **Package Attributes**
  - Pin Count, Lead Pitch (P), Grid Size (x by y), Body Size (B), Ball Size (N), and Grid Pattern

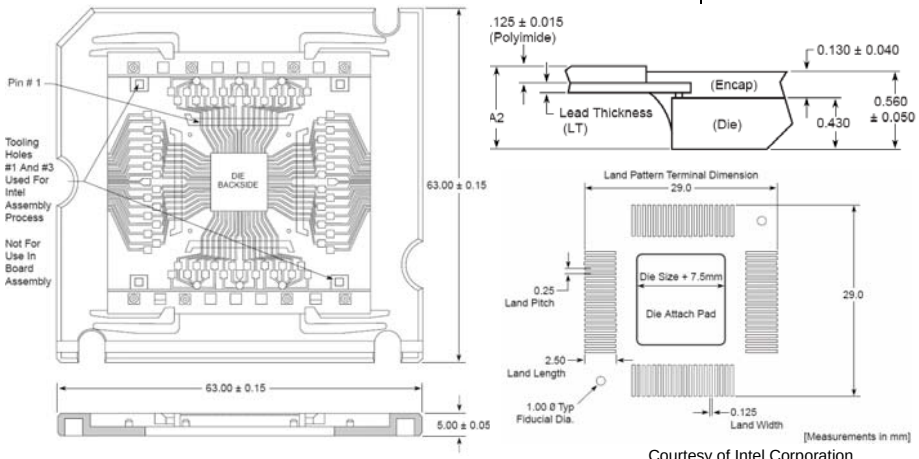
Land Grid Array (LGA)



Courtesy of NEC Electronics

- **Description**
  - This is a package with electrodes aligned in an array on its back.
  - It is suited for high-speed operation since its parasitic inductance is low. Further, in contrast to BGA, LGA does not have solder balls, so the mounting height can be reduced..
- **Package Variations**
  - Fine-pitch Land Grid Array (FLGA)
- **Package Attributes**
  - Pin Count, Lead Pitch (P), Grid Size (x by y), Body Size (B), and Grid Pattern

Tape Carrier Package (TCP)

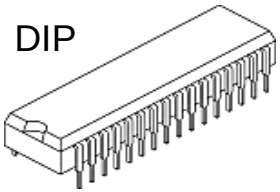


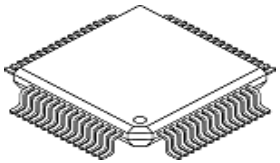
Courtesy of Intel Corporation

- **Description**
  - In the TCP package, silicon chips are packaged onto flexible tape-shaped films. TCP packages are thin, compact, with high pin count, and can be bent. TCP packages are mainly used for LCD drivers.
- **Package Variations**
  - Chip On Film (COF)
  - Ink Jet Printer Driver (IJTCP)
- **Package Attributes**
  - Pin Count, Lead Pitch (P), Grid Size (x by y), and Grid Pattern, Package Thickness,

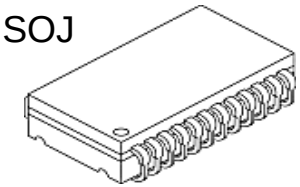
Typical Package Profiles

DIP

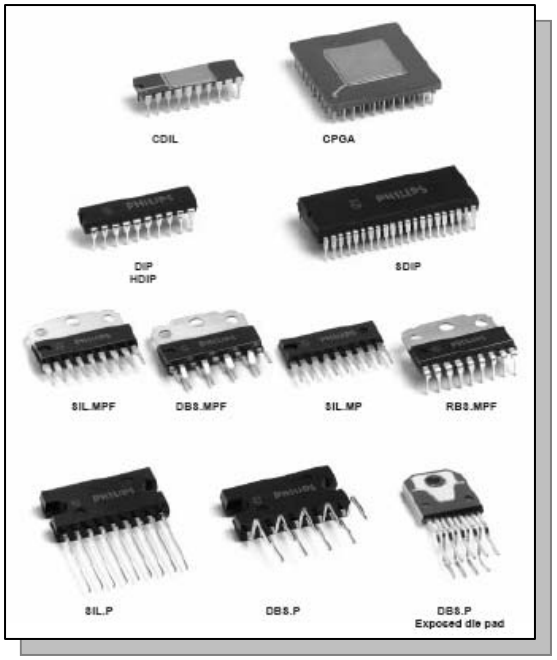




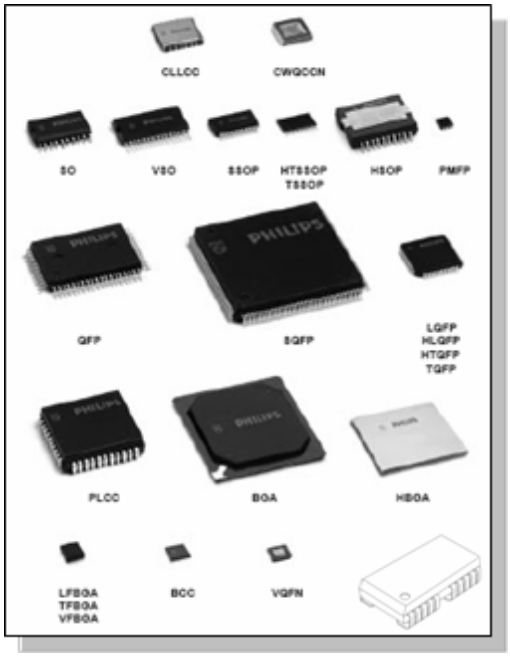
SOJ



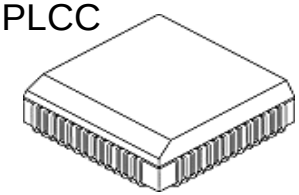
Through Hole Packages



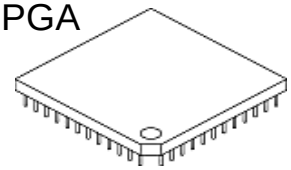
Surface Mount Packages



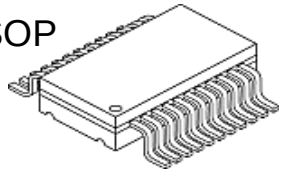
PLCC



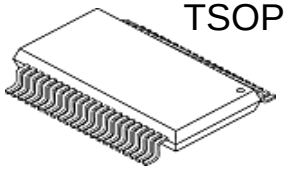
PGA



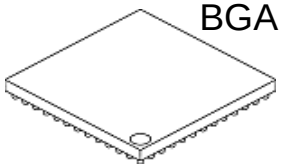
SOP



TSOP



BGA



Summary

- Handling Precautions for Electronic Circuits
  - Electrostatic Discharge
- Understanding Data Sheets
  - Hardware and software components
  - Scope and consideration for diverse target applications
- Basic Interface for uP-based Systems
  - Power requirements
  - Clock sources
  - Hardware reset
  - Software initialization
  - Interfacing Considerations
- Basic Interface for the MSP430