ECSE 325 – Digital Systems
Winter 2020

Lab 1: Basics of Mapping VHDL to FPGA Hardware

Overview

In this lab, you will learn the basics of compiling synchronous circuit VHDL description to a target FPGA.

The goal of this lab exercise is to become familiar with the Quartus tool, especially dealing with how compiler maps the design onto the FPGA hardware. This introductory exercise contains a step-by-step tutorial on getting started.

After completing this exercise, you should know how to:

- Start the Altera Quartus II software
- Create the framework for a new project
- Write a VHDL description of a logic circuit
- Understand logic utilization within the FPGA board
- Understand the floorplan and RTL viewer of a circuit

This lab will have a number of items that each lab group must complete, as well as a project report that will be submitted for each group. The report requirements are described at the end of the lab description. While there is no explicit demonstration to TAs required in this lab, future labs will all require well-done demonstration. The demo requirement sheet is attached at the end of this lab handout.

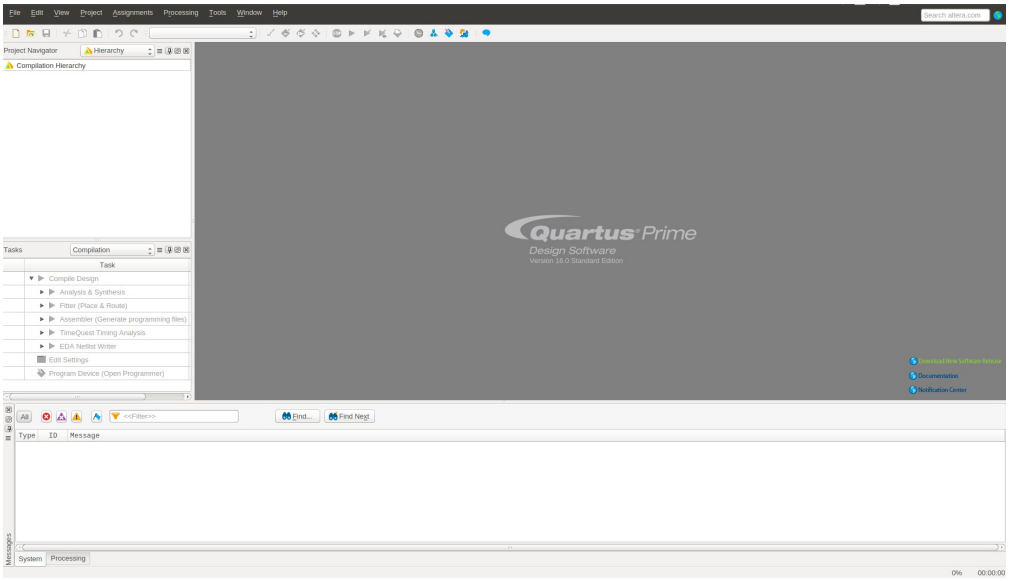
Exercise Details

Tool Startup and Project Creation

You can start the Quartus tool by selecting the icon on the Windows start menu: 

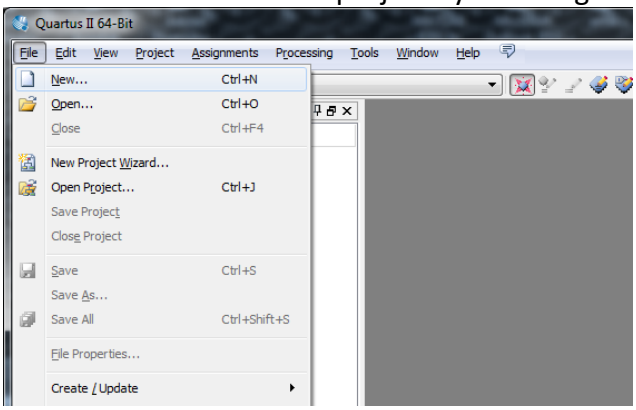
We should be using the version 16.1 as it supports the DE1-SoC lab kits the best.

On startup, you should see the following window (it might slightly differ in your case) for an empty project.

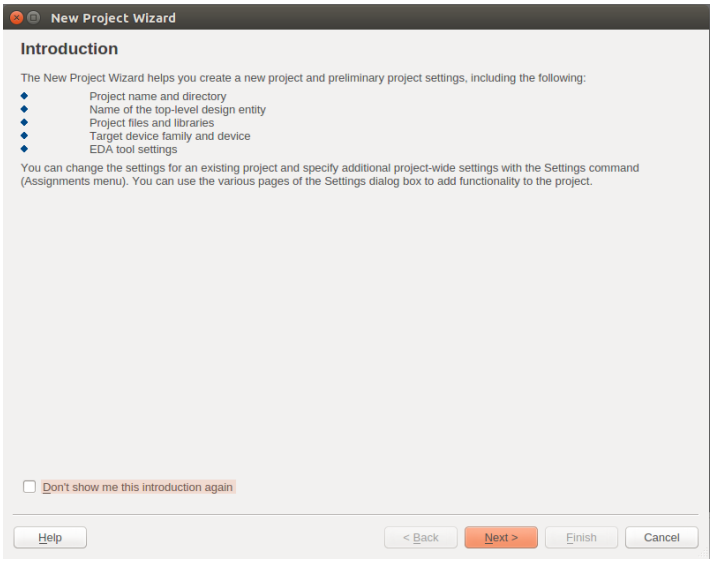


Project Creation

You have to first create a project by selecting **File->New Project Wizard**.

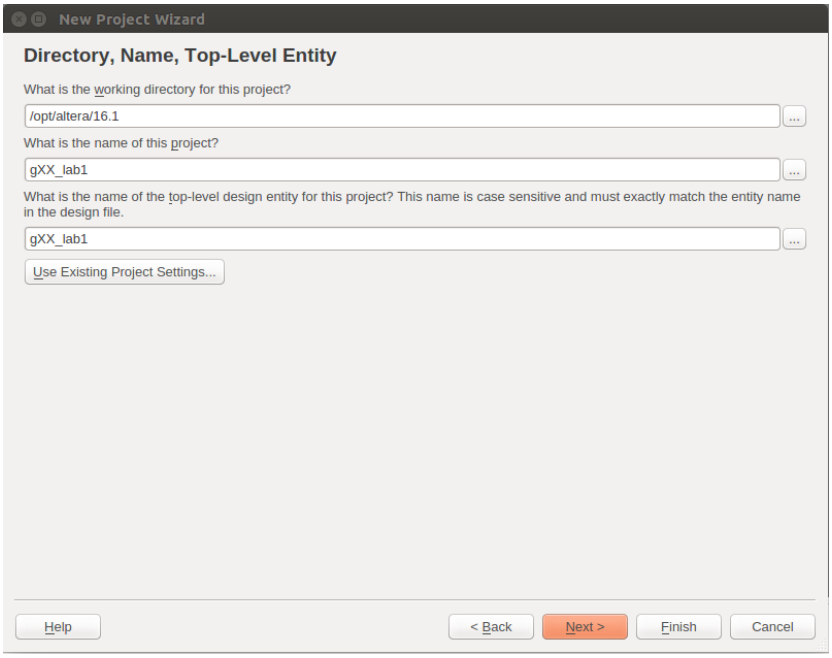


You should then go through a series of windows to create the project, starting with the following

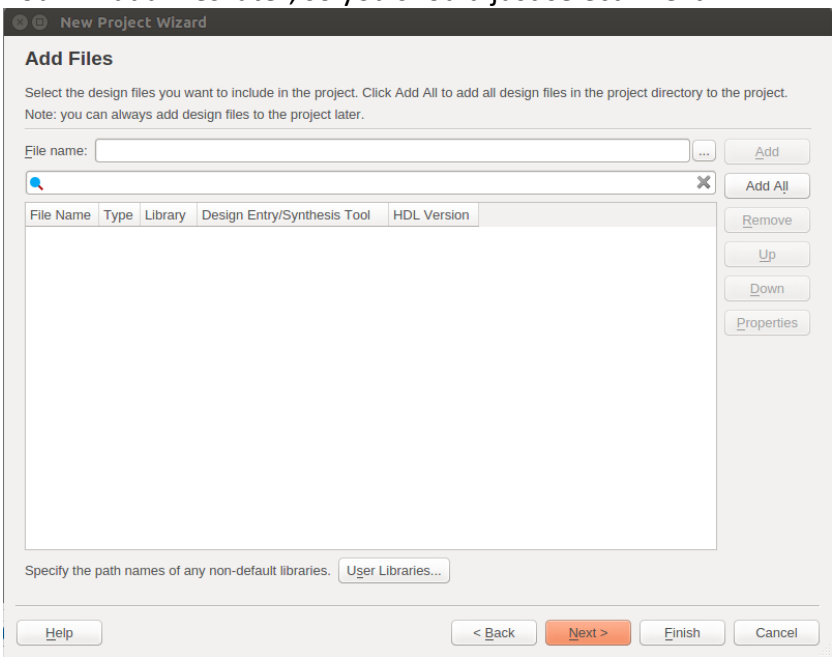


In the second window you should give the project the name: gNN lab1 where NN is replaced with your 2-digit group number. The working directory for your project will be different than that shown here, since you should use your network drive for all project files.

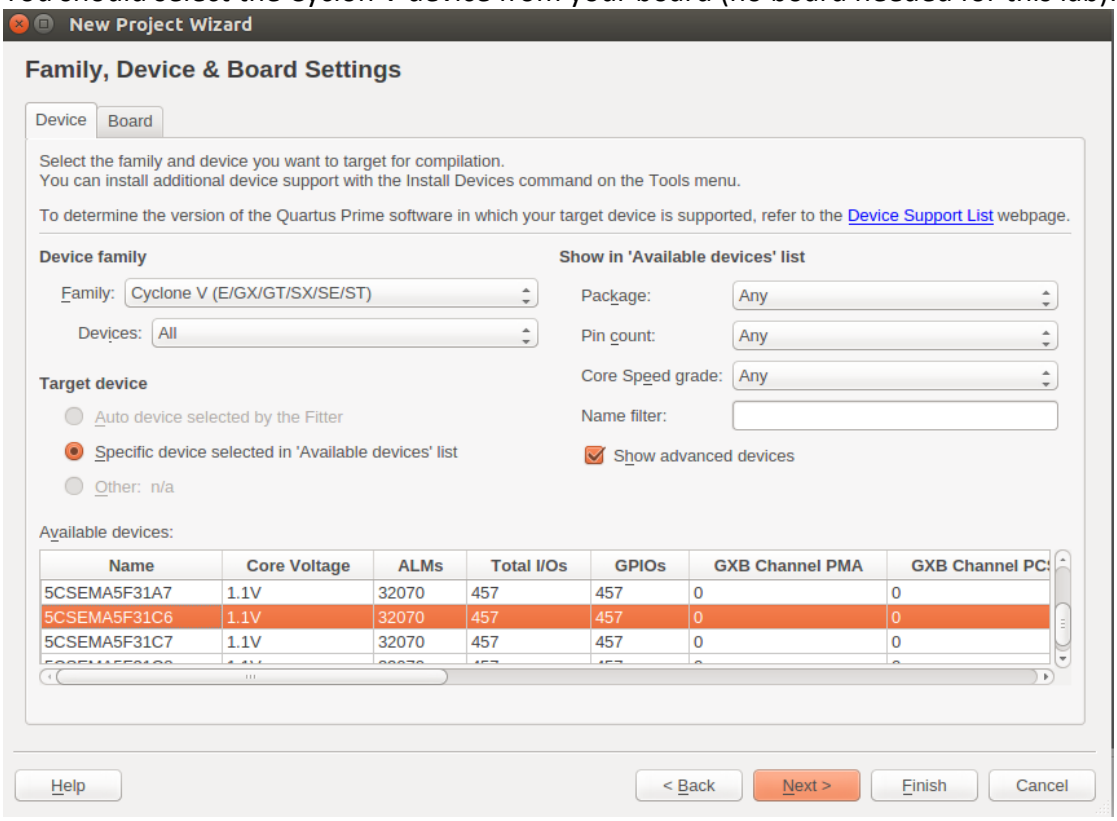
Since you do not have a project template, you can proceed with the Empty Project selection



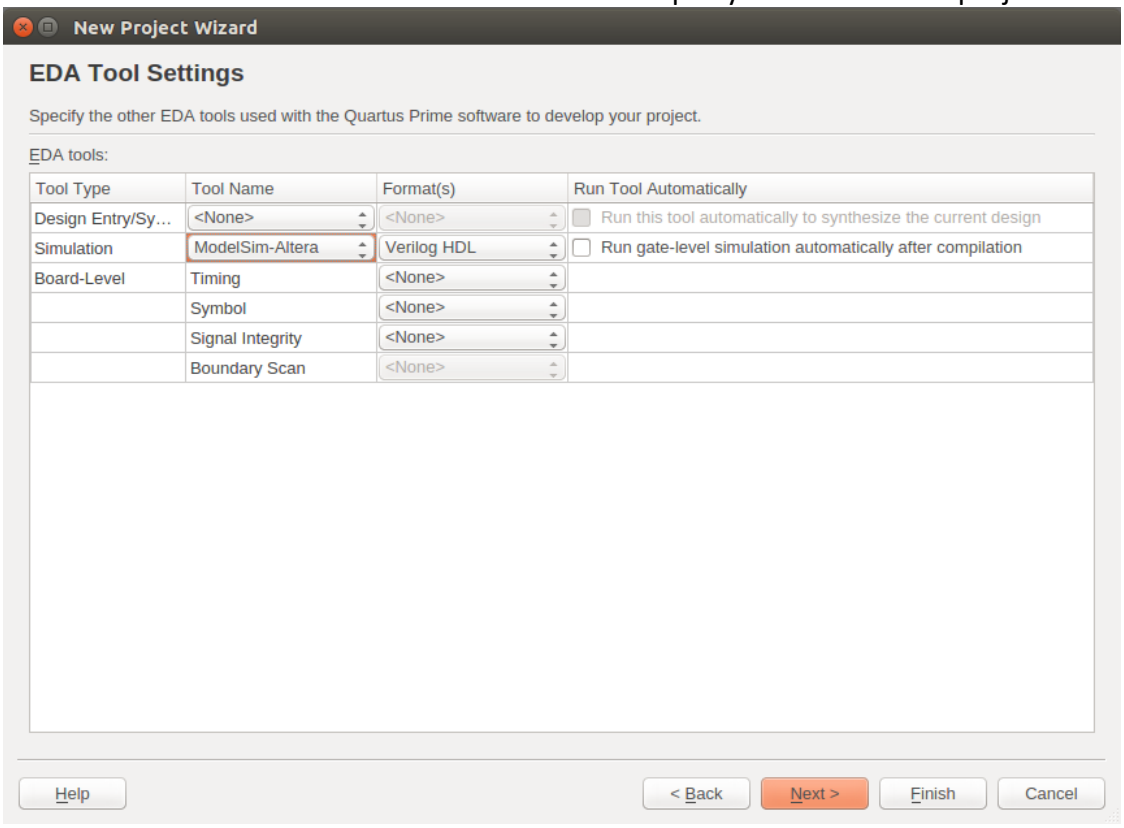
You will add files later, so you should just select “Next>”



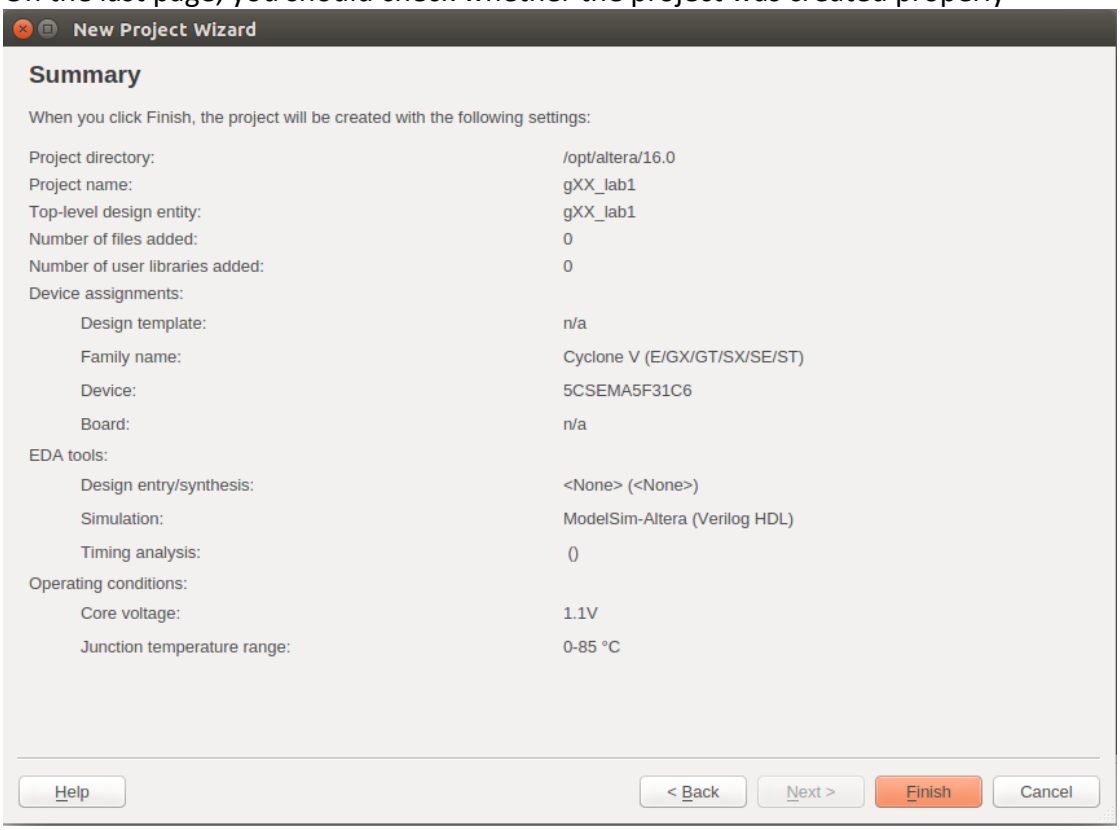
You should select the Cyclon V device from your board (no board needed for this lab):



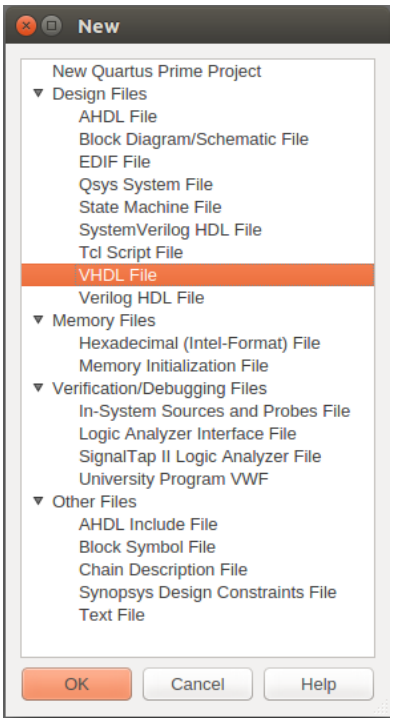
You should also include Modelsim-Altera as a third-party tool used in the project



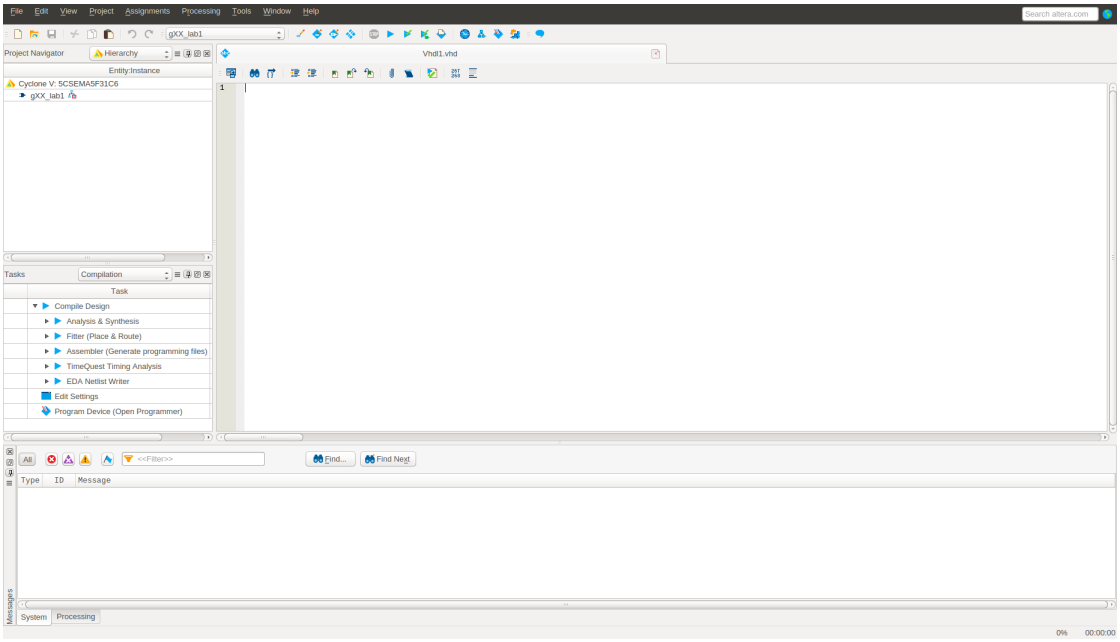
On the last page, you should check whether the project was created properly



You are now ready to create a new VHDL file



VHDL Editor should open next, where you can enter your code



Synchronous Dual Rate Counter in VHDL

You need to create a synchronous 8-bit counter with the following characteristics:

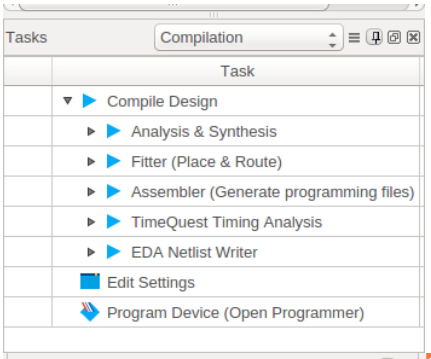
- Synchronous reset
- Counting by ones or twos features
  - Should never overcount
  - If counting by twos, should only have even outputs
- Enable counting option

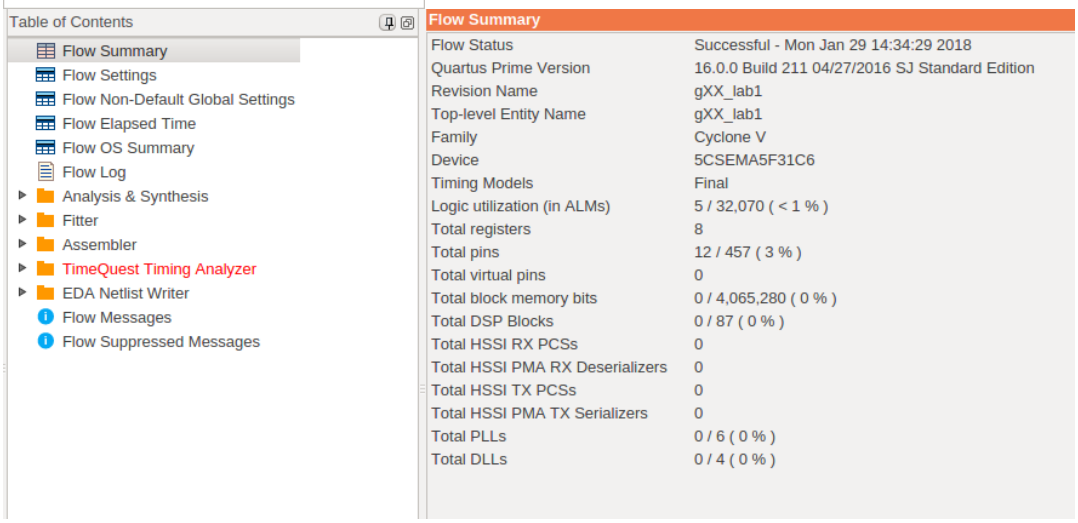
The library and entity declarations are:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
entity gXX_lab1 is
   Port (      clk          : in     std_logic;
               countbytwo   : in     std_logic;
               rst          : in     std_logic;
               enable       : in     std_logic;
               output       : out    std_logic_vector(7 downto 0));
end gXX_lab1;
```

where “XX” is replaced by your group number.

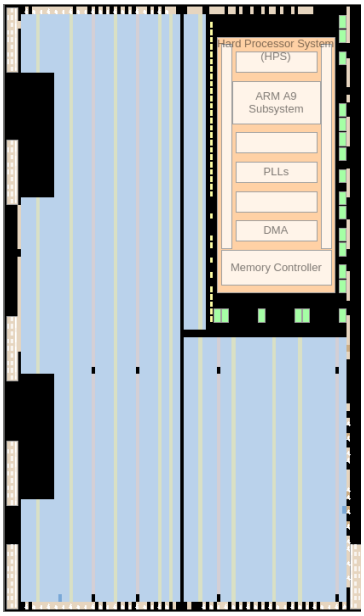
Once you have completed your sequential circuit, you can compile your design with **Processing->Start Compilation** selection. Once your code is free of errors and compiles well, all the tasks should be available (turn green on the display)





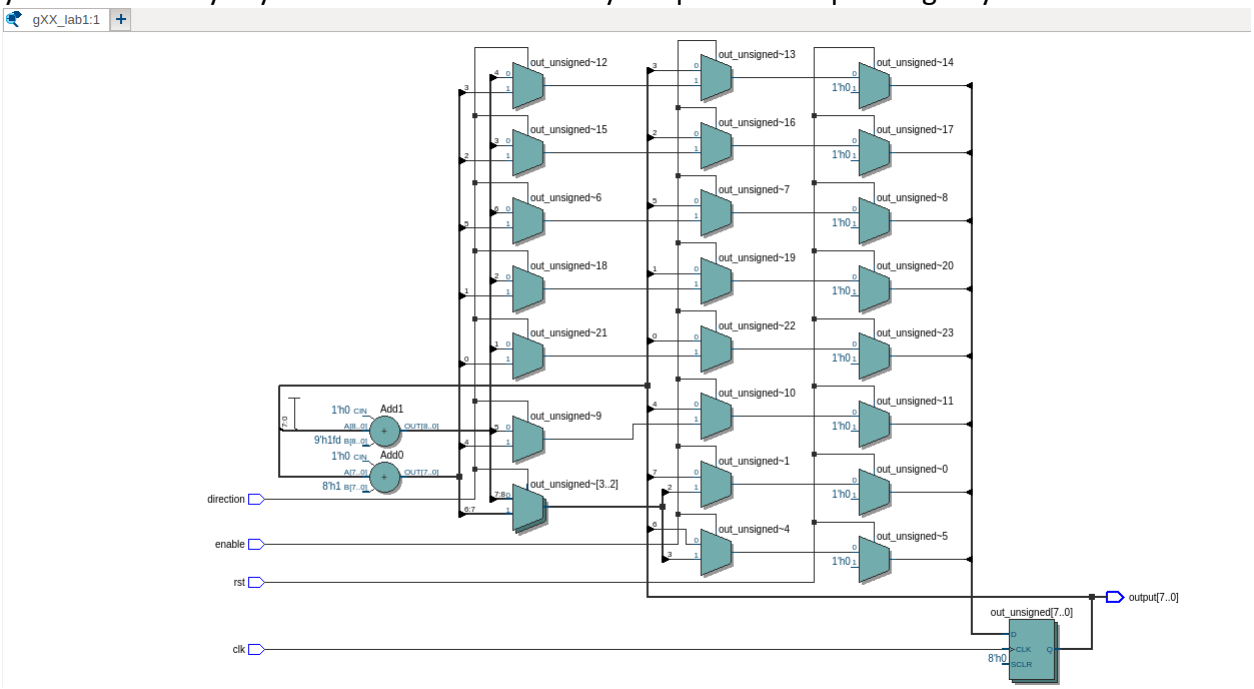
Chip Planner

By selecting **Tools-> Chip Planner**, you can observe the FPGA utilization and the layout of your circuit.



RTL Viewer

A very useful and powerful tool is available at **Tools->Netlist Viewers->RTL Viewer** that will show you the logic schematic of your circuit. The figure below is included for illustration purposes, as you should analyze your schematic and identify the parts corresponding to your code.



Lab Report

At the end of the lab, you should know how to prepare and compile a VHDL code and understand how it maps to FPGAs. You are required to submit a single PDF file that:

- is written in the standard technical report format
- documents every design choice clearly
- is organized for the grader to easily reproduce your results by running your code
- contains the code that is well-documented and easy to read
- should not cause the struggle for a grader to understand

Necessary parts

- The VHDL code you wrote for the complex counter
- Compilation report (Flow Summary) of your design
- Discussion on the resource utilization of your design (i.e. how many registers are used and why? What changes would you respect in the resource utilization if you increased the bit size of the counter?)
- Chip planner screenshot, with used resources highlighted
- RTL view of the circuit, with description of resources

Grading Sheet

Task	Grade	/Total	Comments
Creating Project		/10	
VHDL for counter		/50	
Resource Utilization		/20	
Floorplan & RTL		/20	